Rockchip
RK628D
Technical Reference Manual

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Revision 1.1
Aug. 2021

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Revision History

Date	Revision	Description
2021-08-10	1.1	Description update
2020-10-15	1.0	Initial Release

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Chapter 1 System Overview

1.1 Address Mapping

RK628D supports different interface protocols and features, in order to ensure the correct use of function, the address mapping relationship shown in the following figure below should be followed .Instructions of register configuration will be described in the chapter of each module.

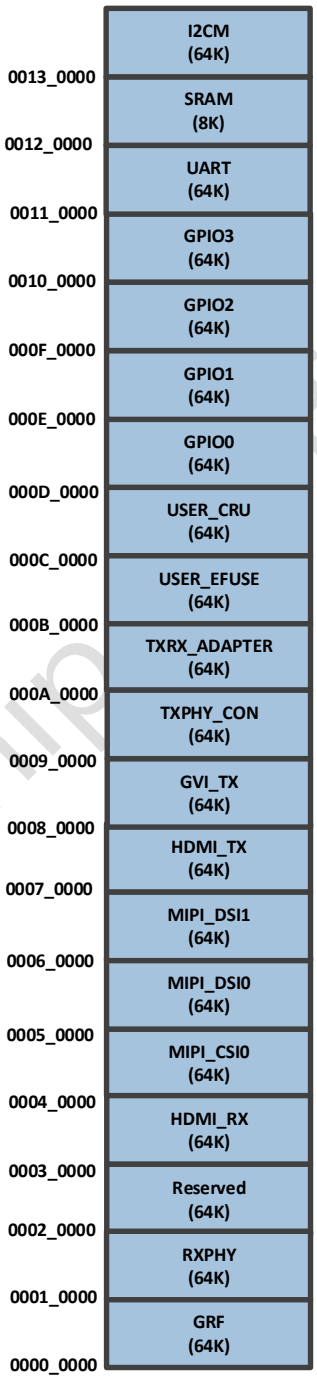

Fig. 1-1 RK628D Address Mapping

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Chapter 2 Clock and reset unit(CRU)

2.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets of chip. CRU generates system clock from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset.
CRU supports the following features:

- Compliance to the AMBA APB interface
- Embedded 2 PLLs: CPLL/GPLL
- Flexible selection of clock source
- Supports the respective gating of all clocks
- Supports the respective software reset of all modules

2.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

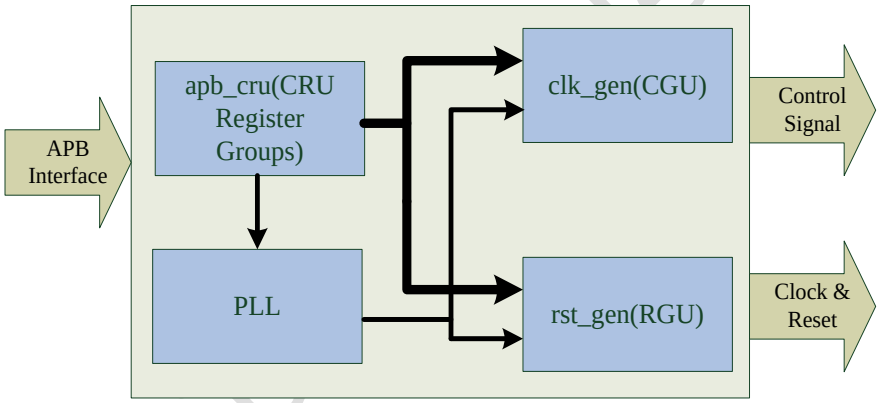

Fig. 2-1 CRU Architecture

2.3 System Clock Solution

The following diagrams show clock architecture (mux and divider information).

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	clk		parents (ID)											
MODULE	ID	CLKNAME	0	1	2	3	4	5	6	7	MUX	GATE	DIV	FRAC
SRC_CLK	0	xin_osc0_func<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	1	occ_scan_clk<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	2	clk_cpll_i	50	3	-	-	-	-	-	-	soc_scan_ls_mode	-	-	-
SRC_CLK	3	occ_scan_clk_cru<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	4	clk_gpll_i	52	3	-	-	-	-	-	-	soc_scan_ls_mode	-	-	-
SRC_CLK	5	clk_cpll_mux	0	2	-	-	-	-	-	-	GF_MODE0[0]{0}	-	-	-
SRC_CLK	6	clk_gpll_mux	0	4	-	-	-	-	-	-	GF_MODE0[2]{0}	-	-	-
SRC_CLK	7	xin_osc0_half	0	-	-	-	-	-	-	-	-	-	F2	-
SRC_CLK	8	i2s_mclkin<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	9	phy_hdrx_pclk<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	10	phy_hdrx_tmdsclk<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	11	phy_dsi_clkout1n<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	12	phy_dsi_clkout1<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	13	io_vop_dclk_in<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	14	phy_clk_txphy<IO>	-	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	50	clk_cpll	0	-	-	-	-	-	-	-	-	-	-	-
SRC_CLK	52	clk_gpll	0	-	-	-	-	-	-	-	-	-	-	-
pd_logic.i2s	100	clk_i2s_8ch_src	5	6	-	-	-	-	-	-	S3[13]{1}	G3[9]{0}	S3[12:8]{9}	-
pd_logic.i2s	101	clk_i2s_8ch_frac	100	-	-	-	-	-	-	-	-	G3[10]{0}	-	S4[31:0]{53826656}
pd_logic.i2s	102	mclk_i2s_8ch	100	101	8	7	-	-	-	-	S3[15:14]{0}	G3[11]{0}	-	-
pd_logic.gpio	200	pclk_gpio0	401	-	-	-	-	-	-	-	-	G1[0]{0}	-	-
pd_logic.gpio	201	pclk_gpio1	401	-	-	-	-	-	-	-	-	G1[1]{0}	-	-
pd_logic.gpio	202	pclk_gpio2	401	-	-	-	-	-	-	-	-	G1[2]{0}	-	-
pd_logic.gpio	203	pclk_gpio3	401	-	-	-	-	-	-	-	-	G1[3]{0}	-	-
pd_logic.gpio	204	clk_gpio_db0	0	-	-	-	-	-	-	-	-	G1[4]{0}	S8[9:0]{0}	-
pd_logic.gpio	205	clk_gpio_db1	0	-	-	-	-	-	-	-	-	G1[5]{0}	S9[9:0]{0}	-
pd_logic.gpio	206	clk_gpio_db2	0	-	-	-	-	-	-	-	-	G1[6]{0}	S10[9:0]{0}	-
pd_logic.gpio	207	clk_gpio_db3	0	-	-	-	-	-	-	-	-	G1[7]{0}	S11[9:0]{0}	-

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	clk		parents (ID)											
MODULE	ID	CLKNAME	0	1	2	3	4	5	6	7	MUX	GATE	DIV	FRAC
pd_logic.vo	300	clk_bt1120dec	5	6	-	-	-	-	-	-	S2[7]{0}	G0[12]{0}	S2[4:0]{7}	-
pd_logic.vo	301	clk_rx_read	5	6	-	-	-	-	-	-	S2[8]{0}	G0[11]{0}	-	S14[31:0]{65538}
pd_logic.vo	302	sclk_vop	5	6	-	-	-	-	-	-	S2[9]{0}	G0[13]{0}	-	S13[31:0]{65538}
pd_logic.vo	303	clk_hdmirx_aud	5	6	-	-	-	-	-	-	S5[15]{1}	G2[10]{0}	S5[13:6]{9}	-
pd_logic.vo	304	clk_imodet	5	6	-	-	-	-	-	-	S5[5]{0}	G2[11]{0}	S5[4:0]{23}	-
pd_logic.vo	305	clk_txesc	0	-	-	-	-	-	-	-	-	G2[12]{0}	-	-
pd_logic.vo	306	occ_scan_clk_txesc	1	-	-	-	-	-	-	-	-	-	-	-
pd_logic.vo	307	clk_txesc_func	305	306	-	-	-	-	-	-	soc_scan_mode	-	-	-
pd_logic.vo	308	clk_cfg_dphy0	0	-	-	-	-	-	-	-	-	G2[13]{0}	-	-
pd_logic.vo	309	clk_cfg_dphy1	0	-	-	-	-	-	-	-	-	G2[14]{0}	-	-
pd_logic.vo	310	clk_hdmirx_cec	0	-	-	-	-	-	-	-	-	G2[15]{0}	-	S12[31:0]{2645848}
pd_logic.vo	311	pclk_hdmirx	401	-	-	-	-	-	-	-	-	G2[2]{0}	-	-
pd_logic.vo	312	pclk_dsi0	401	-	-	-	-	-	-	-	-	G2[6]{0}	-	-
pd_logic.vo	313	pclk_dsi1	401	-	-	-	-	-	-	-	-	G2[7]{0}	-	-
pd_logic.vo	314	pclk_csi0	401	-	-	-	-	-	-	-	-	G2[8]{0}	-	-
pd_logic.vo	315	pclk_hdmitx	401	-	-	-	-	-	-	-	-	G2[4]{0}	-	-
pd_logic.vo	316	pclk_gvihost	401	-	-	-	-	-	-	-	-	G2[5]{0}	-	-
pd_logic.vo	317	pclk_rxphy	401	-	-	-	-	-	-	-	-	G2[0]{0}	-	-
pd_logic.vo	318	pclk_txphy_con	401	-	-	-	-	-	-	-	-	G2[3]{0}	-	-
pd_logic.plogic	401	pclk_logic	5	6	-	-	-	-	-	-	S0[7]{0}	G0[0]{0}	S0[4:0]{11}	-
pd_logic.plogic	402	pclk_cru	401	-	-	-	-	-	-	-	-	G0[1]{0}	-	-
pd_logic.plogic	403	pclk_regfile	401	-	-	-	-	-	-	-	-	G0[2]{0}	-	-
pd_logic.plogic	404	pclk_efuse	401	-	-	-	-	-	-	-	-	G0[5]{0}	-	-
pd_logic.plogic	405	pclk_adapter	401	-	-	-	-	-	-	-	-	G0[7]{0}	-	-
pd_logic.plogic	406	pclk_mcu_ram	401	-	-	-	-	-	-	-	-	G0[8]{0}	-	-
pd_logic.plogic	407	pclk_uart	401	-	-	-	-	-	-	-	-	G0[9]{0}	-	-
pd_logic.hlogic	500	hclk_logic	5	6	-	-	-	-	-	-	S0[15]{0}	G4[0]{0}	S0[13:8]{11}	-
pd_logic.hlogic	501	hclk_mcu_core	500	-	-	-	-	-	-	-	-	G4[1]{0}	-	-

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	clk		parents (ID)											
MODULE	ID	CLKNAME	0	1	2	3	4	5	6	7	MUX	GATE	DIV	FRAC
pd_logic.hlogic	502	hclk_mcu_rom	500	-	-	-	-	-	-	-	-	G4[2]{0}	-	-
pd_logic.hlogic	503	hclk_h2p	500	-	-	-	-	-	-	-	-	G4[3]{0}	-	-
pd_logic.hlogic	504	pclk_h2p	hclk_logic_ndft	-	-	-	-	-	-	-	-	G0[10]{0}	ICG_DFS10[15:11]{0}	-
pd_logic.hlogic	505	hclk_sfcxip	500	-	-	-	-	-	-	-	-	G4[4]{0}	-	-
pd_logic.hlogic	506	hclk_sfc	500	-	-	-	-	-	-	-	-	G4[5]{0}	-	-
pd_logic.hlogic	507	sclk_sfc	5	6	-	-	-	-	-	-	S7[15]{0}	G4[8]{0}	S7[7:0]{11}	-
pd_logic.hlogic	508	clk_mcu_core_rtc	0	-	-	-	-	-	-	-	-	G4[6]{0}	-	-
pd_logic.i2c	600	sclk_i2cm	5	6	-	-	-	-	-	-	S8[15]{0}	G4[10]{0}	S8[14:10]{11}	-
pd_logic.i2c	601	pclk_i2c2apb	401	-	-	-	-	-	-	-	-	G0[3]{0}	-	-
pd_logic.i2c	602	pclk_i2cm	401	-	-	-	-	-	-	-	-	G0[4]{0}	-	-
pd_logic.uart	700	clk_uart_src	5	6	-	-	-	-	-	-	S21[15]{1}	G4[12]{0}	S21[12:8]{9}	-
pd_logic.uart	701	clk_uart_frac	700	-	-	-	-	-	-	-	-	G4[11]{0}	-	S20[31:0]{65546}
pd_logic.uart	702	sclk_uart	700	701	0	-	-	-	-	-	S6[15:14]{0}	G4[9]{0}	-	-
pd_top.test	800	occ_scan_clk_hdrx_vid	5	6	-	-	-	-	-	-	S15[7]{0}	G5[3]{0}	S15[5:0]{3}	-
pd_top.test	801	clk_hdrx_vid_func	9	800	-	-	-	-	-	-	soc_scan_mode	-	-	-
pd_top.test	802	occ_scan_clk_hdrx_tmds	5	6	-	-	-	-	-	-	S15[15]{0}	G5[5]{0}	S15[12:8]{1}	-
pd_top.test	803	clk_hdrx_tmds_func	10	802	-	-	-	-	-	-	soc_scan_mode	-	-	-
pd_top.test	804	occ_scan_clk_dsi_clkout1n	5	-	-	-	-	-	-	-	-	G5[4]{0}	-	-
pd_top.test	805	clk_dsi_clkout1n_func	11	804	-	-	-	-	-	-	soc_scan_mode	-	-	-
pd_top.test	806	occ_scan_clk_dsi_clkout	5	-	-	-	-	-	-	-	-	G5[6]{0}	-	-
pd_top.test	807	clk_dsi_clkout_func	12	806	-	-	-	-	-	-	soc_scan_mode	-	-	-
pd_top.test	808	occ_scan_vop_dclk_in	5	6	-	-	-	-	-	-	S18[15]{0}	G5[1]{0}	S18[12:8]{7}	-
pd_top.test	809	clk_vop_dclk_in_func	13	808	-	-	-	-	-	-	soc_scan_mode	-	-	-
pd_top.test	810	occ_scan_clk_txphy	5	6	-	-	-	-	-	-	S17[7]{0}	G5[0]{0}	S17[4:0]{3}	-
pd_top.test	811	clk_txphy_func	14	810	-	-	-	-	-	-	soc_scan_mode	-	-	-
pd_top.test	812	occ_scan_clk_gpio	1	-	-	-	-	-	-	-	-	-	-	-
pd_top.test	813	occ_scan_clk_apb_cru	1	-	-	-	-	-	-	-	-	-	-	-

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	clk		parents (ID)											
MODULE	**ID**	**CLKNAME**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**MUX**	**GATE**	**DIV**	**FRAC**
pd_top.test	814	occ_scan_clk_clk_gen	1	-	-	-	-	-	-	-	-	-	-	-
pd_top.test	815	occ_scan_clk_rst_gen	1	-	-	-	-	-	-	-	-	-	-	-
pd_top.test	816	occ_scan_clk_mbist	1	-	-	-	-	-	-	-	-	-	-	-
pd_top.test	817	occ_scan_clk_func	1	-	-	-	-	-	-	-	-	-	-	-
pd_top.test	818	occ_scan_clk_cru	1	-	-	-	-	-	-	-	-	-	-	-
pd_top.test	819	occ_scan_clk_jtagtck	1	-	-	-	-	-	-	-	-	-	-	-
pd_top.test	820	occ_scan_clk_bt1120_delay_in	5	6	-	-	-	-	-	-	S17[15]{0}	G5[9]{0}	S17[12:8]{7}	-
pd_top.test	821	occ_scan_clk_sclk_vop_div2	5	6	-	-	-	-	-	-	S16[15]{0}	G5[7]{0}	S16[13:8]{3}	-
pd_top.test	822	occ_scan_clk_dsi_csi	5	-	-	-	-	-	-	-	-	G5[8]{0}	S21[5:0]{7}	-

Note:

DT_S/GF_S*/S**	*CRU_CLKSEL_CON**
*G**	*CRU_GATE_CON**
*GF_MODE**	*CRU_MODE_CON*
*GF_ * *ICG_ ** *F** *<IO>/{IO}*	*Glitch-free signals, if no register information means signal from block* *ICG DIV* *Fixed_div=** *Signal from IO*

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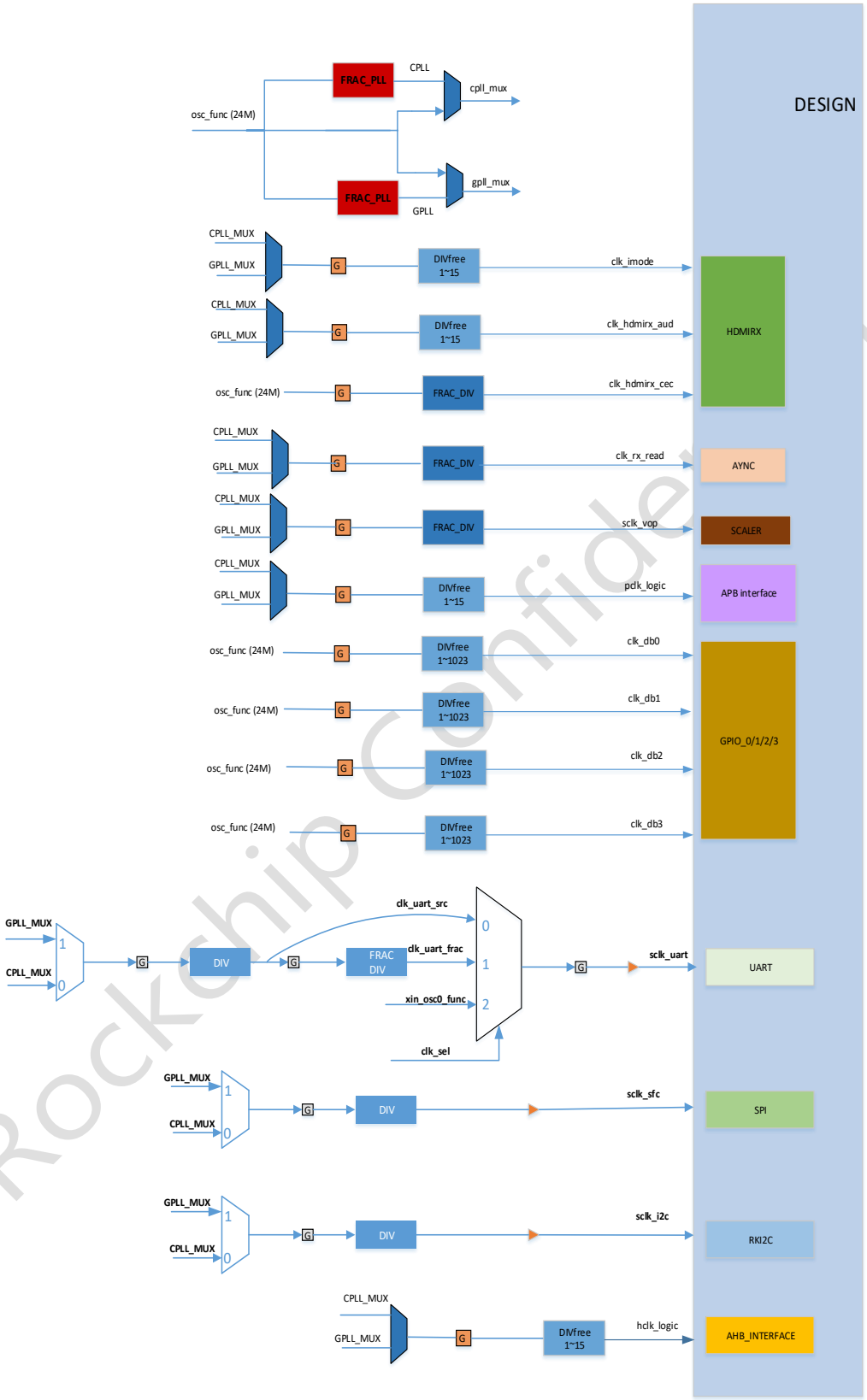

Fig. 2-2 Chip Clock Architecture Diagram

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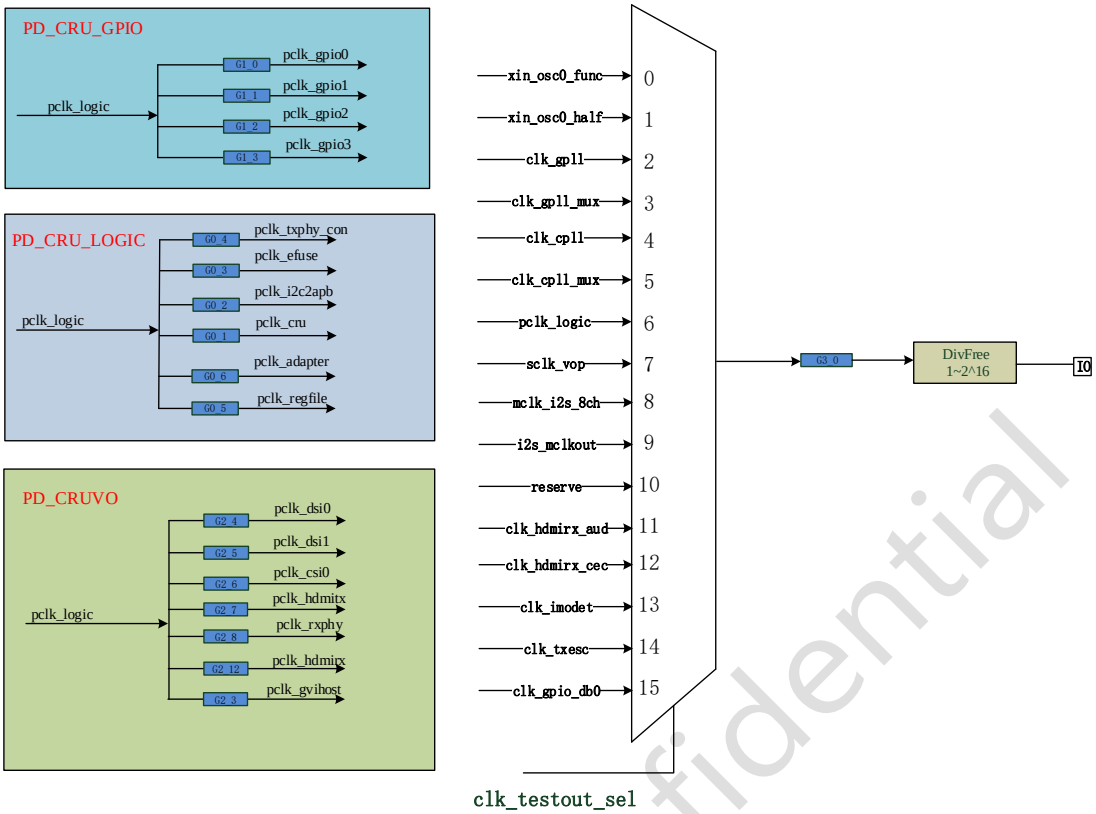

Fig. 2-3 Chip Clock Architecture Diagram

Description about input clock

The source of input clock in upper diagrams is listed as following Table.

Table 2-1 Input clock description in clock architecture diagram

Input Clock	Source	IO Name
xin_osc0_24m	External crystal oscillator (24MHz)	IO_OSCclkp/n

2.4 System Reset Solution

The following diagrams show reset architecture in This device.

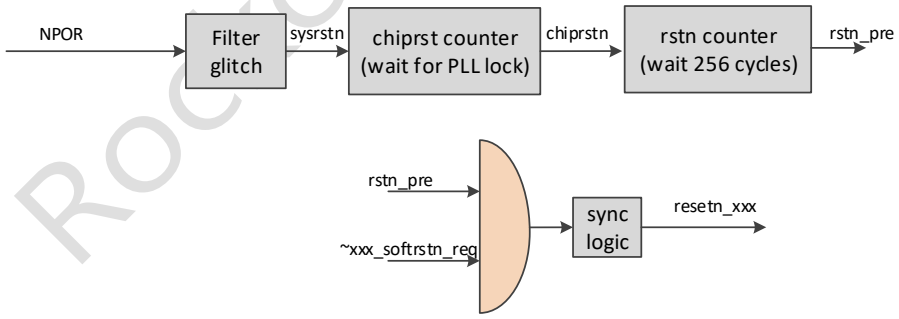

Fig. 2-4 Reset Architecture Diagram

Reset source of each reset signal includes:

- hardware reset(NPOR).
- software reset request(xxx_softrstn_req).

The 'xxx' of resetn_xxx and xxx_softrstn_req is the module name.

2.5 Function Description

There are two PLLs in RK628D: CPLL, GPLL. Both of them support only one crystal oscillator: 24MHz. Each PLL can only receive 24MHz oscillator.

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Those two PLLs all can be set to slow mode or deep slow mode, directly output selectable 24MHz. When power on or changing PLL setting, we must force PLL into slow mode to ensure output stable clock.
To maximize the flexibility, some of clocks can select divider source from multi PLLs.
To provide some **specific** frequency, another solution is integrated: fractional divider.
All clocks can be software gated and all reset can be software generated.

2.6 PLL Introduction

2.6.1 Overview

The chip uses 2.4GHz PLL for all four PLLs.The 2.4GHz PLL is a general purpose, high-performance PLL-based clock generator. The PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity,the PLL is ideal for use in noisy mixed signal SoC environments. By combining ultra-low jitter output clocks into a low power, low area, widely programmable design, Silicon Creations can greatly simplify an SoC by enabling a single macro to be used for all clocking applications in the system.
2.4GHz PLL supports the following features:

- Input Frequency Range:1MHz to 800MHz(Integer Mode) and 10MHz to 800MHz (Fractional Mode)
- Output Frequency Range: 12MHz to 2.4GHz
- 24 bit fractional accuracy, and fractional mode jitter performance to nearly match integer mode performance.
- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power.
- Isolated analog supply (2.5V) allows for excellent supply rejection in noisy SoC applications.
- Lock Detect Signal indicates when frequency lock has been achieved.

2.6.2 Block diagram

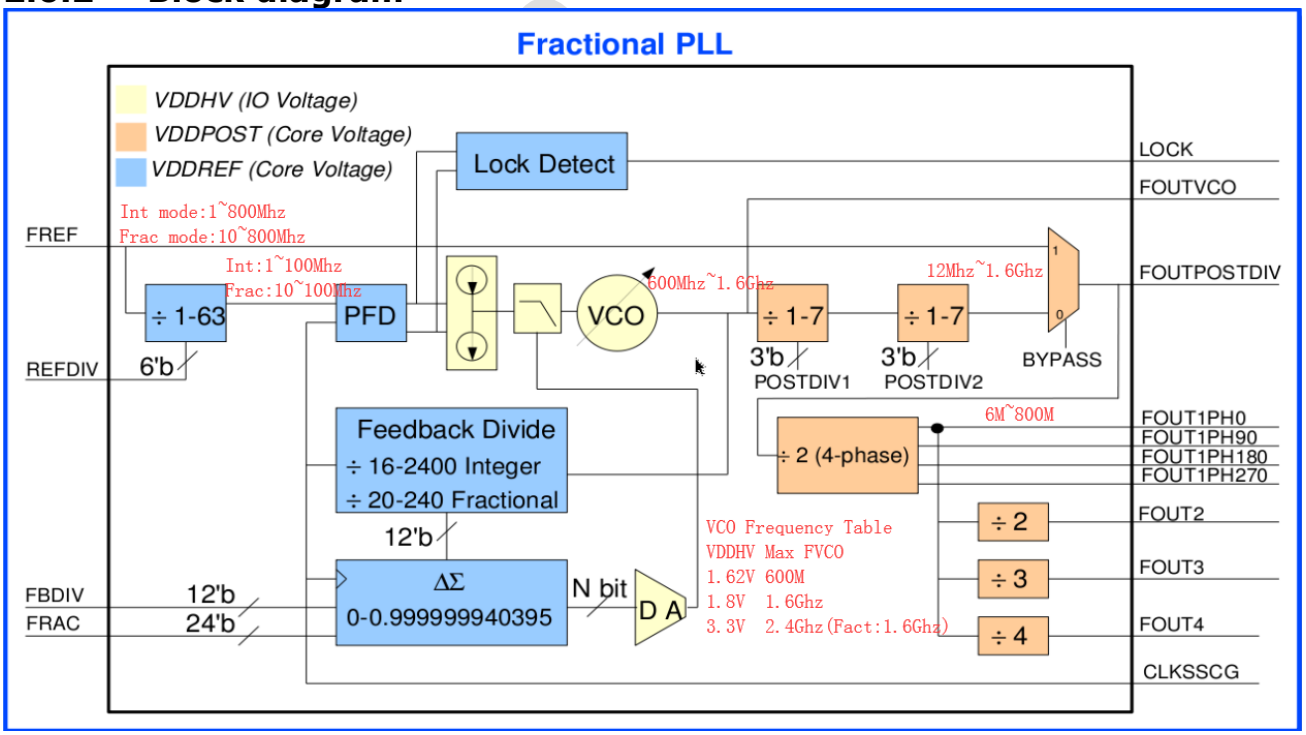

Fig. 2-5 CPLL/GPLL Block Diagram

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2.7 Register Description

2.7.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.7.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_CPLL_CON0	0x0000	W	0x00001063	CPLL configuration register0
CRU_CPLL_CON1	0x0004	W	0x00001042	CPLL configuration register1
CRU_CPLL_CON2	0x0008	W	0x00000000	CPLL configuration register2
CRU_CPLL_CON3	0x000C	W	0x00000007	CPLL configuration register3
CRU_CPLL_CON4	0x0010	W	0x00007F00	CPLL configuration register4
CRU_GPLL_CON0	0x0020	W	0x00001028	CPLL configuration register0
CRU_GPLL_CON1	0x0024	W	0x00000041	CPLL configuration register1
CRU_GPLL_CON2	0x0028	W	0x00F5C28F	CPLL configuration register2
CRU_GPLL_CON3	0x002C	W	0x00000007	CPLL configuration register3
CRU_GPLL_CON4	0x0030	W	0x00007F00	CPLL configuration register4
CRU_MODE_CON00	0x0060	W	0x00000000	Internal clock select and division register 0
CRU_CLKSEL_CON00	0x0080	W	0x00000B0B	Internal clock select and division register 0
CRU_CLKSEL_CON02	0x0088	W	0x00000007	Internal clock select and division register 2
CRU_CLKSEL_CON03	0x008C	W	0x00002980	Internal clock select and division register 3
CRU_CLKSEL_CON04	0x0090	W	0x03355460	Internal clock select and division register 4
CRU_CLKSEL_CON05	0x0094	W	0x00008257	Internal clock select and division register 5
CRU_CLKSEL_CON06	0x0098	W	0x00000004	Internal clock select and division register 6
CRU_CLKSEL_CON07	0x009C	W	0x0000000B	Internal clock select and division register 7
CRU_CLKSEL_CON08	0x00A0	W	0x00002C00	Internal clock select and division register 8
CRU_CLKSEL_CON09	0x00A4	W	0x00000000	Internal clock select and division register 9
CRU_CLKSEL_CON10	0x00A8	W	0x00000000	Internal clock select and division register 10
CRU_CLKSEL_CON11	0x00AC	W	0x00000000	Internal clock select and division register 11
CRU_CLKSEL_CON12	0x00B0	W	0x00285F58	Internal clock select and division register 12
CRU_CLKSEL_CON13	0x00B4	W	0x00010002	Internal clock select and division register 13
CRU_CLKSEL_CON14	0x00B8	W	0x00010002	Internal clock select and division register 14
CRU_CLKSEL_CON15	0x00BC	W	0x00000103	Internal clock select and division register 15
CRU_CLKSEL_CON16	0x00C0	W	0x00000300	Internal clock select and division register 16
CRU_CLKSEL_CON17	0x00C4	W	0x00000703	Internal clock select and division register 17

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON18	0x00C8	W	0x00000700	Internal clock select and division register 18
CRU_CLKSEL_CON20	0x00D0	W	0x0001000A	Internal clock select and division register 20
CRU_CLKSEL_CON21	0x00D4	W	0x00008907	Internal clock select and division register 21
CRU_GATE_CON00	0x0180	W	0x00000000	Internal clock gate and division register 0
CRU_GATE_CON01	0x0184	W	0x00000000	Internal clock gate and division register 1
CRU_GATE_CON02	0x0188	W	0x00000000	Internal clock gate and division register 2
CRU_GATE_CON03	0x018C	W	0x00000000	Internal clock gate and division register 3
CRU_GATE_CON04	0x0190	W	0x00000000	Internal clock gate and division register 4
CRU_GATE_CON05	0x0194	W	0x00000000	Internal clock gate and division register 5
CRU_SOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0
CRU_SOFTRST_CON01	0x0204	W	0x00000000	Internal clock reset register 1
CRU_SOFTRST_CON02	0x0208	W	0x00000000	Internal clock reset register 2
CRU_SOFTRST_CON04	0x0210	W	0x00000000	Internal clock reset register 4
CRU_GLB_CNT_TH	0x0300	W	0x00640064	Global reset counter threshold register
CRU_GLB_SRST_FST	0x0308	W	0x00000000	Global software first reset register
CRU_GLB_SRST_SND	0x030C	W	0x00000000	Global software second reset register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

2.7.3 Detail Register Description

CRU_CPLL_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV. 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x063	fbdiv Feedback Divide Value, valid divider settings. [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_CPLL_CON1

Address: Operational Base + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection. If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise PLL is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request. 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request. 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable. 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RO	0x0	pll_lock PLL lock status. 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x02	refdiv Reference Clock Divide Value, (1-63)

CRU_CPLL_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks. 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock. 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock. 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC. 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback division register. (fraction = FRAC/2^24)

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CRU_CPLL_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	WO	0x00	ssmod_spread Spread amplitude. % = 0.1 * SPREAD[4: 0]
7:4	WO	0x0	ssmod_divval Divider required to set the modulation frequency
3	WO	0x0	ssmod_downspread Selects center spread or down spread. 1'b0: Down spread 1'b1: Center spread
2	WO	0x1	ssmod_reset Reset modulator state. 1'b0: No reset 1'b1: Reset
1	WO	0x1	ssmod_disable_sscg Bypass SSMOD by module. 1'b0: No bypass 1'b1: Bypass
0	WO	0x1	ssmod_bp Bypass SSMOD by integration. 1'b0: No bypass 1'b1: Bypass

CRU_CPLL_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	WO	0x7f	ssmod_ext_maxaddr External wave table data inputs. (0-255)
7:1	RO	0x00	reserved
0	WO	0x0	ssmod_sel_ext_wave Select external wave. 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_GPLL_CON0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV. 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x028	fbdiv Feedback Divide Value, valid divider settings. [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_GPLL_CON1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection. If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise PLL is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request. 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request. 1'b0: No power down 1'b1: Power down
12	RW	0x0	dsmpd PLL delta sigma modulator enable. 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RO	0x0	pll_lock PLL lock status. 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

CRU_GPLL_CON2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks. 1'b0: No power down 1'b1: Power down

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Bit	Attr	Reset Value	Description
26	RW	0x0	foutvcopd Power down buffered VCO clock. 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock. 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC. 1'b0: No power down 1'b1: Power down
23:0	RW	0xf5c28f	fracdiv Fractional part of feedback division register. (fraction = FRAC/2^24)

CRU_GPLL_CON3

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	WO	0x00	ssmod_spread Spread amplitude. % = 0.1 * SPREAD[4: 0]
7:4	WO	0x0	ssmod_divval Divider required to set the modulation frequency
3	WO	0x0	ssmod_downspread Selects center spread or down spread. 1'b0: Down spread 1'b1: Center spread
2	WO	0x1	ssmod_reset Reset modulator state. 1'b0: No reset 1'b1: Reset
1	WO	0x1	ssmod_disable_sscg Bypass SSMOD by module. 1'b0: No bypass 1'b1: Bypass
0	WO	0x1	ssmod_bp Bypass SSMOD by integration. 1'b0: No bypass 1'b1: Bypass

CRU_GPLL_CON4

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:8	WO	0x7f	ssmod_ext_maxaddr External wave table data inputs. (0-255)
7:1	RO	0x00	reserved
0	WO	0x0	ssmod_sel_ext_wave Select external wave. 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_MODE_CON00

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	clk_gpll_mode clk_gpll_mux clock mux. 1'b0: xin_osc0_func 1'b1: clk_gpll
1	RO	0x0	reserved
0	RW	0x0	clk_cpll_mode clk_cpll_mux clock mux. 1'b0: xin_osc0_func 1'b1: clk_cpll

CRU_CLKSEL_CON00

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_logic_sel hclk_logic clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14	RO	0x0	reserved
13:8	RW	0x0b	hclk_logic_div Divide hclk_logic by (div_con + 1)
7	RW	0x0	pclk_logic_sel pclk_logic clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
6:5	RO	0x0	reserved
4:0	RW	0x0b	pclk_logic_div Divide pclk_logic by (div_con + 1)

CRU_CLKSEL_CON02

Address: Operational Base + offset (0x0088)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	sclk_vop_sel sclk_vop clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
8	RW	0x0	clk_rx_read_sel clk_rx_read clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
7	RW	0x0	clk_bt1120dec_sel clk_bt1120dec clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
6:5	RO	0x0	reserved
4:0	RW	0x07	clk_bt1120dec_div Divide clk_bt1120dec by (div_con + 1)

CRU_CLKSEL_CON03

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	mclk_i2s_8ch_sel mclk_i2s_8ch clock mux. 2'b00: clk_i2s_8ch_src 2'b01: clk_i2s_8ch_frac 2'b10: i2s_mclkin 2'b11: xin_osc0_half
13	RW	0x1	clk_i2s_8ch_src_sel clk_i2s_8ch_src clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
12:8	RW	0x09	clk_i2s_8ch_src_div Divide clk_i2s_8ch_src by (div_con + 1)
7	RW	0x1	i2s_mclkout_sel i2s_mclkout clock mux. 1'b0: mclk_i2s_8ch 1'b1: xin_osc0_half
6:0	RO	0x00	reserved

CRU_CLKSEL_CON04

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x03355460	clk_i2s_8ch_frac_div clk_i2s_8ch_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON05

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Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_hdmirx_aud_sel clk_hdmirx_aud clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14	RO	0x0	reserved
13:6	RW	0x09	clk_hdmirx_aud_div Divide clk_hdmirx_aud by (div_con + 1)
5	RW	0x0	clk_imodet_sel clk_imodet clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
4:0	RW	0x17	clk_imodet_div Divide clk_imodet by (div_con + 1)

CRU_CLKSEL_CON06

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	sclk_uart_sel sclk_uart clock mux. 2'b00: clk_uart_src 2'b01: clk_uart_frac 2'b10: xin_osc0_func
13:8	RW	0x00	clk_testout_div Divide clk_testout by (div_con + 1)
7:4	RO	0x0	reserved
3:0	RW	0x4	clk_testout_sel clk_testout clock mux. 4'b0000: xin_osc0_func 4'b0001: xin_osc0_half 4'b0010: clk_gpll 4'b0011: clk_gpll_mux 4'b0100: clk_cpll 4'b0101: clk_cpll_mux 4'b0110: pclk_logic 4'b0111: sclk_vop 4'b1000: mclk_i2s_8ch 4'b1001: i2s_mclkout 4'b1010: creserve 4'b1011: clk_hdmirx_aud 4'b1100: clk_hdmirx_cec 4'b1101: clk_imodet 4'b1110: clk_txesc 4'b1111: clk_gpio_db0

CRU_CLKSEL_CON07

Address: Operational Base + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sclk_sfc_sel sclk_sfc clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14:8	RO	0x00	reserved
7:0	RW	0x0b	sclk_sfc_div Divide sclk_sfc by (div_con + 1)

CRU_CLKSEL_CON08

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sclk_i2cm_sel sclk_i2cm clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14:10	RW	0x0b	sclk_i2cm_div Divide sclk_i2cm by (div_con + 1)
9:0	RW	0x000	clk_gpio_db0_div Divide clk_gpio_db0 by (div_con + 1)

CRU_CLKSEL_CON09

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	clk_gpio_db1_div Divide clk_gpio_db1 by (div_con + 1)

CRU_CLKSEL_CON10

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x00	pclk_h2p_div Divide pclk_h2p by (div_con + 1)
10	RO	0x0	reserved
9:0	RW	0x000	clk_gpio_db2_div Divide clk_gpio_db2 by (div_con + 1)

CRU_CLKSEL_CON11

Address: Operational Base + offset (0x00AC)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	clk_gpio_db3_div Divide clk_gpio_db3 by (div_con + 1)

CRU_CLKSEL_CON12

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00285f58	clk_hdmirx_cec_div clk_hdmirx_cec fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON13

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010002	sclk_vop_div sclk_vop fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON14

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010002	clk_rx_read_div clk_rx_read fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON15

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	occ_scan_clk_hdrx_tmds_sel occ_scan_clk_hdrx_tmds clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14:13	RO	0x0	reserved
12:8	RW	0x01	occ_scan_clk_hdrx_tmds_div Divide occ_scan_clk_hdrx_tmds by (div_con + 1)
7	RW	0x0	occ_scan_clk_hdrx_vid_sel occ_scan_clk_hdrx_vid clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
6	RO	0x0	reserved
5:0	RW	0x03	occ_scan_clk_hdrx_vid_div Divide occ_scan_clk_hdrx_vid by (div_con + 1)

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CRU_CLKSEL_CON16
Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	occ_scan_clk_sclk_vop_div2_sel occ_scan_clk_sclk_vop_div2 clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14	RO	0x0	reserved
13:8	RW	0x03	occ_scan_clk_sclk_vop_div2_div Divide occ_scan_clk_sclk_vop_div2 by (div_con + 1)
7:0	RO	0x00	reserved

CRU_CLKSEL_CON17
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	occ_scan_clk_bt1120_delay_in_sel occ_scan_clk_bt1120_delay_in clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14:13	RO	0x0	reserved
12:8	RW	0x07	occ_scan_clk_bt1120_delay_in_div Divide occ_scan_clk_bt1120_delay_in by (div_con + 1)
7	RW	0x0	occ_scan_clk_txphy_sel occ_scan_clk_txphy clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
6:5	RO	0x0	reserved
4:0	RW	0x03	occ_scan_clk_txphy_div Divide occ_scan_clk_txphy by (div_con + 1)

CRU_CLKSEL_CON18
Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	occ_scan_vop_dclk_in_sel occ_scan_vop_dclk_in clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14:13	RO	0x0	reserved
12:8	RW	0x07	occ_scan_vop_dclk_in_div Divide occ_scan_vop_dclk_in by (div_con + 1)
7:0	RO	0x00	reserved

CRU_CLKSEL_CON20
Address: Operational Base + offset (0x00D0)

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Bit	Attr	Reset Value	Description
31:0	RW	0x0001000a	clk_uart_frac_div clk_uart_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON21

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_uart_src_sel clk_uart_src clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
14:13	RO	0x0	reserved
12:8	RW	0x09	clk_uart_src_div Divide clk_uart_src by (div_con + 1)
7:6	RO	0x0	reserved
5:0	RW	0x07	occ_scan_clk_dsi_csi_div Divide occ_scan_clk_dsi_csi by (div_con + 1)

CRU_GATE_CON00

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	sclk_vop_en sclk_vop clock gating control. When high, disable clock
12	RW	0x0	clk_bt1120dec_en clk_bt1120dec clock gating control. When high, disable clock
11	RW	0x0	clk_rx_read_en clk_rx_read clock gating control. When high, disable clock
10	RW	0x0	pclk_h2p_en pclk_h2p clock gating control. When high, disable clock
9	RW	0x0	pclk_uart_en pclk_uart clock gating control. When high, disable clock
8	RW	0x0	pclk_mcu_ram_en pclk_mcu_ram clock gating control. When high, disable clock
7	RW	0x0	pclk_adapter_en pclk_adapter clock gating control. When high, disable clock
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	pclk_efuse_en pclk_efuse clock gating control. When high, disable clock
4	RW	0x0	pclk_i2cm_en pclk_i2cm clock gating control. When high, disable clock
3	RW	0x0	pclk_i2c2apb_en pclk_i2c2apb clock gating control. When high, disable clock
2	RW	0x0	pclk_regfile_en pclk_regfile clock gating control. When high, disable clock
1	RW	0x0	pclk_cru_en pclk_cru clock gating control. When high, disable clock
0	RW	0x0	pclk_logic_en pclk_logic clock gating control. When high, disable clock

CRU_GATE_CON01

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_gpio_db3_en clk_gpio_db3 clock gating control. When high, disable clock
6	RW	0x0	clk_gpio_db2_en clk_gpio_db2 clock gating control. When high, disable clock
5	RW	0x0	clk_gpio_db1_en clk_gpio_db1 clock gating control. When high, disable clock
4	RW	0x0	clk_gpio_db0_en clk_gpio_db0 clock gating control. When high, disable clock
3	RW	0x0	pclk_gpio3_en pclk_gpio3 clock gating control. When high, disable clock
2	RW	0x0	pclk_gpio2_en pclk_gpio2 clock gating control. When high, disable clock
1	RW	0x0	pclk_gpio1_en pclk_gpio1 clock gating control. When high, disable clock
0	RW	0x0	pclk_gpio0_en pclk_gpio0 clock gating control. When high, disable clock

CRU_GATE_CON02

Address: Operational Base + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_hdmirx_cec_en clk_hdmirx_cec clock gating control. When high, disable clock
14	RW	0x0	clk_cfg_dphy1_en clk_cfg_dphy1 clock gating control. When high, disable clock
13	RW	0x0	clk_cfg_dphy0_en clk_cfg_dphy0 clock gating control. When high, disable clock
12	RW	0x0	clk_txesc_en clk_txesc clock gating control. When high, disable clock
11	RW	0x0	clk_imodet_en clk_imodet clock gating control. When high, disable clock
10	RW	0x0	clk_hdmirx_aud_en clk_hdmirx_aud clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	pclk_csi0_en pclk_csi0 clock gating control. When high, disable clock
7	RW	0x0	pclk_dsi1_en pclk_dsi1 clock gating control. When high, disable clock
6	RW	0x0	pclk_dsi0_en pclk_dsi0 clock gating control. When high, disable clock
5	RW	0x0	pclk_gvihost_en pclk_gvihost clock gating control. When high, disable clock
4	RW	0x0	pclk_hdmitx_en pclk_hdmitx clock gating control. When high, disable clock
3	RW	0x0	pclk_txphy_con_en pclk_txphy_con clock gating control. When high, disable clock
2	RW	0x0	pclk_hdmirx_en pclk_hdmirx clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	pclk_rxphy_en pclk_rxphy clock gating control. When high, disable clock

CRU_GATE_CON03

Address: Operational Base + offset (0x018C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	i2s_mclkout_en i2s_mclkout clock gating control. When high, disable clock
11	RW	0x0	mclk_i2s_8ch_en mclk_i2s_8ch clock gating control. When high, disable clock
10	RW	0x0	clk_i2s_8ch_frac_en clk_i2s_8ch_frac clock gating control. When high, disable clock
9	RW	0x0	clk_i2s_8ch_en clk_i2s_8ch_src clock gating control. When high, disable clock
8:0	RO	0x000	reserved

CRU_GATE_CON04

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_uart0_en clk_uart_src clock gating control. When high, disable clock
11	RW	0x0	clk_uart0_frac_en clk_uart_frac clock gating control. When high, disable clock
10	RW	0x0	sclk_i2cm sclk_i2cm clock gating control. When high, disable clock
9	RW	0x0	sclk_uart_en sclk_uart clock gating control. When high, disable clock
8	RW	0x0	sclk_sfc_en sclk_sfc clock gating control. When high, disable clock
7	RW	0x0	clk_testout_en clk_testout clock gating control. When high, disable clock
6	RW	0x0	clk_mcu_core_rtc_en clk_mcu_core_rtc clock gating control. When high, disable clock
5	RW	0x0	hclk_sfc_en hclk_sfc clock gating control. When high, disable clock
4	RW	0x0	hclk_sfcxip_en hclk_sfcxip clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_h2p_en hclk_h2p clock gating control. When high, disable clock
2	RW	0x0	hclk_mcu_rom_en hclk_mcu_rom clock gating control. When high, disable clock
1	RW	0x0	hclk_mcu_core_en hclk_mcu_core clock gating control. When high, disable clock
0	RW	0x0	hclk_logic_en hclk_logic clock gating control. When high, disable clock

CRU_GATE_CON05

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	occ_scan_clk_bt1120_delay_in_en occ_scan_clk_bt1120_delay_in clock gating control. When high, disable clock
8	RW	0x0	occ_scan_clk_dsi_csi_en occ_scan_clk_dsi_csi clock gating control. When high, disable clock
7	RW	0x0	occ_scan_clk_sclk_vop_div2_en occ_scan_clk_sclk_vop_div2 clock gating control. When high, disable clock
6	RW	0x0	occ_scan_clk_dsi_clkout_en occ_scan_clk_dsi_clkout clock gating control. When high, disable clock
5	RW	0x0	occ_scan_clk_hdrx_tmds_en occ_scan_clk_hdrx_tmds clock gating control. When high, disable clock
4	RW	0x0	occ_scan_clk_dsi_clkout1n_en occ_scan_clk_dsi_clkout1n clock gating control. When high, disable clock
3	RW	0x0	occ_scan_clk_hdrx_vid_en occ_scan_clk_hdrx_vid clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	occ_scan_vop_dclk_in_en occ_scan_vop_dclk_in clock gating control. When high, disable clock
0	RW	0x0	occ_scan_clk_txphy_en occ_scan_clk_txphy clock gating control. When high, disable clock

CRU_SOFTRST_CON00

Address: Operational Base + offset (0x0200)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	sresetn_vop When high, reset relative logic
12	RW	0x0	resetn_bt1120dec When high, reset relative logic
11	RW	0x0	resetn_clk_rx When high, reset relative logic
10	RW	0x0	presetn_h2p When high, reset relative logic
9	RW	0x0	presetn_uart When high, reset relative logic
8	RW	0x0	presetn_mcu_ram When high, reset relative logic
7	RW	0x0	presetn_adapter When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	presetn_efuse When high, reset relative logic
4	RW	0x0	presetn_i2cm When high, reset relative logic
3	RW	0x0	presetn_i2c2apb When high, reset relative logic
2	RW	0x0	presetn_regfile When high, reset relative logic
1	RW	0x0	presetn_cru When high, reset relative logic
0	RW	0x0	presetn_logic When high, reset relative logic

CRU_SOFTRST_CON01

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	resetn_gpio_db3 When high, reset relative logic
6	RW	0x0	resetn_gpio_db2 When high, reset relative logic
5	RW	0x0	resetn_gpio_db1 When high, reset relative logic
4	RW	0x0	resetn_gpio_db0 When high, reset relative logic
3	RW	0x0	presetn_gpio3 When high, reset relative logic
2	RW	0x0	presetn_gpio2 When high, reset relative logic

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Bit	Attr	Reset Value	Description
1	RW	0x0	presetn_gpio1 When high, reset relative logic
0	RW	0x0	presetn_gpio0 When high, reset relative logic

CRU_SOFTRST_CON02

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	resetn_txesc When high, reset relative logic
13	RW	0x0	resetn_txbtyehs When high, reset relative logic
12	RW	0x0	resetn_hdmirx_pon When high, reset relative logic
11	RW	0x0	resetn_encoder When high, reset relative logic
10	RW	0x0	resetn_decoder When high, reset relative logic
9	RW	0x0	resetn_txdata When high, reset relative logic
8	RW	0x0	presetn_csi0 When high, reset relative logic
7	RW	0x0	presetn_dsi1 When high, reset relative logic
6	RW	0x0	presetn_dsi0 When high, reset relative logic
5	RW	0x0	presetn_gvihost When high, reset relative logic
4	RW	0x0	presetn_hdmitx When high, reset relative logic
3	RW	0x0	presetn_txphy_con When high, reset relative logic
2	RW	0x0	presetn_hdmirx When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	presetn_rxphy When high, reset relative logic

CRU_SOFTRST_CON04

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	sresetn_i2cm When high, reset relative logic

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Bit	Attr	Reset Value	Description
9	RW	0x0	sresetn_uart When high, reset relative logic
8	RW	0x0	sresetn_sfc When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	hresetn_sfc When high, reset relative logic
4	RW	0x0	hresetn_sfcxip When high, reset relative logic
3	RW	0x0	hresetn_h2p When high, reset relative logic
2	RW	0x0	hresetn_mcu_rom When high, reset relative logic
1	RW	0x0	hresetn_mcu_core When high, reset relative logic
0	RO	0x0	reserved

CRU_GLB_CNT_TH

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:0	RW	0x00640064	global_reset_counter_threshold Global soft reset, wdt reset or tsadc_shut reset asserted time counter threshold. Measured in OSC clock cycles

CRU_GLB_SRST_FST

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srst_fst_value The first global software reset configuration value, write 0xfdb9 to reset

CRU_GLB_SRST_SND

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srst_second_value The second global software reset configuration value, write 0xeca8 to reset

2.8 Timing Diagram

Power on reset timing is shown as follow:

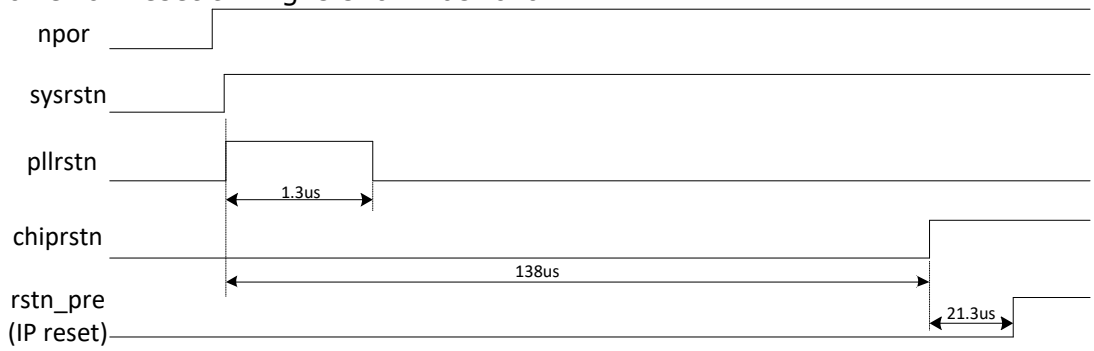

Fig. 2-6 Chip Power On Reset Timing Diagram

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NPOR is hardware reset signal from out-chip, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the PLL reset signal (pllrstn) must maintain high for more than 1us, and PLLs start to lock when pllrstn deassert, and the PLL max lock time is 1500 PLL REFCLK cycles. And then the system will wait about 138us, and then deactive reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 512cycles (21.3us) to deactive signal rstn_pre, which is used to generate power on reset of all IP.

2.9 Application Notes

2.9.1 PLL usage

The chip uses 2.4GHz for all four PLLs (CPLL, GPLL).

A. CPLL output frequency configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_CPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_CPLL_CON1.
FRAC can be configured by programming CRU_CPLL_CON2.

If DSMPD = 1 (DSM is disabled, "integer mode")
FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 700MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 175
POSTDIV1=1
POSTDIV2=1

And then
FOUTVCO = (FREF / REFDIV) * FBDIV = 24/6*175=700
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=700/1/1=700

If DSMPD = 0 (DSM is enabled, "fractional mode")
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24))
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 491.52MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 0
REFDIV = 1
FBDIV = 40
FRAC = 24’hf5c28f
POSTDIV1=2
POSTDIV2=1

And then
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24)) = 983.04
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=983.04/(2*1)=491.52

B. GPLL output frequency configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_GPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_GPLL_CON1.

FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 700MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 175
POSTDIV1=1
POSTDIV2=1

And then

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FOUTVCO = (FREF / REFDIV) * FBDIV = 24/6*175=700
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=700/1/1=700

C. PLL setting consideration

- If the POSTDIV value is changed during operation a short pulse (glitch) may occur on FOUTPOSTDIV. The minimum width of the short pulse will be equal to twice the period of the VCO. Therefore, if the circuitry clocked by the PLL is sensitive to short pulses, the new divide value should be re-timed so that it is synchronous with the rising edge of the output clock (FOUTPOSTDIV). Glitches cannot occur on any of the other outputs.
- For lowest power operation, the minimum VCO and FREF frequencies should be used. For minimum jitter operation, the highest VCO and FREF frequencies should be used. The normal operating range for the VCO is described above in .
- The supply rejection will be worse at the low end of the VCO range so care should be taken to keep the supply clean for low power applications.
- The feedback divider is not capable of dividing by all possible settings due to the use of a power-saving architecture. The following settings are valid for FBDIV:
  - DSMPD=1 (Integer Mode):
    12,13,14,16-4095 (practical value is limited to 3200, 2400, or 1600 (FVCOMAX / FREFMIN))
  - DSMPD=0 (Fractional Mode):
    19-4091 (practical value is limited to 320, 240, or 160 (FVCOMAX / FREFMIN))
- The PD input places the PLL into the lowest power mode. In this case, all analog circuits are turned off and FREF will be "ignored". The FOUTPOSTDIV and FOUTVCO pins are forced to logic low (0V).
- The BYPASS pin controls a mux which selects FREF to be passed to the FOUTPOSTDIV when active high. However, the PLL continues to run as it normally would if bypass were low. This is a useful feature for PLL testing since the clock path can be verified without the PLL being required to work. Also, the effect that the PLL induced supply noise has on the output buffering can be evaluated. It is not recommended to switch between BYPASS mode and normal mode for regular chip operation since this may result in a glitch. Also, FOUTPOSTDIVPD should be set low if the PLL is to be used in BYPASS mode.

2.9.2 PLL frequency change and lock check

The PLL programming supports changed on-the-fly and the PLL will simply slew to the new frequency.
PLL lock state can be checked in CRU_CPLL_CON1[10], CRU_GPLL_CON1[10], register. The lock state is high when both original hardware PLL lock and PLL counter lock are high. The PLL counter lock initial value is CRU_GLB_CNT_TH[31:16].
The max delay time is 1500*REFDIV/FREF.
PLL locking consists of three phases.

- Phase 1 is control voltage slewing. During this phase one of the clocks (reference or divide) is much faster than the other, and the PLL frequency adjusts almost continuously. When locking from power down, the divide clock is initially very slow and steadily increases frequency. It will take slightly longer for faster VCO settings when locking from power down, since the PLL must slew further.
- Phase 2 is small signal phase acquisition. During this phase, the internal up/down signals alternate semi-chaotically as the phase slowly adjusts until the two signals are aligned. The duration of this phase depends on the loop bandwidth and is faster with higher bandwidth. Bandwidth can be estimated as FREF / REFDIV / 20 for integer mode and FREF /REFDIV / 40 for fractional mode. The duration of small signal locking is about 1/Bandwidth.
- Phase 3 is the digital cycle count. After the last cycle slip is detected, an internal counter waits 256 FREF / REFDIV cycles before the lock signal goes high. This is frequently the dominant factor in lock time – especially for slower reference clock signals or large reference divide settings. This time can be calculated as 256*REFDIV/FREF.

2.9.3 Fractional divider usage

To get specific frequency, clocks of I2S and HDMIRX_CEC，can be generated by fractional divider. Generally you must set that denominator is 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low

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frequency clock like I2S, HDMIRX_CEC,GPIO_DB.

Table 2-2 Source Clock Limitation of Fractional Divider

Clock Name	Fractional divider source clock Limit
i2s_mclkout	983.04MHz
clk_hdmirx_aud	983.04MHz
clk_hdmirx_cec	24MHz
clk_gpio_db0/1/2/3	24MHz
clk_txesc	24MHz
clk_cfg_dphy0/1	24MHz

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Chapter 3 General Register File(GRF)

3.1 Overview

The general register file will be used to do static set by software, which is composed of many registers for system control.

3.2 Features

The function of general register file is:

- IOMUX control
- Control the state of GPIO in power-down mode
- GPIO PAD pull down and pull up control
- Used for common system control
- Used to record the system state

3.3 Register Description

3.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

3.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_SYSTEM_CON0	0x0000	W	0x0000060B	System ctrl register0
GRF_SYSTEM_CON1	0x0004	W	0x00000000	System ctrl register1
GRF_SYSTEM_CON2	0x0008	W	0x00000000	System ctrl register2
GRF_SYSTEM_CON3	0x000C	W	0x00000100	System ctrl register3
GRF_SCALER_CON0	0x0010	W	0x00000000	Scaler ctrl register
GRF_SCALER_CON1	0x0014	W	0x00000000	Scaler horizontal/vertical factor register
GRF_SCALER_CON2	0x0018	W	0x00000000	Scaler output scanning start setting register
GRF_SCALER_CON3	0x001C	W	0x00000000	Scaler output scanning horizontal timing
GRF_SCALER_CON4	0x0020	W	0x00000000	Scaler output horizontal active window
GRF_SCALER_CON5	0x0024	W	0x00000000	Scaler output scanning vertical timing
GRF_SCALER_CON6	0x0028	W	0x00000000	Scaler output vertical active window
GRF_SCALER_CON7	0x002C	W	0x00000000	Scaler output horizontal border window
GRF_SCALER_CON8	0x0030	W	0x00000000	Scaler output vertical border window
GRF_POST_PROC_CON	0x0034	W	0x00000000	Post process ctrl register
GRF_CSC_CTRL_CON	0x0038	W	0x00000000	CSC(color space convert) control register
GRF_LVDS_TX_CON	0x003C	W	0x00000000	LVDS ctrl register
GRF_RGB_DEC_CON0	0x0040	W	0x00000000	RGB/BT1120/YUV decoder control register0
GRF_RGB_DEC_CON1	0x0044	W	0x00000000	RGB/BT1120/YUV decoder control register1
GRF_RGB_DEC_CON2	0x0048	W	0x00000000	RGB/BT1120/YUV decoder control register2

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Name	Offset	Size	Reset Value	Description
GRF_RGB_ENC_CON	0x004C	W	0x00000000	RGB/BT1120/YUV encoder ctrl register
GRF_MIPI_LANE_DELAY_CON0	0x0050	W	0x00000000	MIPI lane delay count register, LSB32
GRF_MIPI_LANE_DELAY_CON1	0x0054	W	0x00000000	MIPI lane delay count register,MSB32
GRF_BT1120_DCLK_DELAY_CON0	0x0058	W	0x00000000	BT1120 dclk delay line count register, LSB32
GRF_BT1120_DCLK_DELAY_CON1	0x005C	W	0x00000000	BT1120 dclk delay line count register, LSB32
GRF_MIPI_TX0_CON	0x0060	W	0x00000000	MIPI dsi0 control register
GRF_DPHY0_STATUS	0x0064	W	0x00000000	MIPI dphy0 status
GRF_MIPI_TX1_CON	0x0068	W	0x00000000	MIPI dsi1 control register
GRF_DPHY1_STATUS	0x006C	W	0x00000000	MIPI dphy1 status
GRF_GPIO0AB_SEL_CON	0x0070	W	0x00000000	GPIO0A,GPIO0B iomux control
GRF_GPIO1AB_SEL_CON	0x0074	W	0x00005000	GPIO1A,GPIO1B iomux control
GRF_GPIO2AB_SEL_CON	0x0078	W	0x00000000	GPIO2A,GPIO2B iomux control
GRF_GPIO2C_SEL_CON	0x007C	W	0x0000AA80	GPIO2C iomux control
GRF_GPIO3AB_SEL_CON	0x0080	W	0x00001000	GPIO3A,GPIO3B iomux control
GRF_GPIO2A_SMT	0x0090	W	0x00000000	GPIO2A schmitt control
GRF_GPIO2B_SMT	0x0094	W	0x00000000	GPIO2B schmitt control
GRF_GPIO2C_SMT	0x0098	W	0x00000000	GPIO2C schmitt control
GRF_GPIO3AB_SMT	0x009C	W	0x00000000	GPIO3A GPIO3B smitter control
GRF_GPIO0A_P_CON	0x00A0	W	0x0000AA8A	GPIO0A PU/PD control
GRF_GPIO1A_P_CON	0x00A4	W	0x0000AA8A	GPIO1A PU/PD control
GRF_GPIO2A_P_CON	0x00A8	W	0x0000AAAA	GPIO2A PU/PD control
GRF_GPIO2B_P_CON	0x00AC	W	0x0000AAAA	GPIO2B PU/PD control
GRF_GPIO2C_P_CON	0x00B0	W	0x0000AAAA	GPIO2C PU/PD control
GRF_GPIO3A_P_CON	0x00B4	W	0x000000AA	GPIO3A PU/PD control
GRF_GPIO3B_P_CON	0x00B8	W	0x00000296	GPIO3B PU/PD control
GRF_GPIO0B_D_CON	0x00C0	W	0x00000000	GPIO0B driver strength control
GRF_GPIO1B_D_CON	0x00C4	W	0x00000000	GPIO1B driver strength control
GRF_GPIO2A_D0_CON	0x00C8	W	0x00000000	GPIO2A driver strength control0
GRF_GPIO2A_D1_CON	0x00CC	W	0x00000000	GPIO2A driver strength control1
GRF_GPIO2B_D0_CON	0x00D0	W	0x00000000	GPIO2B driver strength control0
GRF_GPIO2B_D1_CON	0x00D4	W	0x00000000	GPIO2B driver strength control1
GRF_GPIO2C_D0_CON	0x00D8	W	0x00000000	GPIO2C driver strength control0
GRF_GPIO2C_D1_CON	0x00DC	W	0x00000000	GPIO2C driver strength control1
GRF_GPIO3A_D0_CON	0x00E0	W	0x00000000	GPIO3A driver strength control0
GRF_GPIO3A_D1_CON	0x00E4	W	0x00000000	GPIO3A driver strength control1
GRF_GPIO3B_D_CON	0x00E8	W	0x00000000	GPIO3B driver strength control
GRF_GPIO_SR_CON	0x00EC	W	0x00000000	GPIO slow rate control
GRF_GRF_INTR0_EN	0x0100	W	0x00000000	Interrupt enable
GRF_GRF_INTR0_CLR_EN	0x0104	W	0x00000000	Interrupt status clear enable
GRF_GRF_INTR0_STATUS	0x0108	W	0x00000000	Interrupt status
GRF_GRF_INTR0_RAW_STATUS	0x010C	W	0x00000000	Interrupt raw status
GRF_GRF_INTR1_EN	0x0110	W	0x00000000	Interrupt enable
GRF_GRF_INTR1_CLR_EN	0x0114	W	0x00000000	Interrupt clear control register
GRF_GRF_INTR1_STATUS	0x0118	W	0x00000000	Interrupt status
GRF_GRF_INTR1_RAW_STATUS	0x011C	W	0x00000000	Interrupt raw status

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Name	Offset	Size	Reset Value	Description
GRF_SYSETM_STATUS0	0x0120	W	0x00000000	System status register0
GRF_SYSTEM_STATUS3	0x012C	W	0x00000000	System status register3 bt1120 decoder last line address
GRF_SYSTEM_STATUS4	0x0130	W	0x00000000	System status register4 bt1120 last pix number
GRF_OS_REG0	0x0140	W	0x00000000	OS reserved register0
GRF_OS_REG1	0x0144	W	0x00000000	OS reserved register1
GRF_OS_REG2	0x0148	W	0x00000000	OS reserved register2
GRF_OS_REG3	0x014C	W	0x00000000	OS reserved register3
GRF_SOC_VERION	0x0150	W	0x01343B1A	SoC version register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.3.3 Detail Register Description

GRF_SYSTEM_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_hdmirx_audclk_ready HDMIRX audclk is valid. 1'b0: Unvalid clk 1'b1: Valid clk
26	RW	0x0	sw_vsync_pol 1'b1: Reverse vsync' pol 1'b0: None
25	RW	0x0	sw_hsync_pol 1'b1: Reverse hsync' pol 1'b0: None
24:22	RW	0x0	sw_adapter_i2csladr I2C slave address:0~7
21	RW	0x0	sw_edid_mode 1'b0: EDID ram can be access by RX's i2c 1'b1: EDID ram can be access by APB
20:17	RW	0x0	sw_i2c_flt_f Falling timeout period register for I2C glitch filter,typical value is 4
16:13	RW	0x0	sw_i2c_flt_r Rising timeout period register for I2C glitch filter,typical value is 4
12	RW	0x0	sw_scr1_soft_irq x'bxxx(bits < 4), x'hxxxx(bits >= 4)
11	RW	0x0	sw_bootroom_pgen 1'b0Normal mode 1'b1Powersave mode
10	RW	0x1	sw_i2s_data_oen The direction of I2S data on GPIO, when in function mode. 1'b0: Output 1'b1: Input
9	RW	0x1	sw_bt_data_oen The direction of BT1120/RGB data on GPIO, when in function mode. 1'b0: Output 1'b1: Input

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_efuse_hdcp_en 1'b1: HDCP ram can be access by APB 1'b0: HDCP ram can be access by RX's key memory interface
7:3	RW	0x01	sw_output_mode Output mode select sw_output_mode[4:3]: 2'b01: TX_BT1120 2'b10: TX_RGB 2'b11: TX_YUV Other: Disable sw_output_mode[2:0] 3'b001: TX_GVI 3'b010: TX_LVDS 3'b011: TX_HDMI 3'b100: TX_MIPI_CSI 3'b101: TX_MIPI_DSI Others: Interface above disabale
2:0	RW	0x3	sw_input_mode Input mode select 3'b000: HDMI 3'b001: reserve 3'b010: BT1120 3'b011: RGB 3'b100: YUV

GRF_SYSTEM_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_con_uart2rx_low_dly x'bxxx(bits < 4), x'hxxxx(bits >= 4)

GRF_SYSTEM_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Reserved

GRF_SYSTEM_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	sw_uart_cts_inv_en 1'b0: Disable 1'b1: Enable
10	RW	0x0	sw_uart_rts_inv_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	sw_uart_iomux_sel x'bxxx(bits < 4), x'hxxxx(bits >= 4)
8	RW	0x1	sw_force_jtag_m1 Force IO to JTAG IOMUX group enabl 1'b0: Diabl 1'b1: Enable

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Bit	Attr	Reset Value	Description
7	RW	0x0	sw_hdmirx_cec_iomux_sel Hdmirx_cec signals input select 1'b0: HDMIRX_cec0 1'b1: HDMIRX_cec1
6	RW	0x0	sw_rxddc_sda_iomux_sel IOMUX input select 1'b0: Select rxddc_sda0 1'b1: Select rxddc_sda1
5	RW	0x0	sw_rxddc_scl_iomux_sel IOMUX input select 1'b0: Select rxddc_scl0 1'b1: Select rxddc_scl1
4	RW	0x0	sw_i2s_ws_iomux_sel IOMUX input select 1'b0: Select i2s_lrm0 1'b1: Select i2s_lrm1
3	RW	0x0	sw_i2s_sd_iomux_sel IOMUX input select 1'b0: Select i2s_dm0 1'b1: Select i2s_dm1
2	RW	0x0	sw_i2s_sck_iomux_sel IOMUX input select 1'b0: Select i2s_sckm0 1'b1: Select i2s_sckm1
1:0	RO	0x0	reserved

GRF_SCALER_CON0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x00	reserved
8	RW	0x0	scl_ver_down_mode 1'b0: Bilinear 1'b1: Proprietary averaging filter
7	RW	0x0	scl_hor_down_mode 1'b0: Bilinear 1'b1: Proprietary averaging filter
6:5	RW	0x0	scl_bic_coe_sel scl_coe_bic_sel 2'b0: Precise(a=-0.75) 2'b1: Spline(a=0) 2'b2: Catrom(a=-0.5) 2'b3: Mitchell(a=-1/3)
4:3	RW	0x0	scl_ver_mode 2’b0: No scale 2’b1: Scale up 2’b2: Scale down

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	scl_hor_mode 2'b0: No scale 2'b1: Scale up 2'b2: Scale down
0	RW	0x0	scl_en 1'b0: Scaler disable 1'b1: Scaler enable

GRF_SCALER_CON1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	scl_v_factor scl_v_factor (1)scaling up: (Vin_act-1)/(Vout_act-1)*2^16; (2)scaling down(bilinear): if(Hin_act-1)/(Vout_act-1)>2.0, (Vin_act-1)/(Vout_act-1)*2^14; else (Vin_act-2)/(Vout_act-1)*2^14; (3)scaling down(average): (Vout_act)/(Vin_act-1)*2^16;
15:0	RW	0x0000	scl_h_factor (1)scaling up: (Hin_act-1)/(Hout_act-1)*2^16; (2)scaling down(bilinear): (Hin_act-1)/(Hout_act-1)*2^14 if(Hin_act-1)/(Hout_act-1)>2.0, (Hin_act-1)/(Hout_act-1)*2^14; else (Hin_act-2)/(Hout_act-1)*2^14 (3)scaling down(average): (Hout_act)/(Hin_act-1)*2^16;

GRF_SCALER_CON2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_frame_vst Scaler dsp frame v start point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_frame_hst Scaler dsp frame h start point

GRF_SCALER_CON3

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dsp_hs_end Scaler dsp hs end
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_htotal Scaler dsp htotal

GRF_SCALER_CON4

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_hact_st Scaler dsp horizontal active start point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hact_end Scaler dsp horizontal active end point

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GRF_SCALER_CON5
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dsp_vs_end Scaler dsp vs end
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vtotal Scaler dsp vtotal

GRF_SCALER_CON6
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vact_st Scaler dsp vertical active start point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vact_end Scaler dsp vertical active end point

GRF_SCALER_CON7
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_hbor_st Scaler dsp horizontal border st point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hbor_end Scaler dsp horizontal border end point

GRF_SCALER_CON8
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vbor_st Scaler dsp vertical border st point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vbor_end Scaler dsp vertical border end point

GRF_POST_PROC_CON
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	sw_i2s_sclk_out_inv_en x'bxxx(bits < 4), x'hxxxx(bits >= 4)
10	RW	0x0	sw_i2s_sclk_in_inv_en x'bxxx(bits < 4), x'hxxxx(bits >= 4)
9	RW	0x0	sw_dclk_out_inv_en x'bxxx(bits < 4), x'hxxxx(bits >= 4)
8	RW	0x0	sw_dclk_in_inv_en x'bxxx(bits < 4), x'hxxxx(bits >= 4)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	sw_txphy_refclk_sel 2'b0: Xin_osc_24m 2'b1: LVDS_clock 2'b2: HDMITX_vclk 2'b3: Xin_osc_24m
4	RW	0x0	sw_hdmitx_vclk_pllref_sel 1'b0: Osc_xin_24m 1'b1: Pin_vclk
3	RW	0x0	sw_hdmitx_dclk_inv_en 1'b0: Disable 1'b1: Enable
2	RO	0x0	reserved
1	RW	0x0	sw_split_mode Reserved
0	RW	0x0	sw_split_en 1'b0: Disable 1'b1: Enable

GRF_CSC_CTRL_CON

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15:9	RO	0x00	reserved
8	RW	0x0	sw_yuv2vyu_swp 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	sw_r2y_csc_mode Color space conversion mode. 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	sw_r2y_en 1'b0: Bypass 1'b1: Enable
3:2	RW	0x0	sw_y2r_csc_mode Color space conversion mode. 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	sw_y2r_en 1'b0: Bypass 1'b1: Enable

GRF_LVDS_TX_CON

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	sw_lvds_con_dual_sel 1'b0: odd_even dual channel 1'b1: left_right dual channel
11	RW	0x0	sw_lvds_con_den_polarity LVDS hsync polarity, used in dual channel lvds mode 1'b0: Low active 1'b1: High active
10	RW	0x0	sw_lvds_con_hs_polarity LVDS hsync polarity, used in dual channel lvds mode 1'b0: Low active 1'b1: High active
9	RW	0x0	sw_lvds_con_clkinv LVDS dclk_div2 invert enable, used in dual channel lvds mode. 1'b0: No invert 1'b1: Invert
8	RW	0x0	sw_lvds_startphase Dclk_div2 start phase at beginning of hs 1'b0: H_BP width is even, dclk_div2 reset to 0 at beginning of hs 1'b1: H_BP width is odd, dclk_div2 reset to 1 at beginning of hs
7	RW	0x0	sw_lvds_con_startsel LVDS start channel select 1'b0: Channel 0 transmit odd pixel 1'b1: Channel 0 transmit even pixel
6	RW	0x0	sw_lvds_con_chasel LVDS output channel select 1'b0: Just channel 0 output 1'b1: Channel 0 and channel 1 output
5	RW	0x0	sw_lvds_tie_vsync_value Only valid when lvds_tie_den_only== 1 1'b0: LVDS vsync are tied to 0 1'b1: LVDS vsync are tied to 1
4	RW	0x0	sw_lvds_tie_hsync_value Only valid when lvds_tie_den_only== 1 1'b0: LVDS hsync are tied to 0 1'b1: LVDS hsync are tied to 1
3	RW	0x0	grf_con_lvds_den_only_tie_value 1'b0: LVDS vsync/hsync normal output sw_lvds_tie_den_only 1'b1: LVDS vsync/hsync are tied to
2	RW	0x0	sw_lvds_con_msbsel LVDS lane input format 1'b0: LSB 1'b1: MSB
1:0	RW	0x0	sw_lvds_con_select LVDS output format 2'b00: VESA 24bit 2'b01: JEIDA 24bit 2'b10: JEIDA 18bit 2'b11: VESA 18bit

GRF_RGB_DEC_CON0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_hres reserved
15:10	RO	0x00	reserved
9	RW	0x0	sw_yuv_uv_swap 1'b0: No swap for cb and cr 1'b1: Swap for cb and cr Only for YUV decoder mode
8	RW	0x0	sw_yuv_yc_swap 1'b0: No swap for y and c 1'b1: Swap for y and c Only for YUV decoder mode
7	RO	0x0	reserved
6	RW	0x0	sw_bt1120_dual_data_swap 1'b0: Swap disable 1'b1: Swap enable
5	RW	0x0	sw_bt1120_dec_dualedge_en 1'b0: single_edge 1'b1: dual_edge Only for BT1120 decoder mode
4	RW	0x0	sw_bt1120_progress_en 1'b0: Interlace 1'b1: Progress Note, only for BT1120 mode
3	RW	0x0	sw_bt1120_yc_swap 1'b0: No swap for y and c 1'b1: Swap for y and c Only for BT1120 decoder mode
2	RW	0x0	sw_bt1120_uv_swap 1'b0: No swap for cb and cr 1'b1: Swap for cb and cr Only for BT1120 decoder mode
1	RW	0x0	sw_cap_en_async 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_cap_en_psync 1'b0: Disable 1'b1: Enable

GRF_RGB_DEC_CON1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_set_x The expected width of received image
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_start_x The horizontal ordinate of the start point

GRF_RGB_DEC_CON2

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_set_y The expected height of received image

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_start_y The vertical ordinate of the start point

GRF_RGB_ENC_CON

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15:10	RO	0x00	reserved
9	RW	0x0	sw_yuv_uv_swap 1'b0: No swap for cb and cr 1'b1: Swap for cb and cr Only for YUV encoder mode
8	RW	0x0	sw_yuv_yc_swap 1'b0: No swap for y and c 1'b1: Swap for y and c Only for YUV encoder mode
7	RW	0x0	sw_dsp_interlace 1'b0: Progress 1'b1: Interlace
6	RO	0x0	reserved
5	RW	0x0	sw_bt1120_uv_swap 1'b0: No swap for cb and cr 1'b1: Swap for cb and cr Only for BT1120 encoder mode
4	RW	0x0	sw_bt1120_yc_swap 1'b0: No swap for y and c 1'b1: Swap for y and c Only for BT1120 encoder mode
3	RW	0x0	sw_enc_dualedge_en 1'b0: single_edge 1'b1: dual_edge Only for BT1120 encoder mode
2:0	RO	0x0	reserved

GRF_MIPI_LANE_DELAY_CON0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mipi_lane_delay_con0 MIPI lane_delay count register, LSB32

GRF_MIPI_LANE_DELAY_CON1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mipi_lane_delay_con1 MIPI lane_delay count register, MSB32

GRF_BT1120_DCLK_DELAY_CON0

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mipi_lane_delay_con0 MIPI lane_delay count register, LSB32

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GRF_BT1120_DCLK_DELAY_CON1

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mipi_lane_delay_con0 MIPI lane_delay count register, LSB32

GRF_MIPI_TX0_CON

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	dsi0_dpiuptdatecfg This signal is used to indicate that the next frame will have new video configuration
25	RW	0x0	dsi0_dpicolorm It is used to switching between normal color and reduce color mode
24	RW	0x0	dsi0_dpishutdn It is used to shutdown the display
23:22	RO	0x0	reserved
21	RW	0x0	csi_phyrstz This line is used to place the digital section of the PHY in reset state when MIPI_CSI work
20	RW	0x0	csi_physhutdownz This line is used to place the PHY in shutdown when mipi csi work
19	RW	0x0	dphy0_forcetxstopmode_3 Force lane module into transmit mode and generate stop state
18	RW	0x0	dphy0_forcetxstopmode_2 Force lane module into transmit mode and generate stop state
17	RW	0x0	dphy0_forcetxstopmode_1 Force lane module into transmit mode and generate stop state
16	RW	0x0	dphy0_forcetxstopmode_0 Force lane module into transmit mode and generate stop state
15	RW	0x0	dphy0_forcerxmode_3 Force lane module into receive Mode/Wait for stop state
14	RW	0x0	dphy0_forcerxmode_2 Force lane module into receive Mode/Wait for stop state
13	RW	0x0	dphy0_forcerxmode_1 Force lane module into receive Mode/Wait for stop state
12	RW	0x0	dphy0_forcerxmode_0 Force lane module into receive Mode/Wait for stop state
11	RO	0x0	reserved
10	RW	0x0	dphy0_testclr Vendor-specific interface clear signal
9	RW	0x0	dphy0_testclk Vendor-specific interface operation strobe signal, it's used to clock the TESTDIN bus contents into the DPHY
8	RW	0x0	dphy0_test_en Vendor-specific interface operation type selector
7:0	RW	0x00	dphy0_testdin Vendor-specific input 8-bit data bus for internal register programming and test functionalities access

GRF_DPHY0_STATUS

Address: Operational Base + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	dphy_phylock When set, it signals that the PLL acquired lock with input REFCLK
23	RO	0x0	dphy_txulpsactivenot_3 This signal indicates that the lane is in the Ultra Low Power state
22	RO	0x0	dphy_txulpsactivenot_2 This signal indicates that the lane is in the Ultra Low Power state
21	RO	0x0	dphy_txulpsactivenot_1 This signal indicates that the lane is in the Ultra Low Power state
20	RO	0x0	dphy_txulpsactivenot_0 This signal indicates that the lane is in the Ultra Low Power state
19	RO	0x0	dphy_stopstate_3 This signal indicate that the data3 lane module is in stop state
18	RO	0x0	dphy_stopstate_2 This signal indicate that the data2 lane module is in stop state
17	RO	0x0	dphy_stopstate_1 This signal indicate that the data1 lane module is in stop state
16	RO	0x0	dphy_stopstate_0 This signal indicate that the data0 lane module is in stop state
15:8	RO	0x00	dphy_testdout Vendor-specific output 8-bit data bus for read-bak and internal probing functionalities
7:5	RO	0x0	reserved
4:0	RO	0x00	dphy_phyerr0lane DPHY error status

GRF_MIPI_TX1_CON

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	dsi1_dpiuptdatecfg This signal is used to indicate that the next frame will have new video configuration
25	RW	0x0	dsi1_dpicolorm It is used to switching between normal color and reduce color mode
24	RW	0x0	dsi1_dpishutdn It is used to shutdown the display
23:20	RO	0x0	reserved
19	RW	0x0	dphy1_forcetxstopmode_3 Force lane module into transmit mode and generate stop state
18	RW	0x0	dphy1_forcetxstopmode_2 Force lane module into transmit mode and generate stop state
17	RW	0x0	dphy1_forcetxstopmode_1 Force lane module into transmit mode and generate stop state
16	RW	0x0	dphy1_forcetxstopmode_0 Force lane module into transmit mode and generate stop state
15	RW	0x0	dphy1_forcerxmode_3 Force lane module into receive Mode/Wait for stop state
14	RW	0x0	dphy1_forcerxmode_2 Force lane module into receive Mode/Wait for stop state
13	RW	0x0	dphy1_forcerxmode_1 Force lane module into receive Mode/Wait for stop state

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Bit	Attr	Reset Value	Description
12	RW	0x0	dphy1_forcerxmode_0 Force lane module into receive Mode/Wait for stop state
11	RO	0x0	reserved
10	RW	0x0	dphy1_testclr Vendor-specific interface clear signal
9	RW	0x0	dphy1_testclk Vendor-specific interface operation strobe signal, it's used to clock the TESTDIN bus contents into the DPHY
8	RW	0x0	dphy1_test_en Vendor-specific interface operation type selector
7:0	RW	0x00	dphy1_testdin Vendor-specific input 8-bit data bus for internal register programming and test functionalities access

GRF_DPHY1_STATUS

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	dphy_phylock When set 1'b1, it signals that the PLL acquired lock with input REFCLK
23	RO	0x0	dphy_txulpsactivenot_3 This signal indicates that the lane is in the Ultra Low Power state
22	RO	0x0	dphy_txulpsactivenot_2 This signal indicates that the lane is in the Ultra Low Power state
21	RO	0x0	dphy_txulpsactivenot_1 This signal indicates that the lane is in the Ultra Low Power state
20	RO	0x0	dphy_txulpsactivenot_0 This signal indicates that the lane is in the Ultra Low Power state
19	RO	0x0	dphy_stopstate_3 This signal indicate that the data3 lane module is in stop state
18	RO	0x0	dphy_stopstate_2 This signal indicate that the data2 lane module is in stop state
17	RO	0x0	dphy_stopstate_1 This signal indicate that the data1 lane module is in stop state
16	RO	0x0	dphy_stopstate_0 This signal indicates that the data0 lane module is in stop state
15:8	RO	0x00	dphy_testdout Vendor-specific output 8-bit data bus for read-back and internal probing functionalities
7:5	RO	0x0	reserved
4:0	RO	0x00	dphy_phyerr0lane DPHY error status

GRF_GPIO0AB_SEL_CON

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15	RW	0x0	gpio0b3_sel GPIO function sel 1'b0: GPIO0b3 1'b1: CECtx

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Bit	Attr	Reset Value	Description
14	RW	0x0	gpio0b2_sel GPIO function sel 1'b0: GPIO0b2 1'b1: DDCscltx
13	RW	0x0	gpio0b1_sel GPIO function sel 1'b0: GPIO0b1 1'b1: DDCsdatx
12	RW	0x0	gpio0b0_sel GPIO function sel 1'b0: GPIO0b0 1'b1: HPDin
11:10	RW	0x0	gpio0a7_sel GPIO function sel 2'b0: GPIO0a7 2'b1: I2SM0d3 2'b2: Uart_rtsnm1
9:8	RW	0x0	gpio0a6_sel GPIO function sel 2'b0: GPIO0a6 2'b1: I2SM0d2 2'b2: Uart_ctsnm1
7:6	RW	0x0	gpio0a5_sel GPIO function sel 2'b0: GPIO0a5 2'b1: I2SM0d1 2'b2: Uart_rxm1
5:4	RW	0x0	gpio0a4_sel GPIO function sel 2'b0: GPIO0a4 2'b1: I2SM0d0 2'b2: Uart_txm1
3	RW	0x0	gpio0a3_sel GPIO function sel 1'b0: GPIO0a3 1'b1: I2Slr_m0
2	RW	0x0	gpio0a2_sel GPIO function sel 1'b0: GPIO_0a2 1'b1: I2S_sckm0
1:0	RO	0x0	reserved

GRF_GPIO1AB_SEL_CON

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15:14	RW	0x1	gpio1b5_sel GPIO function sel 2'b0: GPIO1b5 2'b1: I2Cs_sda 2'b2: I2Cm_sda

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Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio1b4_sel GPIO function sel 2'b0: GPIO1b4 2'b1: I2Cs_scl 2'b2: I2Cm_scl
11	RW	0x0	gpio1b3_sel GPIO function sel 1’b0: GPIO1b3 1’b1: CECM0rx
10	RW	0x0	gpio1b2_sel GPIO function sel 1'b0: GPIO1b2 1'b1: DDCM0sclrx
9	RW	0x0	gpio1b1_sel GPIO function sel 1’b0: GPIO1b1 1’b1: DDCM0sdarx
8	RW	0x0	gpio1b0_sel GPIO function sel 1’b0: GPIO1b0 1’b1: HPDM0out
7	RW	0x0	gpio1a7_sel GPIO function sel 1’b0: GPIO1a7 1’b1: I2SM1d3
6	RW	0x0	gpio1a6_sel GPIO function sel 1’b0: GPIO1a6 1’b1: I2SM1d2
5	RW	0x0	gpio1a5_sel GPIO function sel 1’b0: GPIO1a5 1’b1: I2SM1d1
4	RW	0x0	gpio1a4_sel GPIO function sel 1’b0: GPIO1a4 1’b1: I2SM1d0
3	RW	0x0	gpio1a3_sel GPIO function sel 1’b0: GPIO1a3 1’b1: I2SM1lr
2	RW	0x0	gpio1a2_sel GPIO function sel 1’b0: GPIO1a2 1’b1: I2Ssckm1
1	RW	0x0	gpio1a1_sel GPIO function sel 1’b0: GPIO1a1 1’b1: Xipsfc_sclk
0	RW	0x0	gpio1a0_sel GPIO function sel 1’b0: GPIO1a0 1’b1: TESTclkout

GRF_GPIO2AB_SEL_CON

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Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15	RW	0x0	gpio2b7_sel GPIO function sel 1'b0: GPIO2b7 1'b1: VOPd15
14	RW	0x0	gpio2b6_sel GPIO function sel 1'b0: GPIO2b6 1'b1: VOPd14
13	RW	0x0	gpio2b5_sel GPIO function sel 1'b0: GPIO2b5 1'b1: VOPd13
12	RW	0x0	gpio2b4_sel GPIO function sel 1'b0: GPIO2b4 1'b1: VOPd12
11	RW	0x0	gpio2b3_sel GPIO function sel 1'b0: GPIO2b3 1'b1: VOPd11
10	RW	0x0	gpio2b2_sel GPIO function sel 1'b0: GPIO2b2 1'b1: VOPd10
9	RW	0x0	gpio2b1_sel GPIO function sel 1'b0: GPIO2b1 1'b1: VOPd9
8	RW	0x0	gpio2b0_sel GPIO function sel 1'b0: GPIO2b0 1'b1: VOPd8
7	RW	0x0	gpio2a7_sel GPIO function sel 1'b0: GPIO2a7 1'b1: VOPd7
6	RW	0x0	gpio2a6_sel GPIO function sel 1'b0: GPIO2a6 1'b1: VOPd6
5	RW	0x0	gpio2a5_sel GPIO function sel 1'b0: GPIO2a5 1'b1: VOPd5
4	RW	0x0	gpio2a4_sel GPIO function sel 1'b0: GPIO2a4 1'b1: VOPd4
3	RW	0x0	gpio2a3_sel GPIO function sel 1'b0: GPIO2a3 1'b1: VOPd3

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio2a2_sel GPIO function sel 1'b0: GPIO2a2 1'b1: VOPd2
1	RW	0x0	gpio2a1_sel GPIO function sel 1'b0: GPIO2a1 1'b1: VOPd1
0	RW	0x0	gpio2a0_sel GPIO function sel 1'b0: GPIO2a0 1'b1: VOPd0

GRF_GPIO2C_SEL_CON

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15:14	RW	0x2	gpio2c7_sel GPIO function sel 2'b0: GPIO2c7 2'b1: VOPd23 2'b2: Risvjtag_trstn
13:12	RW	0x2	gpio2c6_sel GPIO function sel 2'b0: GPIO2c6 2'b1: VOPd22 2'b2: Risvjtag_tck 2'b3: UART_rtsnm0
11:10	RW	0x2	gpio2c5_sel GPIO function sel 2'b0: GPIO2c5 2'b1: VOPd21 2'b2: Risvjtag_tms 2'b3: UART_ctsnm0
9:8	RW	0x2	gpio2c4_sel GPIO function sel 2'b0: GPIO2c4 2'b1: VOPd20 2'b2: Risvjtag_tdi 2'b3: UART_rxm0
7:6	RW	0x2	gpio2c3_sel GPIO function sel 2'b0: GPIO2c3 2'b1: VOPd19 2'b2: Risvjtag_tdo 2'b3: UART_txm0
5:4	RW	0x0	gpio2c2_sel GPIO function sel 2'b0: GPIO2c2 2'b1: VOPd18 2'b2: Xipsfc_mosi

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio2c1_sel GPIO function sel 2'b0: GPIO2c1 2'b1: VOPd17 2'b2: Xipsfc_miso
1:0	RW	0x0	gpio2c0_sel GPIO function sel 2'b0: GPIO2c0 2'b1: VOPd16 2'b2: Xipsfc_csn

GRF_GPIO3AB_SEL_CON

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15:14	RO	0x0	reserved
13:12	RW	0x1	gpio3b4_sel GPIO function sel 2'b1: SPIboot 2'b2: Int Others: GPIO3b4
11	RO	0x0	reserved
10	RW	0x0	gpio3b2_sel GPIO function sel 1'b0: GPIO3b2 1'b1: GVIlock
9	RW	0x0	gpio3b1_sel GPIO function sel 1'b0: GPIO3b1 1'b1: GVIhpd
8	RW	0x0	gpio3b0_sel GPIO function sel 1'b0: GPIO3b0 1'b1: VOPdclk
7	RW	0x0	gpio3a7_sel GPIO function sel 1'b0: GPIO3a7 1'b1: CECM1rx
6	RW	0x0	gpio3a6_sel GPIO function sel 1'b0: GPIO3a6 1'b1: DDCM1sclrx
5	RW	0x0	gpio3a5_sel GPIO function sel 1'b0: GPIO3a5 1'b1: DDCM1sdarx
4	RW	0x0	gpio3a4_sel GPIO function sel 1'b0: GPIO3a4 1'b1: HPDM1out

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Bit	Attr	Reset Value	Description
3	RW	0x0	gpio3a3_sel GPIO function sel 1'b0: GPIO3a3 1'b1: VOPvsync
2	RO	0x0	reserved
1	RW	0x0	gpio3a1_sel GPIO function sel 1'b0: GPIO3a1 1'b1: VOPhsync
0	RW	0x0	gpio3a0_sel GPIO function sel 1'b0: GPIO3a0 1'b1: VOPden

GRF_GPIO2A_SMT

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x00	reserved
7	RW	0x0	gpio2a7_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
6	RW	0x0	gpio2a6_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
5	RW	0x0	gpio2a5_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
4	RW	0x0	gpio2a4_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
3	RW	0x0	gpio2a3_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
2	RW	0x0	gpio2a2_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
1	RW	0x0	gpio2a1_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
0	RW	0x0	gpio2a0_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

GRF_GPIO2B_SMT

Address: Operational Base + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x00	reserved
7	RW	0x0	gpio2b7_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
6	RW	0x0	gpio2b6_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
5	RW	0x0	gpio2b5_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
4	RW	0x0	gpio2b4_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
3	RW	0x0	gpio2b3_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
2	RW	0x0	gpio2b2_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
1	RW	0x0	gpio2b1_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
0	RW	0x0	gpio2b0_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

GRF_GPIO2C_SMT

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x00	reserved
7	RW	0x0	gpio2c7_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
6	RW	0x0	gpio2c6_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
5	RW	0x0	gpio2c5_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

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Bit	Attr	Reset Value	Description
4	RW	0x0	gpio2c4_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
3	RW	0x0	gpio2c3_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
2	RW	0x0	gpio2c2_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
1	RW	0x0	gpio2c1_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
0	RW	0x0	gpio2c0_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

GRF_GPIO3AB_SMT

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x00	reserved
8	RW	0x0	gpio3b0_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
7:4	RO	0x0	reserved
3	RW	0x0	gpio2a3_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
2	RO	0x0	reserved
1	RW	0x0	gpio2a1_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
0	RW	0x0	gpio2a0_smt 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

GRF_GPIO0A_P_CON

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15:14	RW	0x2	gpio0a7_ren 2'b00: High-z 2'b10: Pull down Other: reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	gpio0a6_ren 2'b00: High-z 2'b10: Pull down Other: reserved
11:10	RW	0x2	gpio0a5_ren 2'b00: High-z 2'b10: Pull down Other: reserved
9:8	RW	0x2	gpio0a4_ren 2'b00: High-z 2'b10: Pull down Other: reserved
7:6	RW	0x2	gpio0a3_ren 2'b00: High-z 2'b10: Pull down Other: reserved
5:4	RO	0x0	reserved
3:2	RW	0x2	gpio0a1_ren 2'b00: High-z 2'b10: Pull down Other: reserved
1:0	RW	0x2	gpio0a0_ren 2'b00: High-z 2'b10: Pull down Other: reserved

GRF_GPIO1A_P_CON

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15:14	RW	0x2	gpio1a7_ren 2'b00: High-z 2'b10: Pull down Other: reserved
13:12	RW	0x2	gpio1a6_ren 2'b00: High-z 2'b10: Pull down Other: reserved
11:10	RW	0x2	gpio1a5_ren 2'b00: High-z 2'b10: Pull down Other: reserved
9:8	RW	0x2	gpio1a4_ren 2'b00: High-z 2'b10: Pull down Other: reserved
7:6	RW	0x2	gpio1a3_ren 2'b00: High-z 2'b10: Pull down Other: reserved
5:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio1a1_ren 2'b00: High-z 2'b10: Pull down Other: reserved
1:0	RW	0x2	gpio1a0_ren 2'b00: High-z 2'b10: Pull down Other: reserved

GRF_GPIO2A_P_CON

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x:/'hxxxx(bits >= 4)
15:14	RW	0x2	gpio_2a7_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
13:12	RW	0x2	gpio_2a6_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
11:10	RW	0x2	gpio_2a5_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
9:8	RW	0x2	gpio_2a4_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
7:6	RW	0x2	gpio_2a3_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
5:4	RW	0x2	gpio_2a2_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
3:2	RW	0x2	gpio_2a1_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
1:0	RW	0x2	gpio_2a0_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z

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GRF_GPIO2B_P_CON

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x:/'hxxxx(bits >= 4)
15:14	RW	0x2	gpio_2b7_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
13:12	RW	0x2	gpio_2b6_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
11:10	RW	0x2	gpio_2b5_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
9:8	RW	0x2	gpio_2b4_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
7:6	RW	0x2	gpio_2b3_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
5:4	RW	0x2	gpio_2b2_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
3:2	RW	0x2	gpio_2b1_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
1:0	RW	0x2	gpio_2b0_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z

GRF_GPIO2C_P_CON

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x:/'hxxxx(bits >= 4)
15:14	RW	0x2	gpio_2c7_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	gpio_2c6_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
11:10	RW	0x2	gpio_2c5_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
9:8	RW	0x2	gpio_2c4_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
7:6	RW	0x2	gpio_2c3_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
5:4	RW	0x2	gpio_2c2_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
3:2	RW	0x2	gpio_2c1_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z
1:0	RW	0x2	gpio_2c0_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z

GRF_GPIO3A_P_CON

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15:8	RO	0x00	reserved
7:6	RW	0x2	gpio_3a3_pu_pd x'bxxx(bits < 4), x'hxxxx(bits >= 4)
5:4	RW	0x2	gpio_3a2_ren 2'b00: High-z 2'b10: Pull down Other: reserved
3:2	RW	0x2	gpio_3a1_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z

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Bit	Attr	Reset Value	Description
1:0	RW	0x2	gpio_3a0_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z

GRF_GPIO3B_P_CON

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15:10	RO	0x00	reserved
9:8	RW	0x2	gpio_3b4_ren 2'b00: High-z 2'b10: Pull down Other: reserved
7:6	RW	0x2	gpio_3b3_ren 2'b00: High-z 2'b10: Pull down Other: reserved
5:4	RW	0x1	gpio_3b2_ren 2'b00: High-z 2'b01: Pull up Other: reserved
3:2	RW	0x1	gpio_3b1_ren 2'b00: High-z 2'b01: Pull up Other: reserved
1:0	RW	0x2	gpio_3b0_pu_pd pu,pd 2'b01: Pull_down 2'b10: Pull_up Else : High-z

GRF_GPIO0B_D_CON

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15:8	RO	0x00	reserved
7:6	RW	0x0	gpio0b3_d High level driver strength setting condition gpio0b3_d1, gpio0b3_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio0b2_d High level driver strength setting condition gpio0b2_d1, gpio0b2_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)
3:2	RW	0x0	gpio0b1_d High level driver strength setting condition gpio0b1_d1, gpio0b1_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)
1:0	RW	0x0	gpio0b0_d High level driver strength setting condition gpio0b0_d1, gpio0b0_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)

GRF_GPIO1B_D_CON

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15:12	RO	0x0	reserved
11:10	RW	0x0	gpio1b5_d High level driver strength setting condition gpio1b0_d1, gpio1b0_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)
9:8	RW	0x0	gpio1b4_d High level driver strength setting condition gpio1b0_d1, gpio1b0_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)
7:6	RW	0x0	gpio1b3_d High level driver strength setting condition gpio1b0_d1, gpio1b0_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio1b2_d High level driver strength setting condition gpio1b0_d1, gpio1b0_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)
3:2	RW	0x0	gpio1b1_d High level driver strength setting condition gpio1b0_d1, gpio1b0_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)
1:0	RW	0x0	gpio1b0_d High level driver strength setting condition gpio1b0_d1, gpio1b0_d0 2'b00: 33.1mA(Ioh2.4V)/19.3mA(Iol0.4V) 2'b01: 39.7mA(Ioh2.4V)/23.1mA(Iol0.4V) 2'b10: 46.4mA(Ioh2.4V)/26.9.3mA(Iol0.4V) 2'b11: 53mA(Ioh2.4V)/30.8mA(Iol0.4V)

GRF_GPIO2A_D0_CON

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15	RO	0x0	reserved
14:12	RW	0x0	gpio2a3_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11	RO	0x0	reserved
10:8	RW	0x0	gpio2a2_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2a1_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3	RO	0x0	reserved
2:0	RW	0x0	gpio2a0_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO2A_D1_CON

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15	RO	0x0	reserved
14:12	RW	0x0	gpio2a7_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11	RO	0x0	reserved
10:8	RW	0x0	gpio2a6_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2a5_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3	RO	0x0	reserved
2:0	RW	0x0	gpio2a4_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO2B_D0_CON

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15	RO	0x0	reserved
14:12	RW	0x0	gpio2b3_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11	RO	0x0	reserved
10:8	RW	0x0	gpio2b2_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2b1_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3	RO	0x0	reserved
2:0	RW	0x0	gpio2b0_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO2B_D1_CON

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2b7_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11	RO	0x0	reserved
10:8	RW	0x0	gpio2b6_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2b5_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3	RO	0x0	reserved
2:0	RW	0x0	gpio2b4_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO2C_D0_CON

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2c3_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11	RO	0x0	reserved
10:8	RW	0x0	gpio2c2_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2c1_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3	RO	0x0	reserved
2:0	RW	0x0	gpio2c0_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO2C_D1_CON

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2c7_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11	RO	0x0	reserved
10:8	RW	0x0	gpio2c6_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2c5_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3	RO	0x0	reserved
2:0	RW	0x0	gpio2c4_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO3A_D0_CON

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15	RO	0x0	reserved
14:12	RW	0x0	gpio3a3_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11:7	RO	0x00	reserved
6:4	RW	0x0	gpio3a1_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	gpio3a0_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO3A_D1_CON

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable 1'b0: Disable 1'b1: Enable
15:14	RO	0x0	reserved
13:12	RW	0x0	gpio3a7_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
11:10	RO	0x0	reserved
9:8	RW	0x0	gpio3a6_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
7:6	RO	0x0	reserved
5:4	RW	0x0	gpio3a5_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio3a4_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO3B_D_CON

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable x'bxxx(bits < 4), x'hxxxx(bits >= 4)
15:3	RO	0x0000	reserved
2:0	RW	0x0	gpio3b_ds High level driver strength setting condition ds2,ds1,ds0: 3'b000: 17.8mA(Ioh0.75)/10.8mA(Iol0.125) 3'b001: 26.9mA(Ioh0.75)/16.1mA(Iol0.25) 3'b010: 35.8mA(Ioh0.75)/21.5mA(Iol0.25) 3'b011: 44.7mA(Ioh0.75)/26.9mA(Iol0.25) 3'b100: 53.6mA(Ioh0.75)/32.2mA(Iol0.25) 3'b101: 62.6mA(Ioh0.75)/37..5mA(Iol0.25) 3'b110: 89.4mA(Ioh0.75)/53.7mA(Iol0.25) 3'b111: 98.4mA(Ioh0.75)/59.1mA(Iol0.25)

GRF_GPIO_SR_CON

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	gpio_3a7_sl 1'b0: Slow 1'b1: Fast
14	RW	0x0	gpio_3a6_sl 1'b0: Slow 1'b1: Fast
13	RW	0x0	gpio_3a5_sl 1'b0: Slow 1'b1: Fast
12	RW	0x0	gpio_3a4_sl 1'b0: Slow 1'b1: Fast
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	gpio_1b5_sl 1'b0: Slow 1'b1: Fast
8	RW	0x0	gpio_1b4_sl 1'b0: Slow 1'b1: Fast
7	RW	0x0	gpio_1b3_sl 1'b0: Slow 1'b1: Fast
6	RW	0x0	gpio_1b2_sl 1'b0: Slow 1'b1: Fast
5	RW	0x0	gpio_1b1_sl 1'b0: Slow 1'b1: Fast
4	RW	0x0	gpio_1b0_sl 1'b0: Slow 1'b1: Fast
3	RW	0x0	gpio_0b3_sl 1'b0: Slow 1'b1: Fast
2	RW	0x0	gpio_0b2_sl 1'b0: Slow 1'b1: Fast
1	RW	0x0	gpio_0b1_sl 1'b0: Slow 1'b1: Fast
0	RW	0x0	gpio_0b0_sl 1'b0: Slow 1'b1: Fast

GRF_GRF_INTR0_EN

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x00	reserved
8	RO	0x0	hdmirx_int_en HDMIRX interrupt status
7	RO	0x0	reserved
6	RO	0x0	csi0_int_en MIPI_CSI0 interrupt status
5	RO	0x0	dsi0_int_en MIPI_DSI0 interrupt status
4	RO	0x0	dsi1_int_en MIPI_DSI1 interrupt status
3	RO	0x0	vbo_int_en VBO interrupt status

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Bit	Attr	Reset Value	Description
2	RO	0x0	hdmitx_int_en HDMITX raw interrupt status
1	RW	0x0	hdmitx_hpd_low_int_en x'bxxx(bits < 4), x'hxxxx(bits >= 4)
0	RW	0x0	hdmitx_hpd_high_int_en x'bxxx(bits < 4), x'hxxxx(bits >= 4)

GRF_GRF_INTR0_CLR_EN

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x00	reserved
8	W1C	0x0	hdmirx_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
7	RO	0x0	reserved
6	W1C	0x0	csi0_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
5	W1C	0x0	dsi0_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
4	W1C	0x0	dsi1_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
3	W1C	0x0	vbo_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
2	W1C	0x0	hdmitx_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
1	W1C	0x0	hdmitx_hpd_low_int_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
0	W1C	0x0	hdmitx_hpd_high_int_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear

GRF_GRF_INTR0_STATUS

Address: Operational Base + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	hdmirx_intr_status HDMIRX interrupt status
7	RO	0x0	reserved
6	RO	0x0	csi0_intr_status MIPI_CSI0 interrupt status
5	RO	0x0	dsi0_intr_status MIPI_DSI0 interrupt status
4	RO	0x0	dsi1_intr_status MIPI_DSI1 interrupt status
3	RO	0x0	vbo_intr_status VBO interrupt status
2	RO	0x0	hdmitx_intr_status HDMITX raw interrupt status
1	RW	0x0	hdmitx_hpd_low_int_status x'bxxx(bits < 4), x'hxxxx(bits >= 4)
0	RW	0x0	hdmitx_hpd_high_int_status x'bxxx(bits < 4), x'hxxxx(bits >= 4)

GRF_GRF_INTR0_RAW_STATUS

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	hdmirx_intr_raw_status HDMIRX raw interrupt status
7	RO	0x0	reserved
6	RO	0x0	csi0_intr_raw_status MIPI_CSI0 raw interrupt status
5	RO	0x0	dsi0_intr_raw_status MIPI_DSI0 raw interrupt status
4	RO	0x0	dsi1_intr_raw_status MIPI_DSI1 raw interrupt status
3	RO	0x0	vbo_intr_raw_status VBO raw interrupt status
2	RO	0x0	hdmitx_raw_status HDMITX raw interrupt status
1	RW	0x0	hdmitx_hpd_low_raw_int_status x'bxxx(bits < 4), x'hxxxx(bits >= 4)
0	RW	0x0	hdmitx_hpd_high_raw_int_status x'bxxx(bits < 4), x'hxxxx(bits >= 4)

GRF_GRF_INTR1_EN

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	i2cm_intr_en I2C master interrupt enable control
6	RW	0x0	uart_intr_en UART interrupt enable control
5	RW	0x0	xipsfc_intr_en Xipsfc interrupt enable control
4	RW	0x0	efuse_intr_en Efuse interrupt enable control
3	RW	0x0	gpio3_intr_en GPIO3 interrupt enable control
2	RW	0x0	gpio2_intr_en GPIO2 interrupt enable control
1	RW	0x0	gpio1_intr_en GPIO1 interrupt enable control
0	RW	0x0	gpio0_intr_en GPIO0 interrupt enable control

GRF_GRF_INTR1_CLR_EN

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x00	reserved
7	RW	0x0	i2cm_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
6	RW	0x0	uart_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
5	RW	0x0	xipsfc_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
4	W1C	0x0	efuse_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
3	W1C	0x0	gpio3_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
2	W1C	0x0	gpio2_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear

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Bit	Attr	Reset Value	Description
1	W1C	0x0	gpio1_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear
0	W1C	0x0	gpio0_intr_clr_en Interrupt clear enable signal 1'b0: Unclear 1'b1: Clear

GRF_GRF_INTR1_STATUS

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x00	reserved
7	RW	0x0	i2cm_intr_status I2C master interrupt status register
6	RW	0x0	uart_intr_status UART interrupt status register
5	RW	0x0	xipsfc_intr_status Xipsfc interrupt status register
4	RO	0x0	efuse_intr_status Efuse interrupt status register
3	RO	0x0	gpio3_intr_status GPIO3 interrupt status register
2	RO	0x0	gpio2_intr_status GPIO2 interrupt status register
1	RO	0x0	gpio1_intr_status GPIO1 interrupt status register
0	RO	0x0	gpio0_intr_status GPIO0 interrupt status register

GRF_GRF_INTR1_RAW_STATUS

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit16=1, bit0 can be written by software. When bit16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x00	reserved
7	RW	0x0	i2cm_intr_raw_status I2C master raw interrupt status
6	RW	0x0	uart_intr_raw_status UART raw interrupt status

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Bit	Attr	Reset Value	Description
5	RW	0x0	spi_intr_raw_status Xipsfc raw interrupt status
4	RO	0x0	efuse_raw_status EFUSE raw interrupt status
3	RO	0x0	gpio3_raw_status GPIO3 raw interrupt status
2	RO	0x0	gpio2_raw_status GPIO2 raw interrupt status
1	RO	0x0	gpio1_raw_status GPIO1 raw interrupt status
0	RW	0x0	gpio0_raw_status GPIO0 raw interrupt status

GRF_SYSETM_STATUS0

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RO	0x0	current_i2cslv_addr i2c_slv address
7:5	RO	0x0	reserved
4	RO	0x0	hpd_status_i HPD status of HDMI_TX or GVI_TX
3	RO	0x0	rx_hpd_status HPD out of dprx or hdmirx
2	RW	0x0	cpll_lock x'bxxx(bits < 4), x'hxxxx(bits >= 4)
1	RO	0x0	reserved
0	RW	0x0	combtxphy_pll_lock x'bxxx(bits < 4), x'hxxxx(bits >= 4)

GRF_SYSTEM_STATUS3

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	decoder_1120_last_line_num_y Decoder 1120 last line_number of Y
15:13	RO	0x0	reserved
12:0	RO	0x0000	decoder_1120_last_line_num_c Decoder 1120 last line_number of CbCr

GRF_SYSTEM_STATUS4

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:13	RO	0x000	decoder_1120_last_pix_num_y Decoder 1120 last pixel number of Y
12:0	RO	0x0000	decoder_1120_last_pix_num_c Decoder 1120 last pixel number of CbCr

GRF_OS_REG0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg0 os register0

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GRF_OS_REG1

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg1 os register1

GRF_OS_REG2

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg2 os register2

GRF_OS_REG3

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg3 os register3

GRF_SOC_VERION

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RO	0x01343b1a	soc_chip_version SOC version

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Chapter 4 I2C SLAVE

4.1 Overview

The APB module can read or write all registers via I2C slave bus.

4.2 Block Diagram

This module supports I2C bus to APB bus converter.

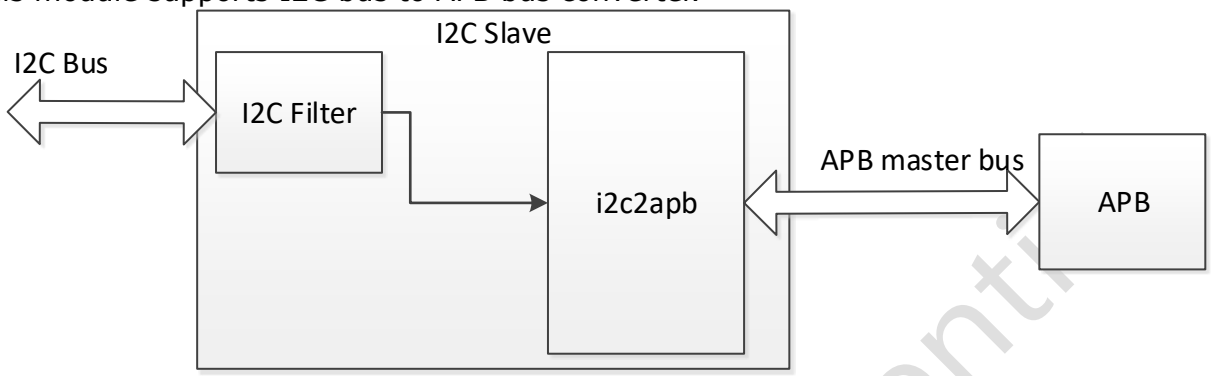

Fig. 5-1 I2C slave Block Diagram

4.3 Function Description

4.3.1 I2C Filter

I2C glitch filter is designed for avoiding the I2C communication error because of SDA and SCL signal glitches.
The SCL and SDA input signals from I2C bus are filtered (both positive edge and negative edge) by the glitch filter block. Then they are input to the i2c2apb module.
The glitch filter timeout values of both positive edge and negative edge can be configured with SYSTEM_CON[19:12].

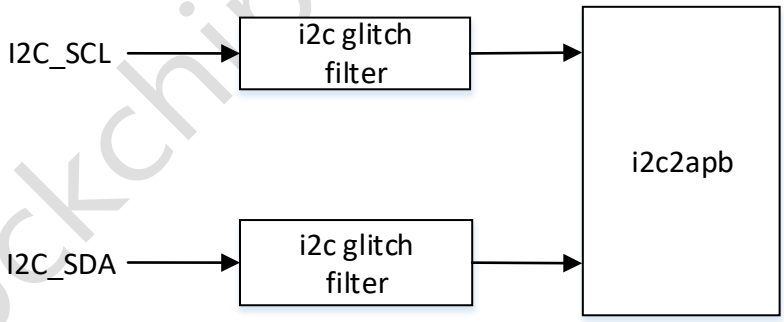

Fig. 5-2 I2C Glitch Filter

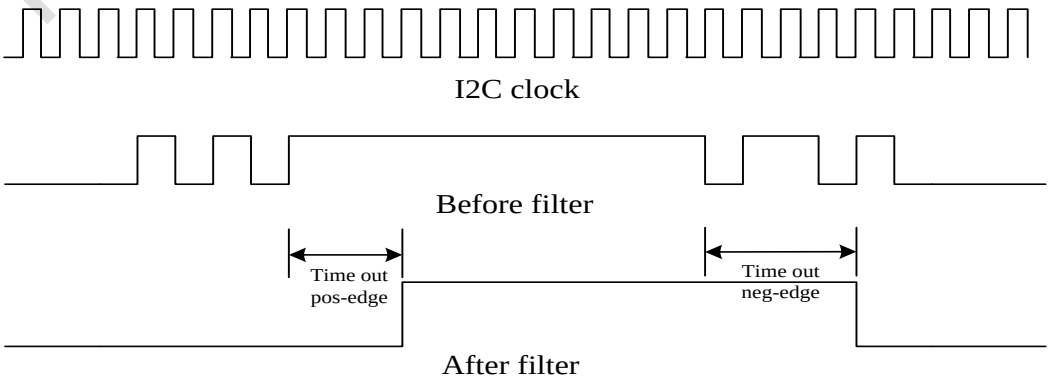

Fig. 5-3 I2C Glitch Filter Waveform

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4.3.2 i2c2apb

I2c2apb module converts I2C bus to APB master interface. AP can use it to access all registers and memory.

The i2c address consists of 7 bits, where the upper four bits are the identifier of the i2c device and the value is set to 4b'1010, the lower three bits are the device address. In order to meet the application of different scenarios, the I2C slave device address can be programmed through GOIO, the mapping of address to GPIO show as Table 4-1, the typical slave address is 7'b1010000.

Table 4-1 Mapping of i2c slave address to GPIO

Addr bit	Pad Name	GPIO Setting
cfg_slvadr[2]	IO_GPIO0a1	GPIO0A_OE[1]=1'b1
cfg_slvadr[1]	IO_GPIO0a0	GPIO0A_OE[0]=1'b1
cfg_slvadr[0]	IO_GPIO3b3	GPIO3B_OE[2]=1'b1

- Single Read Operation
  - First, AP asserts I2C start signal.
  - Second, AP sends device address (7bits) and R/W bit (1'b0). I2C Slave will reply ACK when receiving the right device address. If the device address doesn't match, I2C slave will ignore this operation.
  - Third, AP sends 4 bytes register address. Low bytes first. I2C Slave replies ACK.
  - Fourth, AP asserts I2C re-start signal.
  - Fifth, AP sends device address (7bits) and R/W bit (1'b1). I2C Slave will reply ACK when receiving the right device address.
  - Sixth, I2C slave reply the 4 bytes read data. Low bytes first. AP replies ACK.
  - Seventh, AP asserts I2C stop signal to finish this operation.

- Single Write Operation
  - First, AP asserts I2C start signal.
  - Second, AP sends device address (7bits) and R/W bit (1'b0). I2C slave will reply ACK when receiving the right device address. If the device address doesn't match, I2C slave will ignore this operation.
  - Third, AP sends 4 bytes register address. Low bytes first. I2C slave replies ACK.
  - Fourth, AP sends device 4 bytes write data. Low bytes first. I2C slave replies ACK when no APB error response received, or else I2C slave replies NAK.
  - Fifth, AP asserts I2C stop signal to finish this operation.

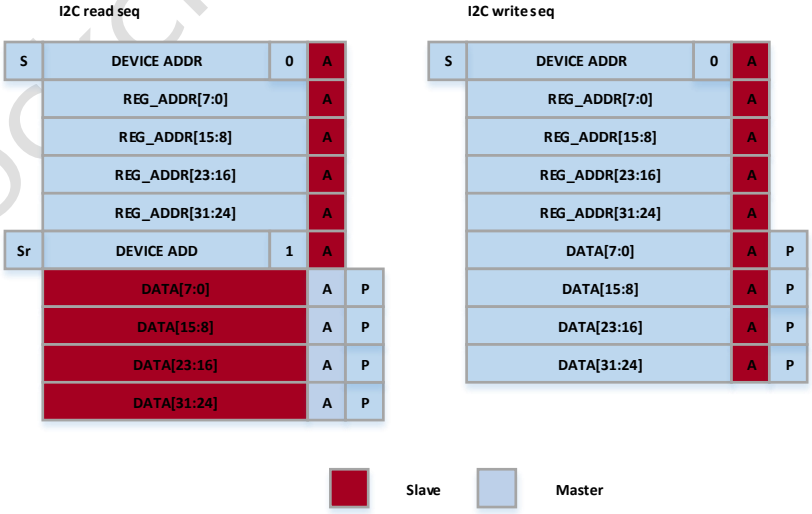

Fig. 5-4 I2C to APB single read and write

- Continuous Read Operation
  - First, AP asserts I2C start signal.
  - Second, AP sends device address (7bits) and R/W bit (1'b0). I2C slave will reply ACK when receiving the right device address. If the device address doesn't match, I2C

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slave will ignore this operation.
- Third, AP sends 4 bytes register address. Low bytes first. I2C slave replies ACK.
- Fourth, AP asserts I2C re-start signal.
- Fifth, AP sends device address (7bits) and R/W bit (1'b1). I2C slave will reply ACK when receiving the right device address.
- Sixth, I2C slave reply the 4 bytes read data. Low bytes first.
  AP replies NAK if it doesn't want to read data any more, or else replies ACK.
- Seventh, AP asserts I2C stop signal to finish this operation.

- Continuous Write Operation,
  - First, AP asserts I2C start signal.
  - Second, AP sends device address (7bits) and R/W bit (1'b0). I2C slave will reply ACK when receiving the right device address. If the device address doesn't match, I2C slave will ignore this operation.
  - Third, AP sends 4 bytes register address. Low bytes first. I2C slave replies ACK.
  - Fourth, AP sends device 4 bytes write data. Low bytes first. I2C slave replies ACK when no APB error response received, or else I2C slave replies NAK.
  - Fifth, AP continue to write the data to I2C slave.
    The I2C slave adds 0x4 to the register address automatically every 4 bytes data.
  - Fifth, AP asserts I2C stop signal to finish this operation.

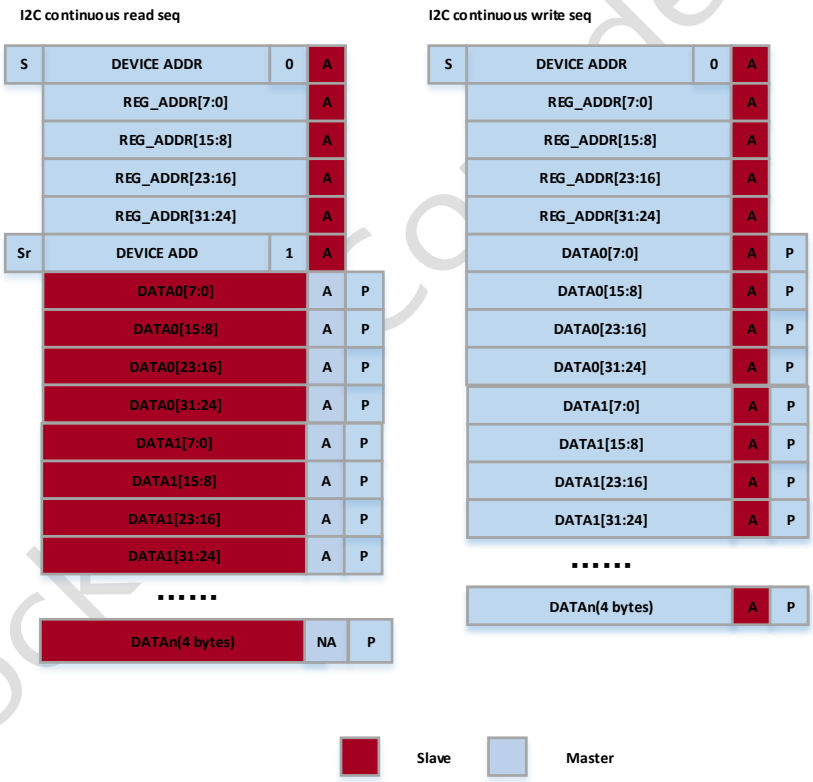

Fig. 5-5 I2C to APB continuous read and write

4.3.3 APB interface address allocation

AP can access all registers and memory through APB_BUS, so allocation suitable address space for them is very necessary. The Table 1-2 shows the allocated offset addresses of the APB interfaces on this chip.

Table 4-2 APB address allocation

Module name	Address offset
GRF_REGFILE	32'h0000_0000
COMB_RXPHY	32'h0001_0000
Reserved	32'h0002_0000
RX_HDMI	32'h0003_0000

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Module name	Address offset
TX_MIPI_CSI0	32'h0004_0000
TX_MIPI_DSI0	32'h0005_0000
TX_MIPI_DSI1	32'h0006_0000
TX_HDMI	32'h0007_0000
TX_GVI	32'h0008_0000
COMBTXPHY_CON	32'h0009_0000
TXRX_ADAPTER	32'h000a_0000
USER_EFUSE	32'h000b_0000
USER_CRU	32'h000c_0000
GPIO0	32'h000d_0000
GPIO1	32'h000e_0000
GPIO2	32'h000f_0000
GPIO3	32'h0010_0000

4.4 Interface Description

Table 4-3 I2C Slave Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2c_scl	I/O	IO_I2Cscl	GRF_GPIO0A_P[3:0]=4'b1010
i2c_sda	I/O	IO_I2Csda	GRF_GPIO3B_P[7:6]=2'b10

Notes: I=input, O=output, I/O=input/output, bidirectional

4.5 Application Notes

Considering the frequency of the pclk_i2c2apb is unstable in a period after power on and the chip reset signal release, the i2c_timeout_f、i2c_timeout_r register should not be set during this period. In normal mode, the value of the filter registers are recommended to be set to 4.

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Chapter 5 I2S

5.1 Overview

The I2S bus (Inter-IC sound bus) is a serial link for digital audio data transfer between devices in the system and be invented by Philips Semiconductor. Now it is widely used by many semiconductor manufacturers. The I2S interface is both used in RK628D RX and TX. Devices often use the I2S bus are ADC, DAC, DSP, CPU, etc. With the I2S interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.
It supports following features:

- Support HDMI RX I2S interface, up to 192kHz sample rate, 8 channel
- Support I/O I2S interface, 8 channel
- Support HDMI TX I2S interface, 8 channel
- Support the connection of RX and TX's I2S

5.2 Block Diagram

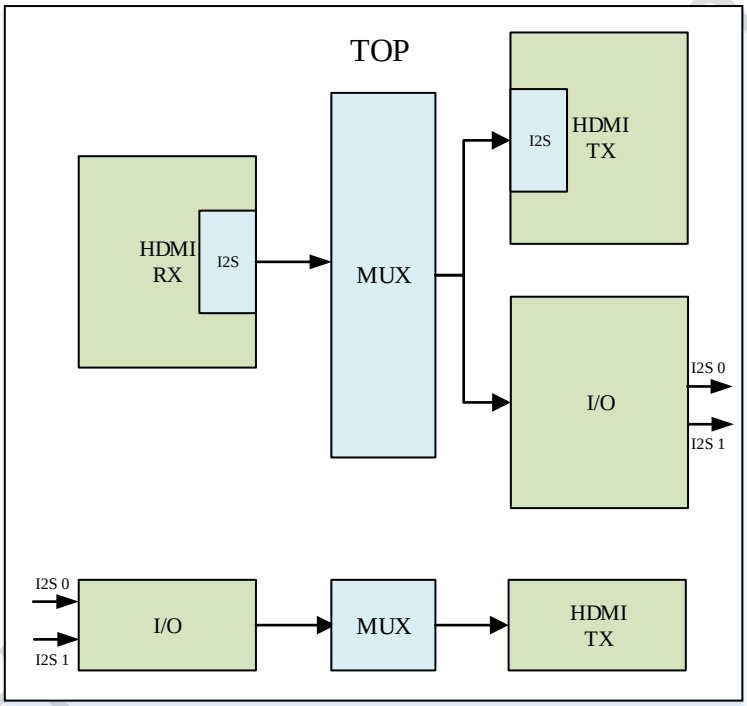

Fig. 5-1 I2S Connection Block Diagram

I/O I2S can not be used as input and output at the same time because it is a multiplexing port.

MUX
The system select which I2S works.
HDMI RX I2S
HDMI RX receive audio data and output in I2S format.
HDMI TX I2S
HDMI TX receive I2S format data and send audio package.
I/O I2S
Multiplexing port for I2S input and output on I/O.

5.3 Function description

For I2S connection, there are 4 conditions: HDMI RX I2S to HDMI TX I2S, HDMI RX I2S to I/O I2S, HDMI RX I2S both to HDMI TX and IO, I/O I2S to HDMI TX I2S.
This is the waveform of I2S normal mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes

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low to indicate left channel and high to right channel. For SD (i2s_sdo, i2s_sdi) signal, it transfers MSB or LSB first and sends the first bit one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits.

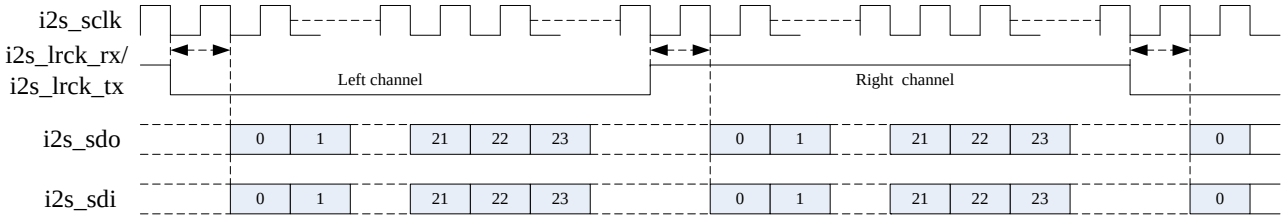

Fig. 5-2 I2S normal mode timing format

5.4 Application Notes

Select I2S channel by setting input and output mode in GRF SYSTEM_CON0 register.

Table 5-1 I2S Input mode

sw_input_mode value	mode	I2S SEL
3'b000	HDMI	HDMI I2S
Others	BT1120,RGB,YUV	I/O I2S

Table 5-2 I2S Output mode

sw_output_modevalue	mode	I2S SEL
3’b011	HDMI	HDMI TX
Others	Others	I/O I2S

5.4.1 Input Mode HDMI RX

Firstly,config audio clk.

```
word32(CRU_BASE+CRU_CLKSEL_CON05)= (0x3fc0<<16) | ((audio_freq_div&0xff)<<6);
```

The calculation formula of audio_freq_div[7:0] just like this.

freq_audio = N/(CTS/pixelclk)

audio_freq_div = (983.04/freq_audio) - 1

N and CTS is config in case，pixelclk is hdmi_rx pixelclk frequency。The critical value of audio_freq_div is 0x9f.

Secondly,config hdmirx audio controller.

```
word32(HDMI_RX_BASE+HDMI_RX_AUDPLL_GEN_CTS) = AUDIO_CTS;
word32(HDMI_RX_BASE+HDMI_RX_AUDPLL_GEN_N) = AUDIO_N;
word32(HDMI_RX_BASE+HDMI_RX_AUD_CLK_CTRL) = 0x10;
word32(HDMI_RX_BASE+HDMI_RX_AUD_PLL_CTS) = AUD_PLL_LOCK_TDIV<<24;
word32(HDMI_RX_BASE+HDMI_RX_AUD_FIFO_TH) = (0x10<<18)|(0x8<<9)|0x8;
word32(HDMI_RX_BASE+HDMI_RX_AUD_FIFO_CTRL)=(MSA_CHANNEL_DESELECT<<24)|A
FIF_SUBPACKETS<<16;
word32(HDMI_RX_BASE+HDMI_RX_AUD_SAO_CTRL)=(I2S_LPCM_BPCUV<<11)|I2S_16or3
2;
word32(HDMI_RX_BASE+HDMI_RX_AUD_MUTE_CTRL) = (APPLY_INT_MUTE<<31) |
                                             (APORT_SHDW_CTRL<<21)|
                                             (AUTO_ACLK_MUTE<<19)|
                                             (AUD_MUTE_SPEED<<10)|
                                             (0x1 <<7) |
                                             (AUD_MUTE_SEL << 5) |
                                             (AUD_MUTE_MODE << 3);
word32(HDMI_RX_BASE+HDMI_RX_AUD_PAO_CTRL)=AUD_PAO_RATE<<16;
word32(HDMI_RX_BASE+HDMI_RX_AUD_CHEXTR_CTRL)=AUD_LAYOUT_CTRL;
word32(HDMI_RX_BASE+HDMI_RX_PDEC_AUDIODET_CTRL)=AUD_DET_TH<<9;
```

5.4.2 Input Mode RGB(I2S I/O)

Attention: can not use i2s I/O out at the same time

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For I2S I/O input, the steps is described as follow.
//Config I/O
If select I2S 0 I/O
    write <GRF_BASE+SYSTEM_CON3> bit [4:2] = 0x0; //enable i2s 0 gpio
    write <GRF_BASE+GPIO0AB_SEL_CON>, set <GPIO 0a2, 0a3, 0a4, 0a5, 0a6, 0a7 sel> as I2S function
else if select I2S 1 I/O
    write <GRF_BASE+SYSTEM_CON3> bit [4:2] = 0x3; //enable i2s 1 gpio
    write <GRF_BASE+GPIO0AB_SEL_CON>, set <GPIO 1a2, 1a3, 1x4, 1a5, 1a6, 1a7 sel> as I2S function

data = reg_read(GRF_BASE + SYSTEM_CON0);
reg_write(GRF_BASE + SYSTEM_CON0) = data & (~0x3) | 0x3; //input mode: RGB;
data = reg_read(GRF_BASE + SYSTEM_CON0);
reg_write(GRF_BASE + SYSTEM_CON0) = data | 0x400; //bit10 set 1, I2S GPIO direction is input;

5.4.3 Output Mode RGB(I2S I/O)

Attention: can not use i2s I/O in at the same time
For I2S I/O output, the steps is described as follow.
//Config I/O
If select I2S 0 I/O
    write <GRF_BASE+SYSTEM_CON3> bit [4:2] = 0x0; //enable i2s 0 gpio
    write <GRF_BASE+GPIO0AB_SEL_CON>, set <GPIO 0a2, 0a3, 0a4, 0a5, 0a6, 0a7 sel> as I2S function
else if select I2S 1 I/O
    write <GRF_BASE+SYSTEM_CON3> bit [4:2] = 0x3; //enable i2s 1 gpio
    write <GRF_BASE+GPIO0AB_SEL_CON>, set <GPIO 1a2, 1a3, 1x4, 1a5, 1a6, 1a7 sel> as I2S function

reg_write(GRF_BASE + SYSTEM_CON) = xxx; //output mode: RGB, BT1120, MIPI, etc

reg_write(GRF_BASE + SYSTEM_CON) = data | (~0x400); //bit10 set 0, I2S GPIO direction is output;

5.4.4 Output Mode HDMI TX

Refer to HDMI TX PHY_full document.
I2S I/O can output at the same time when set HDMI TX output mode. Enable I2S GPIO as 1.5.3.

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Chapter 6 COMB RX PHY

6.1 Overview

HDMI RX IP is composed of the physical and the PHY logic.The physical layer contains 3 data channels,a clock channel and bias circuit .The data channel consists of termination, level-shifter, equalizer circuit.
In each data channel, the terminal provides common mode voltage and termination resistance for the differential pair at the receiver end. The level-shifter changes the common mode voltage of input signals from the termination supply domain to a proper level that satisfies the input voltage range of equalizer.The input signals are reshaped by equalizer for frequency compensation. Then the serial stream is recovered by CDR and converted to 10-bit parallel output.
The PHY logic receives the recovered parallel data and clock signals of 4 data channels. These data are firstly synchronized to the same clock, then aligned to eliminate the channel skew and finally output to the controller for further process.
It supports following features:

- Compliant with HDMI2.0 specifications
- Support clock input up to 297MHz
- Support data input up to 2.97Gbps per data channel
- Typical 24MHz/27MHz reference clock
- Support termination connected to 3.3V supply
- Support 10-bit parallel output up to 297MHz for each data lane
- Support automatic termination resistance and offset calibration
- Support equalizer gain adaption
- Support BIST logic
- APB slave interface for internal register access
- Built-in bandgap reference
- 3.3V IO supply and 1.1V core supply
- SMIC 40nmLL1P7M process
- Area:1120umx1120um including IO and ESD
- Power consumption: typical 300mW@2.97Gbps

6.2 Block Diagram

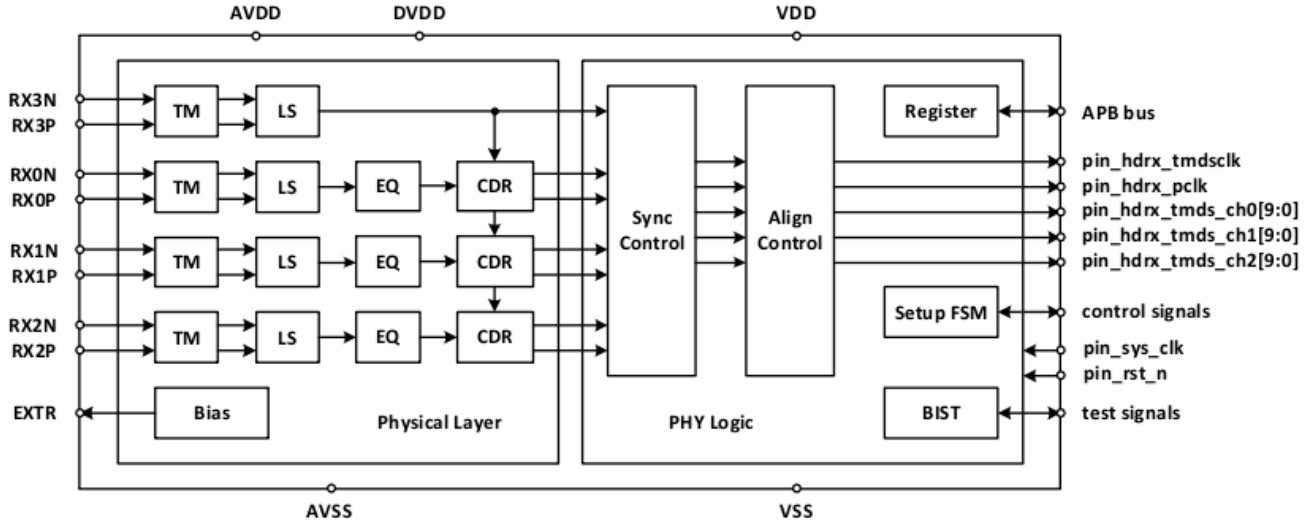

Fig. 6-1 COMB RX PHY Diagram

The block diagram of COMB RX PHY is shown in Fig 1-1, which integrates complete physical layer and PHY logic to recover and output video, audio data.

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6.3 Function description

The physical layer contains 3 data channels,1 clock channel and bias circuit. The clock channel receives the TMDS clock with the frequency up to 340MHz. The other 3 data channel receive TMDS data to form a TMDS link in combination with the clock channel. The data rate is up to 2.97Gbps.
Each data channel consists of termination,level-shifter and equalizer circuit. The termination provides termination voltage and resistance for the differential pair at the receiver end. The link connection is typical DC-coupled and the two 50Ω termination resistors are connected to 3.3V supply,which results in a common mode voltage around 3.0V.
The level-shifter changes the common mode voltage of input signals from the termination voltage domain to a proper level that satisfies the input voltage range of equalizer.The level-shifter circuit shifts the common mode voltage from 3.3V power domain to the 1.1V power domain.

Equalizer amplifies high frequency portion of input signals to compensate the channel loss and increases the sampling window for CDR.CDR tracks the input data phase and generates sampling clocks to recover the serial data.The recovered serial data are then converted to 10bit parallel output. In each data channel,CDR outputs 10bit parallel data and a synchronous clock with the same frequency to PHY logic.
The CDR reference clock for 3 data channels is generated by TMDS clock received from the clock channel.
The PHY logic receives the recovered parallel data and synchronous clocks from multiple data channels. These data are firstly synchronized to the same clock and then aligned to eliminate the channel skew. PHY logic outputs 3-channel,10bit parallel data,tmds clock and pixel clock to the HDMI receiver controller.
The PHY logic also contains a setup finite state machine(FSM)to control the PHY operation after power up, including mode control,PHY configuration,termination resistance calibration,offset calibration and equalizer gain adaption.

6.4 Register Description

This section describes the control/status registers of the design.

6.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
COMBRXPHY_REG6600	0x6600	W	0x80020000	BG clock controller
COMBRXPHY_REG6608	0x6608	W	0x00000000	rx phy controller reg1
COMBRXPHY_REG660c	0x660c	W	0xde03a000	rx phy controller reg2
COMBRXPHY_REG6614	0x6614	W	0x00000000	rx phy equ ctrl0
COMBRXPHY_REG6618	0x6618	W	0x00000000	rx phy equ ctrl1
COMBRXPHY_REG661c	0x661c	W	0x00000000	rx phy equ ctrl2
COMBRXPHY_REG6624	0x6624	W	0x0e07a120	rx phy bias cnt and freq div low
COMBRXPHY_REG6628	0x6628	W	0x07a12081	rx phy det load cnt and freq div high
COMBRXPHY_REG662c	0x662c	W	0x00000000	rx phy pll div
COMBRXPHY_REG6630	0x6630	W	0x00000000	rx phy pll ctrl
COMBRXPHY_REG6654	0x6654	W	0x00000000	rx phy clock freq
COMBRXPHY_REG66a0	0x66a0	W	0x00000003	rx phy ana ctrl
COMBRXPHY_REG66a4	0x66a4	W	0x00000000	rx phy pll input data cap0

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Name	Offset	Size	Reset Value	Description
COMBRXPHY_REG66a8	0x66a8	W	0x00000000	rx phy pll input data cap1
COMBRXPHY_REG66ac	0x66ac	W	0x00000000	rx phy pll input data ctrl
COMBRXPHY_REG66b0	0x66b0	W	0x00000000	rx phy pll input data fifo ctrl
COMBRXPHY_REG66b4	0x66b4	W	0x00000000	rx phy pll lane status0
COMBRXPHY_REG66b8	0x66b8	W	0x00000000	rx phy pll lane status1
COMBRXPHY_REG66e8	0x66e8	W	0x00000000	rx phy pll lane status2
COMBRXPHY_REG66f0	0x66f0	W	0x00000300	rx phy rst ctrl0
COMBRXPHY_REG66f4	0x66f4	W	0x00000001	rx phy rst ctrl1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

6.4.2 Detail Register Description

COMBRXPHY_REG6600

Address: Operational Base + offset (0x6600)

Bit	Attr	Reset Value	Description
31	RW	0x1	BG_clock_enable Enable BG clock
30:16	RW	0x0002	BG_clock_divider BG clock divider,frequency of bg = sys_clk/bg_divider[14:0]
15:0	RO	0x0	reserved

COMBRXPHY_REG6608

Address: Operational Base + offset (0x6608)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	reference_clock_sel HDMI RX PHY reference clock is 27M,Active high,default is 24M
24	RW	0x0	extern_load_detect_en Extern load detect enable,active high
23:20	RW	0x0	equ_peak2 4'b0000：min high frequency boost ... 4'b1111：max high frequency boost
19:16	RW	0x0	equ_peak1 4'b0000：min high frequency boost ... 4'b1111：max high frequency boost
15:12	RO	0x0	reserved
11:8	RW	0x0	equ_peak0 4'b0000：min high frequency boost ... 4'b1111：max high frequency boost
7:0	RO	0x0	reserved

COMBRXPHY_REG660c

Address: Operational Base + offset (0x660c)

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Bit	Attr	Reset Value	Description
31:16	RW	0xde03	load_detect_clock_counter_length load detect clock domain counter length for load detection
15:0	RW	0xa000	ref_clock_counter_length reference clock domain counter length for load detection

COMBRXPHY_REG6614
Address: Operational Base + offset (0x6614)
rx phy equ ctrl0

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	equ_bias1 2'b00: min bias current ... 2'b11: max bias current
23:18	RO	0x0	reserved
17:16	RW	0x0	equ_bias0 2'b00: min bias current ... 2'b11: max bias current
15:0	RO	0x0	reserved

COMBRXPHY_REG6618
Address: Operational Base + offset (0x6618)
rx phy equ ctrl1

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x0	equ_gain2 4'b0000: min high frequency gain ... 4'b1111: max high frequency gain
19:16	RW	0x0	equ_gain1 4'b0000: min high frequency gain ... 4'b1111: max high frequency gain
15:12	RO	0x0	reserved
11:8	RW	0x0	equ_gain0 4'b0000: min high frequency gain ... 4'b1111: max high frequency gain
7:2	RO	0x0	reserved
1:0	RW	0x0	equ_bias2 2'b00: min bias current ... 2'b11: max bias current

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COMBRXPHY_REG661c
Address: Operational Base + offset (0x661c)
rx phy equ ctrl2

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	equ_dc2 4'b0000：min low frequency gain ... 4'b1111：max low frequency gain
15:12	RW	0x0	equ_dc1 4'b0000：min low frequency gain ... 4'b1111：max low frequency gain
11:8	RO	0x0	reserved
7:4	RW	0x0	equ_dc0 4'b0000：min low frequency gain ... 4'b1111：max low frequency gain
3:0	RO	0x0	reserved

COMBRXPHY_REG6624
Address: Operational Base + offset (0x6624)

Bit	Attr	Reset Value	Description
31:24	RW	0x0e	reg_cal1_freqdiv_low_8bit reg_cal1_freqdiv[7:0]
23:0	RW	0x07a120	reg_bias_cnt reg_bias_cnt it is time to turn on the bias circuit

COMBRXPHY_REG6628
Address: Operational Base + offset (0x6628)

Bit	Attr	Reset Value	Description
31:8	RW	0x07a120	reg_det_load_cnt time to detect overload
7:0	RW	0x81	reg_cal1_freqdiv_high_7bit reg_cal1_freqdiv[14:8] for termination resistance calibration,reg_cal1_freqdiv controls its frequency at 100kHz,it related to pin_sys_clk. for example: for 27MHz pin_sys_clk,reg_cal1_freqdiv should set to 15'd270. for 24MHz pin_sys_clk,reg_cal1_freqdiv should set to 15'd240.

COMBRXPHY_REG662c
Address: Operational Base + offset (0x662c)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	pll_fbdiv pll fbdiv[8:0],the ch0/1/2 tmds_clk= (ch3_tmds_clk*fbdiv[8:0])/pre_div[4:0],in normal 10bit rate = ch3_tmds_clk, however bit rate>3.4G,10bit rate = ch3_tmds_clk*4,so in this case the pll need configure by manual, and reg30[3]should be 1'b1.
23:17	RO	0x0	reserved
16:8	RW	0x000	pll_pre_div pll pre_div[4:0]
7:0	RO	0x0	reserved

COMBRXPHY_REG6630
Address: Operational Base + offset (0x6630)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x1	reg_pll_cfg_manually 1:manually 0:auto
2:0	RO	0x0	reserved

COMBRXPHY_REG6654
Address: Operational Base + offset (0x6654)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RO	0x00	ch3_clock_freq HDMI rx phy detect rx3p clock frequency 5'd31:Error mode 5'd30:manual mode detected 5'd18:rx3p clock = 297M 5'd17:rx3p clock = 162M 5'd16:rx3p clock = 148.5M 5'd15:rx3p clock = 135M 5'd14:rx3p clock = 119M 5'd13:rx3p clock = 108M 5'd12:rx3p clock = 101M 5'd11:rx3p clock = 92.8125M 5'd10:rx3p clock = 88.75M 5'd9:rx3p clock = 85.5M 5'd8:rx3p clock = 83.5M 5'd7:rx3p clock = 74.25M 5'd6:rx3p clock = 68.25M 5'd5:rx3p clock = 65M 5'd4:rx3p clock = 59.4M 5'd3:rx3p clock = 40M 5'd2:rx3p clock = 33.75M 5'd1:rx3p clock = 27M 5'd0:rx3p clock = 25.17M
15:0	RO	0x0	reserved

COMBRXPHY_REG66a0
Address: Operational Base + offset (0x66a0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	input_ch0_data external input channel0 data[7:0]
23	RW	0x0	input_data_en external input data enable
22:17	RO	0x0	reserved
16	RW	0x0	tmds_valid_en external tmds_valid enable
15:10	RO	0x0	reserved
9	RW	0x0	pclk_invert_en pin_hdrx_pclk invert enable,active high
8	RW	0x0	tmdsclk_invert_en pin_hdrx_tmdsclk invert enable,active high
7	RW	0x0	phy_fifo_reset hdmi rx phy fifo reset,active low
6:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x1	phy_digital_soft_reset hdmi phy phy digital soft reset,active low
0	RW	0x1	phy_analog_soft_reset hdmi phy analog soft reset,active low

COMBRXPHY_REG66a4
Address: Operational Base + offset (0x66a4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	input_ch2_data_low_bit extern input channel2 data[7:0]
23:18	RO	0x0	reserved
17:16	RW	0x0	input_ch1_data_high_bit extern input channel 1 data[9:8]
15:8	RW	0x00	input_ch1_data_low_8bit extern input channel 1 data[7:0]
7:2	RO	0x0	reserved
1:0	RW	0x0	input_ch0_data_high_bit extern input channel0 data[9:8]

COMBRXPHY_REG66a8
Address: Operational Base + offset (0x66a8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:13	RW	0x0	ch_clk_select channel clock select 3'bx0x:ch3 tmds clock when rate > 3.4G this clock should not be selected 3'b01x:ch2 tmds clock 3'b110:ch0 tmds clock 3'b111:ch1 tmds clock
12:11	RO	0x0	reserved
10:8	RW	0x0	clk_out_ch_select pixel clock output channel select 3'bx0x:ch0 tmds clock 3'b11x:tmds clock div2 3'b010:tmds clock div1.5 3'b011:tmds clock div1.25
7:2	RO	0x0	reserved
1:0	RW	0x0	input_ch2_data_high_bit extern input channel 2 data[9:8]

COMBRXPHY_REG66ac
Address: Operational Base + offset (0x66ac)

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Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	input_data_lsb_msb_reverse input 10bit data from lsb to msb reverse
22	RW	0x0	ouput_data_lsb_msb_reverse output 10bit data from lsb to msb reverse
21:20	RO	0x0	reserved
19	RW	0x0	ch2_ch0_data_exchange ch2 and ch0 data exchange
18	RW	0x0	ch2_data_invert ch2 data invert by bit
17	RW	0x0	ch1_data_invert ch1 data invert by bit
16	RW	0x0	ch0_data_invert ch0 data invert by bit
15:0	RO	0x0	reserved

COMBRXPHY_REG66b0
Address: Operational Base + offset (0x66b0)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	rx_phy_fifo_rd_en hdmi rx phy fifo read enable,active high.
20	RW	0x0	rx_phy_fifo_wr_en hdmi rx phy fifo write enable,active high
19:0	RO	0x0	reserved

COMBRXPHY_REG66b4
Address: Operational Base + offset (0x66b4)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RO	0x0	ch1_lock_status ch1 lock status,active high
24	RO	0x0	ch1_time_out_status ch1 not lock and time out status,active high
23:16	RO	0x00	ch1_stable_lock_count ch1 stable lock count
15:10	RO	0x0	reserved
9	RO	0x0	ch0_lock_status ch0 lock status, active high
8	RO	0x0	ch0_time_out_status ch0 not lock and time out status,active high
7:0	RO	0x00	ch0_stable_lock_count ch0 stable lock count

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COMBRXPHY_REG66b8
Address: Operational Base + offset (0x66b8)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RO	0x0	ch2_lock_status ch2 lock status,active high
8	RO	0x0	ch2_time_out_status ch2 not lock and time out status,active high
7:0	RO	0x00	ch2_stable_lock_count ch2 stable lock count

COMBRXPHY_REG66e8
Address: Operational Base + offset (0x66e8)
rx phy pll lane status2

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	i_ch2_phase_err i_ch2_phase_err status
12	RW	0x0	i_ch1_phase_err i_ch1_phase_err status
11	RW	0x0	i_ch0_phase_err i_ch0_phase_err status
10	RW	0x0	i_ch2_lock_err i_ch2_lock_err status
9	RW	0x0	i_ch1_lock_err i_ch1_lock_err status
8	RW	0x0	i_ch0_lock_err i_ch0_lock_err status
7:6	RO	0x0	reserved
5	RW	0x0	i_ch2_empty i_ch2_empty status
4	RW	0x0	i_ch2_full i_ch2_full status
3	RW	0x0	i_ch1_empty i_ch1_empty status
2	RW	0x0	i_ch1_full i_ch1_full status
1	RW	0x0	i_ch0_empty i_ch0_empty status
0	RW	0x0	i_ch0_full i_ch0_full status

COMBRXPHY_REG66f0
Address: Operational Base + offset (0x66f0)

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Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	obs_mux 8'h00 :obs_clk_i = ad_rx_tmdsclk_ch0 ; 8'h01 :obs_clk_i = ad_rx_tmdsclk_ch1 ; 8'h02 :obs_clk_i = ad_rx_tmdsclk_ch2 ; 8'h03 :obs_clk_i = ad_rx_clk20_ch3 ; 8'h04 :obs_clk_i = ad_rx_pclk_div6p25 ; 8'h05 :obs_clk_i = ad_rx_pclk_div7p5 ; 8'h06 :obs_clk_i = ad_rx_tmdsclk_ch3 ; 8'h07 :obs_clk_i = w_out_data_vld ; 8'h08 :obs_clk_i = da_pll_refclk ; others : obs_clk_i = da_pll_refclk;
15	RO	0x0	reserved
14	RW	0x0	equ_rstn2 equ_reset2 1:normal 0:reset
13	RW	0x0	equ_rstn1 equ_reset1 1:normal 0:reset
12	RW	0x0	equ_rstn0 equ_reset0 1:normal 0:reset
11	RW	0x0	rx_sample_rstn2 rx_sample_reset2 1:normal 0:reset
10	RW	0x0	rx_sample_rstn1 rx_sample_reset1 1:normal 0:reset
9	RW	0x1	rx_sample_rstn0 rx_sample_reset0 1:normal 0:reset
8	RW	0x1	ana_rstn reg_ana_rstn 1:normal 0:reset
7:3	RO	0x0	reserved
2:1	RW	0x0	hdmi_mode 2'b10: hdmi mode

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Bit	Attr	Reset Value	Description
0	RW	0x0	auto_setup_en 1:enable 0:disable

COMBRXPHY_REG66f4
Address: Operational Base + offset (0x66f4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	reg_hd_rstn reg_hd_rstn reset hdmi module 1:normal 0:reset

6.5 Application Notes

6.5.1 Initial Steps For HDMI Mode

The power up configuration of inno HDMI RX PHY IP is described as follow:
Step1: clk detect
rd_op(0x6620, clk_detect_value);
if (clk_detect_value == 0x0)
{
rd_op(0x6620, clk_detect_value);
}
And retry 10 times or more.
In normal operation,clk_detect_value will be 0x6666 or 0x6565,and it indicates the termination impedance value,and it has detected clk.
If ((clk_detec_value[7:0] == 0x0) || (clk_detec_value[15:8] == 0x0) ||
((clk_detec_value[23:16] == 0x0) || (clk_detec_value[31:24] == 0x0)),
it indicates that clk detection fail.

Step2: get cdr_mode and cdr_data.
rd_op(0x6654,cdr_data_value);
cdr_data_value[15:0] is cdr_data, it indicates the clk frequency value.
read 0x6654 100 times, and get the max value of cdr_data_value[15:0]:cdr_data_max
and the min value of cdr_data_value[15:0]:cdr_data_min.
if ((cdr_data_max - cdr_data_min <= CLK_STABLE_THRESHOLD) && (cdr_data_min >= 60)), clock is stable.
read 0x6654 again,0x6654[21:16] is cdr_mode,if cdr_mode is 0x1f,it indicates that clock error.
//CLK_STABLE_THRESHOLD is configurable,the current parameter is 6.
Step3: configure PLL manually
wr_op(0x662c,0x01000500);
wr_op(0x66a8,0x0000c600);
tmds_bitrate_per_lane = cdr_mode_to_khz[cdr_mode] * 10;
if (tmds_bitrate_per_lane < 400000)
pll_man = 0x7960c;
else if (tmds_bitrate_per_lane < 600000)
pll_man = 0x7750c;
else if (tmds_bitrate_per_lane < 800000)
pll_man = 0x7964c;

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```
        else if (tmds_bitrate_per_lane < 1000000)
              pll_man = 0x7754c;
        else if (tmds_bitrate_per_lane < 1600000)
              pll_man = 0x7a108;
        else if (tmds_bitrate_per_lane < 2400000)
              pll_man = 0x73588;
        else if (tmds_bitrate_per_lane < 3400000)
              pll_man = 0x7a108;
        else
              pll_man = 0x7f0c8;

        wr_op(0x6630, pll_man);
```

The definition of cdr_mode_to_khz[] just like this.

```
const u32 cdr_mode_to_khz[] = {25170, 27000, 33750, 40000, 59400, 65000, 68250,
74250, 83500, 85500, 88750, 92812, 101000, 108000, 119000, 135000, 148500,
162000, 297000};
```

Step4: search and configure EQ and edge sample

Step4.1: set sample edge mode for channel 0~2.

```
wr_op(0x6634[15:4], 0x0);
```

Step4.2: select channel.

```
wr_op(0x6700[1:0], 0x0); //select channel0
wr_op(0x6700[1:0], 0x1); //select channel1
wr_op(0x6700[1:0], 0x2); //select channel2
wr_op(0x6730[15:0], 0x1); //configure sample_time_cnt
```

Step4.3: configure sample edge and channel dc gain

```
if(cdr_mode<16)
{
    dc_gain = 0x0;
    rd_offset = 0x0;
}
else if (cdr_mode<18)
{
    dc_gain = 0x1;
    rd_offset = 0x0;
}
else
{

    dc_gain = 0x3;
    rd_offset = 0x2;
}
if (cdr_mode <= 1) //27M vic17 720x576p50
{
    edge = 864*625;
}
else if (cdr_mode <= 4) //59.4M vic81 1680x720p30
{
    edge = 2640*750;
}
else if (cdr_mode <= 7) //74.25M vic34 1920x1080p30
{
    edge = 2200*1125;
}
else if (cdr_mode <= 14) //119M vic88 2560x1180p30
{
    edge = 3520*1125;
```

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```
}
else if (cdr_mode <= 16) //148.5M vic31 1920x1080p50
{
    edge = 2640*1125;
}
else if (cdr_mode <= 17) //162M vic89 2560x1080p50
{
    edge = 3300*1125;
}
else if (cdr_mode <= 18) //297M vic95 3840x2160p30
{
    edge = 4400*2250;
}
else //default 148.5M vic16 1920x1080p60
{
    edge = 2200*1125;
}
wr_op(0x6700[1:0], 0x0); //select channel0
wr_op(0x6708,edge);
wr_op(0x6700[1:0], 0x1); //select channel1
wr_op(0x6708,edge);
wr_op(0x6700[1:0], 0x2); //select channel2
wr_op(0x6708,edge);
wr_op(0x661c[7:4],dc_gain); //channel2 configure dc gain
wr_op(0x661c[15:12],dc_gain); //channel1 configure dc gain
wr_op(0x661c[23:20],dc_gain); //channel0 configure dc gain
Step4.4: search for the best EQ value
    Step4.4.1: set sample edge round value n,n=0~5
    wr_op(0x6618[11:8],n); //config equ_gain_ch2
wr_op(0x6618[19:16],n); //config equ_gain_ch1
wr_op(0x6618[23:20],n); //config equ_gain_ch0
    Step4.4.2: start sample edge
    wr_op(0x66f0[11:9],0x0); //channel0~2 sample reset
wr_op(0x66f0[11:9],0x7); //
    delay(41ms);//wait for more than one frame.
Step4.4.3: get data of round n
    wr_op(0x6700,ch); //select channel
    rd_op(0x6740,data[0]);//get data of round
    rd_op(0x6744,data[1]);//get data of round
    ...
    rd_op(0x6780,data[15]);//get data of round
    data_in[0]  = data[0];
data_in[1]  = data[7];
data_in[2]  = data[13];
data_in[3]  = data[14];
data_in[4]  = data[15];
data_in[5]  = data[1];
data_in[6]  = data[2];
data_in[7]  = data[3];
data_in[8]  = data[4];
data_in[9]  = data[5];
data_in[10] = data[6];
data_in[11] = data[8];
data_in[12] = data[9];
data_in[13] = data[10];
data_in[14] = data[11];
data_in[15] = data[12];
```

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Step4.4.4: get the max data of round n

```
    //search for the max data_in[]
for (i = 0; i < 16; i++) {
        if (max_v < data_in[i])
            max_v = data_in[i];
    }
    //calculate the max_cnt
    for (i = 0; i < 16; i++) {
        if (data_in[i] == 0)
            cnt = cnt + 200;
        else if ((data_in[i] > 0) && (data_in[i] < 100))
            cnt = cnt + 100 - data_in[i];
    }
    max_cnt = (cnt >= 3200) ? 0 : cnt;
    max_zero[n] = max_cnt;
    max_val[n] = max_v;
```

channel0/channel1/channel2 has its max_zero[n] and max_val[n].

Loop 4.4.1Step ~ 4.4.4Step for 6 times,and every channel has six result, max_zero[0]~max_zero[5],max_val[0]~max_val[5].

Step4.4.5: get the final max data for each channel

```
for (i = 0; i < 6; i++) {
        if (rd_max_zero[i] > max) {
            max = rd_max_zero[i];
            max_v = rd_max_val[i];
            rd = i;
        } else if (rd_max_zero[i] == max && rd_max_val[i] > max_v) {
            max = rd_max_zero[i];
            max_v = rd_max_val[i];
            rd = i;
        }
}
```

ch_round[0] = rd[0], ch_round[1] = rd[1], ch_round[2] = rd[2].

The rd[ch] is the best EQ for each channel.

Step4.5: Configure the best EQ

```
wr_op(0x6618[11:8],ch_round[2]);
wr_op(0x6618[19:16],ch_round[0]);
wr_op(0x6618[23:20],ch_round[1]);
```

Step4.6: start sample edge

```
wr_op(0x66f0[11:9],0x0); //channel0~2 sample reset
wr_op(0x66f0[11:9],0x7); //
delay(41ms);//wait for more than one frame.
```

Step5:Deassert fifo reset,enable fifo write and read

```
        wr_op(0x66a0,0x3);//reset rxphy infifo
        wr_op(0x66b0,0x00080060);//rxphy infifo wr/rd disable
wr_op(0x66a0,0x83);//deassert rxphy infifo reset
wr_op(0x66b0,0x00380060);//enable rxphy infifo wr/rd en
delay(6ms);
```

Step6: check all 3 data channel alignment

```
        count = 0;
        for (i = 0; i < 100; i++) {
            delay(1ms);
            rd_op(0x66b4, data_a);
            rd_op(0x66b8, data_b);
            /* ch0 ch1 ch2 lock */
            if ((data_a[7:0] == 0xff) && (data_a[23:16] == 0xff) &&
                (data_b[7:0] == 0xff)) {
                count++;
```

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```
            }
        }

 if (count >= 100) {
            printf("channel alignment done\n");
            printf("rx initial done\n");
            ret = 0;
        } else if (count > 0) {
            printf("link not stable, count:%d of 100\n", count);
            ret = 0;
        } else {
            printf("channel alignment failed!\n");
            ret = -1;
        }

        return ret;
```

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Chapter 7 COMB TX PHY

7.1 Overview

GVIMIPIS40LL is designed for chips that perform high bandwidth data communication while operating at low power consumption. It can be easily fabricated and implemented in a GVI, LVDS or MIPI DSI system.
For GVI/LVDS system, Macro consists of multi-transmitter channels and one SU unit. The speed of transmitter macro is up to 3.75Gbps and can be configured to GVI or LVDS mode.
Features:

- GVI
  - Support data rate:0.5~3.75Gbps
  - Configurable reference clock frequency
  - Per-lane 10-bit/9-bit/8-bit/7-bit parallel interface
  - Support Spread Spectrum clock generation: up to±5000ppm@31.5Khz
  - AC coupling, 75nf~200nF at both ends and one end in TX near-end
  - One shared PLL for all lanes
  - Individually power down for each lane
  - Support 0~9dB programmable 2-tap FFE(Feed forward equalization)
- LVDS
  - Support data rate: 0.25~1.0Gbps
  - Configurable reference clock frequency
  - Per-lane 10-bit/9-bit/8-bit/7-bit parallel interface
  - DC coupling
  - One shared PLL for all lanes
  - Individually power down for each lane
  - Support 0~9dB programmable 2-tap FFE(Feed forward equalization)
- MIPI DSI
  - One clock lane channel and four Data Channels
  - Data Channel 0: Bi-directional with Low-Power RX(LP-RX) and Low-Power CD(LP-CD)
  - Channel1~4: High-Speed TX(HS-TX) and a low-Power TX(LP-TX)
  - HS operation rate: 0.1875~1.2Gps
  - LP operation rate: 10Mbps
  - DC coupling
  - One shared PLL for all lanes
  - Contention detection module
- Common Features
  - Embedded BIST
  - Support wire bonding package
  - Reliability
    - Life time: 20 years, with average temperature up to 100degC
      10 years, with average temperature up to 110degC
    - Availability: 100%
    - ESD(HBM): over 2000V
    - ESD(CDM): over 500V
    - Latch-up: >100mA

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7.2 Block Diagram

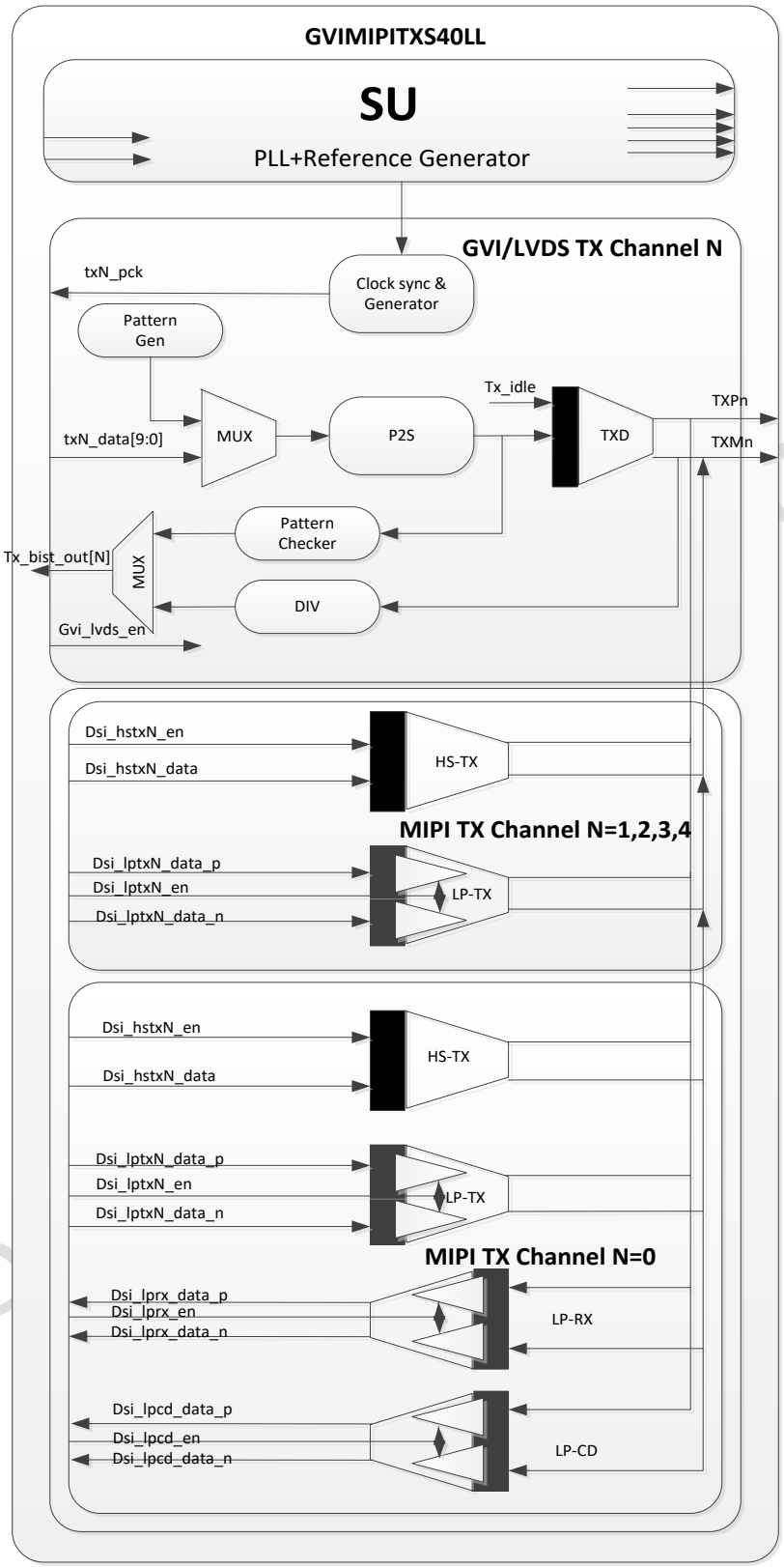

Fig. 7-1 Comb PHY TX Block Diagram

7.3 Function

7.3.1 SU

PLL takes input reference clock to generate a high speed clock for high speed data transmission. The high speed clock generated by PLL will be SSC(spectrum spread clock) modulated if SSC

mode is turned on. The VCO operation frequency is decided by reference clock frequency, reference clock pre-divider's factor and PLL loop-divider's factor.
The reference generator includes a voltage and current reference generator, which comprise a Bandgap Reference and a Voltage Regulator. Reference voltage and current are generated for internal circuit usage, no off-chip components are needed for this reference generator. This block is physically located in PLL, GVI/LVDS and MIPI channels will share the same reference generator block. The reference generator block is always on as long as IP power up, it will consume 90us@3.3V static current all the time.

7.3.2 GVI/LVDS Transmitter

The P2S block convert parallel data txN_data to high speed serial data by using high speed clock generated by PLL.
TX driver will convert the serial data to differential signal on TXPn/TXMn. The differential output amplitude and Pre-emphasis level can be programmed. Also a 2-tap pre-emphasis is in the TX driver for ISI compensation.
The block includes an internal loopback for check the main function of the TX. A divider to divide D10.2 signal from driver output for verify the driver function.

7.3.3 MIPI DSI Configuration

The MIPI DSI channel-0 data TX module includes follows blocks:

- HS-TX
- LP-TX
- LP-RX
- Low-Power contention detector(LP-CD)

7.4 Register Description

7.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

7.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
COMBTXPHY_CON_COMBTXPHY_CON	0x0000	W	0x00000010	COMB PHY TX control register
COMBTXPHY_CON_COMBTXPHY_AMP_SCAL	0x0004	W	0x01550155	The amplitude scale control
COMBTXPHY_CON_COMBTXPHY_AMP	0x0008	W	0x36db36db	The adjustment for the amplitude level
COMBTXPHY_CON_COMBTXPHY_EMP_C0	0x000c	W	0x00000000	The adjustment for the emphasis level of the driver(N=0~4)
COMBTXPHY_CON_COMBTXPHY_EMP_C1	0x0010	W	0x00000000	The adjustment for the emphasis level of the driver(N=5~9)
COMBTXPHY_CON_COMBTXPHY_PLL_DIV	0x0014	W	0x00004000	COMB PHY TX PLL divider
COMBTXPHY_CON_COMBTXPHY_PLL_CTRL0	0x0018	W	0x00000000	COMB PHY TX control register6
COMBTXPHY_CON_COMBTXPHY_PLL_CTRL1	0x001c	W	0x00100000	COMB PHY TX control register7
COMBTXPHY_CON_COMBTXPHY_SSC	0x0020	W	0x00018d00	COMB PHY TX SSC FUNCTION
COMBTXPHY_CON_COMBTXPHY_DSI_CTRL	0x0024	W	0x00000000	COMB PHY TX control register for DSI

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Name	Offset	Size	Reset Value	Description
COMBTXPHY_CON_COMBTXPHY_CLK_DRV	0x0028	W	0x00000000	COMB PHY LVDS TX channel-n clk enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

7.4.3 Detail Register Description

COMBTXPHY_CON_COMBTXPHY_CON

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_tx_idle Force the high speed differential signal to common mode，this signal can be set during IP power up stage to prevent unexpected leakage current in TXP/TXM 1'b0: Normal operation 1'b1: Force TXPn/TXMn to common mode
19:18	RO	0x0	reserved
17:8	RW	0x000	sw_tx_pd Power down control signal of channel N=0~9 1'b0: Normal operation 1'b1: Power down channel
7	RO	0x0	reserved
6:5	RW	0x0	sw_bus_width Parallel data bus width select 2'b00: 10-bit parallel data 2'b01: 9-bit parallel data, data[9] can be arbitrary state 2'b10: 8-bit parallel data, data[9:8] can be arbitrary state 2'b11: 7-bit parallel data, data[9:7] can be arbitrary state
4	RW	0x1	sw_pd_pll Shared PLL block power down signal 1'b0:Normal operation 1'b1:Power down PLL (a) In GVI/LVDS mode, all channels are not working (b) In MIPI DSI mode, channels are not controlled by pd_pll
3	RW	0x0	sw_gvi_lvds_en Enable GVI/LVDS operation mode 1'b0 : disable 1'b1 : enable
2	RW	0x0	sw_mipi_dsi_en Enable MIPI DSI operation mode 1'b0 : disable 1'b1 : enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_moduleb_en Enable all 5-channel of CombTXPHYb 1'b0: Disable Module-B channels, the output of TXPn/TXMn is Hi-Z 1'b1: Enable Module-B channels (Module-B includes channel N=5,6,7,8,9)
0	RW	0x0	sw_modulea_en Enable all 5-channel of CombTXPHYa 1'b0: Disable Module-A channels,the output of TXPn/TXMn is Hi-Z 1'b1: Enable Module-A channels (Module-A includes channel N=0,1,2,3,4)

COMBTXPHY_CON_COMBTXPHY_AMP_SCAL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x1	sw_tx9_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
23:22	RW	0x1	sw_tx8_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
21:20	RW	0x1	sw_tx7_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
19:18	RW	0x1	sw_tx6_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
17:16	RW	0x1	sw_tx5_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
15:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	sw_tx4_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
7:6	RW	0x1	sw_tx3_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
5:4	RW	0x1	sw_tx2_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
3:2	RW	0x1	sw_tx1_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%
1:0	RW	0x1	sw_tx0_amp_scale The amplitude scale factor control 2'b00: Scale down the output amplitude to 75% 2'b01/10: Keep the output amplitude 2'b11: Scale up the output amplitude to 125%

COMBTXPHY_CON_COMBTXPHY_AMP

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x3	sw_tx9_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
27:25	RW	0x3	sw_tx8_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
24:22	RW	0x3	sw_tx7_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
21:19	RW	0x3	sw_tx6_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
18:16	RW	0x3	sw_tx5_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x3	sw_tx4_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
11:9	RW	0x3	sw_tx3_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
8:6	RW	0x3	sw_tx2_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
5:3	RW	0x3	sw_tx1_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)
2:0	RW	0x3	sw_tx0_amp The adjustment for the amplitude level (signal-end amplitude) of the driver (N=0~9)

COMBTXPHY_CON_COMBTXPHY_EMP_C0

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	sw_tx4_emp The adjustment for the emphasis level of the driver(N=0~9)
15:12	RW	0x0	sw_tx3_emp The adjustment for the emphasis level of the driver(N=0~9)
11:8	RW	0x0	sw_tx2_emp The adjustment for the emphasis level of the driver(N=0~9)
7:4	RW	0x0	sw_tx1_emp The adjustment for the emphasis level of the driver(N=0~9)
3:0	RW	0x0	sw_tx0_emp The adjustment for the emphasis level of the driver(N=0~9)

COMBTXPHY_CON_COMBTXPHY_EMP_C1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	sw_tx9_emp The adjustment for the emphasis level of the driver(N=0~9)
15:12	RW	0x0	sw_tx8_emp The adjustment for the emphasis level of the driver(N=0~9)
11:8	RW	0x0	sw_tx7_emp The adjustment for the emphasis level of the driver(N=0~9)
7:4	RW	0x0	sw_tx6_emp The adjustment for the emphasis level of the driver(N=0~9)

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_tx5_emp The adjustment for the emphasis level of the driver(N=0~9)

COMBTXPHY_CON_COMBTXPHY_PLL_DIV

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:24	RW	0x0	sw_rate Rate control for TX 2'b00: Full rate,data rate=FVCO 2'b01: Half rate,data rate=0.5*FVCO 2'b10: Quarter rate,data rate=0.25*FVCO 2'b11: Reserved
23:21	RO	0x0	reserved
20:16	RW	0x00	sw_ref_div Reference clock divider control
15	RO	0x0	reserved
14:0	RW	0x4000	sw_pll_div The initial divider control for PLL

COMBTXPHY_CON_COMBTXPHY_PLL_CTRL0

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved Reserved register for PLL

COMBTXPHY_CON_COMBTXPHY_PLL_CTRL1

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:20	RW	0x1	sw_tx_rterm TX termination resistance adjustment 3'b000: 44 ohm; 3'b001: 50 ohm; 3'b010: 57 ohm; 3'b011: 67 ohm; 3'b100: 80 ohm; 3'b101: 100 ohm; 3'b110: 133 ohm; 3'b111: 4000ohm only for CML mode
19:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_tx_mode Control the TX driver mode 2'b00/01: Mode 1: the termination resistor connects to AVDL 2'b10/11: Mode 2: common mode voltage sets to meet LVDS.
15:0	RO	0x0	reserved

COMBTXPHY_CON_COMBTXPHY_SSC

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:8	RW	0x18d	sw_ssc_cnt SSC frequency control
7:4	RW	0x0	sw_ssc_depth SSC depth control signal
3:1	RO	0x0	reserved
0	RW	0x0	sw_ssc_en SSC function enable signal ,only applicable in GVI mode 1'b0：SSC function is power down 1'b1: SSC function is turn on

COMBTXPHY_CON_COMBTXPHY_DSI_CTRL

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_dsi_fset_en Enable fast transmission between LP-TX and HS-TX 1'b0 : disable 1'b1 : enable
28	RW	0x0	sw_dsi_rcal_en Enable HS-TX output impedance trimming 1'b0 : disable 1'b1 : enable
27:24	RW	0x0	sw_dsi_rcal_trim HS-TX output resistance initial value 4'b0000 : maximum 4'b1111 : minimum

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	sw_dsi_rcal_ctl sw_dsi_rcal_ctl[0] : Reserved sw_dsi_rcal_ctl[1] : Bypass vref detector sw_dsi_rcal_ctl[2] : Bypass Rout Trimming function sw_dsi_rcal_ctl[4:3] : Adjust Rout Trimming time sw_dsi_rcal_ctl[6:5] : Select Exit Resistance value 2'bX0 : 4.02K 2'b1X : 2.0K sw_dsi_rcal_ctl[7] : Manual and auto trimming select
15:12	RW	0x0	sw_lpcd_vref_trim LP-CD input threshold voltage trimming for channel 0~5 4'b0001 : VL175mV~VH425mV 4'b0010 : VL200mV~VH450mV 4'b1000 : VL225mV~VH475mV 4'b1000 : VL250mV~VH500mV others : reserved
11:7	RW	0x00	sw_lprx_vref_trim ULP/LP-RX input threshold voltage trimming for channel 0~5 4'b0001 : VL275mV/525mV~VH855mV 4'b0010 : VL300mV/550mV~VH880mV 4'b1000 : VL325mV/575mV~VH905mV 4'b1000 : VL350mV/600mV~VH930mV others : reserved
6:4	RW	0x0	sw_dsi_lptx_sr_trim LP-TX output slew-rate trimming for channel 0~9 3'b000 : minimum 3'b111 : maximum
3	RO	0x0	reserved
2:0	RW	0x0	sw_dsi_hstx_amp_trim HS-TX output VOD trimming for channel 0~9 3'b000 : 237.50mv 3'b001 : 231.25mv 3'b010 : 225.00mv 3'b011 : 217.75mv 3'b100 : 212.50mv 3'b101 : 206.25mv 3'b110 : 200.00mv 3'b111 : 193.25mv

COMBTXPHY_CON_COMBTXPHY_CLK_DRV

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	tx9_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
8	RW	0x0	tx8_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
7	RW	0x0	tx7_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
6	RW	0x0	tx6_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
5	RW	0x0	tx5_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
4	RW	0x0	tx4_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
3	RW	0x0	tx3_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others

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Bit	Attr	Reset Value	Description
2	RW	0x0	tx2_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
1	RW	0x0	tx1_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others
0	RW	0x0	tx0_ckdrv_en Enable channel-N to be used for LVDS synchronous clock channel 1'b0: Normal data operation mode; 1'b1: Channel TX used for clock channel ,tx_data[9:0] can be arbitrary state Note: support LVDS mode，tied to low others

7.5 Interface Timing

7.5.1 GVI TX Parallel Data Interface timing

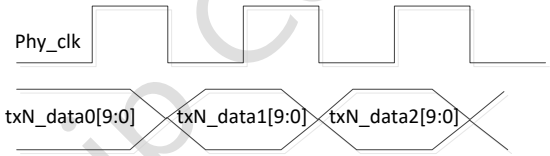

Fig. 7-2 Transmitter timing with phy_clk for GVI

7.5.2 LVDS TX parallel Data Interface timing

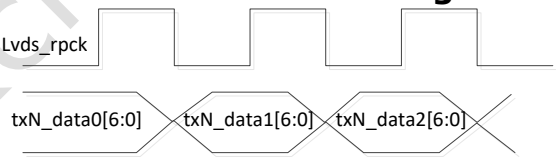

Fig. 7-3 Transmitter timing with lvds_rpck for LVDS

7.5.3 TX Latency and Data Sequence

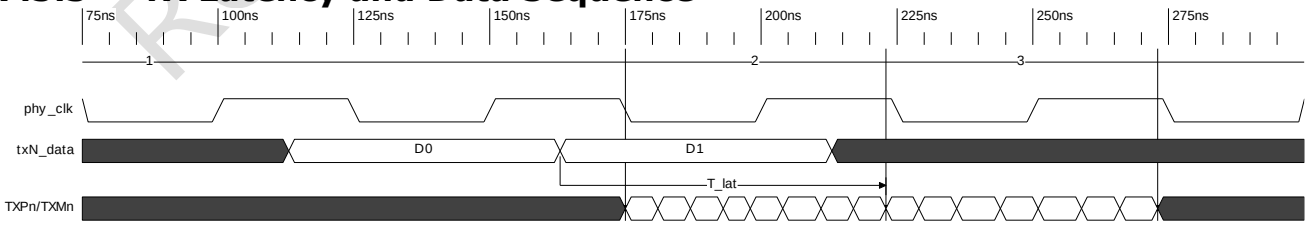

Fig. 7-4 Transmitter latency

7.6 PLL

7.6.1 PLL Basic Setting

The PLL is a fractional-N PLL. When pll_div[9:0]=10’b0, the PLL work as integer-N PLL, and pll_div[14:10] control the loop divider.

The fractional part can be calculated as follow: pll_div [9:0]/1024.

The reference clock at PFD(FPFD) about 25Mhz is recommended(FPFD must be range from

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16Mhz to 35Mhz), if frequency of the reference clock is larger then 35Mhz, ref_div[4:0] can be used to divide down the reference clock to meet the requirement of FPFD, the ref_div[4:0].

7.6.2 GVI Data Rate Setting

The PLL VCO clock frequency is decided by ref_div and pos_div/pre_div. The pos_div is a fractional-N divide, which can realize the spectrum spread clock. The VCO can work from 2.0 Ghz to 4.0Ghz. The PLL structure shown as follows.

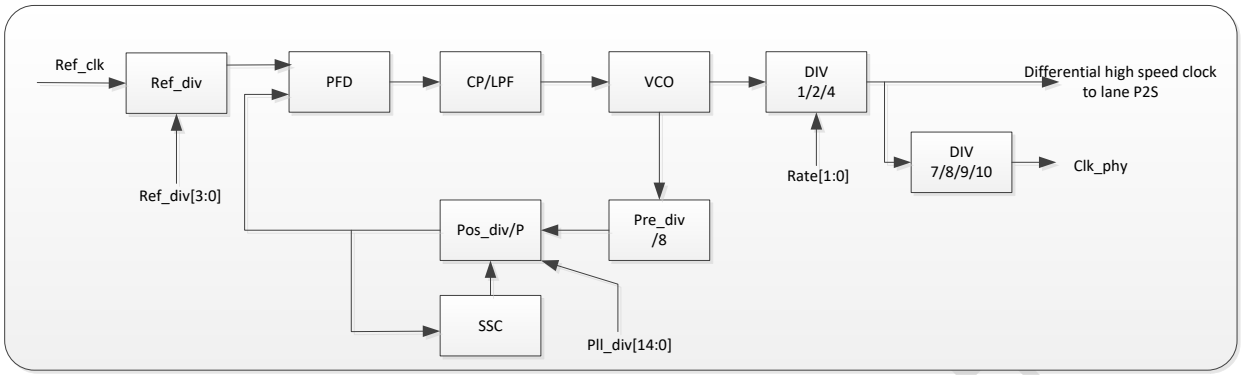

Fig. 7-5 PLL function diagram for GVI

The VCO clock frequency(FVCO) can be calculation as bellow.

$$FVCO = refclk * pll_div * 8/(1024*(ref_div+1))$$

The PLL will supply high speed clock(FHSC) for each lane for data serialization, and

$$FHSC = FVCO / 2^{rate[1:0]}$$

7.6.3 LVDS Data Rate Setting

The frequency of lvds_rpck is a seventh of the LVDS data rate, which is confirmed, so the coefficient of ref_div and pre_div/post_div are configured by rate[1:0] to get better performance.

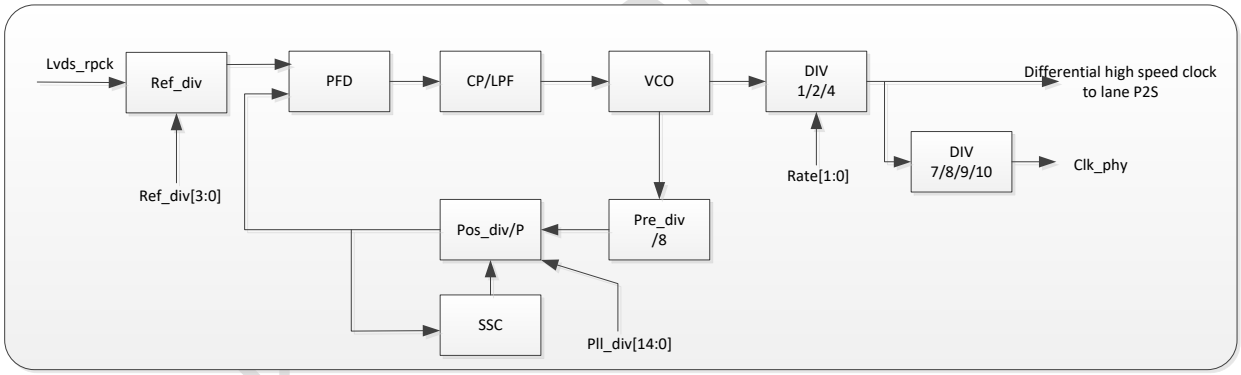

Fig. 7-6 PLL function diagram for LVDS

The VCO clock frequency (FVCO) can be calculation as bellow.

$$FVCO = lvds_rpck * (2^{rate[1:0]} / 8) * 112$$

- pll_div[14:0]=15'b011_1000_0000_0000
- bus_width[1:0]=2'b11

The PLL will supply high speed clock (FHSC) for each lane for data serialization, and

$$FHSC = FVCO / 2^{(rate[1:0]+1)}$$

7.6.4 MIPI DSI PLL Setting

The PLL VCO clock frequency is decided by ref_div and pos_div/pre_div. The pos_div is a fractional-N divide, which can realize the spectrum spread clock. The VCO can work from 1.5 Ghz to 3.0Ghz. The PLL structure shows as follows.

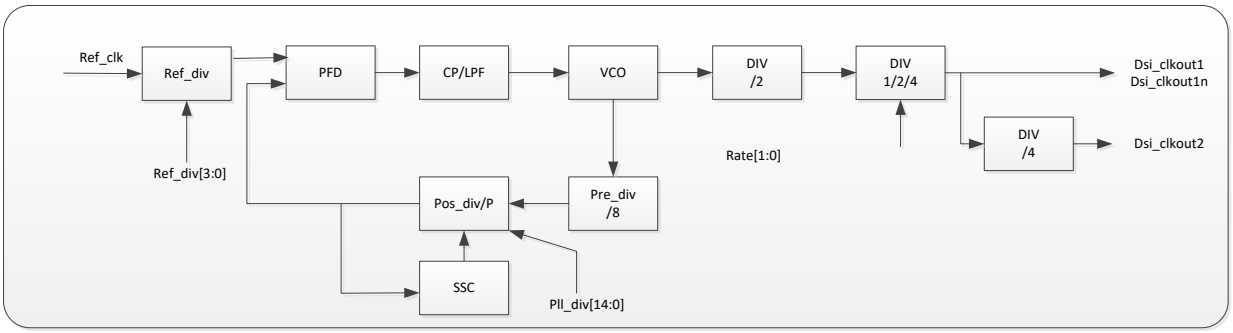

Fig. 7-7 PLL function diagram for MIPI DSI

7.7 Application Notes

7.7.1 GVI/LVDS start-up sequence

Before power up the PLL and lane macro, make sure the power supply and the reference clock is ready, and the register should be accessed before releasing pd_pll. A purposed power up sequence list below:

1) Power up the chip and power on reset
2) Access registers if necessary
3) After reference clock is available, release pd_pll and tx_pd[N]
4) When pll_rdy = 1, clk_phy are available and ready to be used
5) Set tx_idle[N]=0 to start normal data transmission

7.7.2 MIPI DSI start-up sequence

Before power up the PLL and lane macro, make sure the power supply and the reference clock is ready, and the registers should be accessed before releasing pd_pll. A proposed power up sequence list below:

1) Power up the chip and power on reset
2) Access registers if necessary
3) After reference clock is available, release pd_pll and set rcal_en
4) When pll_rdy=1, dsi_clkout1/dsi_clkout2 are available and ready to be used. While the HS-TX Rout calibration is done, rcal_done is turned high, digital can send data to lane

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Chapter 8 HDMI TX PHY

8.1 Overview

HDMI TX is fully compliant with HDMI 1.4a specification. It offers a simple implementation for consumer electronics like DVD/player/recorder and camcorder. HDMI TX consists of one HMDI transmitter controller and one HMDI transmitter PHY.
It supports the following features:

- Ultra low power operation, less than 60mW in PHY during 1080P HD display
- HDMI 1.4a/b/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- Supports data rate from 25MHz, 1.65Gbps up to 3.4Gbps over a Single channel HDMI
- Support 3D function defined in HDMI 1.4 a/b spec
- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Supports all DTV resolutions including 480p /576p /720p /1080p
- Digital video interface supports a pixel size of 24bits color depth in RGB
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as additional feature
- Lower power operation with optimal power management feature
- Embedded ESD, scan support logic.
- Library delivered to support all major EDA tools and detailed guide to integrate into pad ring/BGA bumps
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug
- 3.3V high speed I/O and 1.2V/1.0V core power supply

8.2 Block Diagram

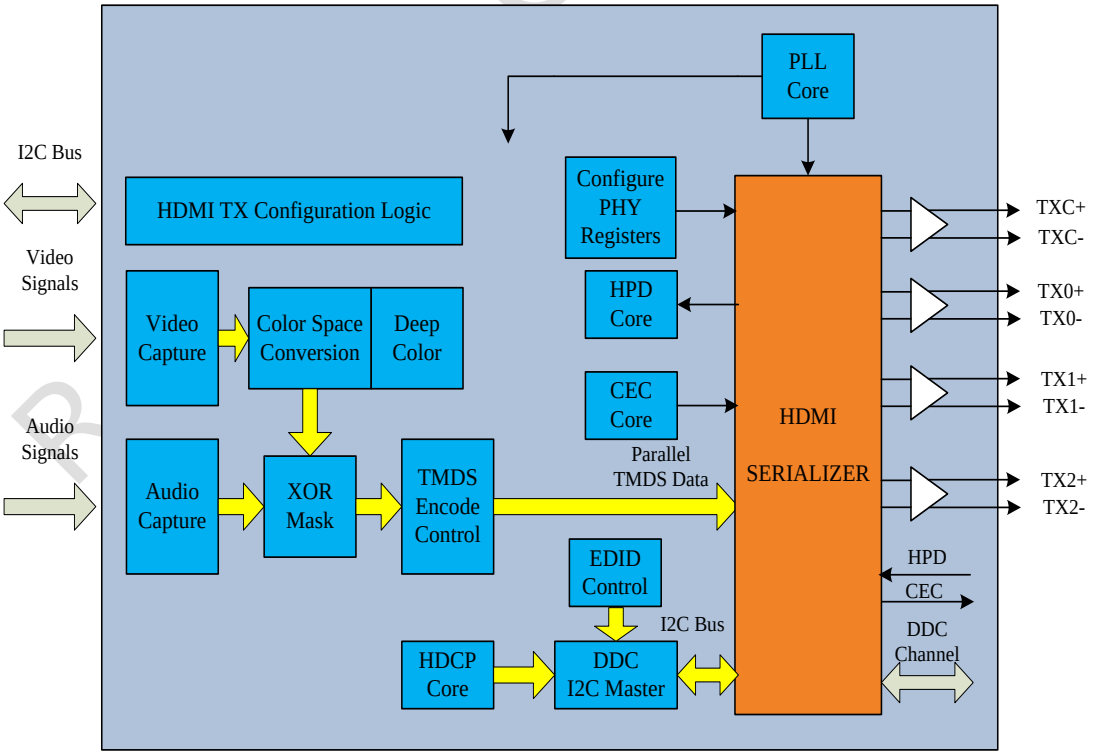

Fig. 8-1 HDMI TX Block Diagram

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8.3 Function Description

8.3.1 Video Data Processing

The video processing contain video format timings, pixel encodings(RGB to YCbCr, or YCbCr to RGB), colorimetry and corresponding requirements. This function is implemented by some functional blocks, Video Capture block, Color Space Conversion block, and Deep Color block.

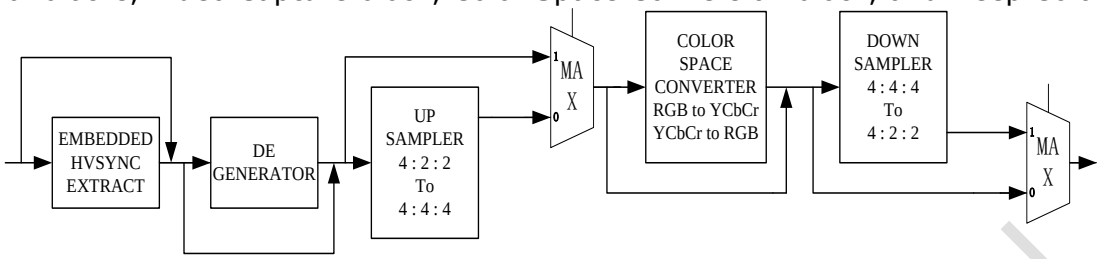

Fig. 8-2 HDMI Video Data Processing

The input video pixels can be encoded in either RGB, YCBCR 4:4:4 or YCBCR 4:2:2 formats by Color Space Conversion block.

The input Video data can have a pixel size of 24, 30, 36 or 48 bits. The deep color block is used to deal with different pixel size. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate. HDMI Transmitter support video formats with TMDS rates below 25MHz (e.g. 13.5MHz for 480i/NTSC) that can be transmitted using a pixel-repetition scheme by setting relative registers.

The following interface timing diagram outlines the Video interface signal format. 24 bit data (we also support 36 bit data for deep color) in RGB can be captured by the rising edge of VCLK with 1ns setup time and 1ns hold time requirements. Control signals such DE and VSync/HSync/FSync going with the same timing relationship.

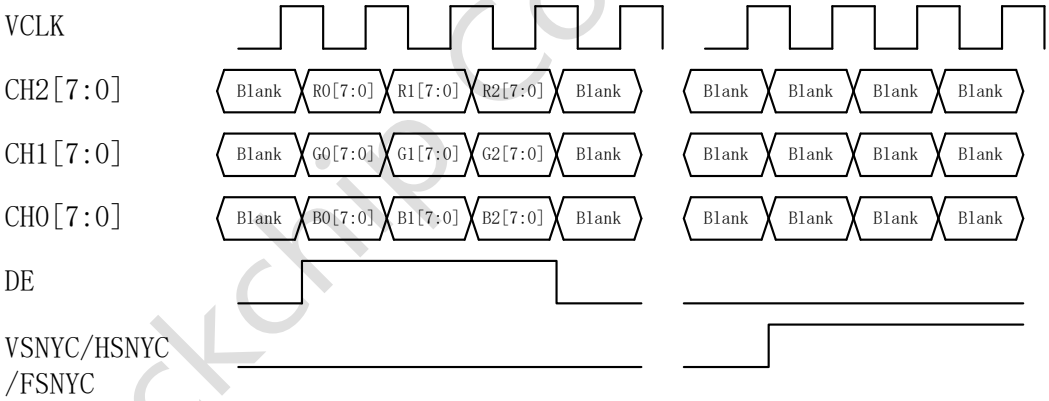

Fig. 8-3 HDMI Video Processing Timing

1.Video Data Capture Logic

HDMI TX support input video data related format table is listed below.

Table 8-1 HDMI Supported Input Video Formats

Color Space	Pixel Encoding	Sync	Channel Width	Pin Nums
RGB	4:4:4	Separate	8	24
RGB	4:4:4	Separate	10	30
YCbCr	4:4:4	Separate	8	24
YCbCr	4:4:4	Separate	10	30
YCbCr	4:2:2	Separate	8	16
YCbCr	4:2:2	Separate	10	20
YCbCr	4:4:4	Embedded	8	24
YCbCr	4:4:4	Embedded	10	30
YCbCr	4:2:2	Embedded	8	16
YCbCr	4:2:2	Embedded	10	20

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2.Embedded Sync Extraction Module
The module is used to extract Vsync and Hsync signals from input video data stream such as ITU656 format. With setting the relative registers, this functional module can extract correct video sync signals for later process block using.
3.Data Enable (DE) Generator
HDMI Transmitter has DE signal generator by incoming HSYNCs, VSYNCs and Video clock. External DE is optional and selected by appropriate register settings. This feature is particularly useful when interfacing to MPEG decoders that do not provide a specific DE output signal.
4.Color Space Conversion
HDMI Transmitter Color space conversion (CSC) is available to interface for several MPEG decoders like with YCbCr-only outputs, and to provide full DVI backwards compatibility. The function of this module is to perform color space conversion functionality as listed below.

a. Convert RGB input Video data to YCbCr Video data.
b. Convert YCbCr input Video data to RGB Video data.
c. upsample for YCbCr 4:2:2 to YCbCr 4:4:4
d. downsample for YCbCr 4:4:4 to YCbCr 4:2:2

8.3.2 Audio Data Processing

The HDMI TX audio process contain audio clock regeneration, placement of audio samples within packets, packet timing control, audio sample rates setting, and channel/speaker assignments. This function is implemented by Audio Capture blocks.
The Audio Capture support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz.
The scheme of audio processing as shown in the figure below:

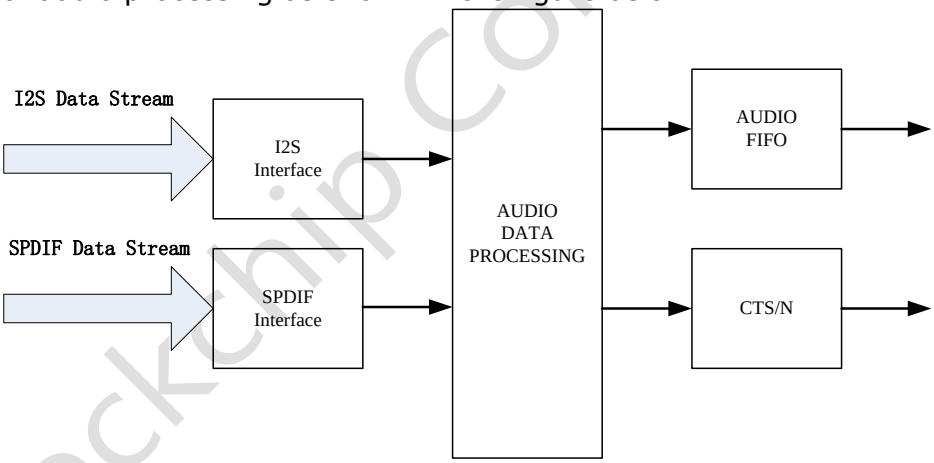

Fig. 8-4 HDMI Audio Data Processing Diagram

1.I2S
The function of this module is to implement I2S audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. Four I2S inputs also allow transmission of DVD-Audio to A/V Receivers and high-end displays. The interface supports from 2-channel to 8-channel audio up to 192 kHz. The I2S pins must also be coherent with mclk. The appropriate registers must be configured to describe the format of audio being input. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets. Table shows the I2S 8 channel audio formats that are supported for each of the video formats.

Table 8-2 HDMI TX I2S 2 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

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1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 8-3 HDMI TX I2S 8 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	No	No	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

1.Audio Sample Clock Capture and Regeneration
Audio data being carried across the HDMI link, which is driven by a TMDS clock running at a rate corresponding to the video pixel rate, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.
The HDMI Transmitter determine the fractional relationship between the TMDS clock and an audio reference clock (128 audio sample rate [fs]) and pass the numerator and denominator of that fraction to the HDMI Sink across the HDMI link. The Sink then re-create the audio clock from the TMDS clock by using a clock divider and a clock multiplier.
The exact relationship between the two clocks will be.

$$128 \cdot fS = fTMDS_clock \cdot N / CTS.$$

The scheme of the Audio Sample Clock Capture and Regeneration as shown below:

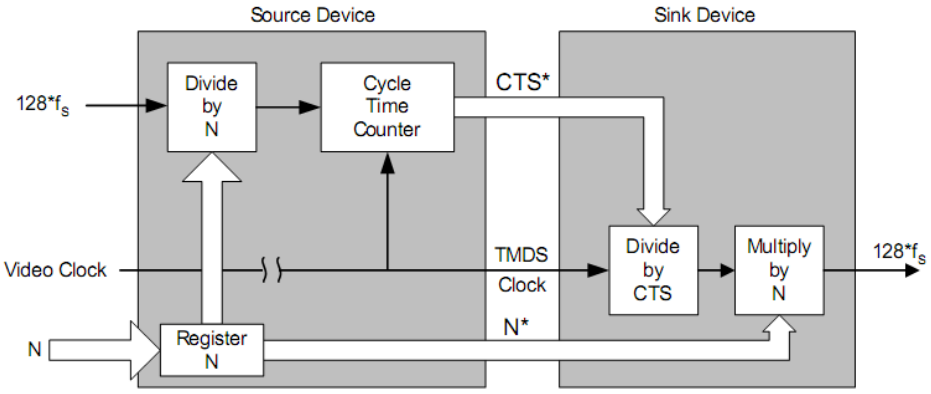

Fig. 8-5 HDMI Audio Clock Regeneration Model

8.3.3 DDC

The DDC functional block is used for configuration and status exchange between the HDMI Source and HDMI Sink. HMDI Transmitter Controller has I2C Master Interface for DDC transactions. It enables for host controller to read EDID, HDCP authentication by issuing simple register access. The I2C bus speed is limited by DDC specification. DDC bus access frequency can be controlled.

8.3.4 EDID

Extended Display Identification Data (EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which is stored in the sink device, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the DTV Monitor. The function of this module is to implement EDID feature.

8.3.5 HDCP

HDMI Transmitter has a capability for HDCP authentication by hardware. The function of this module is to implement HDCP encryption feature. This feature can be turned on or off depending on register setting.

8.3.6 Hot Plug Detect

HDMI Transmitter has a capability for detecting the Sink plug in or plug out, and launch an interrupt and registers state indicating for software controlling.

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8.3.7 TMDS encoder

The TMDS encoder converts the 2/4/8 bits data into the 10 bit DC-balanced TMDS data. HDMI TX put the TMDS encoding on the audio /video /aux data received from the HDCP XOR mask. This data is output onto three TMDS differential data lines along with a TMDS differential clock.

8.3.8 CEC

The CEC functional block provides high-level control functions between all of the various audiovisual products in a user's environment through one line.

8.3.9 Optional Lipsync

HDMI sinks and repeaters can now declare audio/video latency information in their EDIDs. HDMI TX can read the audio/video latency information from HDMI sinks, than it may delay audio or video to compensate for latencies in downstream devices.

8.4 Register Description

8.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
HDMI_reg00	0x0000	B	0x67	Register00
HDMI_reg01	0x0004	B	0x01	Register01
HDMI_reg02	0x0008	B	0x30	Register02
HDMI_reg04	0x0010	B	0x08	Register04
HDMI_reg05	0x0014	B	0x00	Register05
HDMI_reg08	0x0020	B	0x00	Register08
HDMI_reg09	0x0024	B	0x00	Register09
HDMI_reg0a	0x0028	B	0x00	Register0a
HDMI_reg0b	0x002c	B	0x00	Register0b
HDMI_reg0c	0x0030	B	0x00	Register0c
HDMI_reg0d	0x0034	B	0x00	Register0d
HDMI_reg0e	0x0038	B	0x00	Register0e
HDMI_reg0f	0x003c	B	0x00	Register0f
HDMI_reg10	0x0040	B	0x00	Register10
HDMI_reg11	0x0044	B	0x00	Register11
HDMI_reg12	0x0048	B	0x00	Register12
HDMI_reg13	0x004c	B	0x00	Register13
HDMI_reg14	0x0050	B	0x00	Register14
HDMI_reg15	0x0054	B	0x00	Register15
HDMI_reg35	0x00d4	B	0x01	Register35
HDMI_reg37	0x00dc	B	0x00	Register37
HDMI_reg38	0x00e0	B	0x3c	Register38
HDMI_reg39	0x00e4	B	0x00	Register39
HDMI_reg3a	0x00e8	B	0x00	Register3a
HDMI_reg3f	0x00fc	B	0x00	Register3f
HDMI_reg40	0x0100	B	0x18	Register40
HDMI_reg41	0x0104	B	0x00	Register41
HDMI_reg45	0x0114	B	0x00	Register45
HDMI_reg46	0x0118	B	0x00	Register46
HDMI_reg47	0x011c	B	0x00	Register47

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Name	Offset	Size	Reset Value	Description
HDMI_reg4a	0x0128	B	0x00	Register4a
HDMI_reg4b	0x012c	B	0x40	Register4b
HDMI_reg4c	0x0130	B	0x00	Register4c
HDMI_reg4d	0x0134	B	0x00	Register4d
HDMI_reg4e	0x0138	B	0x00	Register4e
HDMI_reg4f	0x013c	B	0x00	Register4f
HDMI_reg50	0x0140	B	0x00	Register50
HDMI_reg52	0x0148	B	0x12	Register52
HDMI_reg53	0x014c	B	0x04	Register53
HDMI_reg57	0x015c	B	0x20	Register57
HDMI_reg58	0x0160	B	0x00	Register58
HDMI_reg63	0x018c	B	0x26	Register63
HDMI_reg65	0x0194	B	0x00	Register65
HDMI_reg66	0x0198	B	0x00	Register66
HDMI_reg67	0x019c	B	0x00	Register67
HDMI_reg68	0x01a0	B	0x00	Register68
HDMI_reg69	0x01a4	B	0x00	Register69
HDMI_reg6a	0x01a8	B	0x00	Register6a
HDMI_reg6c	0x01b0	B	0x00	Register6c
HDMI_reg95	0x0254	B	0x00	Register95
HDMI_reg96	0x0258	B	0x00	Register96
HDMI_reg97	0x025c	B	0x00	Register97
HDMI_reg98	0x0260	B	0x03	Register98
HDMI_reg9c	0x0270	B	0x00	Register9c
HDMI_reg9e	0x0278	B	0x01	Register9e
HDMI_reg9f	0x027c	B	0x00	Register9f
HDMI_rega0	0x0280	B	0x00	Registera0
HDMI_rega1	0x0284	B	0x00	Registera1
HDMI_rega2	0x0288	B	0x00	Registera2
HDMI_rega3	0x028c	B	0x00	Registera3
HDMI_rega4	0x0290	B	0x00	Registera4
HDMI_rega5	0x0294	B	0x00	Registera5
HDMI_rega6	0x0298	B	0x00	Registera6
HDMI_rega7	0x029c	B	0x00	Registera7
HDMI_rega8	0x02a0	B	0x00	Registera8
HDMI_rega9	0x02a4	B	0x00	Registera9
HDMI_regaa	0x02a8	B	0x00	Registeraa
HDMI_regab	0x02ac	B	0x00	Registerab
HDMI_regac	0x02b0	B	0x00	Registerac
HDMI_regad	0x02b4	B	0x00	Registerad
HDMI_regae	0x02b8	B	0x00	Registerae
HDMI_regaf	0x02bc	B	0x00	Registeraf

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Name	Offset	Size	Reset Value	Description
HDMI_regb0	0x02c0	B	0x00	Registerb0
HDMI_regb1	0x02c4	B	0x00	Registerb1
HDMI_regb2	0x02c8	B	0x00	Registerb2
HDMI_regb3	0x02cc	B	0x00	Registerb3
HDMI_regb4	0x02d0	B	0x00	Registerb4
HDMI_regb5	0x02d4	B	0x00	Registerb5
HDMI_regb6	0x02d8	B	0x00	Registerb6
HDMI_regb7	0x02dc	B	0x00	Registerb7
HDMI_regb8	0x02e0	B	0x00	Registerb8
HDMI_regb9	0x02e4	B	0x00	Registerb9
HDMI_regba	0x02e8	B	0x00	Registerba
HDMI_regbb	0x02ec	B	0x00	Registerbb
HDMI_regbc	0x02f0	B	0x00	Registerbc
HDMI_regbd	0x02f4	B	0x00	Registerbd
HDMI_regbe	0x02f8	B	0x00	Registerbe
HDMI_regc0	0x0300	B	0xc0	Registerc0
HDMI_regc1	0x0304	B	0x00	Registerc1
HDMI_regc2	0x0308	B	0x78	Registerc2
HDMI_regc3	0x030c	B	0x00	Registerc3
HDMI_regc4	0x0310	B	0x00	Registerc4
HDMI_regc5	0x0314	B	0x00	Registerc5
HDMI_regc8	0x0320	B	0x00	Registerc8
HDMI_regc9	0x0324	B	0x50	Registerc9
HDMI_regce	0x0338	B	0x01	Registerce
HDMI_regd0	0x0340	B	0x00	Registerd0
HDMI_regd1	0x0344	B	0x00	Registerd1
HDMI_regd2	0x0348	B	0x00	Registerd2
HDMI_regd3	0x034c	B	0x00	Registerd3
HDMI_regd4	0x0350	B	0x03	Registerd4
HDMI_regd5	0x0354	B	0x09	Registerd5
HDMI_regd6	0x0358	B	0x03	Registerd6
HDMI_regd7	0x035c	B	0x00	Registerd7
HDMI_regd8	0x0360	B	0xff	Registerd8
HDMI_regd9	0x0364	B	0xff	Registerd9
HDMI_regda	0x0368	B	0x00	Registerda
HDMI_regdb	0x036c	B	0x00	Registerdb
HDMI_regdc	0x0370	B	0xd0	Registerdc
HDMI_regdd	0x0374	B	0x20	Registerdd
HDMI_regde	0x0378	B	0x00	Registerde
HDMI_rege0	0x0380	B	0x23	Registere0
HDMI_rege1	0x0384	B	0x0f	Registere1
HDMI_rege2	0x0388	B	0xaa	Registere2

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Name	Offset	Size	Reset Value	Description
HDMI_rege3	0x038c	B	0x0f	Registere3
HDMI_rege7	0x039c	B	0x1e	Registere7
HDMI_rege8	0x03a0	B	0x00	Registere8
HDMI_reged	0x03b4	B	0x03	Registered

8.4.2 Detail Register Description

HDMI_reg00

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6	RW	0x1	sw_reset_ana Soft reset for analog part 1'b0: reset 1'b1: not
5	RW	0x1	sw_reset_dig Soft reset for digital part 1'b0: reset 1'b1: not
4	RW	0x0	reserved
3	RW	0x1	vclk_inv Vclk invert select 1'b0: not invert 1'b1: invert
2	RO	0x0	reserved
1	RW	0x0	pd_dig System power down for digital function 1'b0: not 1'b1: power down
0	RW	0x0	interrupt_polarity Interrupt polarity 1'b1: Active High 1'b0: Active low

HDMI_reg01

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:1	RW	0x0	input_video_fmt Input video format 3'b000: RGB and YCbCr 4:4:4 3'b101: DDR RGB 4:4:4 or YCbCr 4:4:4 3'b110: DDR YCbCr 4:2:2

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Bit	Attr	Reset Value	Description
0	RW	0x1	de_sel DE select 1'b0: internal DE 1'b1: external DE

HDMI_reg02
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	video_output_fmt Video output format 2'b00: RGB 4:4:4 2'b01: YCbCr 4:4:4 2'b10: YCbCr 4:2:2
5:4	RW	0x3	data_width_422 Data width for 4:2:2 input 2'b00: 12 bits 2'b01: 10 bits 2'b11: 8 bits
3:1	RW	0x0	reserved
0	RW	0x0	Video input color space 1'b0：RGB 1'b1：YCbCr

HDMI_reg04
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x1	sof_sel After 1st SOF(the first edge of the Vsync) for external DE sample 1'b0: after SOF 1'b1: Not
2:1	RW	0x0	reserved
0	RW	0x0	csc_en CSC (Color Space Convert) enable. 1'b0: no CSC 1'b1: enable CSC

HDMI_reg05
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
7	RW	0x0	clear_avmute Clear avmute
6	RW	0x0	set_avmute Set avmute
5:2	RW	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	audio_mute Audio mute
0	RW	0x0	video_black Video black

HDMI_reg08

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x0	vs_polarity VSYNC polarity 1'b0: Negative 1'b1: Positive
2	RW	0x0	hs_polarity HSYNC polarity 1'b0: Negative 1'b1: Positive
1	RW	0x0	interlace_progressiv_sel Interlace/Progressive 1'b0: Progressive 1'b1: Interlace
0	RW	0x0	ext_video_para_set_en External video parameter setting enable 1'b0: disable 1'b1: enable

HDMI_reg09

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_total_part1 External horizontal total part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0a

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	ext_hs_total_part2 External horizontal total part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0b

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_blank_part1 External horizontal blank part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

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HDMI_reg0c
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
7:3	RW	0x0	reserved
2:0	RW	0x0	ext_hs_blank_part2 External horizontal blank part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0d
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Ext_hs_hback_part1 External horizontal Hsync plus Hback part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0e
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1:0	RW	0x0	Ext_hs_hback_part2 External horizontal Hsync plus Hback part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0f
Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_sync_part1 External horizontal duration part1. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg10
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1:0	RW	0x0	ext_hs_sync_part2 External horizontal duration part2. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg11
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_vertical_total_part1 External vertical total part1. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg12

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Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	ext_vertical_total_part2 External vertical total part2. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg13

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:0	RW	0x00	ext_vertical_blank External vertical blank. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg14

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:0	RW	0x00	ext_vertical_vsync_vback External vertical Vsync plus Vback. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg15

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved
5:0	RW	0x00	ext_vertical_duration External vertical duration. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg35

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
7	RW	0x0	cts_sel CTS source select 1'b0: internal CTS 1'b1: external CTS
6:5	RW	0x0	reserved
4:3	RW	0x0	audio_type_sel Audio type select 2'b00: I2S
2	RW	0x0	mclk_sel MCLK select

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Bit	Attr	Reset Value	Description
1:0	RW	0x1	mclk_ratio MCLK ratio 2'b00: 128 fs 2'b01: 256 fs 2'b10: 384 fs 2'b11: 512 fs

HDMI_reg37
Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	sample_freq_sel Sampling frequency for I2S audio 4'b0011: 32 kHz 4'b0000: 44.1 kHz 4'b0010: 48 kHz 4'b1000: 88.2 kHz 4'b1010: 96 kHz 4'b1100: 176.4 kHz 4'b1110: 192 kHz

HDMI_reg38
Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved
5:2	RW	0xf	i2s_sel I2S enable for the four I2S pins 4'b0001: I2S0 4'b0010: I2S1 4'b0100: I2S2 4'b1000: I2S3
1:0	RW	0x0	i2s_fmt I2S format 2'b00: standard I2S mode 2'b01: right-justified I2S mode 2'b10: left-justified I2S mode

HDMI_reg39
Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	audio_channel3_input_sel Audio channel3 input 2'b00: I2S3 2'b01: I2S2 2'b10: I2S1 2'b11: I2S0

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	audio_channel2_input_sel Audio channel2 input 2'b00: I2S2 2'b01: I2S1 2'b10: I2S0 2'b11: I2S3
3:2	RW	0x0	audio_channel1_input_sel Audio channel1 input 2'b00: I2S1 2'b01: I2S0 2'b10: I2S3 2'b11: I2S2
1:0	RW	0x0	audio_channel0_input_sel Audio channel0 input 2'b00: I2S0 2'b01: I2S3 2'b10: I2S2 2'b11: I2S1

HDMI_reg3a
Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
7	RW	0x0	lr_swap_ch7_8 Left/Right data swap for ch7/8
6	RW	0x0	lr_swap_ch5_6 Left/Right data swap for ch5/6
5	RW	0x0	lr_swap_ch3_4 Left/Right data swap for ch3/4
4	RW	0x0	lr_swap_ch1_2 Left/Right data swap for ch1/2
3:0	RW	0x0	spdif_sample_freq S/PDIF sampling frequency 4’b0011: 32 kHz. 4’b0000: 44.1 kHz. 4’b0010: 48 kHz. 4’b1000: 88.2 kHz. 4’b1010: 96 kHz. 4’b1100: 176.4 kHz. 4’b1110: 192 kHz.

HDMI_reg3f
Address: Operational Base + offset (0x00fc)

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	ncts_part1 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg40
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
7:0	RW	0x18	ncts_part2 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg41
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ncts_part3 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg45
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
7:4	RW	0x00	reserved
3:0	RW	0x00	When use external CTS (reg0x35[7]=1)then set these three regs. CTS={reg45[3:0],reg46[7:0], reg47[7:0]}

HDMI_reg46
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	When use external CTS (reg0x35[7]=1)then set these three regs. CTS={reg45[3:0],reg46[7:0], reg47[7:0]}

HDMI_reg47
Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	When use external CTS (reg0x35[7]=1)then set these three regs. CTS={reg45[3:0],reg46[7:0], reg47[7:0]}

HDMI_reg4a
Address: Operational Base + offset (0x0128)

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Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1	RO	0x0	ddc_sda_bus_statue DDC SDA bus status
0	RO	0x0	ddc_scl_bus_statue DDC SCL bus status

HDMI_reg4b
Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
7:0	RW	0x40	ddc_bus_access_freq_lsb DDC bus access frequency (LSB)

HDMI_reg4c
Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ddc_bus_access_freq_msb DDC bus access frequency (MSB)

HDMI_reg4d
Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_segment_pointer EDID segment pointer

HDMI_reg4e
Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_word_addr EDID word address

HDMI_reg4f
Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_fifo_rd_addr EDID FIFO read address

HDMI_reg50
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	edid_rd_access_window EDID reading access window

HDMI_reg52
Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
7	RW	0x0	authentication_start Authentication start

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Bit	Attr	Reset Value	Description
6	RW	0x0	bksv_not_in_blacklist BKSV is not in the blacklist
5	RW	0x0	bksv_in_blacklist BKSV is in the blacklist
4	RW	0x1	encypte_en current frame encypted en 1'b0: current frame should not be encrypted 1'b1: current frame should be encrypted
3	RW	0x0	authentication_stop Authentication Stop
2	RW	0x0	advanced_mode_sel 1'b0: do not use advanced cipher mode 1'b1: use advanced cipher mode
1	RW	0x1	mode_sel mode selection 1'b0: DVI mode 1'b1: HDMI mode
0	RW	0x0	hdcp_reset HDCP reset

HDMI_reg53

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
7	RW	0x0	disable_127_chk Disable 127 check
6	RW	0x0	skip_bksv_blacklist_chk Skip BKSV blacklist check
5	RW	0x0	pj_chk_en Enable Pj check
4	RW	0x0	disable_dev_num_check Disable device number check
3	RW	0x1	dly_ri_chk Delay Ri check by one clock
2	RW	0x0	use_preset Use preset An value
1:0	RW	0x0	key_comb Key combination

HDMI_reg57

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
7	RW	0x0	Authenticated enable 1'b0：Authenticated 1'b1：Not authenticated
6	RW	0x0	1'b0：AV content is not encrypted 1'b1：AV content is encrypted

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Bit	Attr	Reset Value	Description
5	RW	0x0	reserved
4	RW	0x0	HDCP_work 1'b0：HDCP is working 1'b1：HDCP is not working
3	RW	0x0	advanced_cipher_en advanced cipher enable 1'b0: Advanced cipher is not enabled 1'b1: Advanced cipher is enabled
2:0	RW	0x0	reserved

HDMI_reg58
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	rx_bcaps_value RX Bcaps value

HDMI_reg63
Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
7:5	RW	0x00	reserved
4:0	RW	0x06	timer_100ms Registers for timer 100ms

HDMI_reg65
Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x0	ddc_channel_no_ack DDC channels no acknowledge
2	RW	0x0	pj_mismatch Pj mismatch
1	RW	0x0	ri_mismatch Ri mismatch
0	RW	0x0	bksv_wrong Bksv is wrong

HDMI_reg66
Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg67
Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg68
Address: Operational Base + offset (0x01a0)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg69
Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg6a
Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Bksv value with least significant byte first

HDMI_reg6c
Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	seed_an An seed for generate An

HDMI_reg95
Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hdcp_fifo_first_wr_byte_addr HDCP KEY FIFO first write byte num address

HDMI_reg96
Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hdcp_fifo_first_rd_byte_addr HDCP KEY FIFO first read byte num address

HDMI_reg97
Address: Operational Base + offset (0x025c)

Bit	Attr	Reset Value	Description
7:2	RO	0x0	reserved
1	RW	0x0	hdcp_fifo_rd_addr8 HDCP KEY FIFO first read byte num address[8]
0	RW	0x0	hdcp_fifo_wr_addr8 HDCP KEY FIFO first write byte num address[8]

HDMI_reg98
Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
7:0	RW	0x03	hdcp_fifo_wr_rd_addr HDCP KEY FIFO write or read point address

HDMI_reg9c
Address: Operational Base + offset (0x0270)

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Bit	Attr	Reset Value	Description
7	RW	0x0	general_control_packet General control packet 1'b1: enable 1'b0: disable
6	RW	0x0	mpeg_source_frame_packet MPEG source InfoFrame packet 1'b1: enable 1'b0: disable
5	RW	0x0	source_descriptor_frame_packet Source product descriptor InfoFrame packet 1'b1: enable 1'b0: disable
4	RW	0x0	vendor_specific_frame_packet Vendor specific InfoFrame packet 1'b1: enable 1'b0: disable
3	RW	0x0	gamut_metadata_packet Gamut metadata packet 1'b1: enable 1'b0: disable
2	RW	0x0	isrc1_packet ISRC1 packet 1'b1: enable 1'b0: disable
1	RW	0x0	acp_packet ACP packet 1'b1: enable 1'b0: disable
0	RW	0x0	generic_packet Generic packet 1'b1: enable 1'b0: disable

HDMI_reg9e
Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x1	auto_checksum_frame Auto checksum for InfoFrame 1'b1: enable 1'b0: disable It enables checksum calculation for any InfoFrame packets by hardware.

HDMI_reg9f
Address: Operational Base + offset (0x027c)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	packet_offset packet offset register for 0xa0~0xbe 8'h0: Generic packet 8'h1: ACP packet 8'h2: ISRC1 packet 8'h3: ISRC2 packet 8'h4: Gamut metadata packet 8'h5: Vendor specific InfoFrame 8'h6: AVI InfoFrame 8'h7: Source product descriptor InfoFrame packet 8'h8: Audio InfoFrame packet 8'h9: MPEG source InfoFrame

HDMI_rega0

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega1

Address: Operational Base + offset (0x0284)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega2

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega3

Address: Operational Base + offset (0x028c)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega4

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega5

Address: Operational Base + offset (0x0294)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega6

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega7

Address: Operational Base + offset (0x029c)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega8

Address: Operational Base + offset (0x02a0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega9

Address: Operational Base + offset (0x02a4)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regaa

Address: Operational Base + offset (0x02a8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regab

Address: Operational Base + offset (0x02ac)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regac

Address: Operational Base + offset (0x02b0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regad

Address: Operational Base + offset (0x02b4)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regae

Address: Operational Base + offset (0x02b8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regaf

Address: Operational Base + offset (0x02bc)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb0

Address: Operational Base + offset (0x02c0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb1

Address: Operational Base + offset (0x02c4)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb2

Address: Operational Base + offset (0x02c8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb3

Address: Operational Base + offset (0x02cc)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb4

Address: Operational Base + offset (0x02d0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb5

Address: Operational Base + offset (0x02d4)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb6

Address: Operational Base + offset (0x02d8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb7

Address: Operational Base + offset (0x02dc)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb8

Address: Operational Base + offset (0x02e0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb9

Address: Operational Base + offset (0x02e4)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regba

Address: Operational Base + offset (0x02e8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbb

Address: Operational Base + offset (0x02ec)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbc

Address: Operational Base + offset (0x02f0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbd

Address: Operational Base + offset (0x02f4)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbe

Address: Operational Base + offset (0x02f8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regc0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	mask_int Mask for Interrupt 0: masked 1: not mask [5] Interrupt for active Vsync edge [2] Interrupt for EDID Ready

HDMI_regc1

Address: Operational Base + offset (0x0304)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	int_statu Interrupt status [5] Interrupt for active Vsync edge This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [2] Interrupt for EDID Ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.

HDMI_regc2

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
7:3	RW	0x0f	int_mask Mask for interrupt: 0: masked 1: not masked [7] for HDCP error [6] for bksv fifo ready [5] for bksv update [4] for authentication success [3] for ready to start authentication
2:0	RW	0x0	reserved

HDMI_regc3

Address: Operational Base + offset (0x030c)

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Bit	Attr	Reset Value	Description
7:3	RW	0x00	int_status Interrupt status [7] HDCP error Interrupt This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [6] bksv fifo ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [5] bksv update This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [4] authentication success This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [3] ready to start authentication This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.
2:0	RW	0x0	reserved

HDMI_regc4

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
7	RW	0x00	reserved
6:0	RW	0x00	int_mask Mask for interrupt: 0: masked 1: not masked [6] for HDCP authentication M0 ready [5] for first frame arrive [4] for HDCP An ready [3] [2] for HDCP encrypted [1] for HDCP not encrypted (av mute) [0] for HDCP not encrypted (no av mute)

HDMI_regc5

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
7	RW	0x00	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	int_status_group3 Interrupt status Group3 This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [6] HDCP authentication M0 ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [5] irst frame arrive This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [4] HDCP An ready This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [2] HDCP encrypted This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [1] HDCP not encrypted (av mute) This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [0] HDCP not encrypted (no av mute) This bit will active when the mask for this bit to be set 1.When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.

HDMI_regc8

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
7	RO	0x0	hot_plug_pin_status Hot plug pin status 1'b1: Plug in 1'b0: Plug out
6	RO	0x0	reserved
5	RW	0x1	Mask_hpd_int Mask for hot plug detect(HPG) interrupt 1'b0：masked 1'b1：not mask
4:2	RW	0x4	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	Int_hpd Interrupt for hot plug detect(HPD) This bit will active when the mask for this bit to be set 1.When interrupt occurs,this bit will be equal to 1. Clear interrupt：write 1 to this bit.
0	RW	0x0	reserved

HDMI_regc9

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	video_bist_mode Video BIST mode 2'b00: normal color bar. 2'b01: special color bar. 2'b10: black
5	RW	0x0	flush_en Flush enable. After enable it the screen will flush from color bar to black again and again. 1'b1: enable 1'b0: disable
4	RW	0x1	disable_colorbar_bist_test Disable color bar BIST test 1'b1: disable 1'b0: enable
3:0	RW	0x0	reserved

HDMI_regce

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x1	tmds_channel_sync The synchronization for TMDS channels The synchronization for TMDS channels is automatic after Reset the HDMI. But you can synchronization for TMDS channels manually. The operation for this function is: first send 0 to this bit, then send 1, and keep 1 into this bit.

HDMI_regd0

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	modify_start_bit_timing_hisense_tv Modify the start bit timing for Hisense TV 1'b1: Modify the start bit timing for Hisense TV 1'b0: Not modify
5	RW	0x0	reject_rec_cec_broadcast_message Reject receive CEC broadcast message 1'b1: Reject receive CEC broadcast message 1'b0: Not reject
4:3	RW	0x0	reserved
2	RW	0x0	CEC_bus_free_time_cnt_en Enable count CEC bus free time 1'b1: Enable count CEC bus free time 1'b0: Not enable
1	RW	0x0	forbid_receive_cec_message Forbid receive CEC message 1'b1: Forbid receive CEC message 1'b0: Not forbid
0	RW	0x0	start_transmit_cec_message Start transmit CEC message 1'b1: Start transmit CEC message 1'b0: Not start

HDMI_regd1
Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_rx_tx_data_in_fifo CEC RX/TX data in FIFO

HDMI_regd2
Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	wr_cec_tx_data_addr Point address for write CEC TX data

HDMI_regd3
Address: Operational Base + offset (0x034c)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	cec_rx_data_addr Point address for CEC RX data

HDMI_regd4
Address: Operational Base + offset (0x0350)

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Bit	Attr	Reset Value	Description
7:0	RW	0x03	cec_clk_freq CEC working clock frequency register1

HDMI_regd5
Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
7:0	RW	0x09	cec_work_clk_freq CEC working clock frequency register1

HDMI_regd6
Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x03	tx_block_length Length of TX blocks

HDMI_regd7
Address: Operational Base + offset (0x035c)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	rx_block_length Length of RX blocks

HDMI_regd8
Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
7:0	RW	0xff	cec_tx_int_mask Mask for CEC TX Interrupts 1'b0: masked 1'b1: not mask [3] Interrupt for TX done [2] Interrupt for TX no ACK from follower [1] Interrupt for TX broadcast rejected [0] Interrupt for CEC line free time not satisfied

HDMI_regd9
Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
7:0	RW	0xff	cec_rx_int_mask Mask for CEC RX Interrupts 1'b0: masked 1'b1: not mask [4] Interrupt for RX receive logic address error [3] Interrupt for RX receive glitch error [2] Interrupt for RX ACK detect overtime [1] Interrupt for RX sending broadcast reject [0] Interrupt for RX done

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HDMI_regda
Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_tx_int CEC TX Interrupts [3] Interrupt for TX done [2] Interrupt for TX no ACK from follower [1] Interrupt for TX broadcast rejected [0] Interrupt for CEC line free time not satisfied

HDMI_regdb
Address: Operational Base + offset (0x036c)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_tx_int CEC RX Interrupts [4] Interrupt for RX receive logic address error [3] Interrupt for RX receive glitch error [2] Interrupt for RX ACK detect overtime [1] Interrupt for RX sending broadcast reject [0] Interrupt for RX done

HDMI_regdc
Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
7:0	RW	0xd0	signal_free_time_l Signal free time length_L

HDMI_regdd
Address: Operational Base + offset (0x0374)

Bit	Attr	Reset Value	Description
7:0	RW	0x20	signal_free_time_h Signal free time length_H

HDMI_regde
Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	dev_addr Device logic address

HDMI_rege0
Address: Operational Base + offset (0x0380)

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4	RW	0x1	TMDS_clk_sel 1'b0: select TMDS clock from PLL; 1'b1: select TMDS clock generated by serializer
3	RW	0x0	TMDS_phase_sel 1'b0: select default phase for TMDS clock; 1'b1: select synchronized phase for TMDS clock with regard to TMDS data
2	RW	0x0	hdmi_band_gap_pd HDMI Band gap power down. 1'b1: Active
1	RW	0x1	hdmi_pll_pd HDMI PLL power down. 1'b1: Active
0	RW	0x1	tmds_channel_pd TMDS channel power down. 1'b1: Active

HDMI_rege1

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x1	clk_channel_driver_en Clock channel driver enable 1'b0: disable 1'b1: enable
2:0	RW	0x7	data_channels_driver_en Three data channels driver enable [2]-ch2 [1]-ch1 [0]-ch0 1'b0: disable 1'b1: enable

HDMI_rege2

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
7:4	RW	0xa	clk_driver_strength Clock channel main-driver strength 4'b0000~4'b1111: the strength from low to high
3:0	RW	0xa	data_driver_strength Three data channels main-driver strength 4'b0000~4'b1111: the strength from low to high

HDMI_rege3

Address: Operational Base + offset (0x038c)

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Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:4	RW	0x0	pre_emphasis_strength Pre-emphasis strength 3'b000~3'b111: the strength from 0 to high
3:2	RW	0x3	clk_driver_strength Clock channel pre-driver strength Slew rate from low to high 2'b00~2'b11: the strength from low to high
1:0	RW	0x3	data_driver_strength Three data channels pre-driver strength Slew rate from low to high 2'b00~2'b11: the strength from low to high

HDMI_rege7

Address: Operational Base + offset (0x039c)

Bit	Attr	Reset Value	Description
7:0	RW	0x78	feedback_dividing_ratio_part1 The value of feedback dividing ratio

HDMI_rege8

Address: Operational Base + offset (0x03a0)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x0	feedback_dividing_ratio_part2 The value of feedback dividing ratio

HDMI_reged

Address: Operational Base + offset (0x03b4)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x0c	pre_dividing_ratio The value of pre-dividing ratio

Note1: There are some bits of registers have not description in the registers table above, are reserved for other using, please keep it into default value.

8.5 Application Notes

This chapter describes how to bring up HDMI transmitter in your system. As shown few examples below, these introduce the basically HDMI transmitter application, likes, the Hot Plug Detect, EDID read back, multiple audio format input and different video resolution displaying.

You can easily configure these functions with proper registers value setting by HDMI TX APB BUS.

8.5.1 Initial Operation

The default HDMI transmitter is configured to 24bit RGB 1080P resolution video with 8 channel 44.1K sample I2S format audio input. It is easily for customer to turn on HDMI transmitter without doing more complex operation. Just do the step, reset the HDMI TX.

8.5.2 Hot Plug Detection

Hot Plug Detect is a special feature for HDMI transmitter spying the state on the HDMI port. You can control this function by using the interrupt signal and proper registers from the

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HDMI transmitter with few operations. The following is a step by step instruction for detecting the hot plug in and out.

Hot Plug in Steps:

Step1: Send 0x63 to register 0x00.
Step2: Plug HDMI receiver in.
Step3: Check the interrupt from signal pin_int.
If the pin_int shows high, that means the HDMI transmitter interrupt have generated.
Step4: Check the interrupt.
Read the bit1 o f the register 0xc8. If bit1=1'b1 that means the hot plug interrupt valid, otherwise there is other interrupt. The n s end the 1'b1 to bit1 of register 0xc8 to clean up the hot plug interrupt.
Step5: Check if really HDMI receiver plug in.
Read the bit7 of the register 0xc8. If bit7=1'b1 that means hot plug in was really happen, otherwise there may be a glitch on the HPD port.

Hot Plug out Steps:

Step1: HDMI transmitter at working state.
Step2: Plug HDMI receiver out.
Step3: Check the interrupt from signal pin_int.
If the pin_int shows high, that means the HDMI transmitter interrupt have generated.
Step4: Check the interrupt.
Read the bit1 of the register 0xc8. If bit1=1'b1 that means the hot plug interrupt valid, otherwise there is other interrupt. Then send the 1'b1 to bit1 of register 0xc8 to clean up the hot plug interrupt.
Step5: Check if really HDMI receiver plug out.
Read the bit7 of the register 0xc8. If bit7=1'b0 that means hot plug out was really happen, otherwise there may be a glitch on the HPD port.

8.5.3 Reading EDID

Read EDID is a function that can make the HDMI transmitter to read the HDMI receiver's Extended Display Identification Data (EDID) in order to discover the HDMI receiver's configuration and capabilities. HDMI transmitter can choose the appropriate audio and video format for playing and displaying by the HDMI receiver through the use of the EDID. Besides, HDMI transmitter support the reading Enhanced Extended Display Identification Data (E-EDID) if HDMI receiver have this enhanced structure.
The following describes how to read E-EDID through HDMI transmitter. The total E-EDID is 512bytes data, which is divided into 2 segments. Each segment has 256bytes data. The Read E-EDID function is only read 128bytes data from HDMI receiver at each time. So, you must read 4 times that can read total 512bytes data back.

Prepare read E-EDID 512bytes Steps:

Step1: Send 0x63 to register 0x00.
System power down mode.
Step2: HDMI transmitter detected Hot Plug in.
Step3: Define DDC clock (SCL) frequency Fscl = 100K.
Fscl = Freg_clk/(4*X). X={register 0x4c, register 0x4b}.
Note Freg_clk is the frequency of the tmds clock.
Assume the tmds clock is 148.5MHz.
Send 0x73 to register 0x4b, Send 0x01 to register 0x4c.
Step4: Enable EDID Ready interrupt.
Send 0x04 to register 0xc0

Read E-EDID segment 0x00 256bytes Steps:

Step1: Set EDID FIFO initial address.
Send 0x00 to register 0x4f
Step2: Set EDID first word address, read first 128bytes.
Send 0x00 to register 0x4e
Step3: Set EDID segment address.
Send 0x00 to register 0x4d
Step4: Waiting and check EDID interrupt from pin_int.

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Check the EDID Ready state from bit2 of register 0xc1. If bit2 = 1'b1 that means EDID data ready. The n send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.
Step5: Read first 128bytes EDID data from EDID FIFO.
for (i = 0, i < 128, i = i + 1)
Read data from register 0x50.
Step6: Set EDID FIFO initial address again.
Send 0x00 to register 0x4f
Step7: Set EDID first word address, read last 128bytes.
Send 0x80 to register 0x4e
Step8: Set EDID segment address.
Send 0x00 to register 0x4d
Step9: Waiting and check EDID interrupt from pin_int.
Check the EDID Ready state from bit2 of register 0xc1. If bit2 = 1'b1 that means EDID data ready. The n send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.
Step10: Read last 128bytes EDID data from EDID FIFO.
for (i = 0, i < 128, i = i + 1)
Read data from register 0x50.

Read E-EDID segment 0x01 256bytes Steps:

Step1: Set EDID FIFO initial address.
Send 0x00 to register 0x4f
Step2: Set EDID first word address, read first 128bytes.
Send 0x00 to register 0x4e
Step3: Set EDID segment address.
Send 0x01 to register 0x4d
Step4: Waiting and check EDID interrupt from pin_int.
Check the EDID Ready state from bit2 of register 0xc1. If bit2 =1'b1 that means EDID data ready. Then send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.
Step5: Read first 128bytes EDID data from EDID FIFO.
for (i = 0, i < 128, i = i + 1)
Read data from register 0x50.
Step6: Set EDID FIFO initial address again.
Send 0x00 to register 0x4f
Step7: Set EDID first word address, read last 128bytes.
Send 0x80 to register 0x4e
Step8: Set EDID segment address.
Send 0x01 to register 0x4d
Step9: Waiting and check EDID interrupt from pin_int.
Check the EDID Ready state from bit2 of register 0xc1. If bit2 =1'b1 that means EDID data ready. Then send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.
Step10: Read last 128bytes EDID data from EDID FIFO.
for (i = 0, i < 128, i = i + 1)
Read data from register 0x50.

Note: The segment address must be sent at each time when read 128bytes E-EDID data.

8.5.4 Audio input configuration

HDMI transmitter audio support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz. The default audio format is I2S input with 8 channels. The audio sample rate is 44.1K.
The following describes how to configure audio input format into I2S input with 2 channels and the sample rate is 44.1K.

Audio input requirement:

SD0 input (2 Channels I2S input)
WS (fs) = 44.1 KHz
SCK = 64fs
MCLK = 256fs

Configure Audio Input Format Steps:

Step1: Select I2S input.

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Send 0x01 to register 0x35
Step2: Select SD0 input.
Send 0x04 to register 0x38
Step3: Select N/CTS for sample rate = 44.1 KHz.
Send 0x18 to register 0x40
Send 0x80 to register 0x41
The following describes how to configure audio input format into I2S input with 8 channels and the sample rate is 44.1K.
Audio input requirement:
SD[3:0] input (8 Channels I2S input)
WS (fs) = 44.1 KHz
SCK = 64fs
MCLK = 256fs
Configure Audio Input Format Steps :
Step1: Select I2S input.
Send 0x01 to register 0x35
Step2: Select SD[3:0] input.
Send 0x3c to register 0x38
Send 0x00 to register 0x39
Step3: Select N/CTS for sample rate = 44.1 KHz.
Send 0x18 to register 0x40
Send 0x80 to register 0x41

8.5.5 Video input configuration

HDMI transmitter support RGB/YCbCr 24/30/36bit video input with different resolution. The default video format is RGB24bit input at resolution of 1080P@60. The following describes how to configure video input format into RGB24bit input at resolution of 480P@60, 720P@60 or 1080P@60.
VOP dclk cannot get invert.
Video input requirement:
24bit RGB 4:4:4 Source.
Resolution is 480P@60, 720P@60 or 1080P@60.
Configure Video Input Format Steps:
Step1: Select configure for video format.
Send 0x06 to register 0x9f
Step2: Configure the AVI info to HDMI RX.
Send 0x82 to register 0xa0 //HB0
Send 0x02 to register 0xa1 //HB1
Send 0x0d to register 0xa2 //HB3
Send 0x00 to register 0xa3 //PB0: checksum is auto set, needn't set this register
Send 0x00 to register 0xa4 //PB1
Send 0x08 to register 0xa5 //PB2
Send 0x70 to register 0xa6 //PB3
Send 0x10 to register 0xa7 //PB4: VID 1920*1080P@60
Send 0x40 to register 0xa8 //PB5
Note: Select correct VID for displaying.
Send 0x02 to register 0xa7 for 720*480P@60.
Send 0x04 to register 0xa7 for 1280*720P@60.
Send 0x05 to register 0xa7 for 1920*1080I@60.
Send 0x10 to register 0xa7 for 1920*1080P@60.
Send 0x11 to register 0xa7 for 720*576P@50.
Send 0x13 to register 0xa7 for 1280*720P@50.
Send 0x14 to register 0xa7 for 1920*1080I@50.
Send 0x1 f to register 0xa7 for 1920*1080P@50.
The detail configuration for AVI information, please refer to the HDMI specification (8.2.1) and CEA-861-D (6.3).

8.5.6 Low Power Mode

HDMI Transmitter can be configured into Low Power Mode at special customer works mode.

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The following is a step by step instruction to describe how to configure our HDMI Transmitter into this mode.

Low Power Enter Steps:

Step1: HDMI Transmitter working.
Step2: Low Power analog module.
Send 0x00 to register 0xe1.//Drive disable
Send 0x17 to register 0xe0.
Step3: Assign pin_vclk = 1'b0 or 1'b1.

Low Power Quit Steps:

Step1: Reset system by pin_rst_n.
Step2: Wait Hot Plug.
Step3: Read EDID.
Step4: Active vclk through p in_vclk
Step5: Bring up analog module.
Send 0x15 to register 0xe0. //PLL power on
Send 0x14 to register 0xe0. //TX power on
Send 0x10 to register 0xe0. //BG power on
Send 0x0f to register 0xe1. //driver enable
Step6: Configuration mode reg at addr 0x00 if needed.
Step7: Configuration Video format if needed.
Step8: Configuration Audio format if needed.
Stap9: Configuration mode reg, power on digital part and select tmds_clk for configuration.
Send 0x61 to register 0x00.
Stap10: Synchronize analog module.
Send 0x00 to register 0xce.
Send 0x01 to register 0xce.

8.5.7 CEC OPERATION

The CEC line is used for high-level user control of HDMI-connected devices.
You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.
The following is a step by step instruction for CEC TX operations and CEC RX operations.

CEC TX steps

(Send the Command : Standby (0x36) for example)
Step1: Set logic address for CEC (logic address = 1).
Send 0x01 to register 0xde.
Step2: Configure the divide numbers for internal reference clock.
Send 0x03 to register 0xd4 and 0x09 to register 0xd5. See Note1 for details.
Step3: Configure the value for signal free time counter.
Send 0xd0 to register 0xdc and 0x20 to register 0xdd. See Note2 for details.
Step4: Configure point address for write CEC TX data.
Send 0x00 to register 0xd2.
Step5: Configure TX data FIFO (the Command o f Standby).
Send 0x01 to register 0xd1, then, send 0x36 to register 0xd1.
The data 0x01 is for the Header Block, in which the high 4bits is for the initiator, the low 4bits is for the destination. The data 0x36 is for the Data Block, it indicate the command for standby.
Step6: Configure TX data length of this packet. The length is 2.
Send 0x02 to register 0xd6.
Step7: Enable count CEC bus free time.
Send 0x04 to register 0xd0.
Step8: Waiting 16.8ms+4 us for CEC bus free.
If Interrupt happened for CEC line free time not satisfied. You should change to receive coming data from opposite. After this you can do CEC TX steps again.
(Note that the time for 16.8ms+4us should be compute by MCU itself)
Step9: Begin TX.
Send 0x05 to register 0xd0.
Step10: Waiting and check interrupt of CEC TX done.

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Waiting the interrupt, then, read the value of register 0xda, if the value is 0x08 that means CEC command was transmitted successfully. At last, send 0x08 to register 0xda to clear up this interrupt.

CEC RX steps:

Step1: Set logic address for CEC (logic address = 1).
Send 0x01 to register 0xde.
Step2: Configure the divide numbers for internal reference clock. See Note1 for details.
Send 0x01 to register 0xd4 and 0x01 to register 0xd5.
Step3: Configure the point address for CEC RX data.
Send 0x00 to register 0xd3.
Step4: Waiting CEC TX send CEC packet to our HDMI Transmitter, then check interrupt of CEC.Read the value of register 0xdb, if the value is 0x80, that means CEC command was received successfully. Then send 0x80 to register 0xdb to clear up this interrupt.
Step5: Read the RX packet length.
Read the value of the register 0xd7.
Step6: Read the received CEC packet.
Read the value of the register 0xd1 according to the RX packet length. If the length is 2, please read twice from the register 0xd1.

***Note1**: The system clock (Default value Fsys = 20MHz from pin_sys_clk), register 0xd4 and 0xd5 are used to configure the CEC logic to generate a reference clock (Fref=5 MHz,more or less is ok), which is used to control the CEC signal's generation. The following is the formula for generating reference clock 5MHz.*
Fref = Fsys / ((register 0xd4 + 1)(register 0xd5 + 1)). Under the default 20MHz system clock, the values of register 0xd4 and 0xd5 are 0x01 and 0x01.*

***Note2**: Before attempting to transmit or re-transmit a frame, a device shall ensure that the CEC line has be e n inactive for a number of bit periods . For example , the signal free time is 7*2.4ms=16.8ms (the bit time is 2.4 ms). According to the 16.8ms/2us = {register 0xdd, register 0xdc}, so the register 0xdd=0x20 and register*
0xdc= 0xd0.

8.5.8 HDCP OPERATION

HDCP is designed to protect the transmission of Audiovisual Content between an HDCP Transmitter and an HDCP Receiver. You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.
The following is a step by step instruction for HDCP operation.

HDCP operation steps（skip BKSV black list check）:

Example Condition: Video Format : 1920×1080p@59.94/60Hz

Step1: Select the TMDS clock to configure registers.
Send 0x61 to register 0x00.
Step2: Write HDCP transmitter's Akey to the chip. **See Note1 for details.**

```
for(i =0; i <= 39 ; i = i+ 1 )
   begin
   hdcp_wdata_temp = akey[i];
     for ( j=0 ; j < 7   ; j = j + 1 )
       begin
       Send hdcp_wdata_temp[7:0] to register 0x98;
       hdcp_wdata_temp = hdcp_wdata_temp >>8;
       end
   end
```

Step3: Write HDCP transmitter's AKSV1 to the chip. **See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv1
for (i = 0, i < 5, i = i + 1)
begin
     Send hdcp_wdata_temp[7:0] to register 0x98;
     hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

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Step4: Write HDCP transmitter's AKSV2 to the chip. **See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv2
for (i = 0, i < 5, i = i + 1)
begin
    Send hdcp_wdata_temp[7:0] to register 0x98;
    hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step5: Check the key_ready signal.

Read the value of register 0x54, if the value is 0x01,that means the Akey and AKSV were load into the chip successfully.

Step6: Configure the DDC frequency. **See Note2 for details.**

Send 0x73 to register 0x4b.

Send 0x01 to register 0x4c.

Step7: Configure the HDCP function.

Send 0x77 to register 0x53.

Step8: Open the mask for HDCP interrupt.

Send 0xff to register 0xc2.

Send 0xff to register 0xc4.

Step9: Start the HDCP authentication.

Send 0x96 to register 0x52.

Step10: Checking HDCP interrupt.

Read the value of register 0xc3 and register 0xc5, if the value of register 0xc3 is 0x10 and the value of register 0xc5 is 0x65, that is means the HDCP authentication was successfully finished.

HDCP operation steps（not skip BKSV black list check）:

Example Condition: Video Format : 1920×1080p@59.94/60Hz

Step1: Select the TMDS clock to configure registers.

Send 0x01 to register 0x00.

Step2: Write HDCP transmitter's Akey to the chip. **See Note1 for details.**

```
for(i =0; i <= 39 ; i = i+ 1 )
   begin
   hdcp_wdata_temp = akey[i];
     for ( j=0 ; j < 7   ; j = j + 1 )
       begin
       Send hdcp_wdata_temp[7:0] to register 0x98;
       hdcp_wdata_temp = hdcp_wdata_temp >>8;
       end
   end
```

Step3: Write HDCP transmitter's AKSV1 to the chip. **See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv1
for (i = 0, i < 5, i = i + 1)
begin
    Send hdcp_wdata_temp[7:0] to register 0x98;
    hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step4: Write HDCP transmitter's AKSV2 to the chip. **See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv2
for (i = 0, i < 5, i = i + 1)
begin
    Send hdcp_wdata_temp[7:0] to register 0x98;
    hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step5: Check the key_ready signal.

Read the value of register 0x54, if the value is 0x01,that means the Akey and AKSV were load into the chip successfully.

Step6: Configure the DDC frequency. **See Note2 for details.**

Send 0x73 to register 0x4b.

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Send 0x01 to register 0x4c.
Step7: Configure the HDCP function.
Send 0x37 to register 0x53(do not skip the BKSV blacklist check).
Step8: Open the mask for HDCP interrupt.
Send 0xff to register 0xc2.
Send 0xff to register 0xc4.
Step9: Start the HDCP authentication.
Send 0x96 to register 0x52.
Step10: Check the BKSV.
Wait for INT from registerc3 bit5(bksv_update),than read register66~register6a for BKSV values to check whether the BKSV is in the revocation list. If the BKSV is not in the revocation list, write 1 to register52 bit6(bksv_pass) , and authentication will continue. Else if the BKSV is in the revocation list, write 1 to register52 bit5(bksv_fail), and authentication will stop.
Step11: Checking HDCP interrupt.
Read the value of register 0xc3 and register 0xc5, if the value of register 0xc3 is 0x10 and the value of register 0xc5 is 0x65, that is means the HDCP authentication was successfully finished.

Note1: For HDCP's akey and KSV write, use the TEST KEYS in HDCP specification for example

```
akey[0] =56'h4da4588f131e69;
akey[1] =56'h1f823558e65009;
akey[2] =56'h8a6a47abb9980d;
akey[3] =56'hf3181b52cbc5ca;
akey[4] =56'hfb147f6896d8b4;
akey[5] =56'he08bc978488f81;
akey[6] =56'ha0d064c8112c41;
akey[7] =56'hb39d5a28242044;
akey[8] =56'hb928b2bdad566b;
akey[9] =56'h91a47b4a6ce4f6;
akey[10] =56'h5600f8205e9d58;
akey[11] =56'h8c7fb706ee3fa0;
akey[12] =56'hc02d8c9d7cbc28;
akey[13] =56'h561261e54b9f05;
akey[14] =56'h74f0de8ccac1cb;
akey[15] =56'h3bb8f60efcdb6a;
akey[16] =56'ha02bbb16b22fd7;
akey[17] =56'h482f8e46785498;
akey[18] =56'h66ae2562274738;
akey[19] =56'h3d4952a323ddf2;
akey[20] =56'he2d231767b3a54;
akey[21] =56'h4d581aede66125;
akey[22] =56'h326082bf7b22f7;
akey[23] =56'hf61b463530ce6b;
akey[24] =56'h360409f0d7976b;
akey[25] =56'ha1e105618d49f9;
akey[26] =56'hc98e9dd1053406;
akey[27] =56'h20c36794426190;
akey[28] =56'h964451ceac4fc3;
akey[29] =56'h3e904504e18c8a;
akey[30] =56'h290010579c2dfc;
akey[31] =56'hd7943b69e5b180;
akey[32] =56'h54c7ea5bdd7b43;
akey[33] =56'h74fb5887c790ba;
akey[34] =56'h935cfa364e1de0;
akey[35] =56'h03075e159a11ae;
akey[36] =56'h05d3408a78fb01;
akey[37] =56'h0059a5d7a04db3;
akey[38] =56'h373b634a2c9e40;
akey[39] =56'h2573bbb4562041;

pre_ksv1 = 40'hb70361f714;
pre_ksv2 = 40'hb70361f714;
```

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Note2: For DDC frequency configuration

In the HDCP specification, the frequency value of DDC(F_{ddc}) support only up to 100Kbps, and now we select the TMDS clock as the reference clock of DDC , and under the condition of 1920×1080p@59.94/60Hz, the frequency of TMDS(F_{TMDS}) is 148.5MHz. Pay attention, internally we use the 4 times of DDC frequency to generate the SCL. So

$X = F_{TMDS}/F_{ddc}/4$ = 'h173, So the values of register 0x4b and 0x4c are 0x73 and 0x01.

8.5.9 NOMAL OPERATION EXAMPLE AT 1080P

After the description of HDMI Transmitter configuration above, the following example shows an entire configuration for HDMI Transmitter works on the 1080P mode.
Audio input requirement:
SD0 input (2 Channels I2S input)
WS (fs) = 48 KHz
SCK = 64fs
MCLK = 256fs
Video input requirement:
24bit RGB 4:4:4 Source.
Resolution is 1080P@60.
Setup Steps:
Step1: Power on HDMI Transmitter.
Step2: Configure the input signals.
Assign pin_test_en = 1'b0.
Step3: Reset HDMI Transmitter.
Assign 0 to the signal pin_rst_n and then assign 1.
Step4: System power down.
Send 0x63 to register 0x00.
Step5: Detect Hot Plug In.
Step6: Read EDID.
Step7: Configure video input format.
Step8: Configure audio input format.
Step9: Assign video and audio source to HDMI Transmitter.
Step10: System power on.
Send 0x61 to register 0x00.
Step11: Now, HDMI Transmitter is ready to go. Start your operation.

8.6 Electrical Specification

HDMI Transmitter contains tunable source termination and pre-emphasis to enable high speed operation. The Transmitter meets the AC specifications below across all operating conditions specified. Rise and fall times are defined as the signal transition time between 20% and 80% of the nominal swing voltage (Vswing) of the device under test. The Transmitter intra-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1, between the true and complement signals of a given differential pair. This time difference is measured at the midpoint on the single-ended signal swing of the true and complement signals. The Transmitter intra-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1.

Table 8-4 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{REF}	Reference Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	$mV_{p.p}$
T_A	Ambient Temperature (with power applied)	0	25	70	☐

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Table 8-5 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}[1.2]	Supply Voltage 3.3V	-0.3		4.0	V
V_1[1.2]	Input Voltage	-0.3		V_{CC}+0.3	V
V_0[1.2]	Output Voltage	-0.3		V_{CC}+0.3	V
V_J[1.2]	Junction Temperature (with power applied)			125	☐

Table 8-6 Transmitter DC Characteristics at TP1

Item	Value
Single-ended high level output voltage, V_H	AV_{cc}-10mV< V_H < AV_{cc}+10mV when sink <= 165Mhz
	AV_{cc}-200mV< V_H < AV_{cc}+10mV when sink >165Mhz
Single-ended low level output voltage, V_L	(AV_{cc} – 600mV) < V_L < (AV_{cc} – 400mV) when sink < =165Mhz
	(AV_{cc} – 700mV) < V_L < (AV_{cc} – 400mV) when sink > 165Mhz
Single-ended output swing voltage, V_{swing}	400mV < V_{swing} < 600mV
Single-ended standby (off) output voltage, V_{OFF}	AV_{cc}+-10mV
Single-ended standby (off) output current, I_{OFF}	| I_{OFF}| < 10uA

Table 8-7 Transmitter AC Characteristics at TP1

Item	Value
Rise time/fall time (20%-80%)	75psec < Rise time/fall time < 0.4 T_{bit}
Overshoot, max	15% of full differential amplitude (V_{swing} *2)
Undershoot, max	25% of full differential amplitude e (V_{swing} *2)
Intra-Pair Skew at Transmitter Connector, max	0.15 T_{bit}
Intra-Pair Skew at Transmitter Connector, max	0.20 T_{pixel}
TMDS Differential Clock Jitter, max	0.25 T_{bit}
Clock duty cycle	40% to 60%

Table 8-8 Programmable Output Resistance and Output Equalization Level

Item	Value
Output Equalization level	10% to 60%
Termination Resistance	50ohm and 75 ohms selectable with fine steps
Output Swing Ranges	4 different levels

8.6.1 CONTROL SIGNAL - DDC

DDC (Display Data Channel) control signals follow the I2C Bus specifications. More details to be filled out from I2C specs.

Table 8-9 DDC AC Characteristics

Item	Value
High Voltage Level (Vih)	-3.0V < Vih < 3.8V

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Item	Value
Low Voltage Level (Vil)	-0.5V < Vil < 1.5V
SCL clock frequency	100KHz (max)
Rise time	< 1000ns
Fall time	< 300ns
Capacitive load on bus line	400pF

8.6.2 CONTROL SIGNAL - HPD

HPD (Hot Plug Detect) signal is used by the source to read the sink's E-DID. The sink needs to meet the following requirements for reliable detection.

For Sink

Table 8-10 HPD Voltage Characteristics for sink

Item	Value
High Voltage Level (Vih)	2.4V < Vih < 5.3V
Low Voltage Level (Vil)	0V < Vil < 0.4V

For Source

Table 8-11 HPD Voltage Characteristics for source

Item	Value
High Voltage Level (Voh)	2.0V < Voh < 5.3V
Low Voltage Level (Vol)	0V < Vol < 0.8V

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Chapter 9 HDMI RX CONTROLLER

9.1 Overview

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.
HDMIRX controller is fully compliant with HDMI 1.4a specification/HDMI2.0 specification. It offers a simple implementation for consumer electronics like DVD/player/recorder and camcorder.
It supports the following features:

- HDMI 1.4/HDMI 2.0, HDCP 1.4
- Supports rgb/yuv444/yuv422/yuv420,up to 4k(4096x2304)
- Supports data rates up to 297MHZ, with phy bit rate 2.97Ghz
- Supports all resolutions including 480p /576p /720p /1080p/4k
- Supports one cycle dual pixel output
- Supports 8bit depth,10bit depth(just yuv420/yuv422)
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support EDID and CEC function

9.2 Block Diagram

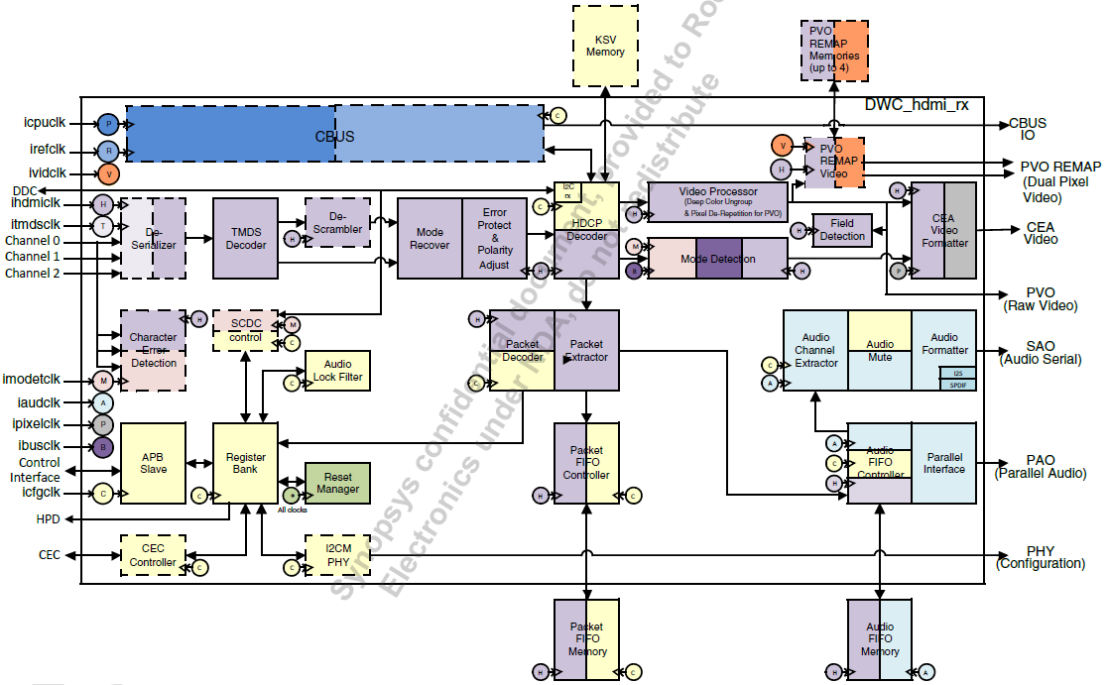

Fig. 9-1 HDMI TX Block Diagram

9.3 Memory

Table 9-1 HDMI RX memory

Module ID	Memory Name	Freq	Deep	Width	wclk	rclk
Audio fifo	G28SLPDPRF1538X30	340MHz/ 600MHz	1538	30	ihdmiclk	iaudclk
Packet fifo	G28SLPDPRF738X32	340MHz/ 600MHz	738	32	ihdmiclk	icfgclk
PVO remap fifo	G28SLPDPRF4096X48 (SIMPLE)	600MHz	2048	48	ihdmiclk	ividclk

9.4 clk

Table 9-2 HDMI RX clk

clk	min freq	typical freq	max freq	description
iaudclk	4.096M	-	196.608M	audio clk
ibusclk	25M	-	600M	hdmi link clk
icecclk	32.709k	32.768k	32.776k	cec clk
icfgclk	100M	100M	300M	register clk(apb clk)
ihdmiclk	25M	-	600M	hdmi link clk
imodetclk	10M	-	50M	mode detection clk
itmdsclk	25M	-	600M	tmds link clk
ividclk	25M	-	600M	output video clk

ividclk and ihdmiclk have constraints based on video format.

Table 9-3 HDMI ividclk freq with ihdmiclk

video format	pixel mode	ividclk freq
YCbCr420	single pixel	2*ihdmiclk
	dual pixel	ihdmiclk
RGB444 YCbCr444/YCbCr422	single pixel	ihdmiclk
	dual pixel	ihdmiclk/2

9.5 interface signal

Table 9-4 Interface signal

signal	I/O	description
clk/reset		
imodetclk	I	Mode Detection Unit clock
icfgclk	I	Register Configuration clock
iaudclk	I	Audio Unit clock
ihdmiclk	I	HDMI link-related clock, PLL buffer
ibusclk	I	HDMI link clock, non PLL buffer
ipixelclk	I	CEA pixel clock
itmdsclk	I	MHL TMDS link related clock
irefclk	I	CBUS Reference clock
ividclk	I	PVO Remapped Video clock
ipon_rst_n	I	Configuration interface and major power reset
phy		
ophy_scl	O	scl clk output for phy
ophy_sda	O	scl data output for phy
iphy_sda_pull_dn_n	I	phy ack/nack for hdmi_rx controller
ophy_i2c_slave_addr[6:0]	O	i2c slave address
ophy_phy_reset	O	phy reset
ophy_pddq	O	power down all analog blocks and reset digital circuit data path
ophy_port_select[1:0]	O	phy port select
ophy_cfgclk_freq[1:0]	O	system clock frequency configuration preset
ophy_svsret_modez	O	reserved
system signal		
ohdmi_int	O	global hdmi interrupt
ohot_plug_detect_a	O	hot plug detect output for HDMI source input A
ohot_plug_detect_b	O	hot plug detect output for HDMI source input B(no used)
ohot_plug_detect_c	O	hot plug detect output for HDMI source input C(no used)
ohot_plug_detect_d	O	hot plug detect output for HDMI source input D(no used)

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signal	I/O	description
ocfg_clk_meas_input_src	O	output signal identifying which HDMI input(A or B) is used for ibusclk clock measurement 0: input A 1: input B
tmds		
itmdsvalid	I	indicate that the PHY has completed its power-up sequence and its output data is valid
itmdsdata0[9:0]	I	TMDS data0
itmdsdata1[9:0]	I	TMDS data1
itmdsdata2[9:0]	I	TMDS data2
apb3 interface		
iapb_rst_n	I	apb bus clk is icfgclk
iapb_psel	I	
iapb_penable	I	
iapb_pwrite	I	
oapb_pready	O	
oapb_pslverr	O	
iapb_paddr[31:0]	I	
iapb_pwdata[31:0]	I	
oapb_prdata[31:0]	O	
Remapped PVO interface		
opvox_data[47:0](x=0,1)	O	pvo data
opvox_dataen	O	pvo data enable
opvox_valid	O	pvo valid
opvox_hsync	O	pvo horizontal sync
opvox_vsync	O	pvo vertical sync
opvox_field	O	pvo field indication
opvox_colordepth[3:0]	O	pvo color depth indication
opvox_format[2:0]	O	pvo format
audio interface		
oaud_spdif[3:0]	O	spdif output
oaud_i2s[3:0]	O	i2s output
oaud_ws	O	word select for i2s audio data
oaud_sck	O	clock line for i2s audio data
oaud_extmute	O	audio external mute
oaud_data[27:0]	O	audio data
oaud_ctrl[1:0]	O	
oaud_fmt[2:0]	O	audio format
oaud_valid	O	audio valid
oaud_clk	O	audio clock reference = iaudclk(128fs)
oaud_sp_st	O	audio sub-packet start,which used to indicate odd/even sample/audio data
oaud_sp_idx[1:0]	O	audio sample subpacket index
ost_amp_chg	O	pulse that indicates when a changed audio metadata packet has been received。
audio pll		
iaud_pll_lock	I	lock indicator form an external audio pll
icfg_audpll_stsbus[63:0]	I	audio pll generic interface status
oaud_pll4x_en	O	pll value multiply 4 enable
ocfg_audpll_mux_cts[19:0]	O	audio pll CTS value
ocfg_audpll_mux_n[19:0]	O	audio pll N value
ocfg_audpll_ctrlbus[63:0]	O	audio pll control signal
ocfg_audpll_p_ctrlbus[31:0]	O	audio pll pulse control signal

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signal	I/O	description
ocfg_audpll_afif_thpass	O	audio fifo threshold pass status
ocfg_audpll_afif_thmin	O	audio fifo threshold min status
ocfg_audpll_afif_thmax	O	audio fifo threshold max status
cec interface		
icecclk	I	cec interface clock
icecin	I	cec interface data in
ocecout	O	cec interface data output
hdcp interface		
ihdcp_scl_a	I	DDC clock input
ihdcp_sda_a	I	DDC data input
ihdcp_scl_b	I	DDC clock input
ihdcp_sda_b	I	DDC data input
ihdcp_scl_c	I	DDC clock input
ihdcp_sda_c	I	DDC data input
ihdcp_scl_d	I	DDC clock input
ihdcp_sda_d	I	DDC data input
ohdcp_scl_out_a	O	DDC clock output
ohdcp_sda_out_a	O	DDC data output
ohdcp_scl_out_b	O	DDC clock output
ohdcp_sda_out_b	O	DDC data output
ohdcp_scl_out_c	O	DDC clock output
ohdcp_sda_out_c	O	DDC data output
ohdcp_scl_out_d	O	DDC clock output
ohdcp_sda_out_d	O	DDC data output
ohdcp_auth_start	O	HDCP authentication state
ohdcp_enc_state	O	hdcp video field encryption state
scan interface		
iscanclk	I	scan clock
iscanen	I	scan enable
iscanrst_n	I	scan reset
iscanin_ctrl	I	scan control input
iscanmode	I	scan mode
oscanout_ctrl	O	scan control output

9.6 Function Description

HDMI rx controller separates the incoming data stream into audio data,video data,and packet data information.It configures itself automatically based on the packet data information received,with no software intervention.You can also configure it manually by using the register interface.The controller has an hdcp1.4 encryption/decryption engine and optional CEC controller.

9.6.1 hdmirx_preprocess

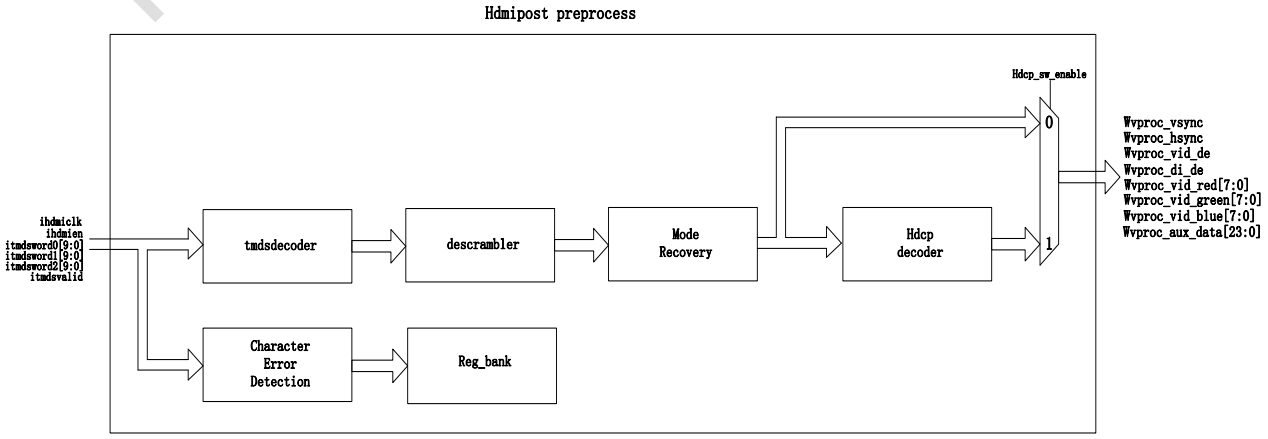

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Fig. 9-2 HDMI RX preprocess data stream

tmdsdecoder module will conduct tmds decoded,convert 10bit to 8bit and extract r/g/b three data channel, and hsync/vsync, and controller data.
descrambler module will conduct de_scramble which just enable when tmdsclk >= 340M.
mode_recovery module will depart video period,data island period,control data period, and output the corresponding indication signal. Signal ovid_de_no_gb indicates it is video period without video guard band period, signal odi_de_no_gb indicates it is data island period without data island guard band period.
hdcp decoder module will conduct hdcp 1.4 decode process.
hdmirx preprocess will output the video data, data island data and control data.

9.6.2 Hdmirx_postprocess

hdmirx_postprocess will process video,audio, packet data dividedly. Once the incoming payload has passed the pre-processing steps,including hdcp, it is split into parallel processing streams for video, packet, and audio data. This kind of post-processing implements hardware accelerated stream preparation in any related SoC memory infrastructure without software interaction.

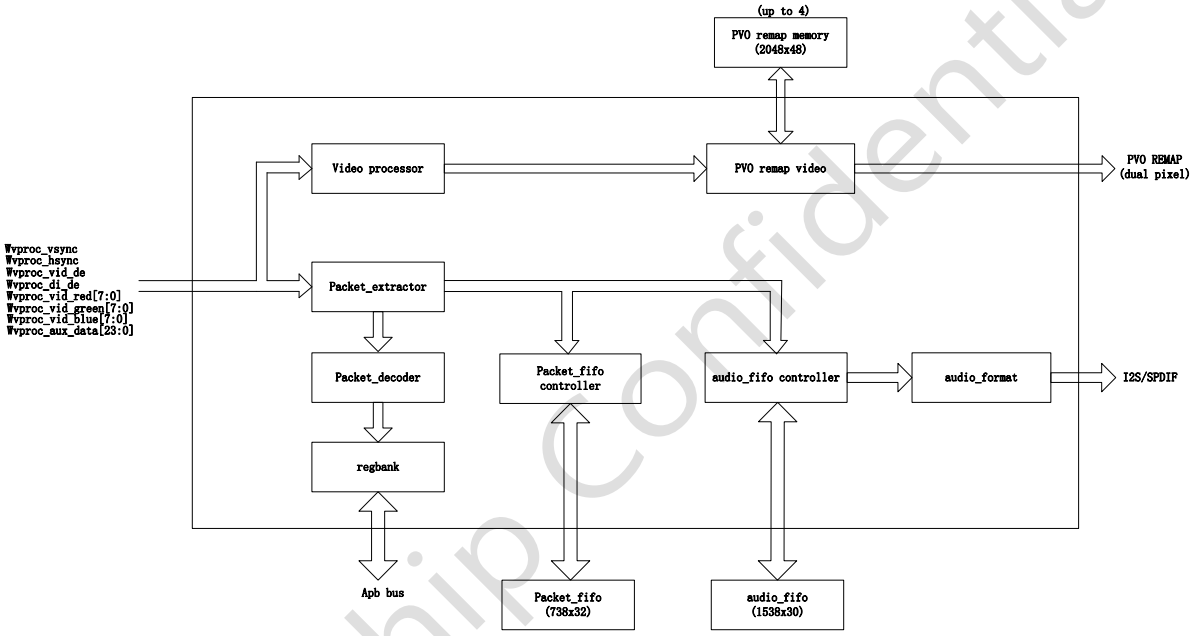

Fig. 9-3 HDMI RX postprocess data stream

packet extractor module will extract packet data and audio data. packet data will be decoded and apb bus can access these packet data in regbank.audio data will be stored in audio fifo.
The audio_format module will read audio_fifo and reframe i2s.
1.audio/packet data
The different packet type include ACR/GCP and so on,which in table below.

Table 9-5 Packet type

Abbr	full_name	description
NULL		null packet,the most lowest priority packet
GCP	General Control packet	include AVMUTE，color_depth，pixel_packing phase
ACP	Audio Content Protection	acp_type,0:generic audio, 1:IEC 60958 Audio,2:DVD-Audio,3:Super Audio
ISRC1	ISRC:International Standard Recoding Code	send UPC/EAM or ISRC encoder
ISRC2		send UPC/EAM or ISRC encoder
VSD	Vendor Specific Data Block	send 24bit IEEE Registration Identifier and vendor information
AVI	Auxiliary Video Information InfoFrame	send auxiliary video information

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Abbr	full_name	description
SPD	Source Data Product Descriptor InfoFrame	Name and product type of the source device。
AUDI	Audio InfoFrame	channel count,sample frequency, channel/speaker allocation, level shift value,downmix inhibit, LFEPBL0, LFEPBL1。
ACR	Audio Clock Regeneration	send N and CTS value for audio clk regenerator
AUDS	Audio sample	audio data
GMD	Gamut Metadata	send Gamut boundary descriptions(GBD) and other gamut-related metadata
NVBI	NTSC VBI packet	
DRM	Dynamic Range and Master	
AMP	Audio Metadata packet	
MPEG	MPEG Source InfoFrame	

I2S output support up to 8 channel, the timing in below diagram.

Figure 5-36 I²S Timing Diagram

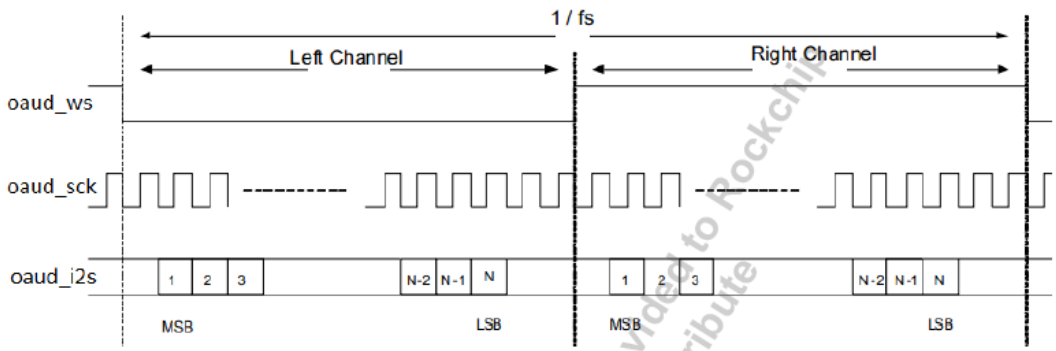

Fig. 9-4 HDMI RX I2S output timing

the serial audio sample rate in below diagram.

Table 9-6 Serial audio output interface bit rates

audio sampling	Bit Rate	BI phase
fs(kHz)	64xfs(Mbps)	Coding Rate 2x64xfs(MHZ)
32	2.048	4.096
44.1	2.8224	5.6448
48	3.072	6.144
88.2	5.6448	11.2896
96	6.144	12.288
176.4	11.2896	22.5792
192	12.288	24.576

2.video data

video data data stream in diagram below.

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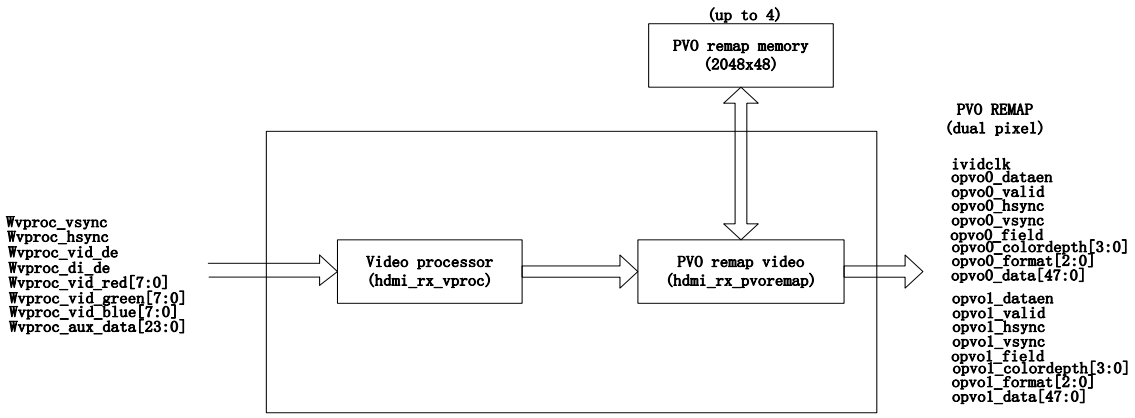

Fig. 9-5 HDMI RX video data stream

video output type is one cycle two pixel.

2.1 video_processor

The video_processor module(hdmi_rx_vproc) will convert data which is 8bit one cycle to 16bit one cycle, even the valid bit is 10/12/16bit one cycle, based on format/colordepth/pixel_phase. Before video_processor, it is one 8bit data one cycle, and after this module, it is one pixel one cycle, and all the pixel will be 16bit with low bit padding 0.

(1)color deep and pixel phase

Table 6-2 Pixel Packing Phase (PP field) Values

PP3	PP2	PP1	PP0	Pixel packing Phase
0	0	0	0	Phase 4 (10P4)
0	0	0	1	Phase 1 (10P1, 12P1, 16P1)
0	0	1	0	Phase 2 (10P2, 12P2)
0	0	1	1	Phase 3 (10P3)
0	1	0	0	Reserved
All other values				Reserved

CD3	CD2	CD1	CD0	Color Depth
0	0	0	0	Color Depth not indicated
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	24 bits per pixel
0	1	0	1	30 bits per pixel
0	1	1	0	36 bits per pixel
0	1	1	1	48 bits per pixel
All other values				Reserved

Fig. 9-6 HDMI RX video color depth and pixel phase

The valid data will be broken when the color depth is 10bit/12bit/16bit.The timing in diagram below.

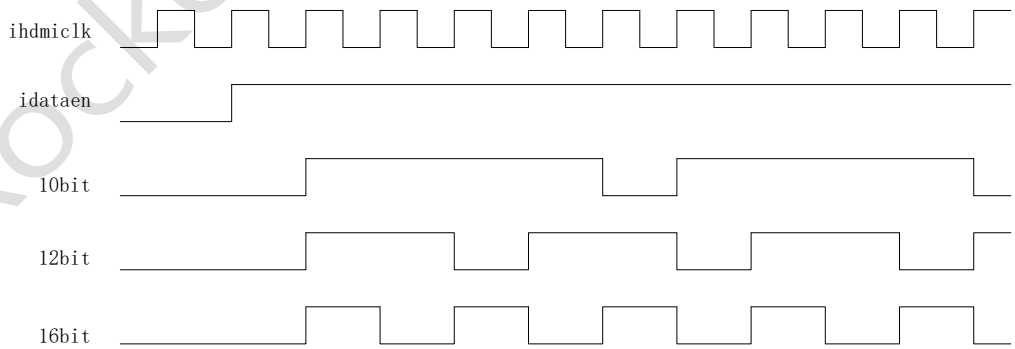

Fig. 9-7 HDMI RX video broken data valid with different colordepth

The pixel phase is the valid data stage, which tx start to divide the 10bit/12bit/16bit valid to 8bit,so if the hdmirx pixel phase different from hdmitx pixel phase, hdmirx will not pad the 10bit/12bit/16bit,and it wil be wrong. So hdmirx must detect the hdmitx pixel phase firstly, if the pixel phase match, the hdmirx 10bit/12bit/16bit will be extracted correctly.

The hdmitx send the pixel phase through GCP packet, which is ipdec_pixel_phase[3:0]. The hdmirx detect the pixel phase, and will lock it, which is ocfg_dcm_last_pixel_phase[3:0]. If these two signal match, the hdmirx will extract 10bit/12bit/16bit data correctly, or the received data will be wrong, with pixel number error.

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In the example above, the hdmirx extract pixel data correctly in third frame beginning, and the first frame, second frame may be wrong.

2.2video remap

video remap will upsample the yuv420/yuv422 to yuv444,and output data is one cycle dual pixel.

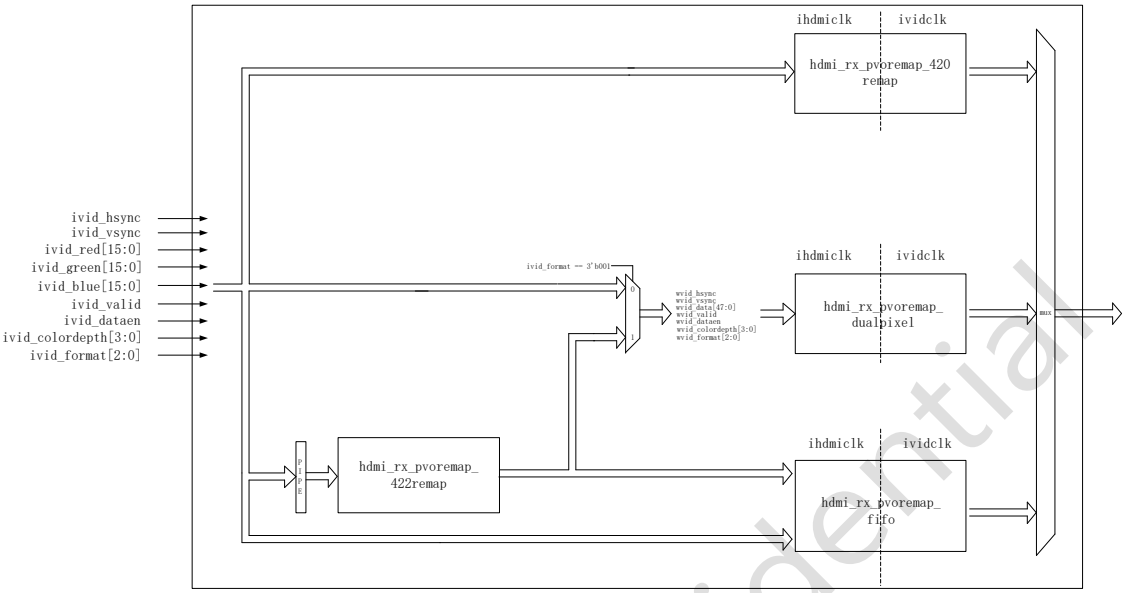

Fig. 9-8 HDMI RX video remap data stream

hdmi_rx_pvoremap_422remap module upsample yuv422 to yuv444, and hdmi_rx_pvoremap_fifo module output one cycle one pixel for yuv422/yuv444/rgb format, hdmi_rx_pvoremap_dualpixel module output one cycle two pixel for yuv422/yuv444/rgb format.for yuv422, it has been upsample to yuv444. hdmi_rx_pvoremap_420remap module output one cycle one pixel or one cycle dual pixel for yuv420 format.

yuv420/yuv422 upsample to yuv444 just in copy way.

a.hdmi_rx_pvoremap_fifo

This module output one cycle one pixel for yuv422/yuv444/rgb format. it just use memory0 and memory1.memory 0 stores data and memory1 stores control signal hsync/vsync/dataen/format/colordepth.

b.hdmi_rx_pvoremap_dualpixel

line0 pixel0 stores in memory0 addr 0, line0 pixel1 stores in memory1 addr 0, line0 pixel2 stores in memory0 addr 1, line0 pixel3 stores in memory1 addr 1, until line0 stored in memory0/memory1. line1 stored in memory2/memory3 on the same way.

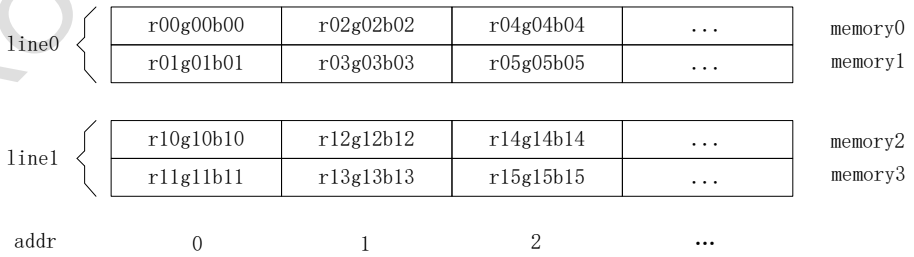

Fig. 9-9 HDMI RX video remap dual pixel fifo stored logic

after store line0 in memory0/memory1, when store the line1 in memory2/memory3, it will read the memory0/memory1 and output line0.

so write line1, output line0, write line2, output line1, and one cycle read two memory and output the odd/even adjacent pixel in one cycle.

c.hdmi_rx_pvoremap_420remap

this module upsample yuv420 to yuv444, and output one cycle two pixel,the logic on the

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same way above.

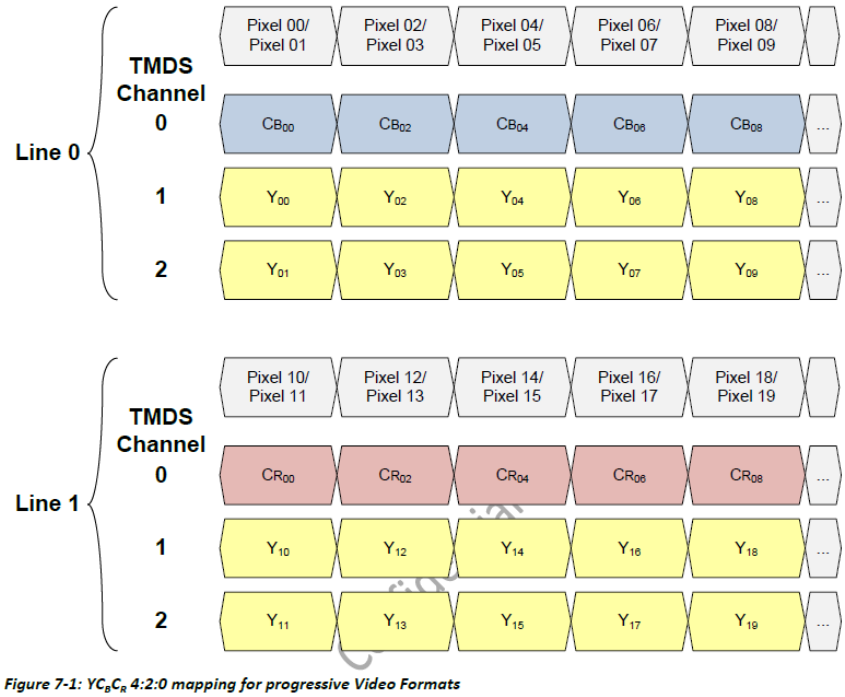

Fig. 9-10 YUV420 pixel map logic in three channel

d.video output clock

ihdmiclk and ividclk have fixed constraints based on format.

Table 9-7 HDMI ividclk freq based on format

video format	pixel mode	ividclk freq
YCbCr420	single pixel	2*ihdmiclk
	dual pixel	ihdmiclk
RGB444 YCbCr444/YCbCr422	single pixel	ihdmiclk
	dual pixel	ihdmiclk/2

ipixelclk and ihdmiclk have fixed constraints based on colordepth.

Table 9-8 HDMI ividclk freq based on format

opvo0_colordepth[3:0]	ivid_clk/ipclk(hdmi_tx_bfm source clk)
4'b5(10bit)	1.25 (10/8)
4'b6(12bit)	1.5 (12/8)
4'b7(16bit)	2 (16/8)

In 10bit pixel format ipixelclk is 148.5M, and ividclk(ihdmiclk) is 185.460M, it is 1.25 times constraints.

If it is yuv420 10bit in 4k resolution, the ipixelclk is 297M, because it has half of yuv444 total data. And ihdmiclk is 297M*1.25 = 371.25M. If the output type is one cycle one pixel, the vidclk will be 371.25M*2 = 742.5M, it is too fast, so if we choose one cycle two pixel, ividclk is 371.25M, and it is easy for user to release.

9.7 Register Description

9.7.1 Register Summary

Name	Offset	Size	Reset Value	Description
HDMI_RX_HDMI_SETUP_CTRL	0x0000	W	0x0d000000	HDMI Setup Control Register You can use this register to enable/send out HPD, reset overrides, regulate Equalizer OSM, use PLL lock, and control the force state

Name	Offset	Size	Reset Value	Description
HDMI_RX_HDMI_OVR_CTRL	0x0004	W	0x00000000	HDMI Override Control Register
HDMI_RX_HDMI_TIMER_CTRL	0x0008	W	0x00000278	HDMI Timing Control Register
HDMI_RX_HDMI_RES_OVR	0x0010	W	0x00000000	HDMI Resistor Override Register
HDMI_RX_HDMI_RES_STS	0x0014	W	0x00000000	HDMI Resistor Status Register
HDMI_RX_HDMI_PLL_CTRL	0x0018	W	0x00000000	HDMI TMDS PLL Control Register
HDMI_RX_HDMI_PLL_FRQSET1	0x001c	W	0x72523121	Register0000 Description
HDMI_RX_HDMI_PLL_FRQSET2	0x0020	W	0x00000000	HDMI TMDS PLL Frequency Range Register 2
HDMI_RX_HDMI_PLL_PAR1	0x0024	W	0x00000000	HDMI TMDS PLL PCP and ICP Range Register 1
HDMI_RX_HDMI_PLL_PAR2	0x0028	W	0x788796a6	HDMI TMDS PLL PCP and ICP Range Register 2
HDMI_RX_HDMI_PLL_PAR3	0x002c	W	0x7ecba998	HDMI TMDS PLL KOSC and CCOLF Range Register
HDMI_RX_HDMI_PLL_LCK_STS	0x0030	W	0x00000000	HDMI Post Lock Filter Register You can use this register to read several values for PLL such as the frequency index, clock gate, protection, configuration, and lock status
HDMI_RX_HDMI_CLK_CTRL	0x0034	W	0x00000000	HDMI PLL Clock Control Register
HDMI_RX_HDMI_PCB_CTRL	0x0038	W	0x00000000	HDMI PCB Diversity Control Register
HDMI_RX_HDMI_PHS_CTR	0x0040	W	0x00000000	HDMI Phase Control Register You can select phases for channels, read the averaging constant and the position of the phase decision window, control the phase shifts, select the phase extraction methodology, and control the noise and equalization
HDMI_RX_HDMI_PHS_USED	0x0044	W	0x00000000	HDMI Used Phases Register

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Name	Offset	Size	Reset Value	Description
HDMI_RX_HDMI_MISC_CTRL	0x0048	W	0x00000000	HDMI Miscellaneous Operations Control Register.You can use hdmi_misc_ctrl to select the channel, phase, and bus for a debug operation, to control the pixels and color lines, along with error detection
HDMI_RX_HDMI_EQOFF_CTRL	0x004c	W	0x00000000	HDMI Equalizer Offset Register You can use hdmi_eqoff_ctrl to select the channel for equalizer offset and gain measurements, to override offset for channels, and to start offset calibration
HDMI_RX_HDMI_EQGAIN_CTRL	0x0050	W	0x00000000	HDMI Equalizer Gain Control Register You can control the equalizer gain by using hdmi_eqgain_ctrl. You can control the output buffer gain, the LSB gain, level shifter peaking, adaptive equalizer algorithm, overrides, sync words, video duration, calibration, number of edges, decision directions, and switch between stages A and B
HDMI_RX_HDMI_EQCAL_STS	0x0054	W	0x00000000	HDMI Equalizer Calibration Status Register You can read the equalizer calibration status by using hdmi_eqcal_sts. It stores information about the calibration offset per channel and offset status
HDMI_RX_HDMI_EQRESULT	0x0058	W	0x00000000	HDMI Equalizer Results Register You can use hdmi_eqresult to read the results of the equalization process
HDMI_RX_HDMI_EQ_MEAS_CTRL	0x005c	W	0x00060000	HDMI Equalizer Measurement Control Register You can control the eye quality factor, the stddev evaluation method, and the measurements per evaluation along with PLL debug
HDMI_RX_HDMI_WR_CFG	0x0060	W	0x00000000	HDMI write configuration register
HDMI_RX_HDMI_CTRL	0x0064	W	0x000000ff	HDMI Control Register

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Name	Offset	Size	Reset Value	Description
HDMI_RX_HDMI_MODE_RECOVER	0x0080	W	0x00000000	HDMI Mode Recover Register You can use the hdmi_mode_recover register to control the vsync polarity, spike filter, mode detection, band detection, OESS, EESS, and signal overwrite
HDMI_RX_HDMI_ERROR_PROTECT	0x0084	W	0x00000000	HDMI Error Protection Register You can use the hdmi_error_protect register to hold or pass signals, to select valid channels, to control VS, HS and DE stability filter order, and DE regeneration
HDMI_RX_HDMI_ERD_STS	0x0088	W	0x00000000	HDMI Validation and Production Test Register
HDMI_RX_HDMI_SYNC_CTRL	0x0090	W	0x00000000	HDMI Video Output Sync Signals Control Register You can use hdmi_sync_ctrl to control the VS and HS polarity and to enable the VS delay
HDMI_RX_HDMI_CKM_EVLTM	0x0094	W	0x0010fff0	HDMI Clock Measurement Register
HDMI_RX_HDMI_CKM_F	0x0098	W	0x00000000	HDMI Legal Clock Register This register has no functional impact over GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs operation. Nevertheless they might be used to identify HDMI clock deviations or HDMI clock rate discovery for system level software purposes
HDMI_RX_HDMI_CKM_RESULT	0x009c	W	0x00000000	HDMI Measured Clock Results Register This register has no functional impact over GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs operation. Nevertheless they might be used to identify HDMI clock deviations or HDMI clock rate discovery for system level software purposes
HDMI_RX_HDMI_PVO_CONFIG	0x00a0	W	0x00000000	HDMI PVO Configuration Register(Exists: HRX_PVO_REMAP_N==1)
HDMI_RX_HDMI_RESMPL_CTRL	0x00a4	W	0x00000000	HDMI De-Repeat Subsampling Control Register

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Name	Offset	Size	Reset Value	Description
HDMI_RX_HDMI_DCM_CTRL	0x00a8	W	0x00000000	HDMI Deep Color Control Register You can reset the phase difference counter, control the phase re-alignment, and control the deep color mode depth, phase, and operation.Note: In MHL operation, this register has no functionality and the values of all these fields are ignored by the HDMI/MHL RX core
HDMI_RX_HDMI_VM_CFG_CH_0_1	0x00b0	W	0x00000000	HDMI Video Output Mute Configuration Register 1
HDMI_RX_HDMI_VM_CFG_CH2	0x00b4	W	0x00000000	HDMI Video Output Mute Configuration
HDMI_RX_HDMI_SPARE	0x00b8	W	0x00000000	HDMI Spare Registers
HDMI_RX_HDMI_STS	0x00bc	W	0x00000000	HDMI Status Register You can read values or status of HDMI configurations by using hdmi_sts
HDMI_RX_HDCP_CTRL	0x00c0	W	0x00000000	HDCP Control Register You can configure various HDCP settings with hdcp_ctrl like the FSM state, AV mute test settings, and encryption mode
HDMI_RX_HDCP_SETTINGS	0x00c4	W	0x00011374	HDCP Settings Register You can use hdcp_settings to configure settings such as the spike suppression mode, I2C transfers, EESS, Advance Cipher and Enhanced Link Verification options
HDMI_RX_HDCP_SEED	0x00c8	W	0x00000000	HDCP Decryption Seed Register
HDMI_RX_HDCP_BKSV1	0x00cc	W	0x00000000	HDCP Receiver Key Selection Vector Register 1(Exists: HDCP_SWDKSET==1)
HDMI_RX_HDCP_BKSV0	0x00d0	W	0x00000000	HDCP Receiver Key Selection Vector Register 0(Exists: HDCP_SWDKSET==1)
HDMI_RX_HDCP_KIDX	0x00d4	W	0x00000000	HDCP Key Index Register
HDMI_RX_HDCP_KEY1	0x00d8	W	0x00000000	HDCP Encrypted Key Index Register 1(Exists: HDCP_SWDKSET==1)
HDMI_RX_HDCP_KEY0	0x00dc	W	0x00000000	HDCP Encrypted Key Index Register 0(Exists: HDCP_SWDKSET==1)
HDMI_RX_HDCP_DBG	0x00e0	W	0x00000000	HDCP Debug Register
HDMI_RX_HDCP_AKSV1	0x00e4	W	0x00000000	HDCP Transmitter Key Selection Vector Register 1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_HDCP_AKSV0	0x00e8	W	0x00000000	HDCP Transmitter Key Selection Vector Register 0
HDMI_RX_HDCP_AN1	0x00ec	W	0x00000000	HDCP Session Random Number Register 1
HDMI_RX_HDCP_AN0	0x00f0	W	0x00000000	HDCP Session Random Number Register 0
HDMI_RX_HDCP_EESS_WOO	0x00f4	W	0x021601ff	HDCP WOO EESS Mode Register You can use this register to fine-tune non-standard conditions on the window of opportunity (WOO) or to debug them. The reset values (of woo_end and woo_start) are the typical conditions. The configured values must be the number of pixels minus one (example: 512 pixels must be configured as 511)
HDMI_RX_HDCP_I2C_TIMEOUT	0x00f8	W	0x00000000	HDCP I2C Slave Timeout Control Register
HDMI_RX_HDCP_STS	0x00fc	W	0x00000000	HDCP Status Register
HDMI_RX_MD_HCTRL1	0x0140	W	0x00000110	Video Mode Control Register 1You can use md_hctrl to regulate the interrupt threshold, active length, and reference for measurements for various signals
HDMI_RX_MD_HCTRL2	0x0144	W	0x00000000	Video Mode Control Register 2
HDMI_RX_MD_HT0	0x0148	W	0x00000000	Horizontal Time Register 0You can read the time spent and sync time in horizontal clocks by using md_ht0
HDMI_RX_MD_HT1	0x014c	W	0x00000000	Horizontal Time Register 1 You can read the time spent and sync time in pixel clocks by using md_ht1
HDMI_RX_MD_HACT_PX	0x0150	W	0x00000000	Horizontal Active Length RegisterYou can use md_hact_px to measure the active lengths of HS and DE
HDMI_RX_MD_HACT_RSV	0x0154	W	0x00000000	Register0000 Description
HDMI_RX_MD_VCTRL	0x0158	W	0x00000000	Vertical Measurement Mode Control Register You can use md_hact_vctrl to select the VS offset, reference edge, and vertical measurement mode

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Name	Offset	Size	Reset Value	Description
HDMI_RX_MD_VSC	0x015c	W	0x00000000	Vertical Timing Sync Pulse Duration Register
HDMI_RX_MD_VTC	0x0160	W	0x00000000	Vertical Timing Frame Duration Register
HDMI_RX_MD_VOL	0x0164	W	0x00000000	Vertical Offset Line Mode Register
HDMI_RX_MD_VAL	0x0168	W	0x00000000	Vertical Active Lines Register
HDMI_RX_MD_VTH	0x016c	W	0x00000812	Vertical Lines Interrupt Threshold Register
HDMI_RX_MD_VTL	0x0170	W	0x00000000	Vertical Total Lines Register
HDMI_RX_MD_IL_CTRL	0x0174	W	0x00000000	Register0000 Description
HDMI_RX_MD_IL_SKEW	0x0178	W	0x00000000	Horizontal/Vertical Skew Register You can read the skew between VS and HS, and the skew measurement activity by using the register md_il_skew
HDMI_RX_MD_IL_POL	0x017c	W	0x00000000	H/V Skew and Field Detection Register
HDMI_RX_MD_STS	0x0180	W	0x00000000	Video Mode Status Register You can read the status of the active interlaced, DE, HS, and VS signals by using the register md_sts
HDMI_RX_AUD_CTRL	0x0200	W	0x00000000	Audio Clock Power Mode Register
HDMI_RX_AUD_PLL_CTRL	0x0208	W	0x00000000	Audio PLL Clock Control Register
HDMI_RX_AUD_CLK_CTRL	0x0214	W	0x00000000	Audio Clock Source Select Register You can choose the CTS and N value sources and the audio clock source by using the register iaudclk_ctrl
HDMI_RX_AUD_CLK_STS	0x023c	W	0x00000000	Audio Clock Status Register You can choose the CTS and N value sources and the audio clock source by using the register iaudclk_ctrl
HDMI_RX_AUD_FIFO_CTRL	0x0240	W	0x00000000	Audio FIFO Control Register
HDMI_RX_AUD_FIFO_TH	0x0244	W	0x00000000	Audio FIFO Threshold Register You can control the minimum and maximum fill-state threshold by using the register aud_fifo_th
HDMI_RX_AUD_FIFO_FILL_S	0x0248	W	0x00000000	Audio FIFO Fill Register
HDMI_RX_AUD_FIFO_CLR_MM	0x024c	W	0x00000000	Audio FIFO Fill Min/Max clear Register

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Name	Offset	Size	Reset Value	Description
HDMI_RX_AUD_FIFO_FILL_STS	0x0250	W	0x00000000	Audio FIFO Fill State Register You can use aud_fifo_fillsts to read the current, minimum, and maximum detected fill state
HDMI_RX_AUD_CHEXTR_CTRL	0x0254	W	0x00000000	Audio Output Interface Configuration Register You can control output channel mapping, configuration, and layouts by using the register aud_chextr_ctrl
HDMI_RX_AUD_MUTE_CTRL	0x0258	W	0x00000000	Audio Mute Control Register You can control various mute functions such as shadowing control, automatic clock mute, time period, types, and test-tone frequencies by using aud_mute_ctrl
HDMI_RX_AUD_FIFO_FILL_STS1	0x025c	W	0x00000000	Audio FIFO Fill Status Register 1
HDMI_RX_AUD_SAO_CTRL	0x0260	W	0x000007fe	Serial Audio Interface Output Control Register
HDMI_RX_AUD_PAO_CTRL	0x0264	W	0x00000000	Parallel Audio Output Format Register You can control the programmable thresholds and PAO format information by using aud_pao_ctrl
HDMI_RX_AUD_SPARE	0x0268	W	0x00000000	Audio Spare Status Information Register
HDMI_RX_AUD_FIFO_STS	0x027c	W	0x00000000	Audio FIFO Status Register You can read the FIFO overflow, underflow, and threshold conditions by using the register aud_fifo_sts
HDMI_RX_AUDPLL_GEN_CTS	0x0280	W	0x00000000	Audio PLL Generic Manual CTS Value The manual value set in this register only takes effect if the aud_clk_ctrl.cts_n_ref register is set to 1 (manual mode enable). You can read the FIFO overflow, underflow, and threshold conditions by using the register aud_fifo_sts.(Exists: HRX_AUDPLL_GENERIC==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_AUDPLL_GEN_N	0x0284	W	0x00000000	Audio PLL Generic Manual N Value Register The manual value set in this register only takes effect if the aud_clk_ctrl.cts_n_ref register is set to 1 (manual mode enable). For more information about the Audio PLL, refer to the HDMI RX Audio PLL .Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_GENERIC==1)
HDMI_RX_AUDPLL_GEN_CTRL_RW1	0x0288	W	0x00000000	Audio PLL Generic Control Bus 1 Register For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_GENERIC==1)
HDMI_RX_AUDPLL_GEN_CTRL_RW2	0x028c	W	0x00000000	Audio PLL Generic Control Bus 2 Register For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_GENERIC==1)
HDMI_RX_AUDPLL_GEN_CTRL_W1	0x0298	W	0x00000000	Audio PLL Generic Pulse Control Bus Register For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_GENERIC==1)
HDMI_RX_AUDPLL_GEN_STS_RO1	0x02a0	W	0x00000000	Audio PLL Generic Status Bus 1 Register For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(HRX_AUDPLL_GENERIC==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_AUDPLL_GEN_STS_RO2	0x02a4	W	0x00000000	Audio PLL Generic Status Bus 2 Register For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_GENERIC==1)
HDMI_RX_AUDPLL_SC_NDIVCTSTH	0x02a8	W	0x00000000	Audio PLL SC N/CTS Division Threshold Register For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_SC==1)
HDMI_RX_AUDPLL_SC_CTS	0x02ac	W	0x00000000	Audio PLL SC Manual CTS Value Register The manual value set in this register only takes effect if the aud_clk_ctrl.cts_n_ref register is set to 1 (manual mode enable). For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_SC==1)
HDMI_RX_AUDPLL_SC_N	0x02b0	W	0x00000000	Audio PLL SC Manual N Value Register The manual value set in this register only takes effect if the aud_clk_ctrl.cts_n_ref register is set to 1 (manual mode enable). For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_SC==1)
HDMI_RX_AUDPLL_SC_CTRL	0x02b4	W	0x00000000	Audio PLL SC Control Register Output controller signals that feed BYPASS, FOUTVCOPD, FOUT4PHASEPD, FOUTPOSTDIVPD, DSMPD, DACPD, and PD SC audio PLL inputs are synchronous with icfgclk. For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_SC==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_AUDPLL_SC_STS1	0x02b8	W	0x00000000	Audio PLL SC Status Register 1POSTDIV2, POSTDIV1, FBDIV and REFDIV are synchronous with HDMI_CLKSRC (FREF input of SC audio PLL). For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_SC==1)
HDMI_RX_AUDPLL_SC_STS2	0x02bc	W	0x00000000	Audio PLL SC Status Register 2FRAC is output to the SC Audio PLL synchronous with HDMI_CLKSRC (FREF input of SC audio PLL). For more information about the Audio PLL, refer to the HDMI RX Audio PLL Interfaces Application Note (available from Synopsys web site).(Exists: HRX_AUDPLL_SC==1)
HDMI_RX_SNPS_PHYG3_CTRL	0x02c0	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL Control Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_I2CM_PHYG3_SLAVE	0x02c4	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master Slave Address Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_I2CM_PHYG3_ADDRESS	0x02c8	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master R/W Address Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_I2CM_PHYG3_DATAO	0x02cc	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master Write Data(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_I2CM_PHYG3_DATAI	0x02d0	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master Read Data Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_I2CM_PHYG3_OPERATION	0x02d4	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master RW Transaction Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_I2CM_PHYG3_MODE	0x02d8	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master Fast Mode Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_I2CM_PHYG3_SOFTRST	0x02dc	W	0x00000000	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master Soft Reset Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_I2CM_PHYG3_SS_CNTS	0x02e0	W	0x019001d6	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master SS SCL Clock Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_I2CM_PHYG3_FS_HCNT	0x02e4	W	0x003c0082	SNPS PHY GEN3, HDMI 2.0, HDMI-MHL I2C Master FS SCL Clock Register(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_JTAG_CONF	0x02ec	W	0x00000011	PHY configuration JTAG interface - Reset and interface selection(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_JTAG_TAP_TCLK	0x02f0	W	0x00000000	PHY configuration JTAG interface - Clock Control(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_JTAG_TAP_IN	0x02f4	W	0x00000000	PHY configuration JTAG interface - Tap IN to PHY(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_JTAG_TAP_OUT	0x02f8	W	0x00000000	PHY configuration JTAG interface - Tap OUT from PHY(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_JTAG_ADDR	0x02fc	W	0x00000000	PHY configuration JTAG interface - Address(Exists: HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
HDMI_RX_PDEC_CTRL	0x0300	W	0x00000000	Packet Decoder and FIFO Control Register By using the register pdec_ctrl, you can enable the packet FIFO store filter and make the packet FIFO store various data types, and perform various operations on packet FIFO such as clear, read, write, or skip
HDMI_RX_PDEC_FIFO_CFG	0x0304	W	0x00000000	Packet Decoder and FIFO Configuration Register You can control the initial start, minimum and maximum fill state threshold measured in words by using the register pdec_fifo_cfg
HDMI_RX_PDEC_FIFO_STS	0x0308	W	0x00000000	Packet Decoder and FIFO Status Register You can read the FIFO fill state by using the register pdec_fifo_sts
HDMI_RX_PDEC_FIFO_DATA	0x030c	W	0x00000000	Packet Decoder and FIFO Byte Data Register
HDMI_RX_PDEC_AUDIODET_CTRL	0x0310	W	0x00000000	Packet Decoder Audio Detection Control Register
HDMI_RX_PDEC_DBG_ACP	0x031c	W	0x00000000	Packet Decoder ACP Frequency Count Register
HDMI_RX_PDEC_DBG_ERR_CORR	0x0320	W	0x00000000	Packet Decoder Signal Errors Register You can enable error code replacement and place an audio sample code by using pdec_dbg_err_corr
HDMI_RX_PDEC_FIFO_STS1	0x0324	W	0x00000000	Packet Decoder and FIFO Status Register
HDMI_RX_PDEC_ACRM_CTRL	0x0330	W	0x00000000	Packet Decoder CTS Measurement Control Register You can control the delta CTS trigger levels and the storage of CTS and N values by using pdec_scrm_ctrl
HDMI_RX_PDEC_ACRM_MAX	0x0334	W	0x00000000	Packet Decoder Maximum CTS N Value Register

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Name	Offset	Size	Reset Value	Description
HDMI_RX_PDEC_ACRM_MIN	0x0338	W	0x00000000	Packet Decoder Minimum CTS N Value Register
HDMI_RX_PDEC_ERR_FILTER	0x033c	W	0x00000000	Packet Decoder BCH/Checksum Error Filter Handling Register
HDMI_RX_PDEC_ASP_CTRL	0x0340	W	0x00000000	Packet Decoder Audio Subpacket Control RegisterYou can control the automatic muting of audio and video channels by using the register pdec_asp_ctrl
HDMI_RX_PDEC_ASP_ERR	0x0344	W	0x00000000	Packet Decoder Audio Subpacket Error Detection Register You can read the frame gaps between errors and the number of errors from the register pdec_asp_err
HDMI_RX_PDEC_STS	0x0360	W	0x00000000	Packet Decoder Status Register You can read the DVI detection status, various checksums related to packet values, packet transfer status, and FIFO and data thresholds from the register pdec_sts
HDMI_RX_PDEC_AUD_STS	0x0364	W	0x00000000	Packet Decoder Audio Status Register This registers allows you to determine what kind of audio stream is received by the HDMI RX
HDMI_RX_PDEC_VSI_PAYLOAD0	0x0368	W	0x00000000	Packet VSI Vendor Specific Payload Register 0(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_VSI_PAYLOAD1	0x036c	W	0x00000000	Packet VSI Vendor Specific Payload Register 1(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_VSI_PAYLOAD2	0x0370	W	0x00000000	Packet VSI Vendor Specific Payload Register 2(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_VSI_PAYLOAD3	0x0374	W	0x00000000	Packet VSI Vendor Specific Payload Register 3(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_VSI_PAYLOAD4	0x0378	W	0x00000000	Packet VSI Vendor Specific Payload Register4(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_PDEC_VSI_PAYLOAD5	0x037c	W	0x00000000	Packet VSI Vendor Specific Payload Register 5(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_GCP_AVMUTE	0x0380	W	0x00000000	Packet Decoder General Control Packet Register
HDMI_RX_PDEC_ACR_CTS	0x0390	W	0x00000000	Packet Decoder CTS Audio Clock Regeneration Register
HDMI_RX_PDEC_ACR_N	0x0394	W	0x00000000	Packet Decoder N Audio Clock Regeneration Register
HDMI_RX_PDEC_AVI_HB	0x03a0	W	0x00000000	Packet Decoder AVI Infoframe Register 0You can read the pixel repetition factor for profiles, the status of the frame content, and the Infoframe properties by using the register pdec_avi_hb
HDMI_RX_PDEC_AVI_PB	0x03a4	W	0x00000000	Packet Decoder AVI Infoframe Register 1You can read various Infoframe properties like the calorimetry, scaling, quantization, active format, picture aspect ratio, and scan information from the register pdec_avi_pb
HDMI_RX_PDEC_AVI_TBB	0x03a8	W	0x00000000	Packet Decoder AVI Infoframe Top/Bottom Bar Register
HDMI_RX_PDEC_AVI_LRB	0x03ac	W	0x00000000	Packet Decoder AVI Infoframe Left/Right Bar Register
HDMI_RX_PDEC_AIF_CTRL	0x03c0	W	0x00000000	Packet Decoder Special Audio Layout Control Register
HDMI_RX_PDEC_AIF_HB	0x03c4	W	0x00000000	Packet Decoder AIF Register 1
HDMI_RX_PDEC_AIF_PB0	0x03c8	W	0x00000000	Packet Decoder AIF Register 2
HDMI_RX_PDEC_AIF_PB1	0x03cc	W	0x00000000	Packet Decoder AIF Register 3
HDMI_RX_PDEC_GMD_HB	0x03d0	W	0x00000000	Packet Decoder Gamut Metadata Register 1You can read the gamut metadata, the packet sequence, and transmission profile number by using the register pdec_gmd_hb
HDMI_RX_PDEC_GMD_PB	0x03d4	W	0x00000000	Packet Decoder Gamut Metadata Register 2You can read the transmission checksum and the length of data transfer from the register pdec_gmd_pb
HDMI_RX_PDEC_VSI_ST0	0x03e0	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Status Register 0

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Name	Offset	Size	Reset Value	Description
HDMI_RX_PDEC_VSI_ST1	0x03e4	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Status Register 1
HDMI_RX_PDEC_VSI_PB0	0x03e8	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Register 0
HDMI_RX_PDEC_VSI_PB1	0x03ec	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Register 1
HDMI_RX_PDEC_VSI_PB2	0x03f0	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Register 2
HDMI_RX_PDEC_VSI_PB3	0x03f4	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Register 3
HDMI_RX_PDEC_VSI_PB4	0x03f8	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Register 4
HDMI_RX_PDEC_VSI_PB5	0x03fc	W	0x00000000	Packet Decoder Vendor-Specific Infoframe Register5
HDMI_RX_CEAVID_CONFIG	0x0400	W	0x00000000	CEA Video Mode Configuration Register(Exists: HRX_CEAVIDOUT==1)
HDMI_RX_CEAVID_3DCONFIG	0x0404	W	0x00000000	CEA Video Mode 3D Configuration Register(Exists: HRX_CEAVIDOUT==1)
HDMI_RX_CEAVID_HCONFIG_LO	0x0408	W	0x00000000	CEA Video Mode Horizontal Configuration Low Register(Exists: HRX_CEAVIDOUT==1)
HDMI_RX_CEAVID_HCONFIG_HI	0x040c	W	0x00000000	CEA Video Mode Horizontal Configuration High Register
HDMI_RX_CEAVID_VCONFIG_LO	0x0410	W	0x00000000	CEA Video Mode Vertical Configuration Low Register(Exists: HRX_CEAVIDOUT==1)
HDMI_RX_CEAVID_VCONFIG_HI	0x0414	W	0x00000000	CEA Video Mode Vertical Configuration High Register(Exists: HRX_CEAVIDOUT==1)
HDMI_RX_CEAVID_STATUS	0x0418	W	0x00000000	CEA Video Mode Status Register(Exists: HRX_CEAVIDOUT==1)
HDMI_RX_PDEC_AMP_HB	0x0480	W	0x00000000	Audio Metadata Packet - Header Content Register This register holds the content of the header of the last Audio Metadata packet received.(Exists: DWC_HDMI_RX_20==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_PDEC_AMP_PAYLOAD0	0x0484	W	0x00000000	Audio Metadata Packet - Payload Content Register 0This register holds the content of the payload of the last Audio Metadata packet received.(Eists: DWCHDMIRX20==1)
HDMI_RX_PDEC_AMP_PAYLOAD1	0x0488	W	0x00000000	Audio Metadata Packet - Payload Content Register1This register holds the content of the payload of the last Audio Metadata packet received.(Eists: DWCHDMIRX20==1)
HDMI_RX_PDEC_AMP_PAYLOAD2	0x048c	W	0x00000000	Audio Metadata Packet - Payload Content Register 2This register holds the content of the payload of the last Audio Metadata packet received.(Eists: DWCHDMIRX20==1)
HDMI_RX_PDEC_AMP_PAYLOAD3	0x0490	W	0x00000000	Audio Metadata Packet - Payload Content Register3This register holds the content of the payload of the last Audio Metadata packet received.(Eists: DWCHDMIRX20==1)
HDMI_RX_PDEC_AMP_PAYLOAD4	0x0494	W	0x00000000	Audio Metadata Packet - Payload Content Register 4This register holds the content of the payload of the last Audio Metadata packet received.(Eists: DWCHDMIRX20==1)
HDMI_RX_PDEC_AMP_PAYLOAD5	0x0498	W	0x00000000	Audio Metadata Packet - Payload Content Register 5This register holds the content of the payload of the last Audio Metadata packet received.(Eists: DWCHDMIRX20==1)
HDMI_RX_PDEC_AMP_PAYLOAD6	0x049c	W	0x00000000	Audio Metadata Packet - Payload Content Register 6This register holds the content of the payload of the last Audio Metadata packet received.(Eists: DWCHDMIRX20==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_PDEC_NTSCVBI_HB	0x04a0	W	0x00000000	Packet NTSC Vertical Blanking Interval Header(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_NTSCVBI_PAYLOAD0	0x04a4	W	0x00000000	Packet NTSC Vertical Blanking Interval Payload 0 Register
HDMI_RX_PDEC_NTSCVBI_PAYLOAD1	0x04a8	W	0x00000000	Packet NTSC Vertical Blanking Interval Payload 1 Register(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_NTSCVBI_PAYLOAD2	0x04ac	W	0x00000000	Packet NTSC Vertical Blanking Interval Payload 2 Register(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_NTSCVBI_PAYLOAD3	0x04b0	W	0x00000000	Packet NTSC Vertical Blanking Interval Payload 3 Register(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_NTSCVBI_PAYLOAD4	0x04b4	W	0x00000000	Packet NTSC Vertical Blanking Interval Payload 4 Register(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_NTSCVBI_PAYLOAD5	0x04b8	W	0x00000000	Packet NTSC Vertical Blanking Interval Payload 5 Register(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_NTSCVBI_PAYLOAD6	0x04bc	W	0x00000000	Packet NTSC Vertical Blanking Interval Payload 6 Register(Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1)
HDMI_RX_PDEC_DRM_HB	0x04c0	W	0x00000000	Packet Dynamic Range and Mastering Header(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_PDEC_DRM_PAYLOAD0	0x04c4	W	0x00000000	Packet Dynamic Range and Mastering Payload 0 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_PDEC_DRM_PAYLOAD1	0x04c8	W	0x00000000	Packet Dynamic Range and Mastering Payload 1 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_PDEC_DRM_PAYLOAD2	0x04cc	W	0x00000000	Packet Dynamic Range and Mastering Payload 2 Register(Exists: DWC_HDMI_RX_20==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_PDEC_DRM_PAYLOAD3	0x04d0	W	0x00000000	Packet Dynamic Range and Mastering Payload 3 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_PDEC_DRM_PAYLOAD4	0x04d4	W	0x00000000	Packet Dynamic Range and Mastering Payload 4 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_PDEC_DRM_PAYLOAD5	0x04d8	W	0x00000000	Packet Dynamic Range and Mastering Payload 5 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_PDEC_DRM_PAYLOAD6	0x04dc	W	0x00000000	Packet Dynamic Range and Mastering Payload 6 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_MHLMODE_CTRL	0x0500	W	0x00000000	MHL Datapath Mode Control Register(Exists: DWC_HDMI_RX_MHL==1)
HDMI_RX_CDSENSE_STATUS	0x0504	W	0x00000000	CDSENSE Status Register(Exists:DWC_HDMI_RX_MHL==1)
HDMI_RX_DESERFIFO_CTRL	0x0508	W	0x00000000	MHL Datapath Deserializer FIFO Control Register(Exists: DWC_HDMI_RX_MHL==1)
HDMI_RX_DESER_INTTRSHCTRL	0x050c	W	0x00000000	MHL Datapath Deserializer Interrupt Threshold Control Register(Exists: DWC_HDMI_RX_MHL==1)
HDMI_RX_DESER_INTCNTCTRL	0x0510	W	0x00000000	MHL Datapath Deserializer Interrupt Counter Clear Control Register(Exists: DWC_HDMI_RX_MHL==1)
HDMI_RX_DESER_INTCNT	0x0514	W	0x00000000	MHL Datapath Deserializer Interrupt Counter Register(Exists: DWC_HDMI_RX_MHL==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_HDCP_RPT_CTRL	0x0600	W	0x00000000	HDCP Repeater KSV List Control Register You can use hdcp_rpt_ctrl to know the status of authentication, KSV FIFO, and repeater. You can also perform auto-clearing.Note: Writing to any register field that is indicated as Read Only (R) has no effect, however, the APB error flag is not asserted.(Exists: HDCP_REPEATER==1)
HDMI_RX_HDCP_RPT_BSTATUS	0x0604	W	0x00000000	HDCP Repeater Status Repeater You can use hdcp_rpt_bstatus to read the HDMI mode, the topology error, repeater status, cascade depth, and the number of downstream devices attached.(Exists: HDCP_REPEATER==1)
HDMI_RX_HDCP_RPT_KSV_FIFO_CTRL	0x0608	W	0x00000000	HDCP Repeater KSV FIFO Control Register(Exists: HDCP_REPEATER==1)
HDMI_RX_HDCP_RPT_KSV_FIFO1	0x060c	W	0x00000000	HDCP Repeater KSV FIFO Register 1(Exists: HDCPREPEATER==1)
HDMI_RX_HDCP_RPT_KSV_FIFO0	0x0610	W	0x00000000	HDCP Repeater KSV FIFO Register 0(Exists: HDCP_REPEATER==1)
HDMI_RX_HDMI20_CONTROL	0x0800	W	0x00000000	HDMI 2.0 Features Control Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_I2CCONFIG	0x0804	W	0x00000000	SCDC I2C Configuration Register(Exists: DWCHDMIRX20==1)
HDMI_RX_SCDC_CONFIG	0x0808	W	0x00000000	SCDC Configuration Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_CHLOCK_CONFIG	0x080c	W	0x00000000	Channel Lock Configuration Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_HDCP22_CONTROL	0x081c	W	0x00000000	HDCP 2.2 Control Register(Exists: HRX_HDCP22_EXTERNAL==1)
HDMI_RX_SCDC_REGS0	0x0820	W	0x00000000	SCDC Registers 0(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_REGS1	0x0824	W	0x00000000	SCDC Registers 1(Exists: DWC_HDMI_RX_20==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_SCDC_REGS2	0x0828	W	0x00000000	SCDC Registers 2(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_REGS3	0x082c	W	0x00000000	SCDC Registers 3(Exists: DWCHDMIRX20==1)
HDMI_RX_SCDC_MANSPEC0	0x0840	W	0x00000000	SCDC Manufacturer Specific Write Data Register 0(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_MANSPEC1	0x0844	W	0x00000000	SCDC Manufacturer Specific Write Data Register 1(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_MANSPEC2	0x0848	W	0x00000000	SCDC Manufacturer Specific Write Data Register 2(Eists: DWCHDMIRX20==1)
HDMI_RX_SCDC_MANSPEC3	0x084c	W	0x00000000	SCDC Manufacturer Specific Write Data Register 3(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_MANSPEC4	0x0850	W	0x00000000	SCDC Manufacturer Specific Write Data Register 4(Exists: DWCHDMIRX20==1)
HDMI_RX_SCDC_WRDATA0	0x0860	W	0x00000000	SCDC Write Data 0 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_WRDATA1	0x0864	W	0x00000000	SCDC Write Data 1 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_WRDATA2	0x0868	W	0x00000000	SCDC Write Data 2 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_WRDATA3	0x086c	W	0x00000000	SCDC Write Data 3 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_WRDATA4	0x0870	W	0x00000000	SCDC Write Data 4 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_WRDATA5	0x0874	W	0x00000000	SCDC Write Data 5 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_WRDATA6	0x0878	W	0x00000000	SCDC Write Data 6 Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_SCDC_WRDATA7	0x087c	W	0x00000000	SCDC Write Data 7 Register(Exists: DWCHDMIRX20==1)
HDMI_RX_HDMI20_STATUS	0x08e0	W	0x00000000	HDMI 2.0 Status Register(Exists: DWC_HDMI_RX_20==1)
HDMI_RX_HDCP2_ESM_GLOBAL_GPIO_IN	0x08e8	W	0x00000000	HDCP2 ESM - Global GPIO interface - Inputs to ESM(Exists: HRX_HDCP22_EXT_GPIOS==1)
HDMI_RX_HDCP2_ESM_GLOBAL_GPIO_OUT	0x08ec	W	0x00000000	HDCP2 ESM - Global GPIO interface - Outputs from ESM(Exists: HRX_HDCP22_EXT_GPIOS==1)

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Name	Offset	Size	Reset Value	Description
HDMI_RX_HDCP2_ESM_P0_GPIO_IN	0x08f0	W	0x00000000	HDCP2 ESM - Port 0 GPIO interface - Inputs to ESM(Exists: HRX_HDCP22_EXT_GPIOS==1)
HDMI_RX_HDCP2_ESM_P0_GPIO_OUT	0x08f4	W	0x00000000	HDCP2 ESM - Port 0 GPIO interface - Outputs from ESM(Exists: HRX_HDCP22_EXT_GPIOS==1)
HDMI_RX_HDCP22_STATUS	0x08fc	W	0x00000000	HDCP 2.2 Status Register(Exists: HRXHDCP22EXTERNAL==1)
HDMI_RX_HDMI2_IEN_CLR	0x0f60	W	0x00000000	External HDCP 2.0 Interrupt - Enable clear Register Note: These fields affect the ohdmi_int interrupt line.(Exists: HRX_HDCP22_EXTERNAL==1)
HDMI_RX_HDMI2_IEN_SET	0x0f64	W	0x00000000	External HDCP 2.0 Interrupt - Enable Set Register Note: These fields affect the ohdmi_int interrupt line.(Exists: HRX_HDCP22_EXTERNAL==1)
HDMI_RX_HDMI2_ISTS	0x0f68	W	0x00000000	External HDCP 2.0 Interrupt Flag Register Note: These interrupts affect the ohdmi_int interrupt line.(Exists: HRX_HDCP22_EXTERNAL==1)
HDMI_RX_HDMI2_IEN	0x0f6c	W	0x00000000	External HDCP 2.0 Interrupt Enable Status Register Note: These fields are related with ohdmi_int interrupt line(Exists: HRX_HDCP22_EXTERNAL==1)
HDMI_RX_HDMI2_ICLR	0x0f70	W	0x00000000	External HDCP 2.0 Interrupt Flag Clear Register Note: These fields affect the ohdmi_int interrupt line.(Exists: HRX_HDCP22_EXTERNAL==1)
HDMI_RX_HDMI2_ISET	0x0f74	W	0x00000000	External HDCP 2.0 interrupt Set Register Note: These fields affect the ohdmi_int interrupt line.(Exists: HRX_HDCP22_EXTERNAL==1)
HDMI_RX_PDEC_IEN_CLR	0x0f78	W	0x00000000	Packet Decoder interrupt - Enable clear Register Note: These fields affect the ohdmi_int interrupt line

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Name	Offset	Size	Reset Value	Description
HDMI_RX_PDEC_IEN_SET	0x0f7c	W	0x00000000	Packet Decoder Interrupt - Enable Set Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_PDEC_ISTS	0x0f80	W	0x00000000	Packet Decoder Interrupt Flag Register Note: These interrupts affect the ohdmi_int interrupt line
HDMI_RX_PDEC_IEN	0x0f84	W	0x00000000	Packet Decoder Interrupt Enable Status Register Note: These fields are related with ohdmi_int interrupt line
HDMI_RX_PDEC_ICLR	0x0f88	W	0x00000000	Packet Decoder Interrupt Flag Clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_PDEC_ISET	0x0f8c	W	0x00000000	Packet Decoder Interrupt Set Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_AUD_CEC_IEN_CLR	0x0f90	W	0x00000000	Audio Clock and CEC interrupt - Enable clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_AUD_CEC_IEN_SET	0x0f94	W	0x00000000	Audio Clock Interrupt - Enable Set Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_AUD_CEC_ISTS	0x0f98	W	0x00000000	Audio Clock Interrupt Flag Register Note: These interrupts affect the ohdmi_int interrupt line
HDMI_RX_AUD_CEC_IEN	0x0f9c	W	0x00000000	Audio Clock Interrupt Enable Status Register Note: These fields are related with ohdmi_int interrupt line
HDMI_RX_AUD_CEC_ICLR	0x0fa0	W	0x00000000	Audio Clock Interrupt Flag Clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_AUD_CEC_ISET	0x0fa4	W	0x00000000	Audio Clock Interrupt Set Status Register Note: These fields affect the ohdmi_int interrupt line

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Name	Offset	Size	Reset Value	Description
HDMI_RX_AUD_FIFO_IEN_CLR	0x0fa8	W	0x00000000	Audio FIFO Interrupt - Enable Clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_AUD_FIFO_IEN_SET	0x0fac	W	0x00000000	Audio FIFO Interrupt - Enable Set Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_AUD_FIFO_ISTS	0x0fb0	W	0x00000000	Audio FIFO Interrupt Flag Register Note: These interrupts affect the ohdmi_int interrupt line
HDMI_RX_AUD_FIFO_IEN	0x0fb4	W	0x00000000	Audio FIFO Interrupt Enable Status Register Note: These fields are related with ohdmi_int interrupt line
HDMI_RX_AUD_FIFO_ICLR	0x0fb8	W	0x00000000	Audio FIFO Interrupt Flag Clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_AUD_FIFO_ISET	0x0fbc	W	0x00000000	Audio FIFO Interrupt Set Status Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_MD_IEN_CLR	0x0fc0	W	0x00000000	Video Mode Interrupt - Enable Clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_MD_IEN_SET	0x0fc4	W	0x00000000	Video Mode Interrupt - Enable Set Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_MD_ISTS	0x0fc8	W	0x00000000	Video Mode Interrupt Flag Register Note: These interrupts affect the ohdmi_int interrupt line
HDMI_RX_MD_IEN	0x0fcc	W	0x00000000	Video Mode Interrupt Enable Status Register Note: These fields are related with ohdmi_int interrupt line
HDMI_RX_MD_ICLR	0x0fd0	W	0x00000000	Video Mode Interrupt Flag Clear Register Note: These fields affect the ohdmi_int interrupt line

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Name	Offset	Size	Reset Value	Description
HDMI_RX_MD_ISET	0x0fd4	W	0x00000000	Video Mode Interrupt Set Status Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_HDMI_IEN_CLR	0x0fd8	W	0x00000000	HDMI Interrupt - Enable Clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_HDMI_IEN_SET	0x0fdc	W	0x00000000	HDMI Interrupt - Enable Set Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_HDMI_ISTS	0x0fe0	W	0x00000000	HDMI Interrupt Flag Register Note: These interrupts affect the ohdmi_int interrupt line
HDMI_RX_HDMI_IEN	0x0fe4	W	0x00000000	HDMI Interrupt Enable Status Register Note: These fields are related with ohdmi_int interrupt line
HDMI_RX_HDMI_ICLR	0x0fe8	W	0x00000000	HDMI Interrupt Flag Clear Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_HDMI_ISET	0x0fec	W	0x00000000	HDMI Interrupt Set Status Register Note: These fields affect the ohdmi_int interrupt line
HDMI_RX_DMI_SW_RST	0x0ff0	W	0x00000000	DMI Software Reset Register You can reset all configuration registers and functional units by using dmi_sw_rst
HDMI_RX_DMI_DISABLE_IF	0x0ff4	W	0x000100ff	DMI Disable Interface Register This register holds bits that are the Main synchronous enable over all individual enables (ocfg_enable, omodet_enable, ohdmi_enable, obus_enable, oaud_enable, ocec_enable)
HDMI_RX_DMI_MODULE_ID_EXT	0x0ff8	W	0x00000000	DMI Module ID Revision Register
HDMI_RX_DMI_MODULE_ID	0x0ffc	W	0x00000000	DMI Module ID Register
HDMI_RX_CEC_CTRL	0x1f00	W	0x00000000	CEC Control Register This register handles the main control of the CEC initiator.Exists: HDMIRXCEC==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_CEC_MASK	0x1f08	W	0x00000000	CEC Interrupt Mask Register This register is readable and writable, which masks/unmasks the interrupt events. When the bit is set to 1 (masked), the corresponding event could not trigger an interrupt signal at SFR interface. When the bit is reset to 0, the interrupt event is unmasked.Exists: HDMIRXCEC==1
HDMI_RX_CEC_ADDR_L	0x1f14	W	0x00000000	CEC Logical Address Low Byte Register This register indicates the logical address(es) allocated to the CEC device. This register is written by software when the logical allocation is finished.Exists: HDMIRXCEC==1
HDMI_RX_CEC_ADDR_H	0x1f18	W	0x00000000	CEC Logical Address High Byte Register This register indicates the logical address(es) allocated to the CEC device. This register is written by software when the logical allocation is finished.Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_CNT	0x1f1c	W	0x00000000	CEC Transmitter Buffer Counter Register This register indicates the size of the frame in bytes (including header and data blocks), which are available in the transmitter data buffer.Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_CNT	0x1f20	W	0x00000000	CEC Receiver Buffer Counter Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_0	0x1f40	W	0x00000000	CEC Byte 0 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_1	0x1f44	W	0x00000000	CEC Byte 1 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_2	0x1f48	W	0x00000000	CEC Byte 2 Transmitter Data Buffer Register Exists: HDMIRXCEC==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_CEC_TX_DATA_3	0x1f4c	W	0x00000000	CEC Byte 3 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_4	0x1f50	W	0x00000000	CEC Byte 4 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_5	0x1f54	W	0x00000000	CEC Byte 5 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_6	0x1f58	W	0x00000000	CEC Byte 6 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_7	0x1f5c	W	0x00000000	CEC Byte 7 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_8	0x1f60	W	0x00000000	CEC Byte 8 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_9	0x1f64	W	0x00000000	CEC Byte 9 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_10	0x1f68	W	0x00000000	CEC Byte 10 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_11	0x1f6c	W	0x00000000	CEC Byte 11 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_12	0x1f70	W	0x00000000	CEC Byte12 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_13	0x1f74	W	0x00000000	CEC Byte 13 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_14	0x1f78	W	0x00000000	CEC Byte 0 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_TX_DATA_15	0x1f7c	W	0x00000000	CEC Byte 15 Transmitter Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_0	0x1f80	W	0x00000000	CEC Byte 0 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_1	0x1f84	W	0x00000000	CEC Byte 1 Receiver Data Buffer Register Exists: HDMIRXCEC==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_CEC_RX_DATA_2	0x1f88	W	0x00000000	CEC Byte 2 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_3	0x1f8c	W	0x00000000	CEC Byte 3 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_4	0x1f90	W	0x00000000	CEC Byte 4 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_5	0x1f94	W	0x00000000	CEC Byte 5 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_6	0x1f98	W	0x00000000	CEC Byte 0 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_7	0x1f9c	W	0x00000000	CEC Byte 7 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_8	0x1fa0	W	0x00000000	CEC Byte 0 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_9	0x1fa4	W	0x00000000	CEC Byte 0 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_10	0x1fa8	W	0x00000000	CEC Byte 10 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_11	0x1fac	W	0x00000000	CEC Byte 11 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_12	0x1fb0	W	0x00000000	CEC Byte 12 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_13	0x1fb4	W	0x00000000	CEC Byte 13 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_14	0x1fb8	W	0x00000000	CEC Byte 14 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_RX_DATA_15	0x1fbc	W	0x00000000	CEC Byte 15 Receiver Data Buffer Register Exists: HDMIRXCEC==1
HDMI_RX_CEC_LOCK	0x1fc0	W	0x00000000	CEC Lock Register Exists: HDMIRXCEC==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_CEC_WAKEUPCTRL	0x1fc4	W	0x00000000	CEC Wakeup Status Register Exists: HDMIRXCEC==1
HDMI_RX_CBUSSWRESETREQ	0x3000	W	0x00000000	CBUS Software Reset Request Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CBUSENABLEIF	0x3004	W	0x00000000	CBUS Synchronous Enable Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CB_LOCKONCLOCK_STS	0x3010	W	0x00000000	CBUS Main Controller Clock Status Indication Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CB_LOCKONCLOCKCLR	0x3014	W	0x00000000	CBUS Main Controller Clear Clock Status Indication Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CBUSIOCTRL	0x3020	W	0x00000000	CBUS I/O Control Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_DD_CTRL	0x3040	W	0x00000000	CBUS Device Discovery Control Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_DD_OP_CTRL	0x3044	W	0x00000000	CBUS Device Discovery Operational Control Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_DD_STS	0x3048	W	0x00000000	CBUS Device Discovery Status Register Exists: DWCHDMIRXMHL==1
HDMI_RX_DD_BYPASS_EN	0x304c	W	0x00000000	CBUS Device Discovery Bypass Enable Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_DD_BYPASS_CTRL	0x3050	W	0x00000000	CBUS Device Discovery Bypass Control Register Exists: DWCHDMIRXMHL==1
HDMI_RX_DD_BYPASS_CBUS	0x3054	W	0x00000000	CBUS Device Discovery CBUS Bypass Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_TXPCKFIFO	0x3080	W	0x00000000	CBUS Link Layer Packet Transmit FIFO Write Access Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_RXPCKFIFO_RD_CLR	0x3084	W	0x00000000	CBUS Link Layer Packet Receiver FIFOs, Read Acknowledge Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_RXPCKFIFO_A	0x3088	W	0x00000000	CBUS Link Layer Packet Receiver FIFO A Read Access Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_RXPCKFIFO_B	0x308c	W	0x00000000	CBUS Link Layer Packet Receiver FIFO B Read Access Register Exists: DWC_HDMI_RX_MHL==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_LL_TXPCKCTRL_0	0x3090	W	0x00000000	CBUS Link Layer Packet Transmit Control 0 Register Exists: DWCHDMIRXMHL==1
HDMI_RX_LL_TXPCKCTRL_1	0x3094	W	0x10200001	CBUS Link Layer Packet Transmit Control 1 Register Exists: DWCHDMIRXMHL==1
HDMI_RX_LL_PCKFIFO_STS	0x309c	W	0x00000000	CBUS Link Layer Transmit and Receive Status Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_RXPCKCTRL_0	0x30a0	W	0x03003d05	CBUS Link Layer Packet Receive Control 0 Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_RXPCKCTRL_1	0x30a4	W	0x10001d37	CBUS Link Layer Packet Receive Control 1 Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_INTTRSHLDCTRL	0x30b0	W	0x00000000	CBUS Link Layer Interrupt Threshold Control Register Exists: DWCHDMIRXMHL==1
HDMI_RX_LL_INTCNTCTRL	0x30b4	W	0x00000000	CBUS Link Layer Interrupt Counter Clear Control Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_LL_INTCNT_0	0x30b8	W	0x00000000	CBUS Link Layer Interrupt Counters status Register 0Exists: DWCHDMIRXMHL==1
HDMI_RX_LL_INTCNT_1	0x30bc	W	0x00000000	CBUS Link Layer Interrupt Counters status Register 1Exists: DWC_HDMI_RX_MHL==1s
HDMI_RX_CBHDCP_OPCTRL	0x3100	W	0x00000000	CBUS HDCP - Operational Control Register Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CBHDCP_WDATA_0	0x3104	W	0x00000000	CBUS HDCP - Write Data 0 Register (bytes 1-4)Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CBHDCP_WDATA_1	0x3108	W	0x00000000	CBUS HDCP - Write Data 1 Register (bytes 1-4)Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CBHDCP_RDATA_0	0x310c	W	0x00000000	CBUS HDCP - Read Data 0 Register (bytes 1-4)Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CBHDCP_RDATA_1	0x3110	W	0x00000000	CBUS HDCP - Read Data 1 Register (bytes 5-8)Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_CBHDCP_STATUS	0x3114	W	0x00000000	CBUS HDCP - Status Register Exists: DWC_HDMI_RX_MHL==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_CBHDCP_DDC_REPORT	0x3118	W	0x00000000	CBUS HDCP - DDC Command Report Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_ISTAT_CB_DD	0x3200	W	0x00000000	CBUS Device Discovery Status Interrupt Register Note: These interrupts affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMASK_CB_DD	0x3204	W	0x0000003f	CBUS Device Discovery Interrupt Mask Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IFORCE_CB_DD	0x3208	W	0x00000000	CBUS Device Discovery Interrupt Force Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_ICLEAR_CB_DD	0x320c	W	0x00000000	CBUS Device Discovery Interrupt Clear Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMUTE_CB_DD	0x3210	W	0x0000003f	CBUS Device Discovery Interrupt Mute Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_ISTAT_CB_LL	0x3220	W	0x00000000	CBUS Link Layer Status Interrupt Register Note: These interrupts affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMASK_CB_LL	0x3224	W	0x0003ffff	CBUS Link Layer Status Interrupt Register Note: These interrupts affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IFORCE_CB_LL	0x3228	W	0x00000000	CBUS Link Layer Interrupt Force Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_ICLEAR_CB_LL	0x322c	W	0x00000000	CBUS Link Layer Interrupt Clear Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMUTE_CB_LL	0x3230	W	0x0003ffff	CBUS Link Layer Interrupt Mute Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_ISTAT_CB_HDCP	0x3240	W	0x00000000	CBUS HDCP Status Interrupt Register Note: These interrupts affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMASK_CB_HDCP	0x3244	W	0x00000001	CBUS HDCP Interrupt Mask Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IFORCE_CB_HDCP	0x3248	W	0x00000000	CBUS HDCP Interrupt Force Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_ICLEAR_CB_HDCP	0x324c	W	0x00000000	CBUS HDCP Interrupt Clear Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMUTE_CB_HDCP	0x3250	W	0x00000001	CBUS HDCP Interrupt Mute Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_ISTAT_CB_MCTRL	0x3260	W	0x00000000	CBUS Main Controller Status Interrupt Register Note: These interrupts affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMASK_CB_MCTRL	0x3264	W	0x00000001	CBUS Main Controller Interrupt Mask Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1

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Name	Offset	Size	Reset Value	Description
HDMI_RX_IFORCE_CB_MCTRL	0x3268	W	0x00000000	CBUS Main Controller Interrupt Mask Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_ICLEAR_CB_MCTRL	0x326c	W	0x00000000	CBUS Main Controller Interrupt Clear Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMUTE_CB_MCTRL	0x3270	W	0x00000000	CBUS Main Controller Interrupt Mute Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IMASTER_MUTE_CB	0x32e0	W	0x00000000	CBUS Interrupt Master Mute Register Note: These fields affect ointcbus interrupt line Exists: DWC_HDMI_RX_MHL==1
HDMI_RX_IVECTOR_INDEX_CB	0x32e4	W	0x00000000	CBUS Interrupt Vector Index Register Note: These fields are related with ointcbus interrupt line

9.7.2 Detail Register Description

HDMI_RX_HDMI_SETUP_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x1	hot_plug_detect_input_d Enable Hot Plug Detect output to input D of the HDMI source. 1'b0: Disabled, hence signal ohot_plug_detect_d = 0 1'b1: Enabled Note: Only present when GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs are used
26	RW	0x1	hot_plug_detect_input_c Enable Hot Plug Detect output to input C of the HDMI source. 1'b0: Disabled, hence signal ohot_plug_detect_c = 0 1'b1: enabled Note: Only present when GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs are used

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Bit	Attr	Reset Value	Description
25	RW	0x0	hot_plug_detect_input_b Enable hot plug detect signal output to input B of the HDMI source. 1'b0: Disabled, hence HOT_PLUG_DETECT_B = 0 1'b1: Enabled
24	RW	0x1	hot_plug_detect_input_a Enable hot plug detect signal output to input A of the HDMI source. 1'b0: Disabled, hence HOT_PLUG_DETECT_A = 0 1'b1: Enabled
23:22	RO	0x0	reserved
21	RW	0x0	hdmibus_reset_over_en PHY HDMI_RST_N override and PHY BUS_RST_N override enable for GEN1,GEN1E202, and GEN2 PHYs. 1'b0: PHY HDMI_RST_N and PHY BUS_RST_N controlled by software reset registers 1'b1: PHY HDMI_RST_N and PHY BUS_RST_N controlled by hdmi_reset_ovr and bus_reset_ovr Note: Only performs functionality for GEN1, GEN1 E202, and GEN2 PHYs
20	RW	0x0	bus_reset_ovr PHY BUS_RST_N override for GEN1, GEN1E202, and GEN2 PHYs. 1'b0: Inactive 1'b1: Active Note: Only performs functionality for GEN1, GEN1 E202, and GEN2 PHYs
19	RW	0x0	hdmi_reste_ovr PHY HDMI_RST_N override for GEN1, GEN1E202, and GEN2 PHYs. 1'b0: Inactive 1'b1: Active Note: Only performs functionality for GEN1, GEN1 E202, and GEN2 PHYs
18	RW	0x0	pon_reset_ovr Has functional use in all except GEN3, HDMI 2.0, HDMIMHL and non-Synopsys PHYs; PON_RST_N override for GEN1, GEN1E202, and GEN2 PHYs. 1'b0: Inactive;ipon_rst_n controls the PON_RST_N PHY port. 1'b1: Active; as long as this bit is held high the PON_RST_N PHY port is set to low (1'b0). Note: Only performs functionality for GEN1, GEN1 E202, and GEN2 PHYs

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Bit	Attr	Reset Value	Description
17	RW	0x0	reset_ovr Reset tmdsclk/ihdmiclk domain override. Note: Only performs functionality for GEN1 and GEN1 E202 PHYs
16	RW	0x0	reset_ovr_en Reset software control enable. 1'b0: Disable 1'b1: Enable Note: Only performs functionality for GEN1 and GEN1 E202 PHYs
15	RW	0x0	eq_osm_ovr Equalizer osm override. Note: Only performs functionality for GEN1 and GEN1 E202 PHYs
14	RW	0x0	eq_osm_ovr_en Enable software control for eq_osm_ovr (Equalizer osm override). 1'b0: Disable 1'b1: Enable Note: Only performs functionality for GEN1 and GEN1 E202 PHYs
13	RW	0x0	nowait_activity Enable no wait activity. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
12:7	RW	0x00	eq_cal_time Equalizer calculation time. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
6	RW	0x0	ues_pll_lock Use PLL lock Note: Only performs functionality for GEN1 and GEN1 E202 PHYs
5	RW	0x0	force_state Force target_state Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
4:1	RW	0x0	target_state Triggers an interrupt when the target state is crossed.If the auto setup controller reaches or crosses target_state, an interrupt is triggered. The interrupt is triggered even if the force_state mode is not activated. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
0	RW	0x0	hot_plug_detect Signal output to HDMI source input A or input B dependent on the input_select bit from the input selector. 1'b0: Receiver not ready 1'b1: Receiver ready If input_select = 0 hot_plug_detect_a = hot_plug_detect AND hot_plug_detect_input_a hot_plug_detect_b = 1 AND hot_plug_detect_input_b If input_select = 1 hot_plug_detect_a = 1 AND hot_plug_detect_input_a hot_plug_detect_b = hot_plug_detect AND hot_plug_detect_input_b

HDMI_RX_HDMI_OVR_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	pon_res_cal_ov 1'b0: Power off 1'b1: Power on Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
30:28	RW	0x0	pon_pll_ovr Channel PLL and data sampler ,Bit 2:0 = channel 2:0. 1'b0: Power off 1'b1: Power on Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
27:26	RO	0x0	reserved
25	RW	0x0	pon_clk_ovr_input_b Clock on input B. 1'b0: Power off 1'b1: Power on Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
24:22	RW	0x0	pon_res_ovr_input_b Data channel internal termination input resistors on input B。 3'b000: inactive on all channels 3'b001: active on channel 0 3'b010: active on channel 1 3'b011: active on channel 0 and 1 3'b100: active on channel 2 3'b101: active on channel 0 and 2 3'b110: active on channel 1 and 2 3'b111: active on all channels 2..0 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
21	RW	0x0	pon_resc_ovr_input_b Clock channel internal termination resistor on input B. 1’b0: Inactive 1’b1: Active Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
20	RW	0x0	pon_clk_ovr_input_a Clock on input A. 1’b0: Power off 1’b1: Power on Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
19:17	RW	0x0	pon_res_ovr_input_a Data channel internal termination input resistors on input A. 3'b000: inactive on all channels 3'b001: active on channel 0 3'b010: active on channel 1 3'b011: active on channel 0 and 1 3'b100: active on channel 2 3'b101: active on channel 0 and 2 3'b110: active on channel 1 and 2 3'b111: active on all channels 2..0 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
16	RW	0x0	pon_resc_ovr_input_a Clock channel internal termination resistor on input A. 1’b0: Inactive 1’b1: Active Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	pon_eq_ovr Channel equalizer. Bit 2:0 = channel 2:0 3'b0: power off 3'b1: power on Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
10:0	RO	0x0	reserved

HDMI_RX_HDMI_TIMER_CTRL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	slowx4 Slow down 4us/64us pulses by four. Note: Only performs functionality for GEN1 (not GEN1 E202)
9:0	RW	0x278	cnt4us Number of sys_clks in 4us. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_RES_OVR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bias_rsv Reserved and read a zero. Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
27:24	RW	0x0	s2p_curr S2P bias current. 4'b0: off 4'b1: minimum current, 0.67 4'b2: 0.89 4'b3: 1.11 4'b4: 1.33 4'b5: 1.55 4'b6: 1.77 4'b7: 2.0 Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs

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Bit	Attr	Reset Value	Description
23	RW	0x0	inv_rr_cmp_out Invert reference resistor comparator output (former bit ctrl_rsv(7)). 1'b0: No inversion 1'b1: Inversion Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
22:16	RW	0x00	ctrl_rsv Reserved for additional analog front end signals. Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
15	RW	0x0	prot_osc_disable Ability to disable the overload recovery oscillator during test. 1'b0: Normal application: oscillator active 1'b1: Test mode: oscillator disabled Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
14:9	RO	0x0	reserved
8	RW	0x0	sw_rescal_en Triggers measurement of reference resistor and setting of termination resistors. 1'b0: Disable 1'b1: Enable Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
7	RW	0x0	ref_ovr_en Manual reference resistor setting force 1'b0: Inactive 1'b1: Forces reference resistor setting to ref_ovride Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
6	RW	0x0	res_ovr_en Manual termination resistor setting force. 1'b0: Inactive 1'b1: Forces termination resistor setting to ref_ovride Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
5:0	RW	0x00	ref_ovride Manual reference resistor value to force. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_RES_STS

Address: Operational Base + offset (0x0014)

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Bit	Attr	Reset Value	Description
31	RO	0x0	state_reached Internal = requested state reached. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
30:24	RO	0x00	status_rev Reserved for PHY debug. Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
23	RO	0x0	refcmp Buffered reference resistor comparator output. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
22:17	RO	0x00	refres Measured reference resistor value. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
16	RO	0x0	rescal_done Indicates that the resistor calibration is complete. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
15:8	RO	0x00	ovl_in_input1 Overload detection at HDMI input B pins [7] RXOp [6] RXOn [5] RX1p [4] RX1n [3] RX2p [2] RX2n [1] RXCp [0] RXCn 1'b0: Nominal 1'b1: Overload Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	ovl_in_input0 Overload detection at HDMI input A pins [7] RXOp [6] RXOn [5] RX1p [4] RX1n [3] RX2p [2] RX2n [1] RXCp [0] RXCn 1'b0: Nominal 1'b1: Overload Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs

HDMI_RX_HDMI_PLL_CTRL

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	pll_rsv Reserved for PLL usage Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15:12	RO	0x0	reserved
11	RW	0x0	pll_pfd_delay Phase frequency detector related charge pump up and down pulse length. 1'b0: Small pulse width 1'b1: Long pulse width For more information, see the latest version of the DesignWare Cores HDMI PHY Databook. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
10	RW	0x0	plldn Forces down pulses to charge pump; only has impact on the charge pump if pll_ovr_pfd =1. 1'b0: Leakage test 1'b1: Force down Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
9	RW	0x0	pullup Forces up/down pulses to charge pump, only has impact on the charge pump if pll_ovr_pfd = 1 1'b0: Leakage test 1'b1: Force up Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
8	RW	0x0	pll_ovr_pfd Override up/down pulses from PFD. 1'b0: Normal operation 1'b1: Force up or down pulses via pllup or plldn Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
7	RW	0x0	disable_clock_gating To ensure proper digital clock generation, the TMDS PLL output is gated using the lock indication. If there is no lock, no output clock is provided to the digital part. 1'b0: Lock output gating enabled 1'b1: Lock output gating disabled Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
6:5	RW	0x0	pll_lockfilter PLL lock signal filtering, PLL lock needs to be inactive for N TMDS clocks until pll_locked is deactivated. 2'b0: 0 2'b1: 280 2'b2: 320 2'b3: 480 Note: Only performs functionality for GEN1 and GEN1 E202 PHYs
4	RW	0x0	hold_cal_en Hold calibration that puts equalizer gain and offset on hold in case the TMDS PLL is not locked anymore 1'b0: Hold calibration disabled 1'b1: Hold calibration enabled Notes: The PLL lock signal is used without any post-filtering. Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
3	RW	0x0	use_freqlocked The pll_locked bit used for interrupt and auto setup unit is used by freq_locked input from clock measurement unit instead of the lock signals from the TMDS PLLs. 1'b0: Use TMDS PLL lock signals for pll_locked 1'b1: Use the freq_locked from the clock measurement unit for pll_locked PLL lock mask bit 2 masks PLL LOCK signal and STS_PLL_LOCKED. It also masks PLL channel 2. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL, non-Synopsys, and GEN1 E202 PHYs
2:1	RW	0x0	pll_lockmask PLL lock masking. 2'b0: Observe all PLLs 2'b1: Observe PLL channel 0 2'b2: Observe PLL channel 1 2'b3: Observe PLL channel 2 PLL lock mask bit 0 and 1 mask PLL LOCK signal and STS_PLL_LOCKED. They also mask PLL channels 0 and 1, respectively. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
0	RW	0x0	uese_pllport Uses PLL-protected outputs. 1'b0: PLL_protected ignored 1'b1: PLL_protected used Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs

HDMI_RX_HDMI_PLL_FRQSET1

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:24	RW	0x72	pll_frq3 TMDS input clock frequency <= 140 MHz. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
23:16	RW	0x52	pll_frq2 TMDS input clock frequency <= 100 MHz. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15:8	RW	0x31	pll_frq1 TMDS input clock frequency <= 60MHz. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
7:0	RW	0x21	pll_frq0 TMDS input clock frequency <= 40 MHz. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_PLL_FRQSET2

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	use_pllh Forces pll_icphi and pll_pcphi values set on hdmi_pll_par2 register to the pll_icp_pcphi signal to PHY. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
30:28	RW	0x0	clocklsb Measurement clock rate division as /2 /4 /8 ... /256. 3'b0: 1/2 3'b1: 1/4 3'b2: 1/8 3'b3: 1/16 3'b4: 1/32 3'b5: 1/64 3'b6: 1/128 3'b7: 1/256 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
27:24	RO	0x0	reserved
23:16	RW	0x00	pll_frq6 TMDS input clock frequency <= 260 MHz. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15:8	RW	0x00	pll_frq5 TMDS input clock frequency <= 220 MHz Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
7:0	RW	0x00	pll_frq4 TMDS input clock frequency <= 180 MHz. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_PLL_PAR1

Address: Operational Base + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	pll_icp_pcp3 ICP and PCP frequency range pll_frqhi composed in the following way: pll_icp_pcphi[7:4] = pll_icphi[3:0] pll_icp_pcphi[3:0] = pll_pcphi[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
23:16	RW	0x00	pll_icp_pcp2 ICP and PCP frequency range pll_frq6 composed in the following way: pll_icp_pcp6[7:4] = pll_icp6[3:0] pll_icp_pcp6[3:0] = pll_pcp6[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15:8	RW	0x00	pll_icp_pcp1 ICP and PCP frequency range pll_frq5 composed in the followingway: pll_icp_pcp5[7:4] = pll_icp5[3:0] pll_icp_pcp5[3:0] = pll_pcp5[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
7:0	RW	0x00	pll_icp_pcp0 ICP and PCP frequency range pll_frq4 composed in the following way: pll_icp_pcp4[7:4] = pll_icp4[3:0] pll_icp_pcp4[3:0] = pll_pcp4[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_PLL_PAR2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x78	pll_icp_pcphi ICP and PCP frequency range pll_frq4 composed in the following way: pll_icp_pcp4[7:4] = pll_icp4[3:0] pll_icp_pcp4[3:0] = pll_pcp4[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
23:16	RW	0x87	pll_icp_pcp6 ICP and PCP frequency range pll_frq5 composed in the following way: pll_icp_pcp5[7:4] = pll_icp5[3:0] pll_icp_pcp5[3:0] = pll_pcp5[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15:8	RW	0x96	pll_icp_pcp5 ICP and PCP frequency range pll_frq6 composed in the followingway: pll_icp_pcp6[7:4] = pll_icp6[3:0] pll_icp_pcp6[3:0] = pll_pcp6[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
7:0	RW	0xa6	pll_icp_pcp4 ICP and PCP frequency range pll_frq6 composed in the following way: pll_icp_pcphi[7:4] = pll_icphi[3:0] pll_icp_pcphi[3:0] = pll_pcphi[3:0] Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_PLL_PAR3

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31	RW	0x0	pll_ccolf_hi Oscillator low frequency mode for frequency range above pll_frqhi. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
30:28	RW	0x7	pll_kosc_hi Oscillator gain adjustment for frequency range above pll_frqhi. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
27	RW	0x1	pll_ccolf_6 Oscillator low frequency mode for frequency range pll_frq6. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
26:24	RW	0x6	pll_kosc_6 Oscillator gain adjustment for frequency range pll_frq6 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
23	RW	0x1	pll_ccolf_5 Oscillator low frequency mode for frequency range pll_frq5. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
22:20	RW	0x4	pll_kosc_5 Oscillator gain adjustment for frequency range pll_frq5 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
19	RW	0x1	pll_ccolf_4 Oscillator low frequency mode for frequency range pll_frq4. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
18:16	RW	0x3	pll_kosc_4 Oscillator gain adjustment for frequency range pll_frq4. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15	RW	0x1	pll_ccolf_3 Oscillator low frequency mode for frequency range pll_frq4. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
14:12	RW	0x2	pll_kosc_3 Oscillator gain adjustment for frequency range pll_frq4. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
11	RW	0x1	pll_ccolf_2 Oscillator low frequency mode for frequency range pll_frq2. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
10:8	RW	0x1	pll_kosc_2 Oscillator gain adjustment for frequency range pll_frq2. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
7	RW	0x1	pll_ccolf_1 Oscillator low frequency mode for frequency range pll_frq1. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
6:4	RW	0x1	pll_kosc_1 Oscillator gain adjustment for frequency range pll_frq1. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
3	RW	0x1	pll_ccolf_0 Oscillator low frequency mode for frequency range pll_frq0. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	pll_kosc_0 Oscillator gain adjustment for frequency range pll_frq0. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_PLL_LCK_STS

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:10	RO	0x0	PLL_FRQ_INDEX Index chosen from the TMDS PLL frequency settings look up table. Note: For GEN3, HDMI 2.0, and HDMI-MHL PHYs, read as zero; fully functional for other PHYs
9	RO	0x0	reserved
8	RO	0x0	PLL_CLOCK_GATED Indicates whether the current clock output is gated because of an unlocked PLL. 1'b0: Output not gated 1'b1: Output gated Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL, non-Synopsys, and GEN1 E202 PHYs where it reads always 0
7	RO	0x0	PLL_PROTECTED_2 PLL channel 2 protection. 1'b0: Inactive 1'b1: Active Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs. For all other PHYs, it reads 0
6	RO	0x0	PLL_PROTECTED_1 PLL channel 1 protection. 1'b0: Inactive 1'b1: Active Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs. For all other PHYs, it reads 0
5	RO	0x0	PLL_PROTECTED_0 PLL channel 0 protection. 1'b0: Inactive 1'b1: Active Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs. For all other PHYs, it reads 0

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Bit	Attr	Reset Value	Description
4	RO	0x0	PLL_INLOCK_2 PLL channel 2 in lock. 1'b0: Unlocked 1'b1: Locked Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
3	RO	0x0	PLL_INLOCK_1 PLL channel 1 in lock. 1'b0: Unlocked 1'b1: Locked Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
2	RO	0x0	PLL_INLOCK_0 PLL channel 0 in lock. 1'b0: Unlocked 1'b1: Locked Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
1	RO	0x0	PLLCFG_DONE PLL configuration status. 1'b0: Not done 1'b1: Done Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
0	RO	0x0	PLL_LOCKED PLL lock status, used for interrupt generation and in the auto-setup unit . 1'b0: Unlocked 1'b1: Locked Note: For PHY GEN3, HDMI 2.0, HDMI-MHL and nonSynopsys , it reads TMDSVALID value

HDMI_RX_HDMI_CLK_CTRL

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	SEL_DEBUG Debug signal selection for BUS_CLKSRC,a possibility to make bus_clksrc available on a pin exists for debug and test purposes. SEL_DEBUG[20]: 1'b0: Normal operation: Clock from connector A/B available at bus_clksrc 1'b1: Debug signals available at bus_clksrc SEL_DEBUG[19:16] select debug signals: 4'h0: Recovery clock for resistor overload protection 4'h1: Overload signal ovl_pc_b 4'h2: Activity detector for channel 0 4'h3: Tmds_clksrc 4'h4: Test_clk (sel_busclock_shift=0xxx) or delayed busclock(sel_busclock_shift=1xxx) 4'h5: PLL0 CCO protection 4'h6: NOR (pll0_locked, NOT(pon_pll0)) -> measure PLL lock-time 4'h7: NOR (pll0_inlock_ana, NOT(pon_pll0)) -> measure PLL lock-time 4'h8: Reserved (bias & clock) 4'h9: Reserved (bias & clock) 4'ha: Reserved (channel 0) 4'hb: Reserved (channel 0) 4'hc: Reserved (channel 1) 4'hd: Reserved (channel 1) 4'he: Reserved (channel 2) 4'hf: Reserved (channel 2) Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:9	RW	0x00	SEL_BUSCLOCK_SHIFT Phase variation of the reference clock to check samplers and S2P paths, use it with sel_refclock. sel_busclock_shift[4]: 1’b0: Disable busclock shift 1’b1: Enable busclock shift sel_busclock_shift[3:0]: 4'h0: Minimum shift 4'hf: Maximum shift For test purposes only Change phase-relation between data and over-sampling phases. Vary selected phase to check if all samplers and all S2P-paths are functional. sel_busclock_shift[4]: 1’b0: busclock shift disabled -> no shift 1’b1: busclock shift enabled and shifted busclock used as reference clock for PLLs -> no longer necessary to set sel_refclock=1 sel_busclock_shift[3:0]: 4'h0: Minimum shift between busclock and input data 4'hf : Maximum shift between busclock and input data Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
8:6	RW	0x0	INV_ALIGNCLOCK Active edge selection of PLL clock to clock out data to DWC_hdmi_rx; data to DWC_hdmi_rx is always aligned to the rising edge of tmds_clksrc. 1’b0: Data is re-timed on inverted clock edge 1’b1: Data is re-timed on non-inverted clock edge Notes: [0]: Clock at interface serial-to-parallel to 1st interface block [1]: Clock at interface 1st interface block to 2nd interface block [2]: Clock at interface to DWC_hdmi_rx (tmds_clksrc) Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
5:3	RW	0x0	CLOCK_RSV Hysteresis of clock input. 3’b0: Disable 3’b1: 25mV 3’b2: 50mV 3’b3: 75mV Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	SEL_TMDSCLOCK Select source of tmdsclksrc to digital 2'b0: PLL-clock channel 0 2'b1: PLL-clock channel 1 2'b2: PLL-clock channel 2 2'b3: Inverted test_clk or delayed ibusclk Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
0	RW	0x0	SEL_REFCLOCK Reference clock for PLLs. 1'b0: Ibusclk, TMDS input clock 1'b1: Test_clk or delayed ibusclk Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs

HDMI_RX_HDMI_PCB_CTRL

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	TTL_IN_EN_INPUT_B Input behavior input B 1'b0: HDMI characteristic 1'b1: TTL characteristic Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL, non-Synopsys and GEN1 E202 PHYs
24	RW	0x0	TTL_IN_EN_INPUT_A Input behavior input A 1'b0: HDMI characteristic 1'b1: TTL characteristic Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL, non-Synopsys, and GEN1 E202 PHYs
23:20	RO	0x0	reserved
19:18	RW	0x0	SEL_PIXCLKSRC Select source divider for signal PIX_CLKSRC: 2'b0: 8 bit, ipixelclk = tmds_clksrc 2'b1: 10 bit, ipixelclk = tmds_clksrc / 1.25 2'b2: 12 bit, ipixelclk = tmds_clksrc / 1.5 2'b3: 16 bit, ipixelclk = tmds_clksrc / 2 Notes: The ipixelclk is only present on the top-level interface when the CEA video output interface is enabled (HRX_VIDOUT = 2 [CEA] or HRX_VIDOUT = 3 [COMBO]). Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
17	RW	0x0	SEL_BIAS_MASTERSLAVE Selector to choose AFE bias unit to work as master or slave 1'b0: Master, this AFE uses its own bias and might deliver bias currents to a 2nd AFE 1'b1: Slave, this AFE gets its bias currents from a 2nd AFE Notes: This bit can be used to share bias and external resistor between two AFEs.Reserved signal, bias sharing not yet implemented Only performs functionality for GEN1 (not GEN1 E202) PHYs
16	RW	0x0	INPUT_SELECT Input selector to select either input A or input B from the 2:1 HDMI input de-multiplexer 1'b0: INPUT0 applied to the reception unit 1'b1: INPUT1 applied to the reception unit Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL,, non-Synopsys, and GEN1 E202 PHYs
15:13	RO	0x0	reserved
12	RW	0x0	INV_BUSCLOCK_INPUT_B INPUT 1: invert clock to cope with PCB diversity 1'b0: No inversion 1'b1: Invert TMDS input clock Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL,, non-Synopsys, and GEN1 E202 PHYs
11	RW	0x0	SEL_BLU_INPUT_B INPUT1: select channel for blue to cope with PCB diversity; default is ch0 = blue, ch2 = red 1'b0: channel 0 1'b1: channel 2 Notes: ■ This channel swap occurs AFTER the analog front end, meaning that every analog channel tuning is associated in this register map to the original channel. ■ Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL,, non-Synopsys, and GEN1 E202 PHYs

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	SWAP_PN_INPUT_B INPUT1: invert channel to cope with PCB diversity 3'b000: No inversion on all channels 3'b001: Invert ch0 3'b010: Invert ch1 3'b011: Invert ch1, invert ch0 3'b100: Invert ch2 3'b101: Invert ch2, invert ch0 3'b110: Invert ch2, invert ch1 3'b111: Invert ch2, invert ch1, invert ch0 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL,non-Synopsys, and GEN1 E202 PHYs
7:5	RO	0x0	reserved
4	RW	0x0	INV_BUSCLOCK_INPUT_A INPUT0: invert clock to cope with PCB diversity 1’b0: No inversion 1’b1: Invert TMDS input clock Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
3	RW	0x0	SEL_BLU_INPUT_A INPUT0: select channel for blue to cope with PCB diversity; default is ch0 = blue, ch2 = red 1’b0: Channel 0 1’b1: Channel 2 Notes: ■ This channel swap occurs AFTER the analog front end, meaning that every analog channel tuning is associated in this register map to the original channel. ■ Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
2:0	RW	0x0	SWAP_PN_INPUT_A INPUT0: invert channel to cope with PCB diversity 3'b000: No inversion on all channels 3'b001: Invert ch0 3'b010: Invert ch1 3'b011: Invert ch1, invert ch0 3'b100: Invert ch2 3'b101: Invert ch2, invert ch0 3'b110: Invert ch2, invert ch1 3'b111: Invert ch2, invert ch1, invert ch0 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_PHS_CTR
Address: Operational Base + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:29	RW	0x0	SELPHASE2 Select phase for channel 2 3'h0: Automatic 3'h1: Force phase 0 3'h2: Force phase 1 3'h3: Force phase 2 3'h4: Force phase 3 3'h5: Force phase 4 3'h6: Force phase 5 3'h7: Automatic Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
28:26	RW	0x0	SELPHASE1 Select phase for channel 1 3'h0: Automatic 3'h1: Force phase 0 3'h2: Force phase 1 3'h3: Force phase 2 3'h4: Force phase 3 3'h5: Force phase 4 3'h6: Force phase 5 3'h7: Automatic Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
25:23	RW	0x0	SELPHASE0 Select phase for channel 0 3'h0: Automatic 3'h1: Force phase 0 3'h2: Force phase 1 3'h3: Force phase 2 3'h4: Force phase 3 3'h5: Force phase 4 3'h6: Force phase 5 3'h7: Automatic Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
22	RO	0x0	reserved
21:16	RW	0x00	AVERAGINGK Averaging constant for all channels (0x00 = slowest reaction ... 0x3F = fastest reaction) Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	WINDOW Position of the phase decision window relative to data 2'h0: 0 bits into future 2'h1: One bit into future 2'h2: Two bits into future 2'h3: Reserved Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
11	RO	0x0	reserved
10	RW	0x0	MAX2PHSHIFT Maximum allowed phase shift away from current average phase. 1’b0: 3 phases 1’b1: 2 phases Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
9	RW	0x0	ALLPHASES4AVG No maximum phase shift restriction for average phase calculation. 1’b0: Disable 1’b1: Enable Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
8	RW	0x0	EXTRACTPHASE Phase extraction methodology. 1’b0: Average methodology that uses the average phase 1’b1: New-phase methodology that uses a new phase Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
7:5	RO	0x0	reserved
4	RW	0x0	HOLDIFNV Hold invalid data, suppress noise. 1’b0: Disable hold 1’b1: Enable hold Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
3:2	RW	0x0	SUMEDGES Sum edges over n clocks. 2’b0: One clock 2’b1: Two clocks 2’b2: Three clocks 2’b3: Four clocks Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	EQUALIZE Digital equalization mode to ensure six-phase-sampled data integrity. 2'b0: Disable 2'b1: Expand short bits to 3 phases 2'b2: Expand short bits to 4 phases 2'b3: Reserved Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_PHS_USED

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RO	0x0	FROZEN_CH2 Channel 2 frozen Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs. For all other PHYs, it reads 0
25	RO	0x0	FROZEN_CH1 Channel 1 frozen Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs. For all other PHYs, it reads 0
24	RO	0x0	FROZEN_CH0 Channel 0 frozen Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs. For all other PHYs, it reads 0
23:22	RO	0x0	reserved
21:16	RO	0x00	PH_USED_CH2 Used phases for measurement channel 2. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
15:14	RO	0x0	reserved
13:8	RO	0x00	PH_USED_CH1 Used phases for measurement channel 1. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
7:6	RO	0x0	reserved
5:0	RO	0x00	PH_USED_CH0 Used phases for measurement channel 0. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs

HDMI_RX_HDMI_MISC_CTRL

Address: Operational Base + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	AFE_DEBUG_MODE_CH_SEL Select the channel to output during debug mode. 2'b0: Channel 0 2'b1: Channel 1 2'b2: Channel 2 2'b3: Reserved Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
29:27	RW	0x0	AFE_DEBUG_MODE_PH_SEL Phase selector for debug mode 01 3'b0: Selected by the phase picker 3'b1: Phase 0 3'b2: Phase 1 3'b3: Phase 2 3'b4: Phase 3 3'b5: Phase 4 3'b6: Phase 5 3'b7: Selected by the phase picker Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
26:25	RW	0x0	AFE_DEBUG_MODE Debug output bus select 2'b0: 10 samples from the analog to digital register interface, phase selected by phase afe_debug_ph_sel bit group 2'b1: 10 samples from the word locker, phase selected by the phase picker 2'b2: 10*6 samples from the analog to digital register interface, all 6 phases included 2'b3: reserved Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
24	RW	0x0	AFE_DEBUG_EN Analog front end debug bus enable 1'b0: Disable 1'b1: Enable Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
23:17	RO	0x0	reserved
16	RW	0x0	TESTTRIG Debug Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	VALIDDIM Valid pixel dimming, highlight non-valid pixels 1'b0: Disable 1'b1: Dim valid pixels to 25%, highlight non-valid to FFh Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
10	RW	0x0	HOLDNV8 Mark not valid with wrong color for 8 pixels 1'b0: Disable 1'b1: If not valid set color to FFh for 8 pixels Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
9	RW	0x0	HOLDNVEL Mark not valid with wrong color till the end of line 1'b0: Disable 1'b1: If not valid, set color to FFh until end of line Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
8	RW	0x0	ERRORDET_EN Error detection 1'b0: disable 1'b1: enable error detector recode comparison Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs
7:1	RO	0x0	reserved
0	RW	0x0	FREEZE Freeze operation mode 1'b0: Relock during sync 1'b1: Freeze at current lock Note: Only performs functionality for GEN1 (not GEN1 E202) PHYs

HDMI_RX_HDMI_EQOFF_CTRL

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:16	RW	0x0	RESULTS_TYPE Select information for cal_result1/cal_result0 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	EQ_SELCHAN Channel selection for equalizer offset and gain measurements. 2'b0: Channel0 2'b1: Channel1 2'b2: Channel2 2'b3: Reserved Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
13	RO	0x0	reserved
12:9	RW	0x0	OFFSET_OVRD_CH2 Offset override channel 2 (0-normal, 1-15 override value) Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
8:5	RW	0x0	OFFSET_OVRD_CH1 Offset override channel 2 (0-normal, 1-15 override value) Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
4:1	RW	0x0	OFFSET_OVRD_CH0 Offset override channel 0 (0-normal, 1-15 override value) Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
0	RW	0x0	SW_OFFSETCAL_EN Starts offset calibration Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_EQGAIN_CTRL
Address: Operational Base + offset (0x0050)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	EQ_RSV Select and control adaptive equalizer algorithm ■ 0: use backwards compatible algorithm ■ 1: use level shifter and equalizer adaptation algorithm Bit Mapping if (eq_rsv0 = 0) then (■ level shifter stage (eq_rsv3 = 0 ? B : A) disable = eq_rsv2 ■ level shifter stage (eq_rsv3 = 0 ? A : B) disable = NOT(eq_rsv1) ■ equalizer gain stage disable = [eq2 eq1 eq0] ■ 000 = maximum peaking ■ 111 = minimum peaking) else (■ level shifter stage (eq_rsv3 = 0 ? B : A) disable = eq_rsv2 ■ level shifter stage (eq_rsv3 = 0 ? A : B) disable = eq2 ■ equalizer gain stage disable = [eq1 eq0 eq_rsv3] ■ 000 = maximum peaking ■ 111 = minimum peaking Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
23	RO	0x0	reserved
22:20	RW	0x0	EQGAIN_OVR_CH2 Override values for channel 2 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
19:17	RW	0x0	EQGAIN_OVR_CH1 Override values for channel 1 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
16:14	RW	0x0	EQGAIN_OVR_CH0 Override values for channels 0 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
13	RO	0x0	reserved
12	RW	0x0	ASSUME_ACTIVITY Reserved and read as zero. Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
11	RW	0x0	SYNCINVIDEO Maximum number of sync words in each video period 1’b0: 16 1’b1: 32 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
10:9	RW	0x0	VIDEOPERIODMIN Minimum duration of video period 3'b0: 600 pixel 3'b1: 400 pixel 3'b2: 200 pixel 3'b3: 100 pixel Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
8:7	RW	0x0	MAXSYNC Proportion of sync words allowed in a measurement 3'b0: No limit to sync data in measurement 3'b1: Maximum 25% of measurement may be sync data 3'b2: Sync required 3'b3: Sync required, but maximum 25% Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
6	RW	0x0	EQ_TEMPOVR_EN Enable equalizer software override using eqgain_ovr_ch0/eqgain_ovr_ch1/eqgain_ovr_ch2 during calibration Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
5	RW	0x0	EQ_OVR_EN Enable equalizer software override using eqgain_ovr_chX Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
4	RW	0x0	SW_EQ_GAIN_EN Starts calibration If override is enabled (bit [6]/[7]) a single measurement is started Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
3:1	RW	0x0	NUMEDGES Number of edges for sdev measurement 3'b0: 32 3'b1: 64 3'b2: 128 3'b3: 192 3'b4: 256 3'b5: 384 3'b6: 512 3'b7: 1008 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

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Bit	Attr	Reset Value	Description
0	RW	0x0	HIGHIFEQUAL Decision direction if measurement results are equal 1'b0: Choose eq setting nearer 000 1'b1: Choose eq setting nearer 111 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs

HDMI_RX_HDMI_EQCAL_STS

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RO	0x0	EQOFFSET_CH2 Equalizer Calibration Offset per channel 2 registers. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
25:22	RO	0x0	EQOFFSET_CH1 Equalizer Calibration Offset per channel 1 registers. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
21:18	RW	0x0	EQOFFSET_CH0 Equalizer Calibration Offset per channel 0 registers. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
17	RO	0x0	OFFSETCAL_FAILED Equalizer Calibration Offset failed. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
16	RO	0x0	OFFSETCAL_DONE Equalizer Calibration Offset complete. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	EQGAIN_BAD_HISTO Combined result with [2..0] grouping 3'b2: Channel 2 3'b1: Channel 1 3'b0: Channel 0 (Signals from CH0/1/2_BAD_HISTOGRAM from PHY. For more details, see the HDMI RX PHY Databook.) Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
11:9	RO	0x0	EQGAIN_CH2 Equalizer calibration gain for channel 2. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
8:6	RO	0x0	EQGAIN_CH1 Equalizer calibration gain for channel 1. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
5:3	RO	0x0	EQGAIN_CH0 Equalizer calibration gain for channel 0. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
2	RO	0x0	ACT_CHANGE act_change input from PHY. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
1	RO	0x0	EQGAIN_FAILED Equalizer calibration failed. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
0	RO	0x0	EQGAIN_DONE Equalizer calibration done. For more details, see the HDMI RX PHY Databook. Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs

HDMI_RX_HDMI_EQRESULT

Address: Operational Base + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:11	RO	0x000	CAL_RESULT1 For results type 12'b0: Stddev 12'b1-3: Edgecount[1][3][5] 12'b4-7: Histogram[1][3][5][7] Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs
10:0	RO	0x000	CAL_RESULT0 For results type 12'b0: Offsetcnt 12'b1-3: Edgecount[0][2][4] 12'b4-7: Histogram[0][2][4][6] Note: For GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs, read as zero; fully functional for other PHYs

HDMI_RX_HDMI_EQ_MEAS_CTRL
Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	EYE3ENOUGH Eye quality factor 1'b0: Only quality factor 1'b1: Eye and quality factor (eye >= 3) Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
18	RW	0x1	AVGSTDDEV stddev evaluation method 1'b0: Evaluate using worst of stddev measurements 1'b1: Evaluate using average of stddev measurements Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
17	RW	0x1	MEAS16STDDEV stddev measurements per evaluation 1'b0: 4 1'b1: 16 Note: Performs functionality in all PHYs except GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
16:0	RO	0x0	reserved

HDMI_RX_HDMI_WR_CFG
Address: Operational Base + offset (0x0060)

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	VSYNC_CNT_CLEAR Vertical sync threshold counter clear

HDMI_RX_HDMI_CTRL

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0xff	VSYNC_CNT_THR Vertical sync counter threshold: Configures the number of vsync_act_edge_ists (seen in the HDMI clock domain) that must be happen to raise the vs_thr_reached_ists interrupt

HDMI_RX_HDMI_MODE_RECOVER

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	PREAMBLE_CNT_LIMIT This register field is only for debug purposes. Do not change from the default value. Minimum number of preambles needed to change to Video Data Period and Data Island Period These configuration bits work independently to Video Data and Data Island preambles, meaning that the value configured should be matched (in terms of number of characters) for each preamble to determine corresponding preamble type
26:21	RO	0x0	reserved
20:19	RW	0x0	OESSCTL3_THR OESS CTL3 threshold value These fields configure the number of HDMI clocks (minus one) that CTL3 must be asserted high to be considered as active encryption enable. Note: Configure the desired value minus one (for example, if you want to consider ENC_EN true when five cycles have been received with CTL3 asserted high, then use [hdmi_mode_recover.oessctl3_thr = 4])
18	RW	0x0	SPIKE_FILTER_EN Spike filter for CTL0..3 and DE, with single pixel spike suppression 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
17:13	RW	0x00	DVI_MODE_HYST DVI mode detection hysteresis for switching from HDMI to DVI 0x0...0x1F = 1...31 frames (frames for progressive video, fields for interlaced video) Note: Setting the value of hysteresis to zero (0) disables the hysteresis mechanism
12:8	RW	0x00	HDMI_MODE_HYST HDMI mode detection hysteresis for switching from DVI to HDMI 0x0...0x1F = 1...31 frames (frames for progressive video, fields for interlaced video) Note: Setting the value of hysteresis to zero (0) disables the hysteresis mechanism
7:6	RW	0x0	HDMI_MODE HDMI-DVI mode setting 2'b0: automatic mode (filtered) 2'b1: DVI mode 2'b2: HDMI mode 2'b3: HDMI mode Note: If MHL mode is enabled, either by software override or by cdsense, the value of this field has no impact in the operation

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	GB_DET Data island and video guard band detection control HDMI and MHL 24-bit-per-pixel Mode: 2'b0: Hard detection data island guard band (2 rows green/2 rows red/2 rows aux data); hard detection video guard band (2 rows blue/2 rows green/2 rows red) 2'b1: Medium detection data island guard band (2 rows green/2 rows red); hard detection video guard band (2 rows blue/2 rows green/2 rows red) 2'b2: Soft detection data island guard band (2 rows blue/2 rows green/1 row red OR 2 rows blue/1 row green/2 rows red OR 1 row blue/2 rows green/2 row red); Soft detection video guard band (2 rows blue/2 rows green OR 2 rows blue/2 rows red OR 2 rows green/2 rows red) 2'b3: Soft detection data island guard band (2 rows blue/2 rows green/1 row red OR 2 rows blue/1 row green/2 rows red OR 1 row blue/2 rows green/2 rows red); soft detection video guard band (2 rows blue/2 rows green OR 2 rows blue/2 rows red OR 2 rows green/2 rows red) ■ MHL PackedPixel Mode: 2'b0: Hard detection data island guard band (2 rows green/2 rows aux data); hard detection video guard band (2 rows blue/2 rows green) 2'b1: Medium detection data island guard band (2 rows green/1 row aux data); hard detection video guard band (2 rows blue/2 rows green) 2'b2: Soft detection (2 rows green) data island guard band; soft detection video guard band (2 rows blue/1 row green OR 1 row blue/2 rows green) 2'b3: Soft detection (2 rows green) data island guard band; soft detection video guard band (2 rows blue/1 row green OR 1 row blue/2 rows green)

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	EESS_OESS EESS/OESS overwrite control 2'b0: New automatic mode (check on HDMI mode or 1.1 features enabled) 2'b1: Force OESS 2'b2: Force EESS 2'b3: Automatic mode. Check for CTL[3:0] = 4'd9 or CTL[3:0] = 4'b8 during WOO. To determine valid EESS, the CTL[3:0] = 4'd9 or CTL[3:0] = 4'b8 must be at this values for at least 15 HDMI cycles. Note: If MHL mode is enabled, the value of this field will be ignored and the controller will assume EESS
1:0	RW	0x0	SEL_CTL01 Ctl0/1 signal overwrite control 2'b0: Ctl0/1 equals ctl0/1 from transmitter 2'b1: Ctl0/1 (b01=control data, b10 =data island, b00 = video data) 2'b2: Guardband area (ctl0 = video guard band, ctl1 = data guard band) 2'b3: (Ctl0 = data island and no guard band, Ctl1 = video data enable and no guard band)

HDMI_RX_HDMI_ERROR_PROTECT

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RW	0x0	RG_BLOCK_OFF Debug purpose. This field controls when the filtering of the control signals is active. 1'b0: Filter disabled (hold output) during video data period 1'b1: Filter enabled during video data period
19	RW	0x0	BLOCK_OFF Debug purpose. The field controls when the sampling of HSYNC, VSYNC, and CTL [3:0] is performed. 1'b0: Input sampling disabled during video data period 1'b1: Input sampling enabled during video data period

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Bit	Attr	Reset Value	Description
18:16	RW	0x0	VALID_MODE Selects which bit (or combination of bits) of TMDSVALID is used in the error protection block. 3’b0: Ch0 3’b1: Ch1 3’b2: Ch2 3’b3: Ch0 AND ch1 AND ch2 3’b4: Ch0 OR ch1 OR ch2 3’b5: any two channels 3’b6: Ch0 AND ch1 AND ch2 3’b7: Ch0 AND ch1 AND ch2
15:14	RO	0x0	reserved
13:12	RW	0x0	CTRL_FILT_SEN HDMI CTL signals stability filter order. Filters glitches with following HDMI clock duration: 2'b00: Disable 2'b01: 1 2'b10: 2 2'b11: 3
11:10	RW	0x0	VS_FILT_SENS VS signal stability filter order. Filters glitches with following HDMI clock duration: 2'b00: Disable 2'b01: 1 2'b10: 2 2'b11: 3
9:8	RW	0x0	HS_FILT_SENS HS signal stability filter order. Filters glitches with following HDMI clock duration: 2'b00: Disable 2'b01: 1 2'b10: 2 2'b11: 3
7:6	RW	0x0	DE_MEASURE_MODE Filter length for assigning DE regeneration length value. DE signal must have continuous length for the following number of consecutive lines: 2'b00: 2 2'b01: 3 2'b10: 5 2'b11: 9

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Bit	Attr	Reset Value	Description
5	RW	0x0	DE_REGEN Data enable regeneration 1'b0: Disable 1'b1: Enable Note: While using a 10-bit deep color mode with video modes that have the Hblanking not divisible by 4 (non-integer rest), this option causes the resulting de (data enables) to be incorrectly generated
4:3	RW	0x0	DE_FILTER_SENS DE signal stability filter order. Filters glitches with following HDMI clock duration: 2'b00: Disable 2'b01: 1 2'b10: 2 2'b11: 3
2:0	RO	0x0	reserved

HDMI_RX_HDMI_ERD_STS

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RO	0x0	ACC_VALID_STS Accumulated TMDSVALID value from each channel; if any TMDSVALID bit becomes zero, the accumulated status bit retains zero until this register is read

HDMI_RX_HDMI_SYNC_CTRL

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:3	RW	0x0	VS_POL_ADJ_MODE VS polarity adjustment 2'b0: Manual. Inverted VSYNC 2'b1: Manual, No VSYNC inversion 2'b2: Automatic 2'b3: Same as 1, Manual, No VSYNC inversion Note: It is highly recommended that you use Automatic adjustment (2) for the VS polarity adjustment. Use caution if you have set this field to Manual mode (0,1 or 3) since several modules (for example, CEA video interface) rely on correct configuration (active high VSYNC detection) to correctly operate, otherwise, the controller behavior may be affected (especially CAE and PVO video interfaces)

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	HS_POL_ADJ_MODE HS polarity adjustment 2'b0: Manual. Inverted HSYNC 2'b1: Manual, No HSYNC inversion 2'b2: Automatic 2'b3: Same as 1, Manual, No HSYNC inversion Note: It is highly recommended that you use Automatic adjustment (2) for the HS polarity adjustment. Use caution if you have set this field to Manual mode (0,1 or 3) since several modules (for example, CEA video interface) rely on correct configuration (active high HSYNC detection) to correctly operate, otherwise, the controller behavior may be affected (especially CAE and PVO video interfaces)
0	RO	0x0	reserved

HDMI_RX_HDMI_CKM_EVLTM

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:20	RW	0x1	LOCK_HYST Hysteresis for PLL lock detection 2'b0: Clk2 2'b1: Clk4 2'b2: Clk8 2'b3: Clk16 Note: This bit field is only used by the PHY in cases where the hdmi_pll_ctrl register use_freqlocked bit field is set to 1.Also, this control does not perform any functionality with GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs
19	RO	0x0	reserved
18:16	RW	0x0	CLK_HYST Maximum ihdmiclk clock variation for a stable clock rate equation: f_clk_curr - f_clk_last <= f_clk_last/(2^(clk_hyst+2))
15:4	RW	0xfff	EVAL_TIME Number of mode detection clock cycles (imodetclk) between two probes of the free running counters
3:1	RO	0x0	reserved
0	RW	0x0	CLK_MEAS_INPUT_SRC Select input0 or input1 bus clock as measurement reference 1'b0: Ibusclk input0 1'b1: Ibusclk input1

HDMI_RX_HDMI_CKM_F

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Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	MAXFREQ Maximum count for legal clock. Per default, set the maximum range 25 to 340 MHz to detect if there is a valid clock. Note: The imodetclk clock is used to sample this limit
15:0	RW	0x0000	MINFREQ Minimum count for legal clock. Per default, set the maximum range 25 to 340 MHz to detect if there is a valid clock. Note: The imodetclk clock is used to sample this limit

HDMI_RX_HDMI_CKM_RESULT

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RO	0x0	CLOCK_IN_RANGE Measured clock is stable. Note: This control has no functional meaning for GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs. The control logic is still implemented but not used for these PHY configurations
16	RO	0x0	FREQ_LOCKED Measured frequency locked. Note: This control has no functional meaning for GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs. The control logic is still implemented but not used for these PHY configurations
15:0	RO	0x0000	CLKRATE Measured clock rate in bits. Note: This control has no functional meaning for GEN3, HDMI 2.0, HDMI-MHL and non-Synopsys PHYs. The control logic is still implemented but not used for these PHY configurations

HDMI_RX_HDMI_PVO_CONFIG

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	PVO_YCC420_IPIMAP PVO YCC 420 IPI Mapping: - 1'b0: Normal Mapping - 1'b1: IPI Mapping (Exists: DWC_HDMI_RX_20==1)
0	RW	0x0	PVO_YCC422_IPIMAP PVO YCC 422 IPI Mapping: - 1'b0: Normal Mapping - 1'b1: IPI Mapping

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HDMI_RX_HDMI_RESMPL_CTRL
Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:1	RW	0x0	MAN_VID_DEREPEAT De-repeat factor for video 4'h0: disable sub-sampling, pixel sent once 4'h1: 2 x sub-sampling, pixel sent twice 4'h2: 3 x sub-sampling, pixel sent 3 times ... 4'h9: 10 x sub-sampling, pixel sent 10 times Others: Reserved
0	RW	0x0	AUTO_DEREPEAT Automatic de-repeat (subsample) as given by decoded info frame 82h 1'b0: Use setting man_vid_derepeat 1'b1: As transmitted in data_byte5[3:0]

HDMI_RX_HDMI_DCM_CTRL
Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	WO	0x0	DCM_PH_DIFF_CNT_CLR_P Reset phase difference counter 1'b0: No clear 1'b1: Clear
27:20	RW	0x00	DCM_PH_DIFF_CNT_THRES Threshold for maximum number of phases re-alignments. Crossing the threshold triggers an ihdmiclk pulse to hdmi_sts.dcm_ph_diff_cnt_overfl, and the HDMI interrupt dcm_ph_diff_cnt_overfl becomes flagged. After crossing the configured threshold, the phase diff counter hdmi_sts.dcm_phase_diff_cnt is reset
19	RO	0x0	reserved
18	RW	0x0	DCM_DEFAULT_PHASE When forcing deep color mode pixel packing phase hdmi_dcm_ctrl.dcm_pixel_phase_sel to 1, this value is: 1'b0: Take pixel packing phase from GCP packet using PP[3..0]. 1'b1: Take packing phase from hdmi_dcm_ctrl.dcm_pixel_phase
17	RW	0x0	DCM_PIXEL_PHASE_SEL Force deep color mode pixel packing phase for the next active video period. 1'b0: take pixel packing phase from GCP packet using PP[3..0] 1'b1: take pixel packing phase from dcm_pixel_phase[3..0]

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Bit	Attr	Reset Value	Description
16:13	RW	0x0	DCM_PIXEL_PHASE Pixel phase forcing setup, activate to determine packing phase used by the deep color mode FSM: 4'b0: Phase 4 (10P) 4'b1: Phase 1 (10P1, 12P1, 16P1) 4'b2: Phase 2 (10P2, 12P2) 4'b3: Phase 3 (10P3) 4'b4-14: Reserved 4'b15: Phase 0 (10P0,12P0,16P0) Values configured here must convey with HDMI deep color mode packing/depacking mechanisms and packing phase values as described in the HDMI specification. Note: Forcing this configuration to phase 0 (15) may cause the video to be incorrectly unpacked
12	RW	0x0	DCM_COLOUR_DEPTH_SEL Force deep color mode depth 1’b0: Take color depth from GCP packet using CD[3..0] 1’b1: Take color depth from dcm_color_depth[3..0]
11:8	RW	0x0	DCM_COLOUR_DEPTH Deep color mode depth selector 4’b0: Not indicated 4’b1-3: Reserved 4’b4: 24 bit 4’b5: 30 bit 4’b6: 36 bit 4’b7: 48 bit 4’b8-15: Reserved
7:6	RO	0x0	reserved
5:2	RW	0x0	DCM_GCP_ZERO_FIELDS Number of video fields with receiving GCPs with Color Depth=0 or reserved value, after which the controller reverts to 24-bit mode: 1’b0: Invalid configuration (Warning: This value forces the controller to operate continuously in 24-bit color mode.) 1’b1: 15 number of fields

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	DCM_DC_OPERATION Deep color operation, 0 = genuine HDMI 1.3 Specification Mode 2'b0: Exit on (GCP CD=0) after dcm_gcp_zero_fields, ignore PP information in these GCPs 2'b1: Exit on (GCP CD=0) after dcm_gcp_zero_fields times, use PP information in these GCPs 2'b2: Exit on (GCP CD=0 OR CD=reserved) after dcm_gcp_zero_fields times, ignore PP information in these GCPs 2'b3: Exit on (GCP CD=0 OR CD=reserved) after dcm_gcp_zero_fields, use PP information in these GCSs Note: This bit group can be used to fine-tune non-standard compliant deep color mode link conditions

HDMI_RX_HDMI_VM_CFG_CH_0_1

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VM_CH1_COL_VALUE 16-bit MSB aligned color value for video output mute function Note: If you use black as the mute color, apply the following values: ■ G_full_range = 0 ■ G_limited_range = 4096 ■ Y_limited_range = 4096
15:0	RW	0x0000	VM_CH0_COL_VALUE 16-bit MSB aligned color value for video output mute function. Note: If you use black as the mute color, apply the following values: B_full_range = 0 B_limited_range = 4096 Cb_limited_range = 32768

HDMI_RX_HDMI_VM_CFG_CH2

Address: Operational Base + offset (0x00b4)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	VM_ENABLE Video output manual mute enable: 1'b0: Video output un-muted 1'b1: Video output muted
15:0	RW	0x0000	VM_CH2_COL_VALUE 16-bit MSB aligned color value for video output mute function Note: If you use black as the mute color, apply the following values: R_full_range = 0 R_limited_range = 4096 Cr_limited_range = 32768

HDMI_RX_HDMI_SPARE

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	ACTIVITY_PKT_STS Bit[0] = activity_pkt_sts (OR of channels 0, 1, 2)

HDMI_RX_HDMI_STS

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	DCM_CURRENT_MODE Current deep color mode depth indicator 4'b0: Deep color mode not indicated 4'b1-3: Reserved 4'b4: 24 bit 4'b5: 30 bit 4'b6: 36 bit 4'b7: 48 bit 4'b8-15: reserved
27:24	RO	0x0	DCM_LAST_PIXEL_PHASE_STS Stored last pixel phase from last video period 4'b0: Phase 4 (10P4) 4'b1: Phase 1 (10P1, 12P1, 16P1) 4'b2: Phase 2 (10P2, 12P2) 4'b3: Phase 3 (10P3) 4'b4-14: Reserved 4'b15: Phase 0 of deep color mode shift FSM (10P0, 12P0, 16P0)

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	DCM_PHASE_DIFF_CNT Counts deep color mode GCP packet PP and internal phase status mismatches 8'b0: 0 mismatches 8'b1: One mismatch 8'b2: Two mismatches ... Note: This is reset as soon as the threshold is passed. 1. Software sets a threshold. 2. Hardware flags an interrupt as soon as the threshold is passed and resets this flag
15	RO	0x0	DCM_PH_DIFF_CNT_OVERFL Threshold on maximum number of phase re-alignment passed 1'b0: Not passed 1'b1: Passed
14	RO	0x0	DCM_GCP_ZERO_FIELDS_PAS Number of video fields with receiving GCPs with CD=0 OR CD=reserved information before switching back to 24-bit mode passed 1'b0: Not passed 1'b1: Passed
13	RO	0x0	CTL3_STS HDMI ctrl3 status 1'b0: Not set 1'b1: Set
12	RO	0x0	CTL2_STS HDMI ctrl2 status 1'b0: Not set 1'b1: Set
11	RO	0x0	CTL1_STS HDMI ctrl1 status 1'b0: Not set 1'b1: Set
10	RO	0x0	CTL0_STS HDMI ctrl0 status 1'b0: Not set 1'b1: Set
9	RO	0x0	VS_POL_ADJ_STS VS polarity adjust status 1'b0: Not active 1'b1: Active
8	RO	0x0	HS_POL_ADJ_STS HS polarity adjust status 1'b0: Not active 1'b1: Active

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Bit	Attr	Reset Value	Description
7	RO	0x0	RES_OVERLOAD_STS Resistor overload status 1'b0: OK 1'b1: Overload
6:4	RO	0x0	reserved
3:0	RW	0x0	DCM_CURRENT_PP Current Packing Phase 4'b0: Phase 4 (10P4) 4'b1: Phase 1 (10P1, 12P1, 16P1) 4'b2: Phase 2 (10P2, 12P2) 4'b3: Phase 3 (10P3) Others: Reserved

HDMI_RX_HDCP_CTRL

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	HDCP_ENDISLOCK HDCP Enable/Disable lock 1'b0: hdcp_enable can be used to enable or disable the HDCP module. 1'b1: lock the last state of the hdcp_enable. After this bit has been set to 1, the hdcp_enable bit only works again after a master reset to the HDMI controller. Attention: In configurations with HRX_HDCP22_EXTERNAL enabled, this bit has a similar and simultaneous effect over the HDCP22 external interface
24	RW	0x0	HDCP_ENABLE HDCP enable control 1'b0: HDCP module is disabled (by de-asserting its synchronous enable signal) and bypassed. 1'b1: HDCP is enabled. Attention: In configurations with HRX_HDCP22_EXTERNAL enabled, this bit has a similar and simultaneous effect over the HDCP22 external interface
23:22	RO	0x0	reserved
21	RW	0x0	FREEZE_HDCP_FSM Freeze HDCP State Machine 1'b0: Freeze disabled 1'b1: Freeze HDCP State Machine Note: When the derived parameter HDCP_FREZEEN = 0, this bit field reads zero.Value After Reset: 0x0 (Exists: HDCP_FREEZEEN==1)

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Bit	Attr	Reset Value	Description
20:15	RW	0x00	FREEZE_HDCP_STATE Freeze HDCP State Machine STATE (applicable only if freeze_hdcp_fsm = 1). Note: When the derived parameter HDCP_FREZEEN = 1, this bit field reads zero. 6'b0: Idle 6'b1: Authent_step0 6'b2: Authent_step1 6'b3: Authent_step2 6'b4: Authent_step3 6'b5: Authent_step4_5_6_7 6'b9: Authent_step8 6'b10: Authent_step9 6'b16: Frame_key_step0 6'b18: Frame_key_step1 6'b19: Frame_key_step2 6'b20: Frame_key_step3 6'b21: Frame_key_step4_5_6_7 6'b25: Frame_key_step8 6'b26: Frame_key_step9 6'b23: D1_frame_key_calculated 6'b22: D2_decrypt_setup 6'b6: D2_di_decrypt_setup 6'b17: D2_decrypt 6'b7: D2_di_decrypt 6'b27: D2_decrypt_finish 6'b11: D2_rekey_setup 6'b28: D2_rekey 6'b13: D2_rekey_finish_1 6'b14: D2_rekey_finish_2 6'b30: D3_unknown_blank 6'b24: D4_rekey 6'b29: D4_horizontal_blank 6'b31: D5_vertical_blank 6'b32: Frame_key_step1_ac 6'b33: Frame_key_step2_ac 6'b34: Frame_key_step3_ac 6'b35: Frame_key_step4_5_6_7_ac 6'b36: Frame_key_step8_ac 6'b37: Frame_key_step9_ac 6'b38: D1_frame_key_calculated_ac (Exists: HDCP_FREEZEEN==1)
14	RW	0x0	HDCP_VID_DE Reserved
13:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	HDCP_SEL_AVMUTE AV mute forcing test, simulate reception of set / clear avmute 2'b0: Normal mode, take data from packet extraction 2'b1: Force (AVmute=0) 2'b2: Force (AVmute=1) 2'b3: Force (AVmute=1) Note: All of these configurations have precedence over whatever is being configured in PDEC AVMUTE control registers
9:8	RW	0x0	HDCP_CTL Encryption mode 2'b0: Automatic 2'b1: OESS 2'b2: EESS 2'b3: EESS In MHL mode the EESS OESS overwrite control has no effect over the HDCP operation and the behavior will be always EESS encryption mode
7:6	RW	0x0	HDCP_RI_RATE Frame cycle period for Ri exchange 2'b0: 128 2'b1: 4 2'b2: 2 2'b3: 1
5:3	RO	0x0	reserved
2	RW	0x0	HDMI_MODE_ENABLE HDMI mode, not implemented 1'b1: Enable 1'b0: Disable
1	RW	0x0	KEY_DECRYPT_ENABLE Key decryption 1'b1: Enable 1'b0: Disable
0	RW	0x0	HDCP_ENC_EN HDCP encryption enable (only enables the encryption; the HDCP does not stop) 1'b1: Enable 1'b0: Disable

HDMI_RX_HDCP_SETTINGS

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17:16	RW	0x1	I2C_SPIKE_SUPPR Select spike suppression mode on DDC I2C, which is performed on positive edge of icfgclk 2'b00: 2 out of 2 2'b01: 2 out of 3 (majority selection) 2'b10: 3 out of 3 2'b11: 4 out of 4
15:14	RO	0x0	reserved
13	RW	0x0	HDMI_RESERVED HDCP bcaps I2C bus register bit hdmi_reserved; set to 0 to indicate no HDMI capabilities
12	RW	0x1	FAST_I2C When set to 1, the controller supports 400 kHz I2C transfers. When 0, only 100 kHz are supported
11:10	RO	0x0	reserved
9	RW	0x1	ONE_DOT_ONE When set to 1, the receiver supports EESS, Advance Cipher and Enhanced Link Verification options
8	RW	0x1	FAST_REAUTH Bcaps.When set to 1, the receiver is capable of receiving (not encrypted) video signal during the session reauthentication
7:1	RW	0x3a	HDCP_DDC_ADDR I2C slave address on DDC
0	RO	0x0	reserved

HDMI_RX_HDCP_SEED

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	KEY_DECRYPT_SEED Key decryption seed Note: In HDCP_DKSET_EXT=1 hardware configurations, writing to this register will make the controller issue a new Device Key Set read operation from the External SRAM

HDMI_RX_HDCP_BKSV1

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	HDCP_BKSV_HI HDCP receiver key selection vector as transferred to the transmitter

HDMI_RX_HDCP_BKSV0

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Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCP_BKSV_LO HDCP receiver key selection vector lower part, writing this register enable latching the entire BKSV value into the internal HDCP BKSV storage shadow register

HDMI_RX_HDCP_KIDX

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RO	0x00	HDCP_KEY_INDEX Valid range is 00h ... 27h. Hardware configuration HDCP_DKSET_EXT=0: this field is auto-incremented each time the hdcp_key0 register is written. Hardware configuration HDCP_DKSET_EXT=1: this field is autoincremented each time a DPK key is read from the Device Key Set external SRAM

HDMI_RX_HDCP_KEY1

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	WO	0x000000	HDCP_KEY_HI Encrypted secret key, only for external storage of encrypted HDCP keys A key is written by first writing the high part to hdcp_key1 and then the low part to hdcp_key0. Writing hdcp_key0 triggers decryption and storage in the key table, as well as auto incrementing of the hdcp_key_index. Note: Before writing a key, the status hdcp_key_wr_ok_sts must be polled to be '1'. The keys are only allowed to be written once after reset to prevent hackers from replacing the keys

HDMI_RX_HDCP_KEY0

Address: Operational Base + offset (0x00dc)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	HDCP_KEY_LO Encrypted secret key, only for external storage of encrypted HDCP keys A key is written by first writing the high part to hdcp_key1 and then the low part to hdcp_key0. Writing hdcp_key0 triggers decryption and storage in the key table, as well as auto incrementing of the hdcp_key_index. Note: Before writing a key, set the status of hdcp_key_wr_ok_sts 1. The keys are only allowed to be written once after reset to prevent hackers from replacing the keys

HDMI_RX_HDCP_DBG

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	HDCP_PJ Enhanced verification response value
23	RO	0x0	HDCP_AINFO Enable 1.1 features flag
22	RO	0x0	HDCP_ENDISLOCKED HDCP disable mechanism locked status indication

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21:16	RO	0x00	HDCP_FSM_STATE HDCP specification 1.4b: ■ Figure 2-7. HDCP Receiver Authentication State Diagram: states B* ■ Figure 3-2. Encryption/Decryption State Diagram (OESS): states D* ■ Figure 3-3. Encryption/Decryption State Diagram (EESS): states G* xxx states means not applicable Note: The HDMI RX HDCP FSM is shared for both OESS and EESS. When reading the hdcp_dbg.hdcp_fsm_state, the values depend on the OESS or EESS mode of operation. For some modes of operation, some values may never appear. 6'h00: Idle - B0 (D0/G0) 6'h01: Authent_step0 - [B1a (D0/G0)] 6'h02: Authent_step1 - [B1b (D0/G0)] 6'h03: Authent_step2 - [B1c (D0/G0)] 6'h04: Authent_step3 - [B1d (D0/G0)] 6'h05: Authent_step4_5_6_7 - [B1e (D0/G0)] 6'h06: D2_di_decrypt_setup - [B2 (xxx/G2'a)] 6'h07: D2_di_decrypt - [B2 (xxx/G2'b)] 6'h09: Authent_step8 - [B1f (D0/G0)] 6'h0A: Authent_step9 - [B1g (D0/G0)] 6'h0B: D2_rekey_setup - [B2 (D3a/G3a)] 6'h0D: D2_rekey_finish_1 - [B2 (D4b/xxx)] 6'h0E: D2_rekey_finish_2 - [B2 (D3c/G3c)] 6'h10: Frame_key_step0 - [B2 (D0/G0)] 6'h11: D2_decrypt - [B2 (D2b/G2b)] 6'h12: Frame_key_step1 - [B3 (D1a/G1a)] 6'h13: Frame_key_step2 - [B3 (D1b/G1b)] 6'h14: Frame_key_step3 - [B3 (D1c/G1c)] 6'h15: Frame_key_step4_5_6_7 - [B3 (D1d/G1d)] 6'h16: D2_decrypt_setup - [B2 (D2a/G2a)] 6'h17: D1_frame_key_calculated - [B2 (D1g/G1g)] 6'h18: D4_rekey - [B2 (D4a/xxx)] 6'h19: Frame_key_step8 - [B3 (D1e/G1e)] 6'h1A: Frame_key_step9 - [B3 (D1f/G1f)] 6'h1B: D2_decrypt_finish - [B2 (D2c/G2c)] 6'h1C: D2_rekey - [B2 (D3b/G3b)] 6'h1D: D4_horizontal_blank - [B2 (D4c/G3')] 6'h1E: D3_unknown_blank - [B2 (D3d/G3d)] 6'h1F: D5_vertical_blank - [B2 (D5/xxx)] 6'h20: Frame_key_step1_ac - [B2 (D1'/G1')] 6'h21: Frame_key_step2_ac - [B2 (D1'/G1')] 6'h22: Frame_key_step3_ac - [B2 (D1'/G1')]

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Bit	Attr	Reset Value	Description
			6'h23: Frame_key_step4_5_6_7_ac - [B2 (D1'/G1')] 6'h24: Frame_key_step8_ac - [B2 (D1'/G1')]
15:0	RO	0x0000	HDCP_RI Link verification response value

HDMI_RX_HDCP_AKSV1

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	HDCP_AKSV_HI Transmitted key selection vector from transmitter

HDMI_RX_HDCP_AKSV0

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HDCP_AKSV_LO Transmitted key selection vector from transmitter

HDMI_RX_HDCP_AN1

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HDCP_AN_HI Session random number

HDMI_RX_HDCP_AN0

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HDCP_AN_LO Session random number

HDMI_RX_HDCP_EESS_WOO

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x216	WOO_END Window of opportunity's last pixel, EESS mode 122 pixels after woo_end new packet transmissions are allowed. After woo_end, 104 pixels are required for frame key calculation. Therefore, the maximum tuning value is 527 + 122 - 104 = 545, else the EESS specification is violated
15:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x1ff	WOO_START Window of opportunity's first pixel, EESS mode

HDMI_RX_HDCP_I2C_TIMEOUT

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31	RW	0x0	I2C_TIMEOUT_EN Timeout enable 1'b1: Enable timeout 1'b0: Disable timeout
30:20	RO	0x0	reserved
19:0	RW	0x00000	I2C_TIMEOUT_CNT Timeout window value

HDMI_RX_HDCP_STS

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RO	0x0	HDCP_ENC_STATE Status bit that indicates the encrypted status of the current video field, as received on the HDMI bus. 1'b0: Input video not encrypted 1'b1: Input video encrypted
8	RO	0x0	HDCP_AUTH_START HDCP decryption state This bit is active after an AKSV is received and is cleared when the following events occur: ■ Controller reset (input port PON_RST_N) ■ Software resets/disables HDMI clock domain (through register dmi_sw_rst or dmi_disable_if) ■ AKSV received from the upstream Source device ■ Hardware configuration parameter HDCP_REPEATER set to True (1); also possible to clear this bit by setting hdcp_rpt_ctrl.rpt_timeout or hdcp_rpt_ctrl.rpt_lost_auth, depending on the authentication state
7:1	RO	0x0	reserved
0	RO	0x0	HDCP_KEY_WR_OK_STS Status flag to indicate whether key set writing is allowed 1'b0: Not allowed 1'b1: Allowed

HDMI_RX_MD_HCTRL1

Address: Operational Base + offset (0x0140)

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Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:8	RW	0x1	HACT_PIX_ITH hact_pix interrupt threshold If the difference in two consecutive values of hact_pix exceeds the defined threshold value, the interrupt hact_pix is triggered. 3'b000: 1 3'b001: 2 3'b010: 4 3'b011: 8 3'b100: 16 3'b101: 32 3'b110: 64 3'b111: 128
7:6	RO	0x0	reserved
5	RW	0x0	HACT_PIX_SRC Active length selection (between DE and HS) 1'b0: DE (counts the length of Data Enable) 1'b1: HS (counts the length of Horizontal Sync)
4	RW	0x1	HTOT_PIX_SRC Reference selection for htot_pix measurements 1'b0: HS 1'b1: DE
3:0	RO	0x0	reserved

HDMI_RX_MD_HCTRL2

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:12	RW	0x0	HS_CLK_ITH hs_clk interrupt threshold If the difference in two consecutive values of hs_clk exceeds the defined threshold value, the interrupt hs_clk is triggered. 3'b0: 1 3'b1: 2 3'b2: 4 3'b3: 8 3'b4: 16 3'b5: 32 3'b6: 64 3'b7: 128
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	HTOT32_CLK_ITH htot32_clk interrupt threshold If the difference in two consecutive values of htot32_clk exceeds the defined threshold value, the interrupt htot32_clk is triggered. 3'b0: 1 3'b1: 2 3'b2: 4 3'b3: 8 3'b4: 16 3'b5: 32 3'b6: 64 3'b7: 128
7:6	RO	0x0	reserved
5	RW	0x0	VS_ACT_TIME Vertical syncs are considered to be inactive when the time between two rising edges is larger than the value indicated in this field. 1'b0: 2^20 imodetclk cycles 1'b1: 2^21 imodetclk cycles
4:3	RW	0x0	HS_ACT_TIME Horizontal syncs and data enable are considered to be inactive, when the time between two rising edges exceeds the value defined by this field. 2'b00: 2^16 - 1 imodetclk cycles 2'b01: 2^17 - 1 imodetclk cycles 2'b10: 3 x 2^16 - 1 imodetclk cycles 2'b11: 2^18 - 1 imodetclk cycles
2	RO	0x0	reserved
1:0	RW	0x0	H_START_POS Start of horizontal measurements 2'b00: 1/8 of frame duration 2'b01: 1/4 of frame duration 2'b10: 3/8 of frame duration 2'b11: 1/2 of frame duration Note: For interlaced modes, h_start_pos cannot be set to 1/2 frame. For the field alternative 3D video mode, you cannot use 1/2 and 1/4 of a frame setting.For any of these conditions, the measurement is performed during a vblank period leading to incorrect horizontal measurements values

HDMI_RX_MD_HT0

Address: Operational Base + offset (0x0148)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	HTOT32_CLK Total time in horizontal imodetclk clock accumulated over 32 lines. This value should be multiplied by two to obtain correct final value. HTOTAL = (2 x htot32_clk x (FtmdsFmodet)32
15:0	RO	0x0000	HS_CLK Horizontal sync time in the imodetclk clock

HDMI_RX_MD_HT1

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	HTOT_PIX Total horizontal sync time in pixel clocks
15:0	RO	0x0000	HOFS_PIX Horizontal offset time in pixel clocks

HDMI_RX_MD_HACT_PX

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	HACT_PIX Depending on the value defined in md_hctrl1.hact_pix_src, this field returns either the measured active length in pixel clocks between two active edges of data enable or horizontal sync

HDMI_RX_MD_HACT_RSV

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	x'bxxx(bits < 4), x'hxxxx(bits >= 4)

HDMI_RX_MD_VCTRL

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	V_OFFS_LIN_MODE VS offset to line measurement mode 1'b0: Measure offset between the selected V-edge and the DE signal of first active line 1'b1: Measure active length of VS
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	V_EDGE Selects reference edge for all vertical based measurements 1'b0: Rising 1'b1: Falling
0	RW	0x0	V_MODE Vertical measurement mode, update on every or every second VS 1'b0: Progressive 1'b1: Interlaced

HDMI_RX_MD_VSC

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	VS_CLK Vertical sync pulse duration (measured number of lines in imodetclk clock cycles)

HDMI_RX_MD_VTC

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VTOT_CLK Frame duration measured between trailing vsync edges (measured number of lines in imodetclk clock cycles)

HDMI_RX_MD_VOL

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	VOFS_LIN Vertical offset lines or vertical sync lines depending on v_offs_lin_mode

HDMI_RX_MD_VAL

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	VACT_LIN Vertical active lines

HDMI_RX_MD_VTH

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x2	VOFS_LIN_ITH Vofs_lin interrupt threshold configuration. Generates corresponding interrupt whenever the difference between two consecutive counts is: 2'b00: 1 2'b01: 2 2'b10: 3 2'b11: 4
9:8	RW	0x0	VACT_LIN_ITH x'bxxx(bits < 4), x'hxxxx(bits >= 4)
7:6	RW	0x0	VTOT_LIN_ITH Vtot_lin interrupt threshold configuration. Generates corresponding interrupt whenever the difference between two consecutive counts is: 2'b00: 1 2'b01: 2 2'b10: 3 2'b11: 4
5:3	RW	0x2	VS_CLK_ITH Vs_clk interrupt threshold, defined by 2^(vs_clk_ith + 3) imodetclk cycles
2:0	RW	0x2	VTOT_CLK_ITH Vtot_clk interrupt threshold, defined by 2^(vtot_clk_ith + 3) imodetclk cycles

HDMI_RX_MD_VTL

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	VTOT_LIN Vertical total lines

HDMI_RX_MD_IL_CTRL

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	PHASE_VALUE Phase value to be used when phase_manual is set to 1
0	RW	0x0	PHASE_MANUAL Forces phase to phase_value value

HDMI_RX_MD_IL_SKEW

Address: Operational Base + offset (0x0178)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RO	0x0	PHASE Phase as determined by skew auto detection mechanism
2:0	RO	0x0	SKEW Skew between VS and HS in actual frame in terms of 1/8 line width, that is, the last measured actual frame skew. It can always keep changing. (0 = 0, 1 = 1, ... 7 = 7)

HDMI_RX_MD_IL_POL

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	FAFIELDDET_EN Enables field detection when in 3D field alternative video mode
1:0	RW	0x0	FIELD_POL_MODE Field polarity mode 2'b00: Normal (automatic detection) 2'b01: Inverted (automatic detection) 2'b10: Field0, set always to field 0, ilace is set to 0 2'b11: Field1, set always to field 1, ilace is set to 0 Note: It is highly recommended that you use Normal mode for the field polarity for CEA Video Output. Use caution if you have set this field to inverted (01), field0 (10), or field1 (11) and are using CEA video output because CEA requires interlace/progressive mode to be accurate, otherwise, the behavior may be affected

HDMI_RX_MD_STS

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RO	0x0	ILACE_STS Video interlace or progressive active status 1'b0: Progressive 1'b1: Interlace
2	RO	0x0	DE_ACTIVITY_STS Active DE status 1'b0: Inactive 1'b1: Active during the md_hctrl2.hs_act_time configured window
1	RO	0x0	VS_ACT_STS Active VS status 1'b0: Inactive 1'b1: Active during the md_hctrl2.vs_act_time configured window

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Bit	Attr	Reset Value	Description
0	RO	0x0	HS_ACT_STS Active HS status 1'b0: Inactive 1'b1: Active during the md_hctrl2.hs_act_time configured window

HDMI_RX_AUD_CTRL

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	HBR_MODE HBR support over S/PDIF and I2S audio interfaces 1'b0: Not supported 1'b1: Supported Note: When the controller is configured with HRX_AUDPLL_SC==1 and receiving HBR audio stream, the Silicon Creation Audio PLL is only configured to multiply the Audio clock by 4 (mandatory for HBR operation) if this bit is set
7:3	RO	0x0	reserved
2:1	RW	0x0	FILT_INIT_MODE Initialization type of asp_filter, not used
0	RW	0x0	ACLK_PWR_MODE Set power mode of external audio clock generation 1'b0: All off 1'b1: Power_on not used

HDMI_RX_AUD_PLL_CTRL

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RO	0x0	PLL_LOCK_STABLE Audio PLL lock stable indication Note: Writing to this bit has no effect. If this bit is written to, however, no APB error flag occurs because APB errors only occur at the register level and not the bit level
30:29	RO	0x0	reserved
28	RW	0x0	PLL_LOCK_FILTER_BYP Bypass PLL lock low level filter (filters glitches with duration less than eight icfgclk cycles)
27:24	RW	0x0	PLL_LOCK_TOGGLE_DIV Number of 64xicfgclk clock cycle windows used to evaluate stability of audio PLL lock (audio pll window defined by 2 * 512 * 64 * (ipll_lock_toggle_div_qstc + 2) * 1/icfgclk)
23:0	RO	0x0	reserved

HDMI_RX_AUD_CLK_CTRL

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Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	CTS_N_REF Use cts_decoded and n_decoded from audio clock regeneration InfoFrames or use manual CTS and N value settings of fields cts_man and n_man 1'b0: Decoded 1'b1: Manual
3:0	RO	0x0	reserved

HDMI_RX_AUD_CLK_STS

Address: Operational Base + offset (0x023c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	CTS_N_REF Use cts_decoded and n_decoded from audio clock regeneration InfoFrames or use manual CTS and N value settings of fields cts_man and n_man. 1'b0: Decoded 1'b1: Manual
3:1	RO	0x0	reserved
0	RW	0x0	x'bxxx(bits < 4), x'hxxxx(bits >= 4)

HDMI_RX_AUD_FIFO_CTRL

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	AFIF_SUBPACKET_DESEL When receiving multi-stream audio, it controls which input streams are stored in the audio FIFO. (Exists: DWC_HDMI_RX_20==1)
23:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	AFIF_SUBPACKETS Consider packet type 0x02 and packet type 0x07 layout 0 sample_present on audio FIFO storage 1'b0: Store all sub packets regardless of sample_present.spX 1'b1: Store only sub packets with sample_present.spX = 1 If you would like to store audio sample subpackets with sample present 1 or 0, this bit field is only to command the FIFO storage. In the HDMI 1.4b specification, sample_present.spX indicates if subpacket X contains audio samples. If sample_present is 1, then the respective subpacket contains a valid sample. If sample_present is 0, it may be ignored because it does not contain data from the audio sample. There is not any value in storing the subpackets with no audio samples. Therefore, you must determine if you want to store them although storing subpackets with no valid samples is of no use and fills the audio FIFO unnecessarily
15:1	RO	0x0	reserved
0	RW	0x0	AFIF_INIT Clear audio FIFO by resetting the write and read pointer 1'b0: No clear 1'b1: Clear Note: This is a audio FIFO functional reset, but the memory is not filled with any reset pattern. To guarantee correct action of this afif_init, the software must grant that this bit is high for at least (icfgclk_max(175 MHz)/(32 kHz*128))*(1/(32 kHz*128)) > 10.4uS

HDMI_RX_AUD_FIFO_TH

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	AFIF_TH_START Fill-state threshold for starting read-out when threshold is crossed (corresponding write/read pointer address = afif_th_start * 4) Note: When afif_thr_start is triggered, afif_fill_max and afif_fill_min are cleared to have valid fill states available later, and the interrupt flag afif_ths_pass is set
17:9	RW	0x000	AFIF_TH_MAX Maximum FIFO fill state threshold (corresponding write/read pointer address = afif_th_max * 4). Note: Refers to FIFO full level; the FIFO level which triggers the audio mute is FIFO depth, afif_th_max, or IRQ afif_th_max_flag can be triggered

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	AFIF_TH_MIN Minimum FIFO fill state threshold (corresponding write/read pointer address = afif_th_min * 4). Note: Refers to FIFO zero-level; audio mute or IRQ afif_th_min_flag can be triggered

HDMI_RX_AUD_FIFO_FILL_S

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	x'bxxx(bits < 4), x'hxxxx(bits >= 4)

HDMI_RX_AUD_FIFO_CLR_MM

Address: Operational Base + offset (0x024c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	AFIFO_CLEAR_FILL Clear afif_fill_min/afif_fill_max 1'b0: No operation 1'b1: Clear Note: To guarantee correct action of this afifo_clear_fill, the software must grant that this bit is high for at least (icfgclk_max(175MHz)/(32KHz*128))*(1/(32KHz*128)) > 10.4uS

HDMI_RX_AUD_FIFO_FILLSTS

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	AFIF_FILL_MAX Long-term maximum detected fill state (corresponding FIFO address = afif_fill_max * 4) Note: Due to synchronization timing differences between ihdmiclk and iaudclk, and depending on the setting of the HDMIRXDATASYNCDEPTH configuration parameter, this value can actually report +1 than the real maximum occupation in the audio FIFO. For this reason, this value should be read as qualitative instead of quantitative

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	AFIF_FILL_MIN Long-term minimum detected fill state (corresponding FIFO address = afif_fill_min * 4) Note: Due to synchronization timing differences between ihdmiclk and iaudclk, and depending on the setting of the HDMIRXDATASYNCDEPTH configuration parameter, this value can actually report +1 than the real maximum occupation in the audio FIFO. For this reason, this value should be read as qualitative instead of quantitative

HDMI_RX_AUD_CHEXTR_CTRL

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:8	RW	0x0	CH_MAP_7_5 Channel allocation bits 7 to 5 according to CEA-861-E specification
7	RW	0x0	CH_MAP_MANUAL Enable manual output channel mapping for layout 1 at the serial audio output interfaces 1’b0: Automatic channel mapping according to the received Audio InfoFrame packet byte 4 1’b1: Manual channel mapping according to ch_map[4..0]
6:2	RW	0x00	CH_MAP_4_0 Configures the output channels as required by the channel mapping according to CEA-861-D, Table 20 at the serial audio output interfaces 5'b0: [ch1 ch2] 5'b1, 2, 3: [ch1 ch2 ch3 ch4] 5'b4, 8: [ch1 ch2 ch5 ch6] 5'b5, 6, 7, 9, 10, 11: [ch1 ch2 ch3 ch4 ch5 ch6] 5'b12, 16, 24, 28: [ch1 ch2 ch5 ch6 ch7 ch8] 5'b20: [ch1 ch2 ch7 ch8] 5'b21, 22, 23: [ch1 ch2 ch3 ch4 ch7 ch8] all others: [ch1 ch2 ch3 ch4 ch5 ch6 ch7 ch8]
1:0	RW	0x0	AUD_LAYOUT_CTRL Configures the audio output layout on the serial audio output interfaces 2’b0: Layout automatically determined by ASP packet information 2’b1: Layout automatically determined by ASP packet information 2’b2: Layout 0 2’b3: Layout 1

HDMI_RX_AUD_MUTE_CTRL

Address: Operational Base + offset (0x0258)

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Bit	Attr	Reset Value	Description
31	RW	0x0	APPLY_INT_MUTE This field applies an internal mute: 1'b0: Internal mute not applied; mute function applied externally and the oaud_extmute output is asserted when a mute condition is raised. 1'b1: Internal mute applied; mute behavior does not change
30:23	RO	0x0	reserved
22:21	RW	0x0	APORT_SHDW_CTRL This field allows the control of when the register fields aud_sao_ctrl.spdif_disable, aud_sao_ctrl.i2s_disable, aud_sao_ctrl.sck_disable, and aud_sao_ctrl.ws_disable are internally shadowed. The options are as follows: 2’b0: VS 2’b1: CTS update 2’b2: Reserved 2’b3: Disabled (instant update)
20:19	RW	0x0	AUTO_ACLK_MUTE Automatic audio output clock mute 2’b0: Disable 2’b1: Overfl_trig, automatically enable/disable sck output when FIFO over- or underflow occurs 2’b2: Mute_trig, automatically enable/disable sck output when mute state is reached/left due to forced audio mute 2’b3: Overfl_mute_trig, both conditions 01 and 10
18:17	RO	0x0	reserved
16:10	RW	0x00	AUD_MUTE_SPEED Mute/unmute time period for all channels 7'd0: Reserved 7'd1 ..127: Allowed range Note: Time_period = (131072 * aud_mute_speed)/frequency(icfgclk)
9:8	RO	0x0	reserved
7	RW	0x0	AUD_AVMUTE_EN Control audio mute according to the pktdec_setavmute/pktdec_clravmute state received. 1’b0: Disable control, consider aud_mute_sel only 1’b1: Enable control

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	AUD_MUTE_SEL Manual/automatic audio mute control 2'b0: Force unmute (overrules all except when underflow condition occurs) 2'b1: Automatic mute when exceeding, FIFO thresholds afif_th_max/min 2'b2: Automatic mute enable for FIFO over- underflow 2'b3: Force mute (overrules all)
4:3	RW	0x0	AUD_MUTE_MODE Selects mute ramp to be applied at audio outputs: 2'b0: When entering in mute, no ramp applied samples set to 0. The -3db ramp is applied to input stream when leaving mute. For aud_mute_sel in automatic mode (1 or 2), this configuration forces mute. 2'b1: -3db amplitude steps for linear audio perception. Always holds last sample when entering mute. Ramp is applied to input stream when leaving mute. 2'b2: -3db amplitude steps for linear audio perception. Always holds last sample when entering mute except when aud_mute_sel is 3, in which case the ramp is applied to input stream. Ramp is applied to input stream when leaving mute. 2'b3: S-curve amplitude variation. Always holds last sample when entering mute. When entering mute, if aud_mute_sel is equal to 0, 1, or 2, the applied curve actually is a -3db amplitude step ramp. An S-Curve Ramp is applied to input stream when leaving mute
2:1	RW	0x0	AUD_TTONE_FS_SEL Test tone sample frequency fs, sinus frequency = fs/32 kHz 2'b0: fs_32 kHz, 32.0 kHz 2'b1: Reserved 2'b2: Reserved 2'b3: Reserved
0	RW	0x0	TESTTONE_EN 16-bit p-p (0 dBfs) sinusoidal test tone (1 kHz for fs=32 kHz) on all channels, sample frequency selection by aud_ttone_fs_sel disabled 1'b0: Disable 1'b1: Enable Note: This functionality only works if the HDMI RX Controller receives the audio input, and the audio is configured for two channels and layout 1

HDMI_RX_AUD_FIFO_FILLSTS1

Address: Operational Base + offset (0x025c)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	AFIF_FILL_STATE Current fill state, corresponding FIFO address = afif_fill_state

HDMI_RX_AUD_SAO_CTRL

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	I2S_LPCM_BPCUV Enable output of BPCUV bits in I2S audio interface, when using Linear PCM audio format. 1'b0: Disabled 1'b1: Enabled Note: This bit can only be set while in I2S 32 bit mode (aud_sao_ctrl:i2s_32_16 = 1)
10	RW	0x1	WS_DISABLE Disable I2S Word Select output (oaud_ws) 1'b0: Output enabled 1'b1: Output disabled
9	RW	0x1	SCK_DISABLE Disable oaudclk output 1'b0: Enabled 1'b1: Disabled
8:5	RW	0xf	I2S_DISABLE Disable i2s[3:0] outputs bit = 0, Audio enabled bit = 1, Audio disabled Note: Shadowing is synchronized, as defined in aport_shdw_ctrl
4:1	RW	0xf	SPDIF_DISABLE Disable spdif[3:0] outputs bit = 0, audio enabled bit = 1, audio disabled Note: Shadowing is synchronized, as defined in aport_shdw_ctrl
0	RW	0x0	I2S_32_16 Select 32 or 16 bit I2S output 1'b0: 16 bit (I2S clock frequency is 32fs) 1'b1: 32 bit (I2S clock frequency is doubled: 64fs) Select I2S clock frequency if hbr_mode is enabled and receiving HBR or NL-PCM audio 1'b0: 32 bit, I2S clock frequency is 128fs 1'b1: 32 bit, I2S clock frequency is 256fs

HDMI_RX_AUD_PAO_CTRL

Address: Operational Base + offset (0x0264)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x0	PAO_RATE Controls the audio rate for the Parallel Audio Output interface. When in auto-mode, the controller uses the type of packet whose detection is configured in the pdec_audiodet_ctrl.audiodet_threshold. 2'b00 - Standard forced mode (AUDS/HBR/DST mode) (default) 2'b01 - OBA forced mode 2'b10 - Reserved 2'b11 - Automatic mode
15:13	RO	0x0	reserved
12	RW	0x0	PAO_DISABLE Parallel Audio Output disable control
11:4	RO	0x0	reserved
3	RW	0x0	AUDIO_FMT_2 1’b0: Multi Audio Stream packets 1’b1: One Bit Multi-Stream packets (Exists: DWC_HDMI_RX_20==1)
2:1	RW	0x0	AUDIO_FMT Parallel audio output format information force value 2’b0: L-PCM or Compressed Audio at Layout 0 / L-PCM Multi-Channel at Layout 1 2’b1: SACD One Bit Audio - DSD 2’b2: Compressed SACD One Bit Audio - DST 2’b3: HBR Compressed Audio
0	RW	0x0	AUDIO_FMT_SEL Parallel audio output format information 1’b0: Automatic long term packet information extraction 1’b1: Manual forcing using audio_fmt information

HDMI_RX_AUD_SPARE

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RO	0x0	OBA_OBM_SAMPLES_INVALID Depending on the audio type received, this bit holds the following information: ■ One Bit Audio Sample Packet (OBA) samples_invalid bits ■ One Bit Multi-Stream Audio Sample Packet (OBM) stream_invalid bits Note: These bits are only updated for the above described audio types. Upon audio type change (to any but the above described types), these bits retain the value from last received AUDS or MAS packet

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	OBA_OBM_SAMPLES_PRESEN Depending on the audio type received, this bit holds the following information: ■ One Bit Audio Sample Packet (OBA) samples_present bits. ■ One Bit Multi-Stream Audio Sample Packet (OBM) stream_present bits Note: These bits are only updated for the above described audio types. Upon audio type change (to any but the above described types), these bits retain the value from last received AUDS or MAS packet
15:8	RO	0x0	reserved
7:4	RO	0x0	AUDS_MAS_SAMPLE_FLAT Depending on the audio type received, this bit holds the following information: ■ Audio Sample Packet (AUDS) sample_flat bits ■ Multi-Stream Audio Sample Packet (MAS) stream_flat bits (for HDMI 2.0 only) Note: These bits are only updated for the above described audio types. Upon audio type change (to any but the above described types), these bits retain the value from last received AUDS or MAS packet
3:0	RO	0x0	AUDS_MAS_SAMPLE_PRESEN Depending on the audio type received, this bit holds the following information: ■ Audio Sample Packet (AUDS) sample_present bits ■ Multi-Stream Audio Sample Packet (MAS) stream_present bits (for HDMI 2.0 only) Note: These bits are only updated for the above described audio types. Upon audio type change (to any but the above described types), these bits retain the value from last received AUDS or MAS packet

HDMI_RX_AUD_FIFO_STS

Address: Operational Base + offset (0x027c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	AFIF_OVERFL_STS FIFO overflow indication, lesser data picked up than delivered by packets 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
3	RW	0x0	AFIF_UNDERFL_STS FIFO underflow indication, more data picked up than delivered by packets 1'b0: OK 1'b1: Underflow
2	RO	0x0	AFIF_THS_PASS_STS Indication that Audio FIFO start threshold is crossed 1'b0: Not crossed 1'b1: Crossed Note: When afif_thr_start is triggered, afif_fill_max and afif_fill_min are cleared to have valid fill states available afterwards and the interrupt flag afif_ths_pass is set
1	RO	0x0	AFIF_TH_MAX_STS Data content above maximum threshold 1'b0: OK 1'b1: Above threshold Note: The maximum threshold value is calculated as a positive offset from the end of the FIFO down into the memory locations
0	RW	0x0	AFIF_TH_MIN_STS Data content below minimum threshold 1'b0: OK 1'b1: Below threshold Note: The minimum threshold value is calculated as a positive offset from the start of the FIFO up into the memory locations

HDMI_RX_AUDPLL_GEN_CTS

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	AUDPLL_CTS_MANUAL Manual CTS value The manual value set in this register only takes effect if register aud_clk_ctrl.cts_n_ref is set to 1 (manual mode enable)

HDMI_RX_AUDPLL_GEN_N

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x00000	AUDPLL_N_MANUAL Manual N value The manual value set in this register only takes effect if register aud_clk_ctrl.cts_n_ref is set to 1 (manual mode enable)

HDMI_RX_AUDPLL_GEN_CTRL_RW1

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPLL_CTRLBUS_31_0 Generic control bits 31 to 0. Any value written here reflects directly in the output control port (at icfgclk)

HDMI_RX_AUDPLL_GEN_CTRL_RW2

Address: Operational Base + offset (0x028c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPLL_CTRLBUS_63_32 Generic control bits 63 to 32. Any value written here reflects directly in the output control port (at icfgclk)

HDMI_RX_AUDPLL_GEN_CTRL_W1

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPLL_P_CTRLBUS_31_0 Pulse generic control bits 31 to 0. Auto-clear register. Value 1 written to a bit generates an active high pulse at the corresponding bit in the pulse output control port (at icfgclk)

HDMI_RX_AUDPLL_GEN_STS_RO1

Address: Operational Base + offset (0x02a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AUDPLL_STSBUS_31_0 Generic status bits 31 to 0. Any value in the interface input status bus is synchronized to this register (by icfgclk)

HDMI_RX_AUDPLL_GEN_STS_RO2

Address: Operational Base + offset (0x02a4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPLL_STSBUS_63_32 Generic status bits 63 to 32. Any value in the interface input status bus is synchronized to this register (by icfgclk)

HDMI_RX_AUDPLL_SC_NDIVCTSTH

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Address: Operational Base + offset (0x02a8)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	AUDPLL_SC_DIVTHRESHOLD N/CTS division threshold

HDMI_RX_AUDPLL_SC_CTS

Address: Operational Base + offset (0x02ac)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	AUDPLL_SC_CTS_MANUAL Manual CTS value The manual value set in this register only takes effect if register aud_clk_ctrl.cts_n_ref is set to 1 (manual mode enable)

HDMI_RX_AUDPLL_SC_N

Address: Operational Base + offset (0x02b0)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	AUDPLL_SC_N_MANUAL Manual N value The manual value set in this register only takes effect if register aud_clk_ctrl.cts_n_ref is set to 1 (manual mode enable)

HDMI_RX_AUDPLL_SC_CTRL

Address: Operational Base + offset (0x02b4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	AUDPLL_SC_CTSTHRESHOLD Threshold value for hysteresis mechanism. Implements an hysteresis filter for CTS variations
7	RO	0x0	reserved
6	RW	0x0	AUDPLL_SC_BYPASS Connects to BYPASS SC audio PLL input. PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV
5	RW	0x0	AUDPLL_SC_FOUTVCOPD Connects to FOUTVCOPD SC audio PLL input, Power down buffered VCO clock
4	RW	0x0	AUDPLL_SC_FOUT4PHASEPD Connects to FOUT4PHASEDPD SC audio PLL input. Power down 4-phase clocks and 2X, 3X, 4X clocks
3	RW	0x0	AUDPLL_SC_FOUTPOSTDIVPD Connects to FOUTPOSTDIVPD SC audio PLL input. Power down all outputs except for buffered VCO clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	AUDPLL_SC_DSMPD Connects to DSMPD SC audio PLL input. Power down delta sigma modulator
1	RW	0x0	AUDPLL_SC_DACPD Connects to DACPD SC audio PLL input. Power down quantization noise cancellation DAC
0	RW	0x0	AUDPLL_SC_PD Connects to PD SC audio PLL input. Global power down

HDMI_RX_AUDPLL_SC_STS1

Address: Operational Base + offset (0x02b8)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:21	RO	0x0	AUDPLL_SC_POSTDIV2 Connects to POSTDIV2 SC audio PLL input. For more information, see Silicon Creations documentation
20:18	RO	0x0	AUDPLL_SC_POSTDIV1 Connects to POSTDIV1 SC audio PLL input. For more information, see Silicon Creations documentation
17:6	RO	0x000	AUDPLL_SC_FBDIV Connects to FBDIV SC audio PLL input. For more information, see Silicon Creations documentation
5:0	RO	0x00	AUDPLL_SC_REFDIV Connects to REFDIV SC audio PLL input. For more information, see Silicon Creations documentation

HDMI_RX_AUDPLL_SC_STS2

Address: Operational Base + offset (0x02bc)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:1	RO	0x0000000	AUDPLL_SC_FRAC Connects to FRAC SC audio PLL input. For more information, see Silicon Creations documentation
0	RO	0x0	AUDPLL_SC_ST_CONFRDY Status signal that becomes high when the controller internal algorithm is done with the new N and CTS values and when the outputs from controller to SC audio PLL are updated

HDMI_RX_SNPS_PHYG3_CTRL

Address: Operational Base + offset (0x02c0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	PHYSVSRETMODEZ PHY GEN3, HDMI 2.0, HDMI-MHL Enables retention mode. For more information, refer to PHY GEN3, HDMI 2.0, HDMIMHL documentation for more information
5:4	RW	0x0	CFGCLKFREQ PHY GEN3, HDMI 2.0, HDMI-MHL configuration clock range selection. For more information, refer to PHY GEN3, HDMI 2.0, HDMIMHL documentation for more information
3:2	RW	0x0	PORTSELECT PHY GEN3, HDMI 2.0, HDMI-MHL port selection control. PHY GEN3, HDMI 2.0, HDMI-MHL macro supports up to four HDMI ports. This bit controls the port that is active in the PHY Macro. For more information, refer to PHY GEN3, HDMI 2.0, HDMI-MHL documentation for more information
1	RW	0x0	PHYPDDQ PHY PDDQ control For more information, refer to PHY GEN3, HDMI 2.0, HDMIMHL documentation for more information
0	RW	0x0	PHYRESET PHY reset control For more information, refer to PHY GEN3, HDMI 2.0, HDMIMHL documentation for more information

HDMI_RX_I2CM_PHYG3_SLAVE

Address: Operational Base + offset (0x02c4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	I2CMP_SLAVEADDR Slave Address for Read/Write Destination

HDMI_RX_I2CM_PHYG3_ADDRESS

Address: Operational Base + offset (0x02c8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	I2CMP_ADDR Address for Read/Write Request

HDMI_RX_I2CM_PHYG3_DATAO

Address: Operational Base + offset (0x02cc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	I2CMP_DATAO Data to be written on register pointed by i2cmp_addr[7:0]

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HDMI_RX_I2CM_PHYG3_DATAI
Address: Operational Base + offset (0x02d0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	I2CMP_DATAI Data to be read into the register pointed by i2cmp_addr[7:0]

HDMI_RX_I2CM_PHYG3_OPERATION
Address: Operational Base + offset (0x02d4)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	I2CMP_READ Read operation request
0	WO	0x0	I2CMP_WRITE Write operation request

HDMI_RX_I2CM_PHYG3_MODE
Address: Operational Base + offset (0x02d8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	I2CMP_FASTMODE I2C fast mode operation 1'b0: Standard Mode 1'b1: Fast Mode

HDMI_RX_I2CM_PHYG3_SOFTRST
Address: Operational Base + offset (0x02dc)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	I2CMP_SOFTRST I2C Master PHY Software Reset. This field can be used to unlock the I2C lines in case they get hanged during an operation. Note: Take caution when using this field in a PHY_EXTERNAL hardware configuration.This SoftReset will immediately set both SCL and SDA lines high without actually ending the current I2C operation, which may cause I2C Slave unexpected behavior

HDMI_RX_I2CM_PHYG3_SS_CNTS
Address: Operational Base + offset (0x02e0)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0190	I2CMP_SS_SCL_HCNT PHY I2C Standard Speed SCL High Level Counter
15:0	RW	0x01d6	I2CMP_SS_SCL_LCNT PHY I2C Standard Speed SCL Low Level Counter

HDMI_RX_I2CM_PHYG3_FS_HCNT
Address: Operational Base + offset (0x02e4)

Bit	Attr	Reset Value	Description
31:16	RW	0x003c	I2CMP_FS_SCL_HCNT PHY I2C Fast Speed SCL High Level Counter
15:0	RW	0x0082	I2CMP_FS_SCL_LCNT PHY I2C Fast Speed SCL Low Level Counter

HDMI_RX_JTAG_CONF
Address: Operational Base + offset (0x02ec)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x1	I2C_JTAGZ Select between I2C/JTAG for PHY configuration interface. Must be stable before any JTAG or I2C operation. 1'b0: JTAG interface selected 1'b1: I2C interface selected Note: This field is only used if Controller input iexternalphycontrol=0
3:1	RO	0x0	reserved
0	RW	0x1	JTAG_TRST_N JTAG interface Reset output to PHY 1'b0: Reset enabled 1'b1: Reset disabled Note: This field is only used if Controller input iexternalphycontrol=0 and register field i2c_jtagz=0

HDMI_RX_JTAG_TAP_TCLK
Address: Operational Base + offset (0x02f0)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	JTAG_TCK JTAG interface Clock output to PHY SW must toggle this bit low/high to emulate the actual clock at the JTAG interface. Note: This field is only used if Controller input iexternalphycontrol=0 and register field i2c_jtagz=0

HDMI_RX_JTAG_TAP_IN
Address: Operational Base + offset (0x02f4)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	JTAG_TMS JTAG interface Test Mode Select (TMS) output to PHY. Note: This field is only used if Controller input iexternalphycontrol=0 and register field i2c_jtagz=0
3:1	RO	0x0	reserved
0	RW	0x0	JTAG_TDI JTAG interface Data In output to PHY Note: This field is only used if Controller input iexternalphycontrol=0 and register field i2c_jtagz=0

HDMI_RX_JTAG_TAP_OUT

Address: Operational Base + offset (0x02f8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	JTAG_TDO_EN JTAG interface Data Out Enable from PHY Note: This field is only used if Controller input iexternalphycontrol=0 and register field i2c_jtagz=0
3:1	RO	0x0	reserved
0	RO	0x0	JTAG_TDO JTAG interface Data Out from PHY Note: This field is only used if Controller input iexternalphycontrol=0 and register field i2c_jtagz=0

HDMI_RX_JTAG_ADDR

Address: Operational Base + offset (0x02fc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	JTAG_ADDR JTAG interface 8-bit Address output to PHY Note: This field is only used if Controller input iexternalphycontrol=0 and register field i2c_jtagz=0

HDMI_RX_PDEC_CTRL

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31	RW	0x0	PFIFO_STORE_FILTER_EN Enable individual packet store filters.Disabling this field allows for all packets (includes NULL packets and excludes all Audio packets) to be stored in the Packet FIFO, regardless of the pfifo_store_xxx individual packet store values
30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RW	0x0	PFIFO_STORE_DRM_IF Enable packet FIFO to store Dynamic Range and Mastering InfoFrame packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO (Exists: DWC_HDMI_RX_20==1)
28	RW	0x0	PFIFO_STORE_AMP Enable packet FIFO to store Audio Metadata packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO (Exists: DWC_HDMI_RX_20==1)
27	RW	0x0	PFIFO_STORE_NTSCVBI_IF Enable packet FIFO to store NTSC VBI InfoFrame packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
26	RW	0x0	PFIFO_STORE_MPEGS_IF Enable packet FIFO to store MPEG Source InfoFrame packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
25	RW	0x0	PFIFO_STORE_AUD_IF Enable packet FIFO to store Audio InfoFrame packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
24	RW	0x0	PFIFO_STORE_SPD_IF Enable packet FIFO to store Source Product Descriptor InfoFrame packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
23	RW	0x0	PFIFO_STORE_AVI_IF Enable packet FIFO to store AVI InfoFrame packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO

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Bit	Attr	Reset Value	Description
22	RW	0x0	PFIFO_STORE_VS_IF Enable packet FIFO to store Vendor Specific InfoFrame packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
21	RW	0x0	PFIFO_STORE_GMTP Enable packet FIFO to store Gamut Metadata packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
20	RW	0x0	PFIFO_STORE_ISRC2 Enable packet FIFO to store ISRC2 packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
19	RW	0x0	PFIFO_STORE_ISRC1 Enable packet FIFO to store ISRC1 packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
18	RW	0x0	PFIFO_STORE_ACP Enable packet FIFO to store ACP packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
17	RW	0x0	PFIFO_STORE_GCP Enable packet FIFO to store GCP packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO
16	RW	0x0	PFIFO_STORE_ACR Enable packet FIFO to store ACR packet. When pfifo_store_filter_en is enabled this bit controls packet insertion: 1'b0: Packet not stored in the packet FIFO 1'b1: Packet is stored in the packet FIFO

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Bit	Attr	Reset Value	Description
15	RW	0x0	GCP_GLOBAVMUTE Global AVMUTE enable. Controls propagation of AVMUTE state from Packet Decoder to all downstream modules: 1'b0: Ignore GCP Set_AVMUTE/Clear_AVMUTE and pdec_ctrl.gcpforce_setavmute/pdec_ctrl.gcpforce_clravmute values. The AVMUTE state that outputs the Packet Decoder is always 1'b0 (no mute) and all downstream modules are affected by this (HDCP, Video Processor and Audio Mute). 1'b1: Normal operation. The GCP Set_AVMUTE/Clear_AVMUTE and pdec_ctrl.gcpforce_setavmute/pdec_ctrl.gcpforce_clravmute determine the Packet Decoder AVMUTE state. This value is forwarded to all downstream modules (HDCP, Video Processor and Audio Mute)
14	RW	0x0	GCPFORCE_CLRAVMUTE While set to 1, this bit field forces the clear_avmute to be set continuously at 1. This forces the configuration to overwrite any value coming in GCP packets for clear_avmute. Note: Software must guarantee that gcpforce_clravmute and gcpforce_setavmute not be simultaneously active (1). In such cases, the set action takes precedence over the clear action. In automatic mode, if a GCP packet (or CMP in MHL operation) is received with set_avmute and clear_avmute set simultaneously, the controller gives precedence over set_avmute
13	RW	0x0	GCPFORCE_SETAVMUTE While set to 1, this forces the set_avmute to be set continuously at 1. This forces the configuration to overwrite any value coming in GCP packets for set_avmute. Note: Software must guarantee that gcpforce_clravmute and gcpforce_setavmute not be simultaneously active (1). In such cases, the set action takes precedence over the clear action. In automatic mode, if a GCP packet (or CMP in MHL operation) is received with set_avmute and clear_avmute set simultaneously, the controller gives precedence over set_avmute
12	RW	0x0	GCP_AVMUTE_ALLSPS 1'b0: Accepts set_avmute and clear_avmute indications by looking only to subpacket 0 of GCP packet 1'b1: Set_avmute and clear_avmute are combinational, and all set_avmute (or clear_avmute) values from the four GCP packet subpackets if they are equal
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	WO	0x0	PD_FIFO_FILL_INFO_CLR Clear pd_fifo_fill_min / pd_fifo_fill_max information 1'b0: No operation 1'b1: Clear Notes: ■ Set by software ■ Reset by hardware ■ If this bit is read from, no APB error flag occurs because APB errors only occur at the register level and not the bit level
7	RO	0x0	reserved
6	WO	0x0	PD_FIFO_SKIP Enables software to skip one packet in the FIFO 1'b0: no skip 1'b1: skip the next packet in the FIFO; taken out and deleted from FIFO
5	RW	0x0	PD_FIFO_CLR Clear packet decoder FIFO, a clear ready will be indicated by the pd_fifo_clr_rdy flag 1'b0: No clear 1'b1: Clear FIFO
4	RW	0x0	PD_FIFO_WE Allows the packet decoder to write into the packet FIFO 1'b0: Disabled 1'b1: Enabled
3:1	RO	0x0	reserved
0	RW	0x0	PDEC_BCH_EN BCH error correction enable 1'b0: Disabled 1'b1: eEnabled

HDMI_RX_PDEC_FIFO_CFG

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	PD_FIFO_TH_START Initial start threshold for packet decoder FIFO in words; refers to FIFO memory start
19:10	RW	0x000	PD_FIFO_TH_MAX Maximum packet decoder FIFO fill state threshold words; refers to FIFO memory end
9:0	RW	0x000	PD_FIFO_TH_MIN Minimal packet decoder FIFO fill state threshold in words; refers to FIFO memory start

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HDMI_RX_PDEC_FIFO_STS

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	PD_FIFO_FILL_MAX Long-term maximum detected FIFO fill state
15:0	RO	0x0000	PD_FIFO_FILL_MIN Long-term minimum detected FIFO fill state

HDMI_RX_PDEC_FIFO_DATA

Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PD_FIFO_DATA Packet byte data software interface to packet decoder FIFO Note: ■ Full packet header visible after the FIFO contains at least one entry (pd_fifo_new = 1 for the first time) ■ Auto-increment per register access ■ Eight subsequent accesses required to read an entire packet

HDMI_RX_PDEC_AUDIODET_CTRL

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:9	RW	0x00	AUDIODET_THRESHOLD Number of consecutive packets to determine the type of audio the HDMI RX is receiving. After an Audio Format has been determined, a hysteresis mechanism ensures that the Audio Format will only change after audiodet_threshold consecutive Audio Packets with the same format are received. Note: Writing either a 0 or 1 performs the same function (the number of packets needed to signal the audio is just one). This field is not intended to be modified along the operation of the HDMI RX core. If modified to a higher number then the initially configured one the threshold counter will count the difference between the previous configured value and the new configured value and trigger a new audio change interrupt. If modified to a lower number then the initial configured one there will be no new audio change interrupt
8:0	RO	0x0	reserved

HDMI_RX_PDEC_DBG_ACP

Address: Operational Base + offset (0x031c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	ACP_FREQ_CNT Debug, not connected
7:0	RO	0x0	reserved

HDMI_RX_PDEC_DBG_ERR_CORR

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	ERROR_CODEINS_EN Error code replacement 1'b0: Disable 1'b1: Enable code replacement for non corrected BCH errors
7:0	RW	0x00	ERROR_INS_CODE MSBs audio sample code for replacement in case of an non corrected error in an audio packet

HDMI_RX_PDEC_FIFO_STS1

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	PD_FIFO_FILL_STATE Current Packet FIFO fill state

HDMI_RX_PDEC_ACRM_CTRL

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:2	RW	0x0	DELTACTS_IRQTRIG Delta CTS trigger level for IRQ cts_change: 3'b0: >=1 3'b1: >= 2 3'b2: >= 4 3'b3: >= 8 3'b4: >= 16 3'b5: >= 32 3'b6: Reserved 3'b7: Reserved
1:0	RW	0x0	CTS_N_MEAS_MODE 2'b0: Reset all measurements 2'b1: Store maximum and minimum CTS values 2'b2: Store maximum and minimum N values 2'b3: Reserved

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HDMI_RX_PDEC_ACRM_MAX

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RO	0x00000	CTS_N_MAX Maximum CTS div N value as decoded from HDMI data stream

HDMI_RX_PDEC_ACRM_MIN

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RO	0x00000	CTS_N_MIN Minimum CTS div N value as decoded from HDMI data stream

HDMI_RX_PDEC_ERR_FILTER

Address: Operational Base + offset (0x033c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	BCHSP_DRM_ERR_FILTER BCH error filter for sub-packet of Dynamic Range and Mastering InfoFrame packets enable. (Exists: DWC_HDMI_RX_20==1)
10	RW	0x0	BCHSP_NTSCVBI_ERR_FILTER BCH error filter for sub-packet of NTSC VBI packets enable. (Exists: DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
9	RW	0x0	BCHSP_AMP_ERR_FILTER BCH error filter for sub-packet of Audio Metadata packets enable. (Exists: DWC_HDMI_RX_20==1)
8	RW	0x0	BCHSP_ISRC_ERR_FILTER BCH error filter for sub-packet of ISRC packets enable
7	RW	0x0	BCHSP_GMD_ERR_FILTER BCH error filter for sub-packet of GMD packets enable
6	RW	0x0	BCHSP_AIF_ERR_FILTER BCH error filter for sub-packet of AIF packets enable
5	RW	0x0	BCHSP_AVI_ERR_FILTER BCH error filter for sub-packet of AVI packets enable
4	RW	0x0	BCHSP_VSI_ERR_FILTER BCH error filter for sub-packet of VSI packets enable
3	RW	0x0	BCHSP_GCP_ERR_FILTER BCH error filter for sub-packet of GCP packets enable
2	RW	0x0	BCHSP_ACRP_ERR_FILTER BCH error filter for sub-packet of ACRP packets enable
1	RW	0x0	BCHPH_ERR_FILTER BCH error filter for packet header enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	CHECKSUM_ERR_FILTER Checksum error filter enable

HDMI_RX_PDEC_ASP_CTRL

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	AUTO_VMUTE Automatic mute of all video channels when Set_AVMUTE/Clear_AVMUTE is send 1'b0: Disable 1'b1: Enable
5:2	RW	0x0	AUTO_SPFLAT_MUTE Automatic mute of audio subpacket X when sample_flat.spX=1 and sample_present.spX=1 is decoded 1'b0: Disable 1'b1: Enable Note: Bit X corresponds to audio subpacket X. Currently, the sample_flat bits have no functional use
1:0	RO	0x0	reserved

HDMI_RX_PDEC_ASP_ERR

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ERRORS_FRAME_GAP Frame gap between two consecutive errors (all Data Island packets, audio or not) as detected by the BCH error detection function.Once this field reaches 0xFFFF it becomes saturated
15:0	RW	0x0000	ERRORS_PER_FRAME Number of ASP Subpacket errors per frame as detected by the BCH error detection function for Data Island packets. Once this field reaches 0xFFFF it becomes saturated

HDMI_RX_PDEC_STS

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31	RO	0x0	DRM_CKS_CHG Checksum from Dynamic Range and Mastering InfoFrame changed its value 1'b0: No change 1'b1: Value changed (Exists: DWC_HDMI_RX_20==1)

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Bit	Attr	Reset Value	Description
30	RO	0x0	DRM_RCV New Dynamic Range and Mastering InfoFrame packet received 1'b0: No change 1'b1: Packet received (Exists: DWC_HDMI_RX_20==1)
29	RO	0x0	NTSCVBI_CKS_CHG Checksum from NTSC VBI changed its value 1'b0: No change 1'b1: Value changed (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
28	RW	0x0	DVIDET DVI detection status 1'b0: No DVI mode detected 1'b1: DVI mode detected
27	RW	0x0	VSI_CKS_CHG Checksum from VSI changed its value 1'b0: No change 1'b1: Value changed
26	RO	0x0	GMD_CKS_CHG GMD packet (gamut meta data) checksum changed value (register field pdec_gmd_pb:gmd_checksum). Only applicable for Transmission Profiles P1, P2 or P3. 1'b0: No change 1'b1: Value changed
25	RO	0x0	AIF_CKS_CHG Checksum from AIF packet changed its value 1'b0: No change 1'b1: Value changed
24	RO	0x0	AVI_CKS_CHG Checksum from AVI packet changed its value. 1'b0: No change 1'b1: Value changed
23	RO	0x0	ACR_N_CHG N value from ACR packet changed its value. 1'b0: No change 1'b1: Value changed
22	RW	0x0	ACR_CTS_CHG CTS value from ACR packet changed its value. 1'b0: No change 1'b1: Value changed

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Bit	Attr	Reset Value	Description
21	RO	0x0	GCP_AV_MUTE_CHG The gcp_av_mute_chg status and interrupt are triggered in the following mute states in the audio mute FSM: ■ ST_MUTE_FIFO ■ ST_MUTE_ALL ■ ST_MUTE_SEPARAT
20	RO	0x0	GMD_RCV New GMD packet received 1'b0: No change 1'b1: Packet received
19	RO	0x0	AIF_RCV New AIF packet received. 1'b0: No change 1'b1: Packet received
18	RO	0x0	AVI_RCV New AVI packet received. 1'b0: No change 1'b1: Packet received
17	RO	0x0	ACR_RCV New ACR packet received 1'b0: No change 1'b1: Packet received
16	RW	0x0	GCP_RCV New GCP packet received 1'b0: No change 1'b1: Packet received
15	RO	0x0	VSI_RCV New VSI packet received 1'b0: No change 1'b1: Packet received
14	RW	0x0	AMP_RCV New Audio Metadata packet received 1'b0: No change 1'b1: Packet received (Exists: DWC_HDMI_RX_20==1)
13	RW	0x0	NTSCVBI_RCV New NTSC VBI packet received 1'b0: No change 1'b1: Packet received (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))

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Bit	Attr	Reset Value	Description
12	RO	0x0	OBA_LAYOUT This bit holds information of One Bit Audio (OBA) packet layout indication. Note: This bit will only be updated on the above described audio type. Upon audio type change (to any but the above described type), this bit will retain its value from previously received OBA packet layout
11	RO	0x0	AUDS_LAYOUT This bit holds information of Audio Sample (AUDS) packet layout indication. Note: This bit will only be updated on the above described audio type. Upon audio type change (to any but the above described type), this bit will retain its value from previously received AUDS packet layout
10:9	RO	0x0	reserved
8	RO	0x0	PD_FIFO_NEW_ENTRY FIFO read pointer position 1'b0: FIFO read pointer is positioned on a new packet body, or when packet FIFO is empty 1'b1: FIFO read pointer is positioned on a new packet header
7:5	RO	0x0	reserved
4	RO	0x0	PD_FIFO_OVERFL FIFO overflow indication, too less data picked up then delivered by packets 1'b0: Inactive 1'b1: Active
3	RO	0x0	PD_FIFO_UNDERFL FIFO underflow indication, more data picked up then delivered by packets 1'b0: OK 1'b1: Underflow
2	RO	0x0	PD_FIFO_TH_START_PASS FIFO start threshold passed indication 1'b0: not passed 1'b1: passed Note: When pd_fifo_th_start is triggered, pd_fifo_fill_max_s and pd_fifo_fill_min_s are cleared to have valid fill states available afterwards, and the interrupt flag afif_ths_pass is set
1	RO	0x0	PD_FIFO_TH_MAX_PASS Data content higher than maximum threshold. 1'b0: OK 1'b1: Higher than threshold Note: The maximum threshold value is calculated as a positive offset from the END of the FIFO down into the memory locations

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Bit	Attr	Reset Value	Description
0	RO	0x0	PD_FIFO_TH_MIN_PASS Data content lower than minimum threshold 1'b0: OK 1'b1: Lower than threshold Note: The maximum threshold value is calculated as a positive offset from the start of the FIFO up to the memory locations

HDMI_RX_PDEC_AUD_STS

Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RO	0x0	MAS_RCV MultiStream Audio Sample packet received (Exists: DWC_HDMI_RX_20==1)
4	RO	0x0	OBM_RCV One Bit MultiStream Audio packet received (Exists: DWC_HDMI_RX_20==1)
3	RO	0x0	HBR_RCV High-Bitrate Audio Stream packet received
2	RO	0x0	DST_RCV DST Audio packet received
1	RO	0x0	OBA_RCV One Bit Audio Sample packet received
0	RO	0x0	AUDS_RCV Audio Samples packet received

HDMI_RX_PDEC_VSI_PAYLOAD0

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	VSI_VSPAYLOAD_3 Packet VSI Vendor Specific Payload byte 3
23:16	RO	0x00	VSI_VSPAYLOAD_2 Packet VSI Vendor Specific Payload byte 2
15:8	RO	0x00	VSI_VSPAYLOAD_1 Packet VSI Vendor Specific Payload byte 1
7:0	RW	0x00	VSI_VSPAYLOAD_0 Packet VSI Vendor Specific Payload byte 0

HDMI_RX_PDEC_VSI_PAYLOAD1

Address: Operational Base + offset (0x036c)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	VSI_VSPAYLOAD_7 Packet VSI Vendor Specific Payload byte 7
23:16	RO	0x00	VSI_VSPAYLOAD_6 Packet VSI Vendor Specific Payload byte 6
15:8	RO	0x00	VSI_VSPAYLOAD_5 Packet VSI Vendor Specific Payload byte 5
7:0	RW	0x00	VSI_VSPAYLOAD_4 Packet VSI Vendor Specific Payload byte4

HDMI_RX_PDEC_VSI_PAYLOAD2

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	VSI_VSPAYLOAD_11 Packet VSI Vendor Specific Payload byte 11
23:16	RO	0x00	VSI_VSPAYLOAD_10 Packet VSI Vendor Specific Payload byte 10
15:8	RO	0x00	VSI_VSPAYLOAD_9 Packet VSI Vendor Specific Payload byte 9
7:0	RW	0x00	VSI_VSPAYLOAD_8 Packet VSI Vendor Specific Payload byte 8

HDMI_RX_PDEC_VSI_PAYLOAD3

Address: Operational Base + offset (0x0374)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	VSI_VSPAYLOAD_15 Packet VSI Vendor Specific Payload byte 15
23:16	RO	0x00	VSI_VSPAYLOAD_14 Packet VSI Vendor Specific Payload byte 14
15:8	RO	0x00	VSI_VSPAYLOAD_13 Packet VSI Vendor Specific Payload byte 13
7:0	RW	0x00	VSI_VSPAYLOAD_12 Packet VSI Vendor Specific Payload byte 12

HDMI_RX_PDEC_VSI_PAYLOAD4

Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	VSI_VSPAYLOAD_19 Packet VSI Vendor Specific Payload byte 19
23:16	RO	0x00	VSI_VSPAYLOAD_18 Packet VSI Vendor Specific Payload byte 18
15:8	RO	0x00	VSI_VSPAYLOAD_17 Packet VSI Vendor Specific Payload byte 17
7:0	RW	0x00	VSI_VSPAYLOAD_16 Packet VSI Vendor Specific Payload byte 16

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HDMI_RX_PDEC_VSI_PAYLOAD5

Address: Operational Base + offset (0x037c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	VSI_VSPAYLOAD_23 Packet VSI Vendor Specific Payload byte 23
23:16	RO	0x00	VSI_VSPAYLOAD_22 Packet VSI Vendor Specific Payload byte 22
15:8	RO	0x00	VSI_VSPAYLOAD_21 Packet VSI Vendor Specific Payload byte 21
7:0	RW	0x00	VSI_VSPAYLOAD_20 Packet VSI Vendor Specific Payload byte 20

HDMI_RX_PDEC_GCP_AVMUTE

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	PKTDEC_DEFAULT_PHASE Default_Phase, indicates whether the transmitter sends deep color pixel groups using the default phase rules 1’b0: Not used 1’b1: Used
11:8	RO	0x0	PKTDEC_GCP_PP PP3 PP2 PP1 PP0, pixel packing phase for deep color mode support; phase 0 is never indicated because no mode is going to end at this phase. 4'b0: Phase 4 (10P4) 4’b1: Phase 1 (10P1, 12P1, 16P1) 4’b2: Phase 2 (10P2, 12P2) 4’b3: Phase 3 (10P3) Others: Reserved
7:4	RO	0x0	PKTDEC_GCP_CD CD3 CD2 CD1 CD0, color depth for deep color mode support. 4’b0: Color depth not indicated 4’b1: Reserved 4’b2: Reserved 4’b3: Reserved 4’b4: 24 bits per pixel 4’b5: 30 bits per pixel 4’b6: 36 bits per pixel 4’b7: 48 bits per pixel Others: Reserved Note: According to the HDMI 1.4b Specification, this value must also be used in Deep Color mode to transmit a GCP, indicating only non-Deep Color information (for example, AVMUTE)

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Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1	RO	0x0	PKTDEC_SETAVMUTE Set_AVMUTE, set audio/video mute. 1'b0: Disabled 1'b1: Enable
0	RW	0x0	PKTDEC_CLRAVMUTE Clear_AVMUTE, release audio/video mute 1'b0: Disable 1'b1: Enable

HDMI_RX_PDEC_ACR_CTS

Address: Operational Base + offset (0x0390)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RO	0x00000	CTS_DECODED CTS19..CTS0, cycle time stamp to re-generate the audio clock from the TMDS clock

HDMI_RX_PDEC_ACR_N

Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RO	0x00000	N_DECODED N19..N0, multiplier value N to re-generate the audio clock from the TMDS clock

HDMI_RX_PDEC_AVI_HB

Address: Operational Base + offset (0x03a0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	QUANT_RANGE HDMI 1.4b specification AVI quantization range field
29:28	RO	0x0	CONTENT_TYPE HDMI 1.4b specification AVI content type field

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Bit	Attr	Reset Value	Description
27:24	RO	0x0	PIX_REP_FACTOR PR3 PR2 PR1 PR0, pixel repetition factor 4’b0: No repetition, pixel sent once 4’b1: Pixel sent 2 times 4’b2: Pixel sent 3 times 4’b3: Pixel sent 4 times 4’b4: Pixel sent 5 times 4’b5: Pixel sent 6 times 4’b6: Pixel sent 7 times 4’b7: Pixel sent 8 times 4’b8: Pixel sent 9 times 4'd9: Pixel sent 10 times 4’b10-15: Reserved
23:16	RO	0x00	AVI_CHECKSUM Used to check whether the frame content is updated with respect to the last transmitted AVI Infoframe
15:13	RO	0x0	reserved
12:8	RO	0x00	AVI_LENGTH Infoframe length. The typical value is 0x0D
7:0	RW	0x00	AVI_VERSION Infoframe version number. The typical value is 0x02

HDMI_RX_PDEC_AVI_PB

Address: Operational Base + offset (0x03a4)

Bit	Attr	Reset Value	Description
31	RO	0x0	VID_IDENT_CODE_VIC7 VIC7 of video mode identification code. For more information, see the CEA861-F Specification. (Exists: DWC_HDMI_RX_20==1)
30:24	RO	0x00	VID_IDENT_CODE VIC6 VIC5 VIC 5 VIC4 VIC3 VIC2 VIC1 VIC0, video mode identification code. For more information, see the CEA861-F Specification
23	RO	0x0	IT_CONTENT ITC0, IT content. 1’b0: No data 1’b1: IT content
22:20	RO	0x0	EXT_COLORIMETRY EC2 EC1 EC0, extended colorimetry 3’b0: xvYCC ITU601 3’b1: xvYCC ITU709 3’b2-7: Reserved

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Bit	Attr	Reset Value	Description
19:18	RO	0x0	RGB_QUANT_RANGE Q1 Q0, RGB quantization range. 2’b0: Default (depends on video format) 2’b1: Limited range 2’b2: Full range 2’b3: Reserved
17:16	RO	0x0	NON_UNIF_SCALE SC1 SC0, non-uniform scaling information 1’b0: Unknown 2'1: H_scaled, picture horizontally scaled 2’b2: V_scaled, picture vertically scaled 2’b3: HV_scaled, picture horizontally and vertically scaled
15:14	RO	0x0	COLORIMETRY C1 C0, colorimetry information 2’b0: No data 2’b1: SMPTE 170M, TU601 2’b2: ITU 709 2’b3: Extended colorimetry information valid (colorimetry indicated in EC2 EC1 EC0)
13:12	RO	0x0	PIC_ASPECT_RAT M1 M0, picture aspect ratio 2’b0: No_data 2’b1: 4:3 2’b2: 16:9 2’b3: Future
11:8	RO	0x0	ACT_ASPECT_RAT R3 R2 R1 R0, active format aspect ratio. 4’b0-7: per DVB AFD active_format field 4’b8: same as picture aspect ratio 4'd9: 4:3 center 4’b10: 16:9 center 4’b11: 14:9 center 4’b11-15 = per DVB AFD active_format field
7	RO	0x0	VIDEO_FORMAT_Y2 Y2, video format (Exists: DWC_HDMI_RX_20==1)
6:5	RO	0x0	VIDEO_FORMAT Y1 Y0, video format 2’b0: RGB 2’b1: YCbCr 4:2:2 2’b2: YCbCr 4:4:4 2’b3: Future

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Bit	Attr	Reset Value	Description
4	RO	0x0	ACT_INFO_PRESENT A0, active format information present. 1'b0: No data 1'b1: Active format R3 R2 R1 R0 information valid
3:2	RO	0x0	BAR_INFO_VALID B1 B0, bar valid information. 2'b0: Not_valid 2'b1: Vertical bar info valid 2'b2: Horizontal bar info valid 2'b3: Vertical and horizontal bar info valid
1:0	RO	0x0	SCAN_INFO S1 S0, scan information from packet extraction 2'b0: No_data 2'b1: Over-scanned, television type 2'b2: Under-scanned, computer type 2'b3: Future

HDMI_RX_PDEC_AVI_TBB

Address: Operational Base + offset (0x03a8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LIN_ST_BOT_BAR Line number to start of bottom bar
15:0	RW	0x0000	LIN_END_TOP_BAR Line numbers to end of top bar

HDMI_RX_PDEC_AVI_LRB

Address: Operational Base + offset (0x03ac)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	PIX_ST_RIG_BAR Pixel numbers of end of left bar
15:0	RO	0x0000	PIX_END_LEF_BAR Pixel numbers of start right bar

HDMI_RX_PDEC_AIF_CTRL

Address: Operational Base + offset (0x03c0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	FC_LFE_EXCHG Exchange FC and LFE channel (speaker allocation) 1'b0: Disable 1'b1: Enable
17:0	RO	0x0	reserved

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HDMI_RX_PDEC_AIF_HB

Address: Operational Base + offset (0x03c4)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RO	0x00	AIF_CHECKSUM AIF checksum information
15:13	RO	0x0	reserved
12:8	RO	0x00	AIF_LENGTH Infoframe length. The typical value is 0x0A
7:0	RW	0x00	AIF_VERSION Infoframe version. The typical value is 0x01

HDMI_RX_PDEC_AIF_PB0

Address: Operational Base + offset (0x03c8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CH_SPEAK_ALLOC CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0, channel speaker allocation. For more information, see the CEA861-D Specification
23:16	RO	0x00	AIF_DATA_BYTE_3 Content depends on audio infoFrame data byte 3 (refer to the HDMI specification)
15:13	RO	0x0	reserved
12:10	RO	0x0	SAMPLE_FREQ SF2 SF1 SF0, sample frequency information. 3'b0: refer to stream header 3'b1: 32 kHz 3'b2: 44.1 kHz 3'b3: 48 kHz 3'b4: 88.2 kHz 3'b5: 96 kHz 3'b6: 176.4 kHz 3'b7: 192 kHz
9:8	RO	0x0	SAMPLE_SIZE SS1 SS0, sample size information 2'b0: refer to stream header 2'b1: 16 bit 2'b2: 20 bit 2'b3: 24 bit

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	CODING_TYPE CT3 CT2 CT1 CT0, coding type information 4’b0: refer to stream header 4’b1: IEC60958 PCM 4’b2: AC-3 4’b3: MPEG1 (Layers 1 and 2) 4’b4: MP3 (MPEG1 Layer 3) 4’b5: MPEG2 (multichannel) 4’b6: AAC 4’b7: reserved 4’b8: ATRAC 4'd9: One Bit Audio 4’b10: reserved 4’b11: reserved 4’b12: MAT (MLP) 4’b13: DST 4’b14: WMA Pro 4’b15: reserved
3	RO	0x0	reserved
2:0	RO	0x0	CHANNEL_COUNT CC2 CC1 CC0, audio channel count information 3’b0: Refer to stream header 3’b1: 2ch 3’b2: 3ch 3’b3: 4ch 3’b4: 5ch 3’b5: 6ch 3’b6: 7ch 3’b7: 8ch

HDMI_RX_PDEC_AIF_PB1

Address: Operational Base + offset (0x03cc)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:8	RO	0x0	LFE_PLAYBACK_LEVEL See HDMI 1.4b specification AIF LFE playback level field
7	RO	0x0	DWNMIX_INHIBIT DM_INH, used together with DVD-audio only 1’b0: Permitted or no information about any assertion of this 1’b1: Prohibited

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Bit	Attr	Reset Value	Description
6:3	RO	0x0	LEVEL_SHIFT_VAL LSV3 LSV1 LSV0, audio level shift value 4’b0: 0 dB 4’b1: 1 dB 4’b2: 2 dB 4’b3: 3 dB 4’b4: 4 dB 4’b5: 5 dB 4’b6: 6 dB 4’b7: 7 dB 4’b8: 8 dB 4'd9: 9 dB 4’b10: 10 dB 4’b11: 11 dB 4’b12: 12 dB 4’b13: 13 dB 4’b14: 14 dB 4’b15: 15 dB
2:0	RO	0x0	reserved

HDMI_RX_PDEC_GMD_HB

Address: Operational Base + offset (0x03d0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RO	0x0	GMD_NO_CMT_GBD Current gbd 1’b0: Gamut metadata available for the currently transmitted video 1’b1: No gamut metadata available for the currently transmitted video
14	RO	0x0	reserved
13:12	RO	0x0	GMD_PACKET_SEQ Packet sequence 2’b0: Intermediate packet in sequence 2’b1: First packet in sequence 2’b2: Last packet in sequence 2’b3: Only one packet in sequence

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Bit	Attr	Reset Value	Description
11:8	RO	0x0	GMD_CUR_GM_SEQ_NUM Indicates the gamut number of the currently transmitted video stream Note: All gamut metadata packets transmitted within the same video field have the same current gamut sequence number even if the affected gamut sequence number varies among the packets. Note: All gamut metadata packets transmitted within the same video field shall have the same current gamut sequence number even if the affected gamut sequence number varies among the packets
7	RO	0x0	GMD_NEXT_FIELD Next field effective, indicates that the GBD carried in this packet is effective on the next video field 1'b0: Not effective 1'b1: Effective Note: The affected gamut sequence number for this packet is equal to the current gamut sequence number for the next field. Set the next field indication even if the GBD is already effective
6:4	RO	0x0	GMD_GBD_PROFILE Transmission profile number. 3'b0: P0 3'b1: P1 3'b2: P2 3'b3: P3 Others: Reserved
3	RO	0x0	reserved
2:0	RO	0x0	GMD_AFF_GAMUT_SEQ Affected gamut sequence number, indicates which video fields are relevant for this metadata

HDMI_RX_PDEC_GMD_PB

Address: Operational Base + offset (0x03d4)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RO	0x00	GMD_CHECKSUM Checksum of every byte transmitted in the packet bytes pb3 - pb27 according to GBD length information for profile P1 and higher
15:0	RO	0x0000	GMD_GBD_LENGTH Total length in bytes of gamut metadata information (pb3 - pb27) not including gbd_length (pb0 - pb1) and checksum (pb2) for profile P1 and higher

HDMI_RX_PDEC_VSI_ST0

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Address: Operational Base + offset (0x03e0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	VSI_CHECKSUM Checksum information
23:0	RO	0x000000	IEEE_REG_ID IEEE ID code

HDMI_RX_PDEC_VSI_ST1

Address: Operational Base + offset (0x03e4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RO	0x0	H3D_META_PRESENT Refer to the HDMI 1.4b specification (h3d_meta_present). Notes: ■ According to the HDMI specification, both hdmi_vic and 3d_structure share the same byte in the VSI packet. The software must correctly interpret the data in these registers based on the required functionality. ■ For configurations supporting HDMI 2.0, MHL, or both, the data on this register is not valid and is not used for software decisions. Instead, the software uses the information in the pdec_vsi_payload registers. (Exists: DWC_HDMI_RX_20==0)
23:20	RO	0x0	H3D_EXT_DATA Refer to the HDMI 1.4b specification (h3d_ext_data). Notes: ■ According to the HDMI specification, both hdmi_vic and 3d_structure share the same byte in the VSI packet. The software must correctly interpret the data in these registers based on the required functionality. ■ For configurations supporting HDMI 2.0, MHL, or both, the data on this register is not valid and is not used for software decisions. Instead, the software uses the information in the pdec_vsi_payload registers. (Exists: DWC_HDMI_RX_20==0)

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	H3D_STRUCTURE Refer to the HDMI 1.4b specification (h3d_structure). Notes: ■ According to the HDMI specification, both hdmi_vic and 3d_structure share the same byte in the VSI packet. The software must correctly interpret the data in these registers based on the required functionality. ■ For configurations supporting HDMI 2.0, MHL, or both, the data on this register is not valid and is not used for software decisions. Instead, the software uses the information in the pdec_vsi_payload registers. (Exists: DWC_HDMI_RX_20==0)
15:8	RO	0x00	HDMI_VIC Refer to the HDMI 1.4b specification (hdmi_vic). Notes: ■ According to the HDMI specification, both hdmi_vic and 3d_structure share the same byte in the VSI packet. The software must correctly interpret the data in these registers based on the required functionality. ■ For configurations supporting HDMI 2.0, MHL, or both, the data on this register is not valid and is not used for software decisions. Instead, the software uses the information in the pdec_vsi_payload registers. (Exists: DWC_HDMI_RX_20==0)
7:5	RO	0x0	HDMI_VIDEO_FORMAT Refer to the HDMI 1.4b specification (hdmi_video_format). Notes: ■ According to the HDMI specification, both hdmi_vic and 3d_structure share the same byte in the VSI packet. The software must correctly interpret the data in these registers based on the required functionality. ■ For configurations supporting HDMI 2.0, MHL, or both, the data on this register is not valid and is not used for software decisions. Instead, the software uses the information in the pdec_vsi_payload registers. (Exists: DWC_HDMI_RX_20==0)
4:0	RO	0x00	LENGTH VSI length

HDMI_RX_PDEC_VSI_PB0

Address: Operational Base + offset (0x03e8)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	H3D_METADATA_3 Refer to the HDMI 1.4b specification (h3d_metadata_3). (Exists: DWC_HDMI_RX_20==0)
23:16	RO	0x00	H3D_METADATA_2 Refer to the HDMI 1.4b specification (h3d_metadata_2). (Exists: DWC_HDMI_RX_20==0)
15:8	RO	0x00	H3D_METADATA_1 Refer to the HDMI 1.4b specification (h3d_metadata_1). (Exists: DWC_HDMI_RX_20==0)
7:3	RO	0x00	H3D_METADATA_LENGTH Refer to the HDMI 1.4b specification (h3d_metadata_length). (Exists: DWC_HDMI_RX_20==0)
2:0	RO	0x0	H3D_METADATA_TYPE Refer to the HDMI 1.4b specification (h3d_metadata_type). (Exists: DWC_HDMI_RX_20==0)

HDMI_RX_PDEC_VSI_PB1

Address: Operational Base + offset (0x03ec)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	H3D_METADATA_7 Refer to the HDMI 1.4b specification (h3d_metadata_7. (Exists: DWC_HDMI_RX_20==0)
23:16	RO	0x00	H3D_METADATA_6 Refer to the HDMI 1.4b specification (h3d_metadata_6). (Exists: DWC_HDMI_RX_20==0)
15:8	RO	0x00	H3D_METADATA_5 Refer to the HDMI 1.4b specification (h3d_metadata_5). (Exists: DWC_HDMI_RX_20==0)
7:0	RO	0x00	H3D_METADATA_4 Refer to the HDMI 1.4b specification (h3d_metadata_4). (Exists: DWC_HDMI_RX_20==0)

HDMI_RX_PDEC_VSI_PB2

Address: Operational Base + offset (0x03f0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	H3D_METADATA_15 Refer to the HDMI 1.4b specification (h3d_metadata_15). (Exists: DWC_HDMI_RX_20==0)
23:16	RO	0x00	H3D_METADATA_14 Refer to the HDMI 1.4b specification (h3d_metadata_14). (Exists: DWC_HDMI_RX_20==0)
15:8	RO	0x00	H3D_METADATA_13 Refer to the HDMI 1.4b specification (h3d_metadata_13). (Exists: DWC_HDMI_RX_20==0)

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	H3D_METADATA_12 Refer to the HDMI 1.4b specification (h3d_metadata_12). (Exists: DWC_HDMI_RX_20==0)

HDMI_RX_PDEC_VSI_PB3

Address: Operational Base + offset (0x03f4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	H3D_METADATA_11 Refer to the HDMI 1.4b specification (h3d_metadata_11). (Exists: DWC_HDMI_RX_20==0)
23:16	RO	0x00	H3D_METADATA_10 Refer to the HDMI 1.4b specification (h3d_metadata_10). (Exists: DWC_HDMI_RX_20==0)
15:8	RO	0x00	H3D_METADATA_9 Refer to the HDMI 1.4b specification (h3d_metadata_9). (Exists: DWC_HDMI_RX_20==0)
7:0	RO	0x00	H3D_METADATA_8 Refer to the HDMI 1.4b specification (h3d_metadata_8). (Exists: DWC_HDMI_RX_20==0)

HDMI_RX_PDEC_VSI_PB4

Address: Operational Base + offset (0x03f8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	H3D_METADATA_19 Refer to the HDMI 1.4b specification (h3d_metadata_19). (Exists: DWC_HDMI_RX_20==0)
23:16	RO	0x00	H3D_METADATA_18 Refer to the HDMI 1.4b specification (h3d_metadata_18). (Exists: DWC_HDMI_RX_20==0)
15:8	RO	0x00	H3D_METADATA_17 Refer to the HDMI 1.4b specification (h3d_metadata_17). (Exists: DWC_HDMI_RX_20==0)
7:0	RO	0x00	H3D_METADATA_16 Refer to the HDMI 1.4b specification (h3d_metadata_16). (Exists: DWC_HDMI_RX_20==0)

HDMI_RX_PDEC_VSI_PB5

Address: Operational Base + offset (0x03fc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	H3D_METADATA_20 Refer to the HDMI 1.4b specification (h3d_metadata_20). (Exists: DWC_HDMI_RX_20==0)

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HDMI_RX_CEAVID_CONFIG

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31	RW	0x0	CEAVID_RS Synchronous clear for CEA video interface, active high
30:22	RO	0x0	reserved
21	RW	0x0	CEAVID_YCC422_IPIMAP CEA YCC 422 IPI Mapping. 1'b0: Normal Mapping 1'b1: IPI Mapping
20	RW	0x0	CEAVID_YCC420_IPIMAP CEA YCC 420 IPI Mapping. 1'b0: Normal Mapping 1'b1: IPI Mapping (Exists: DWC_HDMI_RX_20==1)
19:18	RO	0x0	reserved
17	RW	0x0	CEAVID_AUTO_REALIGN CEA video auto realignment mechanism. 1’b0: The CEA video interface will perform initial alignment and only realign upon ceavid_rst or ceavid_realign_th realignment conditions. 1’b1: The CEA video interface is continuously realigning at every vertical blank region. (If the input video control signals (vertical sync, horizontal sync and data enable) are stable, no changes are caused in the CEA output signals. If the input video control signals (vertical sync, horizontal sync and data enable) change,the realignment mechanism makes the CEA output signals to stabilize upon stable values on the input video control signals.)
16	RW	0x0	CEAVID_VS_FILTER CEA vertical sync (VS) format correction filter for CEA automatic operation mode counters. Only valid for automatic mode. 1’b0: No filtering is applied to VS. 1’b1: VS format filter active. Inside the Mode Detection module a VS format correction filter will be activated and the reformatted VS will be forwarded to the CEA video counters
15	RO	0x0	reserved
14	RW	0x0	CEAVID_VIDID Video identification mode. Only valid for automatic mode and non-DVI 1’b0: Video mode identification through the VIC code 1’b1: Video mode identification uses interlaced indication and threshold counters has the same values (threshold value is 3)

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Bit	Attr	Reset Value	Description
13:10	RW	0x0	CEAVID_REALIGN_TH Set the re-alignment threshold of the back porch (VBack) variations tolerance. Only valid when ceavid_auto_realign is disabled
9:6	RW	0x0	CEAVID_IGNFRAME Prevents unstable initial video to be displayed on the CEA video output interface. The frame counter starts after HDMI reset, HDMI synchronous enable and ceavid_rst have been cleared. By default, three frames are always ignored. The value configured in these fields add to these three initially ignored frames
5	RW	0x0	CEAVID_VBOS Vblank oscillation in manual mode Note: For VIC39, this bit must be zero (0) because this interlaced mode has no vblank oscillation
4	RW	0x0	CEAVID_ILACE Interlace video output in manual mode 1'b0: Progressive 1'b1: Interlaced
3	RW	0x0	CEAVID_VPOL VS output polarity in manual mode 1'b0: Active-low 1'b1: Active-high
2	RW	0x0	CEAVID_HPOL HS output polarity in manual mode 1'b0: Active-low 1'b1: Active-high
1	RW	0x0	CEAVID_MAN Manual operation mode. Frame size, HS, VS and DE values and polarity will be taken from register bank
0	RO	0x0	reserved

HDMI_RX_CEAVID_3DCONFIG

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:1	RW	0x0	CEAVID_3DSTRUCTURE 3D_Structure/MHL_3D_FMT_TYPE when in manual mode. If MHL mode is disabled and manual mode enabled, this register forces HDMI 3D_Structure to the configured value: 4’b0: Frame Packing 4’b1: Field alternative 4’b2: Line alternative 4’b3: Side-by-Side (Full) 4’b4: L + depth 4’b5: L + depth + graphics + graphics-depth 4’b6: Top-and-Bottom 4’b7: Reserved 4’b8: Side-by-Side (Half) 4'd9-15: Reserved If MHL mode is enabled and manual mode enabled, this register forces MHL_3D_FMT_TYPE using its equivalent HDMI 3D_Structure values: 4’b0: Frame Sequential - equivalent to HDMI Frame Packing 4’b1-5: Reserved 4’b6: Top-Bottom - equivalent to HDMI Top-and-Bottom 4’b7: Reserved 4’b8: Left-Right - equivalent to HDMI Side-by-Side (Half) 4'd9-15: Reserved Note: Configuring this register with values described as reserved for MHL operation may lead to incorrect controller behavior
0	RW	0x0	CEAVID_3DEN Enable 3D video when in manual mode

HDMI_RX_CEAVID_HCONFIG_LO

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CEAVID_HBLANK Manual mode hblank
15:0	RW	0x0000	CEAVID_HACTIVE Manual mode hactive

HDMI_RX_CEAVID_HCONFIG_HI

Address: Operational Base + offset (0x040c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CEAVID_HFRONT Manual mode hfront
15:0	RW	0x0000	CEAVID_HSYNC Manual mode hsync

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HDMI_RX_CEAVID_VCONFIG_LO
Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CEAVID_VBLANK Manual mode vblank
15:0	RW	0x0000	CEAVID_VACTIVE Manual mode vactive

HDMI_RX_CEAVID_VCONFIG_HI
Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CEAVID_VFRONT Manual mode vfront
15:0	RW	0x0000	CEAVID_VSYNC Manual mode vsync

HDMI_RX_CEAVID_STATUS
Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	CEAVID_ALIGN_STS Sticky bit. Indicates that a re-aligned occurred. Active high. This bit is cleared on read operation. 1'b0: No 1'b1: Video re-align occurred
0	RO	0x0	CEAVID_VID_STS Indicates when video output is enabled. 1'b0: Video IF is not active 1'b1: Video IF is active

HDMI_RX_PDEC_AMP_HB
Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RO	0x00	AMP_HEADER_BYTE1 Audio Metadata packet header byte 1
7:0	RO	0x00	AMP_HEADER_BYTE0 Audio Metadata packet header byte 0

HDMI_RX_PDEC_AMP_PAYLOAD0
Address: Operational Base + offset (0x0484)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	AMP_PACKET_BYTE3 Audio Metadata packet payload byte 3
23:16	RO	0x00	AMP_PACKET_BYTE2 Audio Metadata packet payload byte 2
15:8	RO	0x00	AMP_PACKET_BYTE1 Audio Metadata packet payload byte 1
7:0	RO	0x00	AMP_PACKET_BYTE0 Audio Metadata packet payload byte 0

HDMI_RX_PDEC_AMP_PAYLOAD1

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	AMP_PACKET_BYTE7 Audio Metadata packet payload byte 7
23:16	RO	0x00	AMP_PACKET_BYTE6 Audio Metadata packet payload byte 6
15:8	RO	0x00	AMP_PACKET_BYTE5 Audio Metadata packet payload byte 5
7:0	RO	0x00	AMP_PACKET_BYTE4 Audio Metadata packet payload byte 4

HDMI_RX_PDEC_AMP_PAYLOAD2

Address: Operational Base + offset (0x048c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	AMP_PACKET_BYTE11 Audio Metadata packet payload byte 11
23:16	RO	0x00	AMP_PACKET_BYTE10 Audio Metadata packet payload byte10
15:8	RO	0x00	AMP_PACKET_BYTE9 Audio Metadata packet payload byte 9
7:0	RO	0x00	AMP_PACKET_BYTE8 Audio Metadata packet payload byte8

HDMI_RX_PDEC_AMP_PAYLOAD3

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	AMP_PACKET_BYTE15 Audio Metadata packet payload byte 15
23:16	RO	0x00	AMP_PACKET_BYTE14 Audio Metadata packet payload byte14
15:8	RO	0x00	AMP_PACKET_BYTE13 Audio Metadata packet payload byte 13
7:0	RO	0x00	AMP_PACKET_BYTE12 Audio Metadata packet payload byte 12

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HDMI_RX_PDEC_AMP_PAYLOAD4
Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	AMP_PACKET_BYTE19 Audio Metadata packet payload byte 19
23:16	RO	0x00	AMP_PACKET_BYTE18 Audio Metadata packet payload byte 18
15:8	RO	0x00	AMP_PACKET_BYTE17 Audio Metadata packet payload byte 17
7:0	RO	0x00	AMP_PACKET_BYTE16 Audio Metadata packet payload byte 16

HDMI_RX_PDEC_AMP_PAYLOAD5
Address: Operational Base + offset (0x0498)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	AMP_PACKET_BYTE23 Audio Metadata packet payload byte 23
23:16	RO	0x00	AMP_PACKET_BYTE22 Audio Metadata packet payload byte 22
15:8	RO	0x00	AMP_PACKET_BYTE21 Audio Metadata packet payload byte 21
7:0	RO	0x00	AMP_PACKET_BYTE20 Audio Metadata packet payload byte 20

HDMI_RX_PDEC_AMP_PAYLOAD6
Address: Operational Base + offset (0x049c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	AMP_PACKET_BYTE27 Audio Metadata packet payload byte27
23:16	RO	0x00	AMP_PACKET_BYTE26 Audio Metadata packet payload byte 26
15:8	RO	0x00	AMP_PACKET_BYTE25 Audio Metadata packet payload byte 25
7:0	RO	0x00	AMP_PACKET_BYTE24 Audio Metadata packet payload byte 24

HDMI_RX_PDEC_NTSCVBI_HB
Address: Operational Base + offset (0x04a0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RO	0x00	NTSCVBI_HEADER_BYTE1 Packet NTSC Vertical Blanking Interval Header Byte 1

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	NTSCVBI_HEADER_BYTE0 Packet NTSC Vertical Blanking Interval Header Byte 0

HDMI_RX_PDEC_NTSCVBI_PAYLOAD0

Address: Operational Base + offset (0x04a4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	NTSCVBI_PAYLOAD_BYTE3 Packet NTSC Vertical Blanking Interval Payload Byte 3
23:16	RW	0x00	NTSCVBI_PAYLOAD_BYTE2 Packet NTSC Vertical Blanking Interval Payload Byte 2
15:8	RO	0x00	NTSCVBI_PAYLOAD_BYTE1 Packet NTSC Vertical Blanking Interval Payload Byte 1
7:0	RO	0x00	NTSCVBI_PAYLOAD_BYTE0 Packet NTSC Vertical Blanking Interval Payload Byte 0

HDMI_RX_PDEC_NTSCVBI_PAYLOAD1

Address: Operational Base + offset (0x04a8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	NTSCVBI_PAYLOAD_BYTE7 Packet NTSC Vertical Blanking Interval Payload Byte7
23:16	RW	0x00	NTSCVBI_PAYLOAD_BYTE6 Packet NTSC Vertical Blanking Interval Payload Byte 6
15:8	RO	0x00	NTSCVBI_PAYLOAD_BYTE5 Packet NTSC Vertical Blanking Interval Payload Byte5
7:0	RO	0x00	NTSCVBI_PAYLOAD_BYTE4 Packet NTSC Vertical Blanking Interval Payload Byte4

HDMI_RX_PDEC_NTSCVBI_PAYLOAD2

Address: Operational Base + offset (0x04ac)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	NTSCVBI_PAYLOAD_BYTE11 Packet NTSC Vertical Blanking Interval Payload Byte 11
23:16	RW	0x00	NTSCVBI_PAYLOAD_BYTE10 Packet NTSC Vertical Blanking Interval Payload Byte 10
15:8	RO	0x00	NTSCVBI_PAYLOAD_BYTE9 Packet NTSC Vertical Blanking Interval Payload Byte 9
7:0	RO	0x00	NTSCVBI_PAYLOAD_BYTE8 Packet NTSC Vertical Blanking Interval Payload Byte8

HDMI_RX_PDEC_NTSCVBI_PAYLOAD3

Address: Operational Base + offset (0x04b0)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	NTSCVBI_PAYLOAD_BYTE15 Packet NTSC Vertical Blanking Interval Payload Byte15
23:16	RW	0x00	NTSCVBI_PAYLOAD_BYTE14 Packet NTSC Vertical Blanking Interval Payload Byte14
15:8	RO	0x00	NTSCVBI_PAYLOAD_BYTE13 Packet NTSC Vertical Blanking Interval Payload Byte 13
7:0	RO	0x00	NTSCVBI_PAYLOAD_BYTE12 Packet NTSC Vertical Blanking Interval Payload Byte 12

HDMI_RX_PDEC_NTSCVBI_PAYLOAD4

Address: Operational Base + offset (0x04b4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	NTSCVBI_PAYLOAD_BYTE19 Packet NTSC Vertical Blanking Interval Payload Byte 19
23:16	RW	0x00	NTSCVBI_PAYLOAD_BYTE18 Packet NTSC Vertical Blanking Interval Payload Byte 18
15:8	RO	0x00	NTSCVBI_PAYLOAD_BYTE17 Packet NTSC Vertical Blanking Interval Payload Byte 17
7:0	RO	0x00	NTSCVBI_PAYLOAD_BYTE16 Packet NTSC Vertical Blanking Interval Payload Byte 16

HDMI_RX_PDEC_NTSCVBI_PAYLOAD5

Address: Operational Base + offset (0x04b8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	NTSCVBI_PAYLOAD_BYTE23 Packet NTSC Vertical Blanking Interval Payload Byte 23
23:16	RW	0x00	NTSCVBI_PAYLOAD_BYTE22 Packet NTSC Vertical Blanking Interval Payload Byte 22
15:8	RO	0x00	NTSCVBI_PAYLOAD_BYTE21 Packet NTSC Vertical Blanking Interval Payload Byte 21
7:0	RO	0x00	NTSCVBI_PAYLOAD_BYTE20 Packet NTSC Vertical Blanking Interval Payload Byte 20

HDMI_RX_PDEC_NTSCVBI_PAYLOAD6

Address: Operational Base + offset (0x04bc)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	NTSCVBI_PAYLOAD_BYTE27 Packet NTSC Vertical Blanking Interval Payload Byte 27
23:16	RW	0x00	NTSCVBI_PAYLOAD_BYTE26 Packet NTSC Vertical Blanking Interval Payload Byte 26
15:8	RO	0x00	NTSCVBI_PAYLOAD_BYTE25 Packet NTSC Vertical Blanking Interval Payload Byte25
7:0	RO	0x00	NTSCVBI_PAYLOAD_BYTE24 Packet NTSC Vertical Blanking Interval Payload Byte 24

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HDMI_RX_PDEC_DRM_HB

Address: Operational Base + offset (0x04c0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RO	0x00	DRM_HEADER_BYTE1 Packet Dynamic Range and Mastering Header Byte HB2
7:0	RO	0x00	DRM_HEADER_BYTE0 Packet Dynamic Range and Mastering Header Byte HB1

HDMI_RX_PDEC_DRM_PAYLOAD0

Address: Operational Base + offset (0x04c4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DRM_PAYLOAD_BYTE3 Packet Dynamic Range and Mastering Payload Byte 3
23:16	RO	0x00	DRM_PAYLOAD_BYTE2 Packet Dynamic Range and Mastering Payload Byte 2
15:8	RO	0x00	DRM_PAYLOAD_BYTE1 Packet Dynamic Range and Mastering Payload Byte 1
7:0	RO	0x00	DRM_PAYLOAD_BYTE0 Packet Dynamic Range and Mastering Payload Byte 0

HDMI_RX_PDEC_DRM_PAYLOAD1

Address: Operational Base + offset (0x04c8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DRM_PAYLOAD_BYTE7 Packet Dynamic Range and Mastering Payload Byte 7
23:16	RO	0x00	DRM_PAYLOAD_BYTE6 Packet Dynamic Range and Mastering Payload Byte6
15:8	RO	0x00	DRM_PAYLOAD_BYTE5 Packet Dynamic Range and Mastering Payload Byte 5
7:0	RO	0x00	DRM_PAYLOAD_BYTE4 Packet Dynamic Range and Mastering Payload Byte 4

HDMI_RX_PDEC_DRM_PAYLOAD2

Address: Operational Base + offset (0x04cc)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DRM_PAYLOAD_BYTE11 Packet Dynamic Range and Mastering Payload Byte11
23:16	RO	0x00	DRM_PAYLOAD_BYTE10 Packet Dynamic Range and Mastering Payload Byte 10
15:8	RO	0x00	DRM_PAYLOAD_BYTE9 Packet Dynamic Range and Mastering Payload Byte9

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	DRM_PAYLOAD_BYTE8 Packet Dynamic Range and Mastering Payload Byte 8

HDMI_RX_PDEC_DRM_PAYLOAD3
Address: Operational Base + offset (0x04d0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DRM_PAYLOAD_BYTE15 Packet Dynamic Range and Mastering Payload Byte15
23:16	RO	0x00	DRM_PAYLOAD_BYTE14 Packet Dynamic Range and Mastering Payload Byte 14
15:8	RO	0x00	DRM_PAYLOAD_BYTE13 Packet Dynamic Range and Mastering Payload Byte 13
7:0	RO	0x00	DRM_PAYLOAD_BYTE12 Packet Dynamic Range and Mastering Payload Byte12

HDMI_RX_PDEC_DRM_PAYLOAD4
Address: Operational Base + offset (0x04d4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DRM_PAYLOAD_BYTE19 Packet Dynamic Range and Mastering Payload Byte19
23:16	RO	0x00	DRM_PAYLOAD_BYTE18 Packet Dynamic Range and Mastering Payload Byte 18
15:8	RO	0x00	DRM_PAYLOAD_BYTE17 Packet Dynamic Range and Mastering Payload Byte 17
7:0	RO	0x00	DRM_PAYLOAD_BYTE16 Packet Dynamic Range and Mastering Payload Byte16

HDMI_RX_PDEC_DRM_PAYLOAD5
Address: Operational Base + offset (0x04d8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DRM_PAYLOAD_BYTE23 Packet Dynamic Range and Mastering Payload Byte23
23:16	RO	0x00	DRM_PAYLOAD_BYTE22 Packet Dynamic Range and Mastering Payload Byte 22
15:8	RO	0x00	DRM_PAYLOAD_BYTE21 Packet Dynamic Range and Mastering Payload Byte 21
7:0	RO	0x00	DRM_PAYLOAD_BYTE20 Packet Dynamic Range and Mastering Payload Byte 20

HDMI_RX_PDEC_DRM_PAYLOAD6
Address: Operational Base + offset (0x04dc)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	DRM_PAYLOAD_BYTE27 Packet Dynamic Range and Mastering Payload Byte 27
23:16	RO	0x00	DRM_PAYLOAD_BYTE26 Packet Dynamic Range and Mastering Payload Byte 26
15:8	RO	0x00	DRM_PAYLOAD_BYTE25 Packet Dynamic Range and Mastering Payload Byte 25
7:0	RO	0x00	DRM_PAYLOAD_BYTE24 Packet Dynamic Range and Mastering Payload Byte 24

HDMI_RX_MHLMODE_CTRL

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	CDSENSE_EN CDSENSE enable. This bit directly drives the output ophy_cdsense_en. It has no impact on the Controller operation 1'b0: Disable CDSENSE circuit 1'b1: Enable CDSENSE circuit
11:9	RO	0x0	reserved
8	RW	0x0	MHLMODE_MAN_OVR Manual MHL mode override 1'b0: MHL mode is controlled by CDSENSE input 1'b1: MHL mode is controlled by the value in mhlmode_man field
7:5	RO	0x0	reserved
4	RW	0x0	MHLPPIXMODE HL PackedPixel mode 1'b0: PackedPixel mode disabled 1'b1: PackedPixel mode enabled Attention: The software must guarantee that this field is only configured high if MHL mode is enabled by one of the following conditions: ■ mhlmode_man_ovr=1 with mhlmode_man=1 or ■ mhlmode_man_ovr=0 with cdsense_status.cdsense_sts=1 Setting mhlppixmode high while MHL mode is disabled may lead to data corruption
3:1	RO	0x0	reserved
0	RW	0x0	MHLMODE_MAN Manual MHL mode selection. Enables MHL mode and emulates the CDSENSE cable attachment detection to the CBUS Device Discovery module. This field is only used by the controller if mhlmode_man_ovr = 1. 1'b0: MHL mode disabled 1'b1: MHL mode enabled

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HDMI_RX_CDSENSE_STATUS
Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	CDSENSE_STS Status of the CDSENSE input, the MHL cable detect mechanism 1'b0: No cable detected 1'b1: Cable attached

HDMI_RX_DESERFIFO_CTRL
Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	DESERFIFOCLR MHL Datapath Deserializer FIFO clear

HDMI_RX_DESER_INTTRSHCTRL
Address: Operational Base + offset (0x050c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	DESER_MISAL_CNTEN Interrupt counter enable for deserializer channel misalignment 1'b0: The interrupt is set every time the related event occurs 1'b1: The interrupt is set when the counter is a multiple of the value set by the threshold
2:0	RW	0x0	DESER_MISAL_TRSHLD Interrupt counter threshold for deserializer channel misalignment; programmable values are: 3'b0: 32 3'b1: 64 3'b2: 128 3'b3: 256 3'b4: 512 3'b5: 1024 3'b6: 2048 3'b7: 4096 Note: The first interrupt source event always triggers an interrupt pulse. The subsequent events are filtered by this threshold counter

HDMI_RX_DESER_INTCNTCTRL
Address: Operational Base + offset (0x0510)

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	DESER_MISAL_CNTCLR Clear deser_misal_cnt interrupt counter 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear

HDMI_RX_DESER_INTCNT

Address: Operational Base + offset (0x0514)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	DESER_MISAL_CNT Interrupt counter for deser_misal If deser_misal_cnten = 1, this counter is incremented every time the related event occurs

HDMI_RX_HDCP_RPT_CTRL

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RO	0x0	RPT_KSV_HOLD Status flag to indicate whether key set writing is: 1'b0: Allowed 1'b1: Not allowed Note: Writes to this bit have no effect. If this bit is written to, however, no APB error flag occurs because APB errors only occur at the register level and not the bit level
5	RO	0x0	RPT_WAITING_KSV Indicates that the HDCP hardware has completed the first part of the authentication, and is currently waiting for the KSV FIFO to be written, and rpt_ksvlist_ready is to be set. Note: Writes to this bit have no effect. If this bit is written to, however, no APB error flag occurs because APB errors only occur at the register level and not the bit level
4	RO	0x0	RPT_READY KSV FIFO ready Status flag to indicate that the HDCP hardware has completed the second part of the authentication process (KSV FIFO ready), and has computed the verification value V. It requires no software action, and is useful in the debug process. Note: Writes to this bit have no effect. If this bit is written to, however, no APB error flag occurs because APB errors only occur at the register level and not the bit level

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Bit	Attr	Reset Value	Description
3	RW	0x0	REPEATER HDCP Repeater capability 1'b0: Only HDCP Receiver is available 1'b1: HDCP Receiver supports downstream connections like HDCP Repeaters
2	WO	0x0	RPT_KSVLIST_READY Auto-clearing. Indicates that software has completed the KSV memory write process. Note: After successfully finish the first part of authentication protocol this value shall only be set to 1'b1 if rpt_waiting_ksv is at 1'b1
1	WO	0x0	RPT_TIMEOUT Auto-clearing. A timeout or a topology error as occurred when gathering the KSV list from the downstream devices
0	WO	0x0	RPT_LOST_AUTH Auto-clearing. Detected the lost of authentication by a downstream device

HDMI_RX_HDCP_RPT_BSTATUS

Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	RPT_MAX_CASCADE_EXCEED Topology error indicator Set it to 1 when more than seven levels of video repeaters are cascaded together
10:8	RW	0x0	RPT_DEPTH Three-bit repeater cascade depth Set it to indicate the number of attached levels through the connection topology. For more information, see Highbandwidth Digital Content Protection Specification
7	RW	0x0	RPT_MAX_DEVS_EXCEEDED Topology error indicator Set to 1 when more than 127 downstream devices are detected, or when the capacity of the KSV FIFO is exceeded
6:0	RW	0x00	RPT_DEVICE_COUNT Total number of attached downstream devices Set to 0 if you have HDCP Receivers only. Do not include the HDCP Repeater itself in this count. Include the devices downstream for the HDCP Repeater

HDMI_RX_HDCP_RPT_KSVFIFO_CTRL

Address: Operational Base + offset (0x0608)

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Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	RPT_KSV_FIFO_INDEX KSV list index pointer

HDMI_RX_HDCP_RPT_KSVFIFO1

Address: Operational Base + offset (0x060c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	RPT_KSV_39_32 Returns the value last written in the register, and not the value written in the FIFO at the currently selected rpt_ksv_fifo_index bit

HDMI_RX_HDCP_RPT_KSVFIFO0

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	RPT_KSV_31_0 Returns the value last written in the register, and not the value written in the FIFO at the currently selected rpt_ksv_fifo_index bit

HDMI_RX_HDMI20_CONTROL

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	PVOREMAP_CLEAR Synchronous clear configuration, active high. (Exists: HRX_PVO_REMAP==1)
29	RW	0x0	PVO1UNMUTE PVO_remap channel 1 unmute when pixel mode is singlepixel mode: 1'b0: PVO_remap channel 1 is muted when pixel mode is single-pixel mode. 1'b1: PVO_remap channel 1 is unmuted when pixel mode is single-pixel mode (PVO_remap channel 1 equal to PVO_remap channel 0). (Exists: HRX_PVO_REMAP==1)
28	RW	0x0	PIXELMODE Pixel mode selection 1'b0: Single-pixel mode 1'b1: Dual-pixel mode (Exists: HRX_PVO_REMAP==1)
27:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	VIDDATACHECKEN Character Error Detection - Video Data period check enable
11	RW	0x0	DATAISCHECKEN Character Error Detection - Data Island Period check enable
10	RW	0x0	GBCHECKEN Character Error Detection - Guard Band Period check enable
9	RW	0x0	PREAMBCHECKEN Character Error Detection - Preamble Period check enable
8	RW	0x0	CTRLCHECKEN Character Error Detection - Control Period check enable
7:5	RO	0x0	reserved
4	RW	0x0	SCDC_ENABLE Status and Control Data Channel enable 1'b0: SCDC disable 1'b1: SCDC enable
3:2	RO	0x0	reserved
1:0	RW	0x0	SCRAMBEN_SEL Scrambling enable selection: 2'b0: SCDC control 2'b1: Auto -> enable when detected scrambled data 2'b2: Auto -> enable when detected scrambled data 2'b3: Forces descrambling

HDMI_RX_SCDC_I2CCONFIG

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	I2CSPIKESUPPR SCDC I2C Select spike suppression mode 2'b00: 2 out of 2 2'b01: 2 out of 3 (majority selection) 2'b10: 3 out of 3 2'b11: 4 out of 4
23:21	RO	0x0	reserved
20	RW	0x0	I2CTIMOUTEN SCDC I2C timeout enable
19:0	RW	0x00000	I2CTIMOUTCNT SCDC I2C timeout window value

HDMI_RX_SCDC_CONFIG

Address: Operational Base + offset (0x0808)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	RR_IFFLAGS_ALREADYSET Read Request sent if RR_Enable bit is set with any of the Update Flags already @ 1 1'b1: Read Request sent when RR_Enable bit is set and any of the Update Flags is already @ 1 1'b0: Read Request sent only when RR_Enable is previously active and any of the Update Flags transitions from 0 to 1
3:2	RO	0x0	reserved
1	RW	0x0	HPDLOW Hot Plug Detect pin has voltage = low for 100 ms or more
0	RW	0x0	POWERPROVIDED Power provided 1'b1: +5V Power Signal is provided by the Source 1'b0: +5V Power Signal is not provided by the Source

HDMI_RX_CHLOCK_CONFIG

Address: Operational Base + offset (0x080c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	CHLOCKMAXER Channel Lock Maximum errors number Configures the maximum number of errors over a 10ms period for a channel to be considered locked
19:16	RO	0x0	reserved
15:0	RW	0x0000	MILISECTIMERLIMIT 1 millisecond Timer limit (used in Channel lock and SCDC Test Configuration) Configure the number of imodetclk cycles in 1ms using the following formula:0.001* imodetclk_freq

HDMI_RX_HDCP22_CONTROL

Address: Operational Base + offset (0x081c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x0	HDCP22_CD_OVR_VAL HDCP 2.2 color depth override value. Refer to HDMI Color Depth specification
19:17	RO	0x0	reserved
16	RW	0x0	HDCP22_CD_OVR_EN HDCP 2.2 color depth override enable
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	HDCP22_HPD HDCP 2.2 HPD value
11:10	RO	0x0	reserved
9	RW	0x0	HDCP22_PKT_ERR_OVR_VAL HDCP 2.2 AVMUTE packet error override value: 1'b0: No packet error 1'b1: Packet error
8	RW	0x0	HDCP22_PKT_ERR_OVR_EN HDCP 2.2 AVMUTE packet error override enable
7:6	RO	0x0	reserved
5	RW	0x0	HDCP22_AVMUTE_OVR_VAL HDCP 2.2 AVMUTE override value: 1'b0: Not AVMUTE 1'b1: AVMUTE
4	RW	0x0	HDCP22_AVMUTE_OVR_EN HDCP 2.2 AVMUTE override enable
3	RO	0x0	reserved
2	RW	0x0	HDCP22_OVR_VAL HDCP 2.2 override value: 1'b0: HDCP 1.4 1'b1: HDCP 2.2
1	RW	0x0	HDCP22_OVR_EN HDCP 2.2 override enable
0	RW	0x0	HDCP22_SWITCH_LCK HDCP 2.2 switch lock

HDMI_RX_SCDC_REGS0

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RO	0x0	SCDC_SCRAMBSTATUS SCDC Status register - Scrambling_Status
23:18	RO	0x0	reserved
17	RO	0x0	SCDC_TMDSBITCLKRATIO SCDC TMDS Configuration register - TMDS_Bit_Clock_ratio
16	RO	0x0	SCDC_SCRAMBEN SCDC TMDS Configuration register - Scrambling_Enable
15:11	RO	0x0	reserved
10	RO	0x0	SCDC_RRTEST SCDC Update Flags register - RR_Test
9	RO	0x0	SCDC_CEDUPDATE SCDC Update Flags register - CED_Update
8	RO	0x0	SCDC_STATUSUPDATE SCDC Update Flags register - Status_Update

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	SCDC_SOURCEREVISION SCDC Source Version/Revision register- Source Revision

HDMI_RX_SCDC_REGS1

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31	RO	0x0	SCDC_ERRDET0_VALID SCDC CED registers- Channel 0 Character Error Valid
30:16	RO	0x0000	SCDC_ERRDET0 SCDC CED registers- Channel 0 Character Error Count
15:12	RO	0x0	reserved
11	RO	0x0	SCDC_CH2LOCKED SCDC Status Flags register - Ch2_Locked
10	RO	0x0	SCDC_CH1LOCKED SCDC Status Flags register - Ch1_Locked
9	RO	0x0	SCDC_CH0LOCKED SCDC Status Flags register - Ch0_Locked
8	RO	0x0	SCDC_CLOCKDETECTED SCDC Status Flags register - Clock_Detected
7:1	RO	0x0	reserved
0	RO	0x0	SCDC_RRENABLE SCDC Configuration register- RR_Enable

HDMI_RX_SCDC_REGS2

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31	RO	0x0	SCDC_ERRDET2_VALID SCDC CED registers- Channel 2 Character Error Valid
30:16	RO	0x0000	SCDC_ERRDET2 SCDC CED registers- Channel 2 Character Error Count
15	RO	0x0	SCDC_ERRDET1_VALID SCDC CED registers- Channel 1 Character Error Valid
14:0	RO	0x0000	SCDC_ERRDET1 SCDC CED registers- Channel 1 Character Error Count

HDMI_RX_SCDC_REGS3

Address: Operational Base + offset (0x082c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RO	0x0	SCDC_TESTREADREQ SCDC Test Configuration register - TestReadRequest
6:0	RO	0x00	SCDC_TESTREADREQDELAY SCDC Test Configuration register - TestReadRequestDelay

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HDMI_RX_SCDC_MANSPEC0
Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	MANUFACTURSPECIFICWR0 SCDC Manufacturer Specific Registers - ManufacturerSpecific_Wr[31:0]

HDMI_RX_SCDC_MANSPEC1
Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	MANUFACTURSPECIFICWR1 SCDC Manufacturer Specific Registers - ManufacturerSpecific_Wr[63:32]

HDMI_RX_SCDC_MANSPEC2
Address: Operational Base + offset (0x0848)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	MANUFACTURSPECIFICWR2 SCDC Manufacturer Specific Registers - ManufacturerSpecific_Wr0[95:64]

HDMI_RX_SCDC_MANSPEC3
Address: Operational Base + offset (0x084c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	MANUFACTURSPECIFICWR3 SCDC Manufacturer Specific Registers - ManufacturerSpecific_Wr[127:96]

HDMI_RX_SCDC_MANSPEC4
Address: Operational Base + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	MANUFACTURSPECIFICWR4 SCDC Manufacturer Specific Registers - ManufacturerSpecific_Wr[143:128]

HDMI_RX_SCDC_WRDATA0
Address: Operational Base + offset (0x0860)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	MANUFACTUREROUI SCDC Manufacturer Specific registers - Manufacturer_OUI
7:0	RW	0x00	SINKVERSION SCDC Sink Version register - Sink Version

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HDMI_RX_SCDC_WRDATA1
Address: Operational Base + offset (0x0864)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DEVICEID_STRING0 SCDC Manufacturer Specific registers - Device ID_String LSBytes

HDMI_RX_SCDC_WRDATA2
Address: Operational Base + offset (0x0868)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DEVICEID_STRING1 SCDC Manufacturer Specific registers - Device ID_String MSBytes

HDMI_RX_SCDC_WRDATA3
Address: Operational Base + offset (0x086c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	DEVICEID_SWMINORREV SCDC Manufacturer Specific registers - Device ID Software Minor Rev
15:8	RW	0x00	DEVICEID_SWMAJORREV SCDC Manufacturer Specific registers - Device ID Software Major Rev
7:4	RW	0x0	DEVICEID_MAJORREV SCDC Manufacturer Specific registers - Device ID Hardware Major Rev
3:0	RW	0x0	DEVICEID_MINORREV SCDC Manufacturer Specific registers - Device ID Hardware Minor Rev

HDMI_RX_SCDC_WRDATA4
Address: Operational Base + offset (0x0870)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MANUFACTURSPECIFIC0 SCDC Manufacturer Specific registers - ManufacturerSpecific_Rd[31:0]

HDMI_RX_SCDC_WRDATA5
Address: Operational Base + offset (0x0874)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MANUFACTURSPECIFIC1 SCDC Manufacturer Specific registers - ManufacturerSpecific_Rd[63:32]

HDMI_RX_SCDC_WRDATA6

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Address: Operational Base + offset (0x0878)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MANUFACTURSPECIFIC2 SCDC Manufacturer Specific registers - ManufacturerSpecific_Rd[95:64]

HDMI_RX_SCDC_WRDATA7

Address: Operational Base + offset (0x087c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MANUFACTURSPECIFIC3 SCDC Manufacturer Specific registers - ManufacturerSpecific_Rd[127:96]

HDMI_RX_HDMI20_STATUS

Address: Operational Base + offset (0x08e0)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	SCRAMBDET Scrambling detected (scramble detected even auto detection control disabled)

HDMI_RX_HDCP2_ESM_GLOBAL_GPIO_IN

Address: Operational Base + offset (0x08e8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_I Global General-Purpose inputs to the HDCP2 ESM block - Check ESM Databook for details

HDMI_RX_HDCP2_ESM_GLOBAL_GPIO_OUT

Address: Operational Base + offset (0x08ec)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_O Global General-Purpose outputs from the HDCP2 ESM block - Check ESM Databook for details

HDMI_RX_HDCP2_ESM_P0_GPIO_IN

Address: Operational Base + offset (0x08f0)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:1	RW	0x0	HDCP2_ESM_P0_GPIO_IN Port 0 General-Purpose inputs to the HDCP2 ESM block - Check ESM Databook for details
0	RO	0x0	reserved

HDMI_RX_HDCP2_ESM_P0_GPIO_OUT

Address: Operational Base + offset (0x08f4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	HDCP2_ESM_P0_GPIO_OUT Port 0 General-Purpose outputs from the HDCP2 ESM block - Check ESM Databook for details

HDMI_RX_HDCP22_STATUS

Address: Operational Base + offset (0x08fc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RO	0x0	HDCP22_CD_STS HDCP 2.2 color depth status
11:10	RO	0x0	reserved
9	RO	0x0	HDCP22_PKT_ERR_STS HDCP 2.2 packet error status
8	RO	0x0	HDCP22_AVMUTE_STS HDCP 2.2 AVMUTE status
7	RO	0x0	HDCP22_SWITCH_LCK_STS HDCP 2.2 switch lock status
6	RO	0x0	HDCP22_OVR_EN_STS HDCP 2.2 override enable status
5	RO	0x0	HDCP22_OVR_VAL_STS HDCP 2.2 override value status 1'b0: HDCP 1.4 1'b1: HDCP 2.2
4	RO	0x0	HDCPTYPESEL_STS HDCP type selection 1'b0: HDCP 1.4 1'b1: HDCP 2.2
3:2	RO	0x0	reserved
1	RO	0x0	HDCP22INAVMUTE HDCP 2 in AVMUTE
0	RO	0x0	HDCP_DECRYPTED HDCP 2 decrypted

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HDMI_RX_HDMI2_IEN_CLR

Address: Operational Base + offset (0x0f60)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[15] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
25	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[14] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
24	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[13] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
23	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[12] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
22	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[11] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
21	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[10] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
20	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[9] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[8] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[7] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[6] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_ENCLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[5] - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HRX_HDCP22_EXT_GPIOS==1)
15:7	RO	0x0	reserved
6	WO	0x0	HDCP_TYPESEL_CHANGE_EN HDCP type (hdcp22_status:hdcptypesel_sts) change interrupt - Enable clear. 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
5	WO	0x0	HDCP_DECRYPTED_CHANGE_ENCLR External HDCP 2.0 decrypted change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

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Bit	Attr	Reset Value	Description
4	WO	0x0	HDCP_AUTHENTICATION_FAIL_ENCLR External HDCP 2.0 authentication fail interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
3	WO	0x0	HDCP_AUTHENTICATED_ENCLR External HDCP 2.0 authenticated interrupt - Enable clear 1'b0: No action 1d'1: Disable the interrupt. The enable status bit changes to 0
2	WO	0x0	HDCP_AUTHENTICATION_LOST_ENCLR External HDCP 2.0 authentication lost interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
1	WO	0x0	HDCP2_NOT_CAPABLE_ENCLR External HDCP 2.0 not capable interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
0	WO	0x0	HDCP2_CAPABLE_ENCLR External HDCP 2.0 capable interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

HDMI_RX_HDMI2_IEN_SET

Address: Operational Base + offset (0x0f64)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[15] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
25	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[14] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
24	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[13] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
23	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[12] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
22	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[11] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
21	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[10] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
20	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[9] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[8] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[7] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[6] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_ENSET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[5] - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1 (Exists: HRX_HDCP22_EXT_GPIOS==1)
15:7	RO	0x0	reserved
6	WO	0x0	HDCP_TYPESEL_CHANGE_ENSET HDCP type (hdcp22_status:hdcptypesel_sts) change interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
5	WO	0x0	HDCP_DECRYPTED_CHANGE_ENSET External HDCP 2.0 decrypted change interrupt - Enableset 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
4	WO	0x0	HDCP_AUTHENTICATION_FAIL_ENSET External HDCP 2.0 authentication fail interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
3	WO	0x0	HDCP_AUTHENTICATED_ENSET External HDCP 2.0 authenticated interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
2	WO	0x0	HDCP_AUTHENTICATION_LOST_ENSET External HDCP 2.0 authentication lost interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
1	WO	0x0	HDCP2_NOT_CAPABLE_ENSET External HDCP 2.0 not capable interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

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Bit	Attr	Reset Value	Description
0	WO	0x0	HDCP2_CAPABLE_ENSET External HDCP 2.0 capable interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

HDMI_RX_HDMI2_ISTS

Address: Operational Base + offset (0x0f68)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[15] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
25	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[14] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
24	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[13] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
23	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[12] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
22	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[11] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
21	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[10] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
20	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[9] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
19	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[8] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
18	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[7] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
17	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[6] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
16	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_ISTS Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[5] - interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HRX_HDCP22_EXT_GPIOS==1)
15:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RO	0x0	HDCP_TYPESEL_CHANGE_ISTS HDCP type (hdcp22_status:hdcptypesel_sts) change interrupt flag status 1'b0: Inactive 1'b1: Active
5	RO	0x0	HDCP_DECRYPTED_CHANGE_ISTS External HDCP 2.0 decrypted change interrupt flag status 1'b0: Inactive 1'b1: Active
4	RO	0x0	HDCP_AUTHENTICATION_FAIL_ISTS External HDCP 2.0 authentication fail interrupt flag status 1'b0: Inactive 1'b1: Active
3	RO	0x0	HDCP_AUTHENTICATED_ISTS External HDCP 2.0 authenticated interrupt flag status 1'b0: Inactive 1'b1: Active
2	RO	0x0	HDCP_AUTHENTICATION_LOST_ISTS External HDCP 2.0 authentication lost interrupt flag status 1'b0: Inactive 1'b1: Active
1	RO	0x0	HDCP2_NOT_CAPABLE_ISTS External HDCP 2.0 not capable interrupt flag status 1'b0: Inactive 1'b1: Active
0	RO	0x0	HDCP2_CAPABLE_ISTS External HDCP 2.0 capable interrupt flag status 1'b0: Inactive 1'b1: Active

HDMI_RX_HDMI2_IEN

Address: Operational Base + offset (0x0f6c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[15] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)

Rockchip Confidential

Bit	Attr	Reset Value	Description
25	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[14] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
24	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[13] -enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
23	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[12] -enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
22	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[11] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
21	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[10] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
20	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[9] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[8] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[7] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[6] -enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_IEN Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[5] - enable status 1'b0: Disabled 1'b1: Enabled (Exists: HRX_HDCP22_EXT_GPIOS==1)
15:7	RO	0x0	reserved
6	WO	0x0	HDCP_TYPESEL_CHANGE_IEN HDCP type (hdcp22_status:hdcptypesel_sts) change interrupt enable status 1'b0: Disabled 1'b1: Enabled
5	WO	0x0	HDCP_DECRYPTED_CHANGE_IEN External HDCP 2.0 decrypted change interrupt interrupt enable status 1'b0: Disabled 1'b1: Enabled
4	WO	0x0	HDCP_AUTHENTICATION_FAIL_IEN External HDCP 2.0 authentication fail interrupt interrupt enable status 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
3	WO	0x0	HDCP_AUTHENTICATED_IEN External HDCP 2.0 authenticated interrupt interrupt enable status 1'b0: Disabled 1'b1: Enabled
2	WO	0x0	HDCP_AUTHENTICATION_LOST_IEN External HDCP 2.0 authentication lost interrupt interrupt enable status 1'b0: Disabled 1'b1: Enabled
1	WO	0x0	HDCP2_NOT_CAPABLE_IEN External HDCP 2.0 not capable interrupt interrupt enable status 1'b0: Disabled 1'b1: Enabled
0	WO	0x0	HDCP2_CAPABLE_IEN External HDCP 2.0 capable interrupt interrupt enable status 1'b0: Disabled 1'b1: Enabled

HDMI_RX_HDMI2_ICLR

Address: Operational Base + offset (0x0f70)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[15] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
25	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[14] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
24	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[13] -flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
23	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[12] -flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
22	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[11] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
21	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[10] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
20	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[9] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[8] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[7] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[6] -flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CLR Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[5] - flag clear 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
15:7	RO	0x0	reserved
6	WO	0x0	HDCP_TYPESEL_CHANGE_CLR HDCP type (hdcp22_status:hdcptypesel_sts) change interrupt flag clear 1'b0: No action 1'b1: Action
5	WO	0x0	HDCP_DECRYPTED_CHANGE_CLR External HDCP 2.0 decrypted change interrupt interrupt flag clear 1'b0: No action 1'b1: Action
4	WO	0x0	HDCP_AUTHENTICATION_FAIL_CLR External HDCP 2.0 authentication fail interrupt interrupt flag clear 1'b0: No action 1'b1: Action
3	WO	0x0	HDCP_AUTHENTICATED_CLR External HDCP 2.0 authenticated interrupt interrupt flag clear 1'b0: No action 1'b1: Action
2	WO	0x0	HDCP_AUTHENTICATION_LOST_CLR External HDCP 2.0 authentication lost interrupt interrupt flag clear 1'b0: No action 1'b1: Action
1	WO	0x0	HDCP2_NOT_CAPABLE_CLR External HDCP 2.0 not capable interrupt interrupt flag clear 1'b0: No action 1'b1: Action
0	WO	0x0	HDCP2_CAPABLE_CLR External HDCP 2.0 capable interrupt interrupt flag clear 1'b0: No action 1'b1: Action

HDMI_RX_HDMI2_ISET

Address: Operational Base + offset (0x0f74)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[15] - set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
25	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[14] - set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
24	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[13] - set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
23	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[12] - set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
22	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[11] -set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
21	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[10] - set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
20	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[9] -set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)

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Bit	Attr	Reset Value	Description
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[8] -set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[7] -set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[6] -set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_SET Port 0 General-Purpose outputs from the HDCP2 ESM block - Change interrupt for bit hdcp2_esm_p0_gpio_out[5] -set 1'b0: No action 1'b1: Action (Exists: HRX_HDCP22_EXT_GPIOS==1)
15:7	RO	0x0	reserved
6	WO	0x0	HDCP_TYPESEL_CHANGE_SET HDCP type (hdcp22_status:hdcptypesel_sts) change interrupt set 1'b0: No action 1'b1: Action
5	WO	0x0	HDCP_DECRYPTED_CHANGE_SET External HDCP 2.0 decrypted change interrupt interrupt flag set 1'b0: No action 1'b1: Action
4	WO	0x0	HDCP_AUTHENTICATION_FAIL_SET External HDCP 2.0 authentication fail interrupt interrupt set 1'b0: No action 1'b1: Action
3	WO	0x0	HDCP_AUTHENTICATED_SET External HDCP 2.0 authenticated interrupt interrupt set 1'b0: No action 1'b1: Action
2	WO	0x0	HDCP_AUTHENTICATION_LOST_SET External HDCP 2.0 authentication lost interrupt interrupt set 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
1	WO	0x0	HDCP2_NOT_CAPABLE_SET External HDCP 2.0 not capable interrupt interrupt set 1'b0: No action 1'b1: Action
0	WO	0x0	HDCP2_CAPABLE_SET External HDCP 2.0 capable interrupt interrupt set 1'b0: No action 1'b1: Action

HDMI_RX_PDEC_IEN_CLR

Address: Operational Base + offset (0x0f78)

Bit	Attr	Reset Value	Description
31	WO	0x0	DRM_CKS_CHG_ENCLR Dynamic Range and Mastering InfoFrame packet checksum change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: DWC_HDMI_RX_20==1)
30	WO	0x0	DRM_RCV_ENCLR Dynamic Range and Mastering InfoFrame packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: DWC_HDMI_RX_20==1)
29	WO	0x0	AUD_TYPE_CHG_ENCLR Audio type change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
28	WO	0x0	DVIDET_ENCLR DVI mode detected interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
27	WO	0x0	VSI_CKS_CHG_ENCLR VSI checksum change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
26	WO	0x0	GMD_CKS_CHG_ENCLR GMD (gamut meta data) checksum change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
25	WO	0x0	AIF_CKS_CHG_ENCLR AIF checksum change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

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Bit	Attr	Reset Value	Description
24	WO	0x0	AVI_CKS_CHG_ENCLR AVI checksum change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
23	WO	0x0	ACR_N_CHG_ENCLR ACR N value change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
22	WO	0x0	ACR_CTS_CHG_ENCLR ACR CTS value change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
21	WO	0x0	GCP_AV_MUTE_CHG_ENCLR GCP AVMUTE change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
20	WO	0x0	GMD_RCV_ENCLR GMD (gamut meta data) packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
19	WO	0x0	AIF_RCV_ENCLR AIF packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
18	WO	0x0	AVI_RCV_ENCLR AVI packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
17	WO	0x0	ACR_RCV_ENCLR ACR packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
16	WO	0x0	GCP_RCV_ENCLR GCP packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
15	WO	0x0	VSI_RCV_ENCLR VSI packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
14	WO	0x0	AMP_RCV_ENCLR Audio multi stream packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: DWC_HDMI_RX_20==1)

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Bit	Attr	Reset Value	Description
13	WO	0x0	AMP_CHG_ENCLR Audio Multistream packet checksum change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: DWC_HDMI_RX_20==1)
12	WO	0x0	NTSCVBI_CKS_CHG_ENCLR NTSC VBI packet checksum change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
11	WO	0x0	NTSCVBI_RCV_ENCLR NTSC VBI packet received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
10:9	RO	0x0	reserved
8	WO	0x0	PD_FIFO_NEW_ENTRY_ENCLR Packet decoder FIFO new entry interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
7:5	RO	0x0	reserved
4	WO	0x0	PD_FIFO_OVERFL_ENCLR Packet decoder FIFO overflow interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
3	WO	0x0	PD_FIFO_UNDERFL_ENCLR Packet decoder FIFO underflow interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
2	WO	0x0	PD_FIFO_TH_START_PASS_ENCLR Packet decoder FIFO start threshold pass interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
1	WO	0x0	PD_FIFO_TH_MAX_PASS_ENCLR Packet decoder FIFO maximum threshold pass interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
0	WO	0x0	PD_FIFO_TH_MIN_PASS_ENCLR Packet decoder FIFO minimum threshold pass interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

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HDMI_RX_PDEC_IEN_SET

Address: Operational Base + offset (0x0f7c)

Bit	Attr	Reset Value	Description
31	WO	0x0	DRM_CKS_CHG_ENSET Dynamic Range and Mastering InfoFrame packet checksum change interrupt-Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: DWC_HDMI_RX_20==1)
30	WO	0x0	DRM_RCV_ENSET Dynamic Range and Mastering InfoFrame packet received interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: DWC_HDMI_RX_20==1)
29	WO	0x0	AUD_TYPE_CHG_ENSET Audio type change interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
28	WO	0x0	DVIDET_ENSET DVI mode detected interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
27	WO	0x0	VSI_CKS_CHG_ENSET VSI checksum change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
26	WO	0x0	GMD_CKS_CHG_ENSET GMD (gamut meta data) checksum change interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
25	WO	0x0	AIF_CKS_CHG_ENSET AIF checksum change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
24	WO	0x0	AVI_CKS_CHG_ENSET AVI checksum change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
23	WO	0x0	ACR_N_CHG_ENSET ACR N value change interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

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Bit	Attr	Reset Value	Description
22	WO	0x0	ACR_CTS_CHG_ENSET ACR CTS value change interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
21	WO	0x0	GCP_AV_MUTE_CHG_ENSET GCP AVMUTE change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
20	WO	0x0	GMD_RCV_ENSET GMD (gamut meta data) packet received interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
19	WO	0x0	AIF_RCV_ENSET AIF packet received interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
18	WO	0x0	AVI_RCV_ENSET AVI packet received interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
17	WO	0x0	ACR_RCV_ENSET ACR packet received interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
16	WO	0x0	GCP_RCV_ENSET GCP packet received interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
15	WO	0x0	VSI_RCV_ENSET VSI packet received interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
14	WO	0x0	AMP_RCV_ENSET Audio multi stream packet received interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: DWC_HDMI_RX_20==1)
13	WO	0x0	AMP_CHG_ENSET Audio Multistream packet checksum change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: DWC_HDMI_RX_20==1)

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Bit	Attr	Reset Value	Description
12	WO	0x0	NTSCVBI_CKS_CHG_ENSET NTSC VBI packet checksum change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
11	WO	0x0	NTSCVBI_RCV_ENSET NTSC VBI packet received interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
10:9	RO	0x0	reserved
8	WO	0x0	PD_FIFO_NEW_ENTRY_ENSET Packet decoder FIFO new entry interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
7:5	RO	0x0	reserved
4	WO	0x0	PD_FIFO_OVERFL_ENSET Packet decoder FIFO overflow interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
3	WO	0x0	PD_FIFO_UNDERFL_ENSET Packet decoder FIFO underflow interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
2	WO	0x0	PD_FIFO_TH_START_PASS_ENSET Packet decoder FIFO start threshold pass interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
1	WO	0x0	PD_FIFO_TH_MAX_PASS_ENSET Packet decoder FIFO maximum threshold pass interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
0	WO	0x0	PD_FIFO_TH_MIN_PASS_ENSET Packet decoder FIFO minimum threshold pass interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

HDMI_RX_PDEC_ISTS

Address: Operational Base + offset (0x0f80)

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Bit	Attr	Reset Value	Description
31	RO	0x0	DRM_CKS_CHG_ISTS Dynamic Range and Mastering InfoFrame packet checksum change interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: DWC_HDMI_RX_20==1)
30	RO	0x0	DRM_RCV_ISTS Dynamic Range and Mastering InfoFrame packet received interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: DWC_HDMI_RX_20==1)
29	RO	0x0	AUD_TYPE_CHG_ISTS Audio type change interrupt flag status 1'b0: Inactive 1'b1: Active
28	RO	0x0	DVIDET_ISTS DVI mode detected interrupt flag status 1'b0: Inactive 1'b1: Active
27	RO	0x0	VSI_CKS_CHG_ISTS VSI checksum change interrupt flag status 1'b0: Inactive 1'b1: Active
26	RO	0x0	GMD_CKS_CHG_ISTS GMD (gamut meta data) checksum change interrupt flag status 1'b0: Inactive 1'b1: Active
25	RO	0x0	AIF_CKS_CHG_ISTS AIF checksum change interrupt flag status 1'b0: Inactive 1'b1: Active
24	RO	0x0	AVI_CKS_CHG_ISTS AVI checksum change interrupt flag status 1'b0: Inactive 1'b1: Active
23	RO	0x0	ACR_N_CHG_ISTS ACR N value change interrupt flag status 1'b0: Inactive 1'b1: Active
22	RO	0x0	ACR_CTS_CHG_ISTS ACR CTS value change interrupt flag status 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
21	RO	0x0	GCP_AV_MUTE_CHG_ISTS GCP AVMUTE change interrupt flag status 1'b0: Inactive 1'b1: Active
20	RO	0x0	GMD_RCV_ISTS GMD (gamut meta data) packet received interrupt flag status 1'b0: Inactive 1'b1: Active
19	RO	0x0	AIF_RCV_ISTS AIF packet received interrupt flag status 1'b0: Inactive 1'b1: Active
18	RO	0x0	AVI_RCV_ISTS AVI packet received interrupt flag status 1'b0: Inactive 1'b1: Active
17	RO	0x0	ACR_RCV_ISTS ACR packet received interrupt flag status 1'b0: Inactive 1'b1: Active
16	RO	0x0	GCP_RCV_ISTS GCP packet received interrupt flag status 1'b0: Inactive 1'b1: Active
15	RO	0x0	VSI_RCV_ISTS VSI packet received interrupt flag status 1'b0: Inactive 1'b1: Active
14	RO	0x0	AMP_RCV_ISTS Audio multi stream packet received interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: DWC_HDMI_RX_20==1)
13	RO	0x0	AMP_CHG_ISTS Audio Multistream packet checksum change interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: DWC_HDMI_RX_20==1)
12	RO	0x0	NTSCVBI_CKS_CHG_ISTS NTSC VBI packet checksum change interrupt flag status 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
11	RO	0x0	NTSCVBI_RCV_ISTS NTSC VBI packet received interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
10:9	RO	0x0	reserved
8	RO	0x0	PD_FIFO_NEW_ENTRY_ISTS Packet decoder FIFO new entry interrupt flag status 1'b0: Inactive 1'b1: Active
7:5	RO	0x0	reserved
4	RO	0x0	PD_FIFO_OVERFL_ISTS Packet decoder FIFO overflow interrupt flag status 1'b0: Inactive 1'b1: Active
3	RO	0x0	PD_FIFO_UNDERFL_ISTS Packet decoder FIFO underflow interrupt flag status 1'b0: Inactive 1'b1: Active
2	WO	0x0	PD_FIFO_TH_START_PASS_ISTS Packet decoder FIFO start threshold pass interrupt flag status 1'b0: Inactive 1'b1: Active
1	RO	0x0	PD_FIFO_TH_MAX_PASS_ISTS Packet decoder FIFO maximum threshold pass interrupt flag status 1'b0: Inactive 1'b1: Active
0	RO	0x0	PD_FIFO_TH_MIN_PASS_ISTS Packet decoder FIFO minimum threshold pass interrupt flag status 1'b0: Inactive 1'b1: Active

HDMI_RX_PDEC_IEN

Address: Operational Base + offset (0x0f84)

Bit	Attr	Reset Value	Description
31	RO	0x0	DRM_CKS_CHG_IEN Dynamic Range and Mastering InfoFrame packet checksum change interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: DWC_HDMI_RX_20==1)

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Bit	Attr	Reset Value	Description
30	RO	0x0	DRM_RCV_IEN Dynamic Range and Mastering InfoFrame packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: DWC_HDMI_RX_20==1)
29	RO	0x0	AUD_TYPE_CHG_IEN Audio type change interrupt enable status 1'b0: Disabled 1'b1: Enabled
28	RO	0x0	DVIDET_IEN DVI mode detected interrupt enable status 1'b0: Disabled 1'b1: Enabled
27	RO	0x0	VSI_CKS_CHG_IEN VSI checksum change interrupt enable status 1'b0: Disabled 1'b1: Enabled
26	RO	0x0	GMD_CKS_CHG_IEN GMD (gamut meta data) checksum change interrupt enable status 1'b0: Disabled 1'b1: Enabled
25	RO	0x0	AIF_CKS_CHG_IEN AIF checksum change interrupt enable status 1'b0: Disabled 1'b1: Enabled
24	RO	0x0	AVI_CKS_CHG_IEN AVI checksum change interrupt enable status 1'b0: Disabled 1'b1: Enabled
23	RO	0x0	ACR_N_CHG_IEN ACR N value change interrupt enable status 1'b0: Disabled 1'b1: Enabled
22	RO	0x0	ACR_CTS_CHG_IEN ACR CTS value change interrupt enable status 1'b0: Disabled 1'b1: Enabled
21	RO	0x0	GCP_AV_MUTE_CHG_IEN GCP AVMUTE change interrupt enable status 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
20	RO	0x0	GMD_RCV_IEN GMD (gamut meta data) packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled
19	RO	0x0	AIF_RCV_IEN AIF packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled
18	RO	0x0	AVI_RCV_IEN AVI packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled
17	RO	0x0	ACR_RCV_IEN ACR packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled
16	RO	0x0	GCP_RCV_IEN GCP packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled
15	RO	0x0	VSI_RCV_IEN VSI packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled
14	RO	0x0	AMP_RCV_IEN Audio multi stream packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: DWC_HDMI_RX_20==1)
13	RO	0x0	AMP_CHG_IEN Audio Multistream packet checksum change interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: DWC_HDMI_RX_20==1)
12	RO	0x0	NTSCVBI_CKS_CHG_IEN NTSC VBI packet checksum change interrupt enable status 1'b0: Disabled 1'b1: Enabled
11	RO	0x0	NTSCVBI_RCV_IEN NTSC VBI packet received interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
10:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RO	0x0	PD_FIFO_NEW_ENTRY_IEN Packet decoder FIFO new entry interrupt enable status 1'b0: Disabled 1'b1: Enabled
7:5	RO	0x0	reserved
4	RO	0x0	PD_FIFO_OVERFL_IEN Packet decoder FIFO overflow interrupt enable status 1'b0: Disabled 1'b1: Enabled
3	RO	0x0	PD_FIFO_UNDERFL_IEN Packet decoder FIFO underflow interrupt enable status 1'b0: Disabled 1'b1: Enabled
2	WO	0x0	PD_FIFO_TH_START_PASS_IEN Packet decoder FIFO start threshold pass interrupt enable status 1'b0: Disabled 1'b1: Enabled
1	RO	0x0	PD_FIFO_TH_MAX_PASS_IEN Packet decoder FIFO maximum threshold pass interrupt enable status 1'b0: Disabled 1'b1: Enabled
0	RO	0x0	PD_FIFO_TH_MIN_PASS_IEN Packet decoder FIFO minimum threshold pass interrupt enable status 1'b0: Disabled 1'b1: Enabled

HDMI_RX_PDEC_ICLR

Address: Operational Base + offset (0x0f88)

Bit	Attr	Reset Value	Description
31	RO	0x0	DRM_CKS_CHG_ICLR Dynamic Range and Mastering InfoFrame packet checksum change interrupt flag clear 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)
30	RO	0x0	DRM_RCV_ICLR Dynamic Range and Mastering InfoFrame packet received interrupt flag clear 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)

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Bit	Attr	Reset Value	Description
29	RO	0x0	AUD_TYPE_CHG_ICLR Audio type change interrupt flag clear 1'b0: No action 1'b1: Action
28	RO	0x0	DVIDET_ICLR DVI mode detected interrupt flag clear 1'b0: No action 1'b1: Action
27	RO	0x0	VSI_CKS_CHG_ICLR VSI checksum change interrupt flag clear 1'b0: No action 1'b1: Action
26	RO	0x0	GMD_CKS_CHG_ICLR GMD (gamut meta data) checksum change interrupt flag clear 1'b0: No action 1'b1: Action
25	RO	0x0	AIF_CKS_CHG_ICLR AIF checksum change interrupt flag clear 1'b0: No action 1'b1: Action
24	RO	0x0	AVI_CKS_CHG_ICLR AVI checksum change interrupt flag clear 1'b0: No action 1'b1: Action
23	RO	0x0	ACR_N_CHG_ICLR ACR N value change interrupt flag clear 1'b0: No action 1'b1: Action
22	RO	0x0	ACR_CTS_CHG_ICLR ACR CTS value change interrupt flag clear 1'b0: No action 1'b1: Action
21	RO	0x0	GCP_AV_MUTE_CHG_ICLR GCP AVMUTE change interrupt flag clear 1'b0: No action 1'b1: Action
20	RO	0x0	GMD_RCV_ICLR GMD (gamut meta data) packet received interrupt flag clear 1'b0: No action 1'b1: Action
19	RO	0x0	AIF_RCV_ICLR AIF packet received interrupt flag clear 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
18	RO	0x0	AVI_RCV_ICLR AVI packet received interrupt flag clear 1'b0: No action 1'b1: Action
17	RO	0x0	ACR_RCV_ICLR ACR packet received interrupt flag clear 1'b0: No action 1'b1: Action
16	RO	0x0	GCP_RCV_ICLR GCP packet received interrupt flag clear 1'b0: No action 1'b1: Action
15	RO	0x0	VSI_RCV_ICLR VSI packet received interrupt flag clear 1'b0: No action 1'b1: Action
14	RO	0x0	AMP_RCV_ICLR Audio multi stream packet received interrupt flag clear 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)
13	RO	0x0	AMP_CHG_ICLR Audio Multi stream packet checksum change interrupt flag clear 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)
12	RO	0x0	NTSCVBI_CKS_CHG_ICLR NTSC VBI packet checksum change interrupt flag clear 1'b0: No action 1'b1: Action
11	RO	0x0	NTSCVBI_RCV_ICLR NTSC VBI packet received interrupt flag clear 1'b0: No action 1'b1: Action (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
10:9	RO	0x0	reserved
8	RO	0x0	PD_FIFO_NEW_ENTRY_ICLR Packet decoder FIFO new entry interrupt flag clear 1'b0: No action 1'b1: Action
7:5	RO	0x0	reserved
4	RO	0x0	PD_FIFO_OVERFL_ICLR Packet decoder FIFO overflow interrupt flag clear 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
3	RO	0x0	PD_FIFO_UNDERFL_ICLR Packet decoder FIFO underflow interrupt flag clear 1'b0: No action 1'b1: Action
2	WO	0x0	PD_FIFO_TH_START_PASS_ICLR Packet decoder FIFO start threshold pass interrupt flag clear 1'b0: No action 1'b1: Action
1	RO	0x0	PD_FIFO_TH_MAX_PASS_ICLR Packet decoder FIFO maximum threshold pass interrupt flag clear 1'b0: No action 1'b1: Action
0	RO	0x0	PD_FIFO_TH_MIN_PASS_ICLR Packet decoder FIFO minimum threshold pass interrupt flag clear 1'b0: No action 1'b1: Action

HDMI_RX_PDEC_ISET

Address: Operational Base + offset (0x0f8c)

Bit	Attr	Reset Value	Description
31	WO	0x0	DRM_CKS_CHG_ISET Dynamic Range and Mastering InfoFrame packet checksum change interrupt set 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)
30	WO	0x0	DRM_RCV_ISET Dynamic Range and Mastering InfoFrame packet received interrupt set 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)
29	WO	0x0	AUD_TYPE_CHG_ISET Audio type change interrupt set 1'b0: No action 1'b1: Action
28	WO	0x0	DVIDET_ISET DVI mode detected interrupt set 1'b0: No action 1'b1: Action
27	WO	0x0	VSI_CKS_CHG_ISET VSI checksum change interrupt set 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
26	WO	0x0	GMD_CKS_CHG_ISET GMD (gamut meta data) checksum change interrupt set 1'b0: No action 1'b1: Action
25	WO	0x0	AIF_CKS_CHG_ISET AIF checksum change interrupt set 1'b0: No action 1'b1: Action
24	WO	0x0	AVI_CKS_CHG_ISET AVI checksum change interrupt set 1'b0: No action 1'b1: Action
23	WO	0x0	ACR_N_CHG_ISET ACR N value change interrupt set 1'b0: No action 1'b1: Action
22	WO	0x0	ACR_CTS_CHG_ISET ACR CTS value change interrupt set 1'b0: No action 1'b1: Action
21	WO	0x0	GCP_AV_MUTE_CHG_ISET GCP AVMUTE change interrupt set 1'b0: No action 1'b1: Action
20	WO	0x0	GMD_RCV_ISET GMD (gamut meta data) packet received interrupt set 1'b0: No action 1'b1: Action
19	WO	0x0	AIF_RCV_ISET AIF packet received interrupt set 1'b0: No action 1'b1: Action
18	WO	0x0	AVI_RCV_ISET AVI packet received interrupt set 1'b0: No action 1'b1: Action
17	WO	0x0	ACR_RCV_ISET ACR packet received interrupt set 1'b0: No action 1'b1: Action
16	WO	0x0	GCP_RCV_ISET GCP packet received interrupt set 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
15	WO	0x0	VSI_RCV_ISET VSI packet received interrupt set 1'b0: No action 1'b1: Action
14	WO	0x0	AMP_RCV_ISET Audio multi stream packet received interrupt set 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)
13	WO	0x0	AMP_CHG_ISET Audio Multi stream packet checksum change interrupt set 1'b0: No action 1'b1: Action (Exists: DWC_HDMI_RX_20==1)
12	WO	0x0	NTSCVBI_CKS_CHG_ISET NTSC VBI packet checksum change interrupt set 1'b0: No action 1'b1: Action
11	WO	0x0	NTSCVBI_RCV_ISET NTSC VBI packet received interrupt set 1'b0: No action 1'b1: Action (Exists: (DWC_HDMI_RX_20==1 || DWC_HDMI_RX_MHL==1))
10:9	RO	0x0	reserved
8	WO	0x0	PD_FIFO_NEW_ENTRY_ISET Packet decoder FIFO new entry interrupt set 1'b0: No action 1'b1: Action
7:5	RO	0x0	reserved
4	WO	0x0	PD_FIFO_OVERFL_ISET Packet decoder FIFO overflow interrupt set 1'b0: No action 1'b1: Action
3	WO	0x0	PD_FIFO_UNDERFL_ISET Packet decoder FIFO underflow interrupt set 1'b0: No action 1'b1: Action
2	WO	0x0	PD_FIFO_TH_START_PASS_ISET Packet decoder FIFO start threshold pass interrupt set 1'b0: No action 1'b1: Action
1	WO	0x0	PD_FIFO_TH_MAX_PASS_ISET Packet decoder FIFO maximum threshold pass interrupt set 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
0	WO	0x0	PD_FIFO_TH_MIN_PASS_ISET Packet decoder FIFO minimum threshold pass interrupt set 1'b0: No action 1'b1: Action

HDMI_RX_AUD_CEC_IEN_CLR

Address: Operational Base + offset (0x0f90)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	WO	0x0	WAKEUPCTRL_ENCLR CEC Wake-up interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HDMIRXCEC==1)
21	WO	0x0	ERROR_FOLL_ENCLR CEC Follower Error interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. Exists: HDMIRXCEC==1
20	WO	0x0	ERROR_INIT_ENCLR CEC Initiator Error interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. Exists: HDMIRXCEC==1
19	WO	0x0	ARBLST_ENCLR CEC Arbitration Loss interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HDMIRXCEC==1)
18	WO	0x0	NACK_ENCLR CEC Not Acknowledge interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HDMIRXCEC==1)
17	WO	0x0	EOM_ENCLR CEC End Of Message interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HDMIRXCEC==1)
16	WO	0x0	DONE_ENCLR CEC done interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0. (Exists: HDMIRXCEC==1)
15:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	WO	0x0	SCK_STABLE_ENCLR Audio PLL stable interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
0	WO	0x0	CTSN_CNT_ENCLR CTS/N updated interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

HDMI_RX_AUD_CEC_IEN_SET

Address: Operational Base + offset (0x0f94)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	WO	0x0	WAKEUPCTRL_ENSET CEC Wake-up interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: HDMIRXCEC==1)
21	WO	0x0	ERROR_FOLL_ENSET CEC Follower Error interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: HDMIRXCEC==1
20	WO	0x0	ERROR_INIT_ENSET CEC Initiator Error interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: HDMIRXCEC==1
19	WO	0x0	ARBLST_ENSET CEC Arbitration Loss interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: HDMIRXCEC==1)
18	WO	0x0	NACK_ENSET CEC Not Acknowledge interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: HDMIRXCEC==1)
17	WO	0x0	EOM_ENSET CEC End Of Message interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: HDMIRXCEC==1)

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Bit	Attr	Reset Value	Description
16	WO	0x0	DONE_ENSET CEC done interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. (Exists: HDMIRXCEC==1)
15:2	RO	0x0	reserved
1	WO	0x0	SCK_STABLE_ENSET Audio PLL stable interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
0	WO	0x0	CTSN_CNT_ENSET CTS/N updated interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

HDMI_RX_AUD_CEC_ISTS

Address: Operational Base + offset (0x0f98)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RO	0x0	WAKEUPCTRL_ISTS CEC Wake-up interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HDMIRXCEC==1)
21	RO	0x0	ERROR_FOLL_ISTS CEC Follower Error interrupt flag status 1'b0: Inactive 1'b1: Active Exists: HDMIRXCEC==1
20	RO	0x0	ERROR_INIT_ISTS CEC Initiator Error interrupt flag status 1'b0: Inactive 1'b1: Active Exists: HDMIRXCEC==1
19	RO	0x0	ARBLST_ISTS CEC Arbitration Loss interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HDMIRXCEC==1)
18	RO	0x0	NACK_ISTS CEC Not Acknowledge interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HDMIRXCEC==1)

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Bit	Attr	Reset Value	Description
17	RO	0x0	EOM_ISTS CEC End Of Message interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HDMIRXCEC==1)
16	RO	0x0	DONE_ISTS CEC done interrupt flag status 1'b0: Inactive 1'b1: Active (Exists: HDMIRXCEC==1)
15:2	RO	0x0	reserved
1	RO	0x0	SCK_STABLE_ISTS Audio PLL stable interrupt flag status 1'b0: Inactive 1'b1: Active
0	RO	0x0	CTSN_CNT_ISTS CTS/N updated interrupt flag status 1'b0: Inactive 1'b1: Active

HDMI_RX_AUD_CEC_IEN

Address: Operational Base + offset (0x0f9c)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RO	0x0	WAKEUPCTRL_IEN CEC Wake-up interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: HDMIRXCEC==1)
21	RO	0x0	ERROR_FOLL_IEN CEC Follower Error interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: HDMIRXCEC==1
20	RO	0x0	ERROR_INIT_IEN CEC Initiator Error interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: HDMIRXCEC==1
19	RO	0x0	ARBLST_IEN CEC Arbitration Loss interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: HDMIRXCEC==1)

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Bit	Attr	Reset Value	Description
18	RO	0x0	NACK_IEN CEC Not Acknowledge interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: HDMIRXCEC==1)
17	RO	0x0	EOM_IEN CEC End Of Message interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: HDMIRXCEC==1)
16	RO	0x0	DONE_IEN CEC done interrupt enable status 1'b0: Disabled 1'b1: Enabled (Exists: HDMIRXCEC==1)
15:2	RO	0x0	reserved
1	RO	0x0	SCK_STABLE_IEN Audio PLL stable interrupt enable status 1'b0: Disabled 1'b1: Enabled
0	RO	0x0	CTSN_CNT_IEN CTS/N updated interrupt enable status 1'b0: Disabled 1'b1: Enabled

HDMI_RX_AUD_CEC_ICLR

Address: Operational Base + offset (0x0fa0)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	WO	0x0	WAKEUPCTRL_CLR CEC Wake-up interrupt flag clear 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
21	WO	0x0	ERROR_FOLL_CLR CEC Follower Error interrupt flag clear 1'b0: No action 1'b1: Action Exists: HDMIRXCEC==1
20	WO	0x0	ERROR_INIT_CLR CEC Initiator Error interrupt flag clear 1'b0: No action 1'b1: Action Exists: HDMIRXCEC==1

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Bit	Attr	Reset Value	Description
19	WO	0x0	ARBLST_CLR CEC Arbitration Loss interrupt flag clear 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
18	WO	0x0	NACK_CLR CEC Not Acknowledge interrupt flag clear 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
17	WO	0x0	EOM_CLR CEC End Of Message interrupt flag clear 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
16	WO	0x0	DONE_CLR CEC done interrupt flag clear 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
15:2	RO	0x0	reserved
1	WO	0x0	SCK_STABLE_CLR Audio PLL stable interrupt flag clear 1'b0: No action 1'b1: Action
0	WO	0x0	CTSN_CNT_CLR CTS/N updated interrupt flag clear 1'b0: No action 1'b1: Action

HDMI_RX_AUD_CEC_ISET

Address: Operational Base + offset (0x0fa4)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	WO	0x0	WAKEUPCTRL_SET CEC Wake-up interrupt 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
21	WO	0x0	ERROR_FOLL_SET CEC Follower Error interrupt 1'b0: No action 1'b1: Action Exists: HDMIRXCEC==1

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Bit	Attr	Reset Value	Description
20	WO	0x0	ERROR_INIT_SET CEC Initiator Error interrupt 1'b0: No action 1'b1: Action Exists: HDMIRXCEC==1
19	WO	0x0	ARBLST_SET CEC Arbitration Loss interrupt 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
18	WO	0x0	NACK_SET CEC Not Acknowledge interrupt 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
17	WO	0x0	EOM_SET CEC End Of Message interrupt 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
16	WO	0x0	DONE_SET CEC done interrupt 1'b0: No action 1'b1: Action (Exists: HDMIRXCEC==1)
15:2	RO	0x0	reserved
1	WO	0x0	SCK_STABLE_SET Audio PLL stable interrupt 1'b0: No action 1'b1: Action
0	WO	0x0	CTSN_CNT_SET CTS/N updated interrupt 1'b0: No action 1'b1: Action

HDMI_RX_AUD_FIFO_IEN_CLR

Address: Operational Base + offset (0x0fa8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	WO	0x0	AFIF_OVERFL_ENCLR Audio FIFO overflow interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

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Bit	Attr	Reset Value	Description
3	WO	0x0	AFIF_UNDERFL_ENCLR Audio FIFO underflow interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
2	WO	0x0	AFIF_THS_PASS_ENCLR Audio FIFO start threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
1	WO	0x0	AFIF_TH_MAX_ENCLR Audio FIFO maximum threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
0	WO	0x0	AFIF_TH_MIN_ENCLR Audio FIFO minimum threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

HDMI_RX_AUD_FIFO_IEN_SET

Address: Operational Base + offset (0x0fac)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	WO	0x0	AFIF_OVERFL_ENSET Audio FIFO overflow interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
3	WO	0x0	AFIF_UNDERFL_ENSET Audio FIFO underflow interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
2	WO	0x0	AFIF_THS_PASS_ENSET Audio FIFO start threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
1	WO	0x0	AFIF_TH_MAX_ENSET Audio FIFO maximum threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
0	WO	0x0	AFIF_TH_MIN_ENSET Audio FIFO minimum threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

HDMI_RX_AUD_FIFO_ISTS

Address: Operational Base + offset (0x0fb0)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	AFIF_OVERFL_ISTS Audio FIFO overflow interrupt flag status 1'b0: Inactive 1'b1: Active
3	RO	0x0	AFIF_UNDERFL_ISTS Audio FIFO underflow interrupt flag status 1'b0: Inactive 1'b1: Active
2	RO	0x0	AFIF_THS_PASS_ISTS Audio FIFO start threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
1	RO	0x0	AFIF_TH_MAX_ISTS Audio FIFO maximum threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
0	RO	0x0	AFIF_TH_MIN_ISTS Audio FIFO minimum threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active

HDMI_RX_AUD_FIFO_IEN

Address: Operational Base + offset (0x0fb4)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	AFIF_OVERFL_IEN Audio FIFO overflow interrupt enable status 1'b0: Disabled 1'b1: Enabled
3	RO	0x0	AFIF_UNDERFL_IEN Audio FIFO underflow interrupt enable status 1'b0: Disabled 1'b1: Enabled
2	RO	0x0	AFIF_THS_PASS_IEN Audio FIFO start threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
1	RO	0x0	AFIF_TH_MAX_IEN Audio FIFO maximum threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
0	RO	0x0	AFIF_TH_MIN_IEN Audio FIFO minimum threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled

HDMI_RX_AUD_FIFO_ICLR

Address: Operational Base + offset (0x0fb8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	WO	0x0	AFIF_OVERFL_CLR Audio FIFO overflow interrupt flag clear 1'b0: No action 1'b1: Action
3	WO	0x0	AFIF_UNDERFL_CLR Audio FIFO underflow interrupt flag clear 1'b0: No action 1'b1: Action
2	WO	0x0	AFIF_THS_PASS_CLR Audio FIFO start threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
1	WO	0x0	AFIF_TH_MAX_CLR Audio FIFO maximum threshold passed interrupt flag clear 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
0	WO	0x0	AFIF_TH_MIN_CLR Audio FIFO minimum threshold passed interrupt flag clear 1'b0: No action 1'b1: Action

HDMI_RX_AUD_FIFO_ISET

Address: Operational Base + offset (0x0fbc)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	WO	0x0	AFIF_OVERFL_SET Audio FIFO overflow interrupt set 1'b0: No action 1'b1: Action
3	WO	0x0	AFIF_UNDERFL_SET Audio FIFO underflow interrupt set 1'b0: No action 1'b1: Action
2	WO	0x0	AFIF_THS_PASS_SET Audio FIFO start threshold passed interrupt set 1'b0: No action 1'b1: Action
1	WO	0x0	AFIF_TH_MAX_SET Audio FIFO maximum threshold passed interrupt set 1'b0: No action 1'b1: Action
0	WO	0x0	AFIF_TH_MIN_SET Audio FIFO minimum threshold passed interrupt set 1'b0: No action 1'b1: Action

HDMI_RX_MD_IEN_CLR

Address: Operational Base + offset (0x0fc0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	WO	0x0	VOFS_LIN_ENCLR vofs_lin_ith interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
10	WO	0x0	VTOT_LIN_ENCLR vtot_lin_ith interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

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Bit	Attr	Reset Value	Description
9	WO	0x0	VACT_LIN_ENCLR vact_lin_ith interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
8	WO	0x0	VS_CLK_ENCLR vs_clk_ists interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
7	WO	0x0	VTOT_CLK_ENCLR vtot_clk_ists interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
6	WO	0x0	HACT_PIX_ENCLR hact_pix_ists interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
5	WO	0x0	HS_CLK_ENCLR hs_clk_ists interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
4	WO	0x0	HTOT32_CLK_ENCLR htot32_clk_ists interrupt threshold passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
3	WO	0x0	ILACE_ENCLR Interlaced mode active interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
2	RW	0x0	DE_ACTIVITY_ENCLR Data enable active interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
1	WO	0x0	VS_ACT_ENCLR Vsync active interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
0	WO	0x0	HS_ACT_ENCLR Hsync active interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

HDMI_RX_MD_IEN_SET

Address: Operational Base + offset (0x0fc4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	WO	0x0	VOFS_LIN_ENSET vofs_lin_ith interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
10	WO	0x0	VTOT_LIN_ENSET vtot_lin_ith interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
9	WO	0x0	VACT_LIN_ENSET vact_lin_ith interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
8	WO	0x0	VS_CLK_ENSET vs_clk_ists interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
7	WO	0x0	VTOT_CLK_ENSET vtot_clk_ists interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
6	WO	0x0	HACT_PIX_ENSET hact_pix_ists interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
5	WO	0x0	HS_CLK_ENSET hs_clk_ists interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
4	WO	0x0	HTOT32_CLK_ENSET htot32_clk_ists interrupt threshold passed interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
3	WO	0x0	ILACE_ENSET Interlaced mode active interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
2	RW	0x0	DE_ACTIVITY_ENSET Data enable active interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
1	WO	0x0	VS_ACT_ENSET Vsync active interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

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Bit	Attr	Reset Value	Description
0	WO	0x0	HS_ACT_ENSET Hsync active interrupt - Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

HDMI_RX_MD_ISTS

Address: Operational Base + offset (0x0fc8)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RO	0x0	VOFS_LIN_ISTS vofs_lin_ith interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
10	RO	0x0	VTOT_LIN_ISTS vtot_lin_ith interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
9	RO	0x0	VACT_LIN_ISTS vact_lin_ith interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
8	RO	0x0	VS_CLK_ISTS vs_clk_ists interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
7	RO	0x0	VTOT_CLK_ISTS vtot_clk_ists interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
6	RO	0x0	HACT_PIX_ISTS hact_pix_ists interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
5	RO	0x0	HS_CLK_ISTS hs_clk_ists interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
4	RO	0x0	HTOT32_CLK_ISTS htot32_clk_ists interrupt threshold passed interrupt flag status 1'b0: Inactive 1'b1: Active
3	RO	0x0	ILACE_ISTS Interlaced mode active interrupt flag status 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
2	RO	0x0	DE_ACTIVITY_ISTS Data enable active interrupt flag status 1'b0: Inactive 1'b1: Active
1	RO	0x0	VS_ACT_ISTS Vsync active interrupt flag status 1'b0: Inactive 1'b1: Active
0	RO	0x0	HS_ACT_ISTS Hsync active interrupt flag status 1'b0: Inactive 1'b1: Active

HDMI_RX_MD_IEN

Address: Operational Base + offset (0x0fcc)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RO	0x0	VOFS_LIN_IEN vofs_lin_ith interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
10	RO	0x0	VTOT_LIN_IEN vtot_lin_ith interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
9	RO	0x0	VACT_LIN_IEN vact_lin_ith interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
8	RO	0x0	VS_CLK_IEN vs_clk_ists interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
7	RO	0x0	VTOT_CLK_IEN vtot_clk_ists interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
6	RO	0x0	HACT_PIX_IEN hact_pix_ists interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
5	RO	0x0	HS_CLK_IEN hs_clk_ists interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
4	RO	0x0	HTOT32_CLK_IEN htot32_clk_ists interrupt threshold passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
3	RO	0x0	ILACE_IEN Interlaced mode active interrupt enable status 1'b0: Disabled 1'b1: Enabled
2	RO	0x0	DE_ACTIVITY_IEN Data enable active interrupt enable status 1'b0: Disabled 1'b1: Enabled
1	RO	0x0	VS_ACT_IEN Vsync active interrupt enable status 1'b0: Disabled 1'b1: Enabled
0	RO	0x0	HS_ACT_IEN Hsync active interrupt enable status 1'b0: Disabled 1'b1: Enabled

HDMI_RX_MD_ICLR

Address: Operational Base + offset (0x0fd0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	WO	0x0	VOFS_LIN_CLR vofs_lin_ith interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
10	WO	0x0	VTOT_LIN_CLR vtot_lin_ith interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
9	WO	0x0	VACT_LIN_CLR vact_lin_ith interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
8	WO	0x0	VS_CLK_CLR vs_clk_ists interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
7	WO	0x0	VTOT_CLK_CLR vtot_clk_ists interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
6	WO	0x0	HACT_PIX_CLR hact_pix_ists interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
5	WO	0x0	HS_CLK_CLR hs_clk_ists interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
4	WO	0x0	HTOT32_CLK_CLR htot32_clk_ists interrupt threshold passed interrupt flag clear 1'b0: No action 1'b1: Action
3	WO	0x0	ILACE_CLR Interlaced mode active interrupt flag clear 1'b0: No action 1'b1: Action
2	WO	0x0	DE_ACTIVITY_CLR Data enable active interrupt flag clear 1'b0: No action 1'b1: Action
1	WO	0x0	VS_ACT_CLR Vsync active interrupt flag clear 1'b0: No action 1'b1: Action
0	WO	0x0	HS_ACT_CLR Hsync active interrupt flag clear 1'b0: No action 1'b1: Action

HDMI_RX_MD_ISET

Address: Operational Base + offset (0x0fd4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	WO	0x0	VOFS_LIN_SET vofs_lin_ith interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action
10	WO	0x0	VTOT_LIN_SET vtot_lin_ith interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action
9	WO	0x0	VACT_LIN_SET vact_lin_ith interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
8	WO	0x0	VS_CLK_SET vs_clk_ists interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action
7	WO	0x0	VTOT_CLK_SET vtot_clk_ists interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action
6	WO	0x0	HACT_PIX_SET hact_pix_ists interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action
5	WO	0x0	HS_CLK_SET hs_clk_ists interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action
4	WO	0x0	HTOT32_CLK_SET htot32_clk_ists interrupt threshold passed interrupt set 1'b0: No action 1'b1: Action
3	WO	0x0	ILACE_SET Interlaced mode active interrupt set 1'b0: No action 1'b1: Action
2	WO	0x0	DE_ACTIVITY_SET Data enable active interrupt set 1'b0: No action 1'b1: Action
1	WO	0x0	VS_ACT_SET Vsync active interrupt flag set 1'b0: No action 1'b1: Action
0	WO	0x0	HS_ACT_SET Hsync active interrupt set 1'b0: No action 1'b1: Action

HDMI_RX_HDMI_IEN_CLR

Address: Operational Base + offset (0x0fd8)

Bit	Attr	Reset Value	Description
31	WO	0x0	HDCP_DKSET_DONE_ENCLR HDCP Device Key Set read operation done interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: HDCP_DKSET_EXT==1

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Bit	Attr	Reset Value	Description
30	WO	0x0	I2CMP_ARBLOST_ENCLR I2C master PHY arbitration lost interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
29	RW	0x0	I2CMPNACK_ENCLR I2C master PHY NACK interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
28	WO	0x0	I2CMPDONE_ENCLR I2C master PHY done interrupt - Enable clear, 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
27	WO	0x0	VS_THR_REACHED_ENCLR Vertical sync threshold reached interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
26	WO	0x0	VSYNC_ACT_EDGE_ENCLR Vsync active edge interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
25	WO	0x0	AKSV_RCV_ENCLR AKSV received interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
24	WO	0x0	PLL_CLOCK_GATED_ENCLR PLL clock gated interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
23	WO	0x0	DESER_MISAL_ENCLR Deserializer misalignment interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: DWC_HDMI_RX_MHL==1

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Bit	Attr	Reset Value	Description
22	WO	0x0	CDSENSE_CHG_ENCLR cdsense change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: DWCHDMIRXMHL==1
21	WO	0x0	CEAVID_EMPTY_ENCLR CEA video FIFO empty interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: HRX_CEAVIDOUT==1
20	WO	0x0	CEAVID_FULL_ENCLR CEA video FIFO full interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: HRX_CEAVIDOUT==1
19	WO	0x0	SCDCTMDSCFGCHANGE_ENC SDCD TMDS Configuration register change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: DWC_HDMI_RX_20==1
18	WO	0x0	SCDCSCSTATUSCHANGE_ENC SCDC Scrambling_Status change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: DWC_HDMI_RX_20==1
17	WO	0x0	SCDCCFGCHANGE_ENCLR SDCD Configuration register change interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: DWC_HDMI_RX_20==1
16	WO	0x0	DCM_CURRENT_MODE_CHG_ENCLR Deep color mode changed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
15	WO	0x0	DCM_PH_DIFF_CNT_OVERFL_ENCLR Threshold on maximum number of phase re-alignment passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

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Bit	Attr	Reset Value	Description
14	WO	0x0	DCM_GCP_ZERO_FIELDS_PASS_ENCLR Number of video fields with receiving GCPs with CD=0 OR CD=reserved information before switching back to 24bit mode passed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
13	WO	0x0	CTL3_CHANGE_ENCLR HDMI CTL3 line changed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
12	WO	0x0	CTL2_CHANGE_ENCLR HDMI CTL2 line changed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
11	WO	0x0	CTL1_CHANGE_ENCLR HDMI CTL1 line changed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
10	WO	0x0	CTL0_CHANGE_ENCLR HDMI CTL0 line changed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
9	WO	0x0	VS_POL_ADJ_ENCLR VS polarity adjust status interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
8	WO	0x0	HS_POL_ADJ_ENCLR HS polarity adjust status interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
7	WO	0x0	RES_OVERLOAD_ENCLR RES overload state from PHY interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
6	WO	0x0	CLK_CHANGE_ENCLR Clock rate changed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
5	WO	0x0	PLL_LCK_CHG_ENCLR PHY PLL lock state changed interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

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Bit	Attr	Reset Value	Description
4	WO	0x0	EQGAIN_DONE_ENCLR EQ gain done from PHY interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
3	WO	0x0	OFFSCAL_DONE_ENCLR offscal done from PHY interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
2	WO	0x0	RESCAL_DONE_ENCLR rescal done from PHY interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
1	WO	0x0	ACT_CHANGE_ENCLR Activity state changed (activity detection signal from PHY) interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0
0	WO	0x0	STATE_REACHED_ENCLR PHY state_reached interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0

HDMI_RX_HDMI_IEN_SET

Address: Operational Base + offset (0x0fdc)

Bit	Attr	Reset Value	Description
31	WO	0x0	HDCP_DKSET_DONE_ENCLR HDCP Device Key Set read operation done interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: HDCP_DKSET_EXT==1
30	WO	0x0	I2CMP_ARBLOST_ENCLR I2C master PHY arbitration lost interrupt - Enable clear 1'b0: No action 1'b1: Disable the interrupt. The enable status bit changes to 0 Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
29	RW	0x0	I2CMPNACK_ENSET I2C master PHY NACK interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)

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Bit	Attr	Reset Value	Description
28	WO	0x0	I2CMPDONE_ENSET I2C master PHY done interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
27	WO	0x0	VS_THR_REACHED_ENSET Vertical sync threshold reached interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
26	WO	0x0	VSYNC_ACT_EDGE_ENSET Vsync active edge interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
25	WO	0x0	AKSV_RCV_ENSET AKSV received interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
24	WO	0x0	PLL_CLOCK_GATED_ENSET PLL clock gated interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
23	WO	0x0	DESER_MISAL_ENSET Deserializer misalignment interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: DWC_HDMI_RX_MHL==1
22	WO	0x0	CDSENSE_CHG_ENSET cdsense change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: DWCHDMIRXMHL==1
21	WO	0x0	CEAVID_EMPTY_ENSET CEA video FIFO empty interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: HRX_CEAVIDOUT==1
20	WO	0x0	CEAVID_FULL_ENSET CEA video FIFO full interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: HRX_CEAVIDOUT==1

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Bit	Attr	Reset Value	Description
19	WO	0x0	SCDCTMDSCFGCHANGE_ENSET SDCD TMDS Configuration register change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: DWC_HDMI_RX_20==1
18	WO	0x0	SCDCSCSTATUSCHANGE_ENSET SCDC Scrambling_Status change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: DWC_HDMI_RX_20==1
17	WO	0x0	SCDCCFGCHANGE_ENSET SDCD Configuration register change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: DWC_HDMI_RX_20==1
16	WO	0x0	DCM_CURRENT_MODE_CHG_ENSET Deep color mode changed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
15	WO	0x0	DCM_PH_DIFF_CNT_OVERFL_ENSET Threshold on maximum number of phase re-alignment passed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
14	WO	0x0	DCM_GCP_ZERO_FIELDS_PASS_ENSET Number of video fields with receiving GCPs with CD=0 OR CD=reserved information before switching back to 24bit mode passed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
13	WO	0x0	CTL3_CHANGE_ENSET HDMI CTL3 line changed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
12	WO	0x0	CTL2_CHANGE_ENSET HDMI CTL2 line changed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
11	WO	0x0	CTL1_CHANGE_ENSET HDMI CTL1 line changed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

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Bit	Attr	Reset Value	Description
10	WO	0x0	CTL0_CHANGE_ENSET HDMI CTL0 line changed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
9	WO	0x0	VS_POL_ADJ_ENSET VS polarity adjust status interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
8	WO	0x0	HS_POL_ADJ_ENSET HS polarity adjust status interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
7	WO	0x0	RES_OVERLOAD_ENSET RES overload state from PHY interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
6	WO	0x0	CLK_CHANGE_ENSET Clock rate changed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
5	WO	0x0	PLL_LCK_CHG_ENSET PHY PLL lock state changed interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
4	WO	0x0	EQGAIN_DONE_ENSET EQ gain done from PHY interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
3	WO	0x0	OFFSCAL_DONE_ENSET offscal done from PHY interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
2	WO	0x0	RESCAL_DONE_ENSET rescal done from PHY interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
1	WO	0x0	ACT_CHANGE_ENSET Activity state changed (activity detection signal from PHY) interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1
0	WO	0x0	STATE_REACHED_ENSET PHY state_reached interrupt-Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1

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HDMI_RX_HDMI_ISTS

Address: Operational Base + offset (0x0fe0)

Bit	Attr	Reset Value	Description
31	RO	0x0	HDCP_DKSET_DONE_ISTS HDCP Device Key Set read operation done interrupt flag status 1'b0: Inactive 1'b1: Active Exists: HDCP_DKSET_EXT==1
30	RO	0x0	I2CMP_ARBLOST_ISTS I2C master PHY arbitration lost interrupt flag status 1'b0: Inactive 1'b1: Active Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
29	RO	0x0	I2CMPNACK_ISTS I2C master PHY NACK interrupt flag status 1'b0: Inactive 1'b1: Active Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
28	RO	0x0	I2CMPDONE_ISTS I2C master PHY done interrupt flag status 1'b0: Inactive 1'b1: Active Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
27	RO	0x0	VS_THR_REACHED_ISTS Vertical sync threshold reached interrupt flag status 1'b0: Inactive 1'b1: Active
26	RO	0x0	VSYNC_ACT_EDGE_ISTS Vsync active edge interrupt flag status 1'b0: Inactive 1'b1: Active
25	RO	0x0	AKSV_RCV_ISTS AKSV received interrupt flag status 1'b0: Inactive 1'b1: Active
24	RO	0x0	PLL_CLOCK_GATED_ISTS PLL clock gated interrupt flag status 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
23	RO	0x0	DESER_MISAL_ISTS Deserializer misalignment interrupt flag status 1'b0: Inactive 1'b1: Active Exists: DWC_HDMI_RX_MHL==1
22	RO	0x0	CDSENSE_CHG_ISTS cdsense change interrupt -Enable set 1'b0: No action 1'b1: Enable the interrupt. The enable status bit changes to 1. Exists: DWCHDMIRXMHL==1
21	RO	0x0	CEAVID_EMPTY_ISTS CEA video FIFO empty interrupt flag status 1'b0: Inactive 1'b1: Active Exists: HRX_CEAVIDOUT==1
20	RO	0x0	CEAVID_FULL_ISTS CEA video FIFO full interrupt flag status 1'b0: Inactive 1'b1: Active Exists: HRX_CEAVIDOUT==1
19	RO	0x0	SCDCTMDSCFGCHANGE_ISTS SDCD TMDS Configuration register change interrupt flag status 1'b0: Inactive 1'b1: Active Exists: DWC_HDMI_RX_20==1
18	RO	0x0	SCDCSCSTATUSCHANGE_ISTS SCDC Scrambling_Status change interrupt flag status 1'b0: Inactive 1'b1: Active Exists: DWC_HDMI_RX_20==1
17	RO	0x0	SCDCCFGCHANGE_ISTS SDCD Configuration register change interrupt flag status 1'b0: Inactive 1'b1: Active Exists: DWC_HDMI_RX_20==1
16	RO	0x0	DCM_CURRENT_MODE_CHG_ISTS Deep color mode changed interrupt flag status 1'b0: Inactive 1'b1: Active
15	RO	0x0	DCM_PH_DIFF_CNT_OVERFL_ISTS Threshold on maximum number of phase re-alignment passed interrupt flag status 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
14	RO	0x0	DCM_GCP_ZERO_FIELDS_PASS_ISTS Number of video fields with receiving GCPs with CD=0 OR CD=reserved information before switching back to 24bit mode passed interrupt flag status 1'b0: Inactive 1'b1: Active
13	RO	0x0	CTL3_CHANGE_ISTS HDMI CTL3 line changed interrupt flag status 1'b0: Inactive 1'b1: Active
12	RO	0x0	CTL2_CHANGE_ISTS HDMI CTL2 line changed interrupt flag status 1'b0: Inactive 1'b1: Active
11	RO	0x0	CTL1_CHANGE_ISTS HDMI CTL1 line changed interrupt flag status 1'b0: Inactive 1'b1: Active
10	RO	0x0	CTL0_CHANGE_ISTS HDMI CTL0 line changed interrupt flag status 1'b0: Inactive 1'b1: Active
9	RO	0x0	VS_POL_ADJ_ISTS VS polarity adjust status interrupt flag status 1'b0: Inactive 1'b1: Active
8	RO	0x0	HS_POL_ADJ_ISTS HS polarity adjust status interrupt flag status 1'b0: Inactive 1'b1: Active
7	RO	0x0	RES_OVERLOAD_ISTS RES overload state from PHY interrupt flag status 1'b0: Inactive 1'b1: Active
6	RO	0x0	CLK_CHANGE_ISTS Clock rate changed interrupt flag status 1'b0: Inactive 1'b1: Active
5	RO	0x0	PLL_LCK_CHG_ISTS PHY PLL lock state changed interrupt flag status 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
4	RO	0x0	EQGAIN_DONE_ISTS EQ gain done from PHY interrupt flag status 1'b0: Inactive 1'b1: Active
3	RO	0x0	OFFSCAL_DONE_ISTS offscal done from PHY interrupt flag status 1'b0: Inactive 1'b1: Active
2	RO	0x0	RESCAL_DONE_ISTS rescal done from PHY interrupt flag status 1'b0: Inactive 1'b1: Active
1	RO	0x0	ACT_CHANGE_ISTS Activity state changed (activity detection signal from PHY) interrupt flag status 1'b0: Inactive 1'b1: Active
0	RO	0x0	STATE_REACHED_ISTS PHY state_reached interrupt flag status 1'b0: Inactive 1'b1: Active

HDMI_RX_HDMI_IEN

Address: Operational Base + offset (0x0fe4)

Bit	Attr	Reset Value	Description
31	RO	0x0	HDCP_DKSET_DONE_IEN HDCP Device Key Set read operation done interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: HDCP_DKSET_EXT==1
30	RO	0x0	I2CMP_ARBLOST_IEN I2C master PHY arbitration lost interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
29	RO	0x0	I2CMPNACK_IEN I2C master PHY NACK interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)

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Bit	Attr	Reset Value	Description
28	RO	0x0	I2CMPDONE_IEN I2C master PHY done interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
27	RO	0x0	VS_THR_REACHED_IEN Vertical sync threshold reached interrupt enable status 1'b0: Disabled 1'b1: Enabled
26	RO	0x0	VSYNC_ACT_EDGE_IEN Vsync active edge interrupt enable status 1'b0: Disabled 1'b1: Enabled
25	RO	0x0	AKSV_RCV_IEN AKSV received interrupt enable status 1'b0: Disabled 1'b1: Enabled
24	RO	0x0	PLL_CLOCK_GATED_IEN PLL clock gated interrupt enable status 1'b0: Disabled 1'b1: Enabled
23	RO	0x0	DESER_MISAL_IEN Deserializer misalignment interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: DWC_HDMI_RX_MHL==1
22	RO	0x0	CDSENSE_CHG_IEN cdsense change interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: DWCHDMIRXMHL==1
21	RO	0x0	CEAVID_EMPTY_IEN CEA video FIFO empty interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: HRX_CEAVIDOUT==1
20	RO	0x0	CEAVID_FULL_IEN CEA video FIFO full interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: HRX_CEAVIDOUT==1

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Bit	Attr	Reset Value	Description
19	RO	0x0	SCDCTMDSCFGCHANGE_IEN SDCD TMDS Configuration register change interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: DWC_HDMI_RX_20==1
18	RO	0x0	SCDCSCSTATUSCHANGE_IEN SCDC Scrambling_Status change interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: DWC_HDMI_RX_20==1
17	RO	0x0	SCDCCFGCHANGE_IEN SDCD Configuration register change interrupt enable status 1'b0: Disabled 1'b1: Enabled Exists: DWC_HDMI_RX_20==1
16	RO	0x0	DCM_CURRENT_MODE_CHG_IEN Deep color mode changed interrupt enable status 1'b0: Disabled 1'b1: Enabled
15	RO	0x0	DCM_PH_DIFF_CNT_OVERFL_IEN Threshold on maximum number of phase re-alignment passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
14	RO	0x0	DCM_GCP_ZERO_FIELDS_PASS_IEN Number of video fields with receiving GCPs with CD=0 OR CD=reserved information before switching back to 24bit mode passed interrupt enable status 1'b0: Disabled 1'b1: Enabled
13	RO	0x0	CTL3_CHANGE_IEN HDMI CTL3 line changed interrupt enable status 1'b0: Disabled 1'b1: Enabled
12	RO	0x0	CTL2_CHANGE_IEN HDMI CTL2 line changed interrupt enable status 1'b0: Disabled 1'b1: Enabled
11	RO	0x0	CTL1_CHANGE_IEN HDMI CTL1 line changed interrupt enable status 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
10	RO	0x0	CTL0_CHANGE_IEN HDMI CTL0 line changed interrupt enable status 1'b0: Disabled 1'b1: Enabled
9	RO	0x0	VS_POL_ADJ_IEN VS polarity adjust status interrupt enable status 1'b0: Disabled 1'b1: Enabled
8	RO	0x0	HS_POL_ADJ_IEN HS polarity adjust status interrupt enable status 1'b0: Disabled 1'b1: Enabled
7	RO	0x0	RES_OVERLOAD_IEN RES overload state from PHY interrupt enable status 1'b0: Disabled 1'b1: Enabled
6	RO	0x0	CLK_CHANGE_IEN Clock rate changed interrupt enable status 1'b0: Disabled 1'b1: Enabled
5	RO	0x0	PLL_LCK_CHG_IEN PHY PLL lock state changed interrupt enable status 1'b0: Disabled 1'b1: Enabled
4	RO	0x0	EQGAIN_DONE_IEN EQ gain done from PHY interrupt enable status 1'b0: Disabled 1'b1: Enabled
3	RO	0x0	OFFSCAL_DONE_IEN offscal done from PHY interrupt enable status 1'b0: Disabled 1'b1: Enabled
2	RO	0x0	RESCAL_DONE_IEN rescal done from PHY interrupt enable status 1'b0: Disabled 1'b1: Enabled
1	RO	0x0	ACT_CHANGE_IEN Activity state changed (activity detection signal from PHY) interrupt enable status 1'b0: Disabled 1'b1: Enabled
0	RO	0x0	STATE_REACHED_IEN PHY state_reached interrupt enable status 1'b0: Disabled 1'b1: Enabled

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HDMI_RX_HDMI_ICLR

Address: Operational Base + offset (0x0fe8)

Bit	Attr	Reset Value	Description
31	WO	0x0	HDCP_DKSET_DONE_CLR HDCP Device Key Set read operation done interrupt flag clear 1'b0: No action 1'b1: Action Exists: HDCP_DKSET_EXT==1
30	WO	0x0	I2CMP_ARBLOST_CLR I2C master PHY arbitration lost interrupt flag clear 1'b0: No action 1'b1: Action Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
29	WO	0x0	I2CMPNACK_CLR I2C master PHY NACK interrupt flag clear 1'b0: No action 1'b1: Action Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
28	WO	0x0	I2CMPDONE_CLR I2C master PHY done interrupt flag clear 1'b0: No action 1'b1: Action Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
27	WO	0x0	VS_THR_REACHED_CLR Vertical sync threshold reached interrupt flag clear 1'b0: No action 1'b1: Action
26	WO	0x0	VSYNC_ACT_EDGE_CLR Vsync active edge interrupt flag clear 1'b0: No action 1'b1: Action
25	WO	0x0	AKSV_RCV_CLR AKSV received interrupt flag clear 1'b0: No action 1'b1: Action
24	WO	0x0	PLL_CLOCK_GATED_CLR PLL clock gated interrupt flag clear 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
23	WO	0x0	DESER_MISAL_CLR Deserializer misalignment interrupt flag clear 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_MHL==1
22	WO	0x0	CDSENSE_CHG_CLR cdsense change interrupt flag clear 1'b0: No action 1'b1: Action Exists: DWCHDMIRXMHL==1
21	WO	0x0	CEAVID_EMPTY_CLR CEA video FIFO empty interrupt flag clear 1'b0: No action 1'b1: Action Exists: HRX_CEAVIDOUT==1
20	WO	0x0	CEAVID_FULL_CLR CEA video FIFO full interrupt flag clear 1'b0: No action 1'b1: Action Exists: HRX_CEAVIDOUT==1
19	WO	0x0	SCDCTMDSCFGCHANGE_CLR SDCD TMDS Configuration register change interrupt flag clear 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_20==1
18	WO	0x0	SCDCSCSTATUSCHANGE_CLR SCDC Scrambling_Status change interrupt flag clear 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_20==1
17	WO	0x0	SCDCCFGCHANGE_CLR SDCD Configuration register change interrupt flag clear 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_20==1
16	WO	0x0	DCM_CURRENT_MODE_CHG_CLR Deep color mode changed interrupt flag clear 1'b0: No action 1'b1: Action
15	WO	0x0	DCM_PH_DIFF_CNT_OVERFL_CLR Threshold on maximum number of phase re-alignment passed interrupt flag clear 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
14	WO	0x0	DCM_GCP_ZERO_FIELDS_PASS_CLR Number of video fields with receiving GCPs with CD=0 OR CD=reserved information before switching back to 24bit mode passed interrupt flag clear 1'b0: No action 1'b1: Action
13	WO	0x0	CTL3_CHANGE_CLR HDMI CTL3 line changed interrupt flag clear 1'b0: No action 1'b1: Action
12	WO	0x0	CTL2_CHANGE_CLR HDMI CTL2 line changed interrupt flag clear 1'b0: No action 1'b1: Action
11	WO	0x0	CTL1_CHANGE_CLR HDMI CTL1 line changed interrupt flag clear 1'b0: No action 1'b1: Action
10	WO	0x0	CTL0_CHANGE_CLR HDMI CTL0 line changed interrupt flag clear 1'b0: No action 1'b1: Action
9	WO	0x0	VS_POL_ADJ_CLR VS polarity adjust status interrupt flag clear 1'b0: No action 1'b1: Action
8	WO	0x0	HS_POL_ADJ_CLR HS polarity adjust status interrupt flag clear 1'b0: No action 1'b1: Action
7	WO	0x0	RES_OVERLOAD_CLR RES overload state from PHY interrupt flag clear 1'b0: No action 1'b1: Action
6	WO	0x0	CLK_CHANGE_CLR Clock rate changed interrupt flag clear 1'b0: No action 1'b1: Action
5	WO	0x0	PLL_LCK_CHG_CLR PHY PLL lock state changed interrupt flag clear 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
4	WO	0x0	EQGAIN_DONE_CLR EQ gain done from PHY interrupt flag clear 1'b0: No action 1'b1: Action
3	WO	0x0	OFFSCAL_DONE_CLR offscal done from PHY interrupt flag clear 1'b0: No action 1'b1: Action
2	WO	0x0	RESCAL_DONE_CLR rescal done from PHY interrupt flag clear 1'b0: No action 1'b1: Action
1	WO	0x0	ACT_CHANGE_CLR Activity state changed (activity detection signal from PHY) interrupt flag clear 1'b0: No action 1'b1: Action
0	WO	0x0	STATE_REACHED_CLR PHY state_reached interrupt flag clear 1'b0: No action 1'b1: Action

HDMI_RX_HDMI_ISET

Address: Operational Base + offset (0x0fec)

Bit	Attr	Reset Value	Description
31	WO	0x0	HDCP_DKSET_DONE_SET HDCP Device Key Set read operation done interrupt set 1'b0: No action 1'b1: Action Exists: HDCP_DKSET_EXT==1
30	WO	0x0	I2CMP_ARBLOST_SET I2C master PHY arbitration lost interrupt set 1'b0: No action 1'b1: Action Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
29	WO	0x0	I2CMPNACK_SET I2C master PHY NACK interrupt set 1'b0: No action 1'b1: Action Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)

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Bit	Attr	Reset Value	Description
28	WO	0x0	I2CMPDONE_SET I2C master PHY done interrupt set 1'b0: No action 1'b1: Action Exists: (HRX_GEN3_NP_PHY==1 || HRX_PHY_EXTERNAL==1 || HRX_H20GEN1_NP_PHY==1 || HRX_H20COMBOGEN1_NP_PHY==1)
27	WO	0x0	VS_THR_REACHED_SET Vertical sync threshold reached interrupt set 1'b0: No action 1'b1: Action
26	WO	0x0	VSYNC_ACT_EDGE_SET Vsync active edge interrupt set 1'b0: No action 1'b1: Action
25	WO	0x0	AKSV_RCV_SET AKSV received interrupt set 1'b0: No action 1'b1: Action
24	WO	0x0	PLL_CLOCK_GATED_SET PLL clock gated interrupt set 1'b0: No action 1'b1: Action
23	WO	0x0	DESER_MISAL_SET Deserializer misalignment interrupt set 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_MHL==1
22	WO	0x0	CDSENSE_CHG_SET cdsense change interrupt set 1'b0: No action 1'b1: Action Exists: DWCHDMIRXMHL==1
21	WO	0x0	CEAVID_EMPTY_SET CEA video FIFO empty interrupt set 1'b0: No action 1'b1: Action Exists: HRX_CEAVIDOUT==1
20	WO	0x0	CEAVID_FULL_SET CEA video FIFO full interrupt set 1'b0: No action 1'b1: Action Exists: HRX_CEAVIDOUT==1

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Bit	Attr	Reset Value	Description
19	WO	0x0	SCDCTMDSCFGCHANGE_SET SDCD TMDS Configuration register change interrupt set 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_20==1
18	WO	0x0	SCDCSCSTATUSCHANGE_SET SCDC Scrambling_Status change interrupt set 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_20==1
17	WO	0x0	SCDCCFGCHANGE_SET SDCD Configuration register change interrupt set 1'b0: No action 1'b1: Action Exists: DWC_HDMI_RX_20==1
16	WO	0x0	DCM_CURRENT_MODE_CHG_SET Deep color mode changed interrupt set 1'b0: No action 1'b1: Action
15	WO	0x0	DCM_PH_DIFF_CNT_OVERFL_SET Threshold on maximum number of phase re-alignment passed interrupt set 1'b0: No action 1'b1: Action
14	WO	0x0	DCM_GCP_ZERO_FIELDS_PASS_SET Number of video fields with receiving GCPs with CD=0 OR CD=reserved information before switching back to 24bit mode passed interrupt set 1'b0: No action 1'b1: Action
13	WO	0x0	CTL3_CHANGE_SET HDMI CTL3 line changed interrupt set 1'b0: No action 1'b1: Action
12	WO	0x0	CTL2_CHANGE_SET HDMI CTL2 line changed interrupt set 1'b0: No action 1'b1: Action
11	WO	0x0	CTL1_CHANGE_SET HDMI CTL1 line changed interrupt set 1'b0: No action 1'b1: Action

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Bit	Attr	Reset Value	Description
10	WO	0x0	CTL0_CHANGE_SET HDMI CTL0 line changed interrupt set 1'b0: No action 1'b1: Action
9	WO	0x0	VS_POL_ADJ_SET VS polarity adjust status interrupt set 1'b0: No action 1'b1: Action
8	WO	0x0	HS_POL_ADJ_SET HS polarity adjust status interrupt set 1'b0: No action 1'b1: Action
7	WO	0x0	RES_OVERLOAD_SET RES overload state from PHY interrupt set 1'b0: No action 1'b1: Action
6	WO	0x0	CLK_CHANGE_SET Clock rate changed interrupt set 1'b0: No action 1'b1: Action
5	WO	0x0	PLL_LCK_CHG_SET PHY PLL lock state changed interrupt set 1'b0: No action 1'b1: Action
4	WO	0x0	EQGAIN_DONE_SET EQ gain done from PHY interrupt set 1'b0: No action 1'b1: Action
3	WO	0x0	OFFSCAL_DONE_SET offscal done from PHY interrupt set 1'b0: No action 1'b1: Action
2	WO	0x0	RESCAL_DONE_SET rescal done from PHY interrupt set 1'b0: No action 1'b1: Action
1	WO	0x0	ACT_CHANGE_SET Activity state changed (activity detection signal from PHY) interrupt set 1'b0: No action 1'b1: Action
0	WO	0x0	STATE_REACHED_SET PHY state_reached interrupt set 1'b0: No action 1'b1: Action

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HDMI_RX_DMI_SW_RST

Address: Operational Base + offset (0x0ff0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	W1C	0x0	TMDS_SWRESET Functional reset per clock domain (tmds). These bits are self clearing. 1'b0: No action 1'b1: Start reset Exists: DWC_HDMI_RX_MHL==1
15:9	RO	0x0	reserved
8	W1C	0x0	HDCP_SWRESET Functional reset per clock domain (hdcp). These bits are self clearing. 1'b0: No action 1'b1: Start reset Exists: HRX_HDCP22_EXTERNAL==1
7	W1C	0x0	VID_SWRESET Functional reset per clock domain (vid). These bits are self clearing. 1'b0: No action 1'b1: Start reset Exists: HRX_PVO_REMAP==1
6	W1C	0x0	PIXEL_SWRESET Functional reset per clock domain (pixel). These bits are self clearing. 1'b0: No action 1'b1: Start reset Exists: HRX_CEAVIDOUT==1
5	W1C	0x0	CEC_SWRESET Functional reset per clock domain (cec). These bits are self clearing. 1'b0: No action 1'b1: Start reset Exists: HDMIRXCEC==1
4	W1C	0x0	AUD_SWRESET Functional reset per clock domain (aud). These bits are self clearing 1'b0: No action 1'b1: Start reset
3	W1C	0x0	BUS_SWRESET Functional reset per clock domain (bus). These bits are self clearing. 1'b0: No action 1'b1: Start reset

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Bit	Attr	Reset Value	Description
2	W1C	0x0	HDMI_SWRESET Functional reset per clock domain (hdmi). These bits are self clearing. 1'b0: No action 1'b1: Start reset
1	W1C	0x0	MODET_SWRESET Functional reset per clock domain (modet). These bits are self clearing. 1'b0: No action 1'b1: Start reset
0	W1C	0x0	MAIN_SWRESET Main reset control field that when activated resets all configuration bits and resets all functional units.This bit is self clearing: 1'b0: No action 1'b1: Start reset

HDMI_RX_DMI_DISABLE_IF

Address: Operational Base + offset (0x0ff4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x1	TMDS_ENABLE TMDS clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain Exists: DWC_HDMI_RX_MHL==1
15:8	RO	0x0	reserved
7	RW	0x1	VID_ENABLE Video clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain Exists: HRX_PVO_REMAP==1
6	RW	0x1	PIXEL_ENABLE Pixel clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain Exists: HRX_CEAVIDOUT==1
5	RW	0x1	CEC_ENABLE CEC clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain Exists: HDMIRXCEC==1

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Bit	Attr	Reset Value	Description
4	RW	0x1	AUD_ENABLE Audio clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain
3	RW	0x1	BUS_ENABLE Bus clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain
2	W1C	0x1	HDMI_ENABLE HDMI clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain
1	RW	0x1	MODET_ENABLE Mode Detection clock synchronous enable control: 1'b1: Enables all flip flops in the clock domain 1'b0: Disables all flip flops in the clock domain
0	RW	0x1	MAIN_ENABLE Main synchronous enable control: This bit acts over all individual enables (ocfg_enable, omodet_enable, ohdmi_enable, obus_enable, oaud_enable, ocec_enable) 1'b1: Individual enables control the corresponding domains (an exception is cfg_enable that can only be controlled by main) 1'b0: All enables are disabled and individual enables become ineffective

HDMI_RX_DMI_MODULE_ID_EXT

Address: Operational Base + offset (0x0ff8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	HDMIRX_REVISION_ID Synopsys revision IP identifier

HDMI_RX_DMI_MODULE_ID

Address: Operational Base + offset (0x0ffc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	HDMIRX_PRODUCT_ID Synopsys product identifier
15:12	RW	0x0	MAJOR_REV Major revision of this IP
11:8	RO	0x0	MINOR_REV Minor revision of this IP

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	APERTURE_SIZE Address aperture on the DTL bus Note: The actual aperture is (aperture_size + 1) * 4 KB

HDMI_RX_CEC_CTRL

Address: Operational Base + offset (0x1f00)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	SLOWDRVSUPPORT_DISABLE 1'b0: CEC controller supports IO drivers with risetime greater than 1 CEC clock period and where the IO driver risetime-falltime < 170us 1'b1: CEC controller supports IO drivers with risetime of up to 1 CEC clock period
4	RW	0x0	STANDBY 1'b0: CEC controller responds with ACK to all messages. 1'b1: CEC controller responds with NACK to all messages only when it receives EOM, and generates wake up status for opcode. Hence only the last block of a frame is responded with a NACK signal.During standby mode, the follower ACKs the message when there is only one head block pointed to the follower
3	RW	0x0	BC_NACK 1'b0: Reset by software to ACK the received broadcast message. 1'b1: Set by software to NACK the received broadcast message. This bit holds till software resets. The broadcasts will be answered with 0. It means the follower reject the message
2:1	RW	0x0	FRAME_TYP 2'b00: Signal Free Time = 3-bit periods.Previous attempt to send frame is unsuccessful. 2'b01: Signal Free Time = 5-bit periods. New initiator wants to send a frame. 2'b10: Signal Free Time = 7-bit periods. Present initiator wants to send another frame immediately after its previous frame. (spec CEC 9.1) 2'b11: Illegal value. If software write this value, hardware will set the value to the default 2'b01
0	WO	0x0	SEND 1'b0: Reset to 0 by hardware when the CEC transmission is done (no matter successful or failed) or when incoming message is being received. It can also work as an indicator checked by software to see whether the transmission is finished 1'b1: Set by software to trigger CEC sending a frame as an initiator. This bit keeps at 1 while the transmission is going on

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HDMI_RX_CEC_MASK

Address: Operational Base + offset (0x1f08)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	WAKEUP Follower wake-up signal mask
5	RW	0x0	ERROR_FLOW An error is notified by a follower. Abnormal logic data bit error (for follower)
4	RW	0x0	ERROR_INITIATOR An error is detected on CEC line (for initiator only)
3	RW	0x0	ARB_LOST The initiator loses the CEC line arbitration to a second initiator. (specification CEC 9)
2	RW	0x0	NACK A frame is not acknowledged in a directly addressed message. Or a frame is negatively acknowledged in a broadcast message (for initiator only)
1	RW	0x0	EOM EOM is detected so that the received data is ready in the receiver data buffer (for follower only)
0	RW	0x0	DONE The current transmission is successful (for initiator only)

HDMI_RX_CEC_ADDR_L

Address: Operational Base + offset (0x1f14)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	CEC_ADDR_L ■ Logical address 0 - Device TV ■ Logical address 1 - Recording Device 1 ■ Logical address 2 - Recording Device 2 ■ Logical address 3 - Tuner 1 ■ Logical address 4 - Playback Device 1 ■ Logical address 5 - Audio System ■ Logical address 6 - Tuner 2 ■ Logical address 7 - Tuner 3

HDMI_RX_CEC_ADDR_H

Address: Operational Base + offset (0x1f18)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	CEC_ADDR_H ■ Logical address 8 - Playback Device 2 ■ Logical address 9 - Playback Device 3 ■ Logical address 10 - Tuner 4 ■ Logical address 11 - Playback Device 3 ■ Logical address 12 - Reserved ■ Logical address 13 - Reserved ■ Logical address 14 - Free use ■ Logical address 15 - Unregistered (as initiator address), Broadcast (as destination address)

HDMI_RX_CEC_TX_CNT

Address: Operational Base + offset (0x1f1c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	CEC_TX_CNT CEC Transmitter Counter register 5'b0: No data needs to be transmitted 5'b1: Frame size is 1 byte ... 5'b16: Frame size is 16 bytes

HDMI_RX_CEC_RX_CNT

Address: Operational Base + offset (0x1f20)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RO	0x00	CEC_RX_CNT 5-bit counter for RX data buffer 5'b0: No data received 5'b1: 1-byte data is received ... 5'b16: 16-byte data is received

HDMI_RX_CEC_TX_DATA_0

Address: Operational Base + offset (0x1f40)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_1

Address: Operational Base + offset (0x1f44)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_2

Address: Operational Base + offset (0x1f48)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_3

Address: Operational Base + offset (0x1f4c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_4

Address: Operational Base + offset (0x1f50)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_5

Address: Operational Base + offset (0x1f54)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_6

Address: Operational Base + offset (0x1f58)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_7

Address: Operational Base + offset (0x1f5c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_8

Address: Operational Base + offset (0x1f60)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_9

Address: Operational Base + offset (0x1f64)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_10

Address: Operational Base + offset (0x1f68)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_11

Address: Operational Base + offset (0x1f6c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_12

Address: Operational Base + offset (0x1f70)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_13

Address: Operational Base + offset (0x1f74)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_14

Address: Operational Base + offset (0x1f78)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_TX_DATA_15

Address: Operational Base + offset (0x1f7c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_0

Address: Operational Base + offset (0x1f80)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_1

Address: Operational Base + offset (0x1f84)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_2

Address: Operational Base + offset (0x1f88)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_3

Address: Operational Base + offset (0x1f8c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_4

Address: Operational Base + offset (0x1f90)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_5

Address: Operational Base + offset (0x1f94)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_6

Address: Operational Base + offset (0x1f98)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_7

Address: Operational Base + offset (0x1f9c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_8

Address: Operational Base + offset (0x1fa0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_9

Address: Operational Base + offset (0x1fa4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_10

Address: Operational Base + offset (0x1fa8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_11

Address: Operational Base + offset (0x1fac)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_12

Address: Operational Base + offset (0x1fb0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_13

Address: Operational Base + offset (0x1fb4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_14

Address: Operational Base + offset (0x1fb8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_RX_DATA_15

Address: Operational Base + offset (0x1fbc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	DATABYTE Data bits

HDMI_RX_CEC_LOCK

Address: Operational Base + offset (0x1fc0)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	LOCKED_BUFFER This bit becomes active when a frame is received. The CEC controller answers all the messages with NACK until the CPU writes it to 0

HDMI_RX_CEC_WAKEUPCTRL

Address: Operational Base + offset (0x1fc4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	OPCODE0X86EN OPCODE 0x86 wake up enable
6	RW	0x0	OPCODE0X82EN OPCODE 0x82 wake up enable
5	RW	0x0	OPCODE0X70EN OPCODE 0x70 wake up enable
4	RW	0x0	OPCODE0X44EN OPCODE 0x44 wake up enable
3	RW	0x0	OPCODE0X42EN OPCODE 0x42 wake up enable
2	RW	0x0	OPCODE0X41EN OPCODE 0x41 wake up enable
1	RW	0x0	OPCODE0X0DEN OPCODE 0x0D wake up enable
0	RW	0x0	OPCODE0X04EN OPCODE 0x04 wake up enable

HDMI_RX_CBUSSWRESETREQ

Address: Operational Base + offset (0x3000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3	WO	0x0	CBAPBSLV_SWRESETREQ ■ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this registers makes the DWC_mhl_tx_reset_manager generate the following synchronized resets that act as an asynchronous reset in the RTL code: ocbapbslvrefrst_n, ocbapbslvapbrst_n (resetting just CBUS apb_slave module). ■ Reading this register always returns zero
2	WO	0x0	REF_SWRESETREQ ■ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this registers makes the DWC_mhl_tx_cb_reset_manager generate the following synchronized reset that acts as an asynchronous reset in the RTL code: orefrst_n. ■ Reading this register always returns zero
1	RO	0x0	reserved
0	WO	0x0	CBMAIN_SWRESETREQ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this register makes the DWC_mhl_tx_cb_reset_manager generate the following synchronized resets that act as an asynchronous reset in the RTL code: ocpurst_n, orefrst_n, ocbapbslvrefrst_n and ocbapbslvapbrst_n. ■ Reading this register always returns zero. Attention: After successfully reset of the CBUS register bank, the istat_cb_mctrl.cb_regbank_ready interrupt is triggered raising the ointcbus line. This interrupt is automatically triggered by the CBUS to warn the software that the CBUS register bank is ready to be accessed

HDMI_RX_CBUSENABLEIF

Address: Operational Base + offset (0x3004)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	REF_ENABLE Synchronous enable control for orefen: ■ If 1'b0 is written, it disables (set to 1'b0) the corresponding synchronous enable bit. ■ If 1'b1 is written, it enables (set to 1'b1) the corresponding synchronous enable bit
1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	CBMAIN_ENABLE Synchronous enable: ■ If 1'b0 is written, it disables (set to 1'b0) the following synchronous enable bits: ocpuen and orefen. ■ If 1'b1 is written, the control of the synchronous enables is performed by individual control bits. Attention: After successful release of this bit field, the istat_cb_mctrl.cb_regbank_ready interrupt is triggered raising oint line. This interrupt is automatically triggered by the CBUS to warn the software that the CBUS register bank is ready to be accessed.Value After Reset: 0x1

HDMI_RX_CB_LOCKONCLOCK_STS

Address: Operational Base + offset (0x3010)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	REF_LOC irefclk clock status; 1’b0: Clock is stopped 1’b1: Clock is active

HDMI_RX_CB_LOCKONCLOCKCLR

Address: Operational Base + offset (0x3014)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	REF_LOCCLR Clear irefclk clock status bit (cb_lockonclock_sts:ref_loc) 1’b1: Clear irefclk clock status. The clock status goes high again as soon as clock activity is detected. 1’b0: No action

HDMI_RX_CBUSIOCTRL

Address: Operational Base + offset (0x3020)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	DATAPATH_CBUSZ Enables the selection of interface control signals to control the CBUS I/O add-on block, which is required for MHL operation: 1’b1: Main PHY control signals selected 1’b0: CBUS control interface selected For HDMI mode of operation, the DATAPATH_CBUSZ signal must always asserted high
23:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	CBUS_SVSRETMODEZ CBUS I/O Enables retention mode; for more information, refer to CBUS I/O documentation
15:9	RO	0x0	reserved
8	RW	0x0	CBUS_PDDQ CBUS I/O PDDQ control; for more information, refer to CBUS I/O documentation
7:1	RO	0x0	reserved
0	RW	0x0	CBUS_RESET CBUS I/O reset control; for more information, refer to CBUS I/O documentation

HDMI_RX_DD_CTRL

Address: Operational Base + offset (0x3040)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	AUTO_FLOATCBUS When a Wake Pulse or Discovery Pulse sequence fails to be detected within the MHL spec time limits, this bit enables an automatic switch to the Float CBUS state, without software action. If enabled, both interrupts 'discoverypulse_fail' and 'wakepulse_fail' are still triggered, specifically at the time the Device Discovery moves to the Float CBUS state. 1’b0: Disabled 1’b1: Enabled
7	RW	0x0	ZSINK_SELECT Select which MHL line Zsink resistor the Device Discovery module will use when the MHL data path is enabled. 1’b0: Use ZRXSENSE_TMDS 1’b1: Use ZRXSENSE_TERM
6	RW	0x0	SINK_DONGLE_SEL Sink or Dongle operation type selection: 1’b0: Operate as Sink 1’b1: Operate as Dongle
5	RW	0x0	SRC_PATH_EN Source PATH_EN bit: 1’b0: Source device TMDS path is not active. 1’b1: Source device TMDS path is active
4	RW	0x0	SNK_PATH_EN Sink PATH_EN bit: 1’b0: Sink device TMDS path is not active. 1’b1: Sink device TMDS path is active

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Bit	Attr	Reset Value	Description
3	RW	0x0	SNK_POW Global Sink/Source POW bit. VBUS output capability in any power state. As a Dongle, POW is set when "Dongle Own Power" is available. This bit must match the DEV_CAT[4].POW bit in the Device Capability Registers: 1'b0: Sink device cannot output power VBUS. 1'b1: Sink device can output power VBUS
2	RW	0x0	STBY_VBUS VBUS output capability while in Standby power state.Only applicable to Sink mode, not Dongle: 1'b0: VBUS output capability disabled in Standby power state 1'b1: VBUS output capability enabled in Standby power state Note: Actual VBUS voltage drive is only active if cable is attached; for instance, cdsense input (or software override) is active
1	RW	0x0	STBY_WAKE Wake Pulse detection while in Standby power state.Only applicable to Sink mode, not Dongle. 1'b0: Wake Pulse Detection disabled in Standby power state 1'b1: Wake Pulse Detection enabled in Standby power state
0	RW	0x0	DISCOVER_EN CBUS Device Discovery enable: 1'b0: Device Discovery is not enabled 1'b1: Device Discovery is enabled

HDMI_RX_DD_OP_CTRL

Address: Operational Base + offset (0x3044)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	WO	0x0	FLOAT_CBUS ■ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this registers requests a Float CBUS condition to force the Source to cancel the CBUS link and repeat the Discovery Sequence. This can be used by software as a response to interrupts 'discoverypulse_fail' or 'wakepulse_fail', if 'auto_floatcbus'=0, or at any time the software needs to reset the CBUS link connection.Reading this register always returns zero
1	WO	0x0	POWER_ACTIVE ■ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this bit requests a transition from Standby to Active power state on Sink/Dongle.Reading this register always returns zero

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Bit	Attr	Reset Value	Description
0	RW	0x0	POWER_STANDBY ■ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this bit requests a transition to Standby power state on Sink/Dongle. This action disables the MHL Data Path. Reading this register always returns zero

HDMI_RX_DD_STS

Address: Operational Base + offset (0x3048)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RO	0x0	ST_CONNECTED Active when the Device Discovery process is successful, cable is still attached, and power state is Active. This bit is set to 1 during states SINK2/3 and DONGLE2/3/6/7 in the Device Discovery FSM. 1'b0: Not connected 1'b1: Connected
18	RO	0x0	ST_ATTACHED Status of the CDSENSE input, the Cable Detect mechanism. When MHL mode manual override bit mhlmode_ctrl:mhlmode_man_ovr=1, this "st_attached" status reflects the value of bit mhlmode_ctrl:mhlmode_man instead of the actual CDSENSE input. 1'b0: No cable detected 1'b1: Cable attached note: This status bit and its interrupt (istat_cb_dd:connected) are independent from any Device Discovery bypass mode (dd_bypass_ mode can have any value)
17	RO	0x0	ST_VBUS_VALID Status of VBUS voltage detector. Used regardless of the VBUS driver is the Source or Sink. 1'b0: No VBUS voltage detected 1'b1: Valid VBUS voltage detected note: This status bit and its interrupt (istat_cb_dd:vbus_valid) are independent from any Device Discovery bypass mode (dd_bypass_ mode can have any value)
16	RO	0x0	ST_POWERSTATE Current Sink Power State, from MHL2.1 specification: 1'b0: Standby 1'b1: Active
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RO	0x00	DDFSM Current state of the Device Discovery FSM. 5'b0: IDLE (Device Discovery is disabled) 5'b1: SINK0 5'b2: SINK1 5'b3: SINK2 5'b4: SINK3 5'b5: SINK4A/B/C 5'b6: SINK5 5'b7: DONGLE0 5'b8: DONGLE1 5'b9: DONGLE2 5'b10: DONGLE3 5'b11: DONGLE4 5'b12: DONGLE5 5'b13: DONGLE6 5'b14: DONGLE7 5'b15: DONGLE8 5'b16L: DONGLE9 Others: Reserved
7:6	RO	0x0	reserved
5	RO	0x0	CBUS_DATAIN Current value of the CBUS line
4	RO	0x0	VBUS_DRIVE Status of VBUS output control. 1'b0: Output disabled 1'b1: Output enabled; i.e. VBUS driving circuitry enabled
3	RO	0x0	ZRXSENSE_TMDS Status of ZRXSENSE_TMDS MHL pull-up: 1'b0: Disabled 1'b1: Enabled
2	RO	0x0	ZRXSENSE_TERM Status of ZRXSENSE_TERM MHL pull-up: 1'b0: Disabled 1'b1: Enabled
1	RO	0x0	ZSINKON Status of ZCBUS_SINK_ON CBUS pull-up: 1'b0: Disabled 1'b1: Enabled
0	RO	0x0	ZSINKDISCOVER Status of ZCBUS_SINK_DISCOVER CBUS pull-up: 1'b0: Disabled 1'b1: Enabled

HDMI_RX_DD_BYPASS_EN

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Address: Operational Base + offset (0x304c)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	VBUS_DRIVE_BYPASS_EN Bypass mode for direct control of driving VBUS. When enabled, VBUS output control is done by bit 'vbus_drive_bypass'.This mode is overridden to Enabled if dd_bypass_mode=10. 1'b0: Disabled 1'b1: Enabled
1:0	RW	0x0	DD_BYPASS_MODE Bypass mode for CBUS IO signals and MHL/CBUS impedance resistor control.CBUS I/O Bypass mode: 2'b00: Bypass mode is disabled, normal operation. 2'b01: Device Discovery sequence is bypassed, and Link Layer is available for CBUS transfers. CBUS/MHL impedance control bits from register 'dd_bypass_ctrl[0:3]' are not available in this mode. 2'b10: Full bypass mode, all CBUS control is active for the System software. This mode overrides 'vbus_drive_bypass_en'. In this mode the Zsinkon resistor must be enabled to be able to correctly receive RX CBUS packets (cbus_zsinkon_bypass=1). 2'b11: Reserved

HDMI_RX_DD_BYPASS_CTRL

Address: Operational Base + offset (0x3050)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	CBUS_RXRCV_EN_BYPASS When Device Discovery Full Bypass mode is enabled (dd_bypass_mode=10), this bit directly controls the enabling of the CBUS Receiver. 1'b0: Disabled 1'b1: Enabled
5	RO	0x0	reserved
4	RW	0x0	VBUS_DRIVE_BYPASS When VBUS Bypass mode is enabled (vbus_drive_bypass_en=1), this bit directly controls the output of VBUS. 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	MHL_ZRXSENSE_TMDS_BYPASS When Device Discovery Full Bypass mode is enabled (dd_bypass_mode=10), this bit directly controls the MHL Zrxsense_tmds pull-down resistor. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	MHL_ZRXSENSE_TERM_BYPASS When Device Discovery Full Bypass mode is enabled (dd_bypass_mode=10), this bit directly controls the MHL Zrxsense_term pull-down resistor. 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	CBUS_ZSINKON_BYPASS When Device Discovery Full Bypass mode is enabled (dd_bypass_mode=10), this bit directly controls the CBUS Zcbus_sinkon pull-down resistor. 1'b0: Disabled. 1'b1: Enabled
0	RW	0x0	CBUS_ZSINKDISCOVER_BYPASS When Device Discovery Full Bypass mode is enabled (dd_bypass_mode=10), this bit directly controls the CBUS Zcbus_sink_discover pull-down resistor. 1'b0: Disabled 1'b1: Enabled

HDMI_RX_DD_BYPASS_CBUS

Address: Operational Base + offset (0x3054)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	CBUS_LL_DATAIN_DISABLE When CBUS SW bypass is enabled (dd_bypass_mode=10), this bit disables the RX engine of the CBUS Link Layer block, by blocking the CBUS datain line input. 1'b0: CBUS Datain into Link Layer Enabled 1'b1: CBUS Datain into Link Layer RX Disabled If this bit is 0 (datain enabled) during a bypass TX packet (SW driving bits cbus_txdrv_en_bypass and cbus_dataout_bypass), the Link Layer RX engine will attempt to receive the same packet, which may result in unexpected interrupts in register fields istat_cb_ll:rx*. To avoid unexpected RX activity, set bit cbus_ll_datain_disable=1 while driving a TX bypass packet. Notes: ■ This bit is only used in bypass mode dd_bypass_mode=10. ■ The current CBUS line value is always available in register 'dd_sts:cbus_datain', regardless of bypass mode (dd_bypass_mode) or 'cbus_ll_datain_disable' value
3:2	RO	0x0	reserved
1	RW	0x0	CBUS_DATAOUT_BYPASS Selects the value driven to the CBUS IO when Bypass TX Driver enable is high (cbus_txdrv_en_bypass=1). 1'b0: Drive CBUS line low 1'b1: Drive CBUS line high
0	RW	0x0	CBUS_TXDRV_EN_BYPASS When CBUS SW bypass is enabled (dd_bypass_mode=10), controls the enabling of the CBUS IO TX driver. 1'b0: Disabled 1'b1: Enabled

HDMI_RX_LL_TXPCKFIFO

Address: Operational Base + offset (0x3080)

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Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	TXFIFOXFERINITFAILEN Incoming RX transfer detection enable for CBUS Packet transmit request (txfifoxferinit = 1): 1'b1: The transmit request is canceled if there is an ongoing RX transfer on the CBUS line, raising the txfifoxferinitfail interrupt. In this case, the TX FIFO contents remain unchanged. If this is selected, TX packet re-arbitration by use of txnarbmax>0 will be disabled. 1'b0: The transmit request is always recorded by the Link Layer for immediate or later transmission, depending on the CBUS line status. For instance, the transmit is performed as soon as possible
11	RO	0x0	reserved
10:0	RW	0x000	TXPCKCONTENT CBUS Packet transmit FIFO write accessCompose txpckcontent in the following way: txpckcontent[10:0] = Header[1:0], Control, Data/Command[7:0] Header[1:0], Control and Data/Command[7:0] must follow the CBUS packet structure specification. Note: The maximum packet transmit FIFO depth is 24, which is the maximum number of consecutive packets that an initiator can transmit before allowing for re-arbitration. Parity is automatically calculated by the Link Layer

HDMI_RX_LL_RXPCKFIFO_RD_CLR

Address: Operational Base + offset (0x3084)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	WO	0x0	RXFIFOCLR_B Clear RX FIFO B contents 1'b1: Clear RX FIFO B contents 1'b0: No action Note: This register is auto-cleared.
23:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	WO	0x0	RXPCKFIFOREAD_B CBUS Packet receiver FIFO B read acknowledge ■ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this bit tells the RX FIFO B to pop the next received packet from the FIFO into field rxpckcontent_b[11:0]. This operation guarantees a new value for the next sequential APB read command from the TL uP. Each time this bit is set to 1, rxfifofilllevel_b is decremented. If rxfifofilllevel_b becomes 0, rxfifoempty_b is set to 1. If rxpckfiforead_b is written to 1 while rxfifoempty_b is 1, rxpckcontent_b[11:0] remains unchanged. Reading this register always returns zero.
15:9	RO	0x0	reserved
8	W1C	0x0	RXFIFOCLR_A Clear RX FIFO A contents: 1’b1: Clear RX FIFO A contents 1’b0: No action Note: This register is auto-cleared.
7:1	RO	0x0	reserved
0	WO	0x0	RXPCKFIFOREAD_A CBUS Packet receiver FIFO A read acknowledge: ■ Writing 1'b0 to this bit has no effect. ■ Writing 1'b1 to this bit tells the RX FIFO A to pop the next received packet from the FIFO into field rxpckcontent_a[11:0]. This operation guarantees a new value for the next sequential APB read command from the TL uP. Each time this bit is set to 1, rxfifofilllevel_a is decremented. If rxfifofilllevel_a becomes 0, rxfifoempty_a is set to 1. If rxpckfiforead_a is written to 1 while rxfifoempty_a is 1, rxpckcontent_a[11:0] remains unchanged. Reading this register always returns zero.

HDMI_RX_LL_RXPCKFIFO_A

Address: Operational Base + offset (0x3088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	RXFIFOFILLLEVEL_A Number of packets in receiver FIFO A, waiting to be read. When this value is 0, rxfifoempty_a is 1.
23:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RO	0x0	RXFIFOEMPTY_A Packet receiver FIFO A empty status: 1'b1: Packet receiver FIFO A is empty. The value at rxpckcontent_a[11:0] while this field is high is invalid and must be disregarded. 1'b0: Packet receiver FIFO A is not empty. Note: Software must continuously read until it sees the high value rxfifoempty_a. This bit is not a sticky bit status indication.
15:12	RO	0x0	reserved
11:0	RO	0x000	RXPCKCONTENT_A CBUS Packet receive FIFO A read access The rxpckcontent_a contains the following data: rxpckcontent_a[11:0] = Header[1:0],Control,Data/Command[7:0],ParityHeader[1:0], Control, Data/Command[7:0] and Parity must follow the CBUS packet structure specification. This bit continuously reads data until rxfifoempty_a status is high (meaning that all data has been read from packet receive FIFO). Note: The maximum packet receiver A FIFO depth is 24

HDMI_RX_LL_RXPCKFIFO_B

Address: Operational Base + offset (0x308c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	RXFIFOFILLLEVEL_B Number of packets in receiver FIFO B, waiting to be read. When this value is 0, rxfifoempty_b is 1.
23:17	RO	0x0	reserved
16	RO	0x0	RXFIFOEMPTY_B Packet receiver FIFO B empty status: 1'b1: Packet receiver FIFO B is empty. The value of rxpckcontent_b[11:0] while this field is high is invalid and must be disregarded. 1'b0: Packet receiver FIFO B is not empty. Note: Software must continuously read until it sees the high value rxfifoempty_b. This bit is not a sticky bit status indication.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RO	0x000	RXPCKCONTENT_B CBUS Packet Receive FIFO B read access The rxpckcontent_b contains the following data: rxpckcontent_b[11:0]=Header[1:0],Control,Data/Command[7:0],ParityHeader[1:0], Control, Data/Command[7:0] and Parity must follow the CBUS packet structure specification. This bit continuously reads data until rxfifoempty_b status is high (meaning that all data has been read from the packet receive FIFO). Note: The maximum packet receiver B FIFO depth is 24.

HDMI_RX_LL_TXPCKCTRL_0

Address: Operational Base + offset (0x3090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	W1C	0x0	TXFIFOCLR Clear TX FIFO contents: 1'b1: Clear TX FIFO contents. If the FIFO is not empty, the following registers fields change accordingly: txfifofilllevel and txfifoempty 1'b0: No action Note: This register is auto-cleared. This register can only be set if st_txfifoxferbusy is 0.
15:9	RO	0x0	reserved
8	W1C	0x0	TXFIFOXFERSTOP Stop TX operation: - 1: Stop Packet transmit buffer action after completing any current transmission, RX or TX. - 0: No action Attention: After a stop request, the SW must guarantee any ongoing packet has finished being sent to the CBUS line, before asserting txfifoxferinit high for a new transfer. This can be accomplished by a software timer of 30 maximum bit times: 30 x 1,2us = 36us. Note 1: This register is auto-cleared. Note 2: Acting on txfifoxferstop clears st_txfifoxferbusy (after current transfer completes) but does not clear the TX FIFO contents (use txfifoclr to clear TX FIFO)
7:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	W1C	0x0	TXFIFOXFERINIT TX transfer initialization request for Packet Transmit FIFO:1: Request a transmission of the current Packet TX FIFO contents: ■ If bit txfifoxferinitfailen = 1, the request may not be recorded due to an ongoing RX transfer, raising the txfifoxferinitfail interrupt. In this case, the TX FIFO contents remain unchanged. ■ If bit txfifoxferinitfailen = 0, the TX request is executed immediately if the CBUS line is idle, or recorded for later transfer if the CBUS line is busy with an RX transfer. ■ If the transmit request is successful, st_txfifoxferbusy status bit is set high until all packets from TX FIFO are sent (or txfifoxferstop is set).0: No action Note: This register is auto-cleared. This bit can only be set if st_txfifoxferbusy is 0.

HDMI_RX_LL_TXPCKCTRL_1

Address: Operational Base + offset (0x3094)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x1	TXPCKCOLLISION_EN CBUS line collision detection enable: 1’b0: Collision detection disabled 1’b1: Collision detection enabled
27:24	RO	0x0	reserved
23:16	RW	0x20	TXNRETRYMAX Maximum number of TX packet retries upon reception of a line NACK from the follower: 8'd0: No packet retry is attempted. Interrupt txnretry is asserted immediately aftyer receiving the first line NACK. 8'd1-8'd255: The initiator retries packet transmission txnretrymax times before giving up and signaling software through the txnretry interrupt. Note: According to the MHL specification 13.10.2, upon reception of a line NACK, the Initiator retries at least 32 times (NRETRY >= 32). This field can only be changed if st_txfifoxferbusy is 0.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	TXNARBMAX Maximum number of consecutive re-arbitrations: 5'b0: No re-arbitration is attempted if line ownership is lost. The software has to request a TX operation again by setting txfifoxferinit=1. Every time the arbitration is lost, the txpckmaxarblost interrupt is set. 5'b1..31: Consecutive re-arbitration of the CBUS line is attempted after ownership is lost, up to the specified maximum. If the maximum count is reached, the txpckmaxarblost interrupt is set. Notes: ■ When set to a value other than 0, the re-arbitrations will only be done if txfifoxferinitfailen=0. ■ This register does not apply to re-arbitrations interleaved by successful packets. A successful packet resets the counter. This field can only be changed if st_txfifoxferbusy is 0.
7:1	RO	0x0	reserved
0	RW	0x1	TXWAITCTRL CBUS hold-off wait control; Selects the time the Link Layer will wait after sending an ACK to a received packet, before arbitrating to gain CBUS control to send a packet. 1'b0: Wait for TWAIT = 12 x TBIT before arbitrating for the CBUS (optional extended wait time) 1'b1: Wait for TRESP_HOLD = 4 x TBIT before arbitrating for the CBUS (according to MHL spec)

HDMI_RX_LL_PCKFIFO_STS

Address: Operational Base + offset (0x309c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RO	0x0	ST_RXFIFOXFERBUSY Receiver FIFO Busy Status: 1'b1: A packet, or a sequence of packets, is currently being received. 1'b0: No activity on receiving packets
15:13	RO	0x0	reserved
12:8	RO	0x00	TXFIFOFILLLEVEL Number of transmit packet FIFO packets still to be transmitted: 5'b0: No packets to be transmitted 5'b1..24: Number of packets still in the transmit packet FIFO (To be successfully transmitted, the packet has to be line ACK by the follower device). Others: Not possible
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RO	0x0	TXFIFOFULL Transmitter FIFO full status: 1'b1: Packet transmit FIFO is full. 1'b0: Packet transmit FIFO is not full.
4	RO	0x0	ST_TXFIFOEMPTY Transmitter FIFO empty status: 1'b1: Packet transmit FIFO is empty. 1'b0: Packet transmit FIFO is not empty
3:1	RO	0x0	reserved
0	RO	0x0	ST_TXFIFOXFERBUSY Transmitter FIFO Busy Status: 1'b1: A request to send Packet transmit FIFO has been acted but not yet fulfilled (pending) 1'b0: No Packet transmit FIFO request pending Note: While signaling a busy state, the transmit packet FIFO cannot be written.

HDMI_RX_LL_RXPCKCTRL_0

Address: Operational Base + offset (0x30a0)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x1	RPLYCTRL_51PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x51 code (STOP): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
24	RW	0x1	RPLYCTRL_50PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x50 code (CONT): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
23:14	RO	0x0	reserved
13	RW	0x1	RPLYCTRL_35PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x35 code (ABORT): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
12	RW	0x1	RPLYCTRL_34PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x34 code (NACK): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.

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Bit	Attr	Reset Value	Description
11	RW	0x1	RPLYCTRL_33PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x33 code (ACK): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
10	RW	0x1	RPLYCTRL_32PCTR Control CBUS Link Layer reply to MSC and DDC control packets with 0x32 code (EOF): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
9	RO	0x0	reserved
8	RW	0x1	RPLYCTRL_30PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x30 code (SOF): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
7:6	RO	0x0	reserved
5	RW	0x0	RPLYCTRL_UNKNOWNPCTRL Control CBUS Link Layer reply to MSC and DDC control packets with unknown code:
4	RW	0x0	RPLYCTRL_BADPAR Control CBUS Link Layer reply to packets with wrong parity: 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
3	RW	0x0	RPLYCTRL_11HEADER Control CBUS Link Layer reply to packets with header bits set to 2'b11 (Reserved packets): 1'b0: Reply with line NACK to all control packets with this bits. 1'b1: Reply with line ACK to all control packets with this bits
2	RW	0x1	RPLYCTRL_10HEADER Control CBUS Link Layer reply to packets with header bits set to 2'b10 (MSC packets): 1'b0: Reply with line NACK to all control packets with this bits. 1'b1: Reply with line ACK to all control packets with this bits
1	RW	0x0	RPLYCTRL_01HEADER Control CBUS Link Layer reply to packets with header bits set to 2'b01 (Vendor-specific packets): 1'b0: Reply with line NACK to all control packets with this bits. 1'b1: Reply with line ACK to all control packets with this bits
0	RW	0x1	RPLYCTRL_00HEADER Control CBUS Link Layer reply to packets with header bits set to 2'b00 (DDC packets): 1'b0: Reply with line NACK to all control packets with this bits. 1'b1: Reply with line ACK to all control packets with this bits

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HDMI_RX_LL_RXPCKCTRL_1

Address: Operational Base + offset (0x30a4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x1	RPLYCTRL_ALLP Control CBUS Link Layer reply to all packets (independent of any packet content): 1'b0: Reply with NACK to all packets. 1'b1: No action. Control of NACK auto response is set by each rplyctrl_* register.
27:14	RO	0x0	reserved
13	RW	0x0	RPLYCTRL_6DPCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x6D code (GET_SC3_ERRORCODE): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
12	RW	0x1	RPLYCTRL_6CPCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x6C code (WRITE_BURST): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code.
11	RW	0x1	RPLYCTRL_6BPCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x6B code (GET_MSC_ERRORCODE): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
10	RW	0x1	RPLYCTRL_6APCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x6A code (GET_DDC_ERRORCODE): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
9	RW	0x0	RPLYCTRL_69PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x69 code (GET_SC1_ERRORCODE): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
8	RW	0x1	RPLYCTRL_68PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x68 code (MSC_MSG): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x1	RPLYCTRL_65PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x65 code (CLR_HPD): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
4	RW	0x1	RPLYCTRL_64PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x64 code (SET_HPD): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
3	RW	0x0	RPLYCTRL_63PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x63 code (GET_VENDOR_ID): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
2	RW	0x1	RPLYCTRL_62PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x62 code (GET_STATE): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
1	RW	0x1	RPLYCTRL_61PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x61 code (READ_DEVCAP): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code
0	RW	0x1	RPLYCTRL_60PCTRL Control CBUS Link Layer reply to MSC and DDC control packets with 0x60 code (WRITE_STAT/SET_INT): 1'b0: Reply with line NACK to all control packets with this code. 1'b1: Reply with line ACK to all control packets with this code

HDMI_RX_LL_INTTRSHLDCTRL

Address: Operational Base + offset (0x30b0)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	RXPCKINVOPCODE_CNTEN Interrupt counter enable for rxpckinvopcode: 1'b0: The interrupt is set every time the related event occurs. 1'b1: The interrupt is set when the counter is a multiple of the value set by the threshold.

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	RXPCKINVOPCODE_TRSHLD Interrupt counter threshold for rxpckinvopcode; programmable values are: 3'b0: 2 3'b1: 4 3'b2: 8 3'b3: 16 3'b4: 32 3'b5: 64 3'b6: 128 3'b7: 256 Note: The first interrupt source event will always trigger an interrupt pulse. The subsequent events will be filtered by this threshold counter
19	RW	0x0	RXPCKINVHEADER_CNTEN Interrupt counter enable for rxpckinvheader: 0: The interrupt is set every time the related event occurs. 1: The interrupt is set when the counter is a multiple of the value set by the threshold
18:16	RW	0x0	RXPCKINVHEADER_TRSHLD Interrupt counter threshold for rxpckinvheader; programmable values are: 3'b0: 2 3'b1: 4 3'b2: 8 3'b3: 16 3'b4: 32 3'b5: 64 3'b6: 128 3'b7: 256 Note: The first interrupt source event always triggers an interrupt pulse. The subsequent events are filtered by this threshold counter.
15	RW	0x0	RXPCKINCOMPLETE_CNTEN Interrupt counter enable for rxpckincomplete: 1'b0: The interrupt is set every time the related event occurs. 1'b1: The interrupt is set when the counter is a multiple of the value set by the threshold.

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	RXPCKINCOMPLETE_TRSHLD Interrupt counter threshold for rxpckincomplete; programmable values are: 3'b0: 2 3'b1: 4 3'b2: 8 3'b3: 16 3'b4: 32 3'b5: 64 3'b6: 128 3'b7: 256 Note: The first interrupt source event always triggers an interrupt pulse. The subsequent events are filtered by this threshold counter.
11	RW	0x0	RXPCKNOSYNC_CNTEN Interrupt counter enable for rxpcknosync: 1'b0: The interrupt is set every time the related event occurs. 1'b1: The interrupt is set when the counter is a multiple of the value set by the threshold
10:8	RW	0x0	RXPCKNOSYNC_TRSHLD Interrupt counter threshold for rxpcknosync; programmable values are: 3'b0: 2 3'b1: 4 3'b2: 8 3'b3: 16 3'b4: 32 3'b5: 64 3'b6: 128 3'b7: 256 Note: The first interrupt source event always triggers an interrupt pulse. The subsequent events are filtered by this threshold counter.
7	RW	0x0	RXPCKBADPAR_CNTEN Interrupt counter enable for rxpckbadpar: 1'b0: The interrupt is set every time the related event occurs. 1'b1: The interrupt is set when the counter is a multiple of the value set by the threshold.

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	RXPCKBADPAR_TRSHLD Interrupt counter threshold for rxpckbadpar; programmable values are: 3'b0: 2 3'b1: 4 3'b2: 8 3'b3: 16 3'b4: 32 3'b5: 64 3'b6: 128 3'b7: 256 Note: The first interrupt source event always triggers an interrupt pulse. The subsequent events are filtered by this threshold counter
3	RW	0x0	TXPCKCOLLISION_CNTEN Interrupt counter enable for txpckcollision: 1'b0: The interrupt is set every time the related event occurs. 1'b1: The interrupt is set when the counter is a multiple of the value set by the threshold
2:0	RW	0x0	TXPCKCOLLISION_TRSHLD Interrupt counter threshold for txpckcollision; programmable values are: 3'b0: 2 3'b1: 4 3'b2: 8 3'b3: 16 3'b4: 32 3'b5: 64 3'b6: 128 3'b7: 256 Note: The first interrupt source event will always trigger an interrupt pulse. The subsequent events are filtered by this threshold counter

HDMI_RX_LL_INTCNTCTRL

Address: Operational Base + offset (0x30b4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	W1C	0x0	RXPCKINVOPCODE_CNTCLR Clear rxpckinvopcode_cnt interrupt counter: 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear

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Bit	Attr	Reset Value	Description
4	W1C	0x0	RXPCKINVHEADER_CNTCLR Clear rxpckinvheader_cnt interrupt counter: 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear
3	W1C	0x0	RXPCKINCOMPLETE_CNTCLR Clear rxpckincomplete_cnt interrupt counter: 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear.
2	W1C	0x0	RXPCKNOSYNC_CNTCLR Clear rxpcknosync_cnt interrupt counter: 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear.
1	W1C	0x0	RXPCKBADPAR_CNTCLR Clear rxpckbadpar_cnt interrupt counter: 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear.
0	RW	0x0	TXPCKCOLLISION_CNTCLR Clear txpckcollision_cnt interrupt counter: 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear.

HDMI_RX_LL_INTCNT_0

Address: Operational Base + offset (0x30b8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	RXPCKINCOMPLETE_CNT Interrupt counter for rxpckincomplete If rxpckincomplete_cnten = 1, this counter is incremented every time the related event occurs.
23:16	RO	0x00	RXPCKNOSYNC_CNT Interrupt counter for rxpcknosync If rxpcknosync_cnten = 1, this counter is incremented every time the related event occurs.
15:8	RO	0x00	RXPCKBADPAR_CNT Interrupt counter for rxpckbadpa If rxpckbadpa_cnten = 1, this counter is incremented every time the related event occurs.
7:0	RO	0x00	TXPCKCOLLISION_CNT Interrupt counter for txpckcollision If txpckcollision_cnten = 1, this counter is incremented every time the related event occurs.

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HDMI_RX_LL_INTCNT_1
Address: Operational Base + offset (0x30bc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RO	0x00	RXPCKINVOPCODE_CNT Interrupt counter for rxpckinvopcode If rxpckinvopcode_cnten = 1, this counter is incremented every time the related event occurs.
7:0	RW	0x00	RXPCKINVHEADER_CNT Interrupt counter for rxpckinvheader If rxpckinvheader_cnten = 1, this counter is incremented every time the related event occurs

HDMI_RX_CBHDCP_OPCTRL
Address: Operational Base + offset (0x3100)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:10	RW	0x0	CBHDCP_NBYTES Number of bytes to be transferred from/to the HDCP register, starting from address offset hdcp_addr[7:0]. 3'b1: 1 byte 3'b2: 2 bytes 3'b3: 3 bytes 3'b4: 4 bytes 3'b5: 5 bytes 3'b6: 6 bytes 3'b7: 7 bytes 3'b0: 8 bytes
9	RW	0x0	CBHDCP_ADDR_INCR Address automatic increment. 1'b1: Auto increment enabled; Each byte will be transferred to an incrementing address, starting at cbhdcp_addr[7:0]. 1'b0: Auto increment disabled; All bytes will be transferred to/from the same address
8:1	RW	0x00	CBHDCP_ADDR HDCP register address for the read or write transfer request
0	RW	0x0	CBHDCP_RWSEL Select transfer request type, for read or write to an HDCP register. 1'b0: Read 1'b1: Write

HDMI_RX_CBHDCP_WDATA_0
Address: Operational Base + offset (0x3104)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CBHDCP_WDATA_0 Data to be written to an HDCP register. Least significant 32 bits from offset hdcp_addr[7:0]. (Bytes 1,2,3,4).

HDMI_RX_CBHDCP_WDATA_1

Address: Operational Base + offset (0x3108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CBHDCP_WDATA_1 Data to be written to an HDCP register. Least significant 32 bits from offset hdcp_addr[7:0]. (Bytes 1,2,3,4).

HDMI_RX_CBHDCP_RDATA_0

Address: Operational Base + offset (0x310c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CBHDCP_RDATA_0 Read data from an HDCP register. Least significant 32 bits from offset hdcp_addr[7:0]. (Bytes 1,2,3,4).

HDMI_RX_CBHDCP_RDATA_1

Address: Operational Base + offset (0x3110)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	CBHDCP_RDATA_1 Read data from an HDCP register. Most significant 32 bits from offset hdcp_addr[7:0]. (Bytes 5,6,7,8).

HDMI_RX_CBHDCP_STATUS

Address: Operational Base + offset (0x3114)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	CBHDCP_BUSY_STS High when the HDCP IF is busy reading or writing a register. When this bit changes from high to low, interrupt hdcp_done is generated.

HDMI_RX_CBHDCP_DDC_REPORT

Address: Operational Base + offset (0x3118)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	W1C	0x0	CBHDCP_DDC_COMPLETE TL software must write a 1 to this bit when a CBUS DDC Command for an HDCP register is complete. For instance, when all bytes have been transferred. 1'b1: Notify HDCP engine of a completed DDC Command 1'b0: No action Note: This register is auto-cleared.

HDMI_RX_ISTAT_CB_DD

Address: Operational Base + offset (0x3200)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RO	0x0	POWERSTATE Status register 'st_powerstate' has changed value
4	RW	0x0	WAKEPULSE_FAIL Wake Pulse sequence detection failed due to 200ms timeout
3	RO	0x0	DISCOVERYPULSE_FAIL Discovery Pulse sequence detection failed due to 1005mstimeout after the Sink transitions to SINK1 state (Attached,Active, but not Connected yet)
2	RO	0x0	VBUS_VALID Status register 'st_vbus_valid' has changed value
1	RO	0x0	CONNECTED Status register 'st_connected' has changed value.
0	RW	0x0	ATTACHED Status register 'st_attached' has changed value.

HDMI_RX_IMASK_CB_DD

Address: Operational Base + offset (0x3204)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	MASK_POWERSTATE powerstate interrupt mask (see corresponding status bit forthis interrupt description): 1'b1: Mask interrupt. This means that the correspondingstatus bit is never high, because this register bit preventsthe corresponding interrupt to be caught by the sticky bitstatus interrupt. 1'b0: Interrupt is not masked

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Bit	Attr	Reset Value	Description
4	RW	0x1	MASK_WAKEPULSE_FAIL wakepulse_fail interrupt mask (see corresponding status bitfor this interrupt description) 1'b1: Mask interrupt. This means that the correspondingstatus bit is never high, because this register bit preventsthe corresponding interrupt to be caught by the sticky bitstatus interrupt. 1'b0: Interrupt is not masked
3	RW	0x1	MASK_DISCOVERYPULSE_FAIL discoverypulse_fail interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the correspondingstatus bit is never high, because this register bit preventsthe corresponding interrupt to be caught by the sticky bitstatus interrupt. 1'b0: Interrupt is not masked
2	RW	0x1	MASK_VBUS_VALID vbus_valid interrupt mask (see corresponding status bit for this interrupt description) 1'b1: Mask interrupt. This means that the correspondingstatus bit is never high, because this register bit preventsthe corresponding interrupt to be caught by the sticky bitstatus interrupt. 1'b0: Interrupt is not masked
1	RW	0x1	MASK_CONNECTED connected interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the correspondingstatus bit is never high, because this register bit preventsthe corresponding interrupt to be caught by the sticky bitstatus interrupt. 1'b0: Interrupt is not masked
0	RW	0x1	MASK_ATTACHED attached interrupt mask (see corresponding status bit for thisinterrupt description) 1'b1: Mask interrupt. This means that the correspondingstatus bit is never high, because this register bit preventsthe corresponding interrupt to be caught by the sticky bitstatus interrupt. 1'b0: Interrupt is not masked

HDMI_RX_IFORCE_CB_DD

Address: Operational Base + offset (0x3208)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	WO	0x0	FORCE_POWERSTATE powerstate interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit. 1'b0: No action.
4	WO	0x0	FORCE_WAKEPULSE_FAIL wakepulse_fail interrupt force (see corresponding status bit for this interrupt description) 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit. 1'b0: No action.
3	WO	0x0	FORCE_DISCOVERYPULSE_FAIL discoverypulse_fail interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit. 1'b0: No action
2	WO	0x0	FORCE_VBUS_VALID vbus_valid interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit. 1'b0: No action
1	WO	0x0	FORCE_CONNECTED connected interrupt force (see corresponding status bit forthis interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit. 1'b0: No action
0	WO	0x0	FORCE_ATTACHED attached interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit. 1'b0: No action

HDMI_RX_ICLEAR_CB_DD
Address: Operational Base + offset (0x320c)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	WO	0x0	CLEAR_POWERSTATE powerstate interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action.
4	WO	0x0	CLEAR_WAKEPULSE_FAIL wakepulse_fail interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action.
3	WO	0x0	CLEAR_DISCOVERYPULSE_FAIL discoverypulse_fail interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action.
2	WO	0x0	CLEAR_VBUS_VALID vbus_valid interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action.
1	WO	0x0	CLEAR_CONNECTED connected interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action.
0	WO	0x0	CLEAR_ATTACHED attached interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action.

HDMI_RX_IMUTE_CB_DD

Address: Operational Base + offset (0x3210)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x1	MUTE_POWERSTATE powerstate interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action. Note: Muting the interrupt does not prevent the interruptstatus bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor.
4	RW	0x1	MUTE_WAKEPULSE_FAIL wakepulse_fail interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action. Note: Muting the interrupt does not prevent the interruptstatus bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor.
3	RW	0x1	MUTE_DISCOVERYPULSE_FAIL discoverypulse_fail interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action. Note: Muting the interrupt does not prevent the interruptstatus bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor.
2	RW	0x1	MUTE_VBUS_VALID vbus_valid interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action. Note: Muting the interrupt does not prevent the interruptstatus bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor.

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Bit	Attr	Reset Value	Description
1	RW	0x1	MUTE_CONNECTED connected interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action. Note: Muting the interrupt does not prevent the interruptstatus bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor.
0	RW	0x1	MUTE_ATTACHED attached interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action. Note: Muting the interrupt does not prevent the interruptstatus bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor.

HDMI_RX_ISTAT_CB_LL

Address: Operational Base + offset (0x3220)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RO	0x0	RXFIFOXFERBUSY Receiver FIFO busy status change (refer to st_rxfifoxferbusy for more information): 1'b1: A change to st_rxfifoxferbusy value has occurred. 1'b0: No Change on st_rxfifoxferbusy value
16	RO	0x0	TXFIFOXFERINITFAIL A TX transfer initialization request was issued (txfifoxferinit=1), but has been canceled due to an ongoing RX transfer
15	RO	0x0	RXFIFOOVERFLOW_B An initiator device has caused a protocol error violating NMAX consecutive packet transmission (for FIFO B).
14	RO	0x0	RXFIFOOVERFLOW_A An initiator device has caused a protocol error violating NMAX consecutive packet transmission (for FIFO A)
13	RW	0x0	RXFIFOREADY_B Receiver FIFO B is ready to be read by Translation Layer. When this interrupt is flagged, the first packet in FIFO A is already available at rxpckcontent_b[11:0] and should be read first, before pulsing rxpckfiforead_b

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Bit	Attr	Reset Value	Description
12	RO	0x0	RXFIFOREADY_A Receiver FIFO A is ready to be read by the Translation Layer. When this interrupt is flagged, the first packet in FIFO A is already available at rxpckcontent_a[11:0] and should be read first, before pulsing rxpckfiforead_a
11	RO	0x0	RXPCKINVOPCODE A packet with an invalid Header has been received, and NACK has been sent back (the respective rplyctrl_XXheader register is 0). Actual frequency of this interrupt is controlled by rxpckinvheader_trshld[2:0].
10	RO	0x0	RXPCKINVHEADER A packet with an invalid Header has been received, and NACK has been sent back (the respective rplyctrl_XXheader register is 0). Actual frequency of this interrupt is controlled by rxpckinvheader_trshld[2:0]
9	RO	0x0	RXPCKINCOMPLETE Link Layer has received a SYNC symbol and is expecting 12 bits of packet data. This interrupt is raised in the following situations: ■ a) Less than 12 bits are received. ■ b) The two bi-phase symbols for a bit take longer than 1.5 nominal bit times. The two situations can happen if a previous receive error caused the Link Layer to start again and detect a false SYNC during a packet, and the following bits do not make up a complete and time correct packet. Actual frequency of this interrupt is controlled by rxpckincomplete_trshld[2:0]
8	RO	0x0	RXPCKNOSYNC Link Layer detects a line negedge to start a packet, but the initial SYNC symbol never completed within two TBIT_CBUSmax. Actual frequency of this interrupt is controlled by rxpcknosync_trshld[2:0].
7	RO	0x0	RXPCKBADPAR A packet with wrong parity has been received, regardless of 'rplyctrl_badpar' setting.Actual frequency of this interrupt is controlled by rxpckbadpar_trshld[2:0]
6	RO	0x0	TXPCKMAXARBLOST Maximum number of line re-arbitrations was reached(defined by txnarbmax), while st_txfifoxferbusy was high by a packet transmission request
5	RO	0x0	TXNRETRY Maximum number of packet transmission retries after line NACK reached (defined by txnretrymax). The Translation Layer SW must decide to force a new device discovery or just re-initiate the TX transfer

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Bit	Attr	Reset Value	Description
4	RO	0x0	TXPCKCOLLISION Collision detected on CBUS. During transmission of a packet, at the end of each bi-phase symbol, the CBUS datain was sampled with a different value than dataout. Actual frequency of this interrupt is controlled by txpckcollision_trshld[2:0]
3	RO	0x0	TXFIFOOVERFLOW TX FIFO overflow when Translation Layer tried to push one more packet. This write attempt is not stored in the TX FIFO
2	RO	0x0	TXFIFOXFERDONE Transmit transfer done (high when all packets in the TX FIFO have been sent. Implies that a transmit FIFO request has been set first)
1	RO	0x0	TXFIFOEMPTY Transmitter FIFO empty status (high when FIFO goes into empty state)
0	RO	0x0	TXFIFOXFERBUSY Transmitter FIFO busy status change (refer to st_txfifoxferbusy for more information): 1'b1: A change to st_txfifoxferbusy value has occurred. 1'b0: No Change on st_txfifoxferbusy value

HDMI_RX_IMASK_CB_LL

Address: Operational Base + offset (0x3224)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RW	0x1	MASK_RXFIFOXFERBUSY rxfifoxferbusy interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
16	RW	0x1	MASK_TXFIFOXFERINITFAIL txfifoxferinitfail interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked

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Bit	Attr	Reset Value	Description
15	RW	0x1	MASK_RXFIFOOVERFLOW_B rxfifooverflow_b interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
14	RW	0x1	MASK_RXFIFOOVERFLOW_A rxfifooverflow_a interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
13	RW	0x1	MASK_RXFIFOREADY_B rxfifoready_b interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
12	RW	0x1	MASK_RXFIFOREADY_A rxfifoready_a interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
11	RW	0x1	MASK_RXPCKINVOPCODE rxpckinvopcode interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked

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Bit	Attr	Reset Value	Description
10	RW	0x1	MASK_RXPCKINVHEADER rxpckinvheader interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
9	RW	0x1	MASK_RXPCKINCOMPLETE rxpckincomplete interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
8	RW	0x1	MASK_RXPCKNOSYNC rxpcknosync interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
7	RW	0x1	MASK_RXPCKBADPAR rxpckbadpar interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
6	RW	0x1	MASK_TXPCKMAXARBLOST txpckmaxarblost interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked

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Bit	Attr	Reset Value	Description
5	RW	0x1	MASK_TXNRETRY txnretry interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
4	RW	0x1	MASK_TXPCKCOLLISION txpckcollision interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
3	RW	0x1	MASK_TXFIFOOVERFLOW txfifooverflow interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
2	RW	0x1	MASK_TXFIFOXFERDONE txfifoxferdone interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
1	RW	0x1	MASK_TXFIFOEMPTY txfifoempty interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked

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Bit	Attr	Reset Value	Description
0	RW	0x1	MASK_TXFIFOXFERBUSY txfifoxferbusy interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked

HDMI_RX_IFORCE_CB_LL

Address: Operational Base + offset (0x3228)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	WO	0x0	FORCE_RXFIFOXFERBUSY rxfifoxferbusy interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
16	WO	0x0	FORCE_TXFIFOXFERINITFAIL txfifoxferinitfail interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
15	WO	0x0	FORCE_RXFIFOOVERFLOW_B rxfifooverflow_b interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
14	WO	0x0	FORCE_RXFIFOOVERFLOW_A rxfifooverflow_a interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action

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Bit	Attr	Reset Value	Description
13	WO	0x0	FORCE_RXFIFOREADY_B rxfifoready_b interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
12	WO	0x0	FORCE_RXFIFOREADY_A rxfifoready_a interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
11	WO	0x0	FORCE_RXPCKINVOPCODE rxpckinvopcode interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
10	WO	0x0	FORCE_RXPCKINVHEADER rxpckinvheader interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
9	WO	0x0	FORCE_RXPCKINCOMPLETE rxpckincomplete interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
8	WO	0x0	FORCE_RXPCKNOSYNC rxpcknosync interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action

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Bit	Attr	Reset Value	Description
7	WO	0x0	FORCE_RXPCKBADPAR rxpckbadpar interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
6	WO	0x0	FORCE_TXPCKMAXARBLOST txpckmaxarblost interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
5	WO	0x0	FORCE_TXNRETRY txnretry interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
4	WO	0x0	FORCE_TXPCKCOLLISION txpckcollision interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
3	WO	0x0	FORCE_TXFIFOOVERFLOW txfifooverflow interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
2	WO	0x0	FORCE_TXFIFOXFERDONE txfifoxferdone interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action

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Bit	Attr	Reset Value	Description
1	WO	0x0	FORCE_TXFIFOEMPTY txfifoempty interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action
0	WO	0x0	FORCE_TXFIFOXFERBUSY txfifoxferbusy interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit 1'b0: No action

HDMI_RX_ICLEAR_CB_LL

Address: Operational Base + offset (0x322c)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	WO	0x0	CLEAR_RXFIFOXFERBUSY rxfifoxferbusy interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
16	WO	0x0	CLEAR_TXFIFOXFERINITFAIL txfifoxferinitfail interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
15	WO	0x0	CLEAR_RXFIFOOVERFLOW_B rxfifooverflow_b interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
14	WO	0x0	CLEAR_RXFIFOOVERFLOW_A rxfifooverflow_a interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
13	WO	0x0	CLEAR_RXFIFOREADY_B rxfifoready_b interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action

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Bit	Attr	Reset Value	Description
12	WO	0x0	CLEAR_RXFIFOREADY_A rxfifoready_a interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
11	WO	0x0	CLEAR_RXPCKINVOPCODE rxpckinvopcode interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
10	WO	0x0	CLEAR_RXPCKINVHEADER rxpckinvheader interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
9	WO	0x0	CLEAR_RXPCKINCOMPLETE rxpckincomplete interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
8	WO	0x0	CLEAR_RXPCKNOSYNC rxpcknosync interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
7	WO	0x0	CLEAR_RXPCKBADPAR rxpckbadpar interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
6	WO	0x0	CLEAR_TXPCKMAXARBLOST txpckmaxarblost interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
5	WO	0x0	CLEAR_TXNRETRY txnretry interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
4	WO	0x0	CLEAR_TXPCKCOLLISION txpckcollision interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action

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Bit	Attr	Reset Value	Description
3	WO	0x0	CLEAR_TXFIFOOVERFLOW txfifooverflow interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
2	WO	0x0	CLEAR_TXFIFOXFERDONE txfifoxferdone interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
1	WO	0x0	CLEAR_TXFIFOEMPTY txfifoempty interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
0	WO	0x0	CLEAR_TXFIFOXFERBUSY txfifoxferbusy interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action

HDMI_RX_IMUTE_CB_LL

Address: Operational Base + offset (0x3230)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RW	0x1	MUTE_RXFIFOXFERBUSY rxfifoxferbusy interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
16	RW	0x1	MUTE_TXFIFOXFERINITFAIL txfifoxferinitfail interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor

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Bit	Attr	Reset Value	Description
15	RW	0x1	MUTE_RXFIFOOVERFLOW_B rxfifooverflow_b interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
14	RW	0x1	MUTE_RXFIFOOVERFLOW_A rxfifooverflow_a interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
13	WO	0x1	MUTE_RXFIFOREADY_B rxfifoready_b interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
12	WO	0x1	MUTE_RXFIFOREADY_A rxfifoready_a interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
11	WO	0x1	MUTE_RXPCKINVOPCODE rxpckinvopcode interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor

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Bit	Attr	Reset Value	Description
10	WO	0x1	MUTE_RXPCKINVHEADER rxpckinvheader interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
9	RW	0x1	MUTE_RXPCKINCOMPLETE rxpckincomplete interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
8	WO	0x1	MUTE_RXPCKNOSYNC rxpcknosync interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
7	RW	0x1	MUTE_RXPCKBADPAR rxpckbadpar interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor

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Bit	Attr	Reset Value	Description
6	RW	0x1	MUTE_TXPCKMAXARBLOST txpckmaxarblost interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
5	WO	0x1	MUTE_TXNRETRY txnretry interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
4	WO	0x1	MUTE_TXPCKCOLLISION txpckcollision interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
3	WO	0x1	MUTE_TXFIFOOVERFLOW txfifooverflow interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor

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Bit	Attr	Reset Value	Description
2	WO	0x1	MUTE_TXFIFOXFERDONE txfifoxferdone interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
1	RW	0x1	MUTE_TXFIFOEMPTY txfifoempty interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor
0	WO	0x1	MUTE_TXFIFOXFERBUSY txfifoxferbusy interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor

HDMI_RX_ISTAT_CB_HDCP

Address: Operational Base + offset (0x3240)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	CBHDCP_DONE Asserted when an HDCP register read or write operation is completed, and status bit hdcp_busy_sts changes to low.

HDMI_RX_IMASK_CB_HDCP

Address: Operational Base + offset (0x3244)

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	MASK_CBHDCP_DONE Interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: Interrupt is not masked

HDMI_RX_IFORCE_CB_HDCP

Address: Operational Base + offset (0x3248)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	FORCE_CBHDCP_DONE Interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, the user must then act over the corresponding clear interrupt bit. 1'b0: No action

HDMI_RX_ICLEAR_CB_HDCP

Address: Operational Base + offset (0x324c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	CLEAR_CBHDCP_DONE Interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action

HDMI_RX_IMUTE_CB_HDCP

Address: Operational Base + offset (0x3250)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x1	MUTE_CBHDCP_DONE Interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC application processor

HDMI_RX_ISTAT_CB_MCTRL

Address: Operational Base + offset (0x3260)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RO	0x0	CB_REGBANK_READY CBUS register bank ready to be accessed (This interrupt is triggered after successful CBUS register bank reset completion triggered by an iponrst_n or cbusswresetreq.cbmain_swresetreq action and after release of synchronous enable cbusenableif.cbmain_enable.)
15:1	RO	0x0	reserved
0	RO	0x0	REF_LOC_AVAIL irefclk Lock On Clock status. Indicates the clock is present in the system

HDMI_RX_IMASK_CB_MCTRL

Address: Operational Base + offset (0x3264)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	MASK_CB_REGBANK_READY cb_regbank_ready interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked
15:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x1	MASK_REF_LOC_AVAIL ref_loc_avail interrupt mask (see corresponding status bit for this interrupt description): 1'b1: Mask interrupt. This means that the corresponding status bit is never high, because this register bit prevents the corresponding interrupt to be caught by the sticky bit status interrupt. 1'b0: interrupt is not masked

HDMI_RX_IFORCE_CB_MCTRL

Address: Operational Base + offset (0x3268)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	FORCE_CB_REGBANK_READY cb_regbank_ready interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, you must act over the corresponding clear interrupt bit. 1'b0: No action
15:1	RO	0x0	reserved
0	WO	0x0	FORCE_REF_LOC_AVAIL ref_loc_avail interrupt force (see corresponding status bit for this interrupt description): 1'b1: Force interrupt. The corresponding status bit is set high. To clear the interrupt, you must act over the corresponding clear interrupt bit. 1'b0: No action

HDMI_RX_ICLEAR_CB_MCTRL

Address: Operational Base + offset (0x326c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	CLEAR_CB_REGBANK_READY cb_regbank_ready interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action
15:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	WO	0x0	CLEAR_REF_LOC_AVAIL ref_loc_avail interrupt clear (see corresponding status bit for this interrupt description): 1'b1: Clear interrupt. The corresponding status bit is cleared. 1'b0: No action

HDMI_RX_IMUTE_CB_MCTRL

Address: Operational Base + offset (0x3270)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	MUTE_CB_REGBANK_READY cb_regbank_ready interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC
15:1	RO	0x0	reserved
0	RW	0x0	MUTE_REF_LOC_AVAIL ref_loc_avail interrupt mute (see corresponding status bit for this interrupt description): 1'b1: Mute interrupt. The corresponding status bit interrupt is not taken into account to raise the global interrupt line. 1'b0: No action Note: Muting the interrupt does not prevent the interrupt status bit to be set high but avoids this corresponding interrupt to raise the global interrupt line to the SoC

HDMI_RX_IMASTER_MUTE_CB

Address: Operational Base + offset (0x32e0)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	MASTER_MUTE_CB CBUS interrupt master mute: 1'b1: Mutes all interrupts. This prevents the interrupt line(s) from going high by any incoming interrupt. 1'b0: No action

HDMI_RX_IVECTOR_INDEX_CB

Address: Operational Base + offset (0x32e4)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RC	0x0	IACT_CB_MCTRL CBUS Main Controller interrupt vector activity: 1'b1: One of the interrupts in the CBUS Main Controller interrupt vector changed since the last read to this interrupt vector activity register. 1'b0: The interrupts in the CBUS Main Controller interrupt vector did not change since the last read to this interrupt vector activity register. Note: This register is cleared on read.
2	RC	0x0	IACT_HDCP CBUS HDCP interrupt vector activity: 1'b1: One of the interrupts in HDCP Interface interrupt vector changed since the last read to this interrupt vector activity register. 1'b0: The interrupts in the HDCP Interface interrupt vector did not change since the last read to this interrupt vector activity register. Note: This register is cleared on read.
1	RC	0x0	IACT_LL CBUS Link Layer interrupt vector activity: 1'b1: One of the interrupts in Link Layer interrupt vector changed since the last read to this interrupt vector activity register. 1'b0: The interrupts in the Link Layer interrupt vector did not change since the last read to this interrupt vector activity register. Note: This register is cleared on read.
0	RO	0x0	IACT_DD CBUS Device Discovery interrupt vector activity: 1'b1: One of the interrupts in the Device Discover interrupt vector changed since the last read to this interrupt vector activity register. 1'b0: The interrupts in the Device Discover interrupt vector did not change since the last read to this interrupt vector activity register. Note: This register is cleared on read.

9.8 Application Notes

This chapter describes how to bring up HDMI rx in your system. As shown few examples below, these introduce the basically HDMI rx application.
You can easily configure these functions with proper registers value setting by HDMI RX APB BUS or i2c bus.

9.8.1 Initial Operation

The hornet hdmirx config process below.

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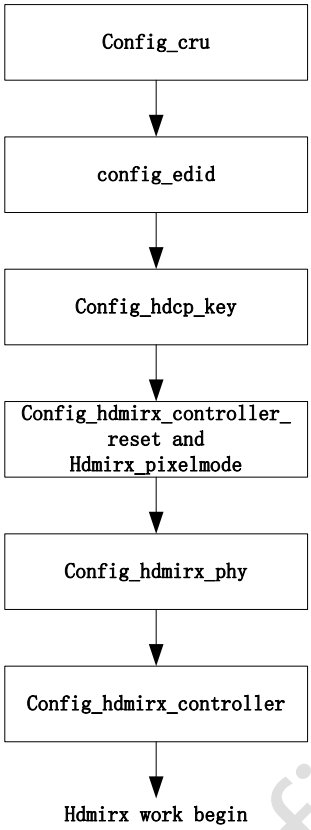

Fig. 9-11 HDMI RX config process

Config hdmirx_controller_reset and hdmirx_pixelmode is the first step for hdmirx controller config, but it must be priority to hdmirx_phy config, because the original config process make the hdmirx output "x" status in the first frame, and it is a bug.

The config hdmirx controller reset and hdmirx_pixelmode reg config process below. The addr is the offset addr.

word32(HDMI_RX_BASE+HDMI_RX_DMI_DISABLE_IF) = 0x00000000; //config DMI_DISABLE_IF

word32(HDMI_RX_BASE+HDMI_RX_DMI_DISABLE_IF) = 0x000001ff; //config DMI_DISABLE_IF

word32(HDMI_RX_BASE+HDMI_RX_DMI_DISABLE_IF) = 0x000101ff; //config DMI_SW_RST

word32(HDMI_RX_BASE+HDMI_RX_HDMI20_CONTROL) = 0x10001f10; //config HDMI20_CONTROL

when config register through apb bus,we must ensure the period between DMI_SW_RST and HDMI20_CONTROL configuration.

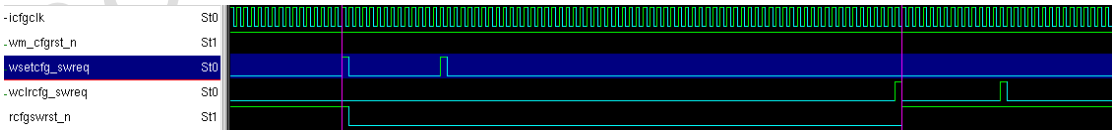

Fig. 9-12 HDMI RX reset timing

After config DMI_SW_RST, it will drive low rcfgwrst_n about 30 imodetclk cycle, and synchronize to icfgclk domain. So it depends on the imodetclk and icfgclk period width, we must ensure the rcfgwrst_n drive high again, before we config HDMI20_CONTROL. RK628D config register through i2c bus, so the next two register configuration period will be long enough.

The process of config rx phy in next diagram.Because the format and the colordepth of the input video stream is unknown,so we apply the roundrobin strategy.

The bit8 of hdmirx reg scdc_regs1(the reg addr is HDMI_RX_SCDC_REGS1) is itmdsvalid,which indicates hdmirx phy pixelclk and tmdsclk valid.

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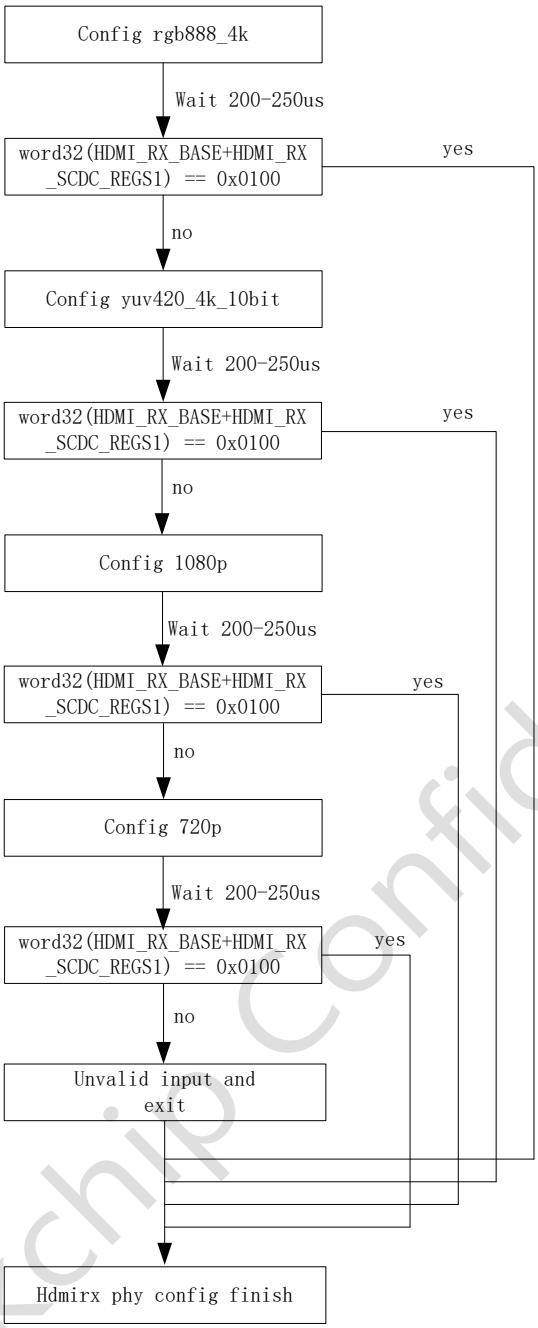

Fig. 9-13 HDMI RX roundrobin config

9.8.2 config cru

cru config process just config apb clk and hdmirx audio clk pll parameter(if hdmi rx audio clk is config manual).

word32(CRU_BASE+CRU_MODE_CON00) = 0x0005_0005;
word32(CRU_BASE+CRU_CLKSEL_CON00) = 0x000b_000b; //apb clk div
word32(CRU_BASE+CRU_CLKSEL_CON05)= (0x3fc0<<16) | ((audio_freq_div&0xff)<<6); //audio clk div

The calculation formula of audio_freq_div[7:0] just like this.

freq_audio = N/(CTS/pixelclk)

audio_freq_div = (983.04/freq_audio) - 1

N and CTS is config in case，pixelclk is hdmi_rx pixelclk frequency。The critical value of audio_freq_div is 0x9f.

9.8.3 Config hdmi rx phy

(1) 1080p(hdmiclk 148.5M)

rxphy_rdata=word32(RXPHY_BASE+0x6630);
word32(RXPHY_BASE+0x6630)=rxphy_rdata&0xffffff6;

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```
delay_ns(1000);
word32(RXPHY_BASE+0x66a8) = 0x0000_c600;
word32(RXPHY_BASE+0x6624) = 0x0e00_0007;
word32(RXPHY_BASE+0x6628) = 0x0000_0881;
word32(RXPHY_BASE+0x66f0) = 0x0000_7f05;
word32(RXPHY_BASE+0x66a0) = 0x0000_0003;
word32(RXPHY_BASE+0x66b0) = 0x0008_0098;
word32(RXPHY_BASE+0x66a0) = 0x0000_0083;
word32(RXPHY_BASE+0x66b0) = 0x0038_0098;
word32(RXPHY_BASE+0x66b4) = 0x8000_0000;
wait(word32(HDMI_RX_BASE + HDMI_RX_SCDC_REGS1) == 0x0100);
hdmirx_phy_config_done = 1'b1;
```

After config hdmirx phy, we must wait the hdmi_rx_scdc_regs1 is 0x0100, it indicates the phy has been active, and the pin_hdrx_tmdsclk and pin_hdrx_pclk has been recovery.

(2) 4k 30p(hdmiclk 297M)

```
rxphy_rdata=word32(RXPHY_BASE+0x6630);
word32(RXPHY_BASE+0x6630)=rxphy_rdata&0xffffff6;
delay_ns(1000);
word32(RXPHY_BASE+0x66a8) = 0x0000_c600;
word32(RXPHY_BASE+0x6624) = 0x0e00_0007;
word32(RXPHY_BASE+0x6628) = 0x0000_0881;
word32(RXPHY_BASE+0x66f0) = 0x0000_7f05;
word32(RXPHY_BASE+0x66a0) = 0x0000_0003;
word32(RXPHY_BASE+0x66b0) = 0x0008_0098;
word32(RXPHY_BASE+0x66a0) = 0x0000_0083;
word32(RXPHY_BASE+0x66b0) = 0x0038_0098;
word32(RXPHY_BASE+0x66b4) = 0x8000_0000;
wait(word32(HDMI_RX_BASE + HDMI_RX_SCDC_REGS1) == 0x0100);
hdmirx_phy_config_done = 1'b1;
```

After config hdmirx phy, we must wait the hdmi_rx_scdc_regs1 is 0x0100, it indicates the phy has been active, and the pin_hdrx_tmdsclk and pin_hdrx_pclk has been recovery.

When hdmiclk<340M,include 297M/148.5M,74.25M and so on,the configuration process is all the same.

9.8.4 Config edid

Edid sram is 256x8bit.

```
word32(GRF_BASE + GRF_SYSTEM_CON1) = 0x0e000100;
word32(GRF_BASE + GRF_SYSTEM_CON0) = 0x00300018;
word32(ADAPTER_BASE+0x00000000*4)=0x10;//write edid begin,first edid data
... //total 256 edid data
word32(ADAPTER_BASE+0x000000ff*4)=0x10;//write edid begin,last edid data
```

9.8.5 Config hdcp key

HDCP sram is 292x8bit.

```
#define ADAPTER_HDCP_BASE   0x800a8000
int sw_system_con0
sw_system_con0 = word32(GRF_BASE+GRF_SYSTEM_CON0);
word32(GRF_BASE + GRF_SYSTEM_CON0) = (sw_system_con0&0xffffeff) | (0x1<<8);
word32(ADAPTER_HDCP_BASE+0x0*4)=0x0000_0000;//write hdcp key begin
word32(ADAPTER_HDCP_BASE+0x1*4)=RX_HDCP_BKSV&0xff;
word32(ADAPTER_HDCP_BASE+0x2*4)=(RX_HDCP_BKSV>>8)&0xff;
word32(ADAPTER_HDCP_BASE+0x3*4)=(RX_HDCP_BKSV>>16)&0xff;
word32(ADAPTER_HDCP_BASE+0x4*4)=(RX_HDCP_BKSV>>24)&0xff;
word32(ADAPTER_HDCP_BASE+0x5*4)=(RX_HDCP_BKSV>>32)&0xff;
word32(ADAPTER_HDCP_BASE+0x6*4)=0x0;
word32(ADAPTER_HDCP_BASE+0x7*4)=0x0;
```

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```
word32(ADAPTER_HDCP_BASE+0x8*4)=0x0;
word32(ADAPTER_HDCP_BASE+0x9*4)=RX_HDCP_KEY0&0xff;
word32(ADAPTER_HDCP_BASE+0xa*4)=(RX_HDCP_KEY0>>8)&0xff;
word32(ADAPTER_HDCP_BASE+0xb*4)=(RX_HDCP_KEY0>>16)&0xff;
word32(ADAPTER_HDCP_BASE+0xc*4)=(RX_HDCP_KEY0>>24)&0xff;
word32(ADAPTER_HDCP_BASE+0xd*4)=(RX_HDCP_KEY0>>32)&0xff;
word32(ADAPTER_HDCP_BASE+0xe*4)=(RX_HDCP_KEY0>>40)&0xff;
word32(ADAPTER_HDCP_BASE+0xf*4)=(RX_HDCP_KEY0>>48)&0xff;
word32(ADAPTER_HDCP_BASE+0x10*4)=RX_HDCP_KEY1&0xff;
....
word32(ADAPTER_HDCP_BASE+0x11A*4)=RX_HDCP_KEY39&0xff;
word32(ADAPTER_HDCP_BASE+0x11B*4)=(RX_HDCP_KEY39>>8)&0xff;
word32(ADAPTER_HDCP_BASE+0x11C*4)=(RX_HDCP_KEY39>>16)&0xff;
word32(ADAPTER_HDCP_BASE+0x11D*4)=(RX_HDCP_KEY39>>24)&0xff;
word32(ADAPTER_HDCP_BASE+0x11E*4)=(RX_HDCP_KEY39>>32)&0xff;
word32(ADAPTER_HDCP_BASE+0x11F*4)=(RX_HDCP_KEY39>>40)&0xff;
word32(ADAPTER_HDCP_BASE+0x120*4)=(RX_HDCP_KEY39>>48)&0xff;
word32(ADAPTER_HDCP_BASE+0x121*4)=0x0;
word32(ADAPTER_HDCP_BASE+0x122*4)=0x0;
word32(ADAPTER_HDCP_BASE+0x123*4)=0x0;//config hdcp key finish
```

9.8.6 4k case example

```
parameter H_ACTIVE                  = 3840;
parameter H_BLANK                   = 560;
parameter H_SYNC_DELAY              = 176;
parameter H_SYNC_WIDTH              = 88;
parameter V_ACTIVE                  = 32;
parameter V_BLANK                   = 90;
parameter V_SYNC_DELAY              = 8;
parameter V_SYNC_WIDTH              = 10;
parameter VIDEO_FREQ                = 60000;
parameter DE_POLARITY               = 1'b1;
//parameter H_SYNC_POLARITY           = 1'b1;
//parameter V_SYNC_POLARITY           = 1'b1;
parameter H_SYNC_POLARITY           = 1'b0;
parameter V_SYNC_POLARITY           = 1'b0;

parameter VG_H_ACTIVE               = 3840;
parameter VG_H_BLANK                = 560;
parameter VG_H_SYNC_DELAY           = 176;
parameter VG_H_SYNC_WIDTH           = 88;
parameter VG_V_ACTIVE               = 32;
parameter VG_V_BLANK                = 90;
parameter VG_V_SYNC_DELAY           = 8;
parameter VG_V_SYNC_WIDTH           = 10;

parameter N_FRAMES       = 2;
//parameter CONFIG_IF_FREQ = 120.0e6;
//parameter MODEDET_FREQ   = 45000000.00;
parameter CONFIG_IF_FREQ = 99.0e6;
parameter MODEDET_FREQ   = 49060000.00;
parameter APBCLK_FREQ    = 124000000.0;

parameter DEFAULT_PHASE = 1'b1;
parameter COLOR_DEPTH   = 4'b0100;
parameter SET_AVMUTE    = 1'b0;
parameter CLEAR_AVMUTE  = 1'b0;

parameter VP_YCC422_EN              = 1'b0;
parameter RGB_YCC_INDICATOR    =  3'b000;
```

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```
`ifdef HRX_PVO_REMAP
parameter PVO_REMAP_DUAL_PIXEL    =  1'b1;
parameter PVO_REMAP_PVO1_UNMUTE   =  1'b0;
`endif
```

color_depth:4’b0100 is 24 bit one pixel
4’b0101 is 30bit one pixel
4’b0110 is 36bit one pixel
4’b0111 is 48bit one pixel
VP_YCC422_EN: 1’b0 : it is not yuv422
1’b1: it is yuv422
RGB_YCC_INDICATOR : 3’b000 is rgb
3’b001 is yuv422
3’b010 is yuv444
3’b011 is yuv420
PVO_REMAP_DUAL_PIXEL: 1’b1 indicate output mode is dual pixel one cycle.
HDMI_REG_MODE: config 2’h3;

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Chapter 10 TX/RX Adapter

10.1 Overview

RK628D contains various video display interface's TX and RX, among HDMI RX2.0 & HDMI TX1.4 is the main application scenario. This module mainly realizes the interaction between RX and TX in the chip.
There are HPD, EDID, HDCP and CEC that need to interact. It supports following features:

- Interaction of HDP signal between HDMI TX and HDMI RX
- Support HDMI TX CEC function.
- Support RX HDCP1.3 inside-key memory. It is readable and writable
- Support HDMI RX/TX HDCP function
- Support on-chip EDID memory. It is readable and writable

10.2 Block Diagram

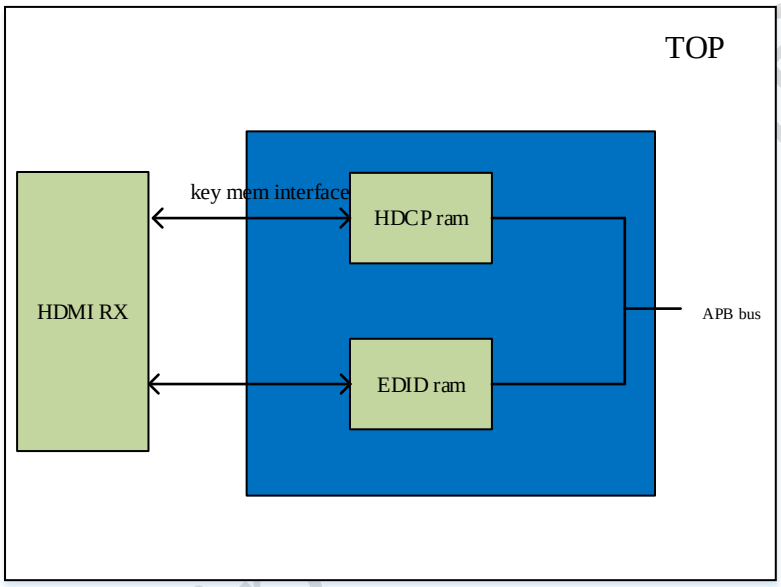

Fig. 10-1 TXRX Adapter Block Diagram

I2C2APB
Connect to I2C interface from RX for reading EDID data from EDID ram.
HDCP ram
SRAM for HDCP key. It can be read and written through APB bus.
EDID ram
SRAM for EDID information. It can be read and written through APB bus.

10.3 Function description

10.3.1 HPD

The process of HPD signal as follows:
(1) TV source initiates HPD to HDMI TX, and HDMI TX receives HPD;
(2) HDMI TX outputs the current HPD state hpd_status (there will be a 100ms detection mechanism to avoid the impact of pulse) to HDMI RX;
(3) HDMI RX decide whether to initiate HPD to AP TX according to the current status of controller and hpd_status.
The connection diagram is as follows:

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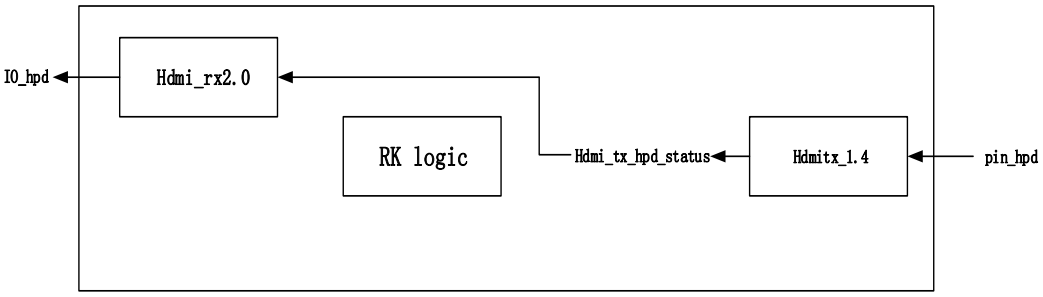

Fig. 10-2 HPD Connection Diagram

10.3.2 CEC

The CEC is HDMI TX's function. AP directly transfers the CEC signal to the output of RK628D, and configures the instructions and data of the CEC through I2C. The diagram is as follows.

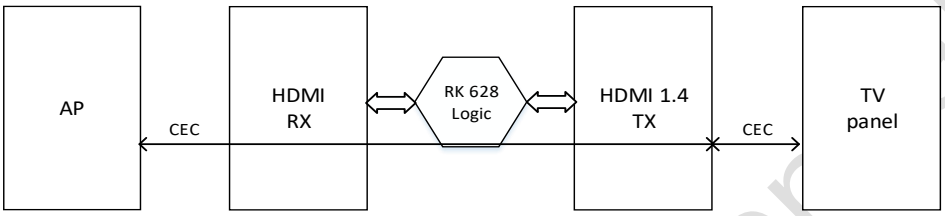

Fig. 10-3 CEC Connection Diagram

The process is as follows:
1. Configure the AP HDMI TX to initiate/receive CEC signals;
2. The CEC signal of AP is directly connected to the CEC interface of HDMI 1.4 TX to complete the transmission and reception of CEC.

10.3.3 EDID

In order to read the EDID information on the screen, AP configures HDMI TX through I2C, and then AP reads the EDID on the screen through the DCC channel of HDMI TX. The diagram is as follows:

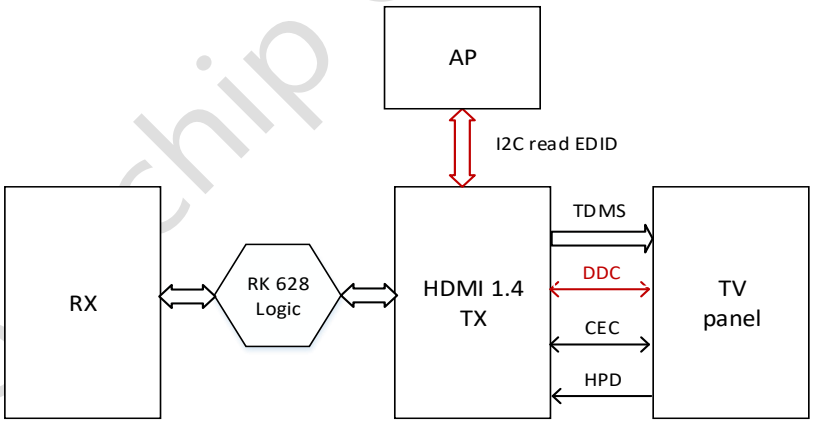

Fig. 10-4 HDMI TX EDID Diagram

Local EDID is stored in RAM. The detailed block diagram is as follows:

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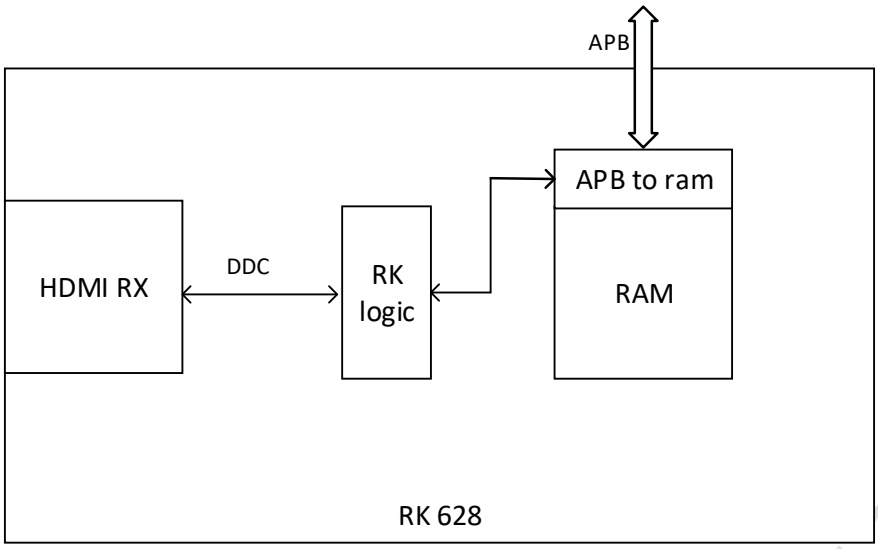

Fig. 10-5 Local EDID Diagram

10.3.4 HDCP

HDMI RX and HDMI TX have their own HDCP processing logic, so RX and TX do not need additional interaction process inside the chip. all the RX require keys to authenticate, encrypt and decrypt, so RAM is built into the chip to store the HDCP key. For HDMI TX, it's HDMP key is written through APB bus configuration, so HDMI TX does not require additional design.

The detailed block diagram is as follows:

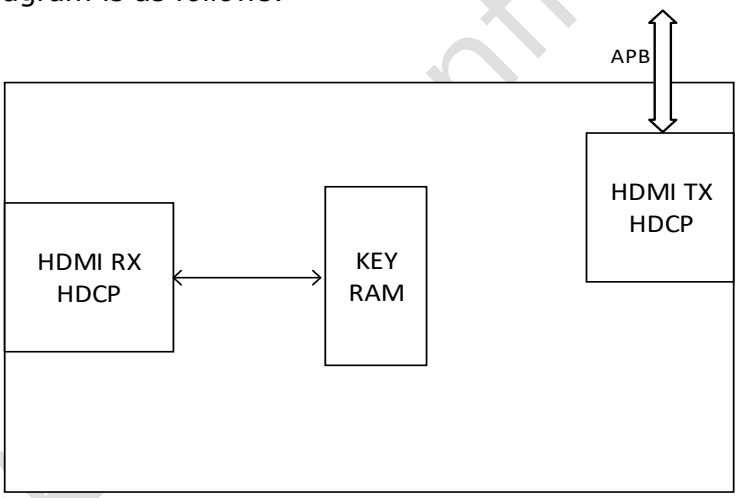

Fig. 10-6 HDCP Key Ram Diagram

10.4 Register Description

This section describes the control/status registers of the design.

10.4.1 Registers Summary

Refer to GRF

10.4.2 Detail Register Description

Refer to GRF

10.5 Application Notes

The base address of EDID ram is 32’h000a_0000;
The base address of HDCP key ram is 32’h000a_8000;
The initial step for EDID and HDCP key ram is as follow:

```
// Edid sram is 256x8bit.
i2cm_write_reg(32’h0000_0010,32’h0030_0000);
i2cm_write_reg(32’h000a_0000,32’h0000_00xx);//write edid begin,first edid data
... //total 256 byte edid data
i2cm_write_reg(32’h000a_00ff,32’h0000_00xx);//write edid begin,last edid data
```

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```
// HDCP sram is 292x8bit.
i2cm_write_reg(32'h0000_0010,32'h0020_0080);
i2cm_write_reg(32'h000a_8000,32'h0000_0000);//write hdcp key begin
i2cm_write_reg(32'h000a_8001,{24'h0,RX_HDCP_BKSV[7:0]});
i2cm_write_reg(32'h000a_8002,{24'h0,RX_HDCP_BKSV[15:8]});
i2cm_write_reg(32'h000a_8003,{24'h0,RX_HDCP_BKSV[23:16]});
i2cm_write_reg(32'h000a_8004,{24'h0,RX_HDCP_BKSV[31:24]});
i2cm_write_reg(32'h000a_8005,{24'h0,RX_HDCP_BKSV[39:32]});
i2cm_write_reg(32'h000a_8006,32'h0000_0000);
i2cm_write_reg(32'h000a_8007,32'h0000_0000);
i2cm_write_reg(32'h000a_8008,32'h0000_0000);
i2cm_write_reg(32'h000a_8009,{24'h0,RX_HDCP_KEY0[7:0]});
i2cm_write_reg(32'h000a_800a,{24'h0,RX_HDCP_KEY0[15:8]});
i2cm_write_reg(32'h000a_800b,{24'h0,RX_HDCP_KEY0[23:16]});
i2cm_write_reg(32'h000a_800c,{24'h0,RX_HDCP_KEY0[31:24]});
i2cm_write_reg(32'h000a_800d,{24'h0,RX_HDCP_KEY0[39:32]});
i2cm_write_reg(32'h000a_800e,{24'h0,RX_HDCP_KEY0[47:40]});
i2cm_write_reg(32'h000a_800f,{24'h0,RX_HDCP_KEY0[55:48]});
i2cm_write_reg(32'h000a_8010,{24'h0,RX_HDCP_KEY1[7:0]});
....
i2cm_write_reg(32'h000a_811A,{24'h0,RX_HDCP_KEY39[7:0]});
i2cm_write_reg(32'h000a_811B,{24'h0,RX_HDCP_KEY39[15:8]});
i2cm_write_reg(32'h000a_811C,{24'h0,RX_HDCP_KEY39[23:16]});
i2cm_write_reg(32'h000a_811D,{24'h0,RX_HDCP_KEY39[31:24]});
i2cm_write_reg(32'h000a_811E,{24'h0,RX_HDCP_KEY39[39:32]});
i2cm_write_reg(32'h000a_811F,{24'h0,RX_HDCP_KEY39[47:40]});
i2cm_write_reg(32'h000a_8120,{24'h0,RX_HDCP_KEY39[55:48]});
i2cm_write_reg(32'h000a_8121,32'h0000_0000);
i2cm_write_reg(32'h000a_8122,32'h0000_0000);
i2cm_write_reg(32'h000a_8123,32'h0000_0000);//config hdcp key finish
i2cm_write_reg(32'h0000_0010,32'h0020_0000);
```

For the CEC configuration, refer to CH10 HDMI TX.

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For HDMI RX2.0 to HDMI TX1.4 scenario, the processing flow is as follows:

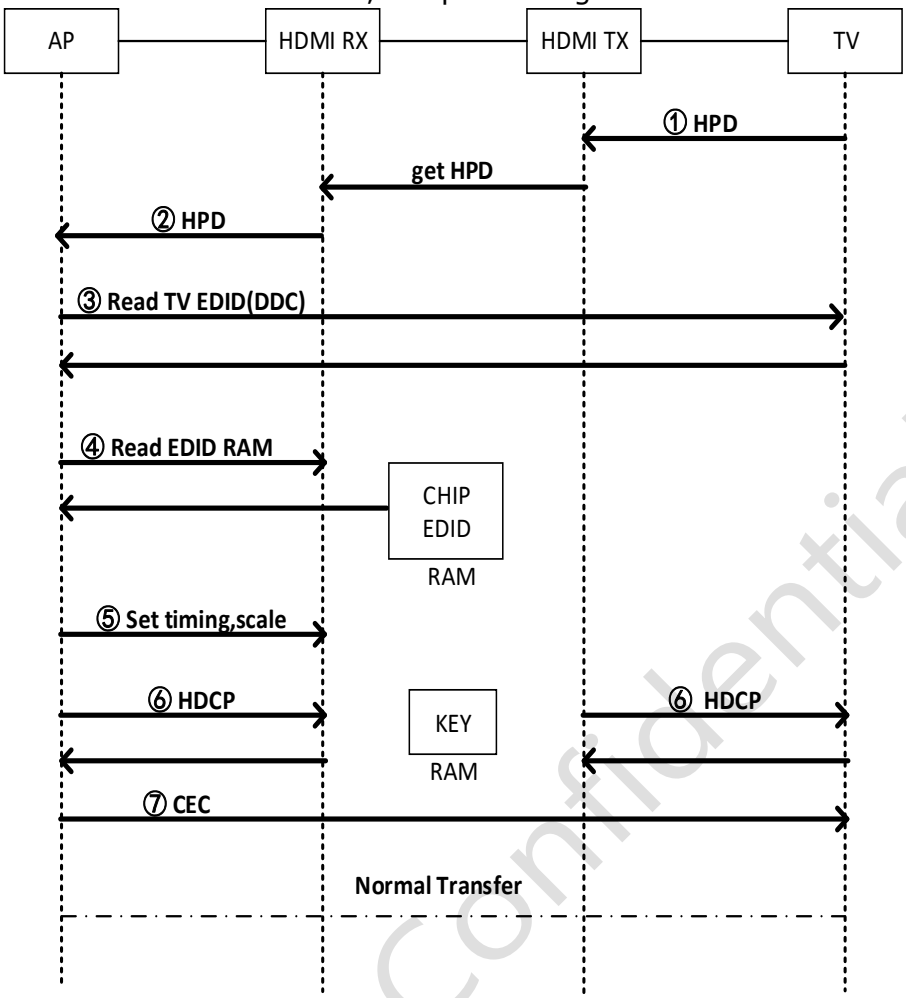

Fig.10-7 HDMI RX to HDMI TX Diagram

The steps shown in the figure are as follows:

①The plug-in device starts to use, TV initiates HPD to RK628D HDMI TX, HDMI TX outputs HDP status to HDMI RX;

② HDMI RX receives HPD status, RK628D HDMI RX initiates HPD to AP, AP recognizes that HPD is successful and hot plug process is over;

③ AP directly configures HDMI TX through I2C bus to initiate the task of Read TV EDID. HDMI TX reads the EDID of screen through DDC and outputs it to top-level AP;

④ The EDID of RK628D stored in RAM is read by AP through I2C bus;

⑤ AP configuration RK628D Timing, Scale and other information;

⑥ HDCP authentication, the interactive part is AP to RK628D RX, RK628D TX to TV, can be seen as two sets of independent HDCP;

⑦ If the CEC command needs to be issued, AP directly transfers the CEC signal to the output of RK628D, and directly interacts with CEC through i2c, including the reading and writing of CEC data.

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For DP RX to HDMI TX1.4 scenario, the processing flow is as follows:

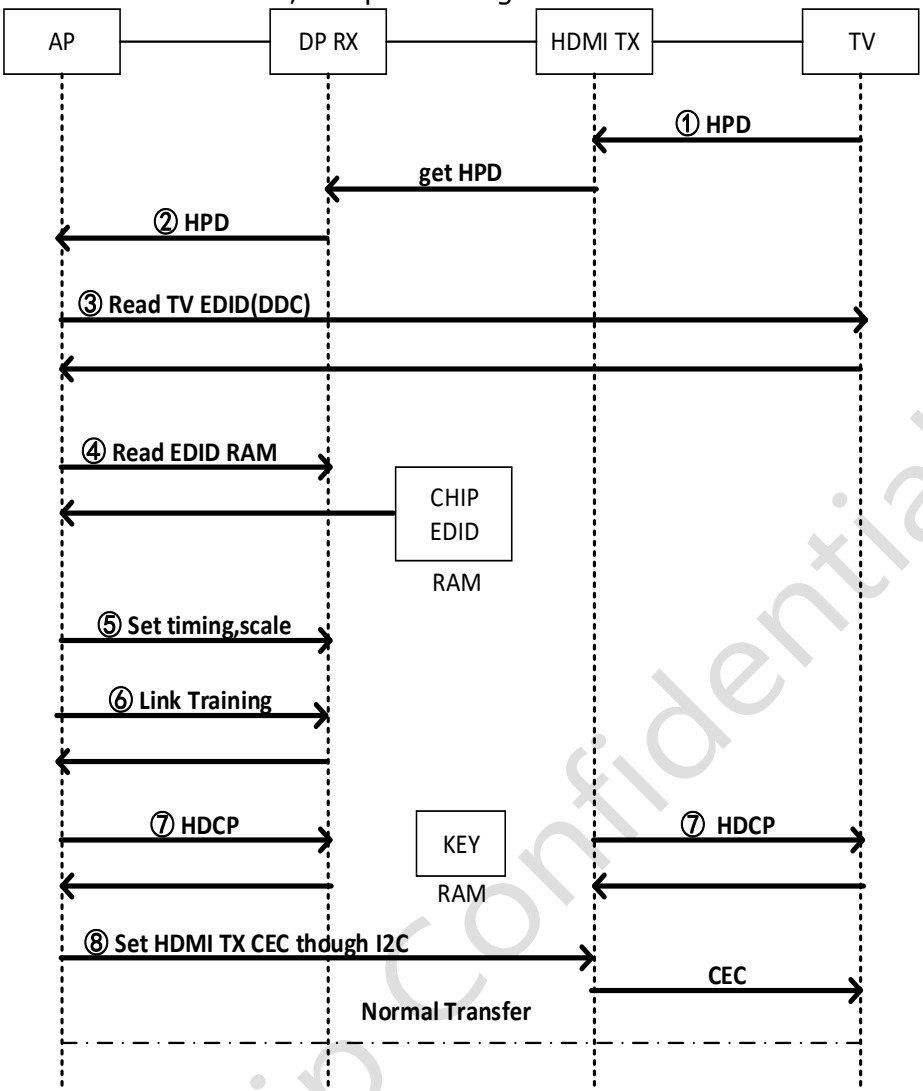

Fig.10-8 DP RX to HDMI TX Diagram

The steps shown in the figure are as follows:
① the plug-in device starts to use, TV initiates HPD to RK628D HDMI TX, HDMI TX outputs HDP status to HDMI RX;
② HDMI RX receives HPD status, RK628D DP RX initiates HPD to AP, AP recognizes that HPD is successful and hot plug process is over;
③ AP directly configures HDMI TX through I2C bus to initiate the task of Read TV EDID. HDMI TX reads the EDID of screen through DDC and outputs it to top-level AP;
④ The EDID of RK628D stored in RAM is read by AP through I2C bus;
⑤ AP configuration RK628D Timing, Scale and other information;
⑥ Read and write DPCD for link training and train the link until it is successful;
⑦ HDCP authentication, the interactive part is AP to RK628D RX, RK628D TX to TV, can be seen as two sets of independent HDCP;
⑧ If CEC commands need to be issued, AP first reads the DPCD register of CEC capability in DP RX, gets that current DP RX does not support CEC, then AP switches to configure the CEC controller of HDMI TX through I2C bus to send and receive CEC instructions and data.

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Chapter 11 Post Process

11.1 Overview

Post process includes color space converter, scaler and spliter.
Color space converter used to convert color space between YUV domain and RGB domain.
Scaler is a synchronous parallel RGB frame converter for different resolution.
The input and output of SCALER should be parallel RGB interface. The output timing settings are programmable due to different display resolution. The frame frequency of output frame must be the same with the input frame. So the output pixel clock frequency (from PLL) should be set to fit this condition.
Spliter is a sharding module that split one screen into two screens.

- CSC
  - RGB2YUV
  - YUV2RGB
  - YUV2VYU
- Display interface
  - Parallel display Interface: 30-bit(RGB/YUV)
  - Asynchronous output pixel clock (PLL required)
  - Flexible display timing setting
  - Configurable border black area
- Scaling down
  - Max input resolution: 4096x2160
  - Arbitrary non-integer scaling ratio
  - Support two mode: bilinear and average
  - Max 1/4 scaling ratio for bilinear scaling down
  - Max 1/6 scaling ratio for average scaling down
- Scaling up
  - Max output resolution: 4096x2160
  - Arbitrary non-integer scaling ratio
  - Support four scaling up mode for different effect
  - Max 6 scaling ratio
- Split
  - Left-right mode

11.2 Block Diagram

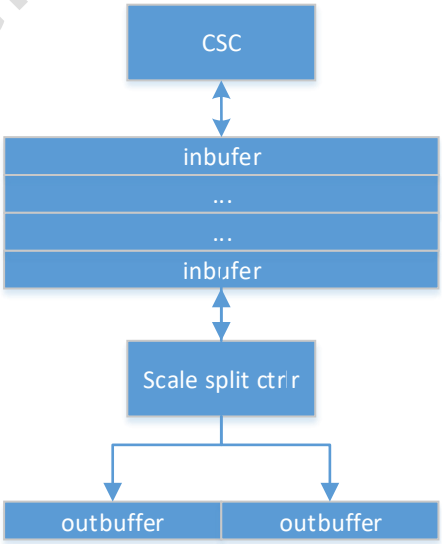

Fig. 11-1 Block diagram of Post process

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11.3 Function Description

11.3.1 Color space conversion

There are 3 standards for YUV2RGB , RGB2YUV and YUV2VYU.

1. YUV to RGB(BT2020)
   R = 1.1636(Y-64) + 1.6778(V-512)
   G = 1.1636(Y-64) - 0.1872(U-512) - 0.6501(V-512)
   B = 1.1636(Y-64) + 2.1406(U-512)

2. RGB to YUV(BT2020)
   Y = 0.2250R + 0.5807G + 0.0508B + 64
   Cb = -0.1223R - 0.3157G + 0.4380B + 512
   Cr = 0.4380R - 0.4028G - 0.0352B + 512

3. YUV to VYU
   Y = U;
   U = V;
   V = Y;

11.3.2 Scaler

Scaler is a synchronous parallel RGB frame converter for different resolution.

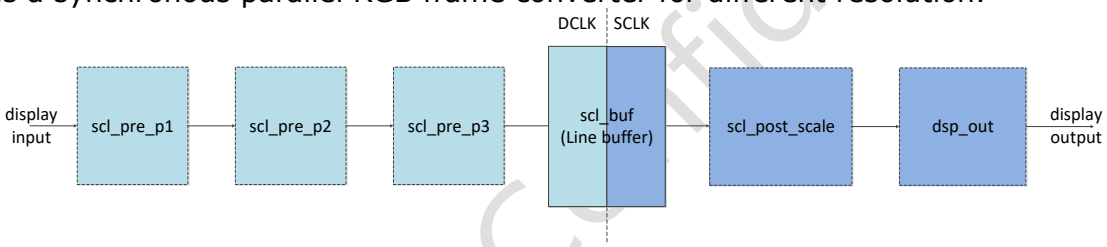

Fig. 11-2 Block diagram of SCALER

Detail description for application refer to application notes.

11.3.3 Split

Left-right mode:

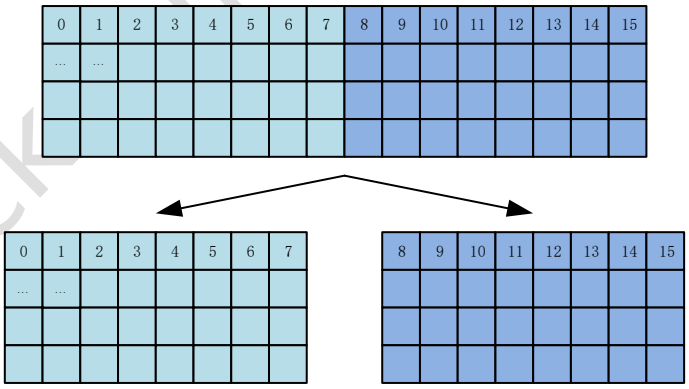

Fig. 11-3 Left-Right split mode

11.4 Register Description

11.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_SCALER_CON0	0x0010	W	0x00000000	Scaler control register
GRF_SCALER_CON1	0x0014	W	0x00000000	Scaler horizontal/vertical factor register

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Name	Offset	Size	Reset Value	Description
GRF_SCALER_CON2	0x0018	W	0x00000000	Scaler output scanning H/V start point setting register
GRF_SCALER_CON3	0x001c	W	0x00000000	Scaler output scanning horizontal setting register
GRF_SCALER_CON4	0x0020	W	0x00000000	Scaler output horizontal active window
GRF_SCALER_CON5	0x0024	W	0x00000000	Scaler output scanning vertical timing
GRF_SCALER_CON6	0x0028	W	0x00000000	Scaler output vertical active window
GRF_SCALER_CON7	0x002c	W	0x00000000	Scaler output horizontal border window
GRF_SCALER_CON8	0x0030	W	0x00000000	Scaler output vertical border window
GRF_POST_PROC_CON	0x0034	W	0x00000000	Post process control register
GRF_CSC_CTRL_CON	0x0038	W	0x00000000	CSC(color space convert) control register

Please refer to GRF Chapter. Register 0x0010~0x0038

11.5 Application Notes

11.5.1 Scaling Factor Setting

The frame scaling is done by horizontal (X) scaling and vertical (Y) scaling independently. The scaling factor is in *GRF_SCALER_CON1*. Software calculates the scaling factor value using the following equations:

scl_h_factor

(1)scaling up: (Hin_act-1)/(Hout_act-1)*2^16;
(2)scaling down(bilinear): (Hin_act-1)/(Hout_act-1)*2^14
    if(Hin_act-1)/(Hout_act-1)>2.0: (Hin_act-1)/(Hout_act-1)*2^14;
    else (Hin_act-2)/(Hout_act-1)*2^14
(3)scaling down(average): (Hout_act)/(Hin_act-1)*2^16;

scl_v_factor

(1)scaling up: (Vin_act-1)/(Vout_act-1)*2^16;
(2)scaling down(bilinear):
    if(Vin_act-1)/(Vout_act-1)>2.0: (Vin_act-1)/(Vout_act-1)*2^14;
    else (Vin_act-2)/(Vout_act-1)*2^14;
(3)scaling down(average): (Vout_act)/(Vin_act-1)*2^16;
    In where,
    Hin_act = (dsp_in_hact_end – dsp_in_hact_st);
    Vin_act = (dsp_in_vact_end – dsp_in_vact_st);

    Hout_act = (dsp_hact_end – dsp_hact_st);
    Vout_act = (dsp_vact_end – dsp_vact_st);

11.5.2 Display Output Timing

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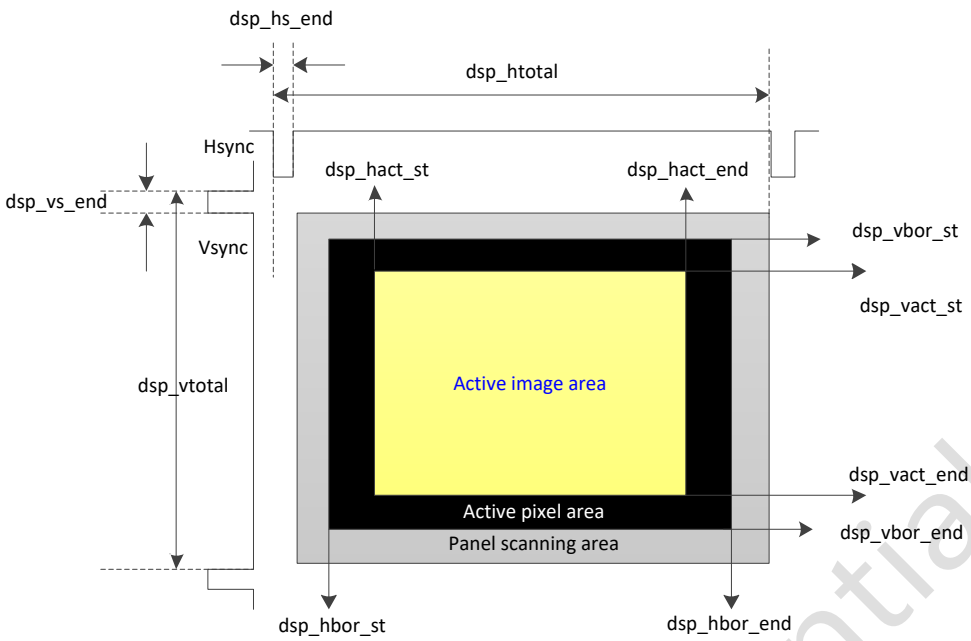

Fig. 11-4 SCALER Output Timing setting

11.5.3 Programming Sequence

Assert scaler_en after all scaler configuration registers are set.

For the frame synchronous of input/output display frames, there are some Programming requirements for SCALER.

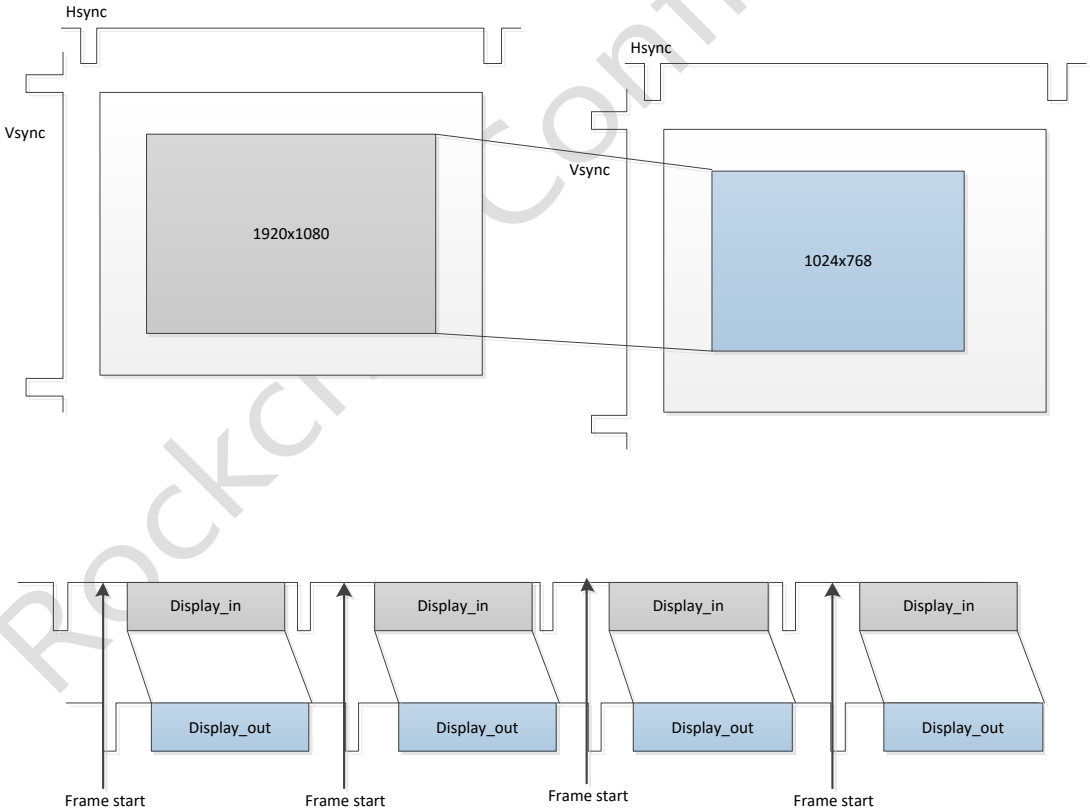

Fig. 11-5 SCALER Frame Sync

Output Pixel Clock Requirement (SCALER Clock Frequency Setting)

The output pixel clock is asynchronous with input pixel clock to support different display resolution. But the input/output frame frequency should be same (FSin=FSout) because there is no frame buffer in SCALER. So there is strict clock frequency requirement for output pixel clock, which is generated from system CRU.

Assume that Fout is the output pixel clock frequency and Fin is the input pixel clock frequency.

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dsp_in_vtotal*dsp_in_htotal*Fin = dsp_vtotal*dsp_in_htotal*Fout;

The total output active frame period (include horizontal blank period, but without vertical blank period) must be close to the total input active frame period. The difference between them should be less than Xmax input active line period(include horizontal blank period).

((dsp_vact_end-dsp_vact_st) *dsp_htotal* 1/Fout) >=
((dsp_in_vact_end-dsp_in_vact_st-Xmax) *(dsp_in_htotal)*1/Fin)
((dsp_vact_end-dsp_vact_st) *dsp_htotal* 1/Fout) <=
((dsp_in_vact_end-dsp_in_vact_st+Xmax)*(dsp_in_htotal)*1/Fin)

(1) vertical scaling up :

Xmin = 4; Xmax = 12;

(2)vertical scaling down(bilinear) :

when V_scale_ratio < 2 : Xmin = 2; Xmax = 14;
when V_scale_ratio >= 2: Xmin = 4; Xmax = 12;

(2) vertical scaling down(average):

Xmin = V_scale_ratio + 1; Xmax = 16 - Xmin;

(3) no vertical scaling:

Xmin = 2; Xmax = 14;

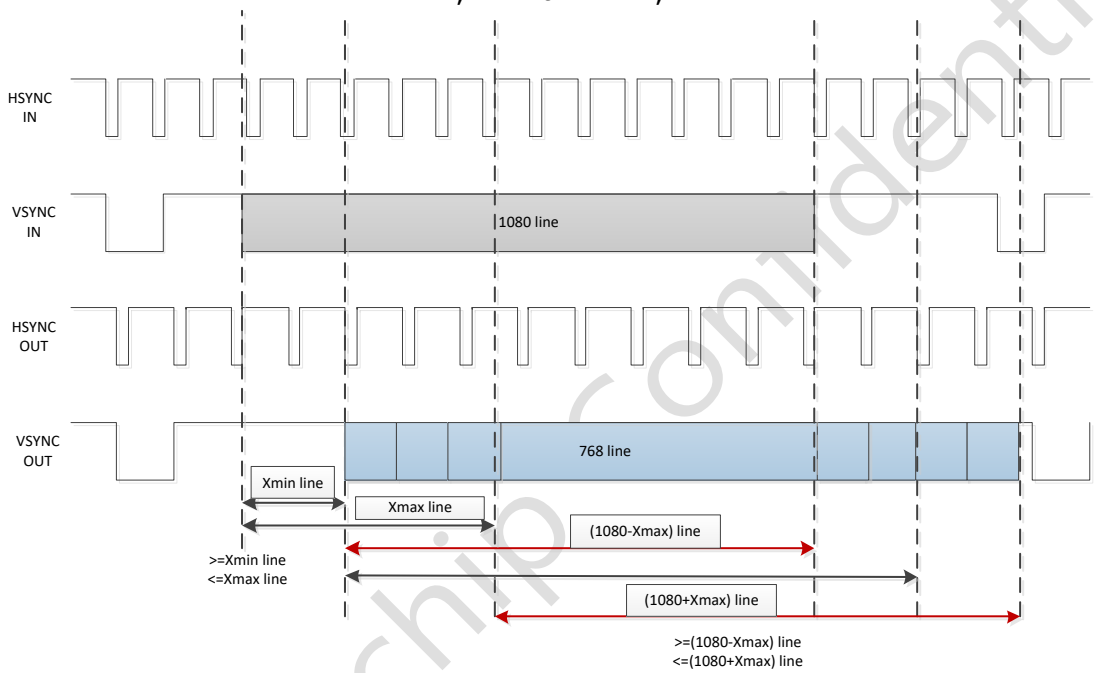

Fig. 11-6 SCALER Input/output Active frame period

Active pixel start point setting

First, the start point of output active image area should be Xmin lines later than the input active image area because of the scaling operation.

Second, because of the PLL precision, the total output active frame period would be not equal to the total input active frame period.

(1)So at a setting of the output pixel clock frequency, if the total output active frame period is larger than the total input active frame period. The start point of output active image area should be set after the beginning of Xmin input active pixel line.

Xmin*dsp_in_htotal*1/Fin <= Delta_T <= Xmax*dsp_in_htotal*1/Fin

Usually,we set Delta_T as follow:

Delta_T=7* dsp_in_htotal*1/Fin;
or
Delta_T=8* dsp_in_htotal*1/Fin;

(2)If the total output active frame period is less than the total input active frame period. The start point of output active image area should be set at the beginning of (Xmax+1) input

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active pixel line.

Delta_T = (Xmax* input_dsp_htotal)*1/Fin

Usually, we still set Delta_T as follow:

Delta_T=7* dsp_in_htotal*1/Fin; or Delta_T=8* dsp_in_htotal*1/Fin;

Output frame scanning start point setting

To meet the requirement of active pixel start point, there are dsp_frm_hst / dsp_frm_vst settings for frame scanning start point adjustment.

The timing delay of output active frame pixel start point behind input active frame pixel start point can be calculated as following equation.

T_frm_st = (T_BP_in + Delta_T + 3*dsp_htotal/Fout - T_BP_out);

In where,

T_frm_st = (dsp_frm_vst*dsp_in_htotal + dsp_frm_hst) / Fin;

T_BP_in is the blank period of input frame;

T_BP_out is the blank period of output frame and.

if(T_frm_st < 0), Delta_T should be adjusted as below:

T_frm_st = Tin –T_frm_st=dsp_in_vtotal * dsp_in_htotal/Fin - Delta_T;

then we can calc out dsp_frm_vst and dsp_frm_hst as below:

dsp_frm_vst = floor((T_frm_st*Fin)/dsp_in_htotal);

dsp_frm_hst = (T_frm_st – dsp_frm_vst*dsp_in_htotal/Fin)*Fin;

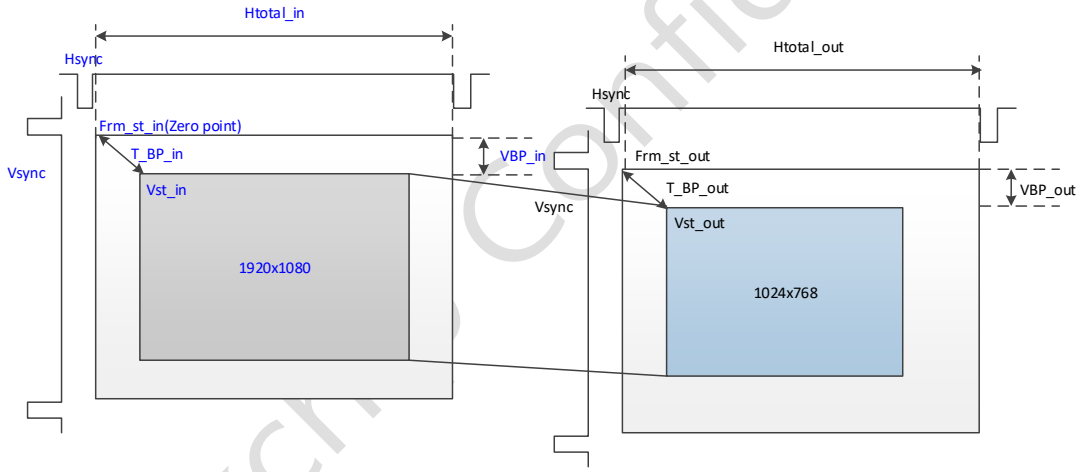

Fig. 11-7 SCALER frame scanning start point

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Chapter 12 General Video Interface（GVI）

12.1 Overview

GVI targets a high speed data transmission of video signals based on internal connection of the equipment, which will be used as an output of chip. With proprietary encoding scheme and CDR architecture, GVI enables transmission up to 40bit video data, up to 24 CTL data, HSYNC, VSYNC, and Data Enable by some differential pair cables with minimal external components.

GVI supports the following features:

- PHY Interface
  - Supports up to 3.75Gbps data rate(effective data rate 3Gbps)
  - Configure 1/2/4/8 lanes
  - Output lanes flexible mapping
  - Supports scrambling and Clock Data Recovery(CDR) to reduce EMI
  - Support ALN training
- RGB Parallel input Interface
  - Max Resolution : 4Kx2K@60Hz
  - Format : RGB666/RGB888/RGB101010/YCbCr422-8bit/YCbCr422-10bit
  - Byte mode : 3-byte/4-byte mode
  - Section mode : one/two section mode
- Apb2.0 slave interface for register read/write
- Interrupt

12.2 Block Diagram

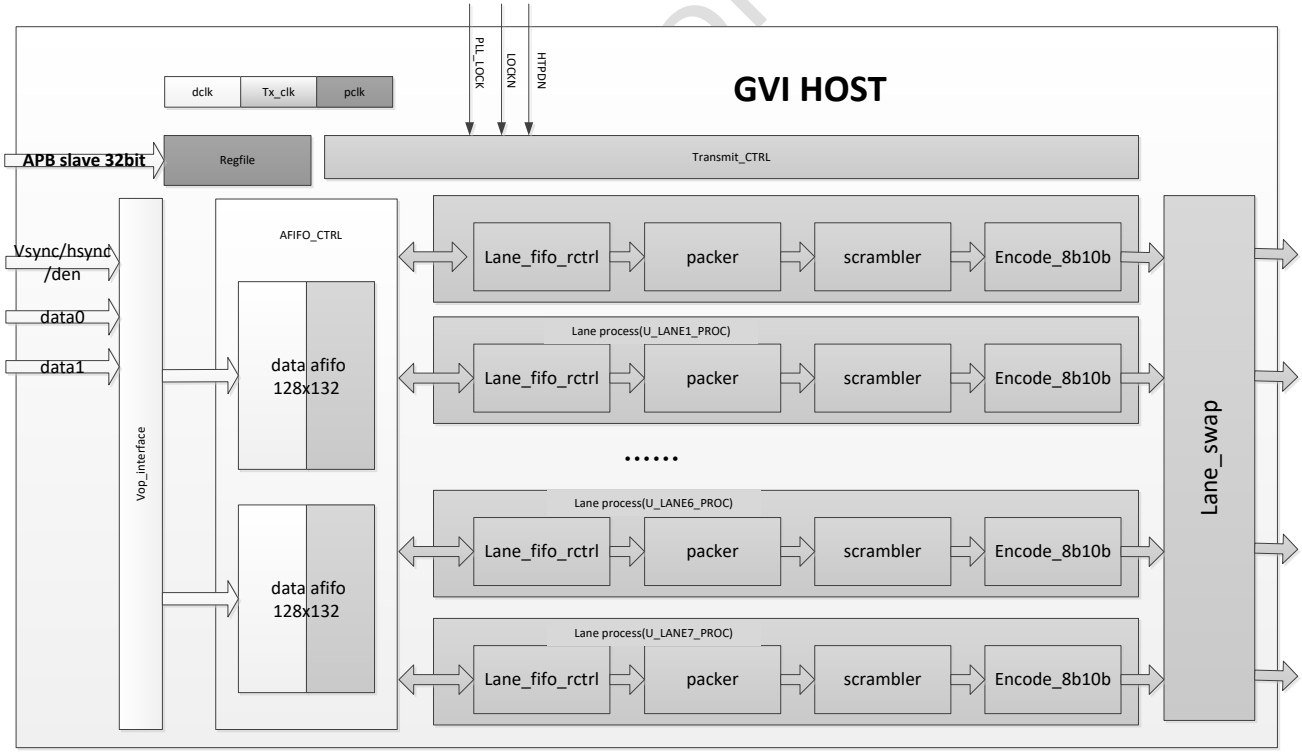

Fig. 12-1 GVI Block Diagram

As shown in above figure, the GVI HOST block have two function clock, one is dclk, another is tx_clk.

12.3 Function

12.3.1 Packer

Packer generate the packet that consists of every 8bits. The packet includes pixel data, control data and timing data. The data mapping of a packet is determined by the framing byte size.

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The order of Packer output is the the least significant byte is the first and most significant byte is the last.

12.3.2 Scrambler

The data scrambling is adopted for EMI reduction prior to ANSI 8B/10B encoding on the Transmitter. Each of Main Link data are scrambled and de-scrambled independently, with a 16bit LFSR as follows:

$$LFSR : G(X) = X16 + X5 + X4 + X3 + 1$$

LFSR shifts 8bits for 1byte character. The BE_SR character is used to reset the LFSR to 0xFFFF.

12.3.3 Encode

The encoder are ANSI standard 8b/10b compatible. On normal mode operation, each 10bit character represents 8bit of pixel data. Encoded characters provide DC balance and sufficient 0-1 and 1-0 transitions in GVI stream, which enable receiver to recover link clock with CDR technology.

12.3.4 Training

CDR training is performed for frequency acquisition of CDR PLL. CDR training conditions are as follows:

1) CDR training is performed when transmitter side HTPDN=low, and LOCKN = high
2) Transmitter transmit repetition of D10.2(0101010101) code until frequency lock of CDR PLL
3) Training pattern frequency is equal to half of the HS link bit rate
4) D10.2 code must not be scrambled
5) When Receiver loses CDR lock, it can indicate the status to Transmitter by LOCKN=high

ALN stands for alignment. ALN training is performed for both byte alignment and pixel alignment. For these purpose, ALN pattern includes BS and BE character. Byte boundary is detected with COMMMA pattern embedded in BS and BE characters. Symbol boundary is detected from K boundaries. ALN training conditions are as follows:

1) ALN training starts when HTPDN and LOCN at the Transmitter input are LOW
2) One DE cycle consist of 64 pixels. The first 32 pixels are high and last 32 pixels are LOW
3) DE cycle is repeat 16 times within ALN training
4) Data, Hsync, and CTL packet to "0" during ALN training after LOCKN is set to "0"
5) DE at the last one pixel is set to "1"
6) Vsync is set to "0" except the 4th last pixel
7) The 4th last pixel of Vsync should be set to "1" in order to replace the BE character with BE_SR
8) The ALN training pattern is scrambled by the scrambler

12.4 Register Description

12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

12.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GVI_SYS_CTRL0	0x0000	W	0x00000000	GVI system control0
GVI_SYS_CTRL1	0x0004	W	0x00000000	GVI system control1
GVI_SYS_CTRL2	0x0008	W	0x00000000	GVI system control2
GVI_SYS_CTRL3	0x000c	W	0x00000000	GVI system control3
GVI_VERSION	0x0010	W	0x00000000	GVI version
GVI_SYS_RST	0x0014	W	0x00000000	GVI system soft reset
GVI_LINE_FLAG	0x0018	W	0x00000000	GVI line flag
GVI_STATUS	0x001c	W	0x00000000	GVI status
GVI_PHY_CTRL0	0x0020	W	0x00000000	GVI PHY control0

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Name	Offset	Size	Reset Value	Description
GVI_PHY_CTRL1	0x0024	W	0x00000000	GVI PHY control1
GVI_PHY_CTRL2	0x0028	W	0x00000000	GVI PHY control2
GVI_PLL_LOCK_TIMEOUT	0x0030	W	0x00000000	GVI PLL lock time-out
GVI_HTPDN_TIMEOUT	0x0034	W	0x00000000	GVI htpdn time-out
GVI_LOCKN_TIMEOUT	0x0038	W	0x00000000	GVI lockn time-out
GVI_WAIT_LOCKN	0x003c	W	0x00000000	GVI lockn minimum effective time
GVI_WAIT_HTPDN	0x0040	W	0x00000000	GVI htpdn minimum effective time
GVI_INTR_EN	0x0050	W	0x00000000	GVI interrupt enable
GVI_INTR_CLR	0x0054	W	0x00000000	GVI interrupt clear
GVI_INTR_RAW_STATUS	0x0058	W	0x00000000	GVI raw interrupt
GVI_INTR_STATUS	0x005c	W	0x00000000	GVI interrupt
GVI_COLOR_BAR_CTRL	0x0060	W	0x00000000	colorbar control register
GVI_COLOR_BAR_TIMING_CTRL0	0x0070	W	0x00000000	color bar timing ctrl 0 ,hpw,hst
GVI_COLOR_BAR_TIMING_CTRL1	0x0074	W	0x00000000	color bar timing ctrl 1 ,hend,htotal
GVI_COLOR_BAR_TIMING_CTRL2	0x0078	W	0x00000000	color bar timing ctrl 2 ,vpw,vst
GVI_COLOR_BAR_TIMING_CTRL3	0x007c	W	0x00000000	color bar timing ctrl 3 ,vend,vtotal

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

12.4.3 Detail Register Description

GVI_SYS_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	force_lockn_value force lockn value
28	RW	0x0	force_lockn_en force lockn enable 1'b0: disable 1'b1: enable
27	RW	0x0	force_pll_value force pll value
26	RW	0x0	force_pll_en force pll enable 1'b0: disable 1'b1: enable
25	RW	0x0	force_htpdn_value force htpdn value

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Bit	Attr	Reset Value	Description
24	RW	0x0	force_htpdn_en force htpdn enable 1'b0: disable 1'b1: enable
23	RW	0x0	init_rd_value initial rd value
22	RW	0x0	init_rd_en initial rd value enable 1'b0: disable 1'b1: enable
21	RW	0x0	encode8b10b_en 8bto10b encoder enable 1'b0: disable 1'b1: enable
20	RW	0x0	scrambler_en scrambler enable 1'b0: disable 1'b1: enable
19	RW	0x0	aln_nor_mode data transmission mode after aln training
18	RW	0x0	nor_en data transmission enable 1'b0: disable 1'b1: enable
17	RW	0x0	aln_en aln training enable 1'b0: disable 1'b1: enable
16	RW	0x0	cdr_en cdr training enable 1'b0: disable 1'b1: enable
15	RW	0x0	enc8b10b_endian_swap 1'b0: jhgfiedcba 1'b1: abcdeifghj
14	RW	0x0	pack_endian_swap 1'b0: pack[7:0] 1'b1: pack[0:7]
13	RW	0x0	pack_byte_swap when 3-byte mode : 1'b0: byte2,byte1,byte0 1'b1: byte0,byte1,byte2 when 4-byte mode : 1'b0: byte3,byte2,byte1,byte0 1'b1: byte0,byte1,byte2,byte3

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Bit	Attr	Reset Value	Description
12	RW	0x0	cdr_endian_swap 1'b0: 10'b1010101010 1'b1: 10'b0101010101
11:10	RW	0x0	section_num 2'b00: one section 2'b01: two section 2'b1x: reserved
9:8	RW	0x0	byte_mode byte mode select 2'b00: 3byte mode 2'b01: 4byte mode 2'b1x: 5byte mode
7:4	RW	0x0	lane_num lane number 4'b0000: one lane 4'b0001: two lanes 4'b0011: four lanes 4'b0111: eight lanes other: reserved
3	RO	0x0	reserved
2	RW	0x0	frm_rst_en enable gvi rst when frame start 1'b0: disable 1'b1: enable
1	RW	0x0	auto_gating clk auto gating enable 1'b0: disable 1'b1: enable
0	RW	0x0	gvi_en gvi enable 1'b0: disable 1'b1: enable

GVI_SYS_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_wcnt_update update afifo wcnt and auto clear when new frame start
30:18	RO	0x0	reserved
17	RW	0x0	nor_protect normal mode protection 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
16	RW	0x0	whole_frm_en whole frame protection 1'b0: disable 1'b1: enable
15	RO	0x0	reserved
14	RW	0x0	yc_swap 1'b0: y,cb/cr 1'b1: cb/cr,y
13	RW	0x0	rb_swap 1'b0: RGB 1'b1: BGR
12	RW	0x0	dual_pixel_swap dual pixel swap 1'b0: disable 1'b1: enable
11:5	RO	0x0	reserved
4	RW	0x0	dual_pixel_en dual-pixel enable 1'b0: disable 1'b1: enable
3:0	RW	0x0	color_depth 4'b0000: 18bit RGB/YCbCr444 4'b0001: 24bit RGB/YCbCr444 4'b0010: 30bit RGB/YCbCr444 4'b1000: 16bit YCbCr422 4'b1001: 20bit YCbCr422

GVI_SYS_CTRL2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	afifo_almost_empty_thold async-fifo almost empty threshold value
23:16	RW	0x00	afifo_almost_full_thold async-fifo almost full threshold value
15:8	RO	0x0	reserved
7:0	RW	0x00	afifo_read_thold async-fifo threshold value

GVI_SYS_CTRL3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:28	RW	0x0	lane7_sel phy_data7 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7
27	RO	0x0	reserved
26:24	RW	0x0	lane6_sel phy_data6 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7
23	RO	0x0	reserved
22:20	RW	0x0	lane5_sel phy_data5 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7
19	RO	0x0	reserved
18:16	RW	0x0	lane4_sel phy_data4 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	lane3_sel phy_data3 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7
11	RO	0x0	reserved
10:8	RW	0x0	lane2_sel phy_data2 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7
7	RO	0x0	reserved
6:4	RW	0x0	lane1_sel phy_data1 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7
3	RO	0x0	reserved
2:0	RW	0x0	lane0_sel phy_data0 select 3'b000: lane0 3'b001: lane1 3'b010: lane2 3'b011: lane3 3'b100: lane4 3'b101: lane5 3'b110: lane6 3'b111: lane7

GVI_VERSION

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Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	version V_BY_ONE host version

GVI_SYS_RST

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	soft_rst soft reset 1'b0: disable 1'b1: enable

GVI_LINE_FLAG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	lane_flag1 lane flag1
15:0	RW	0x0000	lane_flag0 lane flag0

GVI_STATUS

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	afifo1_wcnt write count of afifo1
23:16	RW	0x00	afifo0_wcnt write count of afifo0
15:7	RO	0x0	reserved
6	RW	0x0	pll_lockn dphy pll lock status
5	RW	0x0	lock IO lock status
4	RW	0x0	htdpn IO htpdn status
3:0	RO	0x0	reserved

GVI_PHY_CTRL0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:12	RW	0x00	tx_idle Force the high speed defferential signal to common mode,for initialization of the serdes or special signaling 1'b0: normal operation 1'b1: force TXPn/TXMn to common mode
11:4	RW	0x00	pd_tx power down control signal of channel N(N=0~7) 1'b0: normal operation 1'b1: power down channel
3:1	RO	0x0	reserved
0	RW	0x0	pd_pll shared PLL block power down signal 1'b0: normal operation 1'b1: power down shared PLL,all the channels are not working

GVI_PHY_CTRL1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:24	RW	0x0	rtderm TX termination resistance adjustmemt, 001(default)
23:20	RW	0x0	tx_ampn The adjustment for the amplitude level of the driver(N=0~7)
19:16	RW	0x0	tx_empn The adjustment for the emphasis level of the driver(N=0~7)
15:0	RW	0x0000	pll_div The initial divider control for PLL

GVI_PHY_CTRL2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	phy_ctrl reserved

GVI_PLL_LOCK_TIMEOUT

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pll_lock_time_out pll lock time-out value

GVI_HTPDN_TIMEOUT

Address: Operational Base + offset (0x0034)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	htpdn_time_out htpdn time-out value

GVI_LOCKN_TIMEOUT

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lockn_time_out lockn time-out value

GVI_WAIT_LOCKN

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31	RW	0x0	wait_lockn_time_en lockn minimum effective time enable
30:0	RW	0x00000000	wait_lockn_time lockn minimum effective time

GVI_WAIT_HTPDN

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RW	0x0	wait_htpdn_en htpdn minimum effective time enable
30:0	RW	0x00000000	wait_htpdn_time htpdn minimum effective time

GVI_INTR_EN

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	intr_lockn_err_en lockn pull up when gvi is working
13	RW	0x0	intr_htpdn_err_en htpdn pull up when gvi is working
12	RW	0x0	intr_pll_err_en pll lock pull down when gvi is working
11	RW	0x0	intr_afifo_underflow_en afifo underflow interrupt enable
10	RW	0x0	intr_afifo_overflow_en afifo overflow interrupt enable
9	RW	0x0	intr_line_flag1_en line flag1 interrupt enable
8	RW	0x0	intr_line_flag0_en line flag0 interrupt enable

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Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6	RW	0x0	intr_lockn_timeout_en lockn time-out interrupt enable
5	RW	0x0	intr_htpdn_timeout_en htpdn time-out interrupt enable
4	RW	0x0	intr_pll_timeout_en pll time-out interrupt enable
3	RW	0x0	intr_lockn_en lockn interrupt enable
2	RW	0x0	intr_htpdn_en htpdn interrupt enable
1	RW	0x0	intr_pll_lock_en phy pll lock interrupt enable
0	RW	0x0	intr_frm_st_en frame start interrupt enable

GVI_INTR_CLR

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	intr_lockn_err_clr lockn pull up when gvi is working
13	RW	0x0	intr_htpdn_err_clr htpdn pull up when gvi is working
12	RW	0x0	intr_pll_err_clr pll lock pull down when gvi is working
11	RW	0x0	intr_afifo_underflow_clr afifo underflow interrupt clear
10	RW	0x0	intr_afifo_overflow_clr afifo overflow interrupt clear
9	RW	0x0	intr_line_flag1_clr line flag1 interrupt clear
8	RW	0x0	intr_line_flag0_clr line flag0 interrupt clear
7	RO	0x0	reserved
6	RW	0x0	intr_lockn_timeout_clr lockn time-out interrupt clear
5	RW	0x0	intr_htpdn_timeout_clr htpdn time-out interrupt clear
4	RW	0x0	intr_pll_timeout_clr pll time-out interrupt clear
3	RW	0x0	intr_lockn_clr lockn interrupt clear

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Bit	Attr	Reset Value	Description
2	RW	0x0	intr_htpdn_clr htpdn interrupt clear
1	RW	0x0	intr_pll_lock_clr phy pll lock interrupt clear
0	RW	0x0	intr_frm_st_clr frame start interrupt clear

GVI_INTR_RAW_STATUS

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	raw_intr_lockn_err lockn pull up when gvi is working
13	RW	0x0	raw_intr_htpdn_err htpdn pull up when gvi is working
12	RW	0x0	raw_intr_pll_err pll lock pull down when gvi is working
11	RW	0x0	raw_intr_afifo_underflow afifo underflow interrupt
10	RW	0x0	raw_intr_afifo_overflow afifo overflow interrupt
9	RW	0x0	raw_intr_line_flag1 line flag1 interrupt
8	RW	0x0	raw_intr_line_flag0 line flag0 interrupt
7	RO	0x0	reserved
6	RW	0x0	raw_intr_lockn_timeout lockn time-out interrupt
5	RW	0x0	raw_intr_htpdn_timeout htpdn time-out interrupt
4	RW	0x0	raw_intr_pll_timeout pll time-out interrupt
3	RW	0x0	raw_intr_lockn lockn interrupt
2	RW	0x0	raw_intr_htpdn htpdn interrupt
1	RW	0x0	raw_intr_pll_lock phy pll lock interrupt
0	RW	0x0	raw_intr_frm_st frame start interrupt

GVI_INTR_STATUS

Address: Operational Base + offset (0x005c)

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Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	intr_lockn_err lockn pull up when gvi is working
13	RW	0x0	intr_htpdn_err htpdn pull up when gvi is working
12	RW	0x0	intr_pll_err pll lock pull down when gvi is working
11	RW	0x0	intr_afifo_underflow afifo underflow interrupt
10	RW	0x0	intr_afifo_overflow afifo overflow interrupt
9	RW	0x0	intr_line_flag1 line flag1 interrupt
8	RW	0x0	intr_line_flag0 line flag0 interrupt
7	RO	0x0	reserved
6	RW	0x0	intr_lockn_timeout lockn time-out interrupt
5	RW	0x0	intr_htpdn_timeout htpdn time-out interrupt
4	RW	0x0	intr_pll_timeout pll time-out interrupt
3	RW	0x0	intr_lockn lockn interrupt
2	RW	0x0	intr_htpdn htpdn interrupt
1	RW	0x0	intr_pll_lock phy pll lock interrupt
0	RW	0x0	intr_frm_st frame start interrupt

GVI_COLOR_BAR_CTRL
Address: Operational Base + offset (0x0060)
colorbar control register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	color_bar_clk_sel color bar clk select 1'b0: dclk 1'b1: tx phy clk
0	RW	0x0	color_bar_en 1'b0: enable color bar 1'b1: normal mode

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GVI_COLOR_BAR_TIMING_CTRL0
Address: Operational Base + offset (0x0070)
color bar timing ctrl 0 ,hpw,hst

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	hst horizontal start point
15:13	RO	0x0	reserved
12:0	RW	0x0000	hpw horizontal pulse width

GVI_COLOR_BAR_TIMING_CTRL1
Address: Operational Base + offset (0x0074)
color bar timing ctrl 1 ,hend,htotal

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	htotal horizontal total width
15:13	RO	0x0	reserved
12:0	RW	0x0000	hend horizontal end point

GVI_COLOR_BAR_TIMING_CTRL2
Address: Operational Base + offset (0x0078)
color bar timing ctrl 2 ,vpw,vst

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	vst vertical start point
15:13	RO	0x0	reserved
12:0	RW	0x0000	vpw Vertical pulse width

GVI_COLOR_BAR_TIMING_CTRL3
Address: Operational Base + offset (0x007c)
color bar timing ctrl 3 ,vend,vtotal

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	vtotal vertical total width
15:13	RO	0x0	reserved
12:0	RW	0x0000	vend vertical end point

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12.5 Interface Timing

12.5.1 RGB interface timing

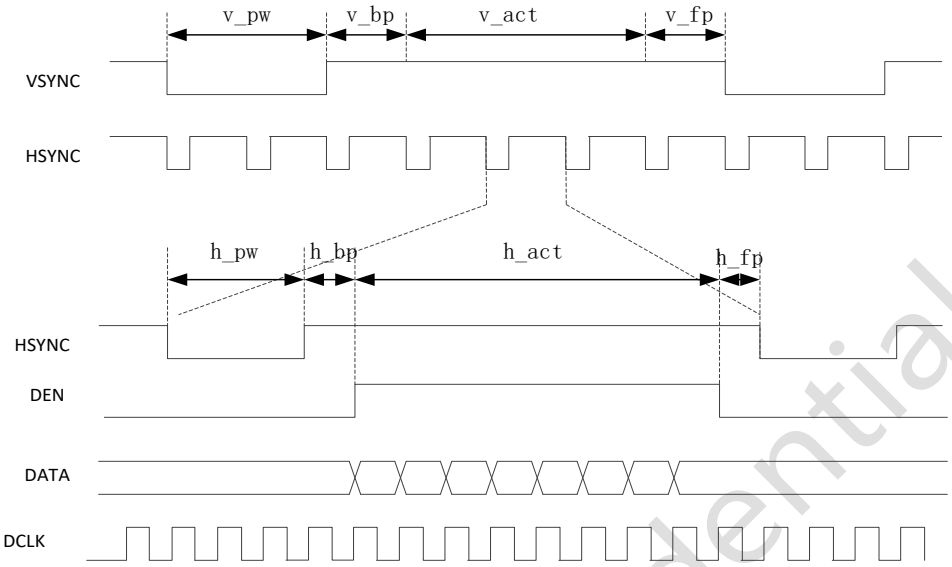

Fig. 12-2 RGB Interface timing

12.5.2 APB interface timing

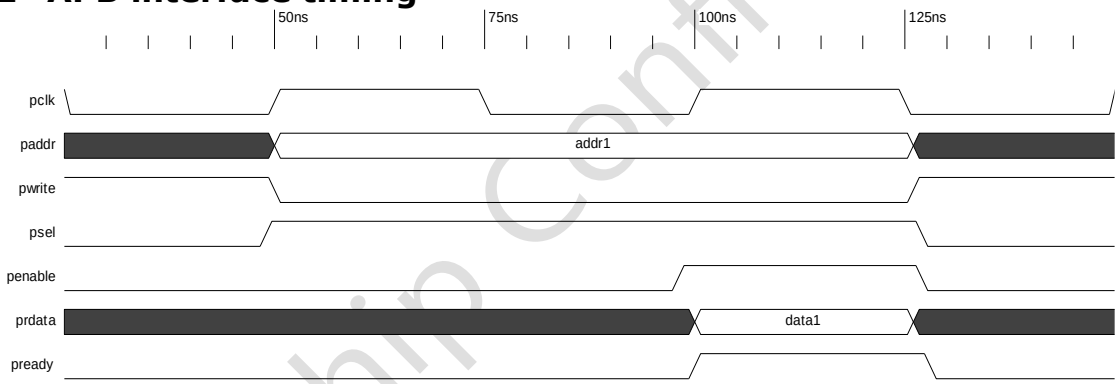

Fig. 12-3 APB Interface Typical Read Timing

12.6 Application Notes

12.6.1 The relationship of section mode and lane number

Table 12-1 Section mode and lane number

Items		Lane number			
		1 lane	2 lanes	4 lanes	8lanes
Section mode	One-section	YES	YES	YES	YES
	Two-section	NO	YES	YES	YES

12.6.2 The relationship of dclk and tx_clk

The relationship of dclk and tx_clk is shown as follows:

$$tx_clk = dclk * byte_mode * section_num / lane_num$$

12.6.3 Recommended lane number

Recommended lane number is shown is following:

Table 12-2 Recommended lane number

Resolution	Refresh rate(Dclk)	Color depth	No of data lane
HD Ex.1280x720p	60Hz(74.25Mhz)	18/24/30 bit	1
	120Hz(148.5Mhz)	18/24/30 bit	2
	240Hz(297Mhz)	18/24/30 bit	4

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Full HD Ex.1920x180p	60Hz(148.5Mhz)	18/24/30 bit	2
	120Hz(297Mhz)	18/24/30 bit	4
	240Hz(594Mhz)	18/24/30 bit	8
Cinema Full HD Ex.2560x1080p	60Hz(185Mhz)	18/24/30 bit	2
	120Hz(370Mhz)	18/24/30 bit	4
4Kx2K Ex.3840x2160p	60Hz(594Mhz)	18/24/30 bit	8

12.6.4 Common configuration

Step1:Set comb PHY PLL , wait PLL lock
Step2:Set lane number
Step3:Select color depth
Step4:Enable GVI
Step5:Other configuration uses default value

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Chapter 13 MIPI DSI HOST Controller

13.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI HOST Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI HOST Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI DSI HOST Controller supports one to four lanes for data transmission with MIPI D-PHY.
The MIPI DSI HOST Controller supports the following features:

- Compliant with MIPI Alliance standards
- Support the DPI interface color coding mappings into 24-bit Interface
  - 16 bits per pixel, configurations 1,2,and 3
  - 18 bits per pixel, configurations 1 and 2
  - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels:
  - Up to 2047 vertical active lines
  - Up to 63 vertical back porch lines
  - Up to 63 vertical front porch lines
  - Maximum resolution is limited by available DSI Physical link bandwidth which depends on the number of lanes and maximum speed per lane
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTp)
- Ultra Low-Power mode
- Fault recovery schemes

13.2 Block Diagram

The following diagram shows the MIPI DSI HOST Controller architecture.

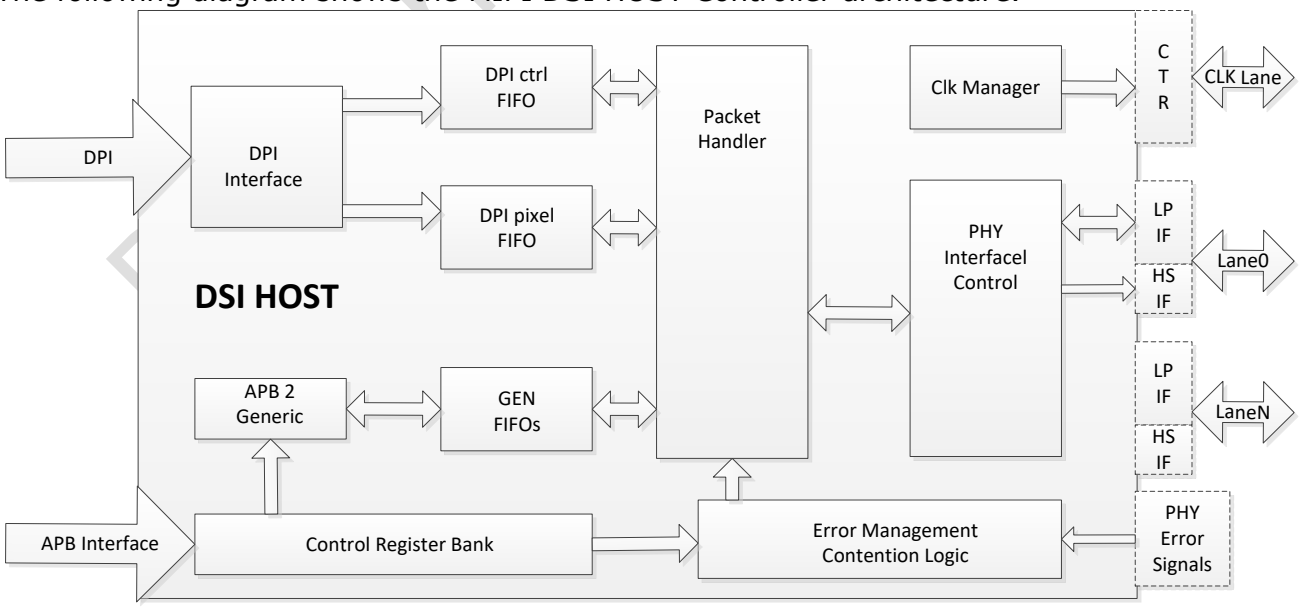

Fig. 13-1 MIPI DSI HOST Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video packets, hen in Video mode.

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The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI DSI HOST Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.
The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.
The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.
The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFOS: Command FIFO, Write payload FIFO, Read payload FIFO.
The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

13.3 Function Description

13.3.1 DPI interface function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by writing to the register of CFG_MISC_CON[2:1]. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.
The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 13-1 Color table

Signal Line	16-bit			18-bit		24bit
Config	**Config1**	**Config2**	**Config3**	**Config1**	**Config2**	**Config1**
Dpidata23	Not used	Not used	Not used	Not used	Not used	R7
Dpidata22	Not used	Not used	Not used	Not used	Not used	R6
Dpidata21	Not used	Not used	R4	Not used	R5	R5
Dpidata20	Not used	R4	R3	Not used	R4	R4
Dpidata19	Not used	R3	R2	Not used	R3	R3
Dpidata18	Not used	R2	R1	Not used	R2	R2
Dpidata17	Not used	R1	R0	R5	R1	R1
Dpidata16	Not used	R0	Not used	R4	R0	R0
Dpidata15	R4	Not used	Not used	R3	Not used	G7
Dpidata14	G3	Not used	Not used	G2	Not used	G6
Dpidata13	G2	G5	G5	G1	G5	G5
Dpidata12	G1	G4	G4	G0	G4	G4
Dpidata11	G0	G3	G3	G5	G3	G3
Dpidata10	G5	G2	G2	G4	G2	G2
Dpidata9	G4	G1	G1	G3	G1	G1
Dpidata8	G3	G0	G0	G2	G0	G0
Dpidata7	G2	Not used	Not used	G1	Not used	B7

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Signal Line	16-bit			18-bit		24bit
Config	Config1	Config2	Config3	Config1	Config2	Config1
Dpidata6	G1	Not used	Not used	G0	Not used	B6
Dpidata5	G0	Not used	B4	B5	B5	B5
Dpidata4	B4	B4	B3	B4	B4	B4
Dpidata3	B3	B3	B2	B3	B3	B3
Dpidata2	B2	B2	B1	B2	B2	B2
Dpidata1	B1	B1	B0	B1	B1	B1
Dpidata0	B0	B0	Not used	B0	B0	B0

The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows:Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI DSI HOST Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.

If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

13.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI DSI HOST Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register.

The valid packets available to be transmitted through the Generic interface are as follows:

- Generic Write Short Packet 0 Parameters
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Generic Write Short Packet 0 Parameter
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Maximum Read Packet Configuration
- Generic Long Write Packet
- DCS Write Short Packet 0 Parameter
- DCS Write Short Packet 1 Parameter
- DCS Write Short Packet 0 Parameter
- DCS Write Long Packet

A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.

Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.

The transfer of packets through the APB bus is based on the following conditions:

The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.

The data input bus has a maximum width of 32 bits. This allows for a relation to be defined

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between the input APB clock frequency and maximum bi rate achievable by the APB interface.
The DSI link bit rate when using solely APB is equal to (APB clock frequency) *16 Mbps. The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.
To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI DSI HOST Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.
The memory write commands require maximum throughout from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least significant byte position of the APB data bus.
After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figures show how the pixel data should be organized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams.In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

4.1.1 Transmission of Commands in Video Mode

The MIPI DSI HOST Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

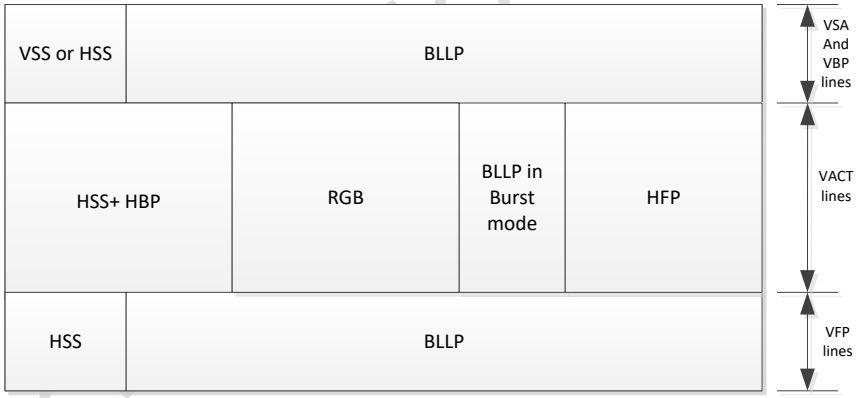

Fig. 13-2 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Bertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.
The MIPI DSI HOST Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being (1/2 cycle) * (number of lines -1) shorter than tL.
The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the

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lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the ouvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DSI HOST does not transmit these commands on the last line.
If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DSI HOST after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpihalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).
If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch(VFP) regions.
The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP
Outvact_lpcmd_time=(tL-(Time to transmit HSS and HSE frames +tHSA+Time to enter and leave LP mode+Time to send the D-PHY LPDT command)) / escape clock period / 8 / 2
Where, tL=Line time, and tHSA=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses).
In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles. The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field. This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.
Consider an example with 12.6 μs per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:

- Sync pulses are not being transmitted
- Two lane byte clock ticks are required to transmit a short packet

$$phy_lp2hs_time = 16$$

$$phy_lp2p_time = 20$$

In this example, a 11-byte command can be transmitted as follows:

$$outvact_lpcmd_time = 11bytes$$

The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmite a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:
Invact_lpcmd_time=((tHFP-Time to enter and leave low-power mode + Blanking period before the HFP when in Burst mode- Time to send the D-PHY LPDT command) / escape clock period) / 8. Where,

$$tHFP = line_time - tHSA - tHBP - tHACT$$

tHACT=vid_pkt_size*bits_per_pixel*lane_byte_clock_period / num_lanes
The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.
Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is 12.6μs. With a lane byte clock of 100 MHz, 1260 clock ticks are available to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks (4.6μs) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3μs is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.
A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this exampled, commands are not sent in the VACT region. If Burst mode is enabled,

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more time is available to transmit commands in the VACT region. The following are assumed:
The controller is not in Burst mode:

$$phy_lp2hs_time = 16$$

In this example invact_lpcmd_time is calculated as follows:
Invact_lpcmd_time = (2.3μs –(16*10 ns)-(20*10 ns)-(8*66 ns)) /66 ns / 8 = 2 bytes
The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparison to determine if a command can be transmitted in any of the BLLP periods.
Following figure illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

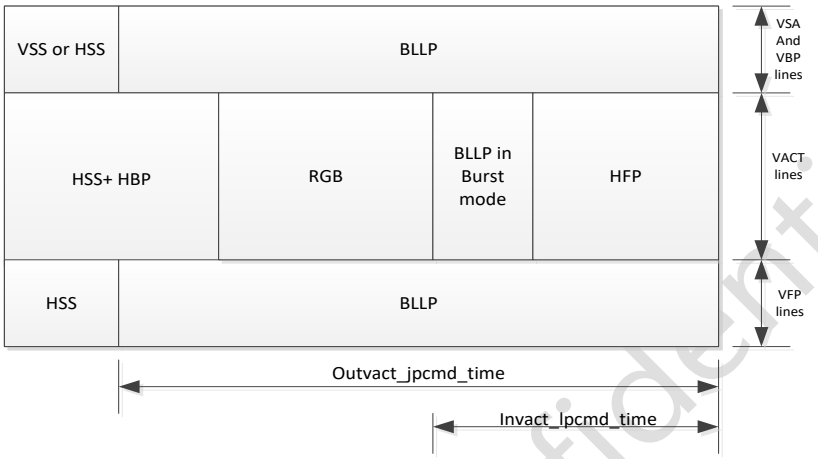

Fig. 13-3 Location in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DSI HOST automatically determines the area where each command can be sent and no programming or calculation is required.
On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.
The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) =Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.
The time to return the read data packet from the peripheral depends on the number of bytes read and the escape clock frequency of the peripheral; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.
In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time + Time to return the read data packet from the peripheral device + phy_hs2hs_time
In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:
max_rd_time= phy_hs2lp_time +LPDT command time + Read command time in LP mode + Time to return the data read from the peripheral device + phy_lp2hs_time
Where,
LPDT command time = (8*Host escape clock period) / Lane byte clock period
Read command time in LP mode = (32 * host escape clock period) / lane byte clock period
It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time* Lane byte clock period is less than outvact_lpcmd_time *8*Escape clock period of the host.
Otherwise, the read commands are serviced on the last line of a frame and the edpihalt signal may be asserted. If it is necessary to read a large number of parameters (>16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

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13.4 Register Description

13.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

13.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VERSION	0x0000	W	0x3133302a	Version
MIPI_DSI_HOST_PWR_UP	0x0004	W	0x00000000	Power up
MIPI_DSI_HOST_CLKMGR_CFG	0x0008	W	0x00000000	Configure the factor of the internal dividers to divide lanebyteclk
MIPI_DSI_HOST_DPI_VCID	0x000c	W	0x00000000	DPI virtual channel id
MIPI_DSI_HOST_DPI_COLOR_CODING	0x0010	W	0x00000000	DPI color coding
MIPI_DSI_HOST_DPI_CFG_POL	0x0014	W	0x00000000	Polarity of the DPI signals
MIPI_DSI_HOST_DPI_LP_CMD_TIM	0x0018	W	0x00000000	The timing for the low-power command while in video mode
MIPI_DSI_HOST_PCKHDL_CFG	0x002c	W	0x00000000	Configures how EoTp,BTA,CRC and ECC are to be used , to meet the peripheral's characteristics
MIPI_DSI_HOST_GEN_VCID	0x0030	W	0x00000000	The virtual channel id of the read responses to store and return to the Generic interface
MIPI_DSI_HOST_MODE_CFG	0x0034	W	0x00000001	This register configures the mode of operation - Video mode or Command mode(Commands can be sent even in video mode too)
MIPI_DSI_HOST_VID_MODE_CFG	0x0038	W	0x00000000	Configure several aspects of the Video mode operation
MIPI_DSI_HOST_VID_PKT_SIZE	0x003c	W	0x00000000	The video packet size
MIPI_DSI_HOST_VID_NUM_CHUNKS	0x0040	W	0x00000000	The number of chunks to use
MIPI_DSI_HOST_VID_NULL_SIZE	0x0044	W	0x00000000	The size of null packets
MIPI_DSI_HOST_VID_HSA_TIME	0x0048	W	0x00000000	HSA time
MIPI_DSI_HOST_VID_HBP_TIME	0x004c	W	0x00000000	HBP time

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VID_HLINE_TIME	0x0050	W	0x00000000	The overall time for video line
MIPI_DSI_HOST_VID_VSA_LINES	0x0054	W	0x00000000	VSA period
MIPI_DSI_HOST_VID_VBP_LINES	0x0058	W	0x00000000	VBP period
MIPI_DSI_HOST_VID_VFP_LINES	0x005c	W	0x00000000	VFP period
MIPI_DSI_HOST_VID_VACTIVE_LINES	0x0060	W	0x00000000	The vertical resolution of the video
MIPI_DSI_HOST_EDPI_CMD_SIZE	0x0064	W	0x00000000	The size of eDPI packet
MIPI_DSI_HOST_CMD_MODE_CFG	0x0068	W	0x00000000	Configure several aspects of the command mode operation
MIPI_DSI_HOST_GEN_HDR	0x006c	W	0x00000000	Set the header for new packets sent using the Generic interface
MIPI_DSI_HOST_GEN_PLD_DATA	0x0070	W	0x00000000	The payload for the packet sent using the Generic interface
MIPI_DSI_HOST_CMD_PKT_STATUS	0x0074	W	0x00000000	The status of FIFOs related to the Generic interface
MIPI_DSI_HOST_TO_CNT_CFG	0x0078	W	0x00000000	The counters that trigger the timeout error
MIPI_DSI_HOST_HS_RD_TO_CNT	0x007c	W	0x00000000	The Peripheral Response timeout after high-speed read operation
MIPI_DSI_HOST_LP_RD_TO_CNT	0x0080	W	0x00000000	The Peripheral Response timeout after low-power read operation
MIPI_DSI_HOST_HS_WR_TO_CNT	0x0084	W	0x00000000	The Peripheral Response timeout after high-speed write operation
MIPI_DSI_HOST_LP_WR_TO_CNT	0x0088	W	0x00000000	The Peripheral Response timeout after low-power write operation
MIPI_DSI_HOST_BTA_TO_CNT	0x008c	W	0x00000000	The Peripheral Response timeout after the Bus Turnaround completion
MIPI_DSI_HOST_SDF_3D	0x0090	W	0x00000000	The 3D control information for VSS Packets in video mode
MIPI_DSI_HOST_LPCLK_CTRL	0x0094	W	0x00000000	Using non-continuous clock in the clock lane
MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG	0x0098	W	0x00000000	Set the time that the HOST assumes in calculations for the clock lane to switch between high-speed and low-power

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_PHY_TMR_CFG	0x009c	W	0x00000000	Set the time that the HOST assumes in calculations for the data lanes to switch between high-speed and low-power
MIPI_DSI_HOST_PHY_RSTZ	0x00a0	W	0x00000000	The reset of the PLL and DPHY
MIPI_DSI_HOST_PHY_IF_CFG	0x00a4	W	0x00000003	The minimum time to remain in Stop state
MIPI_DSI_HOST_PHY_STATUS	0x00b0	W	0x00000000	The DPHY status
MIPI_DSI_HOST_INT_ST0	0x00bc	W	0x00000000	The status of the interrupt sources
MIPI_DSI_HOST_INT_ST1	0x00c0	W	0x00000000	The status of the interrupt sources
MIPI_DSI_HOST_INT_MSK0	0x00c4	W	0x00000000	The masks of interrupt sources
MIPI_DSI_HOST_INT_MSK1	0x00c8	W	0x00000000	The masks of interrupt sources
MIPI_DSI_HOST_INT_FORCE0	0x00d8	W	0x00000000	Force interrupts
MIPI_DSI_HOST_INT_FORCE1	0x00dc	W	0x00000000	Force interrupts
MIPI_DSI_HOST_VID_SHADOW_CTRL	0x0100	W	0x00000000	Control the DPI shadow register
MIPI_DSI_HOST_DPI_VCID_ACT	0x010c	W	0x00000000	The virtual channel id for the DPI traffic
MIPI_DSI_HOST_DPI_COLOR_CODING_ACT	0x0110	W	0x00000000	DPI color coding
MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT	0x0118	W	0x00000000	The timing for low-power commands sent while in Video mode
MIPI_DSI_HOST_VID_MODE_CFG_ACT	0x0138	W	0x00000000	Configure several aspects of Video mode operation
MIPI_DSI_HOST_VID_PKT_SIZE_ACT	0x013c	W	0x00000000	Configure the video packet size
MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT	0x0140	W	0x00000000	Configure the number of chunks to use
MIPI_DSI_HOST_VID_NULL_SIZE_ACT	0x0144	W	0x00000000	The size of null packets
MIPI_DSI_HOST_VID_HSA_TIME_ACT	0x0148	W	0x00000000	HSA time
MIPI_DSI_HOST_VID_HBP_TIME_ACT	0x014c	W	0x00000000	HBP time

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VID_HLINE_TIME_ACT	0x0150	W	0x00000000	The overall time for each video line
MIPI_DSI_HOST_VID_VSA_LINES_ACT	0x0154	W	0x00000000	VSA period
MIPI_DSI_HOST_VID_VBP_LINES_ACT	0x0158	W	0x00000000	VBP period
MIPI_DSI_HOST_VID_VFP_LINES_ACT	0x015c	W	0x00000000	VFP period
MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT	0x0160	W	0x00000000	The vertical resolution of video
MIPI_DSI_HOST_SDF_3D_ACT	0x0190	W	0x00000000	Store 3D control information for VSS in video mode

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

13.4.3 Detail Register Description

MIPI_DSI_HOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x3133302a	version

MIPI_DSI_HOST_PWR_UP

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	shutdownz This bit configures the core either to power up or to reset. Its default value is 0. After the core configuration, to enable the DWC_mipi_dsi_host, set this register to 1. 1'b0: Reset 1'b1: Power-up

MIPI_DSI_HOST_CLKMGR_CFG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:8	RW	0x00	to_clk_division This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	tx_esc_clk_division This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation

MIPI_DSI_HOST_DPI_VCID

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	Reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	Reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4’b0000: 16-bit configuration 1 4’b0001: 16-bit configuration 2 4’b0010: 16-bit configuration 3 4’b0011: 18-bit configuration 1 4’b0100: 18-bit configuration 2 4’b0101: 24-bit 4’b0110: 20-bit YCbCr 4:2:2 loosely packed 4’b0111: 24-bit YCbCr 4:2:2 4’b1000: 16-bit YCbCr 4:2:2 4’b1001: 30-bit 4’b1010: 36-bit 4’b1011-4’b1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_CFG_POL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	colorm_active_low When set to 1, this bit configures the color mode pin (dpicolorm) as active low
3	RW	0x0	shutd_active_low When set to 1, this bit configures the shutdown pin (dpishutdn) as active low
2	RW	0x0	hsync_active_low When set to 1, this bit configures the horizontal synchronism pin (dpihsync) as active low
1	RW	0x0	vsync_active_low When set to 1, this bit configures the vertical synchronism pin (dpivsync) as active low
0	RW	0x0	dataen_active_low When set to 1, this bit configures the data enable pin (dpidataen) as active low

MIPI_DSI_HOST_DPI_LP_CMD_TIM

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RW	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	Reserved
7:0	RW	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_PCKHDL_CFG

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	Reserved
4	RW	0x0	crc_rx_en When set to 1, this bit enables the CRC reception and error reporting
3	RW	0x0	ecc_rx_en When set to 1, this bit enables the ECC reception, error correction, and reporting

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Bit	Attr	Reset Value	Description
2	RW	0x0	bta_en When set to 1, this bit enables the Bus Turn-Around (BTA) request
1	RW	0x0	eotp_rx_en When set to 1, this bit enables the EoTp reception
0	RW	0x0	eotp_tx_en When set to 1, this bit enables the EoTp transmission

MIPI_DSI_HOST_GEN_VCID

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	gen_vcid_rx This field indicates the Generic interface read-back virtual channel identification

MIPI_DSI_HOST_MODE_CFG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x1	cmd_video_mode This bit configures the operation mode: 1'b0: Video mode 1'b1: Command mode

MIPI_DSI_HOST_VID_MODE_CFG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 1'b0: Vertical mode 1'b1: Horizontal mode
23:21	RO	0x0	Reserved
20	RW	0x0	vpg_mode This field is to select the pattern: 1'b0: Color bar (horizontal or vertical) 1'b1: BER pattern (vertical only)
19:17	RO	0x0	Reserved
16	RW	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator

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Bit	Attr	Reset Value	Description
15	RW	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RW	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RW	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows
12	RW	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows
11	RW	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows
10	RW	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RW	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows
8	RW	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	Reserved
1:0	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RW	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS

Address: Operational Base + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

MIPI_DSI_HOST_VID_HSA_TIME

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14:0	RW	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES

Address: Operational Base + offset (0x0054)

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Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VBP_LINES

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VFP_LINES

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RW	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_EDPI_CMD_SIZE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	edpi_allowed_cmd_size This field configures the maximum allowed size for an eDPI write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled

MIPI_DSI_HOST_CMD_MODE_CFG

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 1'b0: High-speed 1'b1: Low-power
23:20	RO	0x0	Reserved
19	RW	0x0	dcs_lw_tx This bit configures the DCS long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
18	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
17	RW	0x0	dcs_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
16	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
15	RO	0x0	Reserved
14	RW	0x0	gen_lw_tx This bit configures the Generic long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
13	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power

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Bit	Attr	Reset Value	Description
12	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
11	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
10	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
9	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
8	RW	0x0	gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
7:2	RO	0x0	Reserved
1	RW	0x0	ack_rqst_en When set to 1, this bit enables the acknowledge request after each packet transmission
0	RW	0x0	tear_fx_en When set to 1, this bit enables the tearing effect acknowledge request

MIPI_DSI_HOST_GEN_HDR

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RW	0x00	gen_wc_msbyte

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	gen_wc_lsbyte This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets
7:6	RW	0x0	gen_vc This field configures the virtual channel id of the header packet
5:0	RW	0x00	gen_dt This field configures the packet data type of the header packet

MIPI_DSI_HOST_GEN_PLD_DATA

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 This field indicates byte 4 of the packet payload
23:16	RW	0x00	gen_pld_b3 This field indicates byte 3 of the packet payload
15:8	RW	0x00	gen_pld_b2 This field indicates byte 2 of the packet payload
7:0	RW	0x00	gen_pld_b1 This field indicates byte 1 of the packet payload

MIPI_DSI_HOST_CMD_PKT_STATUS

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14	RW	0x0	dbi_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
13	RO	0x0	dbi_pld_r_full This bit indicates the full status of the DBI read payload FIFO
12	RO	0x0	dbi_pld_r_empty This bit indicates the empty status of the DBI read payload FIFO
11	RO	0x0	dbi_pld_w_full This bit indicates the full status of the DBI write payload FIFO
10	RO	0x0	dbi_pld_w_empty This bit indicates the empty status of the DBI write payload FIFO
9	RO	0x0	dbi_cmd_full This bit indicates the full status of the DBI command FIFO
8	RO	0x0	dbi_cmd_empy This bit indicates the empty status of the DBI command FIFO
7	RO	0x0	Reserved
6	RO	0x0	gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO

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Bit	Attr	Reset Value	Description
5	RO	0x0	gen_pld_r_full This bit indicates the full status of the generic read payload FIFO
4	RO	0x0	gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO
3	RO	0x0	gen_pld_w_full This bit indicates the full status of the generic write payload FIFO
2	RO	0x0	gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO
1	RO	0x0	gen_cmd_full This bit indicates the full status of the generic command FIFO
0	RO	0x0	gen_cmd_empty This bit indicates the empty status of the generic command FIFO

MIPI_DSI_HOST_TO_CNT_CFG

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using the non-burst mode and there is no sufficient time to switch from HS to LP and back in the period which is from one line data finishing to the next line sync start, the DSI link returns the LP state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one FRAME data transmission * (1 + 10%) In burst mode, RGB pixel packets are time-compressed, leaving more time during a can line. Therefore, if in burst mode and there is sufficient time to switch from HS to LP and back in the period of time from one line data finishing to the next line sync start, the DSI link can return LP mode and back in this time interval to save power. For this, configure the TO_CLK_DIVISION and hstx_to_cnt to be in ccordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one LINE data transmission * (1 + 10%)
15:0	RW	0x0000	lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles)

MIPI_DSI_HOST_HS_RD_TO_CNT

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Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	hs_rd_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after sending a high-speed read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_RD_TO_CNT

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	lp_rd_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after sending a low-power read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_HS_WR_TO_CNT

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	presp_to_mode When set to 1, this bit ensures that the peripheral response timeout caused by hs_wr_to_cnt is used only once per eDPI frame, when both the following conditions are met: dpivsync_edpiwms has risen and fallen. Packets originated from eDPI have been transmitted and its FIFO is empty again. In this scenario no non-eDPI requests are sent to the D-PHY, even if there is traffic from generic or DBI ready to be sent, making it return to stop state. When it does so, PRESP_TO counter is ctivated and only when it finishes does the controller send any other traffic that is ready
23:16	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	hs_wr_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_WR_TO_CNT

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	lp_wr_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_BTA_TO_CNT

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	bta_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_SDF_3D

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet
15:6	RO	0x0	Reserved
5	RW	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent 1'b1: Right eye data is sent first, and then the left eye data is sent

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Bit	Attr	Reset Value	Description
4	RW	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RW	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved
1:0	RW	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

MIPI_DSI_HOST_LPCLK_CTRL

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1	RW	0x0	auto_clklane_ctrl This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows
0	RW	0x0	phy_txrequestclkhs This bit controls the D-PHY PPI txrequestclkhs signal

MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	Reserved
25:16	RW	0x000	phy_clkhs2lp_time This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles
15:10	RO	0x0	Reserved
9:0	RW	0x000	phy_clklp2hs_time This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles

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MIPI_DSI_HOST_PHY_TMR_CFG

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles
23:16	RW	0x00	phy_lp2hs_time This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles
15	RO	0x0	Reserved
14:0	RW	0x0000	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress

MIPI_DSI_HOST_PHY_RSTZ

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	Reserved
3	RW	0x0	phy_forcepll When the D-PHY is in ULPS, this bit enables the D-PHY PLL. Dependency: DSI_HOST_FPGA = 0. Otherwise, this bit is Reserved
2	RW	0x0	phy_enableclk When set to1, this bit enables the D-PHY Clock Lane module
1	RW	0x0	phy_rstz When set to 0, this bit places the digital section of the D-PHY in the reset state
0	RW	0x0	phy_shutdownz When set to 0, this bit places the D-PHY macro in power-down state

MIPI_DSI_HOST_PHY_IF_CFG

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state
7:2	RO	0x0	Reserved
1:0	RW	0x3	n_lanes This field configures the number of active data lanes: 2'b00: One data lane (lane 0) 2'b01: Two data lanes (lanes 0 and 1) 2'b10: Three data lanes (lanes 0, 1, and 2) 2'b11: Four data lanes (lanes 0, 1, 2, and 3)

MIPI_DSI_HOST_PHY_STATUS

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12	RO	0x0	phy_ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal
11	RO	0x0	phy_stopstate3lane This bit indicates the status of phystopstate3lane D-PHY signal
10	RO	0x0	phy_ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal
9	RO	0x0	phy_stopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal
8	RO	0x0	phy_ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal
7	RO	0x0	phy_stopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal
6	RO	0x0	phy_rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal
5	RO	0x0	phy_ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal
4	RO	0x0	phy_stopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal
3	RO	0x0	phy_ulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal
2	RO	0x0	phy_stopstateclklane This bit indicates the status of phystopstateclklane D-PHY signal
1	RO	0x0	phy_direction This bit indicates the status of phydirection D-PHY signal
0	RO	0x0	phy_lock This bit indicates the status of phylock D-PHY signal

MIPI_DSI_HOST_INT_ST0

Address: Operational Base + offset (0x00bc)

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Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved
20	RO	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RO	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RO	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RO	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report

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Bit	Attr	Reset Value	Description
5	RO	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_ST1

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RO	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RO	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RO	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RO	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RO	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted

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Bit	Attr	Reset Value	Description
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RO	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_MSK0

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RW	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report

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Bit	Attr	Reset Value	Description
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_MSK1

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted

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Bit	Attr	Reset Value	Description
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_FORCE0

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RW	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report

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Bit	Attr	Reset Value	Description
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_FORCE1

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted

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Bit	Attr	Reset Value	Description
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_VID_SHADOW_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	vid_shadow_pin_req When set to 1, the video request is done by external pin. In this mode, vid_shadow_req is ignored
15:9	RO	0x0	Reserved
8	RW	0x0	vid_shadow_req When set to 1, the DPI registers are copied to the auxiliary registers. After copying, this bit is auto cleared
7:1	RO	0x0	Reserved
0	RW	0x0	vid_shadow_en When set to 1, DPI receives the active configuration from the auxiliary registers. When this bit is set along with the id_shadow_req bit, the auxiliary registers are automatically updated

MIPI_DSI_HOST_DPI_VCID_ACT

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING_ACT

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	Reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	Reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4’b0000: 16-bit configuration 1 4’b0001: 16-bit configuration 2 4’b0010: 16-bit configuration 3 4’b0011: 18-bit configuration 1 4’b0100: 18-bit configuration 2 4’b0101: 24-bit 4’b0110: 20-bit YCbCr 4:2:2 loosely packed 4’b0111: 24-bit YCbCr 4:2:2 4’b1000: 16-bit YCbCr 4:2:2 4’b1001: 30-bit 4’b1010: 36-bit 4’b1011-4’b1111: 12-bit YCbCr 4:2:0

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MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RO	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	Reserved
7:0	RO	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_VID_MODE_CFG_ACT

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 1'b0: Vertical mode 1'b1: Horizontal mode
23:21	RO	0x0	Reserved
20	RO	0x0	vpg_mode This field is to select the pattern: 1'b0: Color bar (horizontal or vertical) 1'b1: BER pattern (vertical only)
19:17	RO	0x0	Reserved
16	RO	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RO	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RO	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RO	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows
12	RO	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows
11	RO	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows

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Bit	Attr	Reset Value	Description
10	RO	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RO	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows
8	RO	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	Reserved
1:0	RO	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE_ACT

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RO	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RO	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE_ACT

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

MIPI_DSI_HOST_VID_HSA_TIME_ACT

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RO	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME_ACT

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME_ACT

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14:0	RO	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES_ACT

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RO	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VBP_LINES_ACT

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

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MIPI_DSI_HOST_VID_VFP_LINES_ACT

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RO	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RO	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_SDF_3D_ACT

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet
15:6	RO	0x0	Reserved
5	RO	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent. 1'b1: Right eye data is sent first, and then the left eye data is sent
4	RO	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RO	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

13.5 Application Notes

13.5.1 LOW POWER MODE (FOR DSI ONLY)

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the D-PHY with few operations. The following is a step by step instruction for low power mode in and out.
Perform the following steps to configure the DPI packet transmission:
Step1: Global configuration:
Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.
Step2: Configure the DPI Interface to define how the DPI interface interacts with the controller.
Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.
Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.
Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the dpidataen signal and enables if it is active low.
Configure vsync_active_low (DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
Configure vsync_active_low (DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
Configure vsync_active_low (DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.
Configure vsync_active_low (DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.
Configure en18_loosely (DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.
Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.
Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.
Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.
Configure frame_BTA_ack (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.
Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the DWC_mipi_dsi_host to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.
Configure the register fiedl vid_mode_type (VID_MODE_CFG-[10]), num_chunks (VID_PKT_CFG-[20:11]), and null_pkt_size (VID_PKT_CFG-[30:21]) are automatically ignored by the DWC_mipi_dsi_host.

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Non-Burst mode: In this mode, the processor uses the partitioning properties of the DWC_mipi_dsi_host to divide the video line transmission into several DSI packets. This is done to match th pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration does not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b0x.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b00x to enable the transmission of sync pulses.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b01to enable the transmission of sync events.
Configure the vid_mode_type field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.
Configure the en_multi_pkt field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.
Configure the num_chunks field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.
Configure the en_null_pkt field (VID_MODE_CFG-[10]) to enable the insertion of null packets between video packets.
The field is effective only when en_multi_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.
Configure the null_pkt_size field (VID_MODE_CFG-[30:21]) with the actual size of the inserted null packet.
Step4: Define the DPI Horizontal timing configuration as follows:
Configure the hline_time field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline_time is a result of a round of a number. If the DWC_mipi_dsi_host is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the DWC_mipi_dsi_host can have a number of errors that can cause a malfunction of the video transmission.
Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).
Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.
Step5: Define the Vertical line configuration:
Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.
Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.
Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.
Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

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Chapter 14 MIPI CSI Trasmitter Device (CSI2TX）

14.1 Overview

MIPI CSI Transmitter is used in mobile and high-speed serial applications where a camera can send the video data using it over MIPI lines to the MIPI CSI Receiver for decoding the data and use it for subsequent processing. MIPI CSI Transmitter adheres to MIPI CSI Specification .The MIPI CSI Transmitter along with DPHY provides a complete solution for encoding MIPI data.
The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.
CSI2TX supports the following features:

- Support APB2.0 Slave interface
- Support VOP interface
  - Format : RAW8, RAW10
  - Data type , word count , virtual channel configuration
- Compliant with MIPI CSI-2 Spec v1.3 specification
  - Compliant with MIPI DPHY V1.2
  - Lane configuration: programmable 1,2 or 4 Data Lane Configuration
    - Operate in continuous/non-continuous clock modes
  - Data Rate : up to 1.2Gbps per lane

14.2 Block Diagram

CSI2TX comprises with:
Cam_interface:
The interface from the camera is though sync, data, and data enable signals. This module fetches the data from camera interface, groups the data in 128-bit format and places it in the payload FIFO
Header_AFIFO:
This is an asynchronous FIFO that stores the header of packet
Payload_AFIFO:
This is an asynchronous FIFO, which stores the pixel to byte converted packed sensor data in to 128-bit for internal processing. This buffer also helps in handing delay and difference in clock rates of write and read domains.
Packetizer:
On the transmitter side of a CSI-2 Link, packetizer converts parallel data and signal events are converted into packets. The packetizer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the DPHY.
Tx_FIFO:
Sensor data is stored in this synchronous configurable FIFO before getting distributed in to the lanes based on configuration. This FIFO handle the latency which arises in DHY to start the byte transfer.
LANE_Distributor:
Sensor data is sent across single/multiple lanes based on the lane configuration register
REG_File:
This block holds the complete registers required for CSI transmitter to be operational. APB interface is provided to control the registers. This module works in the apb_clk domain.

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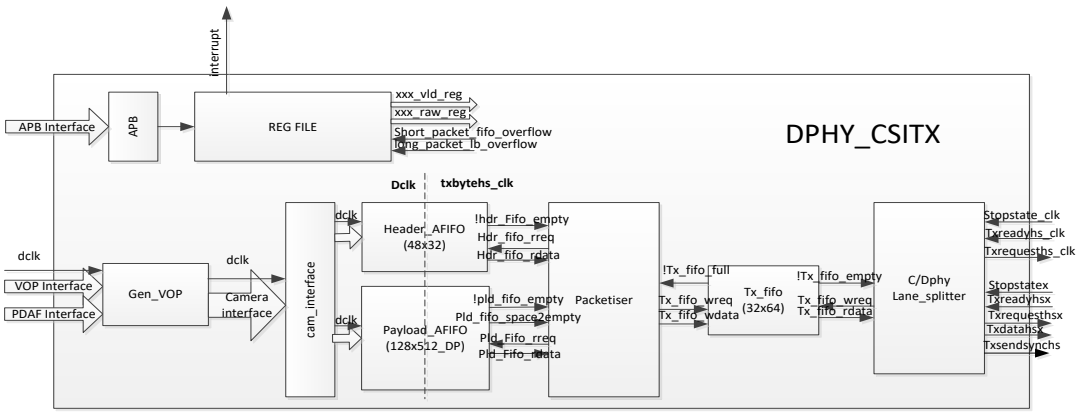

Fig. 14-1 CSI TX Block Diagram

14.3 Register Description

14.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

14.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSITX_CONFIG_DONE	0x0000	W	0x00000000	CSITX config done
CSITX_CSITX_EN	0x0004	W	0x00000000	CSITX enable
CSITX_CSITX_VERSION	0x0008	W	0x00000000	CSITX version
CSITX_SYS_CTRL0_IMD	0x0010	W	0x00000000	System control0
CSITX_SYS_CTRL2	0x0018	W	0x00000001	System control2
CSITX_SYS_CTRL3_IMD	0x001c	W	0x00000001	System control3
CSITX_TIMING_CTRL	0x0020	W	0x00000000	System timing control
CSITX_TIMING_VPW_NUM	0x0024	W	0x00000000	VPW number
CSITX_TIMING_VBP_NUM	0x0028	W	0x00000000	VBP number
CSITX_TIMING_VFP_NUM	0x002c	W	0x00000000	VFP number
CSITX_TIMING_HPW_PADDING_NUM	0x0030	W	0x00000000	HPW number in padding mode
CSITX_VOP_PATH_CTRL	0x0040	W	0x00002a0e	VOP path control
CSITX_VOP_PATH_PKT_CTRL	0x0050	W	0x00000000	VOP path packet control
CSITX_CSITX_STATUS0	0x0070	W	0x00000000	CSITX status0
CSITX_CSITX_STATUS1	0x0074	W	0x00000000	CSITX status1
CSITX_CSITX_STATUS2	0x0078	W	0x00000000	CSITX status2
CSITX_LINE_FLAG_NUM	0x007c	W	0x00000000	Line flag number
CSITX_INTR_EN_IMD	0x0080	W	0x00000000	Interrupt enable
CSITX_INTR_CLR_IMD	0x0084	W	0x00000000	Interrupt clear
CSITX_INTR_STATUS	0x0088	W	0x00000000	Interrupt status
CSITX_INTR_RAW_STATUS	0x008c	W	0x00000000	Interrupt raw status

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Name	Offset	Size	Reset Value	Description
CSITX_ERR_INTR_EN_IMD	0x0090	W	0x00000000	Error interrupt enable
CSITX_ERR_INTR_CLR_IMD	0x0094	W	0x00000000	Error interrupt enable
CSITX_ERR_INTR_STATUS_IMD	0x0098	W	0x00000000	Error interrupt enable
CSITX_ERR_INTR_RAW_STATUS_IMD	0x009c	W	0x00000000	Error interrupt enable
CSITX_ULPS_CTRL_IMD	0x00a0	W	0x00000000	ULPS mode control
CSITX_LPDT_CTRL_IMD	0x00a4	W	0x00000000	LPDT mode control
CSITX_LPDT_DATA_IMD	0x00a8	W	0x00000000	LPDT data
CSITX_DPHY_CTRL	0x00b0	W	0x00000078	DPHY control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

14.3.3 Detail Register Description

CSITX_CONFIG_DONE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	config_done_mode 1'b0: Config done when frm_end_rx 1'b1: Config done when frm_end_tx
7:5	RO	0x0	reserved
4	W1C	0x0	config_done_imd Make register valid immediately
3:1	RO	0x0	reserved
0	RW	0x0	config_done In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame

CSITX_CSITX_EN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	gating_en Auto gating 1'b0: Disable 1'b1: Enable
30:22	RO	0x0	reserved
21	RW	0x0	gating_vop_clk_dis 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	gating_cam_clk_dis 1'b0: Disable 1'b1: Enable
19	RW	0x0	gating_esc_clk_dis 1'b0: Disable 1'b1: Enable
18	RW	0x0	gating_hs_clk_dis 1'b0: Disable 1'b1: Enable
17	RW	0x0	gating_wordhs_clk_dis 1'b0: Disable 1'b1: Enable
16	RW	0x0	gating_bytehs_clk_dis 1'b0: Disable 1'b1: Enable
15:9	RO	0x0	reserved
14	RW	0x0	vop_yc_swap 1'b0: Disable 1'b1: Enable
13	RW	0x0	vop_uv_swap 1'b0: Disable 1'b1: Enable
12	RW	0x0	vop_yuv422_en 1'b0: Disable 1'b1: Enable
11:9	RO	0x0	reserved
8	RW	0x0	vop_p2_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x0	lane_num 2'b00: One-lane 2'b01: Two-lane 2'b10: Three-lane 2'b11: Four-lane
3	RO	0x0	reserved
2	RW	0x0	dphy_en 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	csitx_en 1'b0: Disable 1'b1: Enable

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CSITX_CSITX_VERSION

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csitx_version CSITX version

CSITX_SYS_CTRL0_IMD

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	soft_rst Soft reset 1'b0: Disable 1'b1: Enable

CSITX_SYS_CTRL2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	adv_read_pld_num If adv_read_pld_en is 1 , start to read pld fifo when pld_fifo_space2empty >= wc_128b - adv_read_pld_num
15:9	RO	0x0	reserved
8	RW	0x0	adv_read_pld_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	vop_whole_frm_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	idi_whole_frm_en 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	hsync_enable Send hsync timing short packet
0	RW	0x1	vsync_enable Send vsync timing short packet

CSITX_SYS_CTRL3_IMD

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	cont_mode_clk_clr Disable clock lane txrequesths in continuous mode

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Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4	RW	0x0	cont_mode_clk_set Enable clock lane txrequesths in continuous mode
3:1	RO	0x0	reserved
0	RW	0x1	non_continous_mode Non-continuous mode

CSITX_TIMING_CTRL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hpw_cnt_num HPW timing adjustment number
15:5	RO	0x0	reserved
4	RW	0x0	hpw_padding_en Enable hpw timing adjustment in padding mode 1'b0: Disable 1'b1: Enable
3	RW	0x0	hpw_en Enable hpw timing adjustment 1'b0: Disable 1'b1: Enable
2	RW	0x0	vfp_en Enable vfp timing adjustment 1'b0: Disable 1'b1: Enable
1	RW	0x0	vbp_en Enable vbp timing adjustment 1'b0: Disable 1'b1: Enable
0	RW	0x0	vpw_en Enable vpw timing adjustment 1'b0: Disable 1'b1: Enable

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CSITX_TIMING_VPW_NUM

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vpw_cnt_num VPW timing adjustment number

CSITX_TIMING_VBP_NUM

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vbp_cnt_num VBP timing adjustment number

CSITX_TIMING_VFP_NUM

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vfp_cnt_num VFP timing adjustment number

CSITX_TIMING_HPW_PADDING_NUM

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	hpw_padding_num HPW timing adjustment number in padding mode

CSITX_VOP_PATH_CTRL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	vop_wc_userdefine Word count user-define
15:14	RW	0x0	vop_vc_userdefine Virtual num user-define
13:8	RW	0x2a	vop_dt_userdefine Data type user-define
7:4	RW	0x0	vop_pixel_format 4'b0000: Raw8 4'b0001: Raw10 4'b0010: Pixel10 4'b0011: Pixel128 4'b0100: Raw12 4'b0101: Pixel12 4'b1xxx: Reserved
3	RW	0x1	vop_wc_userdefine_en Enable word count user-define 1'b0: Disable 1'b1: Enable
2	RW	0x1	vop_vc_userdefine_en Enable virtual num user-define 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x1	vop_dt_userdefine_en Enable datatype user-define 1'b0: Disable 1'b1: Enable
0	RW	0x0	vop_path_en Enable channel0 1'b0: Disable 1'b1: Enable

CSITX_VOP_PATH_PKT_CTRL

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	vop_wc_active The active byte number of one packet
15:9	RO	0x0	reserved
8	RW	0x0	vop_pkt_padding_en Enable packet padding 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	vop_line_padding_num Line padding number, real number -1
4	RW	0x0	vop_line_padding_en Enable packet padding 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

CSITX_CSITX_STATUS0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	lane_splitter_idle Lane splitter idle
5	RO	0x0	packetiser_idle Packetizer idle
4	RO	0x0	tx_buff_emtpy TX fifo empty
3	RO	0x0	pld_lb_valid Payload lb valid
2	RO	0x0	pld_lb_empty Payload lb emtpy
1	RO	0x0	hdr_fifo_empty Header fifo empty

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Bit	Attr	Reset Value	Description
0	RO	0x0	csitx_idle CSITX idle

CSITX_CSITX_STATUS1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	txreadyesc_3 Date lane3 txreadyesc
18	RO	0x0	txreadyesc_2 Date lane2 txreadyesc
17	RO	0x0	txreadyesc_1 Date lane1 txreadyesc
16	RO	0x0	txreadyesc_0 Date lane0 txreadyesc
15	RO	0x0	txulpsactivenot_3 Date lane3 txuppsactivenot
14	RO	0x0	txulpsactivenot_2 Date lane2 txuppsactivenot
13	RO	0x0	txulpsactivenot_1 Date lane1 txuppsactivenot
12	RO	0x0	txulpsactivenot_0 Date lane0 txuppsactivenot
11	RO	0x0	txreadyhs_3 Lane3 txreadyhs
10	RO	0x0	txreadyhs_2 Lane2 txreadyhs
9	RO	0x0	txreadyhs_1 Lane1 txreadyhs
8	RO	0x0	txreadyhs_0 Lane0 txreadyhs
7	RO	0x0	stopstate_3 Lane3 stopstate
6	RO	0x0	stopstate_2 Lane2 stopstate
5	RO	0x0	stopstate_1 Lane1 stopstate
4	RO	0x0	stopstate_0 Lane0 stopstate
3	RO	0x0	reserved
2	RO	0x0	txulpsactivenot_clk CLK lane txuppsactivenot
1	RO	0x0	stopstate_clk CLK lane lock

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Bit	Attr	Reset Value	Description
0	RW	0x0	dphy_pll_lock DPHY PLL lock

CSITX_CSITX_STATUS2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cphy_scanline CPHY scan line
15:0	RO	0x0000	dphy_scanline DPHY scan line

CSITX_LINE_FLAG_NUM

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	line_num_flag1 Line num flag1
15:0	RW	0x0000	line_num_flag0 Line num flag0

CSITX_INTR_EN_IMD

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	intr_en_write_enable "Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:11	RO	0x0	reserved
10	RW	0x0	intr_en_csitx_idle Enable csitx idle interrupt
9	RW	0x0	intr_en_pll_lock Enable pll lock interrupt
8	RW	0x0	intr_en_stopstate Enable dphy stopstate interrupt
7	RW	0x0	intr_en_line_flag1 Enable line_flag1 interrupt
6	RW	0x0	intr_en_line_flag0 Enable line_flag0 interrupt
5	RW	0x0	intr_en_line_end_tx Enable transmitted line_end interrupt
4	RW	0x0	intr_en_frm_end_tx Enable transmitted frm_end interrupt
3	RW	0x0	intr_en_frm_st_tx Enable transmitted frm_st interrupt

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Bit	Attr	Reset Value	Description
2	RW	0x0	intr_en_line_end_rx Enable received line_end interrupt
1	RW	0x0	intr_en_frm_end_rx Enable received frm_end interrupt
0	RW	0x0	intr_en_frm_st_rx Enable received frm_st interrupt

CSITX_INTR_CLR_IMD

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	intr_clr_write_enable "Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:11	RO	0x0	reserved
10	W1C	0x0	intr_clr_csitx_idle Clear csitx idle interrupt
9	W1C	0x0	intr_clr_pll_lock Clear pll lock interrupt
8	W1C	0x0	intr_clr_stopstate Clear dphy stopstate interrupt
7	W1C	0x0	intr_clr_line_flag1 Clear line_flag1 interrupt
6	W1C	0x0	intr_clr_line_flag0 Clear line_flag0 interrupt
5	W1C	0x0	intr_clr_line_end_tx Clear transmitted line_end interrupt
4	W1C	0x0	intr_clr_frm_end_tx Clear transmitted frm_end interrupt
3	W1C	0x0	intr_clr_frm_st_tx Clear transmitted frm_st interrupt
2	W1C	0x0	intr_clr_line_end_rx Clear received line_end interrupt
1	W1C	0x0	intr_clr_frm_end_rx Clear received frm_end interrupt
0	W1C	0x0	intr_clr_frm_st_rx Clear received frm_st interrupt

CSITX_INTR_STATUS

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	W1C	0x0	intr_sts_csitx_idle CSITX idle interrupt status

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Bit	Attr	Reset Value	Description
9	RO	0x0	intr_sts_pll_lock PHY PLL lock interrupt status
8	RO	0x0	intr_sts_stopstate PHY stopstate interrupt status
7	RO	0x0	intr_sts_line_flag1 Line flag1 interrupt status
6	RO	0x0	intr_sts_line_flag0 Line flag0 interrupt status
5	RO	0x0	intr_sts_frame_end_tx TX frame end interrupt status
4	RO	0x0	intr_sts_line_end_tx TX line end interrupt status
3	RO	0x0	intr_sts_frm_st_tx TX frame start interrupt status
2	RO	0x0	intr_sts_frm_end_rx RX frame end interrupt status
1	RO	0x0	intr_sts_line_end_rx RX line end interrupt status
0	RW	0x0	intr_sts_frm_st_rx RX frame start interrupt status

CSITX_INTR_RAW_STATUS

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	intr_csitx_idle CSITX idle interrupt raw status
9	RO	0x0	intr_pll_lock PHY PLL lock interrupt raw status
8	RW	0x0	intr_stopstate PHY stopstate interrupt raw status
7	RW	0x0	intr_line_flag1 Line flag1 interrupt raw status
6	RW	0x0	intr_line_flag0 Line flag0 interrupt raw status
5	RO	0x0	intr_frm_end_tx TX frame end interrupt raw status
4	RW	0x0	intr_line_end_tx TX line end interrupt raw status
3	RO	0x0	intr_frm_st_tx TX frame start interrupt raw status
2	RO	0x0	intr_line_end_rx RX frame end interrupt raw status

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Bit	Attr	Reset Value	Description
1	RO	0x0	intr_frm_end_rx RX line end interrupt raw status
0	RO	0x0	intr_frm_st_rx RX frame start interrupt raw status

CSITX_ERR_INTR_EN_IMD

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	intr_en_write_enable "Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	intr_en_txreadyhs_error1 Enable txreadyhs error1 interrupt
10	RW	0x0	intr_en_txreadyhs_error0 Enable txreadyhs error0 interrupt
9	RW	0x0	intr_en_outbuffer_underflow Enable output fifo underflow interrupt
8	RW	0x0	intr_en_outbuffer_overflow Enable output fifo overflow interrupt
7	RW	0x0	intr_en_pld_fifo_underflow Enable payload fifo underflow interrupt
6	RW	0x0	intr_en_pld_fifo_overflow Enable payload fifo overflow interrupt
5	RW	0x0	intr_en_hdr_fifo_underflow Enable header fifo underflow interrupt
4	RW	0x0	intr_en_hdr_fifo_overflow Enable header fifo overflow interrupt
3	RW	0x0	intr_en_idi_pld_fifo_underflow Enable idi payload fifo underflow interrupt
2	RW	0x0	intr_en_idi_pld_fifo_overflow Enable idi payload fifo overflow interrupt
1	RW	0x0	intr_en_idi_hdr_fifo_underflow Enable idi header fifo underflow interrupt
0	RW	0x0	intr_en_idi_hdr_fifo_overflow Enable idi header fifo overflow interrupt

CSITX_ERR_INTR_CLR_IMD

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	intr_clr_write_enable "Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	intr_clr_txreadyhs_error1 Clear txreadyhs error1 interrupt
10	RW	0x0	intr_clr_txreadyhs_error0 Clear txreadyhs error0 interrupt
9	RW	0x0	intr_clr_outbuffer_underflow Clear output fifo underflow interrupt
8	RW	0x0	intr_clr_outbuffer_overflow Clear output fifo overflow interrupt
7	RW	0x0	intr_clr_pld_fifo_underflow Clear payload fifo underflow interrupt
6	RO	0x0	reserved
5	RW	0x0	intr_clr_hdr_fifo_underflow Clear header fifo underflow interrupt
4	RW	0x0	intr_clr_hdr_fifo_overflow Clear header fifo overflow interrupt
3	RW	0x0	intr_clr_idi_pld_fifo_underflow Clear idi payload fifo underflow interrupt
2	RW	0x0	intr_clr_idi_pld_fifo_overflow Clear idi payload fifo overflow interrupt
1	RW	0x0	intr_clr_idi_hdr_fifo_underflow Clear idi header fifo underflow interrupt
0	RW	0x0	intr_clr_idi_hdr_fifo_overflow Clear idi header fifo overflow interrupt

CSITX_ERR_INTR_STATUS_IMD

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	intr_sts_txreadyhs_error1 Txreadyhs error1 interrupt
10	RW	0x0	intr_sts_txreadyhs_error0 Txreadyhs error0 interrupt
9	RW	0x0	intr_sts_outbuffer_underflow Output fifo underflow interrupt
8	RW	0x0	intr_sts_outbuffer_overflow Output fifo overflow interrupt
7	RW	0x0	intr_sts_pld_fifo_underflow Payload fifo underflow interrupt

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Bit	Attr	Reset Value	Description
6	RW	0x0	intr_sts_pld_fifo_overflow Payload fifo overflow interrupt
5	RW	0x0	intr_sts_hdr_fifo_underflow Header fifo underflow interrupt
4	RW	0x0	intr_sts_hdr_fifo_overflow Header fifo overflow interrupt
3	RW	0x0	intr_sts_idi_pld_fifo_underflow IDI payload fifo underflow interrupt
2	RW	0x0	intr_sts_idi_pld_fifo_overflow IDI payload fifo overflow interrupt
1	RW	0x0	intr_sts_idi_hdr_fifo_underflow IDI header fifo underflow interrupt
0	RW	0x0	intr_sts_idi_hdr_fifo_overflow IDI header fifo overflow interrupt

CSITX_ERR_INTR_RAW_STATUS_IMD

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	intr_txreadyhs_error1 Txreadyhs error1 raw interrupt
10	RW	0x0	intr_txreadyhs_error0 Txreadyhs error0 raw interrupt
9	RW	0x0	intr_outbuffer_underflow Output fifo underflow raw interrupt
8	RW	0x0	intr_outbuffer_overflow Output fifo overflow raw interrupt
7	RW	0x0	intr_pld_fifo_underflow Payload fifo underflow raw interrupt
6	RW	0x0	intr_pld_fifo_overflow Payload fifo overflow raw interrupt
5	RW	0x0	intr_hdr_fifo_underflow Header fifo underflow raw interrupt
4	RW	0x0	intr_hdr_fifo_overflow Header fifo overflow raw interrupt
3	RW	0x0	intr_idi_pld_fifo_underflow IDI payload fifo underflow raw interrupt
2	RW	0x0	intr_idi_pld_fifo_overflow IDI payload fifo overflow raw interrupt
1	RW	0x0	intr_idi_hdr_fifo_underflow IDI header fifo underflow raw interrupt
0	RW	0x0	intr_idi_hdr_fifo_overflow IDI header fifo overflow raw interrupt

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CSITX_ULPS_CTRL_IMD

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	ulps_exit_wait The waiting time of exiting ulps mode
15:12	RO	0x0	reserved
11	RW	0x0	data3_lane_ulps_exit Disable data3 lane ulps mode 1'b0: Disable 1'b1: Enable
10	RW	0x0	data3_lane_ulps_entry Enable data3 lane ulps mode 1'b0: Disable 1'b1: Enable
9	RW	0x0	data2_lane_ulps_exit Disable data2 lane ulps mode 1'b0: Disable 1'b1: Enable
8	RW	0x0	data2_lane_ulps_entry Enable data2 lane ulps mode 1'b0: Disable 1'b1: Enable
7	RW	0x0	data1_lane_ulps_exit Disable data1 lane ulps mode 1'b0: Disable 1'b1: Enable
6	RW	0x0	data1_lane_ulps_entry Enable data1 lane ulps mode 1'b0: Disable 1'b1: Enable
5	RW	0x0	data0_lane_ulps_exit Disable data0 lane ulps mode 1'b0: Disable 1'b1: Enable
4	RW	0x0	data0_lane_ulps_entry Enable data0 lane ulps mode 1'b0: Disable 1'b1: Enable
3	RW	0x0	clk_lane_ulps_exit Disable clk lane ulps mode 1'b0: Disable 1'b1: Enable
2	RW	0x0	clk_lane_ulps_entry Enable clk lane ulps mode 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	ulps_en Enable ulps mode 1'b0: Disable 1'b1: Enable

CSITX_LPDT_CTRL_IMD

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x0	lpdt_lane_num LPDT lane num 2'b00: One lane 2'b01: Two lane 2'b1x: Four lane
1	RW	0x0	lpdt_start Start LPDT transfer
0	RW	0x0	lpdt_en Enable LPDT mode

CSITX_LPDT_DATA_IMD

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lpdt_data LPDT data

CSITX_DPHY_CTRL

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	dphy_enable_3 Enable high speed data3 lane
6	RW	0x1	dphy_enable_2 Enable high speed data2 lane
5	RW	0x1	dphy_enable_1 Enable high speed data1 lane
4	RW	0x1	dphy_enable_0 Enable high speed data0 lane
3	RW	0x1	dphy_enableclk Enable high speed clock lane
2:0	RO	0x0	reserved

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14.4 Interface Timing

14.4.1 Camera interface timing

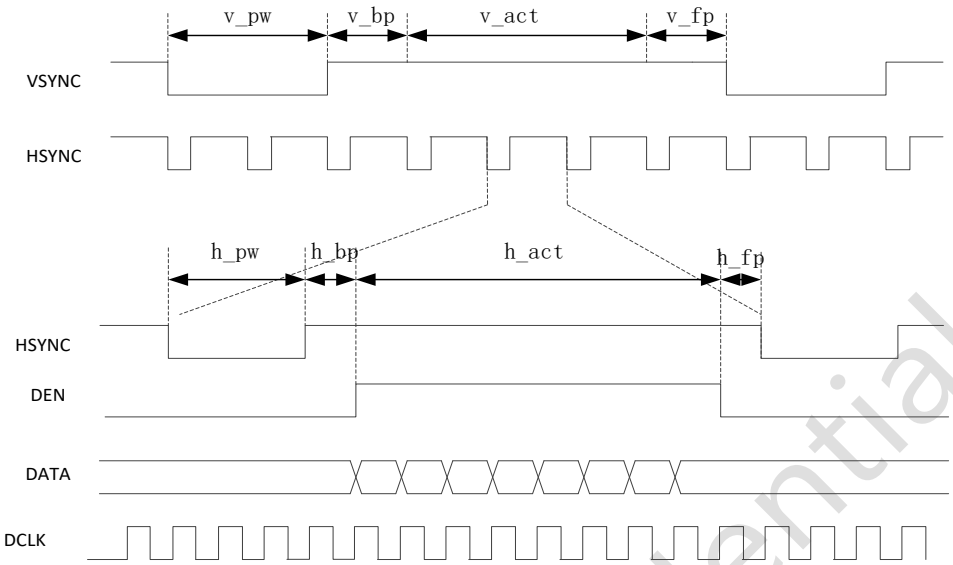

Fig. 14-2 Camera Interface Timing without pdaf

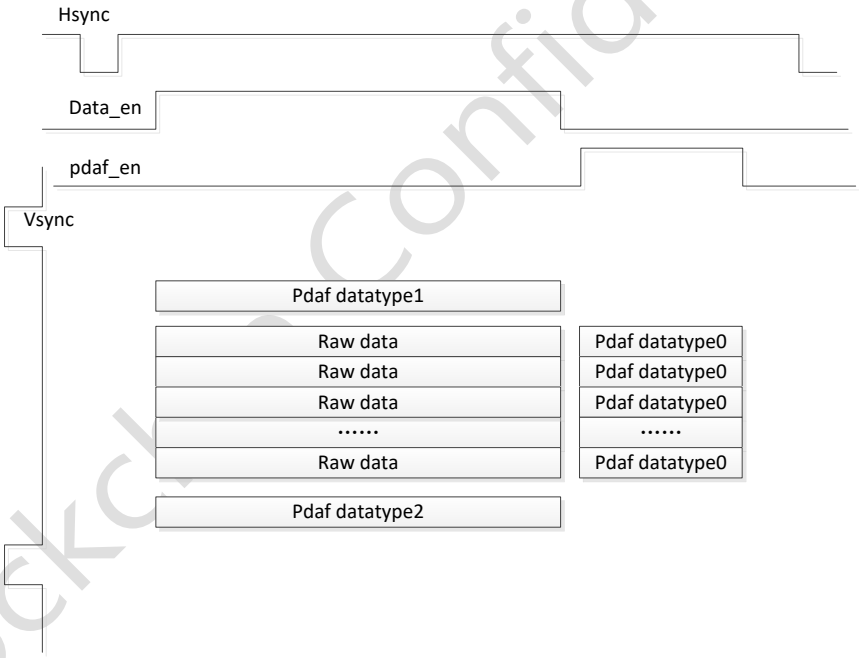

Fig. 14-3 Camera Interface Timing with pdaf

14.4.2 APB interface timing

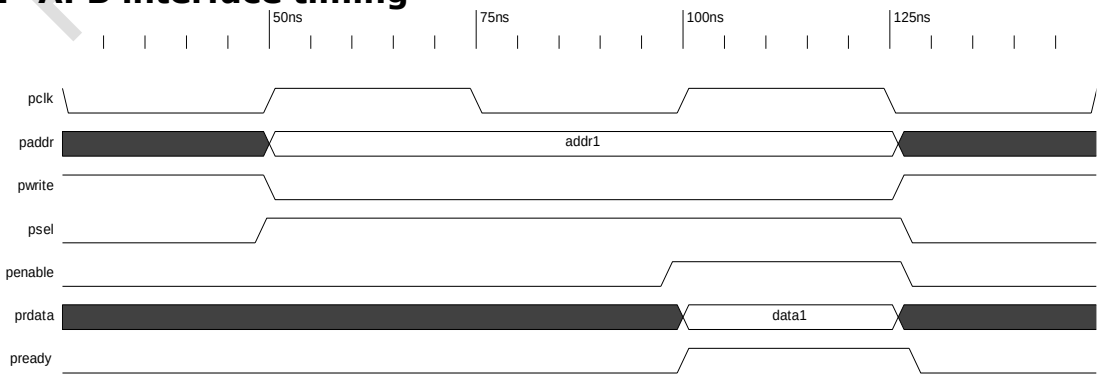

Fig. 14-4 APB Interface Typical Read Timing

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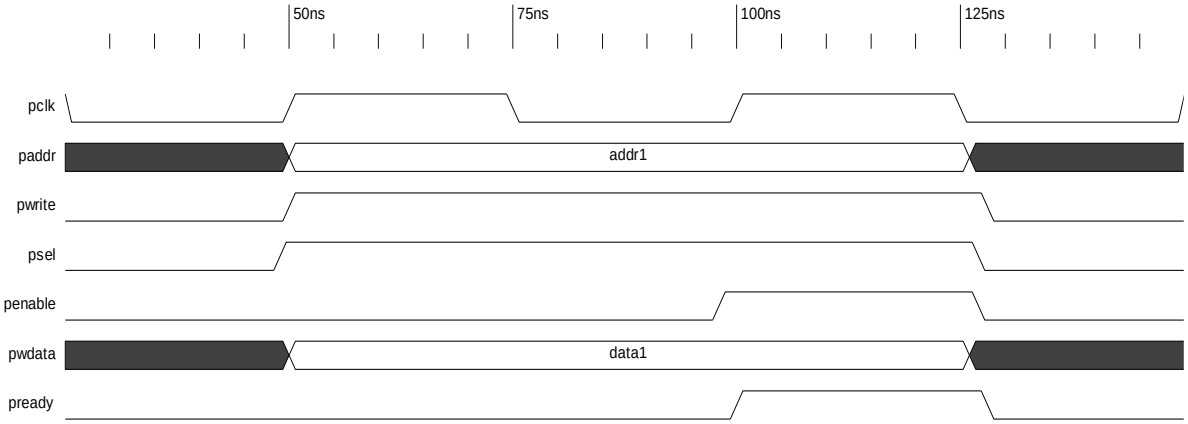

Fig. 14-5 APB Interface Typical Write Timing

14.4.3 DPHY interface timing

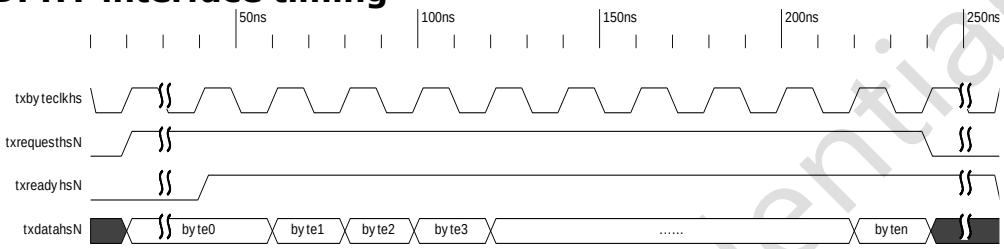

Fig. 14-6 DPHY Interface Typical Write Timing

TxdatahsN is an 8-bit data bus input of data laneN of DPHY that receives data to be transmitted. It is synchronous to the rising edge of txbyteclkhs. When txrequesths is sampled high, the DPHY lane module initiates a Start-of-Transmission (SOT) sequence. When txrequesths is sampled low while txreadyhs is asserted, the lane module initiates an End-of-Transmission (EOT) sequence. TxreadyhsN indicates that txdatahs is accepted by the lane module to be serially transmitted.

14.5 Application Notes

14.5.1 Camera interface configuration guideline

CSI transmitter, to become operational, requires the following register to be programmed.
1. Program CSITX_EN to enable dphy_en, csitx_en and set lane number.
2. Send 0x1 to SYS_CTRL1. Disable bypass_select.
3. Send 0x10 to SYS_CTRL3_IMD to enable continuous mode .Otherwise, send 0x1 to enable non-continuous mode.
4. Program VOP_PATH_CTRL according to application.
5. Program DPHY_CTRL to enable DPHY lane.
6. Send 0x10 to CONFIG_DONE.

The sequence below is for bypass mode.
1. Program CSITX_EN to enable dphy_en, csitx_en and set lane number.
2. Send 0x0 to SYS_CTRL1. Enable bypass_select.
3. Send 0x10 to SYS_CTRL3_IMD to enable continuous mode. Otherwise, send 0x1 to enable non-continuous mode.
4. Program BYPASS_CTRL according to application.
5. Program DPHY_CTRL to enable DPHY lane.
6. Send 0x10 to CONFIG_DONE.

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Chapter 15 LVDS/BT1120/RGB

15.1 Overview

15.1.1 LVDS

LVDS transmitter converts a CMOS signal into a low-voltage differential signal. Using a differential signal reduces the system's susceptibility to noise and EMI emissions. In addition, using a differential signal can deliver high speeds. This results in a very cost-effective solution to some of the greatest bandwidth bottlenecks in many transmission applications.

LVDS supports the following features:

- 150MHz clock support
- LVDS 24bits or 18bits color data output
- PLL requires no external components
- Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode.
- Display mode can be select by input MUX
- Consumes Less Than 1mW When Disabled

15.1.2 BT1120

BT1120 is digital interface for HDTV studio signals. The interface provides a unidirectional interconnection. The data signals are in the form of binary information and are coded accordingly: video data(8-bit); timing reference and identification codes(8-bit); ancillary data.

BT1120 supports the following features:

- 148.5MHz clock support
- BT1120 16bits data output
- Support YUV format
- Support BT1120 dual_edge
- Support Y/C swap and U/V swap
- Maximum support resolution 1920x1080p

15.1.3 RGB

RGB parallel interface. The interface characteristics: generally 3.3V level; need synchronization signal; always refresh image data; need to configure the appropriate timing.

RGB supports the following features:

- RGB 24bits data input
- Support RGB/YUV format
- Maximum support resolution 1920x1080p
- Maximum support clock 150MHz

15.1.4 YUV

The timing of YUV is similar to RGB, but the data bit width is changed from 24bit of YUV to 16bit.

YUV supports the following features:

- 148.5MHz clock support
- YUV 16bits data output
- Support YUV format
- Support Y/C swap and U/V swap
- Maximum support resolution 1920x1080p

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15.2 Block Diagram

15.2.1 LVDS MODULE

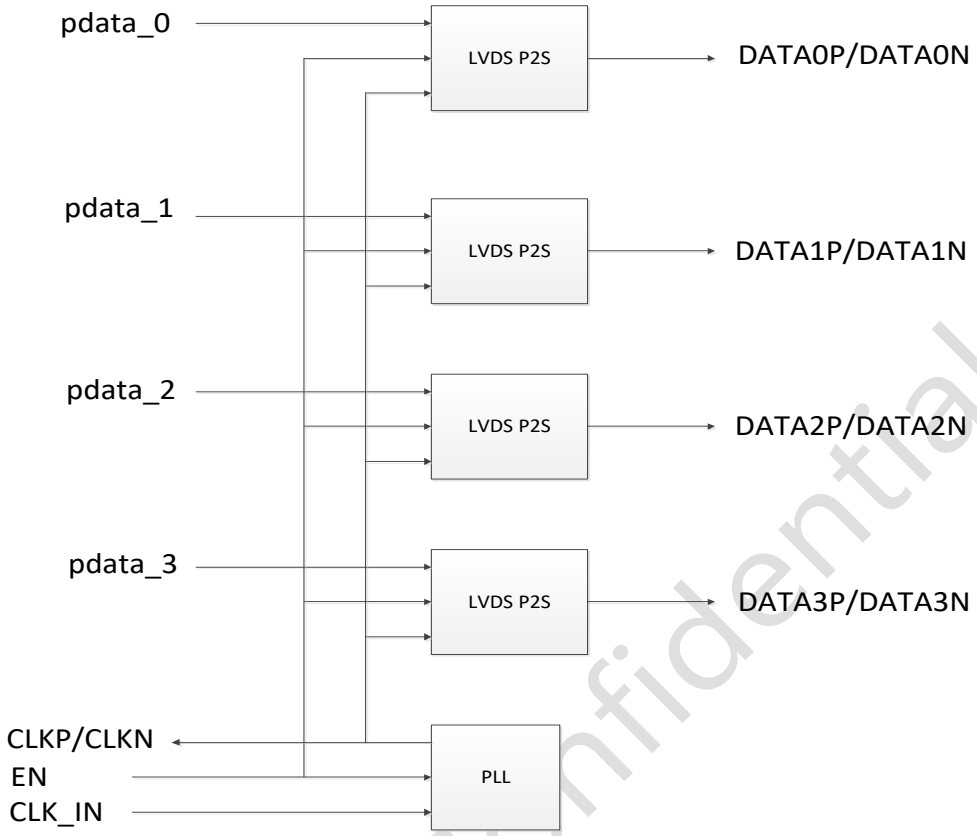
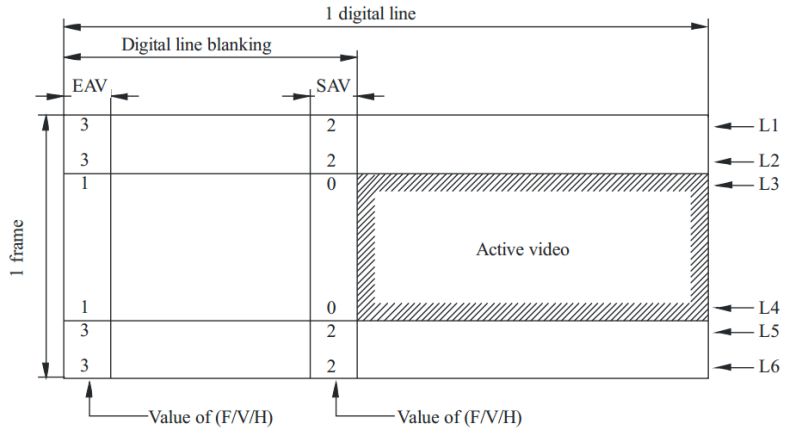


Fig. 15-1 LVDS TX Block Diagram

15.2.2 BT1120 MODULE



(a)frame timing relationship for progressive systems

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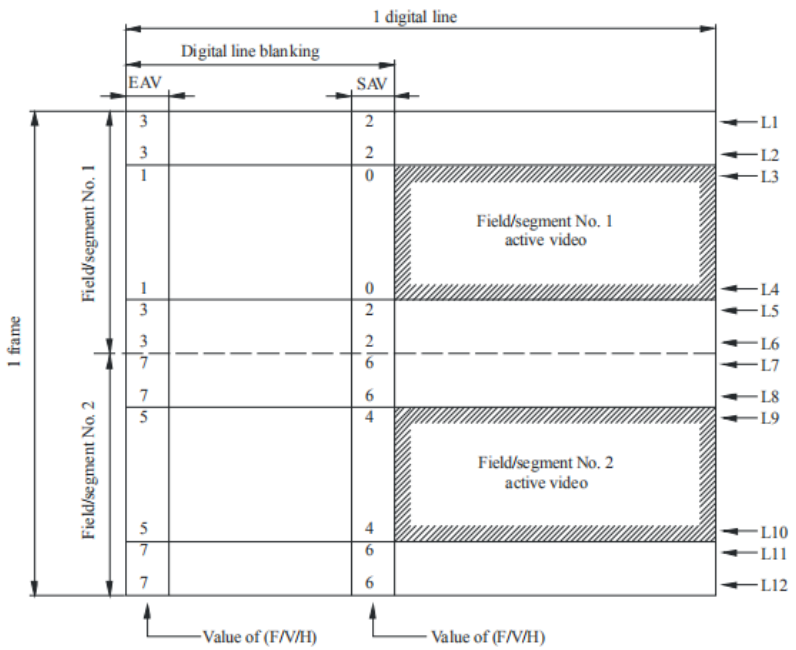

(b)Field/segment timing relationship for interlace and segmented frame systems

Fig. 15-2 frame timing relationship of the BT1120

timing reference code				Line blanking area					timing reference code				Valid pixel(YUV422)						
FF	00	00	EAV	80	10	...	80	10	FF	00	00	SAV	Cb0	Cr0	Cb2	Cr2	...	Cb1919	Cr1919
FF	00	00	EAV	80	10	...	80	10	FF	00	00	SAV	Y0	Y1	Y2	Y3	...	Y1918	Y1919

Fig. 15-3 BT1120 line data format

15.2.3 RGB MODULE

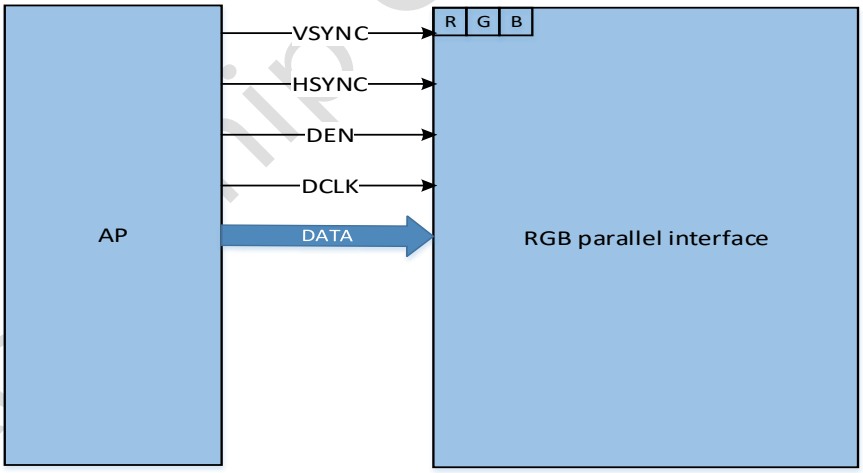

Fig. 15-4 RGB parallel interface

15.3 Function Description

15.3.1 LVDS Data Processing

LVDS PHY implements LVDS TIA/EIA protocol. LVDS PHY contains four 7-bit parallel-load serial-out shift registers, a 7X clock PLL, and five Low Voltage Differential Signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver.

When transmitting, parallel data, pdata0/1/2/3 are each loaded into registers upon the edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times, and then used to unload the data registers in7-bit slices and serially. The four serial streams and

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a phase-locked clock (CLKOUT) are then output to LVDS output drivers.
The frequency of CLKOUT is the same as the input clock, CLKIN.

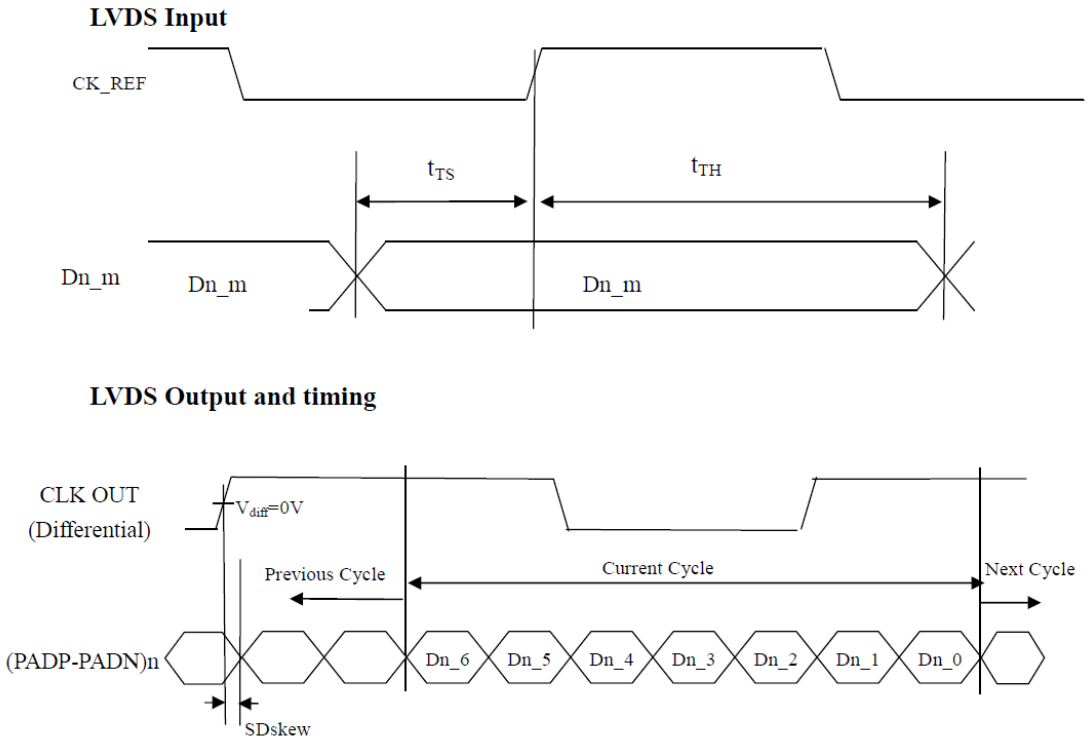

Fig. 15-5 LVDS TX Interface Timing

15.3.2 LVDS Format

LVDS FORMAT converts LCDC RGB interface to LVDS format data, only support 8-bit/6-bit mode. Table 15-1 is LVDSFORMAT input data format.

Table 15-1 LVDS Address Mapping

Serial channel	Data Bits	8-Bit			6-Bit	4-Bit	
		Format-1	Format-2	Format-3		Non-Linear Step Size	Linear Step Size
Y0	D0	R0	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3

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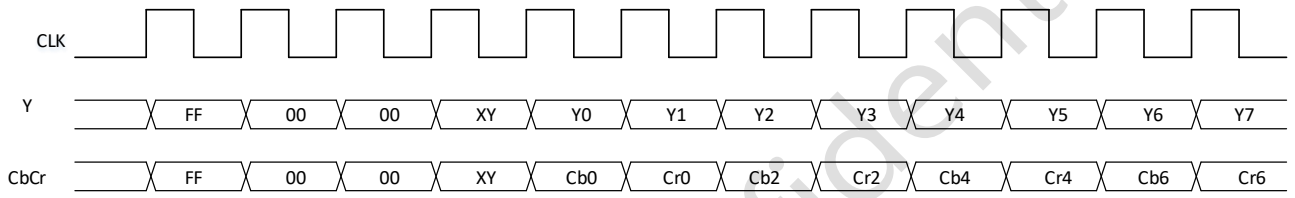
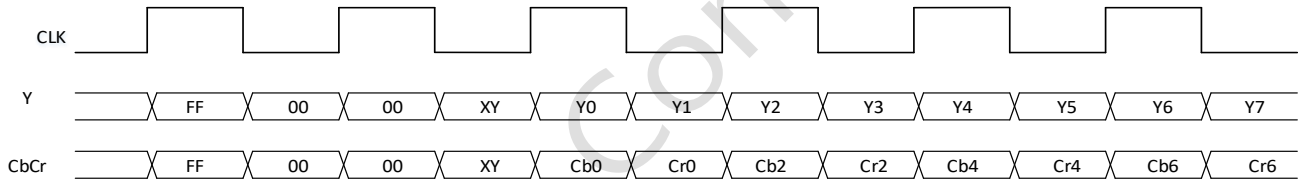
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUIT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

15.3.3 BT1120 Data Processing



(1) bt1120 single_edge



(2) bt1120 dual_edge

Fig. 15-6 relationship between clock and data in the system

15.3.4 RGB Data Processing

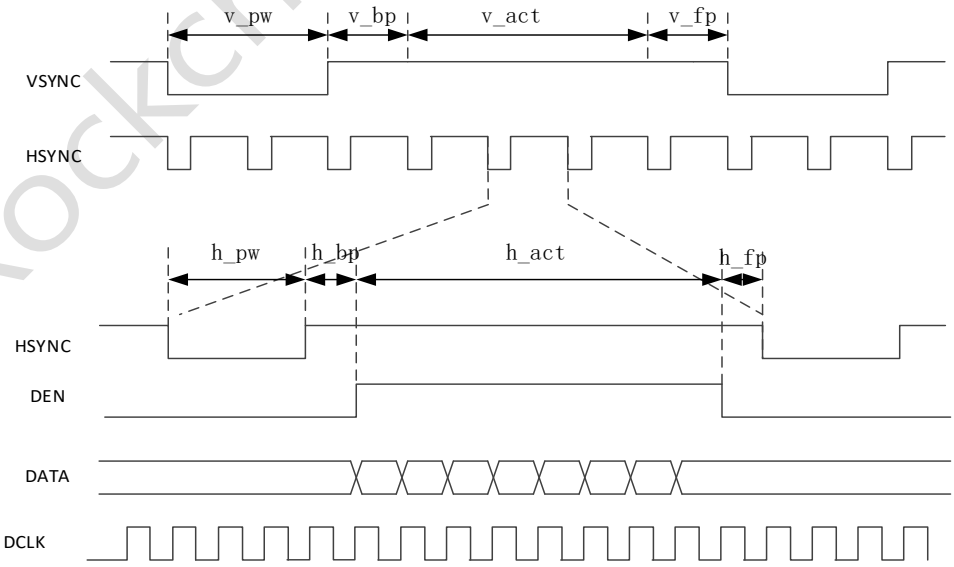


Fig. 15-7 RGB interface timing

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15.3.5 YUV Data Processing

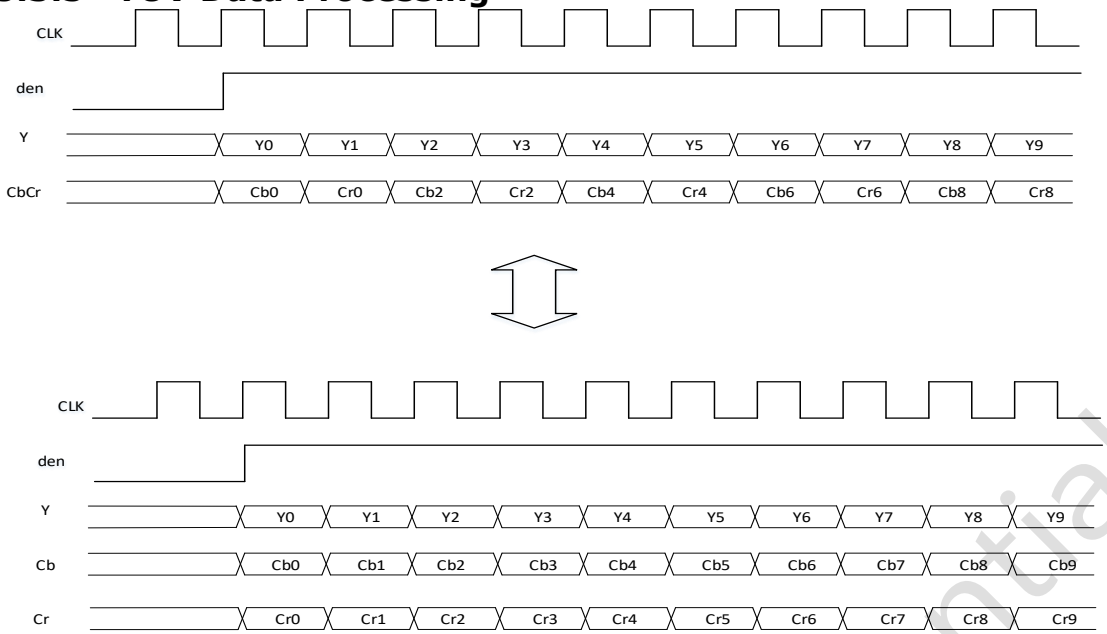

Fig. 15-8 YUV data bit width transform

15.4 Register Description

This section describes the control/status registers of the design.

15.4.1 Registers Summary

Refer to GRF

15.4.2 Detail Register Description

Refer to GRF

15.5 Interface Description

15.5.1 Video Input Source

In this chip, the RGB/BT1120 RX/YUV RX video source come from IO interface. The LVDS and the RGB/BT1120 TX/YUV TX video source come from POST PROCESS.

15.6 Application Notes

15.6.1 LVDS mode

When used in LVDS mode, LVDS transmitter source from post process, vop_dclk need get invert, then input to LVDS.
When LVDS panel is LSB receive mode, lvds_msbsel =1, otherwise lvds_msbsel =0.
When LVDS output format is 8bit mode format-1/8bit mode format-2, configure grf_lvds_con0 in 24-bit color mode.
When LVDS output format is 8bit mode format-3/6bit mode,configure grf_lvds_con0 in 18-bit color mode.
Step1: configure LVDS_TX_CON
Step2: configure TXPHY_CON:
Txphy_con0: grf_bus_width=2’d3, grf_gvi_lvds_en=1’b1, grf_modulea_en= 1’b1;
Txphy_con7: sw_tx_mode=2’d2/2’d3;
Txphy_con10: tx2_ckdrv_en=1’b1, tx7_ckdrv_en;

15.6.2 BT1120 encoder

When use BT1120 encoder mode, BT1120 data source from post process, and output to IO interface. If other devices receive data from the BT1120 encoder, the input clock need get invert.
Step1: configure SYSTEM_CON0
output_mode = 5’b01xxx; sw_bt_data_oen = 1’b0.
Step2: configure RGB_ENC_CON

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Step3: configure SCALER_CON
Configure the timing sequence based on the information of the input image.

15.6.3 BT1120 decoder

When use BT1120 decoder mode, BT1120 data source from IO interface.
Step1: configure SYSTEM_CON0
Input_mode = 3'b010; sw_bt_data_oen = 1'b1.
Step2: configure RGB_DEC_CON
These configuration includes the input image information and other enable signals.
Step3: configure SCALER_CON
Need to configure some timing sequence based on the information of the input image.

15.6.4 RGB in

RGB data comes from IO interface.
Step1: configure SYSTEM_CON0
Input_mode = 3'b011; sw_bt_data_oen = 1'b1.

15.6.5 RGB out

RGB data outputs to IO interface.
Step1: configure SYSTEM_CON0
output_mode = 5'b10xxx; sw_bt_data_oen = 1'b0.

15.6.6 YUV encoder

When use YUV encoder mode, YUV data source from post process, and output to IO interface.
Step1: configure SYSTEM_CON0
output_mode = 5'b11xxx; sw_bt_data_oen = 1'b0.
Step2: configure RGB_ENC_CON0

15.6.7 YUV decoder

When use YUV decoder mode, YUV data source from IO interface.
Step1: configure SYSTEM_CON0
Input_mode = 3'b100; sw_bt_data_oen = 1'b1.
Step2: configure RGB_DEC_CON
These configuration include sw_yuv_yc_swap and sw_yuv_uv_swap.

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Chapter 16 GPIO

16.1 Overview

LVDS transmitter converts a CMOS signal into a low-voltage differential signal.
GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB bus width
- Up to 32 independently configurable signals
- Software control registers with write mask for each bit of each signal
- Configurable debounce logic with an slow clock to debounce interrupts
- Configurable interrupt mode

16.2 Block Diagram

GPIO comprises with:

- APB Interface: Implements the APB slave operation. Data bus width is 32 bits.
- I/O Port Interface: External data interface to or from I/O pads.
- Interrupt Detection: Interrupt interface to or from interrupt controller.

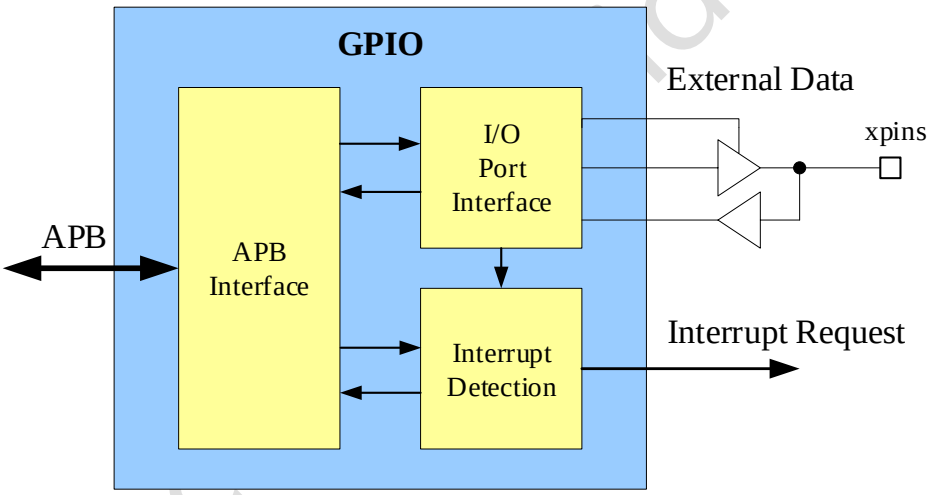

Fig. 16-1 GPIO Block Diagram

16.3 Function Description

16.3.1 Data Control

Under software control, the data and direction control for the signal are sourced from the port data registers (GPIO_SWPORT_DR_L/GPIO_SWPORT_DR_H) and direction control registers (GPIO_SWPORT_DDR_L/GPIO_SWPORT_DRR_H).
The direction of the external I/O pad is controlled by the value of the port data direction registers. The data written to these memory-mapped registers gets mapped onto an output signal (gpio_port_ddr) of the GPIO peripheral. This output signal controls the direction of an external I/O pad. The default data direction is Input.
The data written to the port data registers drives the output buffer (gpio_port_dr) of the I/O pad.
External data are input on the external data signal (gpio_ext_port). Reading the external signal register (GPIO_EXT_PORT) shows the value on this signal, regardless of the direction. This register is read-only, meaning that it cannot be written from the APB software interface.

16.3.2 Interrupts

I/O port can be programmed to accept external signals as interrupt sources on any of the

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bits of the signal. The type of interrupt is programmable with one of the following settings:
- Active-high and level
- Active-low and level
- Rising edge
- Falling edge
- Both the rising edge and the falling edge

The interrupts can be masked by programming the GPIO_INT_MASK_L/GPIO_INT_MASK_H registers. The interrupt status can be read before masking (GPIO_INT_RAWSTATUS) and after masking (GPIO_INT_STATUS).
For edge-sensitive interrupts, the Interrupt Service Routine (ISR) can clear the interrupt by writing a 1 to the corresponding bit of the GPIO_PORT_EOI_L/GPIO_PORT_EOI_H registers. This write also clears the interrupt status and raw status registers. Writing to the interrupt clear registers has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the interrupt raw status register until the interrupt source disappears, or it can write to the interrupt mask register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.
The interrupts are combined into a active-high interrupt output signal. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.
Whenever I/O port is configured for interrupts, the data direction must be set to Input. If the data direction is reprogrammed to Output, then any pending edge-sensitive interrupts are not lost. However, no new interrupts are generated, and level-sensitive interrupts are lost.
Interrupt signals are internally synchronized to a system clock pclk_intr, which is synchronous to the pclk. The pclk_intr needs to be running for interrupt detection even through the pclk is gated.

16.3.3 Debounce Operation

The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.
When an input interrupt signal is debounced using a slow debounce clock (external input clock dbclk or internal divided clock dbclk_div), the signal must be active for a minimum of two cycles of the debounce clock to guarantee that it is registered. Any input pulse widths less than a debounce clock period are bounced. A pulse width between one and two debounce clock widths may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans two rising edges of the debounce clock, it is registered. If it spans only one rising edge, it is not registered.
The debounce function can be controlled by programming the debounce enable registers (GPIO_DEBOUNCE_L/GPIO_DEBOUNCE_H), debounce clock divide enable registers (GPIO_DBCLK_DIV_EN_L/GPIO_DBCLK_DIV_EN_H) and debounce clock divide control register (GPIO_DBCLK_DIV_CON).

16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

16.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DR_L	0x0000	W	0x00000000	Port Data Register (Low)
GPIO_SWPORT_DR_H	0x0004	W	0x00000000	Port Data Register (High)
GPIO_SWPORT_DDR_L	0x0008	W	0x00000000	Port Data Direction Register (Low)

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Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DDR_H	0x000c	W	0x00000000	Port Data Direction Register (High)
GPIO_INT_EN_L	0x0010	W	0x00000000	Interrupt Enable Register (Low)
GPIO_INT_EN_H	0x0014	W	0x00000000	Interrupt Enable register (High)
GPIO_INT_MASK_L	0x0018	W	0x00000000	Interrupt Mask Register (Low)
GPIO_INT_MASK_H	0x001c	W	0x00000000	Interrupt Mask Register (High)
GPIO_INT_TYPE_L	0x0020	W	0x00000000	Interrupt Level Register (Low)
GPIO_INT_TYPE_H	0x0024	W	0x00000000	Interrupt Level Register (High)
GPIO_INT_POLARITY_L	0x0028	W	0x00000000	Interrupt Polarity Register (Low)
GPIO_INT_POLARITY_H	0x002c	W	0x00000000	Interrupt Polarity Register (High)
GPIO_INT_BOTHEDGE_L	0x0030	W	0x00000000	Interrupt Both Edge Type Register (Low)
GPIO_INT_BOTHEDGE_H	0x0034	W	0x00000000	Interrupt Both Edge Type Register (High)
GPIO_DEBOUNCE_L	0x0038	W	0x00000000	Debounce Enable Register (Low)
GPIO_DEBOUNCE_H	0x003c	W	0x00000000	Debounce Enable Register (High)
GPIO_DBCLK_DIV_EN_L	0x0040	W	0x00000000	DBCLK Divide Enable Register (Low)
GPIO_DBCLK_DIV_EN_H	0x0044	W	0x00000000	DBCLK Divide Enable Register (High)
GPIO_DBCLK_DIV_CON	0x0048	W	0x00000001	DBCLK Divide Control Register
GPIO_INT_STATUS	0x0050	W	0x00000000	Interrupt Status Register
GPIO_INT_RAWSTATUS	0x0058	W	0x00000000	Interrupt Raw Status Register
GPIO_PORT_EOI_L	0x0060	W	0x00000000	Interrupt Clear Register (Low)
GPIO_PORT_EOI_H	0x0064	W	0x00000000	Interrupt Clear Register (High)
GPIO_EXT_PORT	0x0070	W	0x00000000	External Port Data Register
GPIO_VER_ID	0x0078	W	0x01000c2b	Version ID Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

16.4.3 Detail Register Description

GPIO_SWPORT_DR_L

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_swport_dr_low Values written to this register are output on the I/O signals for the lower 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DR_H

Address: Operational Base + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_swport_dr_high Values written to this register are output on the I/O signals for the upper 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DDR_L

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_swport_ddr_low Values written to this register independently control the direction of the corresponding data bit in the lower 16 bits of I/O Port. 1'b0: Input (default) 1'b1: Output

GPIO_SWPORT_DDR_H

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_swport_ddr_high Values written to this register independently control the direction of the corresponding data bit in the upper 16 bits of I/O Port. 1'b0: Input (default) 1'b1: Output

GPIO_INT_EN_L

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_int_en_low Allows each bit of the lower 16 bits of I/O Port to be configured for interrupts. Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output. 1'b0: Configure I/O Port bit as normal GPIO signal (default) 1'b1: Configure I/O Port bit as interrupt

GPIO_INT_EN_H

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_en_high Allows each bit of the upper 16 bits of I/O Port to be configured for interrupts. Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output. 1'b0: Configure I/O Port bit as normal GPIO signal (default) 1'b1: Configure I/O Port bit as interrupt

GPIO_INT_MASK_L

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_mask_low Controls whether an interrupt on the lower 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. 1'b0: Interrupt is unmasked (default) 1'b1: Interrupt is masked

GPIO_INT_MASK_H

Address: Operational Base + offset (0x001c)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_mask_high Controls whether an interrupt on the upper 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. 1'b0: Interrupt is unmasked (default) 1'b1: Interrupt is masked

GPIO_INT_TYPE_L

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_type_low Controls the type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Level-sensitive (default) 1'b1: Edge-sensitive

GPIO_INT_TYPE_H

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_type_high Controls the type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Level-sensitive (default) 1'b1: Edge-sensitive

GPIO_INT_POLARITY_L

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_int_polarity_low Controls the polarity of edge or level sensitivity that can occur on the lower 16 bits of I/O Port. Whenever a 0 is written to a bit of this register, it configures the interrupt type to falling-edge or active-low sensitive; otherwise, it is rising-edge or active-high sensitive. 1'b0: Active-low (default) 1'b1: Active-high

GPIO_INT_POLARITY_H

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_polarity_high Controls the polarity of edge or level sensitivity that can occur on the upper 16 bits of I/O Port. Whenever a 0 is written to a bit of this register, it configures the interrupt type to falling-edge or active-low sensitive; otherwise, it is rising-edge or active-high sensitive. 1'b0: Active-low (default) 1'b1: Active-high

GPIO_INT_BOTHEDGE_L

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_bothedge_low Controls the edge type of interrupt that can occur on the lower 16 bits of I/O Port. Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers gpio_int_type and gpio_int_polarity for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the gpio_int_type and gpio_int_polarity registers. 1'b0: No both-edge detection (default) 1'b1: Enable both-edge detection

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GPIO_INT_BOTHEDGE_H

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_int_bothedge_high Controls the edge type of interrupt that can occur on the upper 16 bits of I/O Port. Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers gpio_int_type and gpio_int_polarity for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the gpio_int_type and gpio_int_polarity registers. 1'b0: No both-edge detection (default) 1'b1: Enable both-edge detection

GPIO_DEBOUNCE_L

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_debounce_low Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. 1'b0: No debounce (default) 1'b1: Enable debounce

GPIO_DEBOUNCE_H

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_debounce_high Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. 1'b0: No debounce (default) 1'b1: Enable debounce

GPIO_DBCLK_DIV_EN_L

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	gpio_dbclk_div_en_low Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the lower 16 bits of I/O Port. Whenever a 0 is written to a bit of this register, input clock dbclk is used as debounce clock; otherwise, the clock divided from dbclk is used. The clock divide factor depends on register gpio_dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of register gpio_debounce is set to 0. 1'b0: No divider for debounce clock (default) 1'b1: Enable divider for debounce clock

GPIO_DBCLK_DIV_EN_H

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio_dbclk_div_en_high Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the upper 16 bits of I/O Port. Whenever a 0 is written to a bit of this register, input clock dbclk is used as debounce clock; otherwise, the clock divided from dbclk is used. The clock divide factor depends on register gpio_dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of register gpio_debounce is set to 0. 1'b0: No divider for debounce clock (default) 1'b1: Enable divider for debounce clock

GPIO_DBCLK_DIV_CON

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000001	gpio_dbclk_div_con dbclk_div = dbclk / (gpio_dbclk_div_con + 1)

GPIO_INT_STATUS

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gpio_int_status Interrupt status of I/O Port

GPIO_INT_RAWSTATUS

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gpio_int_rawstatus Interrupt raw status of I/O Port (premasking bits)

GPIO_PORT_EOI_L

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	W1C	0x0000	gpio_port_eoi_low Controls the clearing of edge type interrupts from the lower 16 bits of I/O Port. When a 1 is written into a corresponding bit of this register, the interrupt is cleared. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts. 1'b0: No edge-sensitive interrupt clear (default) 1'b1: Clear edge-sensitive interrupt

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GPIO_PORT_EOI_H

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	W1C	0x0000	gpio_port_eoi_high Controls the clearing of edge type interrupts from the upper 16 bits of I/O Port. When a 1 is written into a corresponding bit of this register, the interrupt is cleared. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts. 1'b0: No edge-sensitive interrupt clear (default) 1'b1: Clear edge-sensitive interrupt

GPIO_EXT_PORT

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gpio_ext_port This register always reflects the value of the signals on the external I/O Port.

GPIO_VER_ID

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x01000c2b	gpio_ver_id Version ID

16.5 Interface Description

Table 16-1 GPIO Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
GPIO0 Interface			
gpio0_port[7:0]	I/O	GPIO0A[7:0]	GRF_GPIO0AB_IOMUX[7 :0]=8'h00
gpio0_port[11:8]	I/O	GPIO0B[3:0]	GRF_GPIO0AB_IOMUX[11:8]=4'h0
GPIO1 Interface			
gpio1_port[7:0]	I/O	GPIO1A[7:0]	GRF_GPIO1AB_IOMUX[7 :0]=8'h00
gpio1_port[13:8]	I/O	GPIO1B[5:0]	GRF_GPIO1AB_IOMUX[15:8]=8'h50
GPIO2 Interface			
gpio2_port[7:0]	I/O	GPIO2A[7:0]	GRF_GPIO2AB_IOMUX[7:0]=8'h00
gpio2_port[15:8]	I/O	GPIO2B[7:0]	GRF_GPIO2AB_IOMUX[15:8]=8'h00
gpio2_port[23:16]	I/O	GPIO2C[7:0]	GRF_GPIO2C_IOMUX [15:0]=16'haa80
GPIO3 Interface			
gpio3_port[7:0]	I/O	GPIO3A[7:0]	GRF_GPIO3AB_IOMUX[7:0]=8'h00
gpio3_port[12:8]	I/O	GPIO3B[4:0]	GRF_GPIO3AV_IOMUX[15:8]=8'h10

Notes: Unused Module Pin is tied to zero! I=input, O=output, I/O=input/output, bidirectional

16.6 Application Notes

- In RK628D those unused GPIO bits are tied to zero
  Reading from an unused location or unused bits in a particular register always returns

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zeros. There is no error mechanism in the APB.

a. GPIO0_PORT[31:12]
b. GPIO1_PORT[31:14]
c. GPIO2_PORT[31:24]
d. GPIO3_PORT[31:13]

Programming the GPIO registers for interrupt detection should be completed prior to enabling the interrupts in order to prevent spurious glitches on the interrupt output signal to the interrupt controller.

- In RK628D those GPIO are used special function

a. IO_GPIO0a1,IO_GPIO0a0,IO_GPIO3b3 are tied to input,used as the i2c_slv address bits.They are satisfied with the following relationships:

I2C_SLV_ADDR={IO_GPIO0a1,IO_GPIO0a0,IO_GPIO3b3}

b. IO_GPIO3a2 is tied to 1

when it ties to high ,it means the chip just work on I2C mode.

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