Quiz 5

Due Jan 31 at 11:59pm **Points** 21 **Questions** 10 **Available** Jan 19 at 12am - Feb 2 at 11:59pm **Time Limit** None

Instructions

Read Sections 5.1-5.4 then answer the following questions. One try. No time limit.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	33 minutes	21 out of 21

Score for this quiz: **21** out of 21
Submitted Jan 29 at 8:43pm
This attempt took 33 minutes.

Question 1

4 / 4 pts

Indicate the addressing mode used by the following instructions:

Note: the text does not address "implicit" addressing mode and presumably lumps it in with register addressing mode. The difference between the implicit and register addressing modes is that for register addressing mode, the register number (e.g. R1) is encoded in the machine code of the instruction itself, whereas for implicit addressing mode, the operand (which may or may not be a register) is implied by the instruction itself. For example the 8051 has an instruction MUL AB (which we shall learn about shortly). Even though A and B are both registers, the is no register number encoded in the instruction, so this would be an example of implicit addressing mode.

Correct! **CPL A** — Implicit

Correct! **PUSH P1** — Direct

Correct! **INC @R1** — Register Indirect

Correct! **DEC R2** — Register

Other Incorrect Match Options:
- Indexed
- Immediate

Question 2

3 / 3 pts

Give the RAM address assigned to the following registers. Give your answers in hexadecimal. Do not add leading zeros or the 'H' suffix.

R6 of register bank 1: E

R3 of register bank 2: 13

R4 of register bank 3: 1C

Answer 1:

Correct! E

Correct Answer 0E

Answer 2:

Correct! 13

Answer 3:

Correct! 1C

Question 3

1 / 1 pts

R3 may be used for register indirect addressing mode.

- True
- Correct! False

Question 4

3 / 3 pts

Which of the following SFRs are bit addressable (select all that apply):

- Correct! PSW
- TMOD
- Correct! IE
- Correct! B
- Correct! ACC
- TL0
- PCON
- DPH
- Correct! TCON
- SBUF
- Correct! SCON
- SP

Question 5

2 / 2 pts

Data RAM addresses in the range 20 to 2F are bit addressable. Give your answers in hexadecimal without leading zeros or the 'H' suffix.

Answer 1:

Correct! 20

Answer 2:

Correct! 2F

Question 6

3 / 3 pts

Indicate the bit address that is altered by the following instructions. Give your answers in hexadecimal without leading zeros or the 'H" suffix.

CLR P2.1 A1

SETB ACC.6 E6

CPL OV D2

Note: OV is one of the bits in the PSW.

Answer 1:

Correct! A1

Answer 2:

Correct! E6

Answer 3:

Correct! D2

Question 7

2 / 2 pts

Give the names of the bits that have the (bit) addresses, below.

Bit 0D6H is called AC

Bit 0D0H is called P

Answer 1:

Correct! AC

Answer 2:

Correct! P

Question 8

1 / 1 pts

The bit addresses assigned to register B are (lowest to highest) F0 to F7 . Give your answers in hexadecimal without leading zeros or the 'H' suffix.

Answer 1:

Correct! F0

Answer 2:

Correct! F7

Question 9

1 / 1 pts

What addressing mode used to access the upper 128 bytes of RAM in the 8052?

- Direct
- Immediate
- Indexed
- Register

Correct! Register Indirect

Question 10

1 / 1 pts

On an 8052, the stack can be placed in the upper RAM.

Correct! True

- False

Quiz Score: **21** out of 21