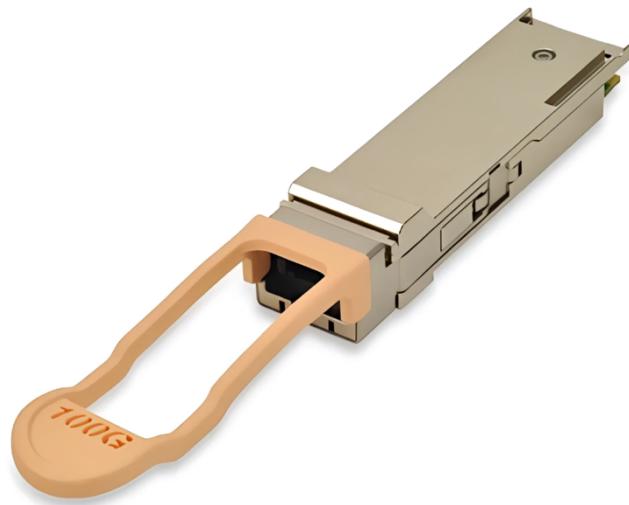


Overview

The Wave2Wave 77-Z010L4 is a hot-pluggable 100G QSFP28 LR4 optical transceiver engineered for long-reach links up to 10 km over single-mode fiber. It delivers four 25.78125 Gbps lanes using cooled LAN-WDM optics that ensure wavelength stability and consistent optical performance.

The module integrates an EEPROM that supports real-time monitoring, diagnostics, and configuration through a standard two-wire QSFP management interface. Designed for modern high-density networks, it provides reliable, high-speed connectivity for data center, enterprise, and carrier applications.



Features and Benefits

- Hot-pluggable QSFP28 MSA package with duplex LC receptacle
- 4x25G lanes supporting 25.78125 Gbps each, up to 10 km over SMF
- 4x25G retimed electrical interface for enhanced signal integrity
- I²C 2-wire interface for Digital Diagnostics and monitoring
- Single +3.3V power supply, consuming <4 W
- Operating case temperature range: 0°C to +70°C

Applications

- Data center interconnects
- 100GBASE-LR4 Ethernet links
- InfiniBand DDR, QDR, and EDR environments

Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T _s	-40	85	°C
Relative Humidity	R _h	5	85	%
Supply Voltage	V _{cc3}	-0.5	3.6	V
Receiver Damage Threshold, per Lane	P _T		5.5	dBm

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T _c	0	25	70	°C
Power Supply Voltage	V _{cc3}	3.135	3.3	3.465	V
	I _{cc3}			1.21	A
Power Dissipation	P _D			4	W
Data Rate (NRZ) per Lane			25.78125		Gbps
Data Rate (NRZ) Total			103.125		Gbps
Transmission Distance				10	km

Optical Characteristics (Transmitter)						
Parameter		Symbol	Min	Typical	Max	Unit
Centre Wavelengths, each Lane	CH0	λ_0	1294.53	1295.53	1296.59	nm
	CH1	λ_1	1299.02	1300.05	1301.09	nm
	CH2	λ_2	1303.54	1304.58	1305.63	nm
	CH3	λ_3	1308.09	1309.14	1310.19	nm
Side-Mode Suppression Ratio	SMSR		30			dB
Laser Off Power	Poff				-30	dBm
Transmit OMA, per Lane	OMA		-1.3		4.5	dBm
Extinction Ratio	ER		3.5			dB
Difference in Power Between Any Two Lanes	Ptx, diff				5	dB
Relative Intensity Noise	Rin				-128	dB/Hz
Optical Return Loss Tolerance					20	dB
Average Launch Power per Lane	Pavg		-4.3		4.5	dBm
Total Average Launch Power	PT				10.5	dBm
Average Launch Power of OFF Transmitter, per lane	Poff				-30	dBm
Transmitter and Dispersion Penalty per Lane					2.3	dB
Transmitter Reflectance	Rr				-12	dB
Operating Data Rate, per Lane				25.78125		Gbps
Operating Date Rate, Total				103.125		Gbps
Optical Eye Mask Margin				>5%		
Transmitter Eye Mask Definition (X1, X2, X3, Y1, Y2, Y3)				(0.31, 0.4, 0.45, 0.34, 0.38, 0.4)		

Optical Characteristics (Receiver)						
Parameter		Symbol	Min	Typical	Max	Unit
Centre Wavelengths, each Lane	CH0	λ_0	1294.53	1295.53	1296.59	nm
	CH1	λ_1	1299.02	1300.05	1301.09	nm
	CH2	λ_2	1303.54	1304.58	1305.63	nm
	CH3	λ_3	1308.09	1309.14	1310.19	nm
Damage Threshold per Lane	THd		5.5			dBm
Average Receive Power, each Lane			-10.6		4.5	dBm
Difference in Receive Power Between Any Two Lanes (OMA)	Prx, diff				5.5	dB
Receive Sensitivity (OMA), each Lane	SEN				-8.6	dBm
Stressed Receive Sensitivity (OMA), each Lane ¹					-6.8	dBm
LOS Assert	LosA		-30			dBm
LOS De-Assert	LosD				-15	dBm
LOS Hysteresis	LosH		0.5			dB
Overload (OMA)	Pin		4.5			dBm
Receiver Reflectance					-26	dB
Operating Data Rate, per Lane				25.78125		Gbps
Operating Data Rate, Total				103.125		Gbps
Receiver Electrical 3 dB Upper Cutoff Frequency, each lane	Fc				31	Gbps

NOTES:

1. Measured with 25.78125Gb/s, PRBS31 NRZ, BER=1E-12

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input Differential Impedance			100		Ω
Differential Data Input Swing		300		900	mV
Differential Data Output Swing		400		900	mV

Control and Status I/O Timing

Parameter	Symbol	Min	Typical	Max	Unit
Initialization Time	t_init			2000	ms
Reset Init Assert Time	t_reset_init			2	us
Serial Bus Hardware Ready Time	t_serial			2000	ms
Reset Asset Time	t_reset			2000	ms
LPMode Assert Time	ton_LPMode			100	us
LPMode De-Assert Time	toff_LPMode			300	ms
IntL Assert Time	ton_IntL			200	ms
IntL De-Assert Time	toff_IntL			500	us
Rx LOS Asset Time	ton_los			100	ms
Tx Fault Assert Time	ton_Txfault			200	ms
Flag Assert Time	ton_flag			200	ms
Mask Assert Time	ton_mask			100	ms
Mask De-Assert Time	ton_mask			100	ms
Power_override or Power_set Assert Time	ton_Pdown			100	ms
Power_override or Power_set De-Assert Time	toff_Pdown			300	ms

Pin-Out Definition

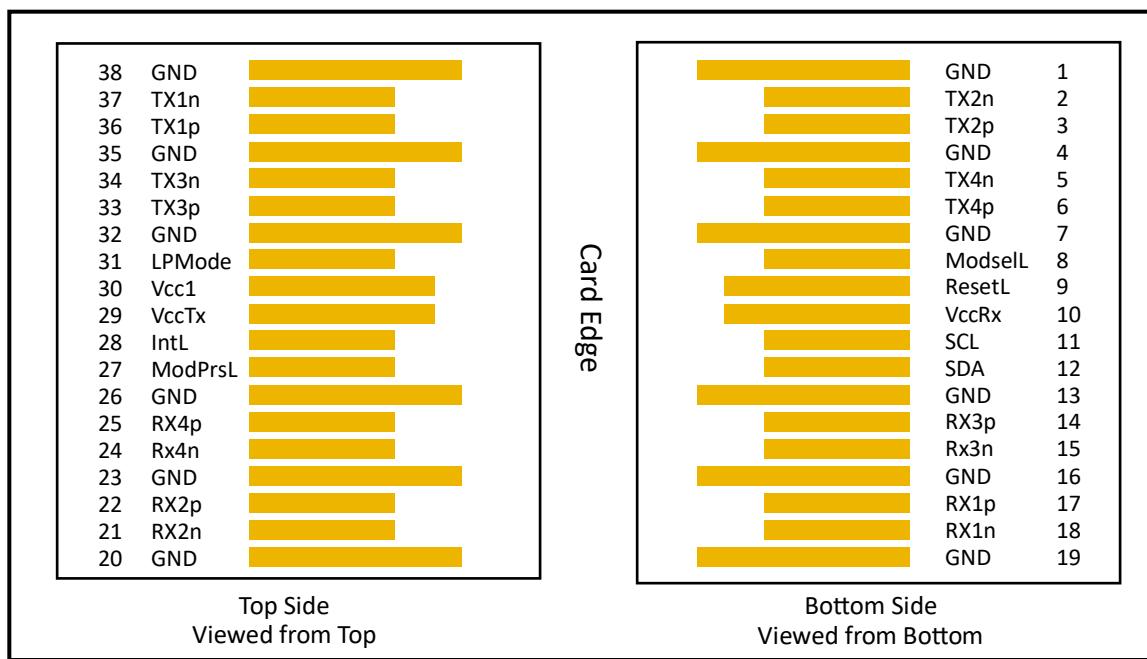


Figure 1. Pin Map

Pin Description			
Pin	Name	Description	Notes
1	GND	Module Ground	Note 1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Module Ground	Note 1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Module Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3V Power Supply Receiver	Note 2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Module Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Module Ground	Note 1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	Note 1
19	GND	Module Ground	Note 1
20	GND	Module Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Module Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Module Ground	Note 1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power Supply Transmitter	Note 2
30	Vcc1	+3.3V Power Supply	Note 2
31	LPMode	Low Power Mode	
32	GND	Module Ground	Note 1
33	Tx3p	Transmitter Non-Inverted Data Output	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Module Ground	Note 1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Module Ground	Note 1

NOTES:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All the common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 7. Vcc Rx Vcc1 and VccTx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Standards Compliance

- IEEE 802.3ba 100GBASE-LR4
- IEEE 802.3bm
- QSFP28 MSA
- SFF-8636
- RoHS

