Table of Contents	
01	TITLE PAGE
02	BLOCK DIAGRAM
03	SOC_PORT0~2
04	SOC_PORT3~5
05	SOC_PWR
06	USB & PWR
07	SD & QSPI & SENSOR
08	CAN PHY & ETHERNET PHY
09	MCU_LINK_USB
10	MCU_LINK_DEBUG
11	SWITCH & LED
12	HEADERS
13	APPENDIX JUMPER/DNP

Revision History

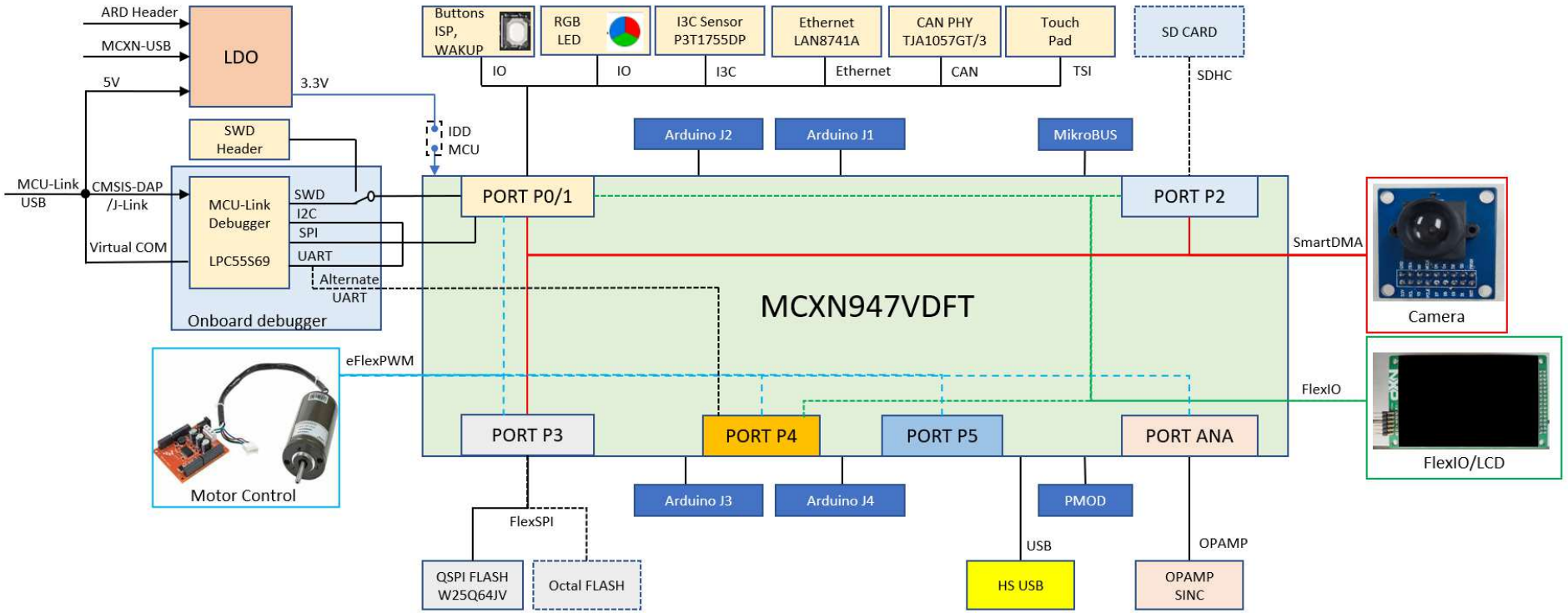
REV	REVISION NOTES	Date
X1	Initial	Jun 10, 2023
A	Final Release	Jul 10, 2023
B	1.Change 3pin solder pads. 2.Update schematic per Ver.A test result.	Sep 15, 2023
B1	1.DNP J12&J7. 2.Change J10 MPN.	Nov 13, 2023
B2	1.Change C21 from 1uf to 4.7uf. 2.Change C24 from 0.1uf to 2.2uf. 3.Change R82&R192&R193 MPN due to material shortage.	Jan 25, 2024

FRDM-MCXN947

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

Designer: John Wu	Drawing Title: FRDM-MCXN947	
Drawn by: Kate Fan	Page Title: TITLE PAGE	
Approved: William Jiang	Size C	Document Number SCH-90818 PDF: SPF-90818 — Rev B2
	Date: Thursday, January 25, 2024	Sheet 1 of 1

BLOCK DIAGRAM



Classification: Company Internal/Proprietary

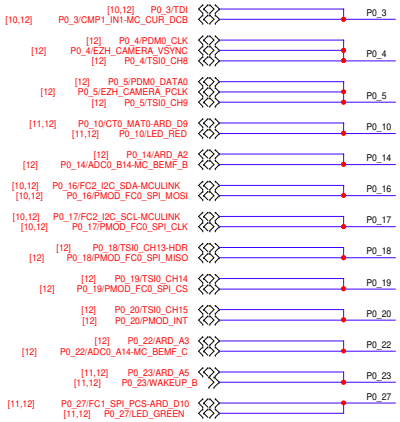
Drawing Title: **FRDM-MCXN947**

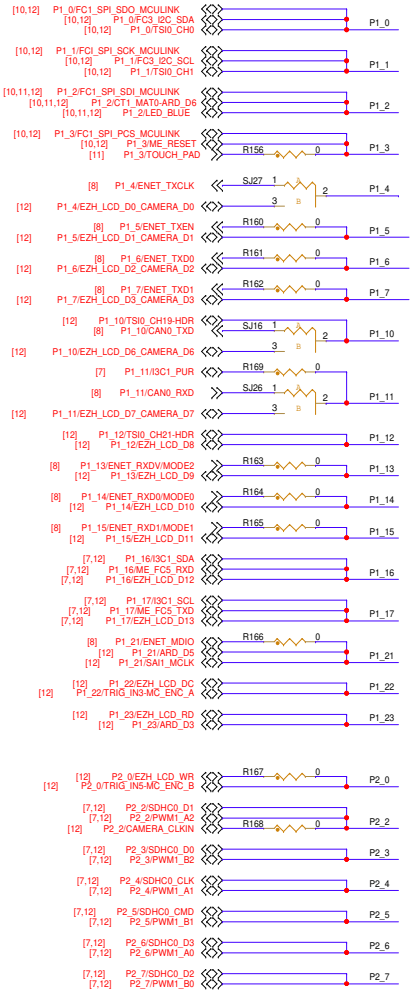
Page Title: **BLOCK DIAGRAM**

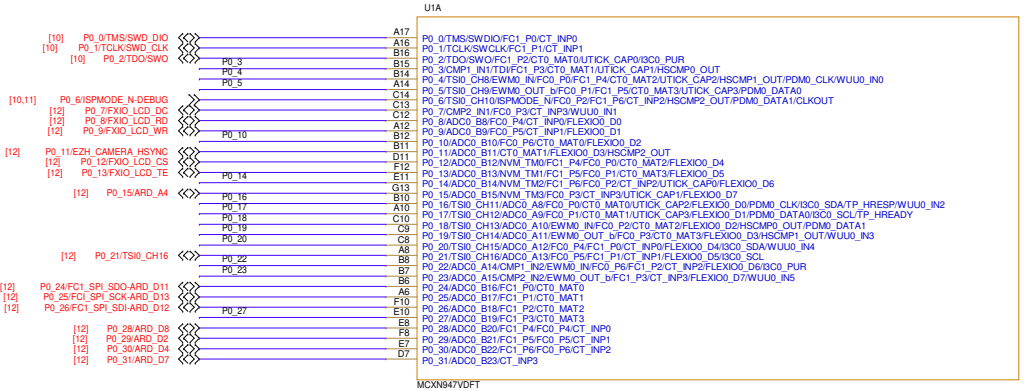
Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

Date: Thursday, January 25, 2024 | Sheet 2 of 13

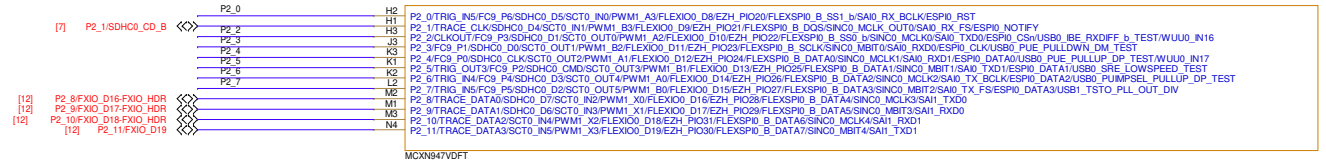
SOC PORT0~2

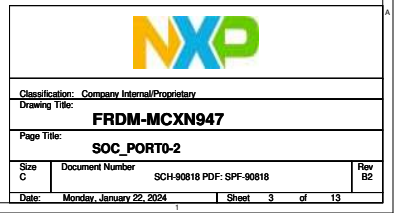

[10,12] P0_3/TDI
[10,12] P0_3/CMP1_IN1-MC_CUR_DCB
P0_3
[12] P0_4/PDM0_CLK
[12] P0_4/EZH_CAMERA_VSYNC
[12] P0_4/TSI0_CH8
P0_4
[12] P0_5/PDM0_DATA0
[12] P0_5/EZH_CAMERA_PCLK
[12] P0_5/TSI0_CH9
P0_5
[11,12] P0_10/CT0_MAT0-ARD_D9
[11,12] P0_10/LED_RED
P0_10
[12] P0_14/ARD_A2
[12] P0_14/ADC0_B14-MC_BEMF_B
P0_14
[10,12] P0_16/FC2_I2C_SDA-MCULINK
[10,12] P0_16/PMOD_FC0_SPI_MOSI
P0_16
[10,12] P0_17/FC2_I2C_SCL-MCULINK
[10,12] P0_17/PMOD_FC0_SPI_CLK
P0_17
[12] P0_18/TSI0_CH13-HDR
[12] P0_18/PMOD_FC0_SPI_MISO
P0_18
[12] P0_19/TSI0_CH14
[12] P0_19/PMOD_FC0_SPI_CS
P0_19
[12] P0_20/TSI0_CH15
[12] P0_20/PMOD_INT
P0_20
[12] P0_22/ARD_A3
[12] P0_22/ADC0_A14-MC_BEMF_C
P0_22
[11,12] P0_23/ARD_A5
[11,12] P0_23/WAKEUP_B
P0_23
P0_27
[11,12] P0_27/FC1_SPI_PCS-ARD_D10
[11,12] P0_27/LED_GREEN


[10,12] P1_0/FC1_SPI_SDO_MCULINK
[10,12] P1_0/FC3_I2C_SDA
[10,12] P1_0/TSI0_CH0
P1_0
[10,12] P1_1/FC1_SPI_SCK_MCULINK
[10,12] P1_1/FC3_I2C_SCL
[10,12] P1_1/TSI0_CH1
P1_1
[10,11,12] P1_2/FC1_SPI_SDI_MCULINK
[10,11,12] P1_2/CT1_MAT0-ARD_D6
[10,11,12] P1_2/LED_BLUE
P1_2
[10,12] P1_3/FC1_SPI_PCS_MCULINK
[10,12] P1_3/ME_RESET
[11] P1_3/TOUCH_PAD
R156 0
P1_3
[8] P1_4/ENET_TXCLK
SJ27 1 2 3
[12] P1_4/EZH_LCD_D0_CAMERA_D0
P1_4
[8] P1_5/ENET_TXEN
R160 0
[12] P1_5/EZH_LCD_D1_CAMERA_D1
P1_5
[8] P1_6/ENET_TXD0
R161 0
[12] P1_6/EZH_LCD_D2_CAMERA_D2
P1_6
[8] P1_7/ENET_TXD1
R162 0
[12] P1_7/EZH_LCD_D3_CAMERA_D3
P1_7
[12] P1_10/TSI0_CH19-HDR
[8] P1_10/CAN0_TXD
SJ16 1 2 3
[12] P1_10/EZH_LCD_D6_CAMERA_D6
P1_10
[7] P1_11/I3C1_PUR
R169 0
[8] P1_11/CAN0_RXD
SJ26 1 2 3
[12] P1_11/EZH_LCD_D7_CAMERA_D7
P1_11
[12] P1_12/TSI0_CH21-HDR
[12] P1_12/EZH_LCD_D8
P1_12
[8] P1_13/ENET_RXDV/MODE2
R163 0
[12] P1_13/EZH_LCD_D9
P1_13
[8] P1_14/ENET_RXD0/MODE0
R164 0
[12] P1_14/EZH_LCD_D10
P1_14
[8] P1_15/ENET_RXD1/MODE1
R165 0
[12] P1_15/EZH_LCD_D11
P1_15
[7,12] P1_16/I3C1_SDA
[7,12] P1_16/ME_FC5_RXD
[7,12] P1_16/EZH_LCD_D12
P1_16
[7,12] P1_17/I3C1_SCL
[7,12] P1_17/ME_FC5_TXD
[7,12] P1_17/EZH_LCD_D13
P1_17
[8] P1_21/ENET_MDIO
R166 0
[12] P1_21/ARD_D5
[12] P1_21/SAI1_MCLK
P1_21
[12] P1_22/EZH_LCD_DC
[12] P1_22/TRIG_IN3-MC_ENC_A
P1_22
[12] P1_23/EZH_LCD_RD
[12] P1_23/ARD_D3
P1_23
[12] P2_0/EZH_LCD_WR
[12] P2_0/TRIG_IN5-MC_ENC_B
R167 0
P2_0
[7,12] P2_2/SDHC0_D1
[7,12] P2_2/PWM1_A2
[12] P2_2/CAMERA_CLKIN
R168 0
P2_2
[7,12] P2_3/SDHC0_D0
[7,12] P2_3/PWM1_B2
P2_3
[7,12] P2_4/SDHC0_CLK
[7,12] P2_4/PWM1_A1
P2_4
[7,12] P2_5/SDHC0_CMD
[7,12] P2_5/PWM1_B1
P2_5
[7,12] P2_6/SDHC0_D3
[7,12] P2_6/PWM1_A0
P2_6
[7,12] P2_7/SDHC0_D2
[7,12] P2_7/PWM1_B0
P2_7


U1A
[10] P0_0/TMS/SWD_DIO
[10] P0_1/TCLK/SWD_CLK
[10] P0_2/TDO/SWO
P0_3
P0_4
P0_5
[10,11] P0_6/ISPMODE_N-DEBUG
[12] P0_7/FXIO_LCD_DC
[12] P0_8/FXIO_LCD_RD
[12] P0_9/FXIO_LCD_WR
P0_10
[12] P0_11/EZH_CAMERA_HSYNC
[12] P0_12/FXIO_LCD_CS
[12] P0_13/FXIO_LCD_TE
P0_14
[12] P0_15/ARD_A4
P0_16
P0_17
P0_18
P0_19
P0_20
[12] P0_21/TSI0_CH16
P0_22
P0_23
[12] P0_24/FC1_SPI_SDO-ARD_D11
[12] P0_25/FC1_SPI_SCK-ARD_D13
[12] P0_26/FC1_SPI_SDI-ARD_D12
P0_27
[12] P0_28/ARD_D8
[12] P0_29/ARD_D2
[12] P0_30/ARD_D4
[12] P0_31/ARD_D7
A17 A16 B16 B15 B14 A14 C14 C13 C12 A12 B12 B11 D11 F12 E11 G13 B10 A10 C10 C9 C8 A8 B8 B7 B6 A6 F10 E10 E8 F8 E7 D7
P0_0/TMS/SWDIO/FC1_P0/CT_INP0
P0_1/TCLK/SWCLK/FC1_P1/CT_INP1
P0_2/TDO/SWO/FC1_P2/CT0_MAT0/UTICK_CAP0/I3C0_PUR
P0_3/CMP1_IN1/TDI/FC1_P3/CT0_MAT1/UTICK_CAP1/HSCMP0_OUT
P0_4/TSI0_CH8/EWM0_IN/FC0_P0/FC1_P4/CT0_MAT2/UTICK_CAP2/HSCMP1_OUT/PDM0_CLK/WUU0_IN0
P0_5/TSI0_CH9/EWM0_OUT_b/FC0_P1/FC1_P5/CT0_MAT3/UTICK_CAP3/PDM0_DATA0
P0_6/TSI0_CH10/ISPMODE_N/FC0_P2/FC1_P6/CT_INP2/HSCMP2_OUT/PDM0_DATA1/CLKOUT
P0_7/CMP2_IN1/FC0_P3/CT_INP3/WUU0_IN1
P0_8/ADC0_B8/FC0_P4/CT_INP0/FLEXIO0_D0
P0_9/ADC0_B9/FC0_P5/CT_INP1/FLEXIO0_D1
P0_10/ADC0_B10/FC0_P6/CT0_MAT0/FLEXIO0_D2
P0_11/ADC0_B11/CT0_MAT1/FLEXIO0_D3/HSCMP2_OUT
P0_12/ADC0_B12/NVM_TM0/FC1_P4/FC0_P0/CT0_MAT2/FLEXIO0_D4
P0_13/ADC0_B13/NVM_TM1/FC1_P5/FC0_P1/CT0_MAT3/FLEXIO0_D5
P0_14/ADC0_B14/NVM_TM2/FC1_P6/FC0_P2/CT_INP2/UTICK_CAP0/FLEXIO0_D6
P0_15/ADC0_B15/NVM_TM3/FC0_P3/CT_INP3/UTICK_CAP1/FLEXIO0_D7
P0_16/TSI0_CH11/ADC0_A8/FC0_P0/CT0_MAT0/UTICK_CAP2/FLEXIO0_D0/PDM0_CLK/I3C0_SDA/TP_HRESP/WUU0_IN2
P0_17/TSI0_CH12/ADC0_A9/FC0_P1/CT0_MAT1/UTICK_CAP3/FLEXIO0_D1/PDM0_DATA0/I3C0_SCL/TP_HREADY
P0_18/TSI0_CH13/ADC0_A10/EWM0_IN/FC0_P2/CT0_MAT2/FLEXIO0_D2/HSCMP0_OUT/PDM0_DATA1
P0_19/TSI0_CH14/ADC0_A11/EWM0_OUT_b/FC0_P3/CT0_MAT3/FLEXIO0_D3/HSCMP1_OUT/WUU0_IN3
P0_20/TSI0_CH15/ADC0_A12/FC0_P4/FC1_P0/CT_INP0/FLEXIO0_D4/I3C0_SDA/WUU0_IN4
P0_21/TSI0_CH16/ADC0_A13/FC0_P5/FC1_P1/CT_INP1/FLEXIO0_D5/I3C0_SCL
P0_22/ADC0_A14/CMP1_IN2/EWM0_IN/FC0_P6/FC1_P2/CT_INP2/FLEXIO0_D6/I3C0_PUR
P0_23/ADC0_A15/CMP2_IN2/EWM0_OUT_b/FC1_P3/CT_INP3/FLEXIO0_D7/WUU0_IN5
P0_24/ADC0_B16/FC1_P0/CT0_MAT0
P0_25/ADC0_B17/FC1_P1/CT0_MAT1
P0_26/ADC0_B18/FC1_P2/CT0_MAT2
P0_27/ADC0_B19/FC1_P3/CT0_MAT3
P0_28/ADC0_B20/FC1_P4/FC0_P4/CT_INP0
P0_29/ADC0_B21/FC1_P5/FC0_P5/CT_INP1
P0_30/ADC0_B22/FC1_P6/FC0_P6/CT_INP2
P0_31/ADC0_B23/CT_INP3
MCXN947VDFT


U1B
P1_0 P1_1 P1_2 P1_3 P1_4 P1_5 P1_6 P1_7
FC4_P0_UART_RXD
FC4_P1_UART_TXD
P1_10 P1_11 P1_12 P1_13 P1_14 P1_15 P1_16 P1_17
XTAL
C6 C5 C4 B4 A4 B3 B2 A2 A1 B1 C3 D3 D2 D1 E4 F6 F4 G4 G5 K5 L5 L4 M4 F1 F2
P1_0/TSI0_CH0/ADC0_A16/CMP0_IN0/TRIG_IN0/FC3_P0/FC4_P4/CT_INP4/SCT0_OUT6/FLEXIO0_D8/SAI1_TX_BCLK/WUU0_IN6/LPTMR0_ALT3
P1_1/TSI0_CH1/ADC0_A17/CMP1_IN0/TRIG_IN1/FC3_P1/FC4_P5/CT_INP5/SCT0_OUT7/FLEXIO0_D9/SAI1_TX_FS/NVM_SDO
P1_2/TSI0_CH2/ADC0_A18/CMP2_IN0/TRIG_OUT0/FC3_P2/FC4_P6/CT1_MAT0/SCT0_IN6/FLEXIO0_D10/ENET0_MDC/SAI1_TXD0/CAN0_TXD/USB0_OBE_TXDATA_b_TEST/ADC1_CONV_CLK
P1_3/TSI0_CH3/ADC0_A19/CMP0_IN1/TRIG_OUT1/FC3_P3/CT1_MAT1/SCT0_IN7/FLEXIO0_D11/ENET0_MDIO/SAI1_RXD0/CAN0_RXD/TP_HTRANS/WUU0_IN7
P1_4/TSI0_CH4/ADC0_A20/CMP0_IN2/FREQME_CLK_IN0/FC3_P4/FC5_P0/CT1_MAT2/SCT0_OUT0/FLEXIO0_D12/EZH_PIO0/ENET0_TX_CLK/SAI0_TXD1/USB0_IND_RXDM_TEST/ADC1_CONV_DATA0/WUU0_IN8
P1_5/TSI0_CH5/ADC0_A21/CMP0_IN3/FREQME_CLK_IN1/FC3_P5/FC5_P1/CT1_MAT3/SCT0_OUT1/FLEXIO0_D13/EZH_PIO1/ENET0_TXEN/SAI0_RXD1/USB0_IND_RXDP_TEST/ADC1_CONV_DATA1
P1_6/TSI0_CH6/ADC0_A22/TRIG_IN2/FC3_P6/FC5_P2/CT_INP6/SCT0_IN0/FLEXIO0_D14/EZH_PIO2/ENET0_TXD0/SAI1_RX_BCLK/CAN1_TXD/USB0_IND_RXDIFF_TEST/ADC1_CONV_DATA2
P1_7/TSI0_CH7/ADC0_A23/TRIG_OUT2/FC5_P3/CT_INP7/SCT0_IN1/FLEXIO0_D15/EZH_PIO3/PLU_CLK/ENET0_TXD1/SAI1_RX_FS/CAN1_RXD/USB0_DO_TXDATA_TEST/ADC1_CONV_DATA3/WUU0_IN9
P1_8/TSI0_CH17/ADC1_A8/TRACE_DATA0/FC4_P0/FC5_P4/CT_INP8/SCT0_OUT2/FLEXIO0_D16/EZH_PIO4/PLU_OUT0/ENET0_TXD2/I3C1_SDA/TP_DATA0/WUU0_IN10/LPTMR1_ALT3
P1_9/TSI0_CH18/ADC1_A9/TRACE_DATA1/FC4_P1/FC5_P5/CT_INP9/SCT0_OUT3/FLEXIO0_D17/EZH_PIO5/PLU_OUT1/ENET0_TXD3/I3C1_SCL/TP_DATA1
P1_10/TSI0_CH19/ADC1_A10/TRACE_DATA2/FC4_P2/FC5_P6/CT2_MAT0/SCT0_IN2/FLEXIO0_D18/EZH_PIO6/PLU_IN0/ENET0_TXER/CAN0_TXD/TP_DATA2
P1_11/TSI0_CH20/ADC1_A11/TRACE_DATA3/FC4_P3/CT2_MAT1/SCT0_IN3/FLEXIO0_D19/EZH_PIO7/PLU_IN1/ENET0_RX_CLK/I3C1_PUR/CAN0_RXD/TP_DATA3/WUU0_IN11
P1_12/TSI0_CH21/ADC1_A12/TRACE_CLK/FC4_P4/FC3_P0/CT2_MAT2/SCT0_OUT4/FLEXIO0_D20/EZH_PIO8/PLU_OUT2/ENET0_RXER/CAN1_RXD/USB0_PUE_PULLDWN_DP_TEST/ADC1_CONV_DATA4/WUU0_IN12
P1_13/TSI0_CH22/ADC1_A13/TRIG_IN3/FC4_P5/FC3_P1/CT2_MAT3/SCT0_OUT5/FLEXIO0_D21/EZH_PIO9/PLU_OUT3/ENET0_RXDV/CAN1_TXD/USB0_OBE_TXBIAS_b_TEST/ADC1_CONV_DATA5
P1_14/TSI0_CH23/ADC1_A14/FC4_P6/FC3_P2/CT_INP10/SCT0_IN4/FLEXIO0_D22/EZH_PIO10/PLU_IN2/ENET0_RXD0/USB0_DO_TXSZERO_TEST/ADC1_CONV_DATA6
P1_15/TSI0_CH24/ADC1_A15/FC3_P3/CT_INP11/SCT0_IN5/FLEXIO0_D23/EZH_PIO11/PLU_IN3/ENET0_RXD1/I3C1_PUR/USB0_SRE_LOWSPEED_TEST/ADC1_CONV_DATA7/WUU0_IN13
P1_16/ADC1_A16/FC5_P0/FC3_P4/CT_INP12/SCT0_OUT6/FLEXIO0_D24/EZH_PIO12/PLU_OUT4/ENET0_RXD2/I3C1_SDA/WUU0_IN14
P1_17/ADC1_A17/FC5_P1/FC3_P5/CT_INP13/SCT0_OUT7/FLEXIO0_D25/EZH_PIO13/PLU_OUT5/ENET0_RXD3/I3C1_SCL
P1_18/ADC1_A18/FREQME_CLK_IN0/FC5_P2/FC3_P6/CT3_MAT0/SCT0_IN6/FLEXIO0_D26/EZH_PIO14/PLU_IN4/ENET0_COL/CAN0_TXD
P1_19/ADC1_A19/FREQME_CLK_IN1/FC5_P3/CT3_MAT1/SCT0_IN7/FLEXIO0_D27/EZH_PIO15/PLU_IN5/ENET0_CRS/CAN0_RXD/WUU0_IN15
P1_20/ADC1_A20/CMP1_IN3/TRIG_IN2/FC5_P4/FC4_P0/CT3_MAT2/SCT0_OUT8/FLEXIO0_D28/EZH_PIO16/PLU_OUT6/ENET0_MDC/CAN1_TXD
P1_21/ADC1_A21/CMP2_IN3/TRIG_OUT2/FC5_P5/FC4_P1/CT3_MAT3/SCT0_OUT9/FLEXIO0_D29/EZH_PIO17/PLU_OUT7/ENET0_MDIO/SAI1_MCLK/CAN1_RXD
P1_22/ADC1_A22/TRIG_IN3/FC5_P6/FC4_P2/CT_INP14/SCT0_OUT4/FLEXIO0_D30/EZH_PIO18
P1_23/ADC1_A23/FC4_P3/CT_INP15/SCT0_OUT5/FLEXIO0_D31/EZH_PIO19
P1_30/XTAL48M/TRIG_OUT3/CT_INP16/SCT0_OUT8/SAI0_MCLK
P1_31/EXTAL48M/TRIG_IN4/CT_INP17/SCT0_OUT9
MCXN947VDFT
[12] P1_8/FC4_P0_UART_RXD_MCULINK
[10,12] P1_9/FC4_P1_UART_TXD_MCULINK
[12] P1_18/EZH_LCD_D14_CAMERA_PDOWN
[12] P1_19/EZH_LCD_D15_CAMERA_RST
[8] P1_20/ENET_MDC
Y1 830108212309
24MHz
EXTAL
C1 4.7pF
C2 4.7pF


U1C
P2_0 P2_2 P2_3 P2_4 P2_5 P2_6 P2_7
H2 H1 H3 J3 K3 K1 K2 L2 M2 M1 M3 N4
P2_0/TRIG_IN5/FC9_P6/SDHC0_D5/SCT0_IN0/PWM1_A3/FLEXIO0_D8/EZH_PIO20/FLEXSPI0_B_SS1_b/SAI0_RX_BCLK/ESPI0_RST
P2_1/TRACE_CLK/SDHC0_D4/SCT0_IN1/PWM1_B3/FLEXIO0_D9/EZH_PIO21/FLEXSPI0_B_DQS/SINC0_MCLK_OUT0/SAI0_RX_FS/ESPI0_NOTIFY
P2_2/CLKOUT/FC9_P3/SDHC0_D1/SCT0_OUT0/PWM1_A2/FLEXIO0_D10/EZH_PIO22/FLEXSPI0_B_SS0_b/SINC0_MCLK0/SAI0_TXD0/ESPI0_CS#/USB0_IBE_RXDIFF_b_TEST/WUU0_IN16
P2_3/FC9_P1/SDHC0_D0/SCT0_OUT1/PWM1_B2/FLEXIO0_D11/EZH_PIO23/FLEXSPI0_B_SCLK/SINC0_MBIT0/SAI0_RXD0/ESPI0_CLK/USB0_PUE_PULLDWN_DM_TEST
P2_4/FC9_P0/SDHC0_CLK/SCT0_OUT2/PWM1_A1/FLEXIO0_D12/EZH_PIO24/FLEXSPI0_B_DATA0/SINC0_MCLK1/SAI0_RXD1/ESPI0_DATA0/USB0_PUE_PULLUP_DP_TEST/WUU0_IN17
P2_5/TRIG_OUT3/FC9_P2/SDHC0_CMD/SCT0_OUT3/PWM1_B1/FLEXIO0_D13/EZH_PIO25/FLEXSPI0_B_DATA1/SINC0_MBIT1/SAI0_TXD1/ESPI0_DATA1/USB0_SRE_LOWSPEED_TEST
P2_6/TRIG_IN4/FC9_P4/SDHC0_D3/SCT0_OUT4/PWM1_A0/FLEXIO0_D14/EZH_PIO26/FLEXSPI0_B_DATA2/SINC0_MCLK2/SAI0_TX_BCLK/ESPI0_DATA2/USB0_PUMPSEL_PULLUP_DP_TEST
P2_7/TRIG_IN6/FC9_P5/SDHC0_D2/SCT0_OUT5/PWM1_B0/FLEXIO0_D15/EZH_PIO27/FLEXSPI0_B_DATA3/SINC0_MBIT2/SAI0_TX_FS/ESPI0_DATA3/USB1_TSTO_PLL_OUT_DIV
P2_8/TRACE_DATA0/SDHC0_D7/SCT0_IN2/PWM1_X0/FLEXIO0_D16/EZH_PIO28/FLEXSPI0_B_DATA4/SINC0_MCLK3/SAI1_TXD0
P2_9/TRACE_DATA1/SDHC0_D6/SCT0_IN3/PWM1_X1/FLEXIO0_D17/EZH_PIO29/FLEXSPI0_B_DATA5/SINC0_MBIT3/SAI1_RXD0
P2_10/TRACE_DATA2/SCT0_IN4/PWM1_X2/FLEXIO0_D18/EZH_PIO31/FLEXSPI0_B_DATA6/SINC0_MCLK4/SAI1_RXD1
P2_11/TRACE_DATA3/SCT0_IN5/PWM1_X3/FLEXIO0_D19/EZH_PIO30/FLEXSPI0_B_DATA7/SINC0_MBIT4/SAI1_TXD1
[12] P2_8/FXIO_D16-FXIO_HDR
[12] P2_9/FXIO_D17-FXIO_HDR
[12] P2_10/FXIO_D18-FXIO_HDR
[12] P2_11/FXIO_D19
[7] P2_1/SDHC0_CD_B
MCXN947VDFT


Classification: Company Internal/Proprietary
Drawing Title:
FRDM-MCXN947
Page Title:
SOC_PORT0-2
Size C
Document Number
SCH-90818 PDF: SPF-90818
Rev B2
Date: Monday, January 22, 2024
Sheet 3 of 13

SOC PORT3~5

Classification: Company Internal/Proprietary

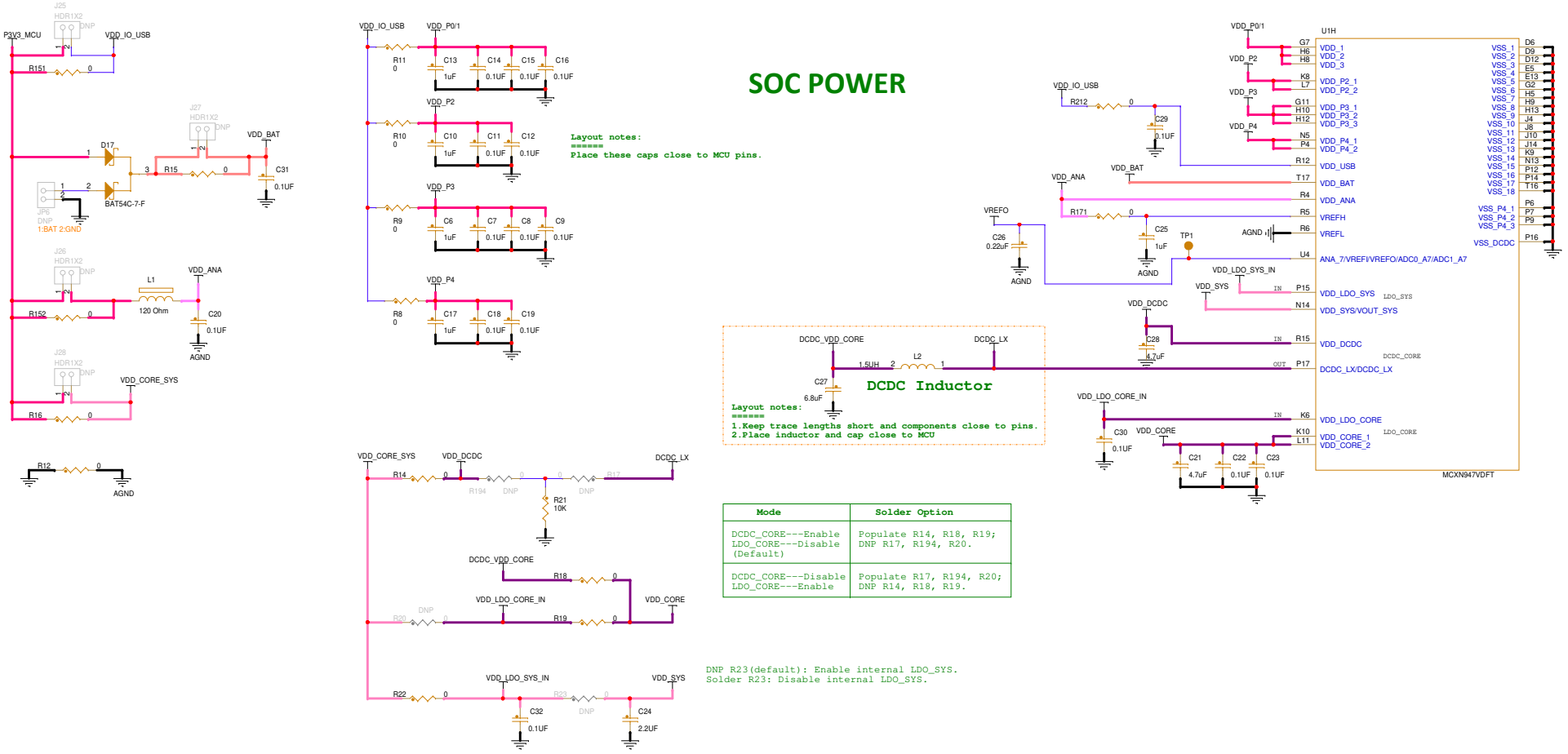
Drawing Title: **FRDM-MCXN947**

Page Title: **SOC_PORT3-5**

Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

Date: Monday, January 22, 2024 | Sheet 4 of 13

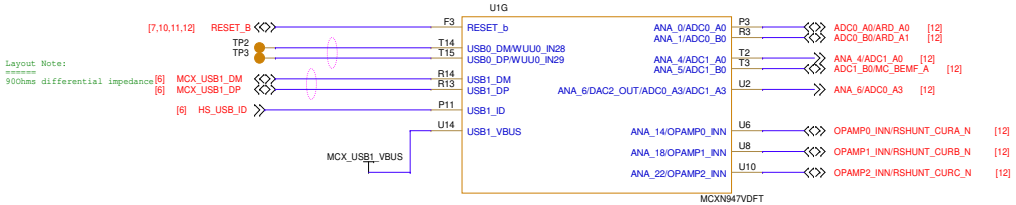
SOC POWER



Mode	Solder Option
DCDC_CORE---Enable LDO_CORE---Disable (Default)	Populate R14, R18, R19; DNP R17, R194, R20.
DCDC_CORE---Disable LDO_CORE---Enable	Populate R17, R194, R20; DNP R14, R18, R19.

DNP R23(default): Enable internal LDO_SYS.
Solder R23: Disable internal LDO_SYS.

SOC USB & Analog Signals



<Core Design>

Classification: Company Internal/Proprietary

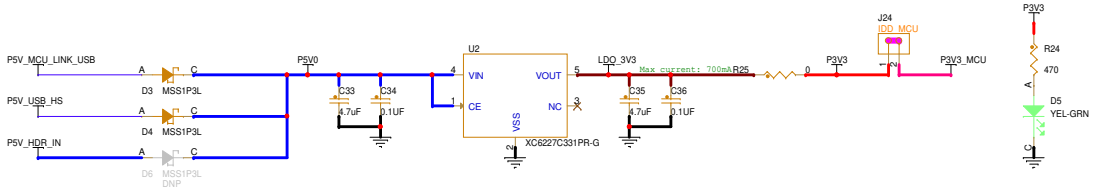
Drawing Title: FRDM-MCXN947

Page Title: SOC_PWR

Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

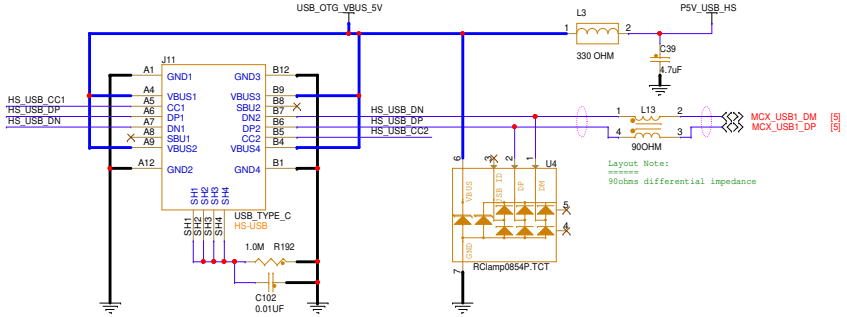
Date: Wednesday, January 24, 2024 Sheet 5 of 13

SYSTEM POWER

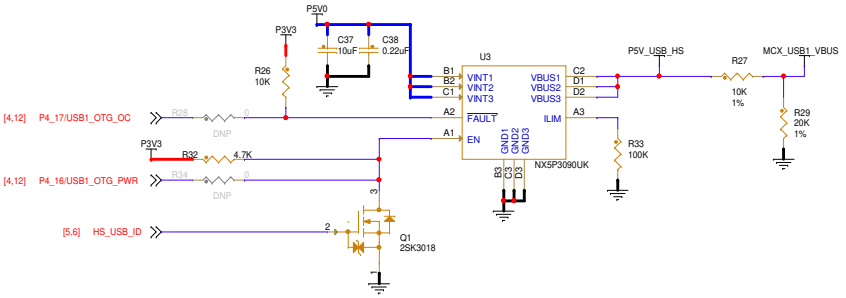


USB1_HIGH SPEED

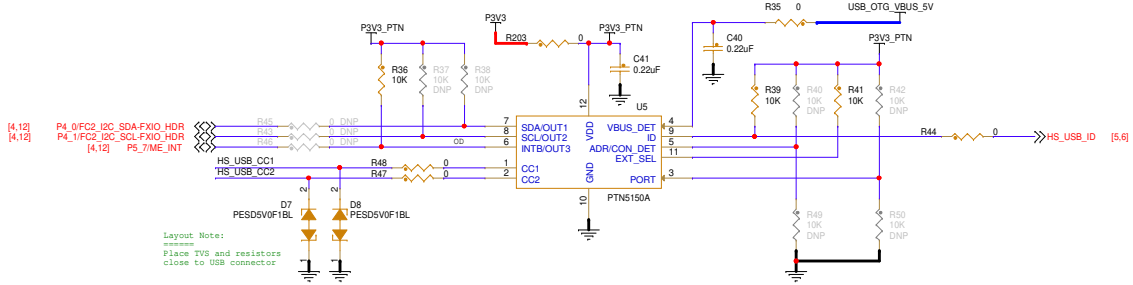
USB2.0 Type C



VBUS Power Control



CC Logic



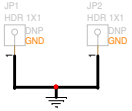
ADR/CON_DET:
When Power-up, ADR(input) function:
ADR=1: I2C Address: 0x7A(ADR)
ADR=0: I2C Address: 0x3A(ADR)
ADR=MID/FLOATING
After TINPUTLATCH, CON_DET(output) function:
CON_DET=1: Connection Detected
CON_DET=0: No Connection

EXT_SEL: External selection
High = CC1 orientation or no valid CC1/CC2 detection
Low = CC2 orientation

PORT=:
1: DFP mode
0: UFP mode
Floating: DRP mode

MOUNTING HOLE

Test Points



<Core Design>

Classification: Company Internal/Proprietary

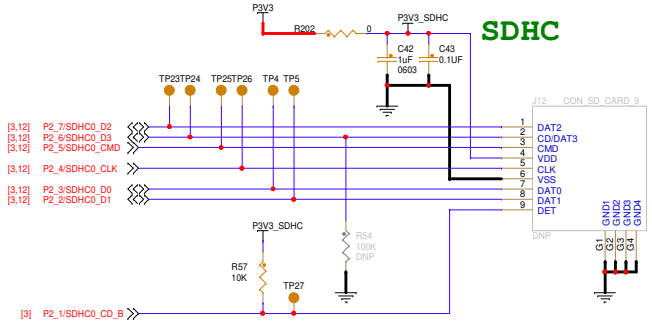
Drawing Title: **FRDM-MCXN947**

Page Title: **USB & PWR**

Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

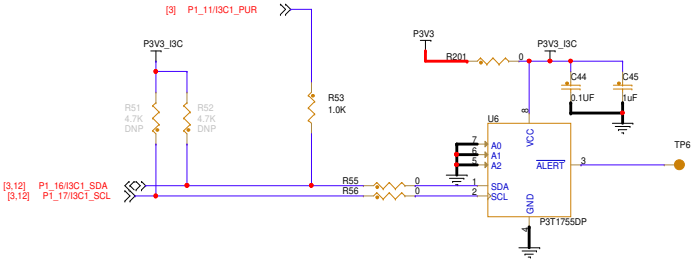
Date: Thursday, January 25, 2024 | Sheet 6 of 13

SDHC



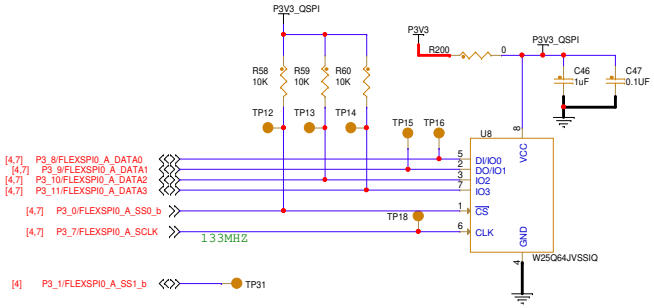
Layout Notes:
=======
1) SDHC signals: equal length routing with 50ohm resistance. And as short as possible.
2) Place R54 to easily rework.

I3C SENSOR



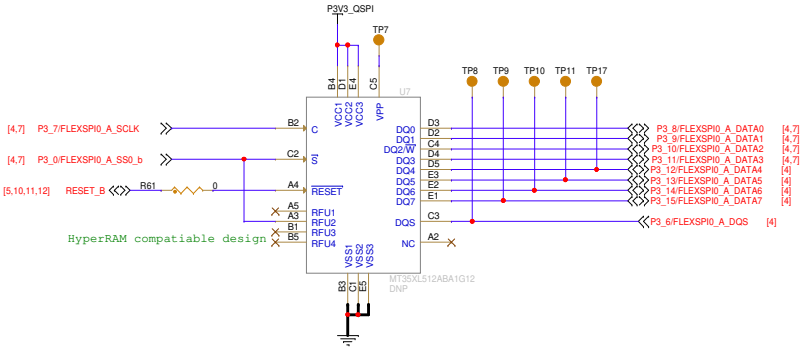
I2C ADDR: 1001000

QSPI



Other QSPI Flash Option: MT25QL128ABA1ESE-0SIT (MICRON)

Octal Flash



Layout Notes:

1. U7 & U8 footprint overlapped.
2. Equal length routing with 50ohm resistance.
3. Place TP31 close to TP12.

<Core Design>

Classification: Company Internal/Proprietary

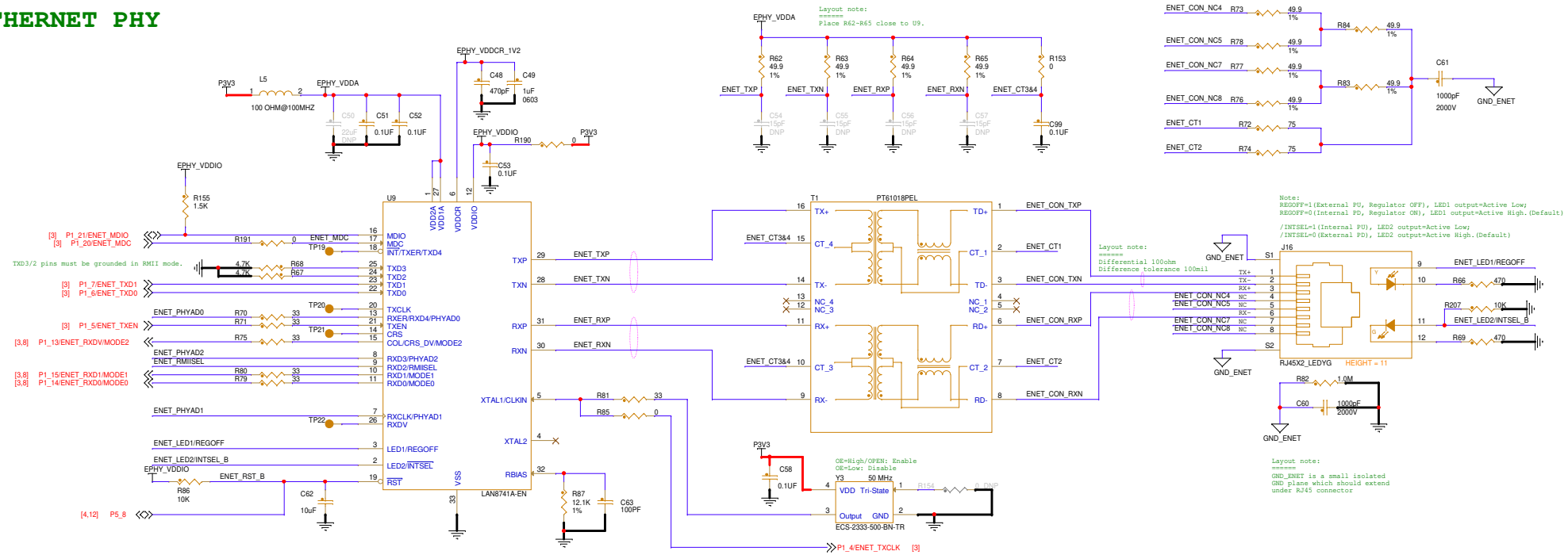
Drawing Title: FRDM-MCXN947

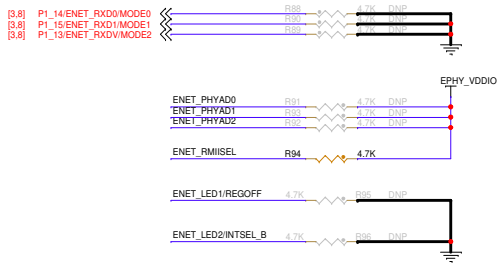
Page Title: SD & QSPI & SENSOR

Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

Date: Monday, January 22, 2024 | Sheet 7 of 13

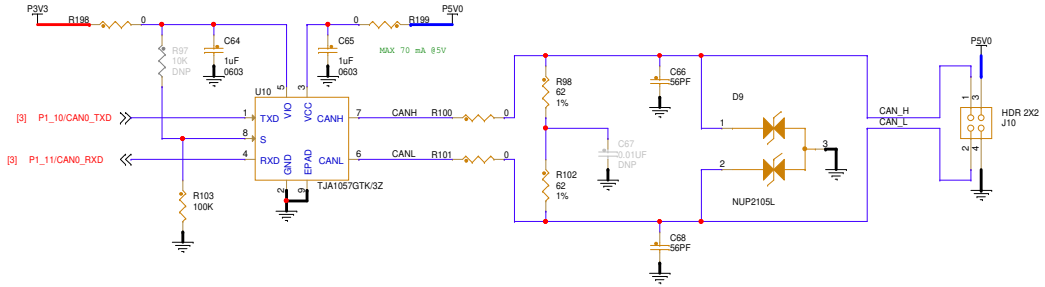
ETHERNET PHY





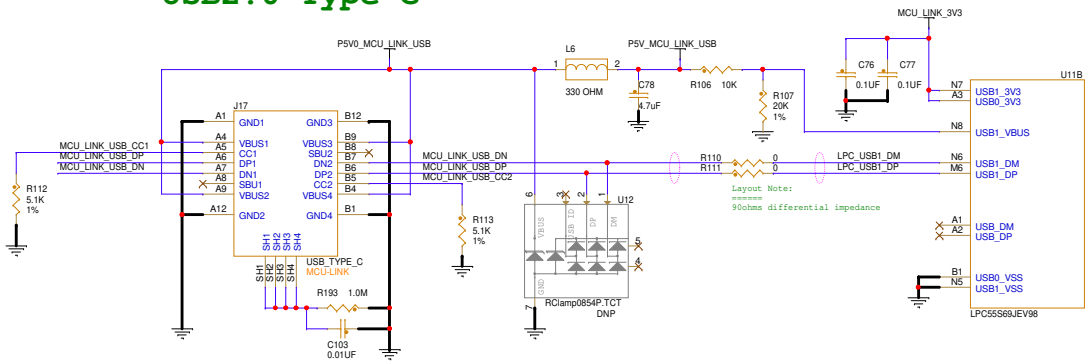
Config Pin (Internal State)	Description	Jumper Setting
MODE[0:2] (PU)	Mode Config 111 => All Capable, auto-neg enabled (Default)	Open (Int PU)
PHYAD[0:2] (PD)	Device Address 000 => Default	Open (Int PU)
RMIISEL (PD)	1 => RMII (Default) 0=> MII	Closed (Ext PU)
REGOFF (PD)	1 => Internal Regulator OFF 0/Floating=> Internal Regulator ON (Default)	Open (Int PU)
INTSEL_B (PU)	Floating 1 => nINT function (Default) 0=> TXD4/TXER function	Open (Int PU)

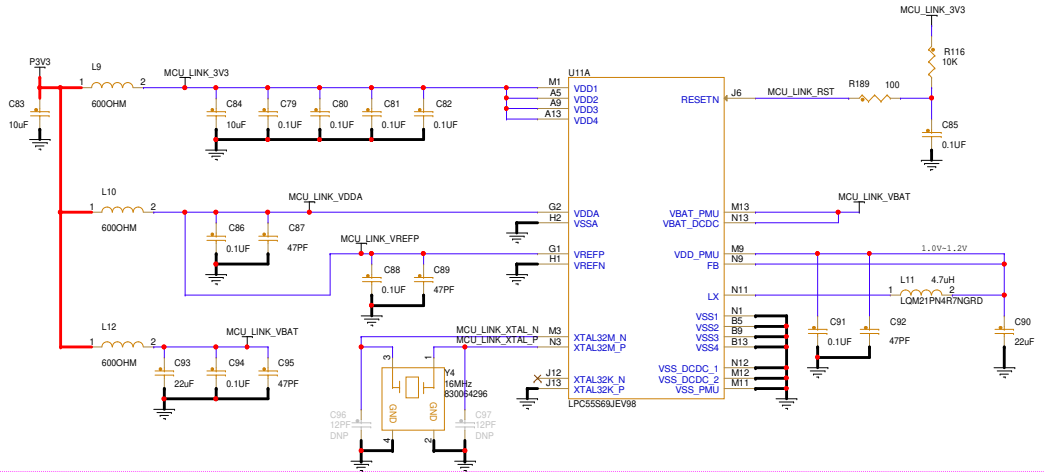
CAN PHY



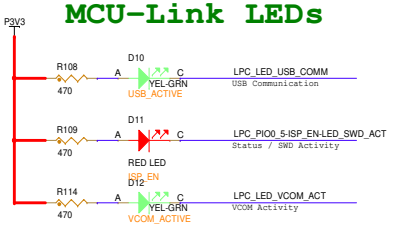
Classification: Company Internal/Proprietary		
Drawing Title: FRDM-MCXN947		
Page Title: CAN PHY & ETHERNET PHY		
Size C	Document Number SCH-90818 PDF: SPF-90818	Rev B2
Date: Thursday, January 25, 2024	Sheet 8 of 13	

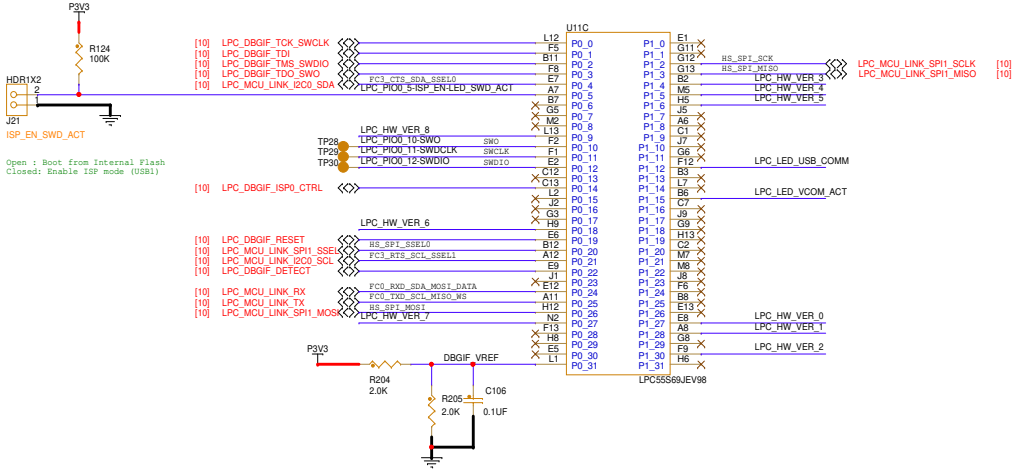
MCU-Link
USB2.0 Type C

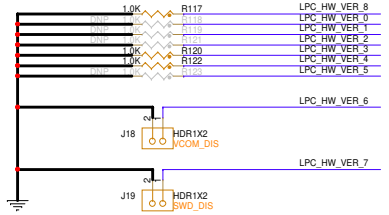




MCU-Link LEDs







Classification: Company Internal/Proprietary

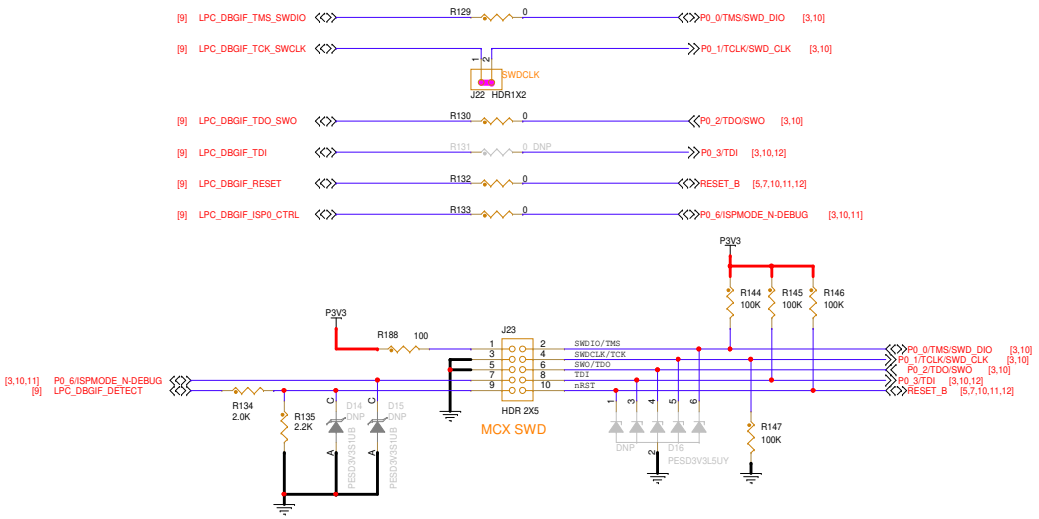
Drawing Title: **FRDM-MCXN947**

Page Title: **MCU_LINK_USB**

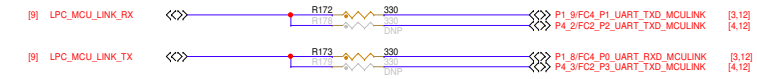
Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

Date: Thursday, January 25, 2024 | Sheet 9 of 13

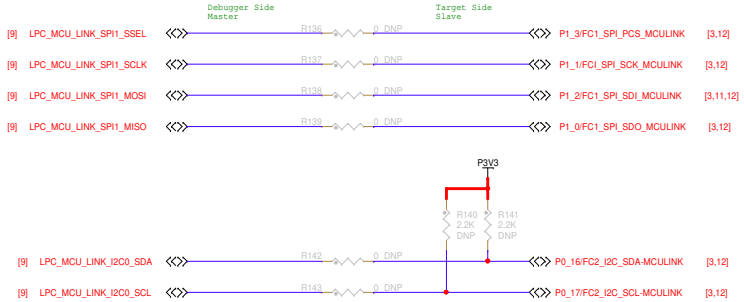
MCU-Link Debug Interface



MCU-Link UART



USB Bridge



Classification: Company Internal/Proprietary

Drawing Title: **FRDM-MCXN947**

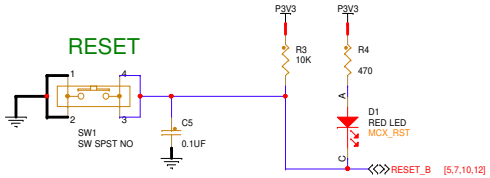
Page Title: **MCU_LINK_DEBUG**

Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

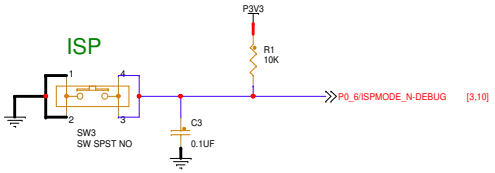
Date: Monday, January 22, 2024 | Sheet 10 of 13

HMI

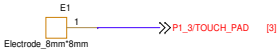
RESET



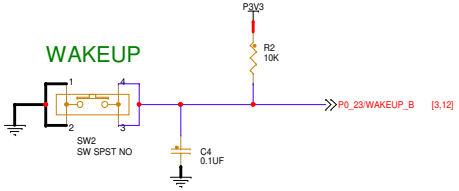
ISP



TOUCH PAD



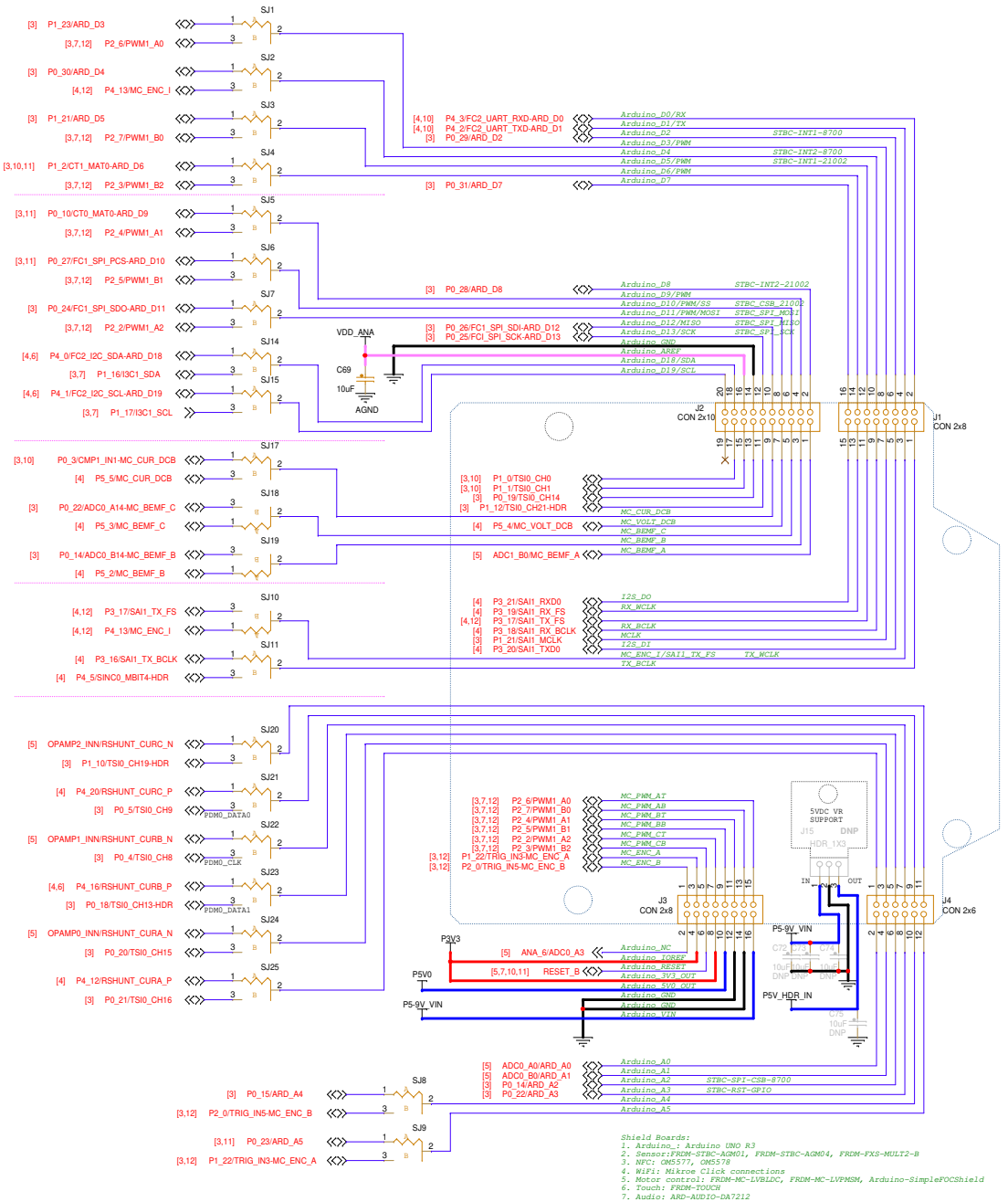
WAKEUP



RGB

Classification: Company Internal/Proprietary		
Drawing Title: FRDM-MCXN947		
Page Title: BLOCK DIAGRAM		
Size C	Document Number SCH-90818 PDF: SPF-90818	Rev B2
Date: Monday, January 22, 2024	Sheet 11 of 13	

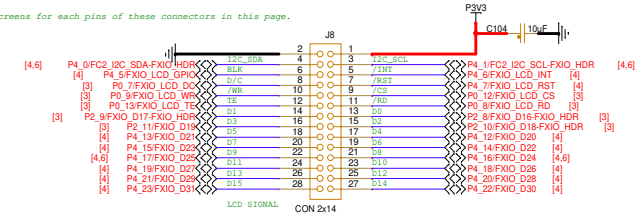
ARDUINO SHIELD COMPATIBLE HEADERS



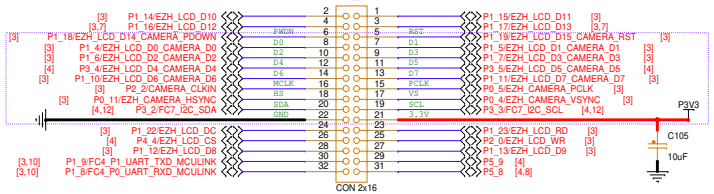
Shield Boards:
1. Arduino_: Arduino UNO R3
2. Sensor:FRDM-STBC-AGM01, FRDM-STBC-AGM04, FRDM-FXS-MULT2-B
3. NFC: OM5577, OM5578
4. WiFi: Mikroe Click connections
5. Motor control: FRDM-MC-LVBLDC, FRDM-MC-LVPMSM, Arduino-SimpleFOCShield
6. Touch: FRDM-TOUCH
7. Audio: ARD-AUDIO-DA7212

FlexIO LCD

Layout notes:
=====
Add clear silkscreens for each pins of these connectors in this page.

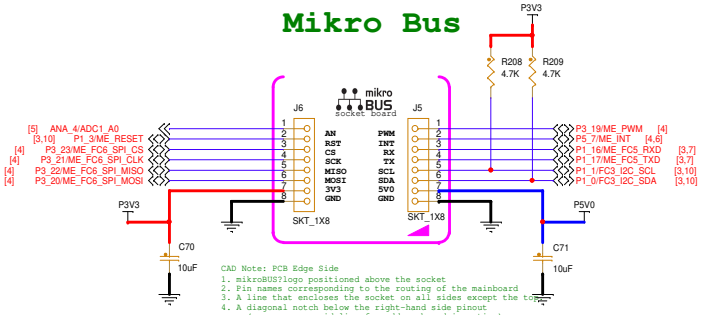


Camera



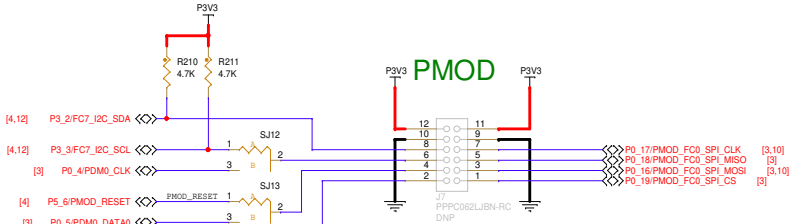
Camera Interface

Mikro Bus



CAD Note: PCB Edge Side
1. mikroBUS?logo positioned above the socket
2. Pin names corresponding to the routing of the mainboard
3. A line that encloses the socket on all sides except the top
4. A diagonal notch below the right-hand side pinout
(serves as a guideline for add-on board insertion)

PMOD



Classification: Company Internal/Proprietary

Drawing Title: **FRDM-MCXN947**

Page Title: **HEADERS**

Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

Date: Monday, January 22, 2024 | Sheet 12 of 13

APPENDIX JUMPER/DNP

REF DES	JUMPER(DEFAULT)	PAGE NAME
J24	1-2	06 USB & PWR
J18,J19	OPEN	09 MCU_LINK_USB
J22	1-2	10 MCU_LINK_DEBUG

REF DES	ASSY_OPT	PAGE NAME
J25,J26,J27,J28,JP6,R17,R20, R23,R194	DNP	05 SOC_PWR
D6,JP1,JP2,R28,R34,R37,R38, R40,R42,R43,R45,R46,R49,R50	DNP	06 USB & PWR
J12,R51,R52,R54,U7	DNP	07 SD & QSPI & SENSOR
C50,C54,C55,C56,C57,C67,R88, R89,R90,R91,R92,R93,R95,R96, R97,R154	DNP	08 CAN PHY & ETHERNET PHY
C96,C97,R118,R119,R121,R123, U12	DNP	09 MCU_LINK_USB
D14,D15,D16,R131,R136,R137, R138,R139,R140,R141,R142, R143,R178,R179	DNP	10 MCU_LINK_DEBUG
C72,C73,C74,C75,J7,J15	DNP	12 HEADERS

REF DES	SHORT(DEFAULT)	PAGE NAME
SJ16,SJ26,SJ27	1-2	03 SOC_PORT0~2
SJ1,SJ2,SJ3,SJ4,SJ5,SJ6,SJ7, SJ8,SJ9,SJ10,SJ11,SJ12,SJ13, SJ14,SJ15,SJ17,SJ18,SJ19, SJ20,SJ21,SJ22,SJ23,SJ24,SJ25	1-2	12 HEADERS

Classification: Company Internal/Proprietary

Drawing Title: FRDM-MCXN947

Page Title: APPENDIX JUMPER/DNP

Size	Document Number	Rev
C	SCH-90818 PDF: SPF-90818	B2

Date: Monday, January 22, 2024 Sheet 13 of 13