

WDDR

version

Contents

WDDR Documentation	1
Overview	2
Features	2
Integration	4
Design Files	4
Configurations	6
Ports	6
Interfaces	12
AHB-Lite Slave Interface	12
AHB-Lite Master Interface	12
DFIv5.0 Interface	12
LPDDR4x Interface	13
LPDDR5 Interface	13
Software	14
MCU subsystem	14
Mailbox Communication	14
Supported Messages	15
Messages from HOST to MCU	15
Messages from MCU to HOST	15
Boot procedure (from HOST level)	15
Registers	17
WAV_MCU__MCUTOP__RSVD	17
WAV_MCU__MCUTOP__CFG	17
WAV_MCU__MCUTOP__STA	17
WAV_MCU__MCUINTF__HOST2MCU_MSG_DATA	17
WAV_MCU__MCUINTF__HOST2MCU_MSG_ID	17
WAV_MCU__MCUINTF__HOST2MCU_MSG_REQ	17
WAV_MCU__MCUINTF__HOST2MCU_MSG_ACK	17
WAV_MCU__MCUINTF__MCU2HOST_MSG_DATA	18
WAV_MCU__MCUINTF__MCU2HOST_MSG_ID	18
WAV_MCU__MCUINTF__MCU2HOST_MSG_REQ	18
WAV_MCU__MCUINTF__MCU2HOST_MSG_ACK	18

WAV_MCU__MCU__IRQ_FAST_CLR_CFG	18
WAV_MCU__MCU__IRQ_FAST_STICKY_CFG	18
WAV_MCU__MCU__IRQ_FAST_MSK_CFG	19
WAV_MCU__MCU__IRQ_FAST_SYNC_CFG	19
WAV_MCU__MCU__IRQ_FAST_EDGE_CFG	19
WAV_MCU__MCU__IRQ_FAST_STA	19
WAV_MCU__MCU__MSIP_CFG	19
WAV_MCU__MCU__MTIME_LO_STA	19
WAV_MCU__MCU__MTIME_HI_STA	20
WAV_MCU__MCU__MTIMECMP_LO_CFG	20
WAV_MCU__MCU__MTIMECMP_HI_CFG	20
WAV_MCU__MCU__MTIMECMP_CFG	20
WAV_MCU__MCU__MTIME_CFG	20
WAV_MCU__MCU__GPO_CFG	20
WAV_MCU__MCU__GP1_CFG	20
WAV_MCU__MCU__GP2_CFG	21
WAV_MCU__MCU__GP3_CFG	21
WAV_MCU__MCU__DEBUG_CFG	21
WAV_MCU__MCU__ITCM_CFG	21
WAV_MCU__MCU__DTCM_CFG	21
WAV_CMN__VREF_M0_CFG	21
WAV_CMN__VREF_M1_CFG	22
WAV_CMN__ZQCAL_CFG	22
WAV_CMN__ZQCAL_STA	22
WAV_CMN__IBIAS_CFG	22
WAV_CMN__TEST_CFG	22
WAV_CMN__LDO_M0_CFG	23
WAV_CMN__LDO_M1_CFG	23
WAV_CMN__CLK_CTRL_CFG	23
WAV_CMN__PMON_ANA_CFG	23
WAV_CMN__PMON_DIG_CFG	24
WAV_CMN__PMON_DIG_NAND_CFG	24
WAV_CMN__PMON_DIG_NOR_CFG	24
WAV_CMN__PMON_NAND_STA	24
WAV_CMN__PMON_NOR_STA	24
WAV_CMN__CLK_STA	24
WAV_CMN__RSTN_CFG	25
WAV_CMN__RSTN_STA	25

WAV_CMN_PLL__CORE_OVERRIDES	25
WAV_CMN_PLL__CORE_SWTICH_VCO	25
WAV_CMN_PLL__CORE_SWTICH_VCO_HW	25
WAV_CMN_PLL__CORE_STATUS	26
WAV_CMN_PLL__CORE_STATUS_INT	26
WAV_CMN_PLL__CORE_STATUS_INT_EN	26
WAV_CMN_PLL__VCO0_BAND	27
WAV_CMN_PLL__VCO0_CONTROL	27
WAV_CMN_PLL__VCO0_FLL_CONTROL1	27
WAV_CMN_PLL__VCO0_FLL_CONTROL2	28
WAV_CMN_PLL__VCO0_FLL_CONTROL3	28
WAV_CMN_PLL__VCO0_FLL_BAND_STATUS	28
WAV_CMN_PLL__VCO0_FLL_COUNT_STATUS	28
WAV_CMN_PLL__VCO0_INT_FRAC_SETTINGS	29
WAV_CMN_PLL__VCO0_PROP_GAINS	29
WAV_CMN_PLL__VCO1_BAND	29
WAV_CMN_PLL__VCO1_CONTROL	29
WAV_CMN_PLL__VCO1_FLL_CONTROL1	29
WAV_CMN_PLL__VCO1_FLL_CONTROL2	30
WAV_CMN_PLL__VCO1_FLL_CONTROL3	30
WAV_CMN_PLL__VCO1_FLL_BAND_STATUS	30
WAV_CMN_PLL__VCO1_FLL_COUNT_STATUS	31
WAV_CMN_PLL__VCO1_INT_FRAC_SETTINGS	31
WAV_CMN_PLL__VCO1_PROP_GAINS	31
WAV_CMN_PLL__VCO1_SSC_CONTROLS	31
WAV_CMN_PLL__VCO2_BAND	31
WAV_CMN_PLL__VCO2_CONTROL	32
WAV_CMN_PLL__VCO2_FLL_CONTROL1	32
WAV_CMN_PLL__VCO2_FLL_CONTROL2	32
WAV_CMN_PLL__VCO2_FLL_CONTROL3	33
WAV_CMN_PLL__VCO2_FLL_BAND_STATUS	33
WAV_CMN_PLL__VCO2_FLL_COUNT_STATUS	33
WAV_CMN_PLL__VCO2_INT_FRAC_SETTINGS	33
WAV_CMN_PLL__VCO2_PROP_GAINS	33
WAV_CMN_PLL__VCO2_SSC_CONTROLS	34
WAV_CMN_PLL__STATE_MACHINE_CONTROLS	34
WAV_CMN_PLL__STATE_MACHINE_CONTROLS2	34
WAV_CMN_PLL__INTR_GAINS	34

WAV_CMN_PLL__INTR_PROP_FL_GAINS	35
WAV_CMN_PLL__INTR_PROP_GAINS_OVERRIDE	35
WAV_CMN_PLL__LOCK_DET_SETTINGS	35
WAV_CMN_PLL__FASTLOCK_DET_SETTINGS	35
WAV_CMN_PLL__ANALOG_EN_RESET	35
WAV_CMN_PLL__MODE_DTST_MISC	36
WAV_CMN_PLL__PROP_CTRLS	36
WAV_CMN_PLL__REFCLK_CONTROLS	36
WAV_CMN_PLL__CLKGATE_DISABLES	36
WAV_FSW__CTRL_CFG	37
WAV_FSW__CTRL_STA	37
WAV_FSW__DEBUG_CFG	37
WAV_FSW__CSP_0_CFG	37
WAV_FSW__CSP_1_CFG	38
WAV_FSW__CSP_STA	38
WAV_CTRL__CLK_CFG	38
WAV_CTRL__CLK_STA	39
WAV_CTRL__AHB_SNOOP_CFG	39
WAV_CTRL__AHB_SNOOP_STA	39
WAV_CTRL__AHB_SNOOP_DATA_STA	39
WAV_CTRL__AHB_SNOOP_PATTERN_CFG	39
WAV_CTRL__AHB_SNOOP_PATTERN_0_CFG	40
WAV_CTRL__AHB_SNOOP_PATTERN_1_CFG	40
WAV_CTRL__AHB_SNOOP_PATTERN_STA	40
WAV_CTRL__DEBUG_CFG	40
WAV_CTRL__DEBUG1_CFG	40
WAV_DFI__TOP_0_CFG	40
WAV_DFI__DATA_BIT_ENABLE_CFG	41
WAV_DFI__PHYFREQ_RANGE_CFG	41
WAV_DFI__STATUS_IF_CFG	41
WAV_DFI__STATUS_IF_STA	41
WAV_DFI__STATUS_IF_EVENT_0_CFG	42
WAV_DFI__STATUS_IF_EVENT_1_CFG	42
WAV_DFI__CTRLUPD_IF_CFG	42
WAV_DFI__CTRLUPD_IF_STA	42
WAV_DFI__CTRLUPD_IF_EVENT_0_CFG	43
WAV_DFI__CTRLUPD_IF_EVENT_1_CFG	43
WAV_DFI__LP_CTRL_IF_CFG	43

WAV_DFI_LP_CTRL_IF_STA	43
WAV_DFI_LP_CTRL_IF_EVENT_0_CFG	43
WAV_DFI_LP_CTRL_IF_EVENT_1_CFG	44
WAV_DFI_LP_DATA_IF_CFG	44
WAV_DFI_LP_DATA_IF_STA	44
WAV_DFI_LP_DATA_IF_EVENT_0_CFG	44
WAV_DFI_LP_DATA_IF_EVENT_1_CFG	44
WAV_DFI_PHYUPD_IF_CFG	45
WAV_DFI_PHYUPD_IF_STA	45
WAV_DFI_PHYMSTR_IF_CFG	45
WAV_DFI_PHYMSTR_IF_STA	45
WAV_DFI_DEBUG_CFG	46
WAV_DFICHO_TOP_1_CFG	46
WAV_DFICHO_TOP_2_CFG	47
WAV_DFICHO_TOP_3_CFG	47
WAV_DFICHO_TOP_STA	47
WAV_DFICHO_IG_DATA_CFG	47
WAV_DFICHO_EG_DATA_STA	47
WAV_DFICHO_WRC_M0_CFG	48
WAV_DFICHO_WRC_M1_CFG	48
WAV_DFICHO_WRCCTRL_M0_CFG	48
WAV_DFICHO_WRCCTRL_M1_CFG	48
WAV_DFICHO_CKCTRL_M0_CFG	48
WAV_DFICHO_CKCTRL_M1_CFG	49
WAV_DFICHO_RDC_M0_CFG	49
WAV_DFICHO_RDC_M1_CFG	49
WAV_DFICHO_RCTRL_M0_CFG	49
WAV_DFICHO_RCTRL_M1_CFG	49
WAV_DFICHO_WCTRL_M0_CFG	50
WAV_DFICHO_WCTRL_M1_CFG	50
WAV_DFICHO_WENCTRL_M0_CFG	50
WAV_DFICHO_WENCTRL_M1_CFG	50
WAV_DFICHO_WCKCTRL_M0_CFG	50
WAV_DFICHO_WCKCTRL_M1_CFG	50
WAV_DFICHO_WRD_M0_CFG	51
WAV_DFICHO_WRD_M1_CFG	51
WAV_DFICHO_RDD_M0_CFG	51
WAV_DFICHO_RDD_M1_CFG	51

WAV_DFICHO_CTRL0_M0_CFG	51
WAV_DFICHO_CTRL0_M1_CFG	52
WAV_DFICHO_CTRL1_M0_CFG	52
WAV_DFICHO_CTRL1_M1_CFG	52
WAV_DFICHO_CTRL2_M0_CFG	52
WAV_DFICHO_CTRL2_M1_CFG	53
WAV_DFICHO_CTRL3_M0_CFG	53
WAV_DFICHO_CTRL3_M1_CFG	53
WAV_DFICHO_CTRL4_M0_CFG	54
WAV_DFICHO_CTRL4_M1_CFG	54
WAV_DFICHO_CTRL5_M0_CFG	54
WAV_DFICHO_CTRL5_M1_CFG	54
WAV_CHO_DQ0_TOP_CFG	54
WAV_CHO_DQ0_TOP_STA	55
WAV_CHO_DQ0_DQ_RX_BSCAN_STA	55
WAV_CHO_DQ0_DQ_RX_M0_CFG	55
WAV_CHO_DQ0_DQ_RX_M1_CFG	55
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_0	55
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_1	55
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_2	56
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_3	56
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_4	56
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_5	56
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_6	56
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_7	56
WAV_CHO_DQ0_DQ_RX_IO_M0_R0_CFG_8	56
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_0	57
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_1	57
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_2	57
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_3	57
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_4	57
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_5	57
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_6	58
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_7	58
WAV_CHO_DQ0_DQ_RX_IO_M0_R1_CFG_8	58
WAV_CHO_DQ0_DQ_RX_IO_M1_R0_CFG_0	58
WAV_CHO_DQ0_DQ_RX_IO_M1_R0_CFG_1	58
WAV_CHO_DQ0_DQ_RX_IO_M1_R0_CFG_2	58

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_3	58
WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_4	59
WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_5	59
WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_6	59
WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_7	59
WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_8	59
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_0	59
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_1	59
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_2	60
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_3	60
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_4	60
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_5	60
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_6	60
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_7	60
WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_8	61
WAV_CH0_DQ0__DQ_RX_IO_STA	61
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_0	61
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_1	61
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_2	61
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_3	62
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_4	62
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_5	62
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_6	63
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_7	63
WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_8	63
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_0	64
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_1	64
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_2	64
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_3	65
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_4	65
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_5	65
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_6	66
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_7	66
WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_8	66
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_0	67
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_1	67
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_2	67
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_3	67

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_4	68
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_5	68
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_6	68
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_7	69
WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_8	69
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_0	69
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_1	70
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_2	70
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_3	70
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_4	71
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_5	71
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_6	71
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_7	72
WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_8	72
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_0	72
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_1	73
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_2	73
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_3	73
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_4	73
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_5	74
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_6	74
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_7	74
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_8	75
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_0	75
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_1	75
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_2	76
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_3	76
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_4	76
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_5	77
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_6	77
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_7	77
WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_8	78
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_0	78
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_1	78
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_2	79
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_3	79
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_4	79
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_5	79

WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_6	80
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_7	80
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R0_CFG_8	80
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_0	81
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_1	81
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_2	81
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_3	82
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_4	82
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_5	82
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_6	83
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_7	83
WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_8	83
WAV_CH0_DQ0__DQ_RX_SA_STA_0	84
WAV_CH0_DQ0__DQ_RX_SA_STA_1	84
WAV_CH0_DQ0__DQ_RX_SA_STA_2	84
WAV_CH0_DQ0__DQ_RX_SA_STA_3	84
WAV_CH0_DQ0__DQ_RX_SA_STA_4	84
WAV_CH0_DQ0__DQ_RX_SA_STA_5	85
WAV_CH0_DQ0__DQ_RX_SA_STA_6	85
WAV_CH0_DQ0__DQ_RX_SA_STA_7	85
WAV_CH0_DQ0__DQ_RX_SA_STA_8	85
WAV_CH0_DQ0__DQ_TX_BSCAN_CFG	86
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_0	86
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_1	86
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_2	86
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_3	86
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_4	86
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_5	87
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_6	87
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_7	87
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_8	87
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_0	87
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_1	87
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_2	88
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_3	88
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_4	88
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_5	88
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_6	88

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_7	88
WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_8	89
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_0	89
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_1	89
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_2	89
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_3	89
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_4	89
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_5	90
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_6	90
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_7	90
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_8	90
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_0	90
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_1	90
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_2	91
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_3	91
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_4	91
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_5	91
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_6	91
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_7	91
WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_8	92
WAV_CH0_DQ0__DQ_TX_ODR_PI_M0_R0_CFG	92
WAV_CH0_DQ0__DQ_TX_ODR_PI_M0_R1_CFG	92
WAV_CH0_DQ0__DQ_TX_ODR_PI_M1_R0_CFG	92
WAV_CH0_DQ0__DQ_TX_ODR_PI_M1_R1_CFG	92
WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M0_R0_CFG	93
WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M0_R1_CFG	93
WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M1_R0_CFG	93
WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M1_R1_CFG	93
WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M0_R0_CFG	93
WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M0_R1_CFG	94
WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M1_R0_CFG	94
WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M1_R1_CFG	94
WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M0_R0_CFG	94
WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M0_R1_CFG	95
WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M1_R0_CFG	95
WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M1_R1_CFG	95
WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M0_R0_CFG	95
WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M0_R1_CFG	95

WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M1_R0_CFG	96
WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M1_R1_CFG	96
WAV_CH0_DQ0__DQ_TX_PI_RT_M0_R0_CFG	96
WAV_CH0_DQ0__DQ_TX_PI_RT_M0_R1_CFG	96
WAV_CH0_DQ0__DQ_TX_PI_RT_M1_R0_CFG	97
WAV_CH0_DQ0__DQ_TX_PI_RT_M1_R1_CFG	97
WAV_CH0_DQ0__DQ_TX_RT_M0_R0_CFG	97
WAV_CH0_DQ0__DQ_TX_RT_M0_R1_CFG	97
WAV_CH0_DQ0__DQ_TX_RT_M1_R0_CFG	97
WAV_CH0_DQ0__DQ_TX_RT_M1_R1_CFG	97
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_0	98
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_1	98
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_2	98
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_3	99
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_4	99
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_5	99
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_6	99
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_7	100
WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_8	100
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_0	100
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_1	101
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_2	101
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_3	101
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_4	102
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_5	102
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_6	102
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_7	103
WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_8	103
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_0	103
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_1	104
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_2	104
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_3	104
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_4	105
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_5	105
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_6	105
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_7	105
WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_8	106
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_0	106

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_1	106
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_2	107
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_3	107
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_4	107
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_5	108
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_6	108
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_7	108
WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_8	109
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_0	109
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_1	109
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_2	110
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_3	110
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_4	110
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_5	111
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_6	111
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_7	111
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_8	111
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_0	112
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_1	112
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_2	112
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_3	113
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_4	113
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_5	113
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_6	114
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_7	114
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_8	114
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_0	115
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_1	115
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_2	115
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_3	116
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_4	116
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_5	116
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_6	117
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_7	117
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_8	117
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_0	117
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_1	118
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_2	118

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_3	118
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_4	119
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_5	119
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_6	119
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_7	120
WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_8	120
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_0	120
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_1	121
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_2	121
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_3	121
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WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_5	122
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_6	122
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_7	123
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_8	123
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_0	123
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_1	123
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_2	124
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_3	124
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_4	124
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_5	125
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_6	125
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_7	125
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_8	126
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WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_1	126
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_2	127
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_3	127
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_4	127
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_5	128
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_6	128
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_7	128
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_8	129
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_0	129
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WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_4	130

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_5	130
WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_6	131
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WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_8	131
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WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_1	132
WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_2	132
WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_3	132
WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_4	133
WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_5	133
WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_6	133
WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_7	133
WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_8	133
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WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_1	134
WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_2	134
WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_3	134
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WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_5	135
WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_6	135
WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_7	135
WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_8	135
WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_0	136
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WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_2	136
WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_3	136
WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_4	137
WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_5	137
WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_6	137
WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_7	137
WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_8	137
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_0	138
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_1	138
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_2	138
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_3	138
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_4	139
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_5	139
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_6	139

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_7	139
WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_8	139
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_0	140
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WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_2	140
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WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_5	141
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_6	141
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_7	141
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_8	141
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_0	142
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_1	142
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_2	142
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WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_4	143
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_5	143
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WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_6	145
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WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_8	145
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WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_3	146
WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_4	147
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WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_6	149
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WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_4	151
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WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_8	154
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WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_1	154

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_2	154
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_3	154
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WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_5	155
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_6	155
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_7	155
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_8	155
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_0	155
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_1	156
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_2	156
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_3	156
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_4	156
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_5	156
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_6	156
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_7	157
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_8	157
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_0	157
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WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_2	157
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_3	158
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_4	158
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_5	158
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_6	158
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_7	158
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_8	158
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_0	159
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_1	159
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_2	159
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_3	159
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_4	159
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_5	159
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_6	160
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_7	160
WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_8	160
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_0	160
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_1	160
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_2	161
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_3	161

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_4	161
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_5	161
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_6	161
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_7	161
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_8	162
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_0	162
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_1	162
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_2	162
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_3	162
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_4	163
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_5	163
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_6	163
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_7	163
WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_8	163
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_0	164
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_1	164
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_2	164
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_3	164
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_4	164
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_5	165
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_6	165
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_7	165
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_8	165
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_0	165
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_1	166
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_2	166
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_3	166
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_4	166
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_5	166
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_6	167
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_7	167
WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_8	167
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_0	167
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_1	167
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_2	168
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_3	168
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_4	168
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_5	169

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_6	169
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_7	169
WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_8	169
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_0	170
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_1	170
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_2	170
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_3	170
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_4	171
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_5	171
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_6	171
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_7	172
WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_8	172
WAV_CH0_DQ0__DQS_RX_M0_CFG	172
WAV_CH0_DQ0__DQS_RX_M1_CFG	172
WAV_CH0_DQ0__DQS_RX_BSCAN_STA	172
WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M0_R0_CFG	173
WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M0_R1_CFG	173
WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M1_R0_CFG	173
WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M1_R1_CFG	173
WAV_CH0_DQ0__DQS_RX_REN_PI_M0_R0_CFG	173
WAV_CH0_DQ0__DQS_RX_REN_PI_M0_R1_CFG	174
WAV_CH0_DQ0__DQS_RX_REN_PI_M1_R0_CFG	174
WAV_CH0_DQ0__DQS_RX_REN_PI_M1_R1_CFG	174
WAV_CH0_DQ0__DQS_RX_RCS_PI_M0_R0_CFG	174
WAV_CH0_DQ0__DQS_RX_RCS_PI_M0_R1_CFG	175
WAV_CH0_DQ0__DQS_RX_RCS_PI_M1_R0_CFG	175
WAV_CH0_DQ0__DQS_RX_RCS_PI_M1_R1_CFG	175
WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M0_R0_CFG	175
WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M0_R1_CFG	175
WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M1_R0_CFG	176
WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M1_R1_CFG	176
WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M0_R0_CFG	176
WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M0_R1_CFG	176
WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M1_R0_CFG	177
WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M1_R1_CFG	177
WAV_CH0_DQ0__DQS_RX_PI_STA	177
WAV_CH0_DQ0__DQS_RX_IO_M0_R0_CFG_0	177
WAV_CH0_DQ0__DQS_RX_IO_M0_R0_CFG_1	177

WAV_CH0_DQ0__DQS_RX_IO_M0_R1_CFG_0	177
WAV_CH0_DQ0__DQS_RX_IO_M0_R1_CFG_1	178
WAV_CH0_DQ0__DQS_RX_IO_M1_R0_CFG_0	178
WAV_CH0_DQ0__DQS_RX_IO_M1_R0_CFG_1	178
WAV_CH0_DQ0__DQS_RX_IO_M1_R1_CFG_0	178
WAV_CH0_DQ0__DQS_RX_IO_M1_R1_CFG_1	178
WAV_CH0_DQ0__DQS_RX_IO_CMN_M0_R0_CFG	179
WAV_CH0_DQ0__DQS_RX_IO_CMN_M0_R1_CFG	179
WAV_CH0_DQ0__DQS_RX_IO_CMN_M1_R0_CFG	179
WAV_CH0_DQ0__DQS_RX_IO_CMN_M1_R1_CFG	180
WAV_CH0_DQ0__DQS_RX_IO_STA	180
WAV_CH0_DQ0__DQS_RX_SA_M0_R0_CFG_0	180
WAV_CH0_DQ0__DQS_RX_SA_M0_R0_CFG_1	180
WAV_CH0_DQ0__DQS_RX_SA_M0_R1_CFG_0	181
WAV_CH0_DQ0__DQS_RX_SA_M0_R1_CFG_1	181
WAV_CH0_DQ0__DQS_RX_SA_M1_R0_CFG_0	181
WAV_CH0_DQ0__DQS_RX_SA_M1_R0_CFG_1	182
WAV_CH0_DQ0__DQS_RX_SA_M1_R1_CFG_0	182
WAV_CH0_DQ0__DQS_RX_SA_M1_R1_CFG_1	182
WAV_CH0_DQ0__DQS_RX_SA_CMN_CFG	183
WAV_CH0_DQ0__DQS_TX_M0_CFG	183
WAV_CH0_DQ0__DQS_TX_M1_CFG	183
WAV_CH0_DQ0__DQS_TX_BSCAN_CTRL_CFG	183
WAV_CH0_DQ0__DQS_TX_BSCAN_CFG	183
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_0	184
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_1	184
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_2	184
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_3	184
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_4	184
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_5	184
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_6	185
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_7	185
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_8	185
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_0	185
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_1	185
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_2	185
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_3	186
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_4	186

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_5	186
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_6	186
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_7	186
WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_8	186
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_0	187
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_1	187
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_2	187
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_3	187
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_4	187
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_5	187
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_6	188
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_7	188
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_8	188
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_0	188
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_1	188
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_2	188
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_3	189
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_4	189
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_5	189
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_6	189
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_7	189
WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_8	189
WAV_CH0_DQ0__DQS_TX_ODR_PI_M0_R0_CFG	190
WAV_CH0_DQ0__DQS_TX_ODR_PI_M0_R1_CFG	190
WAV_CH0_DQ0__DQS_TX_ODR_PI_M1_R0_CFG	190
WAV_CH0_DQ0__DQS_TX_ODR_PI_M1_R1_CFG	190
WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M0_R0_CFG	190
WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M0_R1_CFG	191
WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M1_R0_CFG	191
WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M1_R1_CFG	191
WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M0_R0_CFG	191
WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M0_R1_CFG	192
WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M1_R0_CFG	192
WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M1_R1_CFG	192
WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M0_R0_CFG	192
WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M0_R1_CFG	192
WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M1_R0_CFG	193
WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M1_R1_CFG	193

WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M0_R0_CFG	193
WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M0_R1_CFG	193
WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M1_R0_CFG	194
WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M1_R1_CFG	194
WAV_CH0_DQ0__DQS_TX_PI_RT_M0_R0_CFG	194
WAV_CH0_DQ0__DQS_TX_PI_RT_M0_R1_CFG	194
WAV_CH0_DQ0__DQS_TX_PI_RT_M1_R0_CFG	194
WAV_CH0_DQ0__DQS_TX_PI_RT_M1_R1_CFG	195
WAV_CH0_DQ0__DQS_TX_SDR_PI_M0_R0_CFG	195
WAV_CH0_DQ0__DQS_TX_SDR_PI_M0_R1_CFG	195
WAV_CH0_DQ0__DQS_TX_SDR_PI_M1_R0_CFG	195
WAV_CH0_DQ0__DQS_TX_SDR_PI_M1_R1_CFG	196
WAV_CH0_DQ0__DQS_TX_DFI_PI_M0_R0_CFG	196
WAV_CH0_DQ0__DQS_TX_DFI_PI_M0_R1_CFG	196
WAV_CH0_DQ0__DQS_TX_DFI_PI_M1_R0_CFG	196
WAV_CH0_DQ0__DQS_TX_DFI_PI_M1_R1_CFG	196
WAV_CH0_DQ0__DQS_TX_RT_M0_R0_CFG	197
WAV_CH0_DQ0__DQS_TX_RT_M0_R1_CFG	197
WAV_CH0_DQ0__DQS_TX_RT_M1_R0_CFG	197
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WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_0	197
WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_1	198
WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_2	198
WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_3	198
WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_4	199
WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_5	199
WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_6	199
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WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_8	203

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WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_2	204
WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_3	204
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WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_5	205
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WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_8	205
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_0	206
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_1	206
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_2	206
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_3	207
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_4	207
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_5	207
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_6	208
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_7	208
WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_8	208
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_0	209
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_1	209
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_2	209
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_3	210
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_4	210
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_5	210
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_6	211
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_7	211
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_8	211
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_0	211
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_1	212
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WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_3	212
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_4	213
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_5	213
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_6	213
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_7	214
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_8	214
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_0	214
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_1	215

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_2	215
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_3	215
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_4	216
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_5	216
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_6	216
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_7	217
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_8	217
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_0	217
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_1	217
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_2	218
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_3	218
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_4	218
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_5	219
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_6	219
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_7	219
WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_8	220
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_0	220
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_1	220
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_2	221
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_3	221
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_4	221
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_5	222
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_6	222
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_7	222
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_8	223
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_0	223
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_1	223
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_2	223
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_3	224
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_4	224
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_5	224
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_6	225
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_7	225
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_8	225
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WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_2	226
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_3	227

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_4	227
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_5	227
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WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_0	229
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_1	229
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_2	229
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_3	229
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_4	230
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_5	230
WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_6	230
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WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_8	231
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WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_5	234
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WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_0	237
WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_1	238
WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_2	238
WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_3	238
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WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_5	238
WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_6	239
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WAV_CH0_DQ0__DQS_TX_IO_CMN_M0_R1_CFG	263
WAV_CH0_DQ0__DQS_TX_IO_CMN_M1_R0_CFG	263
WAV_CH0_DQ0__DQS_TX_IO_CMN_M1_R1_CFG	263
WAV_CH0_DQ1__TOP_CFG	263
WAV_CH0_DQ1__TOP_STA	264
WAV_CH0_DQ1__DQ_RX_BSCAN_STA	264
WAV_CH0_DQ1__DQ_RX_M0_CFG	264
WAV_CH0_DQ1__DQ_RX_M1_CFG	264
WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_0	264
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WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_4	283
WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_5	283
WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_6	283
WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_7	283
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WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R1_CFG_2	285
WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R1_CFG_3	285
WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R1_CFG_4	285

WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R1_CFG_5	286
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WAV_CH0_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_3	288
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WAV_CH0_DQ1__DQ_RX_SA_STA_1	293
WAV_CH0_DQ1__DQ_RX_SA_STA_2	293
WAV_CH0_DQ1__DQ_RX_SA_STA_3	293
WAV_CH0_DQ1__DQ_RX_SA_STA_4	294
WAV_CH0_DQ1__DQ_RX_SA_STA_5	294
WAV_CH0_DQ1__DQ_RX_SA_STA_6	294
WAV_CH0_DQ1__DQ_RX_SA_STA_7	294
WAV_CH0_DQ1__DQ_RX_SA_STA_8	294
WAV_CH0_DQ1__DQ_TX_BSCAN_CFG	295
WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_0	295
WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_1	295
WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_2	295
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WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_5	296

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_6	296
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WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_3	297
WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_4	297
WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_5	297
WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_6	297
WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_7	297
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WAV_CH0_DQ1__DQ_TX_ODR_PI_M0_R1_CFG	301
WAV_CH0_DQ1__DQ_TX_ODR_PI_M1_R0_CFG	301
WAV_CH0_DQ1__DQ_TX_ODR_PI_M1_R1_CFG	301
WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M0_R0_CFG	302
WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M0_R1_CFG	302
WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M1_R0_CFG	302
WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M1_R1_CFG	302

WAV_CH0_DQ1__DQ_TX_QDR_PI_1_M0_R0_CFG	303
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WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_4	352
WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_5	352
WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_6	352
WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_7	352
WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_8	353
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WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_7	354

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WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_7	376
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WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_3	377
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WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_7	381
WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_8	381
WAV_CH0_DQ1__DQS_RX_M0_CFG	381
WAV_CH0_DQ1__DQS_RX_M1_CFG	381
WAV_CH0_DQ1__DQS_RX_BSCAN_STA	382
WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M0_R0_CFG	382
WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M0_R1_CFG	382
WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M1_R0_CFG	382
WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M1_R1_CFG	382
WAV_CH0_DQ1__DQS_RX_REN_PI_M0_R0_CFG	383
WAV_CH0_DQ1__DQS_RX_REN_PI_M0_R1_CFG	383
WAV_CH0_DQ1__DQS_RX_REN_PI_M1_R0_CFG	383
WAV_CH0_DQ1__DQS_RX_REN_PI_M1_R1_CFG	383
WAV_CH0_DQ1__DQS_RX_RCS_PI_M0_R0_CFG	384
WAV_CH0_DQ1__DQS_RX_RCS_PI_M0_R1_CFG	384
WAV_CH0_DQ1__DQS_RX_RCS_PI_M1_R0_CFG	384
WAV_CH0_DQ1__DQS_RX_RCS_PI_M1_R1_CFG	384
WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M0_R0_CFG	384

WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M0_R1_CFG	385
WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M1_R0_CFG	385
WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M1_R1_CFG	385
WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M0_R0_CFG	385
WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M0_R1_CFG	386
WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M1_R0_CFG	386
WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M1_R1_CFG	386
WAV_CH0_DQ1__DQS_RX_PI_STA	386
WAV_CH0_DQ1__DQS_RX_IO_M0_R0_CFG_0	386
WAV_CH0_DQ1__DQS_RX_IO_M0_R0_CFG_1	387
WAV_CH0_DQ1__DQS_RX_IO_M0_R1_CFG_0	387
WAV_CH0_DQ1__DQS_RX_IO_M0_R1_CFG_1	387
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WAV_CH0_DQ1__DQS_RX_IO_M1_R0_CFG_1	387
WAV_CH0_DQ1__DQS_RX_IO_M1_R1_CFG_0	387
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WAV_CH0_DQ1__DQS_RX_IO_CMN_M0_R0_CFG	388
WAV_CH0_DQ1__DQS_RX_IO_CMN_M0_R1_CFG	388
WAV_CH0_DQ1__DQS_RX_IO_CMN_M1_R0_CFG	388
WAV_CH0_DQ1__DQS_RX_IO_CMN_M1_R1_CFG	389
WAV_CH0_DQ1__DQS_RX_IO_STA	389
WAV_CH0_DQ1__DQS_RX_SA_M0_R0_CFG_0	389
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WAV_CH0_DQ1__DQS_RX_SA_M1_R1_CFG_0	391
WAV_CH0_DQ1__DQS_RX_SA_M1_R1_CFG_1	392
WAV_CH0_DQ1__DQS_RX_SA_CMN_CFG	392
WAV_CH0_DQ1__DQS_TX_M0_CFG	392
WAV_CH0_DQ1__DQS_TX_M1_CFG	392
WAV_CH0_DQ1__DQS_TX_BSCAN_CTRL_CFG	393
WAV_CH0_DQ1__DQS_TX_BSCAN_CFG	393
WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_0	393
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WAV_CH0_DQ1__DQS_TX_ODR_PI_M1_R1_CFG	399
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WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_2	407
WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_3	407
WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_4	408
WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_5	408
WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_6	408
WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_7	409

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WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_7	469
WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_8	469
WAV_CH0_DQ1__DQS_TX_LPDE_M0_R0_CFG_0	469
WAV_CH0_DQ1__DQS_TX_LPDE_M0_R0_CFG_1	469
WAV_CH0_DQ1__DQS_TX_LPDE_M0_R1_CFG_0	469
WAV_CH0_DQ1__DQS_TX_LPDE_M0_R1_CFG_1	470
WAV_CH0_DQ1__DQS_TX_LPDE_M1_R0_CFG_0	470
WAV_CH0_DQ1__DQS_TX_LPDE_M1_R0_CFG_1	470
WAV_CH0_DQ1__DQS_TX_LPDE_M1_R1_CFG_0	470
WAV_CH0_DQ1__DQS_TX_LPDE_M1_R1_CFG_1	470
WAV_CH0_DQ1__DQS_TX_IO_M0_CFG_0	471
WAV_CH0_DQ1__DQS_TX_IO_M0_CFG_1	471
WAV_CH0_DQ1__DQS_TX_IO_M1_CFG_0	471
WAV_CH0_DQ1__DQS_TX_IO_M1_CFG_1	471
WAV_CH0_DQ1__DQS_TX_IO_CMN_M0_R0_CFG	472
WAV_CH0_DQ1__DQS_TX_IO_CMN_M0_R1_CFG	472
WAV_CH0_DQ1__DQS_TX_IO_CMN_M1_R0_CFG	472
WAV_CH0_DQ1__DQS_TX_IO_CMN_M1_R1_CFG	472
WAV_CH0_CA__TOP_CFG	473
WAV_CH0_CA__TOP_STA	473
WAV_CH0_CA__DQ_RX_BSCAN_STA	473
WAV_CH0_CA__DQ_RX_M0_CFG	473
WAV_CH0_CA__DQ_RX_M1_CFG	473
WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_0	474

WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_1	474
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_2	474
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_3	474
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_4	474
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_5	474
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_6	475
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_7	475
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_8	475
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_9	475
WAV_CHO_CA__DQ_RX_IO_M0_R0_CFG_10	475
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_0	475
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_1	475
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_2	476
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_3	476
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_4	476
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_5	476
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_6	476
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_7	476
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_8	476
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_9	477
WAV_CHO_CA__DQ_RX_IO_M0_R1_CFG_10	477
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WAV_CHO_CA__DQ_RX_IO_M1_R0_CFG_4	478
WAV_CHO_CA__DQ_RX_IO_M1_R0_CFG_5	478
WAV_CHO_CA__DQ_RX_IO_M1_R0_CFG_6	478
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WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_1	479
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WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_3	479
WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_4	479
WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_5	479

WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_6	479
WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_7	480
WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_8	480
WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_9	480
WAV_CHO_CA__DQ_RX_IO_M1_R1_CFG_10	480
WAV_CHO_CA__DQ_RX_IO_STA	480
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_0	480
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_1	481
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_2	481
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_3	481
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_4	482
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_5	482
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_6	482
WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_7	483
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WAV_CHO_CA__DQ_RX_SA_M0_R0_CFG_9	483
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WAV_CHO_CA__DQ_RX_SA_M0_R1_CFG_0	484
WAV_CHO_CA__DQ_RX_SA_M0_R1_CFG_1	484
WAV_CHO_CA__DQ_RX_SA_M0_R1_CFG_2	484
WAV_CHO_CA__DQ_RX_SA_M0_R1_CFG_3	485
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WAV_CHO_CA__DQ_RX_SA_M0_R1_CFG_8	486
WAV_CHO_CA__DQ_RX_SA_M0_R1_CFG_9	487
WAV_CHO_CA__DQ_RX_SA_M0_R1_CFG_10	487
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_0	487
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_1	488
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_2	488
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_3	488
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_4	489
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_5	489
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_6	489
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_7	490
WAV_CHO_CA__DQ_RX_SA_M1_R0_CFG_8	490
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WAV_CHO_CA__DQ_RX_SA_M1_R1_CFG_6	493
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WAV_CHO_CA__DQ_RX_SA_M1_R1_CFG_8	493
WAV_CHO_CA__DQ_RX_SA_M1_R1_CFG_9	494
WAV_CHO_CA__DQ_RX_SA_M1_R1_CFG_10	494
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WAV_CHO_CA__DQ_RX_SA_DLY_M0_R0_CFG_3	495
WAV_CHO_CA__DQ_RX_SA_DLY_M0_R0_CFG_4	496
WAV_CHO_CA__DQ_RX_SA_DLY_M0_R0_CFG_5	496
WAV_CHO_CA__DQ_RX_SA_DLY_M0_R0_CFG_6	496
WAV_CHO_CA__DQ_RX_SA_DLY_M0_R0_CFG_7	496
WAV_CHO_CA__DQ_RX_SA_DLY_M0_R0_CFG_8	497
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WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_1	505
WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_2	505
WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_3	506
WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_4	506
WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_5	506
WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_6	507
WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_7	507
WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_8	507
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WAV_CHO_CA__DQ_RX_SA_DLY_M1_R1_CFG_10	508
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WAV_CHO_CA__DQ_TX_BSCAN_CFG	511
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WAV_CHO_CA__DQ_TX_ODR_PI_M0_R0_CFG	518
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WAV_CHO_CA__DQ_TX_IO_M1_CFG_6	614
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WAV_CHO_CA__DQS_RX_M1_CFG	615
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WAV_CHO_CA__DQS_RX_SDR_LPDE_M0_R0_CFG	616
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WAV_CHO_CA__DQS_RX_SDR_LPDE_M1_R1_CFG	616
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WAV_CHO_CA__DQS_RX_RDQS_PI_0_M1_R0_CFG	619

WAV_CHO_CA__DQS_RX_RDQS_PI_0_M1_R1_CFG	619
WAV_CHO_CA__DQS_RX_RDQS_PI_1_M0_R0_CFG	619
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WAV_CHO_CA__DQS_RX_IO_CMN_M0_R1_CFG	621
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WAV_CHO_CA__DQS_TX_ODR_PI_M1_R1_CFG	626
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WAV_CHO_CA__DQS_TX_QDR_PI_0_M0_R1_CFG	626
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WAV_CHO_CA__DQS_TX_QDR_PI_1_M0_R1_CFG	627

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WAV_CH1_DQ0__TOP_STA	643
WAV_CH1_DQ0__DQ_RX_BSCAN_STA	643
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WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_4	741
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WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_6	741
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WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_5	801
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WAV_CH1_DQ0__DQS_TX_IO_CMN_M1_R1_CFG	851
WAV_CH1_DQ1__TOP_CFG	851
WAV_CH1_DQ1__TOP_STA	852

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WAV_CH1_DQ1__DQ_RX_M0_CFG	852
WAV_CH1_DQ1__DQ_RX_M1_CFG	852
WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_0	852
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WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_4	857
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WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_6	857
WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_7	857

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WAV_CH1_DQ1__DQ_RX_IO_STA	858
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WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_7	969
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WAV_CH1_DQ1__DQS_RX_M0_CFG	969
WAV_CH1_DQ1__DQS_RX_M1_CFG	969

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WAV_CH1_DQ1__DQS_RX_SDR_LPDE_M0_R0_CFG	970
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WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_6	985
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WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_8	985
WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_0	985

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WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_2	986
WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_3	986
WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_4	986
WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_5	986
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WAV_CH1_DQ1__DQS_TX_ODR_PI_M0_R0_CFG	987
WAV_CH1_DQ1__DQS_TX_ODR_PI_M0_R1_CFG	987
WAV_CH1_DQ1__DQS_TX_ODR_PI_M1_R0_CFG	987
WAV_CH1_DQ1__DQS_TX_ODR_PI_M1_R1_CFG	987
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WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_3	1048
WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_4	1048
WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_5	1049
WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_6	1049
WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_7	1049
WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_8	1049
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_0	1049
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_1	1049
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_2	1050
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_3	1050
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_4	1050
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_5	1050
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_6	1050
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_7	1050
WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_8	1051
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_0	1051
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_1	1051
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_2	1051
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_3	1051
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_4	1051
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_5	1052

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_6	1052
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_7	1052
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_8	1052
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_0	1052
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WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_2	1053
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_3	1053
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_4	1053
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_5	1053
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WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_4	1055
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WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_4	1056
WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_5	1056
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WAV_CH1_DQ1__DQS_TX_LPDE_M0_R0_CFG_0	1057
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WAV_CH1_DQ1__DQS_TX_LPDE_M1_R1_CFG_1	1058

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WAV_CH1_DQ1__DQS_TX_IO_M0_CFG_1	1059
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WAV_CH1_DQ1__DQS_TX_IO_CMN_M0_R0_CFG	1060
WAV_CH1_DQ1__DQS_TX_IO_CMN_M0_R1_CFG	1060
WAV_CH1_DQ1__DQS_TX_IO_CMN_M1_R0_CFG	1060
WAV_CH1_DQ1__DQS_TX_IO_CMN_M1_R1_CFG	1060
WAV_CH1_CA__TOP_CFG	1061
WAV_CH1_CA__TOP_STA	1061
WAV_CH1_CA__DQ_RX_BSCAN_STA	1061
WAV_CH1_CA__DQ_RX_M0_CFG	1061
WAV_CH1_CA__DQ_RX_M1_CFG	1061
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_0	1062
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_1	1062
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_2	1062
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_3	1062
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_4	1062
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_5	1062
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_6	1063
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_7	1063
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_8	1063
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_9	1063
WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_10	1063
WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_0	1063
WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_1	1063
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WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_8	1066
WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_9	1066
WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_10	1066
WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_0	1067
WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_1	1067
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WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_7	1068
WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_8	1068
WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_9	1068
WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_10	1068
WAV_CH1_CA__DQ_RX_IO_STA	1068
WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_0	1068
WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_1	1069
WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_2	1069
WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_3	1069
WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_4	1070
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WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_10	1072
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WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_2	1072
WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_3	1073
WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_4	1073
WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_5	1073
WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_6	1074

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_7	1074
WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_8	1074
WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_9	1075
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WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_0	1075
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WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_2	1076
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WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_5	1077
WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_6	1077
WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_7	1078
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WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_9	1082
WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_10	1082
WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_0	1082
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WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_8	1085
WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_9	1085
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WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_7	1088
WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_8	1088
WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_9	1089
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WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_4	1094
WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_5	1094
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WAV_CH1_CA__DQ_TX_BSCAN_CFG	1099
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_0	1099
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_1	1099
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_2	1099
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_3	1099
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_4	1099
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_5	1100
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_6	1100
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_7	1100
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_8	1100
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_9	1100
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_10	1100
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_0	1101
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WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_9	1102
WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_10	1102
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_0	1102
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_1	1103
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_2	1103
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WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_4	1103
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_5	1103
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_6	1103
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_7	1104
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_8	1104
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_9	1104

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WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_0	1104
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_1	1104
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_2	1105
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_3	1105
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_4	1105
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_5	1105
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_6	1105
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_7	1105
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_8	1106
WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_9	1106
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WAV_CH1_CA__DQ_TX_ODR_PI_M0_R1_CFG	1106
WAV_CH1_CA__DQ_TX_ODR_PI_M1_R0_CFG	1106
WAV_CH1_CA__DQ_TX_ODR_PI_M1_R1_CFG	1107
WAV_CH1_CA__DQ_TX_QDR_PI_0_M0_R0_CFG	1107
WAV_CH1_CA__DQ_TX_QDR_PI_0_M0_R1_CFG	1107
WAV_CH1_CA__DQ_TX_QDR_PI_0_M1_R0_CFG	1107
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WAV_CH1_CA__DQ_TX_QDR_PI_1_M0_R0_CFG	1108
WAV_CH1_CA__DQ_TX_QDR_PI_1_M0_R1_CFG	1108
WAV_CH1_CA__DQ_TX_QDR_PI_1_M1_R0_CFG	1108
WAV_CH1_CA__DQ_TX_QDR_PI_1_M1_R1_CFG	1108
WAV_CH1_CA__DQ_TX_DDR_PI_0_M0_R0_CFG	1109
WAV_CH1_CA__DQ_TX_DDR_PI_0_M0_R1_CFG	1109
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WAV_CH1_CA__DQ_TX_RT_M0_R0_CFG	1111
WAV_CH1_CA__DQ_TX_RT_M0_R1_CFG	1111

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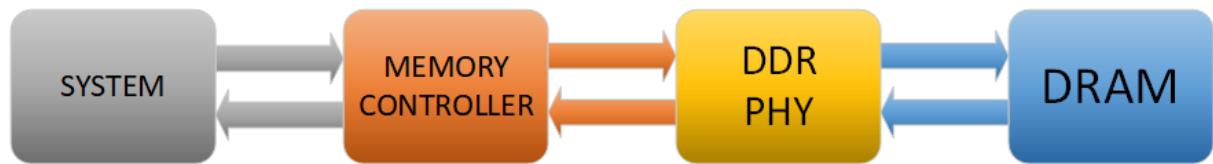
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WAV_CH1_CA__DQS_TX_IO_CMN_M0_R1_CFG	1230

WAV_CH1_CA__DQS_TX_IO_CMN_M1_R0_CFG	1230
WAV_CH1_CA__DQS_TX_IO_CMN_M1_R1_CFG	1230
License	1231
BSD license	1231
MIT license	1231
How to request help?	1232
Indices and tables	1233

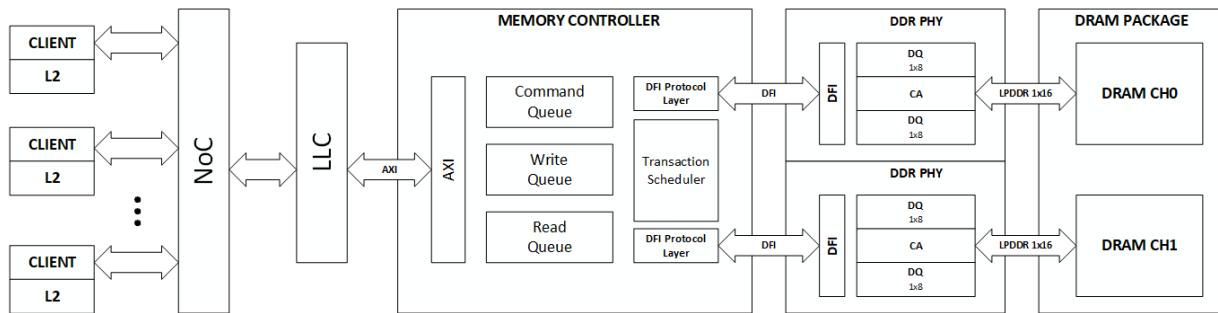
WDDR Documentation



Overview

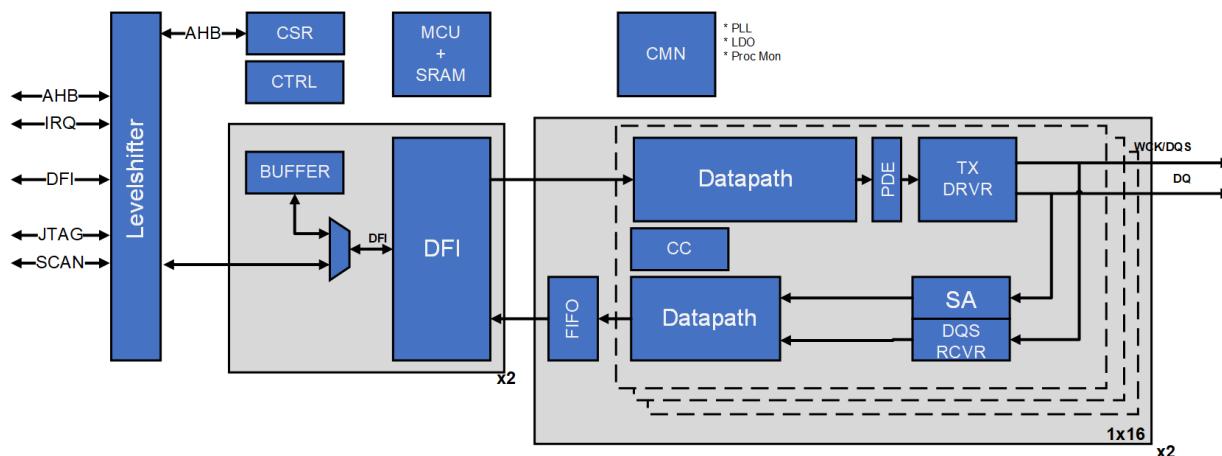
In modern System-On-Chip (SoC) platforms a low-latency and high-bandwidth path to DRAM is critical to meet CPU, GPU, and NPU workloads and performance requirements.

The DDR Physical Interface (PHY) IP provides an interface to external DRAM and is an important component to meet system performance requirements.



System Block Diagram

The Wavious DDR PHY (WDDDR) is designed to be a scalable, high performance, low power, and low area PHY that is compliant to multiple JEDEC specifications.



DDR PHY Top Level Block Diagram

Features

The DDR PHY supports the following features:

- LPDDR4x compliant interface @4266Mbps
- LPDDR5 compliant interface @6400Mbps
- DFIv5.0 compliant Memory Controller interface
- AHB-Lite configuration interface
- Fast frequency switching
- Embedded low-jitter PLL
- Embedded RISC-V MCU + SRAM
- Self-contained training and calibration
- Easily portable to various technology nodes

Overview

- Parameterizable pipeline stages for ease of timing closure
- Power states and clock gating

Integration

The Wavious DDR PHY supports LPDDR4x and LPDDR5 standards and is provided in a 1x32 configuration (Memory Controller side) consisting of two 1x16 channels (DRAM side). The 1x32 channel configuration is chosen to mitigate MCU+SRAM area overhead to DRAM interface width.

Note

- LPDDR5 configuration support may be limited in current release version.
- 1x16 configuration may be supported in a future release version.
- HBM configuration may be supported in a future release version.

Design Files

```

./rtl
|-- ahb
|   |-- wav_ahb.sv
|   |   `-- wav_ahb_pkg.sv
|-- component
|   `-- wav_component_lib.sv
-- custom_ip
|   |-- wphy_2to1_14g_rvt.sv
|   |-- wphy_cgc_diff_lvt.sv
|   |-- wphy_cgc_diff_rh_lvt.sv
|   |-- wphy_cgc_diff_rh_svt.sv
|   |-- wphy_cgc_diff_svt.sv
|   |-- wphy_clk_div_2ph_4g_dlymatch_lvt.sv
|   |-- wphy_clk_div_2ph_4g_dlymatch_svt.sv
|   |-- wphy_clk_div_2ph_4g_lvt.sv
|   |-- wphy_clk_div_2ph_4g_svt.sv
|   |-- wphy_clk_div_4ph_10g_dlymatch_svt.sv
|   |-- wphy_clk_div_4ph_10g_svt.sv
|   |-- wphy_clkmux_3to1_diff.sv
|   |-- wphy_clkmux_diff.sv
|   |-- wphy_gfcm_lvt.sv
|   |-- wphy_gfcm_svt.sv
|   |-- wphy_pi_4g.sv
|   |-- wphy_pi_dly_match_4g.sv
|   |-- wphy_prog_dly_se_4g.sv
|   |-- wphy_prog_dly_se_4g_small.sv
|   '-- wphy_sa_4g_2ph_pdly_no_esd.sv
-- ddr_ip
|   |-- wphy_lp4x5_cke_drvr_w_lpbk.sv
|   |-- wphy_lp4x5_cmn.sv
|   |-- wphy_lp4x5_cmn_clks_svt.sv
|   |-- wphy_lp4x5_dq_drvr_w_lpbk.sv
|   |-- wphy_lp4x5_dqs_drvr_w_lpbk.sv
|   '-- wphy_lp4x5_dqs_rcvr_no_esd.sv
-- ibex
|   |-- ibex_alu.sv
|   |-- ibex_branch_predict.sv
|   |-- ibex_compressed_decoder.sv
|   |-- ibex_controller.sv
|   |-- ibex_core.sv
|   |-- ibex_counter.sv
|   |-- ibex_cs_registers.sv
|   |-- ibex_csr.sv
|   |-- ibex_decoder.sv
|   |-- ibex_ex_block.sv
|   |-- ibex_fetch_fifo.sv
|   |-- ibex_id_stage.sv
|   |-- ibex_if_stage.sv
|   |-- ibex_load_store_unit.sv
|   |-- ibex_multdiv_fast.sv
|   |-- ibex_multdiv_slow.sv
|   |-- ibex_pkg.sv
|   |-- ibex_pmp.sv
|   |-- ibex_prefetch_buffer.sv
|   |-- ibex_register_file_ff.sv
|   |-- ibex_wb_stage.sv
|   '-- prim_assert.sv
|       |-- prim_assert_dummy_macros.svh
|       '-- prim_assert_standard_macros.svh
-- jtag
    `-- wav_jtag_lib.sv
-- mcu_ibex

```

Integration

```
-- prim_clock_gating.sv
|-- wav_mcu_ahb_csr.sv
|-- wav_mcu_csr.sv
|-- wav_mcu_csr_defs.vh
|-- wav_mcu_ibex.sv
|-- wav_mcu_pkg.sv
|-- wav_mcuintf_ahb_csr.sv
|-- wav_mcuintf_csr.sv
|-- wav_mcuintf_csr_defs.vh
|-- wav_mcutoff_ahb_csr.sv
|-- wav_mcutoff_csr.sv
`-- wav_mcutoff_csr_defs.vh
-- mvp_pll
|-- mvp_fll.v
|-- mvp_pll_clk_control.v
|-- mvp_pll_dig.v
|-- mvp_pll_regs_top.v
|-- mvp_pll_sm.v
|-- mvp_sync_pulse.v
|-- wav_reg_model_mvp_pll.svh
`-- wav_reg_model_mvp_pll_no_reg_test.svh
-- mvppll_ip
`-- wphy_rpll_mvp_4g.sv
-- pll_shared
`-- wav_pll_shared_lib.v
-- tech
|-- ddr_stdcell_lib.sv
|-- wav_legacy_stdcell_lib.v
`-- wav_stdcell_lib.sv
`-- wav_tcm_sp.sv
-- wddr
|-- Wpin_uart_lib.sv
|-- ddr_2to1_wrapper.sv
|-- ddr_ahb.sv
|-- ddr_ca_ahb_csr.sv
|-- ddr_ca_csr.sv
`-- ddr_ca_csr_defs.vh
`-- ddr_ca_csr_wrapper.sv
|-- ddr_cke_drvr_lpbk_wrapper.sv
`-- ddr_cke_drvr_lpbk_wrapper_cmn_define.vh
`-- ddr_cke_drvr_lpbk_wrapper_define.vh
`-- ddr_clkmux_3to1_diff_wrapper.sv
`-- ddr_clkmux_diff_wrapper.sv
`-- ddr_clkmux_diff_wrapper_define.vh
`-- ddr_cmn.sv
`-- ddr_cmn_ahb_csr.sv
`-- ddr_cmn_csp_define.vh
`-- ddr_cmn_csr.sv
`-- ddr_cmn_csr_defs.vh
`-- ddr_cmn_wrapper.sv
`-- ddr_cmn_wrapper_define.vh
`-- ddr_component_lib.sv
`-- ddr_ctrl_ahb_csr.sv
`-- ddr_ctrl_csr.sv
`-- ddr_ctrl_csr_defs.vh
`-- ddr_ctrl_plane.sv
`-- ddr_custom_lib.sv
`-- ddr_dfi.sv
`-- ddr_dfi_ahb_csr.sv
`-- ddr_dfi_csr.sv
`-- ddr_dfi_csr_defs.vh
`-- ddr_dfich_ahb_csr.sv
`-- ddr_dfich_csr.sv
`-- ddr_dfich_csr_defs.vh
`-- ddr_dp.sv
`-- ddr_dq_ahb_csr.sv
`-- ddr_dq_csr.sv
`-- ddr_dq_csr_defs.vh
`-- ddr_dq_csr_wrapper.sv
`-- ddr_dq_drvr_lpbk_wrapper.sv
`-- ddr_dq_drvr_lpbk_wrapper_cmn_define.vh
`-- ddr_dq_drvr_lpbk_wrapper_define.vh
`-- ddr_dq_task.svh
`-- ddr_dqs_drvr_lpbk_wrapper.sv
`-- ddr_dqs_drvr_lpbk_wrapper_cmn_define.vh
`-- ddr_dqs_drvr_lpbk_wrapper_define.vh
`-- ddr_dqs_rcvr_no_esd_wrapper.sv
`-- ddr_dqs_rcvr_wrapper_cmn_define.vh
`-- ddr_dqs_rcvr_wrapper_define.vh
`-- ddr_fifo.sv
`-- ddr_fsw_ahb_csr.sv
`-- ddr_fsw_csr.sv
`-- ddr_fsw_csr_defs.vh
`-- ddr_global_define.vh
`-- ddr_global_pkg.sv
`-- ddr_phy.sv
`-- ddr_phy_1x32.sv
`-- ddr_pi_b2t_dec.sv
`-- ddr_pi_match_wrapper.sv
`-- ddr_pi_match_wrapper_define.vh
```

Integration

```
-- ddr_pi_small_wrapper_define.vh  
|-- ddr_pi_wrapper.sv  
|-- ddr_pi_wrapper_define.vh  
|-- ddr_pmon_dig.sv  
|-- ddr_pmon_freqdet.sv  
|-- ddr_prog_dly_dec.sv  
|-- ddr_prog_dly_se_small_wrapper.sv  
|-- ddr_prog_dly_se_wrapper.sv  
|-- ddr_prog_dly_se_wrapper_define.vh  
|-- ddr_prog_dly_wrapper_define.vh  
|-- ddr_project_define.vh  
|-- ddr_project_vpp.vhh  
|-- ddr_rx.sv  
|-- ddr_sa_2ph_pdly_no_esd_wrapper.sv  
|-- ddr_sa_2ph_pdly_wrapper_define.vh  
|-- ddr_sa_2ph_wrapper_cmn_define.vh  
|-- ddr_sa_2ph_wrapper_define.vh  
|-- ddr_sa_4ph_wrapper_cmn_define.vh  
|-- ddr_sa_4ph_wrapper_define.vh  
|-- ddr_snoop.sv  
`-- ddr_tx.sv
```

12 directories, 160 files

Configurations

- Protocol: LP4x, LP5
- Channels: 1x16, 2x16, 4x16, 1x32, etc.
- Frequency (MHz): 422.4, 806.4, 1612.8, 2112, 3187.2, etc.
- Frequency Ratio: 1:2, 1:4
- Rank: Single, dual
- Signaling: Terminated/unterminated, differential/single-ended (CK, WCK)

Note

- Frequencies are not limit of those listed.
- LPDDR5 configuration support may be limited in current release version.
- 1:1 and 1:8 frequency ratio may be supported in future release version.
- Currently, only the 1x32 channel configuration is available. Other configurations may be supported in future release version.

Ports

The Wavious DDR PHY standard interfaces include: 1149.1 TAP, DFIv5.0, AHB-Lite, and LPDDR4x/LPDDR5. For specific signal descriptions and functions, please refer to the interface protocol specifications.

Port Name	Direction	Width	Description
Global Clocks and Reset			
i_phy_rst	input	1	Global PHY reset
i_refclk	input	1	Reference clock @38.4Mhz
o_refclk_on	output	1	Reference clock on request
i_refclk_alt	input	1	Reference clock alternative
Test			
i_gpb	input	[7:0]	General purpose bus

Integration

o_gpb	output	[7:0]	General purpose bus
o_debug	output	[31:0]	Debug bus (low frequency)
i_freeze_n	input	1	Freeze IO (active low)
i_hiz_n	input	1	High impedance (active low)
i_iddq_mode	input	1	IDDQ mode enable
o_dtst	output	1	Digital clock test (high frequency)
Interrupts			
i_irq	input	[3:0]	Interrupt
o_irq	output	[1:0]	Interrupt
DFT			
i_scan_mode	input	1	Scan mode enable
i_scan_clk	input	1	Scan clock
i_scan_en	input	1	Scan shift enable
i_scan_freq_en	input	[7:0]	Scan clock tree frequency enable
i_scan_cgc_ctrl	input	1	CGC override enable
i_scan_RST_ctrl	input	1	Reset override enable
i_scan_set_ctrl	input	1	Set override enable
i_scan	input	[15:0]	Scan chain in
o_scan	output	[15:0]	Scan chain out
TAP			
i_jtag_tck	input	1	
i_jtag_trst_n	input	1	
i_jtag_tms	input	1	
i_jtag_tdi	input	1	
o_jtag_tdo	output	1	
AHB			
i_ahb_clk	input	1	
o_ahb_clk_on	output	1	AHB clock on request
i_ahb_rst	input	1	
i_ahb_CSR_rst	input	1	AHB CSR reset
AHB Slave			
i_ahb_haddr	input	[31:0]	
i_ahb_hwrite	input	1	
i_ahb_hsel	input	1	
i_ahb_hwdata	input	[31:0]	
i_ahb_htrans	input	[1:0]	
i_ahb_hsize	input	[2:0]	
i_ahb_hburst	input	[2:0]	
i_ahb_hreadyin	input	1	HREADY
o_ahb_hready	output	1	HREADYOUT
o_ahb_hrdata	output	[31:0]	
o_ahb_hresp	output	[1:0]	

Integration

AHB Master			
o_ahb_haddr	output	[31:0]	
o_ahb_hwrite	output	1	
o_ahb_hwdata	output	[31:0]	
o_ahb_htrans	output	[1:0]	
o_ahb_hsize	output	[2:0]	
o_ahb_hburst	output	[2:0]	
o_ahb_hbusreq	output	1	
i_ahb_hgrant	input	1	
i_ahb_hready	input	1	
i_ahb_hrdata	input	[31:0]	
i_ahb_hresp	input	[1:0]	
DFI V5.0			
i_dfi_clk_on	input	1	DFI clock on request
o_dfi_clk	output	1	
o_dfi_ctrlupd_ack	output	1	
i_dfi_ctrlupd_req	input	1	
i_dfi_phyupd_ack	input	1	
o_dfi_phyupd_req	output	1	
o_dfi_phyupd_type	output	[1:0]	
i_dfi_freq_fsp	input	[1:0]	
i_dfi_freq_ratio	input	[1:0]	
i_dfi_frequency	input	[4:0]	
o_dfi_init_complete	output	1	
i_dfi_init_start	input	1	
i_dfi_phymstr_ack	input	1	
o_dfi_phymstr_cs_state	output	[1:0]	
o_dfi_phymstr_req	output	1	
o_dfi_phymstr_state_sel	output	1	
o_dfi_phymstr_type	output	[1:0]	
o_dfi_lp_ctrl_ack	output	1	
i_dfi_lp_ctrl_req	input	1	
i_dfi_lp_ctrl_wakeup	input	[5:0]	
o_dfi_lp_data_ack	output	1	
i_dfi_lp_data_req	input	1	
i_dfi_lp_data_wakeup	input	[5:0]	
i_dfi_reset_n_p0	input	1	
i_dfi_reset_n_p1	input	1	
i_dfi_reset_n_p2	input	1	
i_dfi_reset_n_p3	input	1	
i_dfi_address_p0	input	[13:0]	
i_dfi_address_p1	input	[13:0]	

Integration

i_dfi_address_p2	input	[13:0]	
i_dfi_address_p3	input	[13:0]	
i_dfi_cke_p0	input	[1:0]	
i_dfi_cke_p1	input	[1:0]	
i_dfi_cke_p2	input	[1:0]	
i_dfi_cke_p3	input	[1:0]	
i_dfi_cs_p0	input	[1:0]	
i_dfi_cs_p1	input	[1:0]	
i_dfi_cs_p2	input	[1:0]	
i_dfi_cs_p3	input	[1:0]	
i_dfi_dram_clk_disable_p0	input	1	
i_dfi_dram_clk_disable_p1	input	1	
i_dfi_dram_clk_disable_p2	input	1	
i_dfi_dram_clk_disable_p3	input	1	
i_dfi_wrdata_p0	input	[63:0]	
i_dfi_wrdata_p1	input	[63:0]	
i_dfi_wrdata_p2	input	[63:0]	
i_dfi_wrdata_p3	input	[63:0]	
i_dfi_parity_in_p0	input	1	
i_dfi_parity_in_p1	input	1	
i_dfi_parity_in_p2	input	1	
i_dfi_parity_in_p3	input	1	
i_dfi_wrdata_cs_p0	input	[1:0]	
i_dfi_wrdata_cs_p1	input	[1:0]	
i_dfi_wrdata_cs_p2	input	[1:0]	
i_dfi_wrdata_cs_p3	input	[1:0]	
i_dfi_wrdata_mask_p0	input	[7:0]	
i_dfi_wrdata_mask_p1	input	[7:0]	
i_dfi_wrdata_mask_p2	input	[7:0]	
i_dfi_wrdata_mask_p3	input	[7:0]	
i_dfi_wrdata_en_p0	input	1	
i_dfi_wrdata_en_p1	input	1	
i_dfi_wrdata_en_p2	input	1	
i_dfi_wrdata_en_p3	input	1	
i_dfi_wck_cs_p0	input	[1:0]	
i_dfi_wck_cs_p1	input	[1:0]	
i_dfi_wck_cs_p2	input	[1:0]	
i_dfi_wck_cs_p3	input	[1:0]	
i_dfi_wck_en_p0	input	1	
i_dfi_wck_en_p1	input	1	
i_dfi_wck_en_p2	input	1	
i_dfi_wck_en_p3	input	1	

Integration

i_dfi_wck_toggle_p0	input	[1:0]	
i_dfi_wck_toggle_p1	input	[1:0]	
i_dfi_wck_toggle_p2	input	[1:0]	
i_dfi_wck_toggle_p3	input	[1:0]	
i_dfi_rddata_cs_p0	input	[1:0]	
i_dfi_rddata_cs_p1	input	[1:0]	
i_dfi_rddata_cs_p2	input	[1:0]	
i_dfi_rddata_cs_p3	input	[1:0]	
i_dfi_rddata_en_p0	input	1	
i_dfi_rddata_en_p1	input	1	
i_dfi_rddata_en_p2	input	1	
i_dfi_rddata_en_p3	input	1	
o_dfi_rddata_db1_w0	output	[7:0]	
o_dfi_rddata_db1_w1	output	[7:0]	
o_dfi_rddata_db1_w2	output	[7:0]	
o_dfi_rddata_db1_w3	output	[7:0]	
o_dfi_rddata_w0	output	[63:0]	
o_dfi_rddata_w1	output	[63:0]	
o_dfi_rddata_w2	output	[63:0]	
o_dfi_rddata_w3	output	[63:0]	
o_dfi_rddata_valid_w0	output	1	
o_dfi_rddata_valid_w1	output	1	
o_dfi_rddata_valid_w2	output	1	
o_dfi_rddata_valid_w3	output	1	
LPDDR4x/LPDDR5			
pad_ddr_rext	inout	1	Connect to 240 Ohm resistor
pad_ddr_test	inout	1	High frequency test pad
pad_ddr_reset_n	inout	1	
pad_ch0_ddr_ca_ca0	inout	1	
pad_ch0_ddr_ca_ca1	inout	1	
pad_ch0_ddr_ca_ca2	inout	1	
pad_ch0_ddr_ca_ca3	inout	1	
pad_ch0_ddr_ca_ca4	inout	1	
pad_ch0_ddr_ca_ca5	inout	1	
pad_ch0_ddr_ca_ca6	inout	1	LPDDR5 only
pad_ch0_ddr_ca_cs0	inout	1	
pad_ch0_ddr_ca_cs1	inout	1	
pad_ch0_ddr_ca_cke0	inout	1	LPDDR4x only
pad_ch0_ddr_ca_cke1	inout	1	LPDDR4x only
pad_ch0_ddr_ca_ck_c	inout	1	
pad_ch0_ddr_ca_ck_t	inout	1	
pad_ch0_ddr_dq0_dbim	inout	1	

Integration

pad_ch0_ddr_dq0_dq0	inout	1	
pad_ch0_ddr_dq0_dq1	inout	1	
pad_ch0_ddr_dq0_dq2	inout	1	
pad_ch0_ddr_dq0_dq3	inout	1	
pad_ch0_ddr_dq0_dq4	inout	1	
pad_ch0_ddr_dq0_dq5	inout	1	
pad_ch0_ddr_dq0_dq6	inout	1	
pad_ch0_ddr_dq0_dq7	inout	1	
pad_ch0_ddr_dq0_wck_c	inout	1	LPDDR5 only
pad_ch0_ddr_dq0_wck_t	inout	1	LPDDR5 only
pad_ch0_ddr_dq0_dqs_c	inout	1	
pad_ch0_ddr_dq0_dqs_t	inout	1	
pad_ch0_ddr_dq1_dbim	inout	1	
pad_ch0_ddr_dq1_dq0	inout	1	
pad_ch0_ddr_dq1_dq1	inout	1	
pad_ch0_ddr_dq1_dq2	inout	1	
pad_ch0_ddr_dq1_dq3	inout	1	
pad_ch0_ddr_dq1_dq4	inout	1	
pad_ch0_ddr_dq1_dq5	inout	1	
pad_ch0_ddr_dq1_dq6	inout	1	
pad_ch0_ddr_dq1_dq7	inout	1	
pad_ch0_ddr_dq1_wck_c	inout	1	LPDDR5 only
pad_ch0_ddr_dq1_wck_t	inout	1	LPDDR5 only
pad_ch0_ddr_dq1_dqs_c	inout	1	
pad_ch0_ddr_dq1_dqs_t	inout	1	
pad_ch1_ddr_ca_ca0	inout	1	
pad_ch1_ddr_ca_ca1	inout	1	
pad_ch1_ddr_ca_ca2	inout	1	
pad_ch1_ddr_ca_ca3	inout	1	
pad_ch1_ddr_ca_ca4	inout	1	
pad_ch1_ddr_ca_ca5	inout	1	
pad_ch1_ddr_ca_ca6	inout	1	LPDDR5 only
pad_ch1_ddr_ca_cs0	inout	1	
pad_ch1_ddr_ca_cs1	inout	1	
pad_ch1_ddr_ca_cke0	inout	1	LPDDR4x only
pad_ch1_ddr_ca_cke1	inout	1	LPDDR4x only
pad_ch1_ddr_ca_ck_c	inout	1	
pad_ch1_ddr_ca_ck_t	inout	1	
pad_ch1_ddr_dq0_dbim	inout	1	
pad_ch1_ddr_dq0_dq0	inout	1	
pad_ch1_ddr_dq0_dq1	inout	1	
pad_ch1_ddr_dq0_dq2	inout	1	

Integration

pad_ch1_ddr_dq0_dq3	inout	1	
pad_ch1_ddr_dq0_dq4	inout	1	
pad_ch1_ddr_dq0_dq5	inout	1	
pad_ch1_ddr_dq0_dq6	inout	1	
pad_ch1_ddr_dq0_dq7	inout	1	
pad_ch1_ddr_dq0_wck_c	inout	1	LPDDR5 only
pad_ch1_ddr_dq0_wck_t	inout	1	LPDDR5 only
pad_ch1_ddr_dq0_dqs_c	inout	1	
pad_ch1_ddr_dq0_dqs_t	inout	1	
pad_ch1_ddr_dq1_dbim	inout	1	
pad_ch1_ddr_dq1_dq0	inout	1	
pad_ch1_ddr_dq1_dq1	inout	1	
pad_ch1_ddr_dq1_dq2	inout	1	
pad_ch1_ddr_dq1_dq3	inout	1	
pad_ch1_ddr_dq1_dq4	inout	1	
pad_ch1_ddr_dq1_dq5	inout	1	
pad_ch1_ddr_dq1_dq6	inout	1	
pad_ch1_ddr_dq1_dq7	inout	1	
pad_ch1_ddr_dq1_wck_c	inout	1	LPDDR5 only
pad_ch1_ddr_dq1_wck_t	inout	1	LPDDR5 only
pad_ch1_ddr_dq1_dqs_c	inout	1	
pad_ch1_ddr_dq1_dqs_t	inout	1	

Interfaces

AHB-Lite Slave Interface

The AHB slave interface is used for configuration and status register access. The AHB slave interface does not support HPROT or HMASTLOCK signals.

AHB-Lite Master Interface

The DDR PHY's AHB master interface enables the embedded RISC-V MicroController Unit (MCU) to control PHY-external logic, such as, Memory Controller interfaces and CSRs, sensors, etc. The AHB master interface does not support HPROT or HMASTLOCK signals.

DFIv5.0 Interface

The DFIv5.0 compliant interface provides connectivity to a compatible Memory Controller. The DDR PHY uses an embedded PLL to generate a low jitter DRAM clock and provides a DFI clock to the Memory Controller.

The DDR PHY supports the following DFI features.

- 1:2 and 1:4 frequency ratios

The DDR PHY currently does not support the following DFI features.

Integration

- Error interface
- Message interface
- ODT signal

LPDDR4x Interface

The LPDDR4x compliant interface supports up to two 1x16 channels and two ranks. The DDR PHY does not support the ODT output pin. DRAM termination shall be set through MRW.

LPDDR5 Interface

The LPDDR5 compliant interface supports up to two 1x16 channels and two ranks. The DDR PHY does not support the ODT output pin. DRAM termination shall be set through MRW.

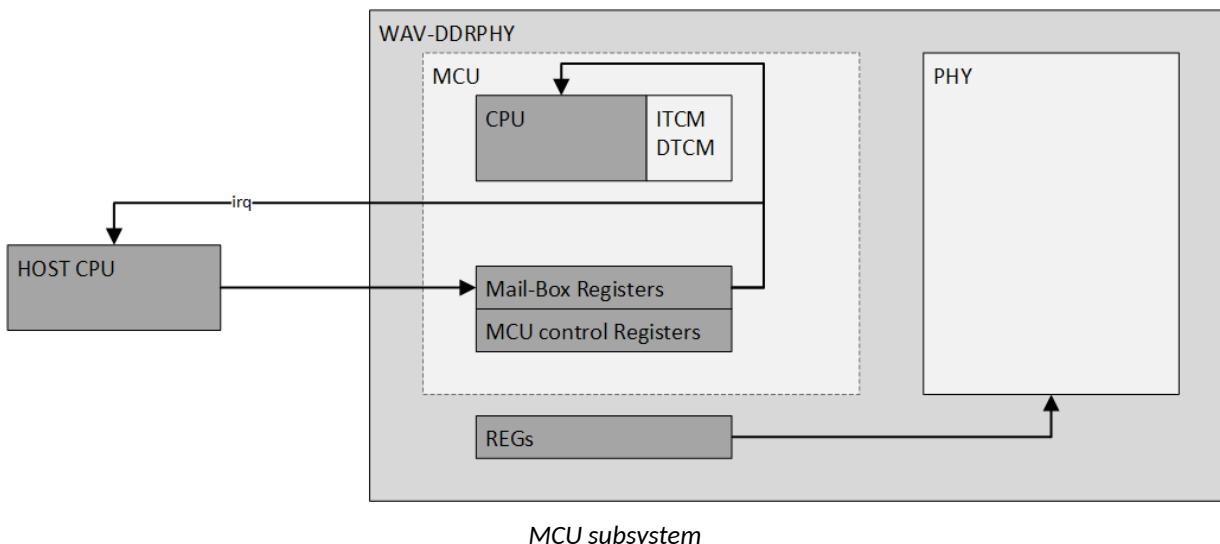
Software

This section describes the programmers model for WDDR. As described earlier, the WDDR Physical Interface (PHY) IP includes an integrated RISC-V MCU and dedicated SRAM for ITCM and DTCM. A software binary for the MCU is included with the WDDR hardware release.

MCU subsystem

- MCU core is lowRISC 32 bit ibex core (<https://github.com/lowRISC/ibex>)
- 64 kB ITCM
- 64 kB DTCM
- Mailbox communication with HOST
 - HOST to MCU mailbox
 - MCU to HOST mailbox
- Control registers for MCU

The high level description of MCU subsystem from software point of view is shown below.



Mailbox Communication

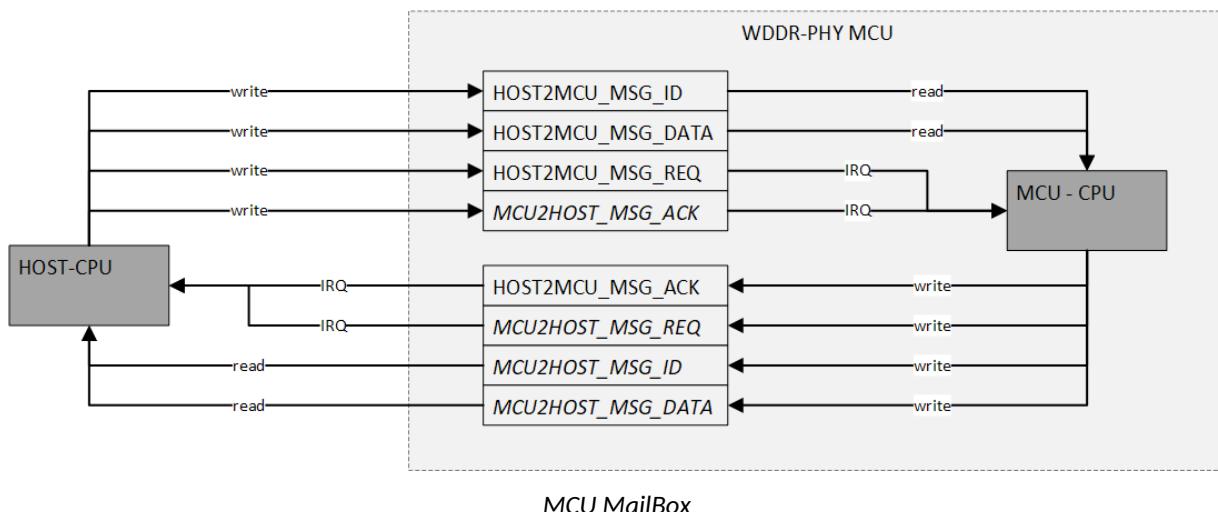
A four-register mailbox is supported to allow a HOST to send messages to the MCU:

- WAV_MCU_MCUINTF_HOST2MCU_MSG_DATA
- WAV_MCU_MCUINTF_HOST2MCU_MSG_ID
- WAV_MCU_MCUINTF_HOST2MCU_MSG_REQ
- WAV_MCU_MCUINTF_HOST2MCU_MSG_ACK

A four-register mailbox is supported to allow the MCU to send messages to a HOST:

- WAV_MCU_MCUINTF_MCU2HOST_MSG_DATA
- WAV_MCU_MCUINTF_MCU2HOST_MSG_ID
- WAV_MCU_MCUINTF_MCU2HOST_MSG_REQ
- WAV_MCU_MCUINTF_MCU2HOST_MSG_ACK

Software



The procedure to send a message from HOST to MCU is listed below:

1. HOST sets registers **HOST2MCU_MSG_ID** and **HOST2MCU_MSG_DATA** with required ID and DATA (list of supported ID/DATA is described below).
2. HOST sets **HOST2MCU_MSG_REQ**=0x1 to indicate that MCU mailbox has a message.
3. MCU will read **HOST2MCU_MSG_ID** and **HOST2MCU_MSG_DATA**.
4. MCU will clear **HOST2MCU_MSG_REQ**=0x0 and set **HOST2MCU_MSG_ACK**=0x1 acknowledging to the HOST that message has been received.
5. HOST need to clear **HOST2MCU_MSG_ACK**=0x0.

Supported Messages

Messages from HOST to MCU

Name	HOST2MCU_M SG_ID	HOST2MCU_M SG_DATA	Description	Response HOST 2MCU_MSG_ID
SW-version-req	0x2	N/A	Report SW version	0x2
BOOT-start	0x3	N/A	Start Booting Process	0x3

Messages from MCU to HOST

Name	MCU2HOST_ MSG_ID	MCU2HOST_ MSG_DATA	Description
SW-ready	0x1	N/A	MCU indicates to HOST that SW is initialized and ready to accept messages
SW-version-rsp	0x2	\$version	MCU will return SW \$version currently running on MCU
BOOT-done	0x3	\$return	MCU will send this message to indicate \$return = 0, boot completed with success, \$return = err, boot completed with error

Boot procedure (from HOST level)

The boot procedure is listed in the order below:

1. Clear reset to WDDR.
2. Move ITCM image to ITCM address 0x10000.

Software

3. Move DTCM image to DTCM address 0x50000.
4. Enable MCU by setting FETCH_EN=0x1 within WAV_MCU__MCUTOP__CFG.
5. Wait until message SW-ready is received.
6. If desired, send SW-version-req message and wait for MCU to report SW-version-rsp.
7. Send BOOT-start message to MCU.
8. Wait till Boot-done message is received.

Registers

Registers

WAV_MCU__MCUTOP__RSVD

Address: 0x00000000

Description:

Name	Index	Type	Reset	Description
RSVD	[31:0]	RW	0x0	TBD.

WAV_MCU__MCUTOP__CFG

Address: 0x00000004

Description:

Name	Index	Type	Reset	Description
DEBUG_EN	[1]	RW	0x0	Enable Debug mode.
FETCH_EN	[0]	RW	0x0	Enable CPU fetch.

WAV_MCU__MCUTOP__STA

Address: 0x00000008

Description:

Name	Index	Type	Reset	Description
RESERVED	[31:0]	R	0x0	Reserved

WAV_MCU__MCUINTF__HOST2MCU_MSG_DATA

Address: 0x00004000

Description:

Name	Index	Type	Reset	Description
DATA	[31:0]	RW	0x0	Refer to SW documentation.

WAV_MCU__MCUINTF__HOST2MCU_MSG_ID

Address: 0x00004004

Description:

Name	Index	Type	Reset	Description
ID	[31:0]	RW	0x0	Refer to SW documentation.

WAV_MCU__MCUINTF__HOST2MCU_MSG_REQ

Address: 0x00004008

Description:

Name	Index	Type	Reset	Description
REQ	[0]	W1T	0x0	Refer to SW documentation.

WAV_MCU__MCUINTF__HOST2MCU_MSG_ACK

Registers

Address: 0x0000400C

Description:

Name	Index	Type	Reset	Description
ACK	[0]	W1T	0x0	Refer to SW documentation.

WAV MCU _MCUINTF__MCU2HOST_MSG_DATA

Address: 0x00004010

Description:

Name	Index	Type	Reset	Description
DATA	[31:0]	RW	0x0	Refer to SW documentation.

WAV MCU _MCUINTF__MCU2HOST_MSG_ID

Address: 0x00004014

Description:

Name	Index	Type	Reset	Description
ID	[31:0]	RW	0x0	Refer to SW documentation.

WAV MCU _MCUINTF__MCU2HOST_MSG_REQ

Address: 0x00004018

Description:

Name	Index	Type	Reset	Description
REQ	[0]	W1T	0x0	Refer to SW documentation.

WAV MCU _MCUINTF__MCU2HOST_MSG_ACK

Address: 0x0000401C

Description:

Name	Index	Type	Reset	Description
ACK	[0]	W1T	0x0	Refer to SW documentation.

WAV MCU _MCU_ IRQ_FAST_CLR_CFG

Address: 0x00008000

Description:

Name	Index	Type	Reset	Description
CLR	[31:0]	WC	0x0000000	Clear interrupt.

WAV MCU _MCU_ IRQ_FAST_STICKY_CFG

Address: 0x00008004

Description:

Name	Index	Type	Reset	Description

Registers

EN	[31:0]	RW	0x00000 0	Enable sticky register.
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WAV_MCU__MCU__IRQ_FAST_MSK_CFG

Address: 0x00008008

Description:

Name	Index	Type	Reset	Description
MSK	[31:0]	RW	0x00000 0	Mask interrupt.

WAV_MCU__MCU__IRQ_FAST_SYNC_CFG

Address: 0x0000800C

Description:

Name	Index	Type	Reset	Description
EN	[31:0]	RW	0x00000 0	Enable synchronize to mcu clk.

WAV_MCU__MCU__IRQ_FAST_EDGE_CFG

Address: 0x00008010

Description:

Name	Index	Type	Reset	Description
EN	[31:0]	RW	0x00000 0	Enable detecting a rising edge on IRQ.

WAV_MCU__MCU__IRQ_FAST_STA

Address: 0x00008014

Description:

Name	Index	Type	Reset	Description
IRQ_STA	[31:0]	R	0x00000 0	Interrupt status.

WAV_MCU__MCU__MSIP_CFG

Address: 0x00008018

Description:

Name	Index	Type	Reset	Description
INTERRUPT	[0]	RW	0x0	MCU SW interrupt.

WAV_MCU__MCU__MTIME_LO_STA

Address: 0x0000801C

Description:

Name	Index	Type	Reset	Description
TIME_LO	[31:0]	R	0x0	Lower 32 bit value of a 64 bit timer in ref clock cycles.

Registers

WAV_MCU__MCU__MTIME_HI_STA

Address: 0x00008020

Description:

Name	Index	Type	Reset	Description
TIME_HI	[31:0]	R	0x0	Higher 32 bit value of a 64 bit timer in ref clock cycles.

WAV_MCU__MCU__MTIMECMP_LO_CFG

Address: 0x00008024

Description:

Name	Index	Type	Reset	Description
TIMECMP_LO	[31:0]	RW	0x0	Lower 32 bit value of a 64 bit timer compare value in ref clock cycles.

WAV_MCU__MCU__MTIMECMP_HI_CFG

Address: 0x00008028

Description:

Name	Index	Type	Reset	Description
TIMECMP_HI	[31:0]	RW	0x0	Higher 32 bit value of a 64 bit timer compare value in ref clock cycles.

WAV_MCU__MCU__MTIMECMP_CFG

Address: 0x0000802C

Description:

Name	Index	Type	Reset	Description
LOAD	[0]	W1T	0x0	Toggle this bit to indicate a new compare value is available.

WAV_MCU__MCU__MTIME_CFG

Address: 0x00008030

Description:

Name	Index	Type	Reset	Description
ENABLE	[0]	RW	0x1	When set high enable timer.

WAV_MCU__MCU__GP0_CFG

Address: 0x00008034

Description:

Name	Index	Type	Reset	Description
RESERVED	[31:0]	RW	0x0	Reserved.

WAV_MCU__MCU__GP1_CFG

Address: 0x00008038

Description:

Registers

Name	Index	Type	Reset	Description
RESERVED	[31:0]	RW	0x0	Reserved.

WAV_MCU__MCU__GP2_CFG

Address: 0x0000803C

Description:

Name	Index	Type	Reset	Description
RESERVED	[31:0]	RW	0x0	Reserved.

WAV_MCU__MCU__GP3_CFG

Address: 0x00008040

Description:

Name	Index	Type	Reset	Description
RESERVED	[31:0]	RW	0x0	Reserved.

WAV_MCU__MCU__DEBUG_CFG

Address: 0x00008044

Description:

Name	Index	Type	Reset	Description
EXIT	[4]	RW	0x0	Debug exit.
INTR	[0]	RW	0x0	Debug Interrupt.
STEP	[2]	RW	0x0	Step one instruction and return to debug mode.

WAV_MCU__MCU__ITCM_CFG

Address: 0x00008048

Description:

Name	Index	Type	Reset	Description
TIMING_PARAM	[7:0]	RW	0x03F	For GF12LPP: 2:0 - EMA, 4:3 - EMAW, 5 - EMAS, 6 - STOV.

WAV_MCU__MCU__DTCM_CFG

Address: 0x0000804C

Description:

Name	Index	Type	Reset	Description
TIMING_PARAM	[7:0]	RW	0x03F	For GF12LPP: 2:0 - EMA, 4:3 - EMAW, 5 - EMAS, 6 - STOV.

WAV_CMN__VREF_M0_CFG

Address: 0x00090008

Description:

Name	Index	Type	Reset	Description
CTRL	[7:0]	RW	0x0	

Registers

EN	[9]	RW	0x0	
HIZ	[10]	RW	0x0	
PWR	[12:11]	RW	0x0	

WAV_CMN__VREF_M1_CFG

Address: 0x0009000C

Description:

Name	Index	Type	Reset	Description
CTRL	[7:0]	RW	0x0	
EN	[9]	RW	0x0	
HIZ	[10]	RW	0x0	
PWR	[12:11]	RW	0x0	

WAV_CMN__ZQCAL_CFG

Address: 0x00090010

Description:

Name	Index	Type	Reset	Description
CAL_EN	[5]	RW	0x0	ZQ calibration enable
NCAL	[4:0]	RW	0x0	
PCAL	[13:8]	RW	0x0	
PD_SEL	[6]	RW	0x0	
VOL_OP6_SEL	[7]	RW	0x0	

WAV_CMN__ZQCAL_STA

Address: 0x00090014

Description:

Name	Index	Type	Reset	Description
COMP	[0]	R	0x0	zqcal comparator output, calibration indicator,stop calib. when 1->0.

WAV_CMN__IBIAS_CFG

Address: 0x00090018

Description:

Name	Index	Type	Reset	Description
EN	[0]	RW	0x0	Enable IBIAS.

WAV_CMN__TEST_CFG

Address: 0x0009001C

Description:

Name	Index	Type	Reset	Description
ATB_MODE	[1:0]	RW	0x0	Analog test mode.

Registers

ATST_SEL	[5:2]	RW	0x0	Analog test select.
DTST_DIV_EN	[17]	RW	0x0	Digital test clock divide enable.
DTST_DRV_R_IMPD	[10:8]	RW	0x0	Test pad driver impedance.
DTST_EXT_SEL	[16:12]	RW	0x0	Digital test select.

WAV_CMN__LDO_M0_CFG

Address: 0x00090020

Description:

Name	Index	Type	Reset	Description
ATST_SEL	[12:10]	RW	0x0	analog test select.
EN	[8]	RW	0x0	ldo enable.
HIZ	[13]	RW	0x0	LDO tri-state.
TRAN_ENH_EN	[9]	RW	0x0	debug only.
VREF_CTRL	[7:0]	RW	0x0	vref control.

WAV_CMN__LDO_M1_CFG

Address: 0x00090024

Description:

Name	Index	Type	Reset	Description
ATST_SEL	[12:10]	RW	0x0	analog test select.
EN	[8]	RW	0x0	ldo enable.
HIZ	[13]	RW	0x0	LDO tri-state.
TRAN_ENH_EN	[9]	RW	0x0	debug only.
VREF_CTRL	[7:0]	RW	0x0	vref control.

WAV_CMN__CLK_CTRL_CFG

Address: 0x00090028

Description:

Name	Index	Type	Reset	Description
GFCM_EN	[3]	RW	0x0	Glitch-free mux enable.
PLLO_DIV_CLK_BYP	[0]	RW	0x0	PLLO clk divider bypass.
PLLO_DIV_CLK_EN	[2]	RW	0x0	PLLO clk divider enable.
PLLO_DIV_CLK_RST	[1]	RW	0x1	PLLO clk divider rst.

WAV_CMN__PMON_ANA_CFG

Address: 0x00090038

Description:

Name	Index	Type	Reset	Description
NAND_EN	[0]	RW	0x0	PMON analog nand enable
NOR_EN	[1]	RW	0x0	PMON analog nor enable

Registers

WAV_CMN__PMON_DIG_CFG

Address: 0x0009003C

Description:

Name	Index	Type	Reset	Description
INITWAIT	[7:0]	RW	0x0	PMON digital count initial wait
REFCLK_RST	[8]	RW	0x1	PMON digital refclk reset

WAV_CMN__PMON_DIG_NAND_CFG

Address: 0x00090040

Description:

Name	Index	Type	Reset	Description
COUNT_EN	[12]	RW	0x0	PMON digital count enable
REFCOUNT	[11:0]	RW	0x0	PMON digital refcount

WAV_CMN__PMON_DIG_NOR_CFG

Address: 0x00090044

Description:

Name	Index	Type	Reset	Description
COUNT_EN	[12]	RW	0x0	PMON digital count enable
REFCOUNT	[11:0]	RW	0x0	PMON digital refcount

WAV_CMN__PMON_NAND_STA

Address: 0x00090048

Description:

Name	Index	Type	Reset	Description
COUNT	[23:0]	R	0x0	PMON nand count value.
DONE	[24]	R	0x0	PMON done.

WAV_CMN__PMON_NOR_STA

Address: 0x0009004C

Description:

Name	Index	Type	Reset	Description
COUNT	[23:0]	R	0x0	PMON nor count value.
DONE	[24]	R	0x0	PMON done.

WAV_CMN__CLK_STA

Address: 0x00090050

Description:

Name	Index	Type	Reset	Description
GFCMO_CLKA_SEL	[0]	R	0x0	Glitch free mux 0/180 cock select status.

Registers

GFCM0_CLKB_SEL	[1]	R	0x0	Glitch free mux 0/180 cock select status.
GFCM1_CLKA_SEL	[2]	R	0x0	Glitch free mux 90/270 cock select status.
GFCM1_CLKB_SEL	[3]	R	0x0	Glitch free mux 90/270 cock select status.

WAV_CMN__RSTN_CFG

Address: 0x00090054

Description:

Name	Index	Type	Reset	Description
RSTN_BS_DIN	[3]	RW	0x0	Resetn Bscan Data In.
RSTN_BS_ENA	[4]	RW	0x0	Resetn Bscan Enable.
RSTN_LPBK_ENA	[2]	RW	0x0	Resetn Loopback Enable.
RSTN_OVR_SEL	[0]	RW	0x0	When set high, selects the override value.
RSTN_OVR_VAL	[1]	RW	0x0	Resetn override value.

WAV_CMN__RSTN_STA

Address: 0x00090058

Description:

Name	Index	Type	Reset	Description
RSTN_LPBK	[0]	R	0x0	Resetn loopback value.

WAV_CMN_PLL__CORE_OVERRIDES

Address: 0x00098000

Description:

Name	Index	Type	Reset	Description
CORE_GFCM_SEL	[5]	RW	0x0	Overrides the GFCM that is external. If you aren't sure what that means, don't play with this.
CORE_GFCM_SEL_MUX	[6]	RW	0x0	
CORE_RESET	[0]	RW	0x0	Main logic reset
CORE_RESET_MUX	[1]	RW	0x0	1 - Use value from register. 0 - Use value from hardware
CORE_VCO_SEL	[3:2]	RW	0x0	Selects which VCO is in PLL mode. Requires core_switch_vco to be written to take new value.
CORE_VCO_SEL_MUX	[4]	RW	0x0	1 - Use value from register. 0 - Use value from hardware

WAV_CMN_PLL__CORE_SWTICH_VCO

Address: 0x00098004

Description:

Name	Index	Type	Reset	Description
CORE_SWITCH_VCO	[0]	RW	0x0	WFIFO Writing a 1 to this will cause the PLL statemachine to switch to the selected VCO.

WAV_CMN_PLL__CORE_SWTICH_VCO_HW

Address: 0x00098008

Registers

Description:

Name	Index	Type	Reset	Description
CORE_SWITCH_VCO_HW	[0]	RW	0x0	HW Override register for core_switch_vco from external HW source. Basically don't use this register value unless someone tells you
CORE_SWITCH_VCO_HW_MUX	[1]	RW	0x0	

WAV_CMN_PLL__CORE_STATUS

Address: 0x0009800C

Description:

Name	Index	Type	Reset	Description
CORE_FASTLOCK_READY	[1]	R	0x0	Asserts when the state machine has gone through the fast lock process (but not entire lock)
CORE_INITIAL_SWITCH_DONE	[2]	R	0x0	Asserts when the state machine has gone through the VCO switch and is on the next VCO.
CORE_READY	[0]	R	0x0	Asserts when the state machine has gone through the entire lock process
FREQ_DETECT_CYCLES	[20:4]	R	0x0	Current FB cycles from freq detection circuit
FREQ_DETECT_LOCK	[3]	R	0x0	Status of the freq detection circuit
FSM_STATE	[24:21]	R	0x0	FSM State

WAV_CMN_PLL__CORE_STATUS_INT

Address: 0x00098010

Description:

Name	Index	Type	Reset	Description
CORE_LOCKED	[1]	R	0x0	W1C Asserts when the main state machine has gone through the PLL enabling routine and lock has been detected. (Informative)
INITIAL_SWITCH_DONE	[2]	R	0x0	W1C Asserts when the main state machine has gone through the initial switch transition.
LOSS_OF_LOCK	[0]	R	0x0	W1C Asserts when the lock detection circuit loses lock after initially seeing lock.
VCO0_FLL_LOCKED	[3]	R	0x0	W1C Asserts when the FLL has completed calibrations and is conceptually locked. (Informative)
VCO0_FLL_THRESHOLD	[4]	R	0x0	W1C Asserts when the FLL hits the threshold value or higher during freq lock.
VCO1_FLL_LOCKED	[5]	R	0x0	W1C Asserts when the FLL has completed calibrations and is conceptually locked. (Informative)
VCO1_FLL_THRESHOLD	[6]	R	0x0	W1C Asserts when the FLL hits the threshold value or higher during freq lock.
VCO2_FLL_LOCKED	[7]	R	0x0	W1C Asserts when the FLL has completed calibrations and is conceptually locked. (Informative)
VCO2_FLL_THRESHOLD	[8]	R	0x0	W1C Asserts when the FLL hits the threshold value or higher during freq lock.

WAV_CMN_PLL__CORE_STATUS_INT_EN

Address: 0x00098014

Registers

Description:

Name	Index	Type	Reset	Description
CORE_LOCKED_INT_EN	[1]	RW	0x0	1 - Enables the core_locked interrupt
INITIAL_SWITCH_DONE_INT_EN	[2]	RW	0x0	1 - Enables the initial_switch_done interrupt
LOSS_OF_LOCK_INT_EN	[0]	RW	0x0	1 - Enables loss_of_lock interrupt
VCO0_FLL_LOCKED_INT_EN	[3]	RW	0x0	1 - Enables the fll_locked interrupt
VCO0_FLL_THRESHOLD_INT_EN	[4]	RW	0x0	1 - Enables fll_threshold interrupt
VCO1_FLL_LOCKED_INT_EN	[5]	RW	0x0	1 - Enables the fll_locked interrupt
VCO1_FLL_THRESHOLD_INT_EN	[6]	RW	0x0	1 - Enables fll_threshold interrupt
VCO2_FLL_LOCKED_INT_EN	[7]	RW	0x0	1 - Enables the fll_locked interrupt
VCO2_FLL_THRESHOLD_INT_EN	[8]	RW	0x0	1 - Enables fll_threshold interrupt

WAV_CMN_PLL__VCO0_BAND

Address: 0x00098018

Description:

Name	Index	Type	Reset	Description
RESERVED	[7]	RW	0x0	
VCO0_BAND	[5:0]	RW	0x0	{BFLOP} Binary representation of VCO band
VCO0_BAND_MUX	[6]	RW	0x1	1 - Use value from register. 0 - Hardware controlled
VCO0_FINE	[13:8]	RW	0x1f	{BFLOP} VCO Fine Control Value
VCO0_FINE_MUX	[14]	RW	0x1	1 - Use value from register. 0 - Hardware controlled

WAV_CMN_PLL__VCO0_CONTROL

Address: 0x0009801C

Description:

Name	Index	Type	Reset	Description
VCO0_BYP_CLK_SEL	[2]	RW	0x0	{BFLOP} Uses refclk for VCO output clock
VCO0_ENA	[0]	RW	0x0	{CORESCAN:0 IDDQ:0 BFLOP} Main Enable of the VCO
VCO0_ENA_MUX	[1]	RW	0x0	1 - Use value from vco0_ena. 0 - Hardware controlled

WAV_CMN_PLL__VCO0_FLL_CONTROL1

Address: 0x00098020

Description:

Name	Index	Type	Reset	Description
VCO0_BAND_START	[7:2]	RW	0x1f	Starting band upon enabling FLL. This should match the same band used to lock the VCO0 in PLL mode.
VCO0_DELAY_COUNT	[17:14]	RW	0x2	Number of Refclk Cycles to wait after deactivation of counters before checking up/dn
VCO0_FINE_START	[13:8]	RW	0x1f	Starting fine code upon enabling FLL. This should match the same fine code used to lock the VCO0 in PLL mode.
VCO0_FLL_BYPASS_BAND	[23]	RW	0x1	1 - Band code is not calibrated during FLL enable. User would want to set the vco_band_start to the desired band setting

Registers

VCOO_FLL_BYPASS_FINE	[24]	RW	0x0	1 - Fine code is not calibrated during FLL enable. User would want to set the vco_fine_start to the desired band setting
VCOO_FLL_ENABLE	[0]	RW	0x0	Enables FLL
VCOO_FLL_MANUAL_MODE	[1]	RW	0x0	0 - FLL will continually change band, 1 - FLL will run once (used for manual SW calibration of band)
VCOO_FLL_PERSISTENT_MODE	[25]	RW	0x1	0 - FLL will run until lock is detected and will hold code. 1 - FLL will continue to run, adapting to frequency changes.
VCOO_LOCKED	[28]	RW	0x0	RO FLL lock indication
VCOO_LOCKED_COUNT_THRESHOLD	[22:19]	RW	0x4	Number of consecutive cycles where band toggles +/-1 before indicating locked
VCOO_TOO_FAST_STATUS	[26]	RW	0x0	RO Asserted if VCO count is higher than target + range (use during manual SW calibration)
VCOO_TOO_SLOW_STATUS	[27]	RW	0x0	RO Asserted if VCO count is lower than target + range (use during manual SW calibration)
VCOO_USE_DEMETED_CHECK	[18]	RW	0x1	1 - up/dn check is based on demeted signals, 0 - up/dn is coming from VCO clock domain (ensure enough delay thorough delay count)

WAV_CMN_PLL__VCO0_FLL_CONTROL2

Address: 0x00098024

Description:

Name	Index	Type	Reset	Description
VCOO_FLL_RANGE	[28:24]	RW	0x4	+/- range to be considered in target. Outside range will increment/decrement band setting
VCOO_FLL_REFCLK_COUNT	[7:0]	RW	0x8	Number of Refclk Cycles to Enable VCO Counter
VCOO_FLL_VCO_COUNT_TARGET	[23:8]	RW	0xd0	Number of expected VCO cycles. Target = (refclk_count * refclk period) / vcoclk period

WAV_CMN_PLL__VCO0_FLL_CONTROL3

Address: 0x00098028

Description:

Name	Index	Type	Reset	Description
VCOO_FLL_BAND_THRESH	[5:0]	RW	0x3c	Threshold to indicate that the FLL band is too high

WAV_CMN_PLL__VCO0_FLL_BAND_STATUS

Address: 0x0009802C

Description:

Name	Index	Type	Reset	Description
VCOO_BAND_PREV_STATUS	[11:6]	R	0x0	N-1 band reading
VCOO_BAND_STATUS	[5:0]	R	0x0	Latest band reading
VCOO_FINE_PREV_STATUS	[23:18]	R	0x0	N-1 fine reading
VCOO_FINE_STATUS	[17:12]	R	0x0	Latest fine reading

WAV_CMN_PLL__VCO0_FLL_COUNT_STATUS

Address: 0x00098030

Registers

Description:

Name	Index	Type	Reset	Description
VCO0_VCO_COUNT	[15:0]	R	0x0	Current VCO count from FLL. To be used for manual calibration

WAV_CMN_PLL__VCO0_INT_FRAC_SETTINGS

Address: 0x00098034

Description:

Name	Index	Type	Reset	Description
VCO0_FRAC	[24:9]	RW	0x0	Fractional value of feedback divider when VCO is in PLL mode
VCO0_FRAC_EN	[25]	RW	0x0	
VCO0_FRAC_EN_AUTO	[26]	RW	0x1	
VCO0_INT	[8:0]	RW	0xa	Integer value of feedback divider when VCO is in PLL mode

WAV_CMN_PLL__VCO0_PROP_GAINS

Address: 0x00098038

Description:

Name	Index	Type	Reset	Description
VCO0_PROP_GAIN	[4:0]	RW	0xa	Proportional gain when this VCO is active

WAV_CMN_PLL__VCO1_BAND

Address: 0x0009803C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7]	RW	0x0	
VCO1_BAND	[5:0]	RW	0x0	{BFLOP} Binary representation of VCO band
VCO1_BAND_MUX	[6]	RW	0x0	1 - Use value from register. 0 - Hardware controlled
VCO1_FINE	[13:8]	RW	0x0	{BFLOP} VCO Fine Control Value
VCO1_FINE_MUX	[14]	RW	0x0	1 - Use value from register. 0 - Hardware controlled

WAV_CMN_PLL__VCO1_CONTROL

Address: 0x00098040

Description:

Name	Index	Type	Reset	Description
VCO1_BYP_CLK_SEL	[2]	RW	0x0	{BFLOP} Uses refclk for VCO output clock
VCO1_ENA	[0]	RW	0x0	{CORESCAN:0 IDDQ:0 BFLOP} Main Enable of the VCO
VCO1_ENA_MUX	[1]	RW	0x0	1 - Use value from vco0_ena. 0 - Hardware controlled
VCO1_POST_DIV	[4:3]	RW	0x0	{BFLOP} 00 - No div, 01 - /2, 10 - /4, 11 - /8

WAV_CMN_PLL__VCO1_FLL_CONTROL1

Address: 0x00098044

Registers

Description:

Name	Index	Type	Reset	Description
VCO1_BAND_START	[7:2]	RW	0x0	Starting band upon enabling FLL.
VCO1_DELAY_COUNT	[17:14]	RW	0x2	Number of Refclk Cycles to wait after deactivation of counters before checking up/dn
VCO1_FINE_START	[13:8]	RW	0x1f	Starting fine code upon enabling FLL. A mid code is **generally** the expected starting value.
VCO1_FLL_BYPASS_BAND	[23]	RW	0x0	1 - Band code is not calibrated during FLL enable. User would want to set the vco_band_start to the desired band setting
VCO1_FLL_BYPASS_FINE	[24]	RW	0x0	1 - Fine code is not calibrated during FLL enable. User would want to set the vco_FINE_start to the desired band setting
VCO1_FLL_ENABLE	[0]	RW	0x0	Enables FLL
VCO1_FLL_MANUAL_MODE	[1]	RW	0x0	0 - FLL will continually change band, 1 - FLL will run once (used for manual SW calibration of band)
VCO1_FLL_PERSISTENT_MODE	[25]	RW	0x0	0 - FLL will run until lock is detected and will hold code. 1 - FLL will continue to run, adapting to frequency changes.
VCO1_LOCKED	[28]	RW	0x0	RO FLL lock indication
VCO1_LOCKED_COUNT_THRESHOLD	[22:19]	RW	0x4	Number of consecutive cycles where band toggles +/-1 before indicating locked
VCO1_TOO_FAST_STATUS	[26]	RW	0x0	RO Asserted if VCO count is higher than target + range (use during manual SW calibration)
VCO1_TOO_SLOW_STATUS	[27]	RW	0x0	RO Asserted if VCO count is lower than target + range (use during manual SW calibration)
VCO1_USE_DEMETED_CHECK	[18]	RW	0x1	1 - up/dn check is based on demeted signals, 0 - up/dn is coming from VCO clock domain (ensure enough delay thorough delay count)

WAV_CMN_PLL__VCO1_FLL_CONTROL2

Address: 0x00098048

Description:

Name	Index	Type	Reset	Description
VCO1_FLL_RANGE	[28:24]	RW	0x4	+/- range to be considered in target. Outside range will increment/decrement band setting
VCO1_FLL_REFCLK_COUNT	[7:0]	RW	0x8	Number of Refclk Cycles to Enable VCO Counter
VCO1_FLL_VCO_COUNT_TARGET	[23:8]	RW	0xd0	Number of expected VCO cycles. Target = (refclk_count * refclk period) / vcoclk period

WAV_CMN_PLL__VCO1_FLL_CONTROL3

Address: 0x0009804C

Description:

Name	Index	Type	Reset	Description
VCO1_FLL_BAND_THRESH	[5:0]	RW	0x3c	Threshold to indicate that the FLL band is too high

WAV_CMN_PLL__VCO1_FLL_BAND_STATUS

Address: 0x00098050

Description:

Registers

Name	Index	Type	Reset	Description
VCO1_BAND_PREV_STATUS	[11:6]	R	0x0	N-1 band reading
VCO1_BAND_STATUS	[5:0]	R	0x0	Latest band reading
VCO1_FINE_PREV_STATUS	[23:18]	R	0x0	N-1 fine reading
VCO1_FINE_STATUS	[17:12]	R	0x0	Latest fine reading

WAV_CMN_PLL__VCO1_FLL_COUNT_STATUS

Address: 0x00098054

Description:

Name	Index	Type	Reset	Description
VCO1_VCO_COUNT	[15:0]	R	0x0	Current VCO count from FLL. To be used for manual calibration

WAV_CMN_PLL__VCO1_INT_FRAC_SETTINGS

Address: 0x00098058

Description:

Name	Index	Type	Reset	Description
VCO1_FRAC	[24:9]	RW	0x0	Fractional value of feedback divider when VCO is in PLL mode
VCO1_FRAC_EN	[25]	RW	0x0	
VCO1_FRAC_EN_AUTO	[26]	RW	0x1	
VCO1_INT	[8:0]	RW	0xa	Integer value of feedback divider when VCO is in PLL mode

WAV_CMN_PLL__VCO1_PROP_GAINS

Address: 0x0009805C

Description:

Name	Index	Type	Reset	Description
VCO1_PROP_GAIN	[4:0]	RW	0xa	Proportional gain when this VCO is active

WAV_CMN_PLL__VCO1_SSC_CONTROLS

Address: 0x00098060

Description:

Name	Index	Type	Reset	Description
VCO1_SSC_AMP	[27:11]	RW	0x0	
VCO1_SSC_CENTER_SPREAD	[29]	RW	0x0	
VCO1_SSC_COUNT_CYCLES	[28]	RW	0x0	
VCO1_SSC_ENABLE	[0]	RW	0x0	
VCO1_SSC_STEPSIZE	[10:1]	RW	0x0	

WAV_CMN_PLL__VCO2_BAND

Address: 0x00098064

Description:

Registers

Name	Index	Type	Reset	Description
RESERVED	[7]	RW	0x0	
VCO2_BAND	[5:0]	RW	0x0	{BFLOP} Binary representation of VCO band
VCO2_BAND_MUX	[6]	RW	0x0	1 - Use value from register. 0 - Hardware controlled
VCO2_FINE	[13:8]	RW	0x0	{BFLOP} VCO Fine Control Value
VCO2_FINE_MUX	[14]	RW	0x0	1 - Use value from register. 0 - Hardware controlled

WAV_CMN_PLL__VCO2_CONTROL

Address: 0x00098068

Description:

Name	Index	Type	Reset	Description
VCO2_BYP_CLK_SEL	[2]	RW	0x0	{BFLOP} Uses refclk for VCO output clock
VCO2_ENA	[0]	RW	0x0	{CORESCAN:0 IDDQ:0 BFLOP} Main Enable of the VCO
VCO2_ENA_MUX	[1]	RW	0x0	1 - Use value from vco2_ena. 0 - Hardware controlled
VCO2_POST_DIV	[4:3]	RW	0x0	{BFLOP} 00 - No div, 01 - /2, 10 - /4, 11 - /8

WAV_CMN_PLL__VCO2_FLL_CONTROL1

Address: 0x0009806C

Description:

Name	Index	Type	Reset	Description
VCO2_BAND_START	[7:2]	RW	0x0	Starting band upon enabling FLL.
VCO2_DELAY_COUNT	[17:14]	RW	0x2	Number of Refclk Cycles to wait after deactivation of counters before checking up/dn
VCO2_FINE_START	[13:8]	RW	0x1f	Starting fine code upon enabling FLL. A mid code is **generally** the expected starting value.
VCO2_FLL_BYPASS_BAND	[23]	RW	0x0	1 - Band code is not calibrated during FLL enable. User would want to set the vco_band_start to the desired band setting
VCO2_FLL_BYPASS_FINE	[24]	RW	0x0	1 - Fine code is not calibrated during FLL enable. User would want to set the vco_fine_start to the desired band setting
VCO2_FLL_ENABLE	[0]	RW	0x0	Enables FLL
VCO2_FLL_MANUAL_MODE	[1]	RW	0x0	0 - FLL will continually change band, 1 - FLL will run once (used for manual SW calibration of band)
VCO2_FLL_PERSISTENT_MODE	[25]	RW	0x0	0 - FLL will run until lock is detected and will hold code. 1 - FLL will continue to run, adapting to frequency changes.
VCO2_LOCKED	[28]	RW	0x0	RO FLL lock indication
VCO2_LOCKED_COUNT_THRESHOLD	[22:19]	RW	0x4	Number of consecutive cycles where band toggles +/-1 before indicating locked
VCO2_TOO_FAST_STATUS	[26]	RW	0x0	RO Asserted if VCO count is higher than target + range (use during manual SW calibration)
VCO2_TOO_SLOW_STATUS	[27]	RW	0x0	RO Asserted if VCO count is lower than target + range (use during manual SW calibration)
VCO2_USE_DEMETED_CHECK	[18]	RW	0x1	1 - up/dn check is based on demeted signals, 0 - up/dn is coming from VCO clock domain (ensure enough delay thorough delay count)

WAV_CMN_PLL__VCO2_FLL_CONTROL2

Registers

Address: 0x00098070

Description:

Name	Index	Type	Reset	Description
VCO2_FLL_RANGE	[28:24]	RW	0x4	+/- range to be considered in target. Outside range will increment/decrement band setting
VCO2_FLL_REFCLK_COUNT	[7:0]	RW	0x8	Number of Refclk Cycles to Enable VCO Counter
VCO2_FLL_VCO_COUNT_TARGET	[23:8]	RW	0xd0	Number of expected VCO cycles. Target = (refclk_count * refclk period) / vcoclk period

WAV_CMN_PLL__VCO2_FLL_CONTROL3

Address: 0x00098074

Description:

Name	Index	Type	Reset	Description
VCO2_FLL_BAND_THRESH	[5:0]	RW	0x3c	Threshold to indicate that the FLL band is too high

WAV_CMN_PLL__VCO2_FLL_BAND_STATUS

Address: 0x00098078

Description:

Name	Index	Type	Reset	Description
VCO2_BAND_PREV_STATUS	[11:6]	R	0x0	N-1 band reading
VCO2_BAND_STATUS	[5:0]	R	0x0	Latest band reading
VCO2_FINE_PREV_STATUS	[23:18]	R	0x0	N-1 fine reading
VCO2_FINE_STATUS	[17:12]	R	0x0	Latest fine reading

WAV_CMN_PLL__VCO2_FLL_COUNT_STATUS

Address: 0x0009807C

Description:

Name	Index	Type	Reset	Description
VCO2_VCO_COUNT	[15:0]	R	0x0	Current VCO count from FLL. To be used for manual calibration

WAV_CMN_PLL__VCO2_INT_FRAC_SETTINGS

Address: 0x00098080

Description:

Name	Index	Type	Reset	Description
VCO2_FRAC	[24:9]	RW	0x0	Fractional value of feedback divider when VCO is in PLL mode
VCO2_FRAC_EN	[25]	RW	0x0	
VCO2_FRAC_EN_AUTO	[26]	RW	0x1	
VCO2_INT	[8:0]	RW	0xa	Integer value of feedback divider when VCO is in PLL mode

WAV_CMN_PLL__VCO2_PROP_GAINS

Address: 0x00098084

Registers

Description:

Name	Index	Type	Reset	Description
VCO2_PROP_GAIN	[4:0]	RW	0xa	Proportional gain when this VCO is active

WAV_CMN_PLL__VCO2_SSC_CONTROLS

Address: 0x00098088

Description:

Name	Index	Type	Reset	Description
VCO2_SSC_AMP	[27:11]	RW	0x0	
VCO2_SSC_CENTER_SPREAD	[29]	RW	0x0	
VCO2_SSC_COUNT_CYCLES	[28]	RW	0x0	
VCO2_SSC_ENABLE	[0]	RW	0x0	
VCO2_SSC_STEPSIZE	[10:1]	RW	0x0	

WAV_CMN_PLL__STATE_MACHINE_CONTROLS

Address: 0x0009808C

Description:

Name	Index	Type	Reset	Description
BIAS_SETTLE_COUNT	[7:0]	RW	0x8	Number of refclk cycles to wait until entering the fastlock routine
DISABLE_LOCK_DET_AFTER_LOCK	[20]	RW	0x0	1 - Lock Detection circuit is disabled after lock is seen. 0 - Lock detection always enabled. Disabling lock detect would mean loss of lock is not possible to detect.
FLL_INITIAL_SETTLE	[24:21]	RW	0x4	Initial settle time for FLLs when enabling. Provides some time for the VCO to ramp up.
PRE_LOCKING_COUNT	[15:8]	RW	0x4	Number of refclk cycles to wait until entering normal lock after fast lock
SWITCH_COUNT	[19:16]	RW	0x1	Number of refclk cycles to wait with FBCLK disabled when performing a VCO switch

WAV_CMN_PLL__STATE_MACHINE_CONTROLS2

Address: 0x00098090

Description:

Name	Index	Type	Reset	Description
PRE_SWITCH_TIME	[3:0]	RW	0x1	Number of cycles prior to enabling the next VCO to disable the FBCLK
SWITCH_1_TIME	[15:8]	RW	0x3	Number of cycles to the next VCO is allowed to be in PLL mode before switching the clock mux. Increasing this can allow the VCO more time to phase lock before switching the clock mux.
SWITCH_2_TIME	[23:16]	RW	0x1	Number of cycles to hold both VCOs enabled after the clock mux switch.
SWITCH_RESET_TIME	[7:4]	RW	0x1	Number of cycles to hold the PLL PFD in reset to allow VCO switch

WAV_CMN_PLL__INTR_GAINS

Registers

Address: 0x00098094

Description:

Name	Index	Type	Reset	Description
NORMAL_INT_GAIN	[4:0]	RW	0xf	Integral Gain when not in fastlock

WAV_CMN_PLL__INTR_PROP_FL_GAINS

Address: 0x00098098

Description:

Name	Index	Type	Reset	Description
FL_INT_GAIN	[4:0]	RW	0x1e	Integral gain when in fastlock
FL_PROP_GAIN	[9:5]	RW	0x1e	Proportional gain when in fastlock

WAV_CMN_PLL__INTR_PROP_GAINS_OVERRIDE

Address: 0x0009809C

Description:

Name	Index	Type	Reset	Description
INT_GAIN	[4:0]	RW	0xf	{BFLOP} Integral gain directly after VCO switch
INT_GAIN_MUX	[5]	RW	0x0	
PROP_GAIN	[10:6]	RW	0x9	{BFLOP} Proportional gain directly after VCO switch
PROP_GAIN_MUX	[11]	RW	0x0	

WAV_CMN_PLL__LOCK_DET_SETTINGS

Address: 0x000980A0

Description:

Name	Index	Type	Reset	Description
LD_RANGE	[21:16]	RW	0x4	Range tolerance for refclk vs. fbclk during normal lock procedure
LD_REFCLK_CYCLES	[15:0]	RW	0x200	Number of refclk cycles to compare against fbclk for detecting lock. A higher number with tighter range equates to a lower PPM tolerance

WAV_CMN_PLL__FASTLOCK_DET_SETTINGS

Address: 0x000980A4

Description:

Name	Index	Type	Reset	Description
FASTLD_RANGE	[21:16]	RW	0x8	Range tolerance for refclk vs. fbclk during fast lock procedure
FASTLD_REFCLK_CYCLES	[15:0]	RW	0x100	Number of refclk cycles to compare against fbclk for detecting lock during fastlock. A higher number with tighter range equates to a lower PPM tolerance

WAV_CMN_PLL__ANALOG_EN_RESET

Address: 0x000980A8

Registers

Description:

Name	Index	Type	Reset	Description
FBDIV_SEL	[12:4]	RW	0x0	{BFLOP} Feedback divider override going to analog
FBDIV_SEL_MUX	[13]	RW	0x0	
PLL_EN	[0]	RW	0x0	{CORESCAN:0 IDDQ:0 BFLOP} PLL Enable override going to analog
PLL_EN_MUX	[1]	RW	0x0	
PLL_RESET	[2]	RW	0x0	{CORESCAN:1 IDDQ:1 BFLOP} PLL reset override going to analog
PLL_RESET_MUX	[3]	RW	0x0	
VCO_SEL	[15:14]	RW	0x0	{BFLOP} VCO Sel override going to analog
VCO_SEL_MUX	[16]	RW	0x0	

WAV_CMN_PLL__MODE_DTST_MISC

Address: 0x000980AC

Description:

Name	Index	Type	Reset	Description
BIAS_LVL	[3:0]	RW	0x8	{BFLOP} Bias Level analog control
BIAS_SEL	[8]	RW	0x0	{BFLOP} 0 - Internal Bias
CP_INT_MODE	[4]	RW	0x0	{CORESCAN:0 IDDQ:0 BSCAN:0} Analog control, keep at 0x0
DIV16EN	[7]	RW	0x0	{BFLOP} Enables div16 from VCO post dividers
EN_LOCK_DET	[5]	RW	0x0	Override for enabling lock detect. Should only be used in testing.
EN_LOCK_DET_MUX	[6]	RW	0x0	1 - Use value from register. 0 - Hardware controlled

WAV_CMN_PLL__PROP_CTRLS

Address: 0x000980B0

Description:

Name	Index	Type	Reset	Description
PROP_C_CTRL	[1:0]	RW	0x0	{BFLOP}
PROP_R_CTRL	[3:2]	RW	0x0	{BFLOP}

WAV_CMN_PLL__REFCLK_CONTROLS

Address: 0x000980B4

Description:

Name	Index	Type	Reset	Description
PFD_MODE	[1:0]	RW	0x0	{BFLOP}
SEL_REFCLK_ALT	[2]	RW	0x0	{BFLOP}

WAV_CMN_PLL__CLKGATE_DISABLES

Address: 0x000980B8

Description:

Registers

Name	Index	Type	Reset	Description
FORCE_FBCLK_GATE	[0]	RW	0x0	1 - Disables clock gating for digital. 0 - Uses hardware control
FORCE_VCO0_CLK_GATE	[1]	RW	0x0	1 - Disables clock gating for digital. 0 - Uses hardware control
FORCE_VCO1_CLK_GATE	[2]	RW	0x0	1 - Disables clock gating for digital. 0 - Uses hardware control
FORCE_VCO2_CLK_GATE	[3]	RW	0x0	1 - Disables clock gating for digital. 0 - Uses hardware control

WAV_FSW__CTRL_CFG

Address: 0x000A0000

Description:

Name	Index	Type	Reset	Description
MSR_OVR	[6]	RW	0x0	Mode Select Register Override.
MSR_OVR_VAL	[7]	RW	0x0	Mode Select Register Override value.
MSR_TOGGLE_EN	[5]	RW	0x1	MSR toggle enable.
POST_GFMSEL_WAIT	[19:16]	RW	0x4	Wait time after switching PLL GFCM.
PREP_DONE	[8]	RW	0x0	Software frequency switch PREP done.
PSTWORK_DONE	[9]	RW	0x0	Software frequency switch PSTWORK done.
PSTWORK_DONE_OVR	[10]	RW	0x1	Software frequency switch PSTWORK done Override. When this bit is set, HW will not wait for SW PSTWORK_DONE to go high before asserting init_complete to MC
SWITCH_DONE_OVR	[11]	RW	0x1	VCO switch done override.
SWITCH_DONE_STICKY_CLR	[12]	RW	0x0	VCO switch done sticky clear.
VCO_SEL_OVR	[0]	RW	0x1	VCO select override enable.
VCO_SEL_OVR_VAL	[2:1]	RW	0x0	VCO select override value. 2: VCO2 output clock, 1: VCO1 output clock.
VCO_TOGGLE_EN	[4]	RW	0x1	VCO toggle enable.

WAV_FSW__CTRL_STA

Address: 0x000A0004

Description:

Name	Index	Type	Reset	Description
CMN_MSR	[3]	R	0x0	MSR value.
CORE_READY	[4]	R	0x0	PLL core ready value.
SWITCH_DONE	[2]	R	0x0	VCO switch done value.
VCO_SEL	[1:0]	R	0x0	VCO select value - 2:VCO2, 1: VCO1, 0:VCO0.

WAV_FSW__DEBUG_CFG

Address: 0x000A0008

Description:

Name	Index	Type	Reset	Description
DEBUG_BUS_SEL	[3:0]	RW	0x0	0 - Drive 0, 1 - PLL Debug bus, 2 - FSW debug bus.

WAV_FSW__CSP_0_CFG

Registers

Address: 0x000A002C

Description:

Name	Index	Type	Reset	Description
PRECLKDIS_WAIT	[3:0]	RW	0x3	Wait time between PI disable and clk disable.
PRERST_WAIT	[7:4]	RW	0x3	Wait time between clk disable and reset assertion.
PSTCLKEN_WAIT	[19:16]	RW	0x3	Wait time between clk enable and PI enable.
PSTPIEN_WAIT	[23:20]	RW	0x3	Wait time after PI enable and sending a req complete.
PSTRST_WAIT	[15:12]	RW	0x3	Wait time between reset deassertion and clk enable.
RST_PULSE_WIDTH	[11:8]	RW	0x3	Clock divider Reset pulse width.

WAV_FSW__CSP_1_CFG

Address: 0x000A0030

Description:

Name	Index	Type	Reset	Description
CGC_EN_OVR	[2]	RW	0x0	Select CSP Clock gating Enable override.
CGC_EN_OVR_VAL	[5]	RW	0x0	CSP Clock gating enable override.
CLK_DISABLE_OVR_VAL	[8]	RW	0x1	Force clock disable.
DIV_RST_OVR_VAL	[7]	RW	0x0	Force divider reset.
PI_DISABLE_OVR_VAL	[6]	RW	0x0	Force PI disable.
REQ_COMPLETE_OVR	[1]	RW	0x0	Select CSP Req complete override.
REQ_COMPLETE_OVR_VAL	[4]	RW	0x0	Req complete override.
REQ_COMPLETE_STA_CLR	[9]	RW	0x0	Clear the Req Complete Status field.
REQ_OVR	[0]	RW	0x0	Select CSP Req override.
REQ_OVR_VAL	[3]	RW	0x0	Req override.

WAV_FSW__CSP_STA

Address: 0x000A0034

Description:

Name	Index	Type	Reset	Description
REQ_COMPLETE	[0]	R	0x0	Request Complete Status Field.

WAV_CTRL__CLK_CFG

Address: 0x000B0000

Description:

Name	Index	Type	Reset	Description
AHCLK_DIV2_EN	[3]	RW	0x1	AHB clock source - 0: MCUCLK used as internal AHB clock 1: DIV2 of MCU clock used as internal AHB clock.
AHB_CLK_ON	[4]	RW	0x0	Software AHB clock-on request. Used to keep the clock running.
MCU_CLK_CGC_EN	[8]	RW	0x1	MCU Clock root clock gating.
MCU_GFM_SEL	[2]	RW	0x0	Select the MCU clock source. 0: DFT REF clock Mux output 1: PLL VCO0 clock

Registers

PLL_CLK_EN	[0]	RW	0x0	Enable VCO0 PLL clock input to MCU GFM.
REF_CLK_CGC_EN	[9]	RW	0x1	REF Clock root clock gating.
REF_CLK_ON	[5]	RW	0x0	Software Reference clock-on request. Used to keep the clock running.
REF_CLK_SEL	[1]	RW	0x0	Select Reference clock routed to MCU clock GFCM. 0: Ref clock 1: Ref alt clock.

WAV_CTRL__CLK_STA

Address: 0x000B0004

Description:

Name	Index	Type	Reset	Description
DFI_CLK_ON	[2]	R	0x0	DFI clock-on request from system.
MCU_GFM_SEL0	[0]	R	0x0	Select the MCU clock source. 0: AHB EXT clock 1: VCO0 clock
MCU_GFM_SEL1	[1]	R	0x0	Select the MCU clock source. 0: AHB EXT clock 1: VCO0 clock

WAV_CTRL__AHB_SNOOP_CFG

Address: 0x000B0008

Description:

Name	Index	Type	Reset	Description
RDATA_CLR	[8]	RW	0x0	Read data FIFO clear.
RDATA_UPDATE	[10]	RW	0x0	Read data update. Loads data into data loader.
SNOOP_MODE	[12]	RW	0x0	Mode select - 1: Enable Snoop, 0: Disable Snoop
TS_ENABLE	[0]	RW	0x0	Timestamp counter enable.
TS_RESET	[1]	RW	0x0	Timestamp counter reset.

WAV_CTRL__AHB_SNOOP_STA

Address: 0x000B000C

Description:

Name	Index	Type	Reset	Description
EMPTY	[0]	R	0x0	Snoop FIFO empty.
FULL	[1]	R	0x0	Snoop FIFO full.

WAV_CTRL__AHB_SNOOP_DATA_STA

Address: 0x000B0010

Description:

Name	Index	Type	Reset	Description
RDATA	[31:0]	R	0x00000 000	Data from snoop data.

WAV_CTRL__AHB_SNOOP_PATTERN_CFG

Address: 0x000B0014

Description:

Registers

Name	Index	Type	Reset	Description
PAT_0_EN	[0]	RW	0x0	Pattern enable.
PAT_0_MODE	[3:2]	RW	0x0	Pattern mode - 2: Less than, 1: Greater than, 0: Equal.
PAT_0_POLARITY	[1]	RW	0x0	Pattern polarity - 1: Inverted, 0: Non-Inverted.
PAT_1_EN	[8]	RW	0x0	Pattern enable.
PAT_1_MODE	[11:10]	RW	0x0	Pattern mode - 2: Less than, 1: Greater than, 0: Equal.
PAT_1_POLARITY	[9]	RW	0x0	Pattern polarity - 1: Inverted, 0: Non-Inverted.

WAV_CTRL__AHB_SNOOP_PATTERN_0_CFG

Address: 0x000B0018

Description:

Name	Index	Type	Reset	Description
PAT_VAL	[31:0]	RW	0x0	Pattern value.

WAV_CTRL__AHB_SNOOP_PATTERN_1_CFG

Address: 0x000B001C

Description:

Name	Index	Type	Reset	Description
PAT_VAL	[31:0]	RW	0x0	Pattern value.

WAV_CTRL__AHB_SNOOP_PATTERN_STA

Address: 0x000B0020

Description:

Name	Index	Type	Reset	Description
PAT_0_DETECT	[0]	W1C	0x0	Pattern detect.
PAT_1_DETECT	[1]	W1C	0x0	Pattern detect.

WAV_CTRL__DEBUG_CFG

Address: 0x000B0024

Description:

Name	Index	Type	Reset	Description
VAL	[31:0]	RW	0x0	Debug bus value.

WAV_CTRL__DEBUG1_CFG

Address: 0x000B0028

Description:

Name	Index	Type	Reset	Description
OVR_SEL	[0]	RW	0x0	Debug bus sw override select. When set to 1 selects the DEBUG_CFG[VAL] field to drive the debug bus.

WAV_DFI__TOP_0_CFG

Registers

Address: 0x000C0000

Description:

Name	Index	Type	Reset	Description
CA_LPBK_SEL	[0]	RW	0x0	Select loopback CA channel in a 1x32 DFI configuration with 2 CA PHY channels. 0x0 select PHY channel0 CA. 0x1 select PHY channel1 CA.

WAV_DFI__DATA_BIT_ENABLE_CFG

Address: 0x000C0004

Description:

Name	Index	Type	Reset	Description
VAL	[31:0]	RW	0x000001FF	Bits that are used for transferring valid data on both the wrdata and rddata buses.

WAV_DFI__PHYFREQ_RANGE_CFG

Address: 0x000C0008

Description:

Name	Index	Type	Reset	Description
VAL	[31:0]	RW	0x0000EFB5	Range of frequency values supported by the PHY. See datasheet frequency plan.

WAV_DFI__STATUS_IF_CFG

Address: 0x000C000C

Description:

Name	Index	Type	Reset	Description
SW_ACK_OVR	[2]	RW	0x1	Acknowledge override enable.
SW_ACK_VAL	[3]	RW	0x1	Acknowledge override value.
SW_EVENT_0_OVR	[4]	RW	0x0	Event (ACK High) override enable.
SW_EVENT_0_VAL	[5]	RW	0x0	Event (ACK High) override value.
SW_EVENT_1_OVR	[6]	RW	0x0	Event (ACK Low) override enable.
SW_EVENT_1_VAL	[7]	RW	0x0	Event (ACK Low) override value.
SW_FREQUENCY_VAL	[20:16]	RW	0x00	Frequency value.
SW_FREQ_FSP_VAL	[13:12]	RW	0x0	Frequency Set Point value.
SW_FREQ_OVR	[8]	RW	0x0	Frequency override enable.
SW_FREQ_RATIO_VAL	[15:14]	RW	0x0	Frequency Ratio value.
SW_REQ_OVR	[0]	RW	0x1	Request override enable.
SW_REQ_VAL	[1]	RW	0x0	Request override value.

WAV_DFI__STATUS_IF_STA

Address: 0x000C0010

Description:

Name	Index	Type	Reset	Description

Registers

ACK	[1]	R	0x0	Interface acknowledge value.
FREQUENCY	[12:8]	R	0x00	Frequency.
FREQ_FSP	[5:4]	R	0x0	Frequency Set Point.
FREQ_RATIO	[7:6]	R	0x0	Frequency Ratio.
REQ	[0]	R	0x0	Interface request value.

WAV_DFI__STATUS_IF_EVENT_0_CFG

Address: 0x000C0014

Description:

Name	Index	Type	Reset	Description
SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__STATUS_IF_EVENT_1_CFG

Address: 0x000C0018

Description:

Name	Index	Type	Reset	Description
SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__CTRLUPD_IF_CFG

Address: 0x000C001C

Description:

Name	Index	Type	Reset	Description
SW_ACK_OVR	[2]	RW	0x0	Acknowledge override enable.
SW_ACK_VAL	[3]	RW	0x0	Acknowledge override value.
SW_EVENT_0_OVR	[4]	RW	0x0	Event (ACK High) override enable.
SW_EVENT_0_VAL	[5]	RW	0x0	Event (ACK High) override value.
SW_EVENT_1_OVR	[6]	RW	0x0	Event (ACK Low) override enable.
SW_EVENT_1_VAL	[7]	RW	0x0	Event (ACK Low) override value.
SW_REQ_OVR	[0]	RW	0x0	Request override enable.
SW_REQ_VAL	[1]	RW	0x0	Request override value.

WAV_DFI__CTRLUPD_IF_STA

Address: 0x000C0020

Description:

Name	Index	Type	Reset	Description
ACK	[1]	R	0x0	Interface acknowledge value.
REQ	[0]	R	0x0	Interface request value.

Registers

WAV_DFI__CTRLUPD_IF_EVENT_0_CFG

Address: 0x000C0024

Description:

Name	Index	Type	Reset	Description
SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__CTRLUPD_IF_EVENT_1_CFG

Address: 0x000C0028

Description:

Name	Index	Type	Reset	Description
SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__LP_CTRL_IF_CFG

Address: 0x000C002C

Description:

Name	Index	Type	Reset	Description
SW_ACK_OVR	[2]	RW	0x0	Acknowledge override enable.
SW_ACK_VAL	[3]	RW	0x0	Acknowledge override value.
SW_EVENT_0_OVR	[4]	RW	0x0	Event (ACK High) override enable.
SW_EVENT_0_VAL	[5]	RW	0x0	Event (ACK High) override value.
SW_EVENT_1_OVR	[6]	RW	0x0	Event (ACK Low) override enable.
SW_EVENT_1_VAL	[7]	RW	0x0	Event (ACK Low) override value.
SW_REQ_OVR	[0]	RW	0x0	Request override enable.
SW_REQ_VAL	[1]	RW	0x0	Request override value.

WAV_DFI__LP_CTRL_IF_STA

Address: 0x000C0030

Description:

Name	Index	Type	Reset	Description
ACK	[1]	R	0x0	Interface acknowledge value.
REQ	[0]	R	0x0	Interface request value.
WAKEUP	[9:4]	R	0x0	Wakeup value.

WAV_DFI__LP_CTRL_IF_EVENT_0_CFG

Address: 0x000C0034

Description:

Name	Index	Type	Reset	Description

Registers

SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__LP_CTRL_IF_EVENT_1_CFG

Address: 0x000C0038

Description:

Name	Index	Type	Reset	Description
SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__LP_DATA_IF_CFG

Address: 0x000C003C

Description:

Name	Index	Type	Reset	Description
SW_ACK_OVR	[2]	RW	0x0	Acknowledge override enable.
SW_ACK_VAL	[3]	RW	0x0	Acknowledge override value.
SW_EVENT_0_OVR	[4]	RW	0x0	Event (ACK High) override enable.
SW_EVENT_0_VAL	[5]	RW	0x0	Event (ACK High) override value.
SW_EVENT_1_OVR	[6]	RW	0x0	Event (ACK Low) override enable.
SW_EVENT_1_VAL	[7]	RW	0x0	Event (ACK Low) override value.
SW_REQ_OVR	[0]	RW	0x0	Request override enable.
SW_REQ_VAL	[1]	RW	0x0	Request override value.

WAV_DFI__LP_DATA_IF_STA

Address: 0x000C0040

Description:

Name	Index	Type	Reset	Description
ACK	[1]	R	0x0	Interface acknowledge value.
REQ	[0]	R	0x0	Interface request value.
WAKEUP	[9:4]	R	0x0	Wakeup value.

WAV_DFI__LP_DATA_IF_EVENT_0_CFG

Address: 0x000C0044

Description:

Name	Index	Type	Reset	Description
SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__LP_DATA_IF_EVENT_1_CFG

Registers

Address: 0x000C0048

Description:

Name	Index	Type	Reset	Description
SW_EVENT_CNT	[19:0]	RW	0x0000	Event timer count value.
SW_EVENT_CNT_SEL	[31]	RW	0x0	0 - Select HW Event count value. 1 - Select SW Event count value.

WAV_DFI__PHYUPD_IF_CFG

Address: 0x000C004C

Description:

Name	Index	Type	Reset	Description
SW_ACK_OVR	[2]	RW	0x0	Acknowledge override enable.
SW_ACK_VAL	[3]	RW	0x0	Acknowledge override value.
SW_EVENT_OVR	[4]	RW	0x0	Event (ACK High) override enable.
SW_EVENT_VAL	[5]	RW	0x0	Event (ACK High) override value.
SW_REQ_OVR	[0]	RW	0x0	Request override enable.
SW_REQ_VAL	[1]	RW	0x0	Request override value.
SW_TYPE	[9:8]	RW	0x0	Type value.

WAV_DFI__PHYUPD_IF_STA

Address: 0x000C0050

Description:

Name	Index	Type	Reset	Description
ACK	[1]	R	0x0	Interface acknowledge value.
EVENT	[2]	R	0x0	Event value.
REQ	[0]	R	0x0	Interface request value.

WAV_DFI__PHYMSTR_IF_CFG

Address: 0x000C0054

Description:

Name	Index	Type	Reset	Description
SW_ACK_OVR	[2]	RW	0x0	Acknowledge override enable.
SW_ACK_VAL	[3]	RW	0x0	Acknowledge override value.
SW_CS_STATE	[8:7]	RW	0x0	CS state value.
SW_EVENT_OVR	[4]	RW	0x0	Event (ACK High) override enable.
SW_EVENT_VAL	[5]	RW	0x0	Event (ACK High) override value.
SW_REQ_OVR	[0]	RW	0x0	Request override enable.
SW_REQ_VAL	[1]	RW	0x0	Request override value.
SW_STATE_SEL	[6]	RW	0x0	State select value.
SW_TYPE	[10:9]	RW	0x0	Type value.

WAV_DFI__PHYMSTR_IF_STA

Registers

Address: 0x000C0058

Description:

Name	Index	Type	Reset	Description
ACK	[1]	R	0x0	Interface acknowledge value.
EVENT	[2]	R	0x0	Event value.
REQ	[0]	R	0x0	Interface request value.

WAV_DFI__DEBUG_CFG

Address: 0x000C005C

Description:

Name	Index	Type	Reset	Description
DEBUG_BUS_SEL	[3:0]	RW	0x0	Debug Bus select mapping: 0 - drives 0, 1 - dfich0_dqwr, 2 - dfich0_dqrd, 3- dfich0_ca, 7 - dfich0_dfibuf, 8 - control interfaces, 4 - dfich1_dqwr, 5 - dfich1_dqrd, 6 - dfich1_ca , all other settings drive 0 on debug bus.

WAV_DFICH0__TOP_1_CFG

Address: 0x000D0000

Description:

Name	Index	Type	Reset	Description
BUF_CLK_EN	[13]	RW	0x1	DFI Buffer clock Enable - 1: Enable clock to DFI Buffer, 0: Disable clock to DFI Buffer
BUF_MODE	[12]	RW	0x0	DFI Mode select - 1: Enable DFI Buffer, 0: Disable DFI Buffer and use DFI interface
CA_RDDATA_EN	[17]	RW	0x0	Set this bit 1 to enable CA Read Loopback path.
DQBYTE_RDVALID_MASK	[31:28]	RW	0x0	Set mask 1'b1 to force RD Valid from DQ bytes high. During training or debug when only some or one of the DQ byte is used, set the mask bit high for other BYTES to force the rdvalid of the DQ byte high. RD valid from all bytes must to high(either from DP or using Mask) to generate DFI rd_valid output. bit[0] - DQ0 Byte, bit[1] - DQ1 byte, bit[2]- DQ2 byte, bit[3] - DQ3 byte.
RDATA_CLR	[8]	RW	0x0	Buffer read data FIFO pointer clear.
RDATA_ENABLE	[9]	RW	0x0	Buffer read data enable. Shifts data from data loader.
RDATA_UPDATE	[10]	RW	0x0	Buffer read data update. Loads data into data loader.
RDOUT_EN_OVR	[19]	RW	0x0	Set this bit 1 to force the DFI Read valid,data, dbi to MC zero. Set this bit to 0 to pass the RD data from datapath to MC.
RDOUT_EN_OVR_SEL	[18]	RW	0x0	Set this bit 1 to enable SW override to gate or ugate DFI read output to MC.
TS_ENABLE	[0]	RW	0x0	Timestamp counter enable.
TS_RESET	[1]	RW	0x0	Timestamp counter reset.
WCK_MODE	[16]	RW	0x0	Protocol mode select - 0: LP4/DDR/HBM mode, 1: LP5/GDDR mode
WDATA_CLR	[4]	RW	0x0	Buffer write data FIFO clear.
WDATA_ENABLE	[6]	RW	0x0	Buffer write data enable. Shifts data from data loader.
WDATA_HOLD	[5]	RW	0x0	Buffer write data FIFO hold data output (persistence).
WDATA_UPDATE	[7]	RW	0x0	Buffer write data update. Loads data into data loader.

Registers

WAV_DFICHO__TOP_2_CFG

Address: 0x000D0004

Description:

Name	Index	Type	Reset	Description
IG_LOAD_PTR	[1]	RW	0x0	Set 1 to load the IG_START_PTR as the start address for IG FIFO WR or RD. Set this bit to 0 before initiating any activity in DFI buffer.
IG_LOOP_MODE	[0]	RW	0x0	Set 1 to loop between Start pointer and Stop Pointer for IG_NUM_LOOPS times.
IG_NUM_LOOPS	[7:4]	RW	0x1	Set to non-zero value when LOOP_MODE is set 1.
IG_START_PTR	[21:16]	RW	0x0	Set to the Start Binary Pointer Address value. Make sure to choose START_PTR and STOP_PTR values such that the STOP_PTR gray code to START_PTR gray code change has a single bit transition.
IG_STOP_PTR	[13:8]	RW	0x0	Set to the Stop Binary Pointer Address value. Make sure to choose START_PTR and STOP_PTR values such that the STOP_PTR gray code to START_PTR gray code change has a single bit transition.

WAV_DFICHO__TOP_3_CFG

Address: 0x000D0008

Description:

Name	Index	Type	Reset	Description
TS_BRKPT_EN	[16]	RW	0x0	Timestamp counter Breakpoint Enable. Set 1 to enable break point. Set 0 to disable break point.
TS_BRKPT_VAL	[15:0]	RW	0x0	Timestamp counter value at which the break point is set.

WAV_DFICHO__TOP_STA

Address: 0x000D000C

Description:

Name	Index	Type	Reset	Description
EG_STATE	[5:4]	R	0x0	bit 1- Egress FIFO full, bit 0 - Egress FIFO empty.
EG_STATE_UPD	[6]	R	0x0	Toggle on this bit indicates there is valid EG FIFO read is done and empty signal status available in EG_STATE.
IG_STATE	[1:0]	R	0x0	bit 1- Ingress FIFO full, bit 0 - Ingress FIFO empty.
IG_STATE_UPD	[2]	R	0x0	Toggle on this bit indicates there is valid IG FIFO write is done and full signal status available in IG_STATE.

WAV_DFICHO__IG_DATA_CFG

Address: 0x000D0010

Description:

Name	Index	Type	Reset	Description
WDATA	[31:0]	RW	0x00000000	Ingress data to be sent to PHY datapath.

WAV_DFICHO__EG_DATA_STA

Registers

Address: 0x000D0014

Description:

Name	Index	Type	Reset	Description
RDATA	[31:0]	R	0x00000000	Egress data from PHY datapath.

WAV_DFICHO__WRC_M0_CFG

Address: 0x000D0018

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WRC_M1_CFG

Address: 0x000D001C

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WRCTRL_M0_CFG

Address: 0x000D0020

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WRCTRL_M1_CFG

Address: 0x000D0024

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__CKCTRL_M0_CFG

Address: 0x000D0028

Description:

Registers

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__CKCTRL_M1_CFG

Address: 0x000D002C

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__RDC_M0_CFG

Address: 0x000D0030

Description:

Name	Index	Type	Reset	Description
GB_MODE	[3:0]	RW	0x6	Gearbox Up mode select.

WAV_DFICHO__RDC_M1_CFG

Address: 0x000D0034

Description:

Name	Index	Type	Reset	Description
GB_MODE	[3:0]	RW	0x6	Gearbox Up mode select.

WAV_DFICHO__RCTRL_M0_CFG

Address: 0x000D0038

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[6:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__RCTRL_M1_CFG

Address: 0x000D003C

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[6:4]	RW	0x0	Cycle delay post DFI GB.

Registers

WAV_DFICHO__WCTRL_M0_CFG

Address: 0x000D0040

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[6:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WCTRL_M1_CFG

Address: 0x000D0044

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[6:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WENCTRL_M0_CFG

Address: 0x000D0048

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[7:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WENCTRL_M1_CFG

Address: 0x000D004C

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[7:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WCKCTRL_M0_CFG

Address: 0x000D0050

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[6:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WCKCTRL_M1_CFG

Registers

Address: 0x000D0054

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[6:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WRD_M0_CFG

Address: 0x000D0058

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__WRD_M1_CFG

Address: 0x000D005C

Description:

Name	Index	Type	Reset	Description
GB_MODE	[15:12]	RW	0x5	Gearbox mode select.
PIPE_EN	[0]	RW	0x0	Enable pipeline.
POST_GB_FC_DLY	[5:4]	RW	0x0	Cycle delay post DFI GB.

WAV_DFICHO__RDD_M0_CFG

Address: 0x000D0060

Description:

Name	Index	Type	Reset	Description
GB_MODE	[3:0]	RW	0x6	Gearbox Up mode select.

WAV_DFICHO__RDD_M1_CFG

Address: 0x000D0064

Description:

Name	Index	Type	Reset	Description
GB_MODE	[3:0]	RW	0x6	Gearbox Up mode select.

WAV_DFICHO__CTRL0_M0_CFG

Address: 0x000D0068

Description:

Name	Index	Type	Reset	Description
RD_INTF_PIPE_EN	[1]	RW	0x1	Set this bit 0 to Bypass DFI RD interface flop to reduce latency.

Registers

WR_INTF_PIPE_EN	[0]	RW	0x1	Set this bit 0 to bypass DFI WR interface flop to reduce latency.
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WAV_DFICHO__CTRL0_M1_CFG

Address: 0x000D006C

Description:

Name	Index	Type	Reset	Description
RD_INTF_PIPE_EN	[1]	RW	0x1	Set this bit 0 to Bypass DFI RD interface flop to reduce latency.
WR_INTF_PIPE_EN	[0]	RW	0x1	Set this bit 0 to bypass DFI WR interface flop to reduce latency.

WAV_DFICHO__CTRL1_M0_CFG

Address: 0x000D0070

Description:

Name	Index	Type	Reset	Description
CA_TRAFFIC_OVR	[6]	RW	0x1	CA WR dynamic clock gating enable override.
CA_TRAFFIC_OVR_SEL	[2]	RW	0x1	CA WR dynamic clock gating override select.
CK_TRAFFIC_OVR	[7]	RW	0x1	CK WR dynamic clock gating enable override.
CK_TRAFFIC_OVR_SEL	[3]	RW	0x1	CK WR dynamic clock gating override select.
DQS_WRTRAFFIC_OVR	[5]	RW	0x1	DQS WR dynamic clock gating enable override.
DQS_WRTRAFFIC_OVR_SEL	[1]	RW	0x1	DQS WR dynamic clock gating override select.
DQ_RDTRAFFIC_OVR	[9]	RW	0x0	DQ RD dynamic clock gating enable override.
DQ_RDTRAFFIC_OVR_SEL	[8]	RW	0x0	DQ RD dynamic clock gating enable override.
DQ_WRTRAFFIC_OVR	[4]	RW	0x1	DQ WR dynamic clock gating enable override.
DQ_WRTRAFFIC_OVR_SEL	[0]	RW	0x1	DQ WR dynamic clock gating override select.

WAV_DFICHO__CTRL1_M1_CFG

Address: 0x000D0074

Description:

Name	Index	Type	Reset	Description
CA_TRAFFIC_OVR	[6]	RW	0x1	CA WR dynamic clock gating enable override.
CA_TRAFFIC_OVR_SEL	[2]	RW	0x1	CA WR dynamic clock gating override select.
CK_TRAFFIC_OVR	[7]	RW	0x1	CK WR dynamic clock gating enable override.
CK_TRAFFIC_OVR_SEL	[3]	RW	0x1	CK WR dynamic clock gating override select.
DQS_WRTRAFFIC_OVR	[5]	RW	0x1	DQS WR dynamic clock gating enable override.
DQS_WRTRAFFIC_OVR_SEL	[1]	RW	0x1	DQS WR dynamic clock gating override select.
DQ_RDTRAFFIC_OVR	[9]	RW	0x0	DQ RD dynamic clock gating enable override.
DQ_RDTRAFFIC_OVR_SEL	[8]	RW	0x0	DQ RD dynamic clock gating enable override.
DQ_WRTRAFFIC_OVR	[4]	RW	0x1	DQ WR dynamic clock gating enable override.
DQ_WRTRAFFIC_OVR_SEL	[0]	RW	0x1	DQ WR dynamic clock gating override select.

WAV_DFICHO__CTRL2_M0_CFG

Registers

Address: 0x000D0078

Description:

Name	Index	Type	Reset	Description
CA_CLK_EN_PULSE_EXT	[11:8]	RW	0x0	DFI CA path clock enable pulse extension in number of DFI clock cycles.
CK_CLK_EN_PULSE_EXT	[15:12]	RW	0x0	DFI CK path clock enable pulse extension in number of DFI clock cycles.
DQS_WRCLK_EN_PULSE_EXT	[7:4]	RW	0x3	DFI DQS Write path clock enable pulse extension in number of DFI clock cycles.
DQ_WRCLK_EN_PULSE_EXT	[3:0]	RW	0x3	DFI DQ Write path clock enable pulse extension in number of DFI clock cycles.
RDCLK_EN_PULSE_EXT	[19:16]	RW	0xF	DFI DQ Read path clock enable pulse extension in number of PHY clock cycles.

WAV_DFICHO__CTRL2_M1_CFG

Address: 0x000D007C

Description:

Name	Index	Type	Reset	Description
CA_CLK_EN_PULSE_EXT	[11:8]	RW	0x0	DFI CA path clock enable pulse extension in number of DFI clock cycles.
CK_CLK_EN_PULSE_EXT	[15:12]	RW	0x0	DFI CK path clock enable pulse extension in number of DFI clock cycles.
DQS_WRCLK_EN_PULSE_EXT	[7:4]	RW	0x3	DFI DQS Write path clock enable pulse extension in number of DFI clock cycles.
DQ_WRCLK_EN_PULSE_EXT	[3:0]	RW	0x3	DFI DQ Write path clock enable pulse extension in number of DFI clock cycles.
RDCLK_EN_PULSE_EXT	[19:16]	RW	0xF	DFI DQ Read path clock enable pulse extension in number of PHY clock cycles.

WAV_DFICHO__CTRL3_M0_CFG

Address: 0x000D0080

Description:

Name	Index	Type	Reset	Description
WRD_CS_PHASE_EXT	[5:0]	RW	0x0	DFI WR CS phase extension.
WRD_EN_PHASE_EXT	[13:8]	RW	0x2	DFI Write data enable phase extension.
WRD_OE_PHASE_EXT	[21:16]	RW	0x2	DFI Output Enable phase extension.

WAV_DFICHO__CTRL3_M1_CFG

Address: 0x000D0084

Description:

Name	Index	Type	Reset	Description
WRD_CS_PHASE_EXT	[5:0]	RW	0x0	DFI WR CS phase extension.
WRD_EN_PHASE_EXT	[13:8]	RW	0x2	DFI Write data enable phase extension.
WRD_OE_PHASE_EXT	[21:16]	RW	0x2	DFI Output Enable phase extension.

Registers

WAV_DFICHO__CTRL4_M0_CFG

Address: 0x000D0088

Description:

Name	Index	Type	Reset	Description
WCK_CS_PHASE_EXT	[13:8]	RW	0x0	DFI WCK CS phase extension.
WCK_OE_PHASE_EXT	[5:0]	RW	0x2	DFI Output Enable phase extension.

WAV_DFICHO__CTRL4_M1_CFG

Address: 0x000D008C

Description:

Name	Index	Type	Reset	Description
WCK_CS_PHASE_EXT	[13:8]	RW	0x0	DFI WCK CS phase extension.
WCK_OE_PHASE_EXT	[5:0]	RW	0x2	DFI Output Enable phase extension.

WAV_DFICHO__CTRL5_M0_CFG

Address: 0x000D0090

Description:

Name	Index	Type	Reset	Description
IE_PHASE_EXT	[13:8]	RW	0x0	DFI Input Enable phase extension.
RCS_PHASE_EXT	[5:0]	RW	0x0	DFI RD CS phase extension.
REN_PHASE_EXT	[29:24]	RW	0x0	DFI RDATA_EN/REN phase extension.
RE_PHASE_EXT	[21:16]	RW	0x0	DFI RX Enable phase extension.

WAV_DFICHO__CTRL5_M1_CFG

Address: 0x000D0094

Description:

Name	Index	Type	Reset	Description
IE_PHASE_EXT	[13:8]	RW	0x0	DFI Input Enable phase extension.
RCS_PHASE_EXT	[5:0]	RW	0x0	DFI RD CS phase extension.
REN_PHASE_EXT	[29:24]	RW	0x0	DFI RDATA_EN/REN phase extension.
RE_PHASE_EXT	[21:16]	RW	0x0	DFI RX Enable phase extension.

WAV_CH0_DQ0__TOP_CFG

Address: 0x000F0000

Description:

Name	Index	Type	Reset	Description
FIFO_CLR	[8]	RW	0x0	FIFO clear.
RCS_SW_OVR	[2]	RW	0x0	Read Chip Select Override.
RCS_SW_OVR_VAL	[3]	RW	0x0	Read Chip Select Override value.
TRAINING_MODE	[9]	RW	0x0	Training Mode.

Registers

WCS_SW_OVR	[0]	RW	0x0	Write Chip Select Override.
WCS_SW_OVR_VAL	[1]	RW	0x0	Write Chip Select Override value.

WAV_CH0_DQ0__TOP_STA

Address: 0x000F0004

Description:

Name	Index	Type	Reset	Description
RCS	[1]	R	0x0	Read Chip Select status.
WCS	[0]	R	0x0	Write Chip Select status.

WAV_CH0_DQ0__DQ_RX_BSCAN_STA

Address: 0x000F0008

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	R	0x000	Boundary Scan per-bit value.

WAV_CH0_DQ0__DQ_RX_M0_CFG

Address: 0x000F000C

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH0_DQ0__DQ_RX_M1_CFG

Address: 0x000F0010

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_0

Address: 0x000F0014

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_1

Address: 0x000F0018

Description:

Name	Index	Type	Reset	Description

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_2

Address: 0x000F001C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_3

Address: 0x000F0020

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_4

Address: 0x000F0024

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_5

Address: 0x000F0028

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_6

Address: 0x000F002C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_7

Address: 0x000F0030

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R0_CFG_8

Address: 0x000F0034

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_0

Address: 0x000F0038

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_1

Address: 0x000F003C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_2

Address: 0x000F0040

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_3

Address: 0x000F0044

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_4

Address: 0x000F0048

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_5

Address: 0x000F004C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_6

Address: 0x000F0050

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_7

Address: 0x000F0054

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M0_R1_CFG_8

Address: 0x000F0058

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_0

Address: 0x000F005C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_1

Address: 0x000F0060

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_2

Address: 0x000F0064

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_3

Address: 0x000F0068

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_4

Address: 0x000F006C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_5

Address: 0x000F0070

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_6

Address: 0x000F0074

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_7

Address: 0x000F0078

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R0_CFG_8

Address: 0x000F007C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_0

Address: 0x000F0080

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_1

Address: 0x000F0084

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_2

Address: 0x000F0088

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_3

Address: 0x000F008C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_4

Address: 0x000F0090

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_5

Address: 0x000F0094

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_6

Address: 0x000F0098

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_7

Address: 0x000F009C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH0_DQ0__DQ_RX_IO_M1_R1_CFG_8

Address: 0x000F00A0

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ0__DQ_RX_IO_STA

Address: 0x000F00A4

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_0

Address: 0x000F00A8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_1

Address: 0x000F00AC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_2

Address: 0x000F00B0

Description:

Registers

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_3

Address: 0x000F00B4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_4

Address: 0x000F00B8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_5

Address: 0x000F00BC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.

Registers

CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_6

Address: 0x000F00C0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_7

Address: 0x000F00C4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R0_CFG_8

Address: 0x000F00C8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.

Registers

CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_0

Address: 0x000F00CC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_1

Address: 0x000F00D0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_2

Address: 0x000F00D4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.

Registers

CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_3

Address: 0x000F00D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_4

Address: 0x000F00DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_5

Address: 0x000F00E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.

Registers

CAL_DIR_90	[17]	RW	0x0	Calibration direction.
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WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_6

Address: 0x000F00E4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_7

Address: 0x000F00E8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M0_R1_CFG_8

Address: 0x000F00EC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_0

Address: 0x000F00F0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_1

Address: 0x000F00F4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_2

Address: 0x000F00F8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_3

Address: 0x000F00FC

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_4

Address: 0x000F0100

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_5

Address: 0x000F0104

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_6

Address: 0x000F0108

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_7

Address: 0x000F010C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R0_CFG_8

Address: 0x000F0110

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_0

Address: 0x000F0114

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_1

Address: 0x000F0118

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_2

Address: 0x000F011C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_3

Address: 0x000F0120

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_4

Address: 0x000F0124

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_5

Address: 0x000F0128

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_6

Address: 0x000F012C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_7

Address: 0x000F0130

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_M1_R1_CFG_8

Address: 0x000F0134

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_0

Address: 0x000F0138

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_1

Address: 0x000F013C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_2

Address: 0x000F0140

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_3

Address: 0x000F0144

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_4

Address: 0x000F0148

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_5

Address: 0x000F014C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_6

Address: 0x000F0150

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_7

Address: 0x000F0154

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_8

Address: 0x000F0158

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_0

Address: 0x000F015C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_1

Address: 0x000F0160

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_2

Address: 0x000F0164

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_3

Address: 0x000F0168

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_4

Address: 0x000F016C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_5

Address: 0x000F0170

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_6

Address: 0x000F0174

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_7

Address: 0x000F0178

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_8

Address: 0x000F017C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_0

Address: 0x000F0180

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_1

Address: 0x000F0184

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_2

Address: 0x000F0188

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_3

Address: 0x000F018C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_4

Address: 0x000F0190

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_5

Address: 0x000F0194

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_6

Address: 0x000F0198

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_7

Address: 0x000F019C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_8

Address: 0x000F01A0

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_0

Address: 0x000F01A4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_1

Address: 0x000F01A8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_2

Address: 0x000F01AC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_3

Address: 0x000F01B0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_4

Address: 0x000F01B4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_5

Address: 0x000F01B8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_6

Address: 0x000F01BC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_7

Address: 0x000F01C0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_8

Address: 0x000F01C4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_RX_SA_STA_0

Address: 0x000F01C8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_1

Address: 0x000F01CC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_2

Address: 0x000F01D0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_3

Address: 0x000F01D4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_4

Address: 0x000F01D8

Registers

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_5

Address: 0x000F01DC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_6

Address: 0x000F01E0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_7

Address: 0x000F01E4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ0__DQ_RX_SA_STA_8

Address: 0x000F01E8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.

Registers

SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.
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WAV_CH0_DQ0__DQ_TX_BSCAN_CFG

Address: 0x000F01EC

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	RW	0x00	Boundary Scan per-bit value.

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_0

Address: 0x000F01F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_1

Address: 0x000F01F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_2

Address: 0x000F01F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_3

Address: 0x000F01FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_4

Address: 0x000F0200

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_5

Address: 0x000F0204

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_6

Address: 0x000F0208

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_7

Address: 0x000F020C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_8

Address: 0x000F0210

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_0

Address: 0x000F0214

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_1

Address: 0x000F0218

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_2

Address: 0x000F021C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_3

Address: 0x000F0220

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_4

Address: 0x000F0224

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_5

Address: 0x000F0228

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_6

Address: 0x000F022C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_7

Address: 0x000F0230

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH0_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_8

Address: 0x000F0234

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_0

Address: 0x000F0238

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_1

Address: 0x000F023C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_2

Address: 0x000F0240

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_3

Address: 0x000F0244

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_4

Address: 0x000F0248

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_5

Address: 0x000F024C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_6

Address: 0x000F0250

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_7

Address: 0x000F0254

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_8

Address: 0x000F0258

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_0

Address: 0x000F025C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_1

Address: 0x000F0260

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_2

Address: 0x000F0264

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_3

Address: 0x000F0268

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_4

Address: 0x000F026C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_5

Address: 0x000F0270

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_6

Address: 0x000F0274

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_7

Address: 0x000F0278

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH0_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_8

Address: 0x000F027C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQ_TX_ODR_PI_M0_R0_CFG

Address: 0x000F0280

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_ODR_PI_M0_R1_CFG

Address: 0x000F0284

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_ODR_PI_M1_R0_CFG

Address: 0x000F0288

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_ODR_PI_M1_R1_CFG

Address: 0x000F028C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M0_R0_CFG

Address: 0x000F0290

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M0_R1_CFG

Address: 0x000F0294

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M1_R0_CFG

Address: 0x000F0298

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_QDR_PI_0_M1_R1_CFG

Address: 0x000F029C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M0_R0_CFG

Address: 0x000F02A0

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M0_R1_CFG

Address: 0x000F02A4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M1_R0_CFG

Address: 0x000F02A8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_QDR_PI_1_M1_R1_CFG

Address: 0x000F02AC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M0_R0_CFG

Address: 0x000F02B0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M0_R1_CFG

Address: 0x000F02B4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M1_R0_CFG

Address: 0x000F02B8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_DDR_PI_0_M1_R1_CFG

Address: 0x000F02BC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M0_R0_CFG

Address: 0x000F02C0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M0_R1_CFG

Address: 0x000F02C4

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M1_R0_CFG

Address: 0x000F02C8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_DDR_PI_1_M1_R1_CFG

Address: 0x000F02CC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_PI_RT_M0_R0_CFG

Address: 0x000F02D0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_PI_RT_M0_R1_CFG

Address: 0x000F02D4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ0__DQ_TX_PI_RT_M1_R0_CFG

Address: 0x000F02D8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_PI_RT_M1_R1_CFG

Address: 0x000F02DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQ_TX_RT_M0_R0_CFG

Address: 0x000F02E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ0__DQ_TX_RT_M0_R1_CFG

Address: 0x000F02E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ0__DQ_TX_RT_M1_R0_CFG

Address: 0x000F02E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ0__DQ_TX_RT_M1_R1_CFG

Address: 0x000F02EC

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN	[8:0]	RW	0x000	Pipeline enable.
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WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_0

Address: 0x000F02F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_1

Address: 0x000F02F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_2

Address: 0x000F02F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_3

Address: 0x000F02FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_4

Address: 0x000F0300

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_5

Address: 0x000F0304

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_6

Address: 0x000F0308

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_7

Address: 0x000F030C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R0_CFG_8

Address: 0x000F0310

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_0

Address: 0x000F0314

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_1

Address: 0x000F0318

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_2

Address: 0x000F031C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_3

Address: 0x000F0320

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_4

Address: 0x000F0324

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_5

Address: 0x000F0328

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_6

Address: 0x000F032C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_7

Address: 0x000F0330

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M0_R1_CFG_8

Address: 0x000F0334

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_0

Address: 0x000F0338

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_1

Address: 0x000F033C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_2

Address: 0x000F0340

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_3

Address: 0x000F0344

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_4

Address: 0x000F0348

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_5

Address: 0x000F034C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_6

Address: 0x000F0350

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_7

Address: 0x000F0354

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R0_CFG_8

Address: 0x000F0358

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_0

Address: 0x000F035C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_1

Address: 0x000F0360

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_2

Address: 0x000F0364

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_3

Address: 0x000F0368

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_4

Address: 0x000F036C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_5

Address: 0x000F0370

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_6

Address: 0x000F0374

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_7

Address: 0x000F0378

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_M1_R1_CFG_8

Address: 0x000F037C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x000F0380

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x000F0384

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x000F0388

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x000F038C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x000F0390

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x000F0394

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x000F0398

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x000F039C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x000F03A0

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x000F03A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x000F03A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x000F03AC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x000F03B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x000F03B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x000F03B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x000F03BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x000F03C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x000F03C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x000F03C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x000F03CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x000F03D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x000F03D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x000F03D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x000F03DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x000F03E0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x000F03E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x000F03E8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x000F03EC

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x000F03F0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x000F03F4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x000F03F8

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x000F03FC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x000F0400

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x000F0404

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x000F0408

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x000F040C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x000F0410

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_1

Address: 0x000F0414

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_2

Address: 0x000F0418

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x000F041C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_4

Address: 0x000F0420

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x000F0424

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x000F0428

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_7

Address: 0x000F042C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_8

Address: 0x000F0430

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_0

Address: 0x000F0434

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_1

Address: 0x000F0438

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x000F043C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x000F0440

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x000F0444

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x000F0448

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x000F044C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x000F0450

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x000F0454

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x000F0458

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x000F045C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x000F0460

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x000F0464

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x000F0468

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_5

Address: 0x000F046C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x000F0470

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x000F0474

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_8

Address: 0x000F0478

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_0

Address: 0x000F047C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_1

Address: 0x000F0480

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_2

Address: 0x000F0484

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x000F0488

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x000F048C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x000F0490

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x000F0494

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x000F0498

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x000F049C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_0

Address: 0x000F04A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_1

Address: 0x000F04A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_2

Address: 0x000F04A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_3

Address: 0x000F04AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
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WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_4

Address: 0x000F04B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_5

Address: 0x000F04B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_6

Address: 0x000F04B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_7

Address: 0x000F04BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R0_CFG_8

Address: 0x000F04C0

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_0

Address: 0x000F04C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_1

Address: 0x000F04C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_2

Address: 0x000F04CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_3

Address: 0x000F04D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_4

Address: 0x000F04D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_5

Address: 0x000F04D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_6

Address: 0x000F04DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_7

Address: 0x000F04E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M0_R1_CFG_8

Address: 0x000F04E4

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_0

Address: 0x000F04E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_1

Address: 0x000F04EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_2

Address: 0x000F04F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_3

Address: 0x000F04F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_4

Address: 0x000F04F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_5

Address: 0x000F04FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_6

Address: 0x000F0500

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_7

Address: 0x000F0504

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R0_CFG_8

Address: 0x000F0508

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_0

Address: 0x000F050C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_1

Address: 0x000F0510

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_2

Address: 0x000F0514

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_3

Address: 0x000F0518

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_4

Address: 0x000F051C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_5

Address: 0x000F0520

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_6

Address: 0x000F0524

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_7

Address: 0x000F0528

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_M1_R1_CFG_8

Address: 0x000F052C

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x000F0530

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x000F0534

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x000F0538

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x000F053C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x000F0540

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x000F0544

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x000F0548

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x000F054C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x000F0550

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x000F0554

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x000F0558

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x000F055C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x000F0560

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x000F0564

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x000F0568

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x000F056C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x000F0570

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x000F0574

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x000F0578

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x000F057C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x000F0580

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x000F0584

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x000F0588

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x000F058C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x000F0590

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x000F0594

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x000F0598

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x000F059C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x000F05A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x000F05A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x000F05A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x000F05AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x000F05B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x000F05B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x000F05B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x000F05BC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_0

Address: 0x000F05C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_1

Address: 0x000F05C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_2

Address: 0x000F05C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_3

Address: 0x000F05CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_4

Address: 0x000F05D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_5

Registers

Address: 0x000F05D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_6

Address: 0x000F05D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_7

Address: 0x000F05DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R0_CFG_8

Address: 0x000F05E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_0

Address: 0x000F05E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_1

Address: 0x000F05E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_2

Address: 0x000F05EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_3

Address: 0x000F05F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_4

Address: 0x000F05F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_5

Address: 0x000F05F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_6

Address: 0x000F05FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_7

Address: 0x000F0600

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH0_DQ0__DQ_TX_QDR_M0_R1_CFG_8

Address: 0x000F0604

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_0

Address: 0x000F0608

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_1

Address: 0x000F060C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_2

Address: 0x000F0610

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_3

Address: 0x000F0614

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_4

Address: 0x000F0618

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_5

Address: 0x000F061C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_6

Address: 0x000F0620

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_7

Address: 0x000F0624

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R0_CFG_8

Address: 0x000F0628

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_0

Address: 0x000F062C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_1

Registers

Address: 0x000F0630

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_2

Address: 0x000F0634

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_3

Address: 0x000F0638

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_4

Address: 0x000F063C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_5

Address: 0x000F0640

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_6

Address: 0x000F0644

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_7

Address: 0x000F0648

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_M1_R1_CFG_8

Address: 0x000F064C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x000F0650

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x000F0654

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x000F0658

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x000F065C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x000F0660

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x000F0664

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x000F0668

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x000F066C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x000F0670

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x000F0674

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x000F0678

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x000F067C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x000F0680

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x000F0684

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x000F0688

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_6

Registers

Address: 0x000F068C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x000F0690

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x000F0694

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x000F0698

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x000F069C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x000F06A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x000F06A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x000F06A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x000F06AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x000F06B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x000F06B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x000F06B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x000F06BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x000F06C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x000F06C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x000F06C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x000F06CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x000F06D0

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x000F06D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x000F06D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x000F06DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_0

Address: 0x000F06E0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_1

Address: 0x000F06E4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

Registers

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_2

Address: 0x000F06E8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_3

Address: 0x000F06EC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_4

Address: 0x000F06F0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_5

Address: 0x000F06F4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_6

Address: 0x000F06F8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_7

Registers

Address: 0x000F06FC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R0_CFG_8

Address: 0x000F0700

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_0

Address: 0x000F0704

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_1

Address: 0x000F0708

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_2

Address: 0x000F070C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_3

Address: 0x000F0710

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_4

Address: 0x000F0714

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_5

Address: 0x000F0718

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_6

Address: 0x000F071C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_7

Address: 0x000F0720

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M0_R1_CFG_8

Address: 0x000F0724

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_0

Address: 0x000F0728

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_1

Address: 0x000F072C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_2

Address: 0x000F0730

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_3

Address: 0x000F0734

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_4

Address: 0x000F0738

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_5

Address: 0x000F073C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_6

Address: 0x000F0740

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_7

Address: 0x000F0744

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R0_CFG_8

Address: 0x000F0748

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_0

Address: 0x000F074C

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_1

Address: 0x000F0750

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_2

Address: 0x000F0754

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_3

Address: 0x000F0758

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_4

Address: 0x000F075C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_5

Address: 0x000F0760

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_6

Address: 0x000F0764

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_7

Address: 0x000F0768

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_LPDE_M1_R1_CFG_8

Address: 0x000F076C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_0

Address: 0x000F0770

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_1

Registers

Address: 0x000F0774

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_2

Address: 0x000F0778

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_3

Address: 0x000F077C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_4

Address: 0x000F0780

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.

Registers

TX_IMPD	[8:6]	RW	0x1	TX impedance code.
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WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_5

Address: 0x000F0784

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_6

Address: 0x000F0788

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_7

Address: 0x000F078C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M0_CFG_8

Address: 0x000F0790

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.

Registers

RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_0

Address: 0x000F0794

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_1

Address: 0x000F0798

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_2

Address: 0x000F079C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_3

Address: 0x000F07A0

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_4

Address: 0x000F07A4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_5

Address: 0x000F07A8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_6

Address: 0x000F07AC

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_7

Address: 0x000F07B0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQ_TX_IO_M1_CFG_8

Address: 0x000F07B4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQS_RX_M0_CFG

Address: 0x000F07B8

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH0_DQ0__DQS_RX_M1_CFG

Address: 0x000F07BC

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH0_DQ0__DQS_RX_BSCAN_STA

Registers

Address: 0x000F07C0

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	R	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M0_R0_CFG

Address: 0x000F07C4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M0_R1_CFG

Address: 0x000F07C8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M1_R0_CFG

Address: 0x000F07CC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_RX_SDR_LPDE_M1_R1_CFG

Address: 0x000F07D0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_RX_REN_PI_M0_R0_CFG

Address: 0x000F07D4

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_REN_PI_M0_R1_CFG

Address: 0x000F07D8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_REN_PI_M1_R0_CFG

Address: 0x000F07DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_REN_PI_M1_R1_CFG

Address: 0x000F07E0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RCS_PI_M0_R0_CFG

Address: 0x000F07E4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ0__DQS_RX_RCS_PI_M0_R1_CFG

Address: 0x000F07E8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RCS_PI_M1_R0_CFG

Address: 0x000F07EC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RCS_PI_M1_R1_CFG

Address: 0x000F07F0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M0_R0_CFG

Address: 0x000F07F4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M0_R1_CFG

Address: 0x000F07F8

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M1_R0_CFG

Address: 0x000F07FC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RDQS_PI_0_M1_R1_CFG

Address: 0x000F0800

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M0_R0_CFG

Address: 0x000F0804

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M0_R1_CFG

Address: 0x000F0808

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M1_R0_CFG

Address: 0x000F080C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_RDQS_PI_1_M1_R1_CFG

Address: 0x000F0810

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_RX_PI_STA

Address: 0x000F0814

Description:

Name	Index	Type	Reset	Description
RCS_PI_PHASE	[1]	R	0x0	Indicates the phase of RE_PI output clock wrt RCS.
REN_PI_PHASE	[0]	R	0x0	Indicates the phase of RE_PI output clock wrt REN.

WAV_CH0_DQ0__DQS_RX_IO_M0_R0_CFG_0

Address: 0x000F0818

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ0__DQS_RX_IO_M0_R0_CFG_1

Address: 0x000F081C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ0__DQS_RX_IO_M0_R1_CFG_0

Registers

Address: 0x000F0820

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ0__DQS_RX_IO_M0_R1_CFG_1

Address: 0x000F0824

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ0__DQS_RX_IO_M1_R0_CFG_0

Address: 0x000F0828

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ0__DQS_RX_IO_M1_R0_CFG_1

Address: 0x000F082C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ0__DQS_RX_IO_M1_R1_CFG_0

Address: 0x000F0830

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ0__DQS_RX_IO_M1_R1_CFG_1

Address: 0x000F0834

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

Registers

WAV_CH0_DQ0__DQS_RX_IO_CMN_M0_R0_CFG

Address: 0x000F0838

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for edge detect EN and IE.

WAV_CH0_DQ0__DQS_RX_IO_CMN_M0_R1_CFG

Address: 0x000F083C

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_DQ0__DQS_RX_IO_CMN_M1_R0_CFG

Address: 0x000F0840

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.

Registers

RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_DQ0__DQS_RX_IO_CMN_M1_R1_CFG

Address: 0x000F0844

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_DQ0__DQS_RX_IO_STA

Address: 0x000F0848

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH0_DQ0__DQS_RX_SA_M0_R0_CFG_0

Address: 0x000F084C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_M0_R0_CFG_1

Address: 0x000F0850

Description:

Registers

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_M0_R1_CFG_0

Address: 0x000F0854

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_M0_R1_CFG_1

Address: 0x000F0858

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_M1_R0_CFG_0

Address: 0x000F085C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.

Registers

CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_M1_R0_CFG_1

Address: 0x000F0860

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_M1_R1_CFG_0

Address: 0x000F0864

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_M1_R1_CFG_1

Address: 0x000F0868

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.

Registers

CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ0__DQS_RX_SA_CMN_CFG

Address: 0x000F086C

Description:

Name	Index	Type	Reset	Description
CAL_EN_0_180	[1]	RW	0x0	Calibration enable.
CAL_EN_90_270	[3]	RW	0x0	Calibration enable.
OVR_EN_0_180	[0]	RW	0x1	Software override value of SA_Enable.
OVR_EN_90_270	[2]	RW	0x1	Software override value of SA_Enable.
SW_OVR	[4]	RW	0x0	Software override for SA enable.

WAV_CH0_DQ0__DQS_TX_M0_CFG

Address: 0x000F0870

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH0_DQ0__DQS_TX_M1_CFG

Address: 0x000F0874

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH0_DQ0__DQS_TX_BSCAN_CTRL_CFG

Address: 0x000F0878

Description:

Name	Index	Type	Reset	Description
IE	[0]	RW	0x0	Boundary Scan IE.
OE	[1]	RW	0x0	Boundary Scan OE.

WAV_CH0_DQ0__DQS_TX_BSCAN_CFG

Address: 0x000F087C

Registers

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	RW	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_0

Address: 0x000F0880

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_1

Address: 0x000F0884

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_2

Address: 0x000F0888

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_3

Address: 0x000F088C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_4

Address: 0x000F0890

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_5

Address: 0x000F0894

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_6

Address: 0x000F0898

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_7

Address: 0x000F089C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_8

Address: 0x000F08A0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_0

Address: 0x000F08A4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_1

Address: 0x000F08A8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_2

Address: 0x000F08AC

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_3

Address: 0x000F08B0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_4

Address: 0x000F08B4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_5

Address: 0x000F08B8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_6

Address: 0x000F08BC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_7

Address: 0x000F08C0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_8

Address: 0x000F08C4

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_0

Address: 0x000F08C8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_1

Address: 0x000F08CC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_2

Address: 0x000F08D0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_3

Address: 0x000F08D4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_4

Address: 0x000F08D8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_5

Address: 0x000F08DC

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_6

Address: 0x000F08E0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_7

Address: 0x000F08E4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_8

Address: 0x000F08E8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_0

Address: 0x000F08EC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_1

Address: 0x000F08F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_2

Address: 0x000F08F4

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_3

Address: 0x000F08F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_4

Address: 0x000F08FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_5

Address: 0x000F0900

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_6

Address: 0x000F0904

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_7

Address: 0x000F0908

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_8

Address: 0x000F090C

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ0__DQS_TX_ODR_PI_M0_R0_CFG

Address: 0x000F0910

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_ODR_PI_M0_R1_CFG

Address: 0x000F0914

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_ODR_PI_M1_R0_CFG

Address: 0x000F0918

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_ODR_PI_M1_R1_CFG

Address: 0x000F091C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M0_R0_CFG

Registers

Address: 0x000F0920

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M0_R1_CFG

Address: 0x000F0924

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M1_R0_CFG

Address: 0x000F0928

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_0_M1_R1_CFG

Address: 0x000F092C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M0_R0_CFG

Address: 0x000F0930

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.

Registers

GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M0_R1_CFG

Address: 0x000F0934

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M1_R0_CFG

Address: 0x000F0938

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_QDR_PI_1_M1_R1_CFG

Address: 0x000F093C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M0_R0_CFG

Address: 0x000F0940

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M0_R1_CFG

Address: 0x000F0944

Registers

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M1_R0_CFG

Address: 0x000F0948

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DDR_PI_0_M1_R1_CFG

Address: 0x000F094C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M0_R0_CFG

Address: 0x000F0950

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M0_R1_CFG

Address: 0x000F0954

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M1_R0_CFG

Address: 0x000F0958

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DDR_PI_1_M1_R1_CFG

Address: 0x000F095C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_PI_RT_M0_R0_CFG

Address: 0x000F0960

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_PI_RT_M0_R1_CFG

Address: 0x000F0964

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_PI_RT_M1_R0_CFG

Address: 0x000F0968

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_PI_RT_M1_R1_CFG

Address: 0x000F096C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_SDR_PI_M0_R0_CFG

Address: 0x000F0970

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_SDR_PI_M0_R1_CFG

Address: 0x000F0974

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_SDR_PI_M1_R0_CFG

Address: 0x000F0978

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ0__DQS_TX_SDR_PI_M1_R1_CFG

Address: 0x000F097C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DFI_PI_M0_R0_CFG

Address: 0x000F0980

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DFI_PI_M0_R1_CFG

Address: 0x000F0984

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DFI_PI_M1_R0_CFG

Address: 0x000F0988

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_DFI_PI_M1_R1_CFG

Address: 0x000F098C

Description:

Name	Index	Type	Reset	Description

Registers

EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other PIs.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ0__DQS_TX_RT_M0_R0_CFG

Address: 0x000F0990

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ0__DQS_TX_RT_M0_R1_CFG

Address: 0x000F0994

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ0__DQS_TX_RT_M1_R0_CFG

Address: 0x000F0998

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ0__DQS_TX_RT_M1_R1_CFG

Address: 0x000F099C

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_0

Address: 0x000F09A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.

Registers

PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.
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WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_1

Address: 0x000F09A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_2

Address: 0x000F09A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_3

Address: 0x000F09AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_4

Address: 0x000F09B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_5

Address: 0x000F09B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_6

Address: 0x000F09B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_7

Address: 0x000F09BC

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R0_CFG_8

Address: 0x000F09C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_0

Address: 0x000F09C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_1

Address: 0x000F09C8

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_2

Address: 0x000F09CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_3

Address: 0x000F09D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_4

Address: 0x000F09D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_5

Address: 0x000F09D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_6

Address: 0x000F09DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_7

Address: 0x000F09E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M0_R1_CFG_8

Address: 0x000F09E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_0

Address: 0x000F09E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_1

Address: 0x000F09EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_2

Address: 0x000F09F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_3

Address: 0x000F09F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_4

Address: 0x000F09F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_5

Address: 0x000F09FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_6

Address: 0x000FOA00

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_7

Address: 0x000FOA04

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R0_CFG_8

Address: 0x000FOA08

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_0

Address: 0x000F0A0C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_1

Address: 0x000F0A10

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_2

Address: 0x000F0A14

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_3

Address: 0x000F0A18

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_4

Address: 0x000F0A1C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_5

Address: 0x000F0A20

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_6

Address: 0x000F0A24

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_7

Address: 0x000F0A28

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_M1_R1_CFG_8

Address: 0x000F0A2C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x000F0A30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x000F0A34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x000F0A38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x000F0A3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x000F0A40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x000F0A44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x000F0A48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x000F0A4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x000F0A50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x000F0A54

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x000F0A58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x000F0A5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x000F0A60

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x000F0A64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x000F0A68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x000F0A6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x000F0A70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x000F0A74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x000F0A78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x000F0A7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x000F0A80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x000F0A84

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x000F0A88

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x000F0A8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x000F0A90

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x000F0A94

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x000F0A98

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x000F0A9C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x000FOAA0

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x000F0AA4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x000F0AA8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x000F0AAC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x000FOAB0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x000FOAB4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x000FOAB8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x000FOABC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x000FOAC0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_1

Address: 0x000FOAC4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_2

Address: 0x000F0AC8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x000F0ACC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_4

Address: 0x000FOAD0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x000F0AD4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x000F0AD8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x000F0ADC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_8

Address: 0x000FOAE0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R1_CFG_0

Address: 0x000FOAE4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R1_CFG_1

Address: 0x000FOAE8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R1_CFG_2

Address: 0x000FOAEC

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x000FOAF0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x000FOAF4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x000FOAF8

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x000FOAFC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x000FOB00

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x000FOB04

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x000F0B08

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x000F0B0C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x000F0B10

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x000F0B14

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x000F0B18

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_5

Address: 0x000F0B1C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x000F0B20

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x000F0B24

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_8

Address: 0x000F0B28

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_0

Address: 0x000F0B2C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_1

Address: 0x000F0B30

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_2

Address: 0x000F0B34

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_3

Address: 0x000F0B38

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x000F0B3C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x000F0B40

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x000F0B44

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x000F0B48

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x000F0B4C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_0

Address: 0x000F0B50

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_1

Address: 0x000F0B54

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_2

Address: 0x000F0B58

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_3

Address: 0x000F0B5C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_4

Address: 0x000F0B60

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_5

Address: 0x000F0B64

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_6

Address: 0x000F0B68

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_7

Address: 0x000F0B6C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R0_CFG_8

Address: 0x000F0B70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_0

Address: 0x000F0B74

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
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WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_1

Address: 0x000F0B78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_2

Address: 0x000F0B7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_3

Address: 0x000F0B80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_4

Address: 0x000F0B84

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_5

Address: 0x000F0B88

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_6

Address: 0x000F0B8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_7

Address: 0x000F0B90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M0_R1_CFG_8

Address: 0x000F0B94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_0

Address: 0x000F0B98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_1

Address: 0x000F0B9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_2

Address: 0x000F0BA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_3

Address: 0x000F0BA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_4

Address: 0x000F0BA8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_5

Address: 0x000F0BAC

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_6

Address: 0x000F0BB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_7

Address: 0x000F0BB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R0_CFG_8

Address: 0x000F0BB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_0

Address: 0x000F0BBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_1

Address: 0x000F0BC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_2

Address: 0x000F0BC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_3

Address: 0x000F0BC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_4

Address: 0x000F0BCC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_5

Address: 0x000F0BD0

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_6

Address: 0x000F0BD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_7

Address: 0x000F0BD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_M1_R1_CFG_8

Address: 0x000F0BDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x000F0BE0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x000F0BE4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x000F0BE8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x000F0BEC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x000F0BF0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x000F0BF4

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x000F0BF8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x000F0BFC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x000F0C00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x000F0C04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x000F0C08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x000F0C0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x000F0C10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x000F0C14

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x000F0C18

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x000F0C1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x000F0C20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x000F0C24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x000F0C28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x000F0C2C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x000F0C30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x000F0C34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x000F0C38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x000F0C3C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x000F0C40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x000F0C44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x000F0C48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x000F0C4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x000F0C50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x000F0C54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x000F0C58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x000F0C5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x000F0C60

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x000F0C64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x000F0C68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x000F0C6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_0

Address: 0x000F0C70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_1

Address: 0x000F0C74

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_2

Address: 0x000F0C78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_3

Address: 0x000F0C7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_4

Address: 0x000F0C80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_5

Address: 0x000F0C84

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_6

Address: 0x000F0C88

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_7

Registers

Address: 0x000F0C8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R0_CFG_8

Address: 0x000F0C90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_0

Address: 0x000F0C94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_1

Address: 0x000F0C98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_2

Address: 0x000F0C9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_3

Address: 0x000FOCA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_4

Address: 0x000F0CA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_5

Address: 0x000F0CA8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_6

Address: 0x000F0CAC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_7

Address: 0x000F0CB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M0_R1_CFG_8

Address: 0x000F0CB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_0

Address: 0x000F0CB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_1

Address: 0x000F0CBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_2

Address: 0x000F0CC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_3

Address: 0x000F0CC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_4

Address: 0x000F0CC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_5

Address: 0x000F0CCC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_6

Address: 0x000F0CD0

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_7

Address: 0x000F0CD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R0_CFG_8

Address: 0x000F0CD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_0

Address: 0x000F0CDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_1

Address: 0x000F0CEO

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_2

Address: 0x000F0CE4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_3

Registers

Address: 0x000F0CE8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_4

Address: 0x000F0CEC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_5

Address: 0x000F0CF0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_6

Address: 0x000F0CF4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_7

Address: 0x000F0CF8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ0__DQS_TX_QDR_M1_R1_CFG_8

Address: 0x000F0CFc

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x000F0D00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x000F0D04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x000F0D08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x000F0D0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x000F0D10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x000F0D14

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x000F0D18

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x000F0D1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x000F0D20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x000F0D24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x000F0D28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x000F0D2C

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x000F0D30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x000F0D34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x000F0D38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x000F0D3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x000F0D40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_8

Registers

Address: 0x000F0D44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x000F0D48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x000F0D4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x000F0D50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x000F0D54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x000F0D58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x000F0D5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x000F0D60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x000F0D64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x000F0D68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x000F0D6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x000F0D70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x000F0D74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x000F0D78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x000F0D7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x000F0D80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x000F0D84

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x000F0D88

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x000F0D8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ0__DQS_TX_LPDE_M0_R0_CFG_0

Address: 0x000F0D90

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_LPDE_M0_R0_CFG_1

Address: 0x000F0D94

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_LPDE_M0_R1_CFG_0

Address: 0x000F0D98

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_LPDE_M0_R1_CFG_1

Address: 0x000F0D9C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_LPDE_M1_R0_CFG_0

Address: 0x000F0DA0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_LPDE_M1_R0_CFG_1

Address: 0x000F0DA4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_LPDE_M1_R1_CFG_0

Address: 0x000F0DA8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_LPDE_M1_R1_CFG_1

Address: 0x000F0DAC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ0__DQS_TX_IO_M0_CFG_0

Address: 0x000F0DB0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.

Registers

OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQS_TX_IO_M0_CFG_1

Address: 0x000F0DB4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQS_TX_IO_M1_CFG_0

Address: 0x000F0DB8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQS_TX_IO_M1_CFG_1

Address: 0x000F0DBC

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ0__DQS_TX_IO_CMN_M0_R0_CFG

Address: 0x000F0DC0

Registers

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_DQ0__DQS_TX_IO_CMN_M0_R1_CFG

Address: 0x000F0DC4

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_DQ0__DQS_TX_IO_CMN_M1_R0_CFG

Address: 0x000F0DC8

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_DQ0__DQS_TX_IO_CMN_M1_R1_CFG

Address: 0x000F0DCC

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_DQ1__TOP_CFG

Address: 0x00100000

Description:

Registers

Name	Index	Type	Reset	Description
FIFO_CLR	[8]	RW	0x0	FIFO clear.
RCS_SW_OVR	[2]	RW	0x0	Read Chip Select Override.
RCS_SW_OVR_VAL	[3]	RW	0x0	Read Chip Select Override value.
TRAINING_MODE	[9]	RW	0x0	Training Mode.
WCS_SW_OVR	[0]	RW	0x0	Write Chip Select Override.
WCS_SW_OVR_VAL	[1]	RW	0x0	Write Chip Select Override value.

WAV_CH0_DQ1__TOP_STA

Address: 0x00100004

Description:

Name	Index	Type	Reset	Description
RCS	[1]	R	0x0	Read Chip Select status.
WCS	[0]	R	0x0	Write Chip Select status.

WAV_CH0_DQ1__DQ_RX_BSCAN_STA

Address: 0x00100008

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	R	0x000	Boundary Scan per-bit value.

WAV_CH0_DQ1__DQ_RX_M0_CFG

Address: 0x0010000C

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH0_DQ1__DQ_RX_M1_CFG

Address: 0x00100010

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_0

Address: 0x00100014

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_1

Address: 0x00100018

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_2

Address: 0x0010001C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_3

Address: 0x00100020

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_4

Address: 0x00100024

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_5

Address: 0x00100028

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_6

Address: 0x0010002C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_7

Address: 0x00100030

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH0_DQ1__DQ_RX_IO_M0_R0_CFG_8

Address: 0x00100034

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_0

Address: 0x00100038

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_1

Address: 0x0010003C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_2

Address: 0x00100040

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_3

Address: 0x00100044

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_4

Address: 0x00100048

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_5

Address: 0x0010004C

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_6

Address: 0x00100050

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_7

Address: 0x00100054

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M0_R1_CFG_8

Address: 0x00100058

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_0

Address: 0x0010005C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_1

Address: 0x00100060

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_2

Address: 0x00100064

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_3

Address: 0x00100068

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_4

Address: 0x0010006C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_5

Address: 0x00100070

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_6

Address: 0x00100074

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_7

Address: 0x00100078

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R0_CFG_8

Address: 0x0010007C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_0

Address: 0x00100080

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_1

Address: 0x00100084

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_2

Address: 0x00100088

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_3

Address: 0x0010008C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_4

Address: 0x00100090

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_5

Address: 0x00100094

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_6

Address: 0x00100098

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_7

Address: 0x0010009C

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_M1_R1_CFG_8

Address: 0x001000A0

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_DQ1__DQ_RX_IO_STA

Address: 0x001000A4

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_0

Address: 0x001000A8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_1

Address: 0x001000AC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_2

Address: 0x001000B0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_3

Address: 0x001000B4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_4

Address: 0x001000B8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_5

Address: 0x001000BC

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_6

Address: 0x001000C0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_7

Address: 0x001000C4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R0_CFG_8

Address: 0x001000C8

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_0

Address: 0x001000CC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_1

Address: 0x001000D0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_2

Address: 0x001000D4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_3

Address: 0x001000D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_4

Address: 0x001000DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_5

Address: 0x001000E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_6

Address: 0x001000E4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_7

Address: 0x001000E8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M0_R1_CFG_8

Address: 0x001000EC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_0

Address: 0x001000F0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_1

Address: 0x001000F4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_2

Address: 0x001000F8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_3

Address: 0x001000FC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_4

Address: 0x00100100

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_5

Address: 0x00100104

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_6

Address: 0x00100108

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_7

Address: 0x0010010C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R0_CFG_8

Address: 0x00100110

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_0

Address: 0x00100114

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_1

Address: 0x00100118

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_2

Address: 0x0010011C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_3

Address: 0x00100120

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_4

Address: 0x00100124

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_5

Address: 0x00100128

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_6

Address: 0x0010012C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_7

Address: 0x00100130

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_M1_R1_CFG_8

Address: 0x00100134

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_0

Address: 0x00100138

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_1

Address: 0x0010013C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_2

Address: 0x00100140

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_3

Address: 0x00100144

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_4

Address: 0x00100148

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_5

Address: 0x0010014C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_6

Address: 0x00100150

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_7

Address: 0x00100154

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_8

Address: 0x00100158

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_0

Address: 0x0010015C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_1

Address: 0x00100160

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_2

Address: 0x00100164

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_3

Address: 0x00100168

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_4

Address: 0x0010016C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_5

Address: 0x00100170

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_6

Address: 0x00100174

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_7

Address: 0x00100178

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DLY_M0_R1_CFG_8

Address: 0x0010017C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_0

Address: 0x00100180

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_1

Address: 0x00100184

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_2

Address: 0x00100188

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_3

Address: 0x0010018C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_4

Address: 0x00100190

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_5

Address: 0x00100194

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_6

Address: 0x00100198

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_7

Address: 0x0010019C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_8

Address: 0x001001A0

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_0

Address: 0x001001A4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_1

Address: 0x001001A8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_2

Address: 0x001001AC

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_3

Address: 0x001001B0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_4

Address: 0x001001B4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_5

Address: 0x001001B8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_6

Address: 0x001001BC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_7

Address: 0x001001C0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_8

Address: 0x001001C4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_RX_SA_STA_0

Address: 0x001001C8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_RX_SA_STA_1

Address: 0x001001CC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_RX_SA_STA_2

Address: 0x001001D0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_RX_SA_STA_3

Address: 0x001001D4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

Registers

WAV_CH0_DQ1__DQ_RX_SA_STA_4

Address: 0x001001D8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_RX_SA_STA_5

Address: 0x001001DC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_RX_SA_STA_6

Address: 0x001001E0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_RX_SA_STA_7

Address: 0x001001E4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_RX_SA_STA_8

Address: 0x001001E8

Description:

Name	Index	Type	Reset	Description

Registers

SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_DQ1__DQ_TX_BSCAN_CFG

Address: 0x001001EC

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	RW	0x00	Boundary Scan per-bit value.

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_0

Address: 0x001001F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_1

Address: 0x001001F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_2

Address: 0x001001F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_3

Address: 0x001001FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_4

Address: 0x00100200

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_5

Address: 0x00100204

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00100208

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_7

Address: 0x0010020C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_8

Address: 0x00100210

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_0

Address: 0x00100214

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_1

Address: 0x00100218

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_2

Address: 0x0010021C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_3

Address: 0x00100220

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_4

Address: 0x00100224

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_5

Address: 0x00100228

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_6

Address: 0x0010022C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_7

Address: 0x00100230

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_8

Address: 0x00100234

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_0

Address: 0x00100238

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_1

Address: 0x0010023C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_2

Address: 0x00100240

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_3

Address: 0x00100244

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_4

Address: 0x00100248

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_5

Address: 0x0010024C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_6

Address: 0x00100250

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_7

Address: 0x00100254

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_8

Address: 0x00100258

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_0

Address: 0x0010025C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_1

Address: 0x00100260

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_2

Address: 0x00100264

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_3

Address: 0x00100268

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_4

Address: 0x0010026C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_5

Address: 0x00100270

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_6

Address: 0x00100274

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_7

Address: 0x00100278

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_8

Address: 0x0010027C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQ_TX_ODR_PI_M0_R0_CFG

Address: 0x00100280

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_ODR_PI_M0_R1_CFG

Address: 0x00100284

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_ODR_PI_M1_R0_CFG

Address: 0x00100288

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_ODR_PI_M1_R1_CFG

Address: 0x0010028C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00100290

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00100294

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00100298

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_QDR_PI_0_M1_R1_CFG

Address: 0x0010029C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ1__DQ_TX_QDR_PI_1_M0_R0_CFG

Address: 0x001002A0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_QDR_PI_1_M0_R1_CFG

Address: 0x001002A4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_QDR_PI_1_M1_R0_CFG

Address: 0x001002A8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_QDR_PI_1_M1_R1_CFG

Address: 0x001002AC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_DDR_PI_0_M0_R0_CFG

Address: 0x001002B0

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_DDR_PI_0_M0_R1_CFG

Address: 0x001002B4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_DDR_PI_0_M1_R0_CFG

Address: 0x001002B8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_DDR_PI_0_M1_R1_CFG

Address: 0x001002BC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_DDR_PI_1_M0_R0_CFG

Address: 0x001002C0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_PI_1_M0_R1_CFG

Address: 0x001002C4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_DDR_PI_1_M1_R0_CFG

Address: 0x001002C8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_DDR_PI_1_M1_R1_CFG

Address: 0x001002CC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_PI_RT_M0_R0_CFG

Address: 0x001002D0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_PI_RT_M0_R1_CFG

Address: 0x001002D4

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_PI_RT_M1_R0_CFG

Address: 0x001002D8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_PI_RT_M1_R1_CFG

Address: 0x001002DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQ_TX_RT_M0_R0_CFG

Address: 0x001002E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ1__DQ_TX_RT_M0_R1_CFG

Address: 0x001002E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ1__DQ_TX_RT_M1_R0_CFG

Address: 0x001002E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_RT_M1_R1_CFG

Address: 0x001002EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_0

Address: 0x001002F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_1

Address: 0x001002F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_2

Address: 0x001002F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.

Registers

PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_3

Address: 0x001002FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_4

Address: 0x00100300

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_5

Address: 0x00100304

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.

Registers

PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.
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WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_6

Address: 0x00100308

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_7

Address: 0x0010030C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R0_CFG_8

Address: 0x00100310

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_0

Address: 0x00100314

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_1

Address: 0x00100318

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_2

Address: 0x0010031C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_3

Address: 0x00100320

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_4

Address: 0x00100324

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_5

Address: 0x00100328

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_6

Address: 0x0010032C

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_7

Address: 0x00100330

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M0_R1_CFG_8

Address: 0x00100334

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_0

Address: 0x00100338

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_1

Address: 0x0010033C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_2

Address: 0x00100340

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_3

Address: 0x00100344

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_4

Address: 0x00100348

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_5

Address: 0x0010034C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_6

Address: 0x00100350

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_7

Address: 0x00100354

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R0_CFG_8

Address: 0x00100358

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_0

Address: 0x0010035C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_1

Address: 0x00100360

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_2

Address: 0x00100364

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_3

Address: 0x00100368

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_4

Address: 0x0010036C

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_5

Address: 0x00100370

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_6

Address: 0x00100374

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_7

Address: 0x00100378

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_M1_R1_CFG_8

Address: 0x0010037C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00100380

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x00100384

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00100388

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x0010038C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00100390

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x00100394

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00100398

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x0010039C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x001003A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x001003A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x001003A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x001003AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x001003B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x001003B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x001003B8

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x001003BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x001003C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x001003C4

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x001003C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x001003CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x001003D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x001003D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x001003D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x001003DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x001003E0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x001003E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x001003E8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x001003EC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x001003F0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x001003F4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x001003F8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x001003FC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x00100400

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x00100404

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x00100408

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x0010040C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00100410

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_1

Address: 0x00100414

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_2

Address: 0x00100418

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x0010041C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_4

Address: 0x00100420

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x00100424

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x00100428

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x0010042C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_8

Address: 0x00100430

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_0

Address: 0x00100434

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_1

Address: 0x00100438

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x0010043C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00100440

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_4

Address: 0x00100444

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_5

Address: 0x00100448

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_6

Address: 0x0010044C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_7

Address: 0x00100450

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00100454

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00100458

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x0010045C

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x00100460

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x00100464

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x00100468

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_5

Address: 0x0010046C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x00100470

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x00100474

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_8

Address: 0x00100478

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x0010047C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_1

Address: 0x00100480

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_2

Address: 0x00100484

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x00100488

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x0010048C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_5

Address: 0x00100490

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_6

Address: 0x00100494

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_7

Address: 0x00100498

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_8

Address: 0x0010049C

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_0

Address: 0x001004A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_1

Address: 0x001004A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_2

Address: 0x001004A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_3

Address: 0x001004AC

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_4

Address: 0x001004B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_5

Address: 0x001004B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_6

Address: 0x001004B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_7

Address: 0x001004BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_M0_R0_CFG_8

Address: 0x001004C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_0

Address: 0x001004C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_1

Address: 0x001004C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_2

Address: 0x001004CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_3

Address: 0x001004D0

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_4

Address: 0x001004D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_5

Address: 0x001004D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_6

Address: 0x001004DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_7

Address: 0x001004E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_M0_R1_CFG_8

Address: 0x001004E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_0

Address: 0x001004E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_1

Address: 0x001004EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_2

Address: 0x001004F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_3

Address: 0x001004F4

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_4

Address: 0x001004F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_5

Address: 0x001004FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_6

Address: 0x00100500

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_7

Address: 0x00100504

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_M1_R0_CFG_8

Address: 0x00100508

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_0

Address: 0x0010050C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_1

Address: 0x00100510

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_2

Address: 0x00100514

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_3

Address: 0x00100518

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_4

Address: 0x0010051C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_5

Address: 0x00100520

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_6

Address: 0x00100524

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_7

Address: 0x00100528

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_M1_R1_CFG_8

Address: 0x0010052C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00100530

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x00100534

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00100538

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x0010053C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00100540

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x00100544

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00100548

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x0010054C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00100550

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00100554

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00100558

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x0010055C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00100560

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00100564

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00100568

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x0010056C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00100570

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00100574

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00100578

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x0010057C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00100580

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x00100584

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x00100588

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x0010058C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x00100590

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x00100594

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x00100598

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x0010059C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x001005A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x001005A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x001005A8

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x001005AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x001005B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x001005B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x001005B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x001005BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_0

Address: 0x001005C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_1

Address: 0x001005C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_2

Address: 0x001005C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_3

Address: 0x001005CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_4

Address: 0x001005D0

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_5

Address: 0x001005D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_6

Address: 0x001005D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_7

Address: 0x001005DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R0_CFG_8

Address: 0x001005E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_0

Address: 0x001005E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_1

Registers

Address: 0x001005E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_2

Address: 0x001005EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_3

Address: 0x001005F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_4

Address: 0x001005F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_5

Address: 0x001005F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_6

Address: 0x001005FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_7

Address: 0x00100600

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M0_R1_CFG_8

Address: 0x00100604

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_0

Address: 0x00100608

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_1

Address: 0x0010060C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_2

Address: 0x00100610

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_3

Address: 0x00100614

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_4

Address: 0x00100618

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_5

Address: 0x0010061C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_6

Address: 0x00100620

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_7

Address: 0x00100624

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R0_CFG_8

Address: 0x00100628

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_0

Address: 0x0010062C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_1

Address: 0x00100630

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_2

Address: 0x00100634

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_3

Address: 0x00100638

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_4

Address: 0x0010063C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_5

Address: 0x00100640

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_6

Registers

Address: 0x00100644

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_7

Address: 0x00100648

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_M1_R1_CFG_8

Address: 0x0010064C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00100650

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x00100654

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x00100658

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x0010065C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x00100660

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x00100664

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x00100668

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x0010066C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x00100670

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00100674

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x00100678

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x0010067C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x00100680

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x00100684

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x00100688

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x0010068C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x00100690

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x00100694

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00100698

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x0010069C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_2

Registers

Address: 0x001006A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x001006A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x001006A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x001006AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x001006B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x001006B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x001006B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x001006BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x001006C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x001006C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x001006C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x001006CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x001006D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x001006D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x001006D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x001006DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_0

Address: 0x001006E0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_1

Address: 0x001006E4

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_2

Address: 0x001006E8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_3

Address: 0x001006EC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_4

Address: 0x001006F0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_5

Address: 0x001006F4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_6

Address: 0x001006F8

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_7

Address: 0x001006FC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R0_CFG_8

Address: 0x00100700

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_0

Address: 0x00100704

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_1

Address: 0x00100708

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_2

Address: 0x0010070C

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_3

Address: 0x00100710

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_4

Address: 0x00100714

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_5

Address: 0x00100718

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_6

Address: 0x0010071C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_7

Address: 0x00100720

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M0_R1_CFG_8

Address: 0x00100724

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_0

Address: 0x00100728

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_1

Address: 0x0010072C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_2

Address: 0x00100730

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_3

Address: 0x00100734

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_4

Address: 0x00100738

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_5

Address: 0x0010073C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_6

Address: 0x00100740

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_7

Address: 0x00100744

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R0_CFG_8

Address: 0x00100748

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_0

Address: 0x0010074C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_1

Address: 0x00100750

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_2

Address: 0x00100754

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_3

Address: 0x00100758

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_4

Address: 0x0010075C

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_5

Address: 0x00100760

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_6

Address: 0x00100764

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_7

Address: 0x00100768

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_LPDE_M1_R1_CFG_8

Address: 0x0010076C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_0

Address: 0x00100770

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_1

Address: 0x00100774

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_2

Address: 0x00100778

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_3

Address: 0x0010077C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_4

Address: 0x00100780

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_5

Address: 0x00100784

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_6

Address: 0x00100788

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_7

Address: 0x0010078C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.

Registers

SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M0_CFG_8

Address: 0x00100790

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_0

Address: 0x00100794

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_1

Address: 0x00100798

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_2

Address: 0x0010079C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.

Registers

OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_3

Address: 0x001007A0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_4

Address: 0x001007A4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_5

Address: 0x001007A8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_6

Address: 0x001007AC

Registers

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_7

Address: 0x001007B0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQ_TX_IO_M1_CFG_8

Address: 0x001007B4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQS_RX_M0_CFG

Address: 0x001007B8

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH0_DQ1__DQS_RX_M1_CFG

Registers

Address: 0x001007BC

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH0_DQ1__DQS_RX_BSCAN_STA

Address: 0x001007C0

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	R	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M0_R0_CFG

Address: 0x001007C4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M0_R1_CFG

Address: 0x001007C8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M1_R0_CFG

Address: 0x001007CC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_RX_SDR_LPDE_M1_R1_CFG

Address: 0x001007D0

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_RX_RN_PI_M0_R0_CFG

Address: 0x001007D4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RN_PI_M0_R1_CFG

Address: 0x001007D8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RN_PI_M1_R0_CFG

Address: 0x001007DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RN_PI_M1_R1_CFG

Address: 0x001007E0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ1__DQS_RX_RCS_PI_M0_R0_CFG

Address: 0x001007E4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RCS_PI_M0_R1_CFG

Address: 0x001007E8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RCS_PI_M1_R0_CFG

Address: 0x001007EC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RCS_PI_M1_R1_CFG

Address: 0x001007F0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M0_R0_CFG

Address: 0x001007F4

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M0_R1_CFG

Address: 0x001007F8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M1_R0_CFG

Address: 0x001007FC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RDQS_PI_0_M1_R1_CFG

Address: 0x00100800

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M0_R0_CFG

Address: 0x00100804

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M0_R1_CFG

Address: 0x00100808

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M1_R0_CFG

Address: 0x0010080C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_RDQS_PI_1_M1_R1_CFG

Address: 0x00100810

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_RX_PI_STA

Address: 0x00100814

Description:

Name	Index	Type	Reset	Description
RCS_PI_PHASE	[1]	R	0x0	Indicates the phase of RE_PI output clock wrt RCS.
REN_PI_PHASE	[0]	R	0x0	Indicates the phase of RE_PI output clock wrt REN.

WAV_CH0_DQ1__DQS_RX_IO_M0_R0_CFG_0

Address: 0x00100818

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

Registers

WAV_CH0_DQ1__DQS_RX_IO_M0_R0_CFG_1

Address: 0x0010081C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ1__DQS_RX_IO_M0_R1_CFG_0

Address: 0x00100820

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ1__DQS_RX_IO_M0_R1_CFG_1

Address: 0x00100824

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ1__DQS_RX_IO_M1_R0_CFG_0

Address: 0x00100828

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ1__DQS_RX_IO_M1_R0_CFG_1

Address: 0x0010082C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ1__DQS_RX_IO_M1_R1_CFG_0

Address: 0x00100830

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.

Registers

DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.
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WAV_CH0_DQ1__DQS_RX_IO_M1_R1_CFG_1

Address: 0x00100834

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_DQ1__DQS_RX_IO_CMN_M0_R0_CFG

Address: 0x00100838

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for edge detect EN and IE.

WAV_CH0_DQ1__DQS_RX_IO_CMN_M0_R1_CFG

Address: 0x0010083C

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_DQ1__DQS_RX_IO_CMN_M1_R0_CFG

Address: 0x00100840

Registers

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_DQ1__DQS_RX_IO_CMN_M1_R1_CFG

Address: 0x00100844

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_DQ1__DQS_RX_IO_STA

Address: 0x00100848

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH0_DQ1__DQS_RX_SA_M0_R0_CFG_0

Address: 0x0010084C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.

Registers

CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQS_RX_SA_M0_R0_CFG_1

Address: 0x00100850

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQS_RX_SA_M0_R1_CFG_0

Address: 0x00100854

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQS_RX_SA_M0_R1_CFG_1

Address: 0x00100858

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.

Registers

CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQS_RX_SA_M1_R0_CFG_0

Address: 0x0010085C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQS_RX_SA_M1_R0_CFG_1

Address: 0x00100860

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQS_RX_SA_M1_R1_CFG_0

Address: 0x00100864

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.

Registers

CAL_DIR_90	[17]	RW	0x0	Calibration direction.
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WAV_CH0_DQ1__DQS_RX_SA_M1_R1_CFG_1

Address: 0x00100868

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_DQ1__DQS_RX_SA_CMN_CFG

Address: 0x0010086C

Description:

Name	Index	Type	Reset	Description
CAL_EN_0_180	[1]	RW	0x0	Calibration enable.
CAL_EN_90_270	[3]	RW	0x0	Calibration enable.
OVR_EN_0_180	[0]	RW	0x1	Software override value of SA_Enable.
OVR_EN_90_270	[2]	RW	0x1	Software override value of SA_Enable.
SW_OVR	[4]	RW	0x0	Software override for SA enable.

WAV_CH0_DQ1__DQS_TX_M0_CFG

Address: 0x00100870

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH0_DQ1__DQS_TX_M1_CFG

Address: 0x00100874

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

Registers

WAV_CH0_DQ1__DQS_TX_BSCAN_CTRL_CFG

Address: 0x00100878

Description:

Name	Index	Type	Reset	Description
IE	[0]	RW	0x0	Boundary Scan IE.
OE	[1]	RW	0x0	Boundary Scan OE.

WAV_CH0_DQ1__DQS_TX_BSCAN_CFG

Address: 0x0010087C

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	RW	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_0

Address: 0x00100880

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_1

Address: 0x00100884

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_2

Address: 0x00100888

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_3

Address: 0x0010088C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_4

Registers

Address: 0x00100890

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_5

Address: 0x00100894

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00100898

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_7

Address: 0x0010089C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_8

Address: 0x001008A0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_0

Address: 0x001008A4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_1

Address: 0x001008A8

Registers

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_2

Address: 0x001008AC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_3

Address: 0x001008B0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_4

Address: 0x001008B4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_5

Address: 0x001008B8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_6

Address: 0x001008BC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_7

Address: 0x001008C0

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_8

Address: 0x001008C4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_0

Address: 0x001008C8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_1

Address: 0x001008CC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_2

Address: 0x001008D0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_3

Address: 0x001008D4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_4

Address: 0x001008D8

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_5

Address: 0x001008DC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_6

Address: 0x001008E0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_7

Address: 0x001008E4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_8

Address: 0x001008E8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_0

Address: 0x001008EC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_1

Address: 0x001008F0

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_2

Address: 0x001008F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_3

Address: 0x001008F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_4

Address: 0x001008FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_5

Address: 0x00100900

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_6

Address: 0x00100904

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_7

Address: 0x00100908

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_8

Address: 0x0010090C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_DQ1__DQS_TX_ODR_PI_M0_R0_CFG

Address: 0x00100910

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_ODR_PI_M0_R1_CFG

Address: 0x00100914

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_ODR_PI_M1_R0_CFG

Address: 0x00100918

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_ODR_PI_M1_R1_CFG

Address: 0x0010091C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00100920

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00100924

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00100928

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_QDR_PI_0_M1_R1_CFG

Address: 0x0010092C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ1__DQS_TX_QDR_PI_1_M0_R0_CFG

Address: 0x00100930

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_QDR_PI_1_M0_R1_CFG

Address: 0x00100934

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_QDR_PI_1_M1_R0_CFG

Address: 0x00100938

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_QDR_PI_1_M1_R1_CFG

Address: 0x0010093C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DDR_PI_0_M0_R0_CFG

Address: 0x00100940

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DDR_PI_0_M0_R1_CFG

Address: 0x00100944

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DDR_PI_0_M1_R0_CFG

Address: 0x00100948

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DDR_PI_0_M1_R1_CFG

Address: 0x0010094C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DDR_PI_1_M0_R0_CFG

Address: 0x00100950

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ1__DQS_TX_DDR_PI_1_M0_R1_CFG

Address: 0x00100954

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DDR_PI_1_M1_R0_CFG

Address: 0x00100958

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DDR_PI_1_M1_R1_CFG

Address: 0x0010095C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_PI_RT_M0_R0_CFG

Address: 0x00100960

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_PI_RT_M0_R1_CFG

Address: 0x00100964

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_PI_RT_M1_R0_CFG

Address: 0x00100968

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_PI_RT_M1_R1_CFG

Address: 0x0010096C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_SDR_PI_M0_R0_CFG

Address: 0x00100970

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_SDR_PI_M0_R1_CFG

Address: 0x00100974

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_DQ1__DQS_TX_SDR_PI_M1_R0_CFG

Address: 0x00100978

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_SDR_PI_M1_R1_CFG

Address: 0x0010097C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DFI_PI_M0_R0_CFG

Address: 0x00100980

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DFI_PI_M0_R1_CFG

Address: 0x00100984

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DFI_PI_M1_R0_CFG

Address: 0x00100988

Description:

Name	Index	Type	Reset	Description

Registers

EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other PIs.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_DFI_PI_M1_R1_CFG

Address: 0x0010098C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other PIs.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_DQ1__DQS_TX_RT_M0_R0_CFG

Address: 0x00100990

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ1__DQS_TX_RT_M0_R1_CFG

Address: 0x00100994

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ1__DQS_TX_RT_M1_R0_CFG

Address: 0x00100998

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ1__DQS_TX_RT_M1_R1_CFG

Address: 0x0010099C

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_0

Address: 0x001009A0

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_1

Address: 0x001009A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_2

Address: 0x001009A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_3

Address: 0x001009AC

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_4

Address: 0x001009B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_5

Address: 0x001009B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_6

Address: 0x001009B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_7

Address: 0x001009BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R0_CFG_8

Address: 0x001009C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_0

Address: 0x001009C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_1

Address: 0x001009C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_2

Address: 0x001009CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_3

Address: 0x001009D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_4

Address: 0x001009D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_5

Address: 0x001009D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_6

Address: 0x001009DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_7

Address: 0x001009E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M0_R1_CFG_8

Address: 0x001009E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_0

Address: 0x001009E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_1

Address: 0x001009EC

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_2

Address: 0x001009F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_3

Address: 0x001009F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_4

Address: 0x001009F8

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_5

Address: 0x001009FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_6

Address: 0x00100A00

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_7

Address: 0x00100A04

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R0_CFG_8

Address: 0x00100A08

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_0

Address: 0x00100A0C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_1

Address: 0x00100A10

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_2

Address: 0x00100A14

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_3

Address: 0x00100A18

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_4

Address: 0x00100A1C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_5

Address: 0x00100A20

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_6

Address: 0x00100A24

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_7

Address: 0x00100A28

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_DQ1__DQS_TX_SDR_M1_R1_CFG_8

Address: 0x00100A2C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00100A30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x00100A34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00100A38

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x00100A3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00100A40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x00100A44

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00100A48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x00100A4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x00100A50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x00100A54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x00100A58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x00100A5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x00100A60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x00100A64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x00100A68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x00100A6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x00100A70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x00100A74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x00100A78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x00100A7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x00100A80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x00100A84

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x00100A88

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x00100A8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x00100A90

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x00100A94

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x00100A98

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x00100A9C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x00100AA0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x00100AA4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x00100AA8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x00100AAC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x00100AB0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x00100AB4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x00100AB8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x00100ABC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00100AC0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_1

Address: 0x00100AC4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_2

Address: 0x00100AC8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_3

Address: 0x00100ACC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_4

Address: 0x00100AD0

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x00100AD4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x00100AD8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x00100ADC

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_8

Address: 0x00100AE0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_0

Address: 0x00100AE4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_1

Address: 0x00100AE8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x00100AEC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00100AF0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x00100AF4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x00100AF8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x00100AFC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x00100B00

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00100B04

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00100B08

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x00100B0C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_2

Address: 0x00100B10

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_3

Address: 0x00100B14

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_4

Address: 0x00100B18

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_5

Address: 0x00100B1C

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x00100B20

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x00100B24

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_8

Address: 0x00100B28

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x00100B2C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_1

Address: 0x00100B30

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_2

Address: 0x00100B34

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x00100B38

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x00100B3C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x00100B40

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x00100B44

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x00100B48

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x00100B4C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_0

Address: 0x00100B50

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_1

Address: 0x00100B54

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_2

Address: 0x00100B58

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_3

Address: 0x00100B5C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_4

Address: 0x00100B60

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_5

Address: 0x00100B64

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_6

Address: 0x00100B68

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_7

Address: 0x00100B6C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R0_CFG_8

Address: 0x00100B70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
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WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_0

Address: 0x00100B74

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_1

Address: 0x00100B78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_2

Address: 0x00100B7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_3

Address: 0x00100B80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_4

Address: 0x00100B84

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_5

Address: 0x00100B88

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_6

Address: 0x00100B8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_7

Address: 0x00100B90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M0_R1_CFG_8

Address: 0x00100B94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_0

Address: 0x00100B98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_1

Address: 0x00100B9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_2

Address: 0x00100BA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_3

Address: 0x00100BA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_4

Address: 0x00100BA8

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_5

Address: 0x00100BAC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_6

Address: 0x00100BB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_7

Address: 0x00100BB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R0_CFG_8

Address: 0x00100BB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_0

Address: 0x00100BBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_1

Address: 0x00100BC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_2

Address: 0x00100BC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_3

Address: 0x00100BC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_4

Address: 0x00100BCC

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_5

Address: 0x00100BD0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_6

Address: 0x00100BD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_7

Address: 0x00100BD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_DDR_M1_R1_CFG_8

Address: 0x00100BDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00100BE0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x00100BE4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00100BE8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x00100BEC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00100BFO

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x00100BF4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00100BF8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x00100BFC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00100C00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00100C04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00100C08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x00100C0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00100C10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00100C14

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00100C18

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x00100C1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00100C20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00100C24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00100C28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x00100C2C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00100C30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x00100C34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x00100C38

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x00100C3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x00100C40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x00100C44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x00100C48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x00100C4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x00100C50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x00100C54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x00100C58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x00100C5C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x00100C60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x00100C64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x00100C68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x00100C6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_0

Address: 0x00100C70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_1

Address: 0x00100C74

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_2

Address: 0x00100C78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_3

Address: 0x00100C7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_4

Address: 0x00100C80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_5

Address: 0x00100C84

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_6

Address: 0x00100C88

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_7

Address: 0x00100C8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R0_CFG_8

Address: 0x00100C90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_0

Address: 0x00100C94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_1

Address: 0x00100C98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_2

Address: 0x00100C9C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_3

Address: 0x00100CA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_4

Address: 0x00100CA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_5

Address: 0x00100CA8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_6

Address: 0x00100CAC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_7

Address: 0x00100CB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M0_R1_CFG_8

Registers

Address: 0x00100CB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_0

Address: 0x00100CB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_1

Address: 0x00100CBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_2

Address: 0x00100CC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_3

Address: 0x00100CC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_4

Address: 0x00100CC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_5

Address: 0x00100CCC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_6

Address: 0x00100CD0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_7

Address: 0x00100CD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R0_CFG_8

Address: 0x00100CD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_0

Address: 0x00100CDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_1

Address: 0x00100CEO

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_2

Address: 0x00100CE4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_3

Address: 0x00100CE8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_4

Address: 0x00100CEC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_5

Address: 0x00100CF0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_6

Address: 0x00100CF4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_7

Address: 0x00100CF8

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_M1_R1_CFG_8

Address: 0x00100CFC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00100D00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x00100D04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x00100D08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x00100D0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_4

Registers

Address: 0x00100D10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x00100D14

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x00100D18

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x00100D1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x00100D20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00100D24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x00100D28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x00100D2C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x00100D30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x00100D34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x00100D38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x00100D3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x00100D40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x00100D44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00100D48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x00100D4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x00100D50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x00100D54

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x00100D58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x00100D5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x00100D60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x00100D64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x00100D68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_0

Registers

Address: 0x00100D6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x00100D70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x00100D74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x00100D78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x00100D7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x00100D80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x00100D84

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x00100D88

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x00100D8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_DQ1__DQS_TX_LPDE_M0_R0_CFG_0

Address: 0x00100D90

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_LPDE_M0_R0_CFG_1

Address: 0x00100D94

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_LPDE_M0_R1_CFG_0

Address: 0x00100D98

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_LPDE_M0_R1_CFG_1

Address: 0x00100D9C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_LPDE_M1_R0_CFG_0

Address: 0x00100DA0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_LPDE_M1_R0_CFG_1

Address: 0x00100DA4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_LPDE_M1_R1_CFG_0

Address: 0x00100DA8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_LPDE_M1_R1_CFG_1

Address: 0x00100DAC

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_DQ1__DQS_TX_IO_M0_CFG_0

Address: 0x00100DB0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQS_TX_IO_M0_CFG_1

Address: 0x00100DB4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQS_TX_IO_M1_CFG_0

Address: 0x00100DB8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQS_TX_IO_M1_CFG_1

Address: 0x00100DBC

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_DQ1__DQS_TX_IO_CMN_M0_R0_CFG

Address: 0x00100DC0

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_DQ1__DQS_TX_IO_CMN_M0_R1_CFG

Address: 0x00100DC4

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_DQ1__DQS_TX_IO_CMN_M1_R0_CFG

Address: 0x00100DC8

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_DQ1__DQS_TX_IO_CMN_M1_R1_CFG

Address: 0x00100DCC

Description:

Registers

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_CA__TOP_CFG

Address: 0x00110000

Description:

Name	Index	Type	Reset	Description
FIFO_CLR	[8]	RW	0x0	FIFO clear.
RCS_SW_OVR	[2]	RW	0x0	Read Chip Select Override.
RCS_SW_OVR_VAL	[3]	RW	0x0	Read Chip Select Override value.
TRAINING_MODE	[9]	RW	0x0	Training Mode.
WCS_SW_OVR	[0]	RW	0x0	Write Chip Select Override.
WCS_SW_OVR_VAL	[1]	RW	0x0	Write Chip Select Override value.

WAV_CH0_CA__TOP_STA

Address: 0x00110004

Description:

Name	Index	Type	Reset	Description
RCS	[1]	R	0x0	Read Chip Select status.
WCS	[0]	R	0x0	Write Chip Select status.

WAV_CH0_CA__DQ_RX_BSCAN_STA

Address: 0x00110008

Description:

Name	Index	Type	Reset	Description
VAL	[10:0]	R	0x000	Boundary Scan per-bit value.

WAV_CH0_CA__DQ_RX_M0_CFG

Address: 0x0011000C

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH0_CA__DQ_RX_M1_CFG

Address: 0x00110010

Description:

Registers

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_0

Address: 0x00110014

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_1

Address: 0x00110018

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_2

Address: 0x0011001C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_3

Address: 0x00110020

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_4

Address: 0x00110024

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_5

Address: 0x00110028

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_6

Address: 0x0011002C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_7

Address: 0x00110030

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_8

Address: 0x00110034

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_9

Address: 0x00110038

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R0_CFG_10

Address: 0x0011003C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_0

Address: 0x00110040

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_1

Address: 0x00110044

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_2

Address: 0x00110048

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_3

Address: 0x0011004C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_4

Address: 0x00110050

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_5

Address: 0x00110054

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_6

Address: 0x00110058

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_7

Address: 0x0011005C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_8

Address: 0x00110060

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_9

Address: 0x00110064

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M0_R1_CFG_10

Address: 0x00110068

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_0

Address: 0x0011006C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_1

Address: 0x00110070

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_2

Address: 0x00110074

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_3

Address: 0x00110078

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_4

Address: 0x0011007C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_5

Address: 0x00110080

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_6

Address: 0x00110084

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_7

Address: 0x00110088

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_8

Address: 0x0011008C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_9

Address: 0x00110090

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R0_CFG_10

Address: 0x00110094

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_0

Address: 0x00110098

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_1

Address: 0x0011009C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_2

Address: 0x001100A0

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_3

Address: 0x001100A4

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_4

Address: 0x001100A8

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_5

Address: 0x001100AC

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_6

Address: 0x001100B0

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_7

Address: 0x001100B4

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_8

Address: 0x001100B8

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_9

Address: 0x001100BC

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_M1_R1_CFG_10

Address: 0x001100C0

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH0_CA__DQ_RX_IO_STA

Address: 0x001100C4

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_0

Address: 0x001100C8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_1

Address: 0x001100CC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_2

Address: 0x001100D0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_3

Address: 0x001100D4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_4

Address: 0x001100D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_5

Address: 0x001100DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_6

Address: 0x001100E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_7

Address: 0x001100E4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_8

Address: 0x001100E8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_9

Address: 0x001100EC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH0_CA__DQ_RX_SA_M0_R0_CFG_10

Address: 0x001100F0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_0

Address: 0x001100F4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_1

Address: 0x001100F8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_2

Address: 0x001100FC

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_3

Address: 0x00110100

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_4

Address: 0x00110104

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_5

Address: 0x00110108

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_6

Address: 0x0011010C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_7

Address: 0x00110110

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_8

Address: 0x00110114

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_9

Address: 0x00110118

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M0_R1_CFG_10

Address: 0x0011011C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_0

Address: 0x00110120

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_1

Address: 0x00110124

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_2

Address: 0x00110128

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_3

Address: 0x0011012C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_4

Address: 0x00110130

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_5

Address: 0x00110134

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_6

Address: 0x00110138

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_7

Address: 0x0011013C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_8

Address: 0x00110140

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_9

Address: 0x00110144

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R0_CFG_10

Address: 0x00110148

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_0

Address: 0x0011014C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_1

Address: 0x00110150

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_2

Address: 0x00110154

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_3

Address: 0x00110158

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_4

Address: 0x0011015C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_5

Address: 0x00110160

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_6

Address: 0x00110164

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_7

Address: 0x00110168

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_8

Address: 0x0011016C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_9

Address: 0x00110170

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_M1_R1_CFG_10

Address: 0x00110174

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_0

Address: 0x00110178

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_1

Address: 0x0011017C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_2

Address: 0x00110180

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_3

Address: 0x00110184

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_4

Address: 0x00110188

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_5

Address: 0x0011018C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_6

Address: 0x00110190

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_7

Address: 0x00110194

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_8

Address: 0x00110198

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_9

Address: 0x0011019C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R0_CFG_10

Address: 0x001101A0

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_0

Address: 0x001101A4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_1

Address: 0x001101A8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_2

Address: 0x001101AC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_3

Address: 0x001101B0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_4

Address: 0x001101B4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_5

Address: 0x001101B8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_6

Address: 0x001101BC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_7

Address: 0x001101C0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_8

Address: 0x001101C4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_9

Address: 0x001101C8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M0_R1_CFG_10

Address: 0x001101CC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_0

Address: 0x001101D0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_1

Address: 0x001101D4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_2

Address: 0x001101D8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_3

Address: 0x001101DC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_4

Address: 0x001101E0

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_5

Address: 0x001101E4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_6

Address: 0x001101E8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_7

Address: 0x001101EC

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_8

Address: 0x001101F0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_9

Address: 0x001101F4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R0_CFG_10

Address: 0x001101F8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_0

Address: 0x001101FC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_1

Address: 0x00110200

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_2

Address: 0x00110204

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_3

Address: 0x00110208

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_4

Address: 0x0011020C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_5

Address: 0x00110210

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_6

Address: 0x00110214

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_7

Address: 0x00110218

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_8

Address: 0x0011021C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_9

Address: 0x00110220

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_DLY_M1_R1_CFG_10

Address: 0x00110224

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_RX_SA_STA_0

Address: 0x00110228

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_1

Address: 0x0011022C

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.

Registers

SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_2

Address: 0x00110230

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_3

Address: 0x00110234

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_4

Address: 0x00110238

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_5

Address: 0x0011023C

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_6

Address: 0x00110240

Registers

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_7

Address: 0x00110244

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_8

Address: 0x00110248

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_9

Address: 0x0011024C

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH0_CA__DQ_RX_SA_STA_10

Address: 0x00110250

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.

Registers

SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.
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WAV_CH0_CA__DQ_TX_BSCAN_CFG

Address: 0x00110254

Description:

Name	Index	Type	Reset	Description
VAL	[10:0]	RW	0x00	Boundary Scan per-bit value.

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_0

Address: 0x00110258

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_1

Address: 0x0011025C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_2

Address: 0x00110260

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_3

Address: 0x00110264

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_4

Address: 0x00110268

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_5

Address: 0x0011026C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00110270

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_7

Address: 0x00110274

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_8

Address: 0x00110278

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_9

Address: 0x0011027C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M0_CFG_10

Address: 0x00110280

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_0

Address: 0x00110284

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_1

Address: 0x00110288

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_2

Address: 0x0011028C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_3

Address: 0x00110290

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_4

Address: 0x00110294

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_5

Address: 0x00110298

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_6

Address: 0x0011029C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_7

Address: 0x001102A0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_8

Address: 0x001102A4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_9

Address: 0x001102A8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_ANA_M1_CFG_10

Address: 0x001102AC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_0

Address: 0x001102B0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_1

Address: 0x001102B4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_2

Address: 0x001102B8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_3

Address: 0x001102BC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_4

Address: 0x001102C0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_5

Address: 0x001102C4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_6

Address: 0x001102C8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_7

Address: 0x001102CC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_8

Address: 0x001102D0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_9

Address: 0x001102D4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M0_CFG_10

Address: 0x001102D8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_0

Address: 0x001102DC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_1

Address: 0x001102E0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_2

Address: 0x001102E4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_3

Address: 0x001102E8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_4

Address: 0x001102EC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_5

Address: 0x001102F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_6

Address: 0x001102F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_7

Address: 0x001102F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_8

Address: 0x001102FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_9

Address: 0x00110300

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_EGRESS_DIG_M1_CFG_10

Address: 0x00110304

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQ_TX_ODR_PI_M0_R0_CFG

Address: 0x00110308

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_ODR_PI_M0_R1_CFG

Address: 0x0011030C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_ODR_PI_M1_R0_CFG

Address: 0x00110310

Registers

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_ODR_PI_M1_R1_CFG

Address: 0x00110314

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00110318

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_QDR_PI_0_M0_R1_CFG

Address: 0x0011031C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00110320

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH0_CA__DQ_TX_QDR_PI_0_M1_R1_CFG

Address: 0x00110324

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_QDR_PI_1_M0_R0_CFG

Address: 0x00110328

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_QDR_PI_1_M0_R1_CFG

Address: 0x0011032C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_QDR_PI_1_M1_R0_CFG

Address: 0x00110330

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_QDR_PI_1_M1_R1_CFG

Address: 0x00110334

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_DDR_PI_0_M0_R0_CFG

Address: 0x00110338

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_DDR_PI_0_M0_R1_CFG

Address: 0x0011033C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_DDR_PI_0_M1_R0_CFG

Address: 0x00110340

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_DDR_PI_0_M1_R1_CFG

Address: 0x00110344

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_CA__DQ_TX_DDR_PI_1_M0_R0_CFG

Address: 0x00110348

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_DDR_PI_1_M0_R1_CFG

Address: 0x0011034C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_DDR_PI_1_M1_R0_CFG

Address: 0x00110350

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_DDR_PI_1_M1_R1_CFG

Address: 0x00110354

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_PI_RT_M0_R0_CFG

Address: 0x00110358

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_PI_RT_M0_R1_CFG

Address: 0x0011035C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_PI_RT_M1_R0_CFG

Address: 0x00110360

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_PI_RT_M1_R1_CFG

Address: 0x00110364

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQ_TX_RT_M0_R0_CFG

Address: 0x00110368

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH0_CA__DQ_TX_RT_M0_R1_CFG

Address: 0x0011036C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH0_CA__DQ_TX_RT_M1_R0_CFG

Address: 0x00110370

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH0_CA__DQ_TX_RT_M1_R1_CFG

Address: 0x00110374

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_RO_CFG_0

Address: 0x00110378

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_RO_CFG_1

Address: 0x0011037C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_2

Address: 0x00110380

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_3

Address: 0x00110384

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_4

Address: 0x00110388

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_5

Address: 0x0011038C

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_6

Address: 0x00110390

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_7

Address: 0x00110394

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_8

Address: 0x00110398

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_9

Address: 0x0011039C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R0_CFG_10

Address: 0x001103A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_0

Address: 0x001103A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_1

Address: 0x001103A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_2

Address: 0x001103AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_3

Address: 0x001103B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_4

Address: 0x001103B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_5

Address: 0x001103B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_6

Address: 0x001103BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_7

Address: 0x001103C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_8

Address: 0x001103C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_9

Address: 0x001103C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_SDR_M0_R1_CFG_10

Address: 0x001103CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_0

Address: 0x001103D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_1

Address: 0x001103D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_2

Address: 0x001103D8

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_3

Address: 0x001103DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_4

Address: 0x001103E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_5

Address: 0x001103E4

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_6

Address: 0x001103E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_7

Address: 0x001103EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_8

Address: 0x001103F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_9

Address: 0x001103F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R0_CFG_10

Address: 0x001103F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_0

Address: 0x001103FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_1

Address: 0x00110400

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_2

Address: 0x00110404

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_3

Address: 0x00110408

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_4

Address: 0x0011040C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_5

Address: 0x00110410

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_6

Address: 0x00110414

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_7

Address: 0x00110418

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_8

Address: 0x0011041C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_9

Address: 0x00110420

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_M1_R1_CFG_10

Address: 0x00110424

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00110428

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x0011042C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00110430

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x00110434

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00110438

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x0011043C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00110440

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x00110444

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x00110448

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_9

Address: 0x0011044C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_10

Address: 0x00110450

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x00110454

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x00110458

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x0011045C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x00110460

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x00110464

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x00110468

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x0011046C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x00110470

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x00110474

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_9

Address: 0x00110478

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_10

Address: 0x0011047C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x00110480

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x00110484

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x00110488

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x0011048C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x00110490

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x00110494

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x00110498

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x0011049C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x001104A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_9

Address: 0x001104A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_10

Address: 0x001104A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x001104AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x001104B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x001104B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x001104B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x001104BC

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x001104C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x001104C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x001104C8

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x001104CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_9

Address: 0x001104D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_10

Address: 0x001104D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x001104D8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_1

Address: 0x001104DC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_2

Address: 0x001104E0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x001104E4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_4

Address: 0x001104E8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x001104EC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x001104F0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x001104F4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_8

Address: 0x001104F8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_9

Address: 0x001104FC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_10

Address: 0x00110500

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_0

Address: 0x00110504

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_1

Address: 0x00110508

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x0011050C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00110510

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x00110514

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x00110518

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x0011051C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x00110520

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00110524

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_9

Address: 0x00110528

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_10

Address: 0x0011052C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00110530

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x00110534

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x00110538

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x0011053C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x00110540

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_5

Address: 0x00110544

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_6

Address: 0x00110548

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_7

Address: 0x0011054C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_8

Address: 0x00110550

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_9

Address: 0x00110554

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_10

Address: 0x00110558

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x0011055C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_1

Address: 0x00110560

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_2

Address: 0x00110564

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x00110568

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x0011056C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x00110570

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x00110574

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x00110578

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x0011057C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_9

Address: 0x00110580

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_10

Address: 0x00110584

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_0

Address: 0x00110588

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_1

Address: 0x0011058C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_2

Address: 0x00110590

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_3

Address: 0x00110594

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_4

Address: 0x00110598

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_5

Address: 0x0011059C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_6

Address: 0x001105A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_7

Address: 0x001105A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_8

Address: 0x001105A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
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WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_9

Address: 0x001105AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R0_CFG_10

Address: 0x001105B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_0

Address: 0x001105B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_1

Address: 0x001105B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_2

Address: 0x001105BC

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_3

Address: 0x001105C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_4

Address: 0x001105C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_5

Address: 0x001105C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_6

Address: 0x001105CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_7

Address: 0x001105D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_8

Address: 0x001105D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_9

Address: 0x001105D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M0_R1_CFG_10

Address: 0x001105DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_0

Address: 0x001105E0

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_1

Address: 0x001105E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_2

Address: 0x001105E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_3

Address: 0x001105EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_4

Address: 0x001105F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_5

Address: 0x001105F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_6

Address: 0x001105F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_7

Address: 0x001105FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_8

Address: 0x00110600

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_9

Address: 0x00110604

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R0_CFG_10

Address: 0x00110608

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_0

Address: 0x0011060C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_1

Address: 0x00110610

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_2

Address: 0x00110614

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_3

Address: 0x00110618

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_4

Address: 0x0011061C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_5

Address: 0x00110620

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_6

Address: 0x00110624

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_7

Address: 0x00110628

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_8

Address: 0x0011062C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_9

Address: 0x00110630

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_M1_R1_CFG_10

Address: 0x00110634

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00110638

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x0011063C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00110640

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x00110644

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00110648

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x0011064C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00110650

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x00110654

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00110658

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_9

Address: 0x0011065C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_10

Address: 0x00110660

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00110664

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00110668

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x0011066C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00110670

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00110674

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00110678

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x0011067C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00110680

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00110684

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_9

Address: 0x00110688

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_10

Address: 0x0011068C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00110690

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x00110694

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00110698

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x0011069C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x001106A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x001106A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x001106A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x001106AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x001106B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_9

Address: 0x001106B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_10

Address: 0x001106B8

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x001106BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x001106C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x001106C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x001106C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x001106CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x001106D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x001106D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x001106D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x001106DC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_9

Address: 0x001106E0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_10

Address: 0x001106E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_0

Address: 0x001106E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_1

Address: 0x001106EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_2

Address: 0x001106F0

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_3

Address: 0x001106F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_4

Address: 0x001106F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_5

Address: 0x001106FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_6

Address: 0x00110700

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_7

Address: 0x00110704

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_8

Registers

Address: 0x00110708

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_9

Address: 0x0011070C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R0_CFG_10

Address: 0x00110710

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_0

Address: 0x00110714

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_1

Address: 0x00110718

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_2

Address: 0x0011071C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_3

Address: 0x00110720

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_4

Address: 0x00110724

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_5

Address: 0x00110728

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_6

Address: 0x0011072C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_7

Address: 0x00110730

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_8

Address: 0x00110734

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_9

Address: 0x00110738

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M0_R1_CFG_10

Address: 0x0011073C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_0

Address: 0x00110740

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_1

Address: 0x00110744

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_2

Address: 0x00110748

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_3

Address: 0x0011074C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_4

Address: 0x00110750

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_5

Address: 0x00110754

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_6

Address: 0x00110758

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_7

Address: 0x0011075C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_8

Address: 0x00110760

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_9

Registers

Address: 0x00110764

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R0_CFG_10

Address: 0x00110768

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_0

Address: 0x0011076C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_1

Address: 0x00110770

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_2

Address: 0x00110774

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_3

Address: 0x00110778

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_4

Address: 0x0011077C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_5

Address: 0x00110780

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_6

Address: 0x00110784

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_7

Address: 0x00110788

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_8

Address: 0x0011078C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_9

Address: 0x00110790

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH0_CA__DQ_TX_QDR_M1_R1_CFG_10

Address: 0x00110794

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00110798

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x0011079C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x001107A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x001107A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x001107A8

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x001107AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x001107B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x001107B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x001107B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_9

Address: 0x001107BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_10

Registers

Address: 0x001107C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x001107C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x001107C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x001107CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x001107D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x001107D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x001107D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x001107DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x001107E0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x001107E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_9

Address: 0x001107E8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_10

Address: 0x001107EC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x001107F0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x001107F4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x001107F8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x001107FC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x00110800

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x00110804

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x00110808

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x0011080C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x00110810

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_9

Address: 0x00110814

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_10

Address: 0x00110818

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_0

Registers

Address: 0x0011081C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x00110820

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x00110824

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x00110828

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x0011082C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x00110830

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x00110834

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x00110838

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x0011083C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_9

Address: 0x00110840

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_10

Address: 0x00110844

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_0

Address: 0x00110848

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_1

Address: 0x0011084C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_2

Address: 0x00110850

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_3

Address: 0x00110854

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_4

Address: 0x00110858

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_5

Address: 0x0011085C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_6

Address: 0x00110860

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_7

Address: 0x00110864

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_8

Address: 0x00110868

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_9

Address: 0x0011086C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R0_CFG_10

Address: 0x00110870

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_0

Address: 0x00110874

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_1

Address: 0x00110878

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_2

Address: 0x0011087C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_3

Address: 0x00110880

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_4

Address: 0x00110884

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_5

Address: 0x00110888

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_6

Address: 0x0011088C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_7

Address: 0x00110890

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_8

Address: 0x00110894

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_9

Address: 0x00110898

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M0_R1_CFG_10

Address: 0x0011089C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_0

Address: 0x001108A0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_1

Address: 0x001108A4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_2

Address: 0x001108A8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_3

Address: 0x001108AC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_4

Address: 0x001108B0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_5

Address: 0x001108B4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_6

Address: 0x001108B8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_7

Address: 0x001108BC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_8

Address: 0x001108C0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_9

Address: 0x001108C4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R0_CFG_10

Address: 0x001108C8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_0

Address: 0x001108CC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_1

Address: 0x001108D0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_2

Address: 0x001108D4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_3

Address: 0x001108D8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_4

Address: 0x001108DC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_5

Address: 0x001108E0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_6

Address: 0x001108E4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_7

Address: 0x001108E8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_8

Address: 0x001108EC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_9

Address: 0x001108F0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_LPDE_M1_R1_CFG_10

Address: 0x001108F4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_0

Address: 0x001108F8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_1

Address: 0x001108FC

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_2

Address: 0x00110900

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_3

Address: 0x00110904

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_4

Address: 0x00110908

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH0_CA__DQ_TX_IO_M0_CFG_5

Address: 0x0011090C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_6

Address: 0x00110910

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_7

Address: 0x00110914

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_8

Address: 0x00110918

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.

Registers

SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_9

Address: 0x0011091C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M0_CFG_10

Address: 0x00110920

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_0

Address: 0x00110924

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_1

Address: 0x00110928

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.

Registers

OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_2

Address: 0x0011092C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_3

Address: 0x00110930

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_4

Address: 0x00110934

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_5

Address: 0x00110938

Registers

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_6

Address: 0x0011093C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_7

Address: 0x00110940

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_8

Address: 0x00110944

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH0_CA__DQ_TX_IO_M1_CFG_9

Address: 0x00110948

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQ_TX_IO_M1_CFG_10

Address: 0x0011094C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQS_RX_M0_CFG

Address: 0x00110950

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH0_CA__DQS_RX_M1_CFG

Address: 0x00110954

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH0_CA__DQS_RX_BSCAN_STA

Registers

Address: 0x00110958

Description:

Name	Index	Type	Reset	Description
VAL	[1:0]	R	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH0_CA__DQS_RX_SDR_LPDE_M0_R0_CFG

Address: 0x0011095C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_RX_SDR_LPDE_M0_R1_CFG

Address: 0x00110960

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_RX_SDR_LPDE_M1_R0_CFG

Address: 0x00110964

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_RX_SDR_LPDE_M1_R1_CFG

Address: 0x00110968

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_RX_REN_PI_M0_R0_CFG

Address: 0x0011096C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_REN_PI_M0_R1_CFG

Address: 0x00110970

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_REN_PI_M1_R0_CFG

Address: 0x00110974

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_REN_PI_M1_R1_CFG

Address: 0x00110978

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RCS_PI_M0_R0_CFG

Address: 0x0011097C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_CA__DQS_RX_RCS_PI_M0_R1_CFG

Address: 0x00110980

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RCS_PI_M1_R0_CFG

Address: 0x00110984

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RCS_PI_M1_R1_CFG

Address: 0x00110988

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RDQS_PI_0_M0_R0_CFG

Address: 0x0011098C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RDQS_PI_0_M0_R1_CFG

Address: 0x00110990

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RDQS_PI_0_M1_R0_CFG

Address: 0x00110994

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RDQS_PI_0_M1_R1_CFG

Address: 0x00110998

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RDQS_PI_1_M0_R0_CFG

Address: 0x0011099C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RDQS_PI_1_M0_R1_CFG

Address: 0x001109A0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_CA__DQS_RX_RDQS_PI_1_M1_R0_CFG

Address: 0x001109A4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_RDQS_PI_1_M1_R1_CFG

Address: 0x001109A8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_RX_PI_STA

Address: 0x001109AC

Description:

Name	Index	Type	Reset	Description
RCS_PI_PHASE	[1]	R	0x0	Indicates the phase of RE_PI output clock wrt RCS.
REN_PI_PHASE	[0]	R	0x0	Indicates the phase of RE_PI output clock wrt REN.

WAV_CH0_CA__DQS_RX_IO_M0_R0_CFG_0

Address: 0x001109B0

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_CA__DQS_RX_IO_M0_R1_CFG_0

Address: 0x001109B4

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_CA__DQS_RX_IO_M1_R0_CFG_0

Registers

Address: 0x001109B8

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_CA__DQS_RX_IO_M1_R1_CFG_0

Address: 0x001109BC

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH0_CA__DQS_RX_IO_CMN_M0_R0_CFG

Address: 0x001109C0

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for edge detect EN and IE.

WAV_CH0_CA__DQS_RX_IO_CMN_M0_R1_CFG

Address: 0x001109C4

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).

Registers

SW_OVR	[23]	RW	0x0	Software override for RE and IE.
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WAV_CH0_CA__DQS_RX_IO_CMN_M1_R0_CFG

Address: 0x001109C8

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_CA__DQS_RX_IO_CMN_M1_R1_CFG

Address: 0x001109CC

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH0_CA__DQS_RX_IO_STA

Address: 0x001109D0

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH0_CA__DQS_RX_SA_M0_R0_CFG_0

Address: 0x001109D4

Description:

Registers

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQS_RX_SA_M0_R1_CFG_0

Address: 0x001109D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQS_RX_SA_M1_R0_CFG_0

Address: 0x001109DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQS_RX_SA_M1_R1_CFG_0

Address: 0x001109E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.

Registers

CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH0_CA__DQS_RX_SA_CMN_CFG

Address: 0x001109E4

Description:

Name	Index	Type	Reset	Description
CAL_EN_0_180	[1]	RW	0x0	Calibration enable.
CAL_EN_90_270	[3]	RW	0x0	Calibration enable.
OVR_EN_0_180	[0]	RW	0x1	Software override value of SA_Enable.
OVR_EN_90_270	[2]	RW	0x1	Software override value of SA_Enable.
SW_OVR	[4]	RW	0x0	Software override for SA enable.

WAV_CH0_CA__DQS_TX_M0_CFG

Address: 0x001109E8

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH0_CA__DQS_TX_M1_CFG

Address: 0x001109EC

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH0_CA__DQS_TX_BSCAN_CTRL_CFG

Address: 0x001109F0

Description:

Name	Index	Type	Reset	Description
IE	[0]	RW	0x0	Boundary Scan IE.
OE	[1]	RW	0x0	Boundary Scan OE.

Registers

WAV_CH0_CA__DQS_TX_BSCAN_CFG

Address: 0x001109F4

Description:

Name	Index	Type	Reset	Description
VAL	[1:0]	RW	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH0_CA__DQS_TX_EGRESS_ANA_M0_CFG_0

Address: 0x001109F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQS_TX_EGRESS_ANA_M1_CFG_0

Address: 0x001109FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH0_CA__DQS_TX_EGRESS_DIG_M0_CFG_0

Address: 0x00110A00

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQS_TX_EGRESS_DIG_M1_CFG_0

Address: 0x00110A04

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH0_CA__DQS_TX_ODR_PI_M0_R0_CFG

Address: 0x00110A08

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH0_CA__DQS_TX_ODR_PI_M0_R1_CFG

Address: 0x00110A0C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_ODR_PI_M1_R0_CFG

Address: 0x00110A10

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_ODR_PI_M1_R1_CFG

Address: 0x00110A14

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00110A18

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00110A1C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00110A20

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_QDR_PI_0_M1_R1_CFG

Address: 0x00110A24

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_QDR_PI_1_M0_R0_CFG

Address: 0x00110A28

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_QDR_PI_1_M0_R1_CFG

Address: 0x00110A2C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_CA__DQS_TX_QDR_PI_1_M1_R0_CFG

Address: 0x00110A30

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_QDR_PI_1_M1_R1_CFG

Address: 0x00110A34

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DDR_PI_0_M0_R0_CFG

Address: 0x00110A38

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DDR_PI_0_M0_R1_CFG

Address: 0x00110A3C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DDR_PI_0_M1_R0_CFG

Address: 0x00110A40

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DDR_PI_0_M1_R1_CFG

Address: 0x00110A44

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DDR_PI_1_M0_R0_CFG

Address: 0x00110A48

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DDR_PI_1_M0_R1_CFG

Address: 0x00110A4C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DDR_PI_1_M1_R0_CFG

Address: 0x00110A50

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_CA__DQS_TX_DDR_PI_1_M1_R1_CFG

Address: 0x00110A54

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_PI_RT_M0_R0_CFG

Address: 0x00110A58

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_PI_RT_M0_R1_CFG

Address: 0x00110A5C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_PI_RT_M1_R0_CFG

Address: 0x00110A60

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_PI_RT_M1_R1_CFG

Address: 0x00110A64

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_SDR_PI_M0_R0_CFG

Address: 0x00110A68

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_SDR_PI_M0_R1_CFG

Address: 0x00110A6C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_SDR_PI_M1_R0_CFG

Address: 0x00110A70

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_SDR_PI_M1_R1_CFG

Address: 0x00110A74

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH0_CA__DQS_TX_DFI_PI_M0_R0_CFG

Address: 0x00110A78

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DFI_PI_M0_R1_CFG

Address: 0x00110A7C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DFI_PI_M1_R0_CFG

Address: 0x00110A80

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_DFI_PI_M1_R1_CFG

Address: 0x00110A84

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH0_CA__DQS_TX_RT_M0_R0_CFG

Address: 0x00110A88

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN	[0:0]	RW	0x000	Pipeline enable.
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WAV_CH0_CA__DQS_TX_RT_M0_R1_CFG

Address: 0x00110A8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[0:0]	RW	0x000	Pipeline enable.

WAV_CH0_CA__DQS_TX_RT_M1_R0_CFG

Address: 0x00110A90

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[0:0]	RW	0x000	Pipeline enable.

WAV_CH0_CA__DQS_TX_RT_M1_R1_CFG

Address: 0x00110A94

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[0:0]	RW	0x000	Pipeline enable.

WAV_CH0_CA__DQS_TX_SDR_M0_R0_CFG_0

Address: 0x00110A98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQS_TX_SDR_M0_R1_CFG_0

Address: 0x00110A9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQS_TX_SDR_M1_R0_CFG_0

Address: 0x00110AA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQS_TX_SDR_M1_R1_CFG_0

Address: 0x00110AA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH0_CA__DQS_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00110AA8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.

Registers

X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQS_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x00110AAC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQS_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x00110AB0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH0_CA__DQS_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x00110AB4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.

Registers

X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.
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WAV_CH0_CA__DQS_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00110AB8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQS_TX_SDR_FC_DLY_M0_R1_CFG_0

Address: 0x00110ABC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQS_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00110AC0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH0_CA__DQS_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x00110AC4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH0_CA__DQS_TX_DDR_M0_R0_CFG_0

Address: 0x00110AC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQS_TX_DDR_M0_R1_CFG_0

Address: 0x00110ACC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQS_TX_DDR_M1_R0_CFG_0

Address: 0x00110AD0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQS_TX_DDR_M1_R1_CFG_0

Registers

Address: 0x00110AD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH0_CA__DQS_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00110AD8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQS_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00110ADC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQS_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00110AE0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQS_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x00110AE4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH0_CA__DQS_TX_QDR_M0_R0_CFG_0

Address: 0x00110AE8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQS_TX_QDR_M0_R1_CFG_0

Address: 0x00110AEC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQS_TX_QDR_M1_R0_CFG_0

Address: 0x00110AF0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQS_TX_QDR_M1_R1_CFG_0

Address: 0x00110AF4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH0_CA__DQS_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00110AF8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQS_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00110AFC

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQS_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00110B00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQS_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x00110B04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH0_CA__DQS_TX_LPDE_M0_R0_CFG_0

Address: 0x00110B08

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_TX_LPDE_M0_R1_CFG_0

Address: 0x00110B0C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_TX_LPDE_M1_R0_CFG_0

Address: 0x00110B10

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_TX_LPDE_M1_R1_CFG_0

Address: 0x00110B14

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH0_CA__DQS_TX_IO_M0_CFG_0

Address: 0x00110B18

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQS_TX_IO_M1_CFG_0

Address: 0x00110B1C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH0_CA__DQS_TX_IO_CMN_M0_R0_CFG

Address: 0x00110B20

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.

Registers

SE_MODE	[13]	RW	0x0	Single-ended mode.
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WAV_CH0_CA__DQS_TX_IO_CMN_M0_R1_CFG

Address: 0x00110B24

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_CA__DQS_TX_IO_CMN_M1_R0_CFG

Address: 0x00110B28

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH0_CA__DQS_TX_IO_CMN_M1_R1_CFG

Address: 0x00110B2C

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ0__TOP_CFG

Address: 0x00120000

Description:

Name	Index	Type	Reset	Description
FIFO_CLR	[8]	RW	0x0	FIFO clear.
RCS_SW_OVR	[2]	RW	0x0	Read Chip Select Override.
RCS_SW_OVR_VAL	[3]	RW	0x0	Read Chip Select Override value.
TRAINING_MODE	[9]	RW	0x0	Training Mode.
WCS_SW_OVR	[0]	RW	0x0	Write Chip Select Override.

Registers

WCS_SW_OVR_VAL	[1]	RW	0x0	Write Chip Select Override value.
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WAV_CH1_DQ0__TOP_STA

Address: 0x00120004

Description:

Name	Index	Type	Reset	Description
RCS	[1]	R	0x0	Read Chip Select status.
WCS	[0]	R	0x0	Write Chip Select status.

WAV_CH1_DQ0__DQ_RX_BSCAN_STA

Address: 0x00120008

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	R	0x000	Boundary Scan per-bit value.

WAV_CH1_DQ0__DQ_RX_M0_CFG

Address: 0x0012000C

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH1_DQ0__DQ_RX_M1_CFG

Address: 0x00120010

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_0

Address: 0x00120014

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_1

Address: 0x00120018

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_2

Address: 0x0012001C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_3

Address: 0x00120020

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_4

Address: 0x00120024

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_5

Address: 0x00120028

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_6

Address: 0x0012002C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_7

Address: 0x00120030

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R0_CFG_8

Address: 0x00120034

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_0

Address: 0x00120038

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_1

Address: 0x0012003C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_2

Address: 0x00120040

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_3

Address: 0x00120044

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_4

Address: 0x00120048

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_5

Address: 0x0012004C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_6

Address: 0x00120050

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_7

Address: 0x00120054

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M0_R1_CFG_8

Address: 0x00120058

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_0

Address: 0x0012005C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_1

Address: 0x00120060

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_2

Address: 0x00120064

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_3

Address: 0x00120068

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_4

Address: 0x0012006C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_5

Address: 0x00120070

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_6

Address: 0x00120074

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_7

Address: 0x00120078

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R0_CFG_8

Address: 0x0012007C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_0

Address: 0x00120080

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_1

Address: 0x00120084

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_2

Address: 0x00120088

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_3

Address: 0x0012008C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_4

Address: 0x00120090

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_5

Address: 0x00120094

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_6

Address: 0x00120098

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_7

Address: 0x0012009C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_M1_R1_CFG_8

Address: 0x001200A0

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ0__DQ_RX_IO_STA

Address: 0x001200A4

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_0

Address: 0x001200A8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_1

Address: 0x001200AC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_2

Address: 0x001200B0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.

Registers

CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_3

Address: 0x001200B4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_4

Address: 0x001200B8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_5

Address: 0x001200BC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.

Registers

CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_6

Address: 0x001200C0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_7

Address: 0x001200C4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R0_CFG_8

Address: 0x001200C8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.

Registers

CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_0

Address: 0x001200CC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_1

Address: 0x001200D0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_2

Address: 0x001200D4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.

Registers

CAL_DIR_90	[17]	RW	0x0	Calibration direction.
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WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_3

Address: 0x001200D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_4

Address: 0x001200DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_5

Address: 0x001200E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_6

Address: 0x001200E4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_7

Address: 0x001200E8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M0_R1_CFG_8

Address: 0x001200EC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_0

Address: 0x001200F0

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_1

Address: 0x001200F4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_2

Address: 0x001200F8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_3

Address: 0x001200FC

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_4

Address: 0x00120100

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_5

Address: 0x00120104

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_6

Address: 0x00120108

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_7

Address: 0x0012010C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R0_CFG_8

Address: 0x00120110

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_0

Address: 0x00120114

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_1

Address: 0x00120118

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_2

Address: 0x0012011C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_3

Address: 0x00120120

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_4

Address: 0x00120124

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_5

Address: 0x00120128

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_6

Address: 0x0012012C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_7

Address: 0x00120130

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_M1_R1_CFG_8

Address: 0x00120134

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_0

Address: 0x00120138

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M0_R0_CFG_1

Address: 0x0012013C

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_2

Address: 0x00120140

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_3

Address: 0x00120144

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_4

Address: 0x00120148

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_5

Address: 0x0012014C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_6

Address: 0x00120150

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_7

Address: 0x00120154

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R0_CFG_8

Address: 0x00120158

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_0

Address: 0x0012015C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_1

Address: 0x00120160

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_2

Address: 0x00120164

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_3

Address: 0x00120168

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M0_R1_CFG_4

Address: 0x0012016C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_5

Address: 0x00120170

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_6

Address: 0x00120174

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_7

Address: 0x00120178

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M0_R1_CFG_8

Address: 0x0012017C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_0

Address: 0x00120180

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_1

Address: 0x00120184

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_2

Address: 0x00120188

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_3

Address: 0x0012018C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_4

Address: 0x00120190

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_5

Address: 0x00120194

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_6

Address: 0x00120198

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_7

Address: 0x0012019C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R0_CFG_8

Address: 0x001201A0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_0

Address: 0x001201A4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_1

Address: 0x001201A8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_2

Address: 0x001201AC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_3

Address: 0x001201B0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_4

Address: 0x001201B4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DLY_M1_R1_CFG_5

Address: 0x001201B8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_6

Address: 0x001201BC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_7

Address: 0x001201C0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_RX_SA_DL_Y_M1_R1_CFG_8

Address: 0x001201C4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH1_DQ0__DQ_RX_SA_STA_0

Address: 0x001201C8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_1

Address: 0x001201CC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_2

Address: 0x001201D0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_3

Address: 0x001201D4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_4

Address: 0x001201D8

Description:

Name	Index	Type	Reset	Description

Registers

SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_5

Address: 0x001201DC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_6

Address: 0x001201E0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_7

Address: 0x001201E4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ0__DQ_RX_SA_STA_8

Address: 0x001201E8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

Registers

WAV_CH1_DQ0__DQ_TX_BSCAN_CFG

Address: 0x001201EC

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	RW	0x00	Boundary Scan per-bit value.

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_0

Address: 0x001201F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_1

Address: 0x001201F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_2

Address: 0x001201F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_3

Address: 0x001201FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_4

Address: 0x00120200

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_5

Registers

Address: 0x00120204

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00120208

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_7

Address: 0x0012020C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M0_CFG_8

Address: 0x00120210

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_0

Address: 0x00120214

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_1

Address: 0x00120218

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_2

Address: 0x0012021C

Registers

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_3

Address: 0x00120220

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_4

Address: 0x00120224

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_5

Address: 0x00120228

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_6

Address: 0x0012022C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_7

Address: 0x00120230

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_ANA_M1_CFG_8

Address: 0x00120234

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_0

Address: 0x00120238

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_1

Address: 0x0012023C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_2

Address: 0x00120240

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_3

Address: 0x00120244

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_4

Address: 0x00120248

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_5

Address: 0x0012024C

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_6

Address: 0x00120250

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_7

Address: 0x00120254

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M0_CFG_8

Address: 0x00120258

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_0

Address: 0x0012025C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_1

Address: 0x00120260

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_2

Address: 0x00120264

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_3

Address: 0x00120268

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_4

Address: 0x0012026C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_5

Address: 0x00120270

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_6

Address: 0x00120274

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_7

Address: 0x00120278

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_EGRESS_DIG_M1_CFG_8

Address: 0x0012027C

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQ_TX_ODR_PI_M0_R0_CFG

Address: 0x00120280

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_ODR_PI_M0_R1_CFG

Address: 0x00120284

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_ODR_PI_M1_R0_CFG

Address: 0x00120288

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_ODR_PI_M1_R1_CFG

Address: 0x0012028C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_0_M0_R0_CFG

Registers

Address: 0x00120290

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00120294

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00120298

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_0_M1_R1_CFG

Address: 0x0012029C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_1_M0_R0_CFG

Address: 0x001202A0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.

Registers

GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_1_M0_R1_CFG

Address: 0x001202A4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_1_M1_R0_CFG

Address: 0x001202A8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_QDR_PI_1_M1_R1_CFG

Address: 0x001202AC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_DDR_PI_0_M0_R0_CFG

Address: 0x001202B0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_DDR_PI_0_M0_R1_CFG

Address: 0x001202B4

Registers

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_DDR_PI_0_M1_R0_CFG

Address: 0x001202B8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_DDR_PI_0_M1_R1_CFG

Address: 0x001202BC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_DDR_PI_1_M0_R0_CFG

Address: 0x001202C0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_DDR_PI_1_M0_R1_CFG

Address: 0x001202C4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH1_DQ0__DQ_TX_DDR_PI_1_M1_R0_CFG

Address: 0x001202C8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_DDR_PI_1_M1_R1_CFG

Address: 0x001202CC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_PI_RT_M0_R0_CFG

Address: 0x001202D0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_PI_RT_M0_R1_CFG

Address: 0x001202D4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_PI_RT_M1_R0_CFG

Address: 0x001202D8

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_PI_RT_M1_R1_CFG

Address: 0x001202DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQ_TX_RT_M0_R0_CFG

Address: 0x001202E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQ_TX_RT_M0_R1_CFG

Address: 0x001202E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQ_TX_RT_M1_R0_CFG

Address: 0x001202E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQ_TX_RT_M1_R1_CFG

Address: 0x001202EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_0

Registers

Address: 0x001202F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_1

Address: 0x001202F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_2

Address: 0x001202F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_3

Address: 0x001202FC

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_4

Address: 0x00120300

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_5

Address: 0x00120304

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_6

Address: 0x00120308

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_7

Address: 0x0012030C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R0_CFG_8

Address: 0x00120310

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_0

Address: 0x00120314

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_1

Address: 0x00120318

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_2

Address: 0x0012031C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_3

Address: 0x00120320

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.

Registers

PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_4

Address: 0x00120324

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_5

Address: 0x00120328

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_6

Address: 0x0012032C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.

Registers

PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.
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WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_7

Address: 0x00120330

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M0_R1_CFG_8

Address: 0x00120334

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_0

Address: 0x00120338

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_1

Address: 0x0012033C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_2

Address: 0x00120340

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_3

Address: 0x00120344

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_4

Address: 0x00120348

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_5

Address: 0x0012034C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_6

Address: 0x00120350

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_7

Address: 0x00120354

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R0_CFG_8

Address: 0x00120358

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_0

Address: 0x0012035C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_1

Address: 0x00120360

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_2

Address: 0x00120364

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_3

Address: 0x00120368

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_4

Address: 0x0012036C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_5

Address: 0x00120370

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_6

Address: 0x00120374

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_7

Address: 0x00120378

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_M1_R1_CFG_8

Address: 0x0012037C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00120380

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x00120384

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00120388

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x0012038C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00120390

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x00120394

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00120398

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x0012039C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x001203A0

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x001203A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x001203A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x001203AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x001203B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x001203B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x001203B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x001203BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x001203C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x001203C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x001203C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x001203CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x001203D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x001203D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x001203D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x001203DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x001203E0

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x001203E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x001203E8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x001203EC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x001203F0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x001203F4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x001203F8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x001203FC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x00120400

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x00120404

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x00120408

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x0012040C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00120410

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_1

Address: 0x00120414

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_2

Address: 0x00120418

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x0012041C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_4

Address: 0x00120420

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_5

Address: 0x00120424

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_6

Address: 0x00120428

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_7

Address: 0x0012042C

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R0_CFG_8

Address: 0x00120430

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_0

Address: 0x00120434

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_1

Address: 0x00120438

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x0012043C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00120440

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x00120444

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x00120448

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x0012044C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x00120450

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00120454

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00120458

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x0012045C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x00120460

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x00120464

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x00120468

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_5

Address: 0x0012046C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_6

Address: 0x00120470

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_7

Address: 0x00120474

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DL_Y_M1_R0_CFG_8

Address: 0x00120478

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x0012047C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_1

Address: 0x00120480

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_2

Address: 0x00120484

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x00120488

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x0012048C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x00120490

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x00120494

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x00120498

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x0012049C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_0

Address: 0x001204A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_1

Address: 0x001204A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_2

Address: 0x001204A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_3

Address: 0x001204AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_4

Address: 0x001204B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_5

Address: 0x001204B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_6

Address: 0x001204B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_7

Address: 0x001204BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R0_CFG_8

Address: 0x001204C0

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_0

Address: 0x001204C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_1

Address: 0x001204C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_2

Address: 0x001204CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_3

Address: 0x001204D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_4

Address: 0x001204D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_5

Address: 0x001204D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_6

Address: 0x001204DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_7

Address: 0x001204E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M0_R1_CFG_8

Address: 0x001204E4

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_0

Address: 0x001204E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_1

Address: 0x001204EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_2

Address: 0x001204F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_3

Address: 0x001204F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_4

Address: 0x001204F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_5

Address: 0x001204FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_6

Address: 0x00120500

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_7

Address: 0x00120504

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R0_CFG_8

Address: 0x00120508

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_0

Address: 0x0012050C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_1

Address: 0x00120510

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_2

Address: 0x00120514

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_3

Address: 0x00120518

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_4

Address: 0x0012051C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_5

Address: 0x00120520

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_6

Address: 0x00120524

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_7

Address: 0x00120528

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_M1_R1_CFG_8

Address: 0x0012052C

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00120530

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x00120534

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00120538

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x0012053C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00120540

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x00120544

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00120548

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x0012054C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00120550

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00120554

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00120558

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x0012055C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00120560

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00120564

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00120568

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x0012056C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00120570

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00120574

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00120578

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x0012057C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00120580

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x00120584

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x00120588

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x0012058C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x00120590

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x00120594

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x00120598

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x0012059C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x001205A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x001205A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x001205A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x001205AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x001205B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x001205B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x001205B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x001205BC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_0

Address: 0x001205C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_1

Address: 0x001205C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_2

Address: 0x001205C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_3

Address: 0x001205CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_4

Address: 0x001205D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_5

Registers

Address: 0x001205D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_6

Address: 0x001205D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_7

Address: 0x001205DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R0_CFG_8

Address: 0x001205E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_0

Address: 0x001205E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_1

Address: 0x001205E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_2

Address: 0x001205EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_3

Address: 0x001205F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_4

Address: 0x001205F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_5

Address: 0x001205F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_6

Address: 0x001205FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_7

Address: 0x00120600

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH1_DQ0__DQ_TX_QDR_M0_R1_CFG_8

Address: 0x00120604

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_0

Address: 0x00120608

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_1

Address: 0x0012060C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_2

Address: 0x00120610

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_3

Address: 0x00120614

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_4

Address: 0x00120618

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_5

Address: 0x0012061C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_6

Address: 0x00120620

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_7

Address: 0x00120624

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R0_CFG_8

Address: 0x00120628

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_0

Address: 0x0012062C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_1

Registers

Address: 0x00120630

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_2

Address: 0x00120634

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_3

Address: 0x00120638

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_4

Address: 0x0012063C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_5

Address: 0x00120640

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_6

Address: 0x00120644

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_7

Address: 0x00120648

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_M1_R1_CFG_8

Address: 0x0012064C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00120650

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x00120654

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x00120658

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x0012065C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x00120660

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x00120664

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x00120668

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x0012066C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x00120670

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00120674

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x00120678

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x0012067C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x00120680

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x00120684

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x00120688

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_6

Registers

Address: 0x0012068C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x00120690

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x00120694

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00120698

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x0012069C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x001206A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x001206A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x001206A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x001206AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x001206B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x001206B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x001206B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x001206BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x001206C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x001206C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x001206C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x001206CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x001206D0

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x001206D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x001206D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x001206DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_0

Address: 0x001206E0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_1

Address: 0x001206E4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

Registers

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_2

Address: 0x001206E8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_3

Address: 0x001206EC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_4

Address: 0x001206F0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_5

Address: 0x001206F4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_6

Address: 0x001206F8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_7

Registers

Address: 0x001206FC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R0_CFG_8

Address: 0x00120700

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_0

Address: 0x00120704

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_1

Address: 0x00120708

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_2

Address: 0x0012070C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_3

Address: 0x00120710

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_4

Address: 0x00120714

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_5

Address: 0x00120718

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_6

Address: 0x0012071C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_7

Address: 0x00120720

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M0_R1_CFG_8

Address: 0x00120724

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_0

Address: 0x00120728

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_1

Address: 0x0012072C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_2

Address: 0x00120730

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_3

Address: 0x00120734

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_4

Address: 0x00120738

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_5

Address: 0x0012073C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_6

Address: 0x00120740

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_7

Address: 0x00120744

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R0_CFG_8

Address: 0x00120748

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_0

Address: 0x0012074C

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_1

Address: 0x00120750

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_2

Address: 0x00120754

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_3

Address: 0x00120758

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_4

Address: 0x0012075C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_5

Address: 0x00120760

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_6

Address: 0x00120764

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_7

Address: 0x00120768

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_LPDE_M1_R1_CFG_8

Address: 0x0012076C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_0

Address: 0x00120770

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_1

Registers

Address: 0x00120774

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_2

Address: 0x00120778

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_3

Address: 0x0012077C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_4

Address: 0x00120780

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.

Registers

TX_IMPD	[8:6]	RW	0x1	TX impedance code.
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WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_5

Address: 0x00120784

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_6

Address: 0x00120788

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_7

Address: 0x0012078C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M0_CFG_8

Address: 0x00120790

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.

Registers

RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_0

Address: 0x00120794

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_1

Address: 0x00120798

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_2

Address: 0x0012079C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_3

Address: 0x001207A0

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_4

Address: 0x001207A4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_5

Address: 0x001207A8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_6

Address: 0x001207AC

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_7

Address: 0x001207B0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQ_TX_IO_M1_CFG_8

Address: 0x001207B4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQS_RX_M0_CFG

Address: 0x001207B8

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH1_DQ0__DQS_RX_M1_CFG

Address: 0x001207BC

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH1_DQ0__DQS_RX_BSCAN_STA

Registers

Address: 0x001207C0

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	R	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH1_DQ0__DQS_RX_SDR_LPDE_M0_R0_CFG

Address: 0x001207C4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_RX_SDR_LPDE_M0_R1_CFG

Address: 0x001207C8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_RX_SDR_LPDE_M1_R0_CFG

Address: 0x001207CC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_RX_SDR_LPDE_M1_R1_CFG

Address: 0x001207D0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_RX_REN_PI_M0_R0_CFG

Address: 0x001207D4

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_REN_PI_M0_R1_CFG

Address: 0x001207D8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_REN_PI_M1_R0_CFG

Address: 0x001207DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_REN_PI_M1_R1_CFG

Address: 0x001207E0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RCS_PI_M0_R0_CFG

Address: 0x001207E4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ0__DQS_RX_RCS_PI_M0_R1_CFG

Address: 0x001207E8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RCS_PI_M1_R0_CFG

Address: 0x001207EC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RCS_PI_M1_R1_CFG

Address: 0x001207F0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RDQS_PI_0_M0_R0_CFG

Address: 0x001207F4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RDQS_PI_0_M0_R1_CFG

Address: 0x001207F8

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RDQS_PI_0_M1_R0_CFG

Address: 0x001207FC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RDQS_PI_0_M1_R1_CFG

Address: 0x00120800

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RDQS_PI_1_M0_R0_CFG

Address: 0x00120804

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RDQS_PI_1_M0_R1_CFG

Address: 0x00120808

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ0__DQS_RX_RDQS_PI_1_M1_R0_CFG

Address: 0x0012080C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_RDQS_PI_1_M1_R1_CFG

Address: 0x00120810

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_RX_PI_STA

Address: 0x00120814

Description:

Name	Index	Type	Reset	Description
RCS_PI_PHASE	[1]	R	0x0	Indicates the phase of RE_PI output clock wrt RCS.
REN_PI_PHASE	[0]	R	0x0	Indicates the phase of RE_PI output clock wrt REN.

WAV_CH1_DQ0__DQS_RX_IO_M0_R0_CFG_0

Address: 0x00120818

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ0__DQS_RX_IO_M0_R0_CFG_1

Address: 0x0012081C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ0__DQS_RX_IO_M0_R1_CFG_0

Registers

Address: 0x00120820

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ0__DQS_RX_IO_M0_R1_CFG_1

Address: 0x00120824

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ0__DQS_RX_IO_M1_R0_CFG_0

Address: 0x00120828

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ0__DQS_RX_IO_M1_R0_CFG_1

Address: 0x0012082C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ0__DQS_RX_IO_M1_R1_CFG_0

Address: 0x00120830

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ0__DQS_RX_IO_M1_R1_CFG_1

Address: 0x00120834

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

Registers

WAV_CH1_DQ0__DQS_RX_IO_CMN_M0_R0_CFG

Address: 0x00120838

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for edge detect EN and IE.

WAV_CH1_DQ0__DQS_RX_IO_CMN_M0_R1_CFG

Address: 0x0012083C

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_DQ0__DQS_RX_IO_CMN_M1_R0_CFG

Address: 0x00120840

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.

Registers

RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_DQ0__DQS_RX_IO_CMN_M1_R1_CFG

Address: 0x00120844

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_DQ0__DQS_RX_IO_STA

Address: 0x00120848

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH1_DQ0__DQS_RX_SA_M0_R0_CFG_0

Address: 0x0012084C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_M0_R0_CFG_1

Address: 0x00120850

Description:

Registers

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_M0_R1_CFG_0

Address: 0x00120854

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_M0_R1_CFG_1

Address: 0x00120858

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_M1_R0_CFG_0

Address: 0x0012085C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.

Registers

CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_M1_R0_CFG_1

Address: 0x00120860

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_M1_R1_CFG_0

Address: 0x00120864

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_M1_R1_CFG_1

Address: 0x00120868

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.

Registers

CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ0__DQS_RX_SA_CMN_CFG

Address: 0x0012086C

Description:

Name	Index	Type	Reset	Description
CAL_EN_0_180	[1]	RW	0x0	Calibration enable.
CAL_EN_90_270	[3]	RW	0x0	Calibration enable.
OVR_EN_0_180	[0]	RW	0x1	Software override value of SA_Enable.
OVR_EN_90_270	[2]	RW	0x1	Software override value of SA_Enable.
SW_OVR	[4]	RW	0x0	Software override for SA enable.

WAV_CH1_DQ0__DQS_TX_M0_CFG

Address: 0x00120870

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH1_DQ0__DQS_TX_M1_CFG

Address: 0x00120874

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH1_DQ0__DQS_TX_BSCAN_CTRL_CFG

Address: 0x00120878

Description:

Name	Index	Type	Reset	Description
IE	[0]	RW	0x0	Boundary Scan IE.
OE	[1]	RW	0x0	Boundary Scan OE.

WAV_CH1_DQ0__DQS_TX_BSCAN_CFG

Address: 0x0012087C

Registers

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	RW	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_0

Address: 0x00120880

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_1

Address: 0x00120884

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_2

Address: 0x00120888

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_3

Address: 0x0012088C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_4

Address: 0x00120890

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_5

Address: 0x00120894

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00120898

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_7

Address: 0x0012089C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M0_CFG_8

Address: 0x001208A0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_0

Address: 0x001208A4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_1

Address: 0x001208A8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_2

Address: 0x001208AC

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_3

Address: 0x001208B0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_4

Address: 0x001208B4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_5

Address: 0x001208B8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_6

Address: 0x001208BC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_7

Address: 0x001208C0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_ANA_M1_CFG_8

Address: 0x001208C4

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_0

Address: 0x001208C8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_1

Address: 0x001208CC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_2

Address: 0x001208D0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_3

Address: 0x001208D4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_4

Address: 0x001208D8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_5

Address: 0x001208DC

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_6

Address: 0x001208E0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_7

Address: 0x001208E4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M0_CFG_8

Address: 0x001208E8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_0

Address: 0x001208EC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_1

Address: 0x001208F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_2

Address: 0x001208F4

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_3

Address: 0x001208F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_4

Address: 0x001208FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_5

Address: 0x00120900

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_6

Address: 0x00120904

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_7

Address: 0x00120908

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_EGRESS_DIG_M1_CFG_8

Address: 0x0012090C

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ0__DQS_TX_ODR_PI_M0_R0_CFG

Address: 0x00120910

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_ODR_PI_M0_R1_CFG

Address: 0x00120914

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_ODR_PI_M1_R0_CFG

Address: 0x00120918

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_ODR_PI_M1_R1_CFG

Address: 0x0012091C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_0_M0_R0_CFG

Registers

Address: 0x00120920

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00120924

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00120928

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_0_M1_R1_CFG

Address: 0x0012092C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_1_M0_R0_CFG

Address: 0x00120930

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.

Registers

GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_1_M0_R1_CFG

Address: 0x00120934

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_1_M1_R0_CFG

Address: 0x00120938

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_QDR_PI_1_M1_R1_CFG

Address: 0x0012093C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DDR_PI_0_M0_R0_CFG

Address: 0x00120940

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DDR_PI_0_M0_R1_CFG

Address: 0x00120944

Registers

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DDR_PI_0_M1_R0_CFG

Address: 0x00120948

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DDR_PI_0_M1_R1_CFG

Address: 0x0012094C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DDR_PI_1_M0_R0_CFG

Address: 0x00120950

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DDR_PI_1_M0_R1_CFG

Address: 0x00120954

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH1_DQ0__DQS_TX_DDR_PI_1_M1_R0_CFG

Address: 0x00120958

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DDR_PI_1_M1_R1_CFG

Address: 0x0012095C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_PI_RT_M0_R0_CFG

Address: 0x00120960

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_PI_RT_M0_R1_CFG

Address: 0x00120964

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_PI_RT_M1_R0_CFG

Address: 0x00120968

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_PI_RT_M1_R1_CFG

Address: 0x0012096C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_SDR_PI_M0_R0_CFG

Address: 0x00120970

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_SDR_PI_M0_R1_CFG

Address: 0x00120974

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_SDR_PI_M1_R0_CFG

Address: 0x00120978

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ0__DQS_TX_SDR_PI_M1_R1_CFG

Address: 0x0012097C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DFI_PI_M0_R0_CFG

Address: 0x00120980

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DFI_PI_M0_R1_CFG

Address: 0x00120984

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DFI_PI_M1_R0_CFG

Address: 0x00120988

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_DFI_PI_M1_R1_CFG

Address: 0x0012098C

Description:

Name	Index	Type	Reset	Description

Registers

EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other PIs.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ0__DQS_TX_RT_M0_R0_CFG

Address: 0x00120990

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQS_TX_RT_M0_R1_CFG

Address: 0x00120994

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQS_TX_RT_M1_R0_CFG

Address: 0x00120998

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQS_TX_RT_M1_R1_CFG

Address: 0x0012099C

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_0

Address: 0x001209A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.

Registers

PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.
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WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_1

Address: 0x001209A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_2

Address: 0x001209A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_3

Address: 0x001209AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_4

Address: 0x001209B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_5

Address: 0x001209B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_6

Address: 0x001209B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_7

Address: 0x001209BC

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R0_CFG_8

Address: 0x001209C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_0

Address: 0x001209C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_1

Address: 0x001209C8

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_2

Address: 0x001209CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_3

Address: 0x001209D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_4

Address: 0x001209D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_5

Address: 0x001209D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_6

Address: 0x001209DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_7

Address: 0x001209E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M0_R1_CFG_8

Address: 0x001209E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_0

Address: 0x001209E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_1

Address: 0x001209EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_2

Address: 0x001209F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_3

Address: 0x001209F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_4

Address: 0x001209F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_5

Address: 0x001209FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_6

Address: 0x00120A00

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_7

Address: 0x00120A04

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R0_CFG_8

Address: 0x00120A08

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_0

Address: 0x00120A0C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_1

Address: 0x00120A10

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_2

Address: 0x00120A14

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_3

Address: 0x00120A18

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_4

Address: 0x00120A1C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_5

Address: 0x00120A20

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_6

Address: 0x00120A24

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_7

Address: 0x00120A28

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_M1_R1_CFG_8

Address: 0x00120A2C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00120A30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x00120A34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00120A38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x00120A3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00120A40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x00120A44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00120A48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x00120A4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x00120A50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x00120A54

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x00120A58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x00120A5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x00120A60

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x00120A64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x00120A68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x00120A6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x00120A70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x00120A74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x00120A78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x00120A7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x00120A80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x00120A84

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x00120A88

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x00120A8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x00120A90

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x00120A94

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x00120A98

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x00120A9C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x00120AA0

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x00120AA4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x00120AA8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x00120AAC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x00120AB0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x00120AB4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x00120AB8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x00120ABC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00120AC0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_1

Address: 0x00120AC4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_2

Address: 0x00120AC8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x00120ACC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_4

Address: 0x00120AD0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x00120AD4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x00120AD8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x00120ADC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_8

Address: 0x00120AE0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R1_CFG_0

Address: 0x00120AE4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R1_CFG_1

Address: 0x00120AE8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M0_R1_CFG_2

Address: 0x00120AEC

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00120AF0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x00120AF4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x00120AF8

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x00120AFC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x00120B00

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00120B04

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00120B08

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x00120B0C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x00120B10

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x00120B14

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x00120B18

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_5

Address: 0x00120B1C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x00120B20

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x00120B24

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R0_CFG_8

Address: 0x00120B28

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_0

Address: 0x00120B2C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_1

Address: 0x00120B30

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_2

Address: 0x00120B34

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DL_Y_M1_R1_CFG_3

Address: 0x00120B38

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x00120B3C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x00120B40

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x00120B44

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x00120B48

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x00120B4C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_0

Address: 0x00120B50

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_1

Address: 0x00120B54

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_2

Address: 0x00120B58

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_3

Address: 0x00120B5C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_4

Address: 0x00120B60

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_5

Address: 0x00120B64

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_6

Address: 0x00120B68

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_7

Address: 0x00120B6C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R0_CFG_8

Address: 0x00120B70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_0

Address: 0x00120B74

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
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WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_1

Address: 0x00120B78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_2

Address: 0x00120B7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_3

Address: 0x00120B80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_4

Address: 0x00120B84

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_5

Address: 0x00120B88

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_6

Address: 0x00120B8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_7

Address: 0x00120B90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M0_R1_CFG_8

Address: 0x00120B94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_0

Address: 0x00120B98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_1

Address: 0x00120B9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_2

Address: 0x00120BA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_3

Address: 0x00120BA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_4

Address: 0x00120BA8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_5

Address: 0x00120BAC

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_6

Address: 0x00120BB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_7

Address: 0x00120BB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R0_CFG_8

Address: 0x00120BB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_0

Address: 0x00120BBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_1

Address: 0x00120BC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_2

Address: 0x00120BC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_3

Address: 0x00120BC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_4

Address: 0x00120BCC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_5

Address: 0x00120BD0

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_6

Address: 0x00120BD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_7

Address: 0x00120BD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_M1_R1_CFG_8

Address: 0x00120BDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00120BE0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x00120BE4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00120BE8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x00120BEC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00120BF0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x00120BF4

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00120BF8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x00120BFC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00120C00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00120C04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00120C08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x00120C0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00120C10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00120C14

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00120C18

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x00120C1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00120C20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00120C24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00120C28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x00120C2C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00120C30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x00120C34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x00120C38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x00120C3C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x00120C40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x00120C44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x00120C48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x00120C4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x00120C50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x00120C54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x00120C58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x00120C5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x00120C60

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x00120C64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x00120C68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x00120C6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_0

Address: 0x00120C70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_1

Address: 0x00120C74

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_2

Address: 0x00120C78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_3

Address: 0x00120C7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_4

Address: 0x00120C80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_5

Address: 0x00120C84

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_6

Address: 0x00120C88

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_7

Registers

Address: 0x00120C8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R0_CFG_8

Address: 0x00120C90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_0

Address: 0x00120C94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_1

Address: 0x00120C98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_2

Address: 0x00120C9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_3

Address: 0x00120CA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_4

Address: 0x00120CA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_5

Address: 0x00120CA8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_6

Address: 0x00120CAC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_7

Address: 0x00120CB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M0_R1_CFG_8

Address: 0x00120CB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_0

Address: 0x00120CB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_1

Address: 0x00120CBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_2

Address: 0x00120CC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_3

Address: 0x00120CC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_4

Address: 0x00120CC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_5

Address: 0x00120CCC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_6

Address: 0x00120CD0

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_7

Address: 0x00120CD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R0_CFG_8

Address: 0x00120CD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_0

Address: 0x00120CDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_1

Address: 0x00120CE0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_2

Address: 0x00120CE4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_3

Registers

Address: 0x00120CE8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_4

Address: 0x00120CEC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_5

Address: 0x00120CF0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_6

Address: 0x00120CF4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_7

Address: 0x00120CF8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ0__DQS_TX_QDR_M1_R1_CFG_8

Address: 0x00120CFC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00120D00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x00120D04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x00120D08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x00120D0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x00120D10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x00120D14

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x00120D18

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x00120D1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x00120D20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00120D24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x00120D28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x00120D2C

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x00120D30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x00120D34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x00120D38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x00120D3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x00120D40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M0_R1_CFG_8

Registers

Address: 0x00120D44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00120D48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x00120D4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x00120D50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x00120D54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x00120D58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x00120D5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x00120D60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x00120D64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x00120D68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x00120D6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x00120D70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x00120D74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x00120D78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x00120D7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x00120D80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x00120D84

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x00120D88

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x00120D8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ0__DQS_TX_LPDE_M0_R0_CFG_0

Address: 0x00120D90

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_LPDE_M0_R0_CFG_1

Address: 0x00120D94

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_LPDE_M0_R1_CFG_0

Address: 0x00120D98

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_LPDE_M0_R1_CFG_1

Address: 0x00120D9C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_LPDE_M1_R0_CFG_0

Address: 0x00120DA0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_LPDE_M1_R0_CFG_1

Address: 0x00120DA4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_LPDE_M1_R1_CFG_0

Address: 0x00120DA8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_LPDE_M1_R1_CFG_1

Address: 0x00120DAC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ0__DQS_TX_IO_M0_CFG_0

Address: 0x00120DB0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.

Registers

OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQS_TX_IO_M0_CFG_1

Address: 0x00120DB4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQS_TX_IO_M1_CFG_0

Address: 0x00120DB8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQS_TX_IO_M1_CFG_1

Address: 0x00120DBC

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ0__DQS_TX_IO_CMN_M0_R0_CFG

Address: 0x00120DC0

Registers

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ0__DQS_TX_IO_CMN_M0_R1_CFG

Address: 0x00120DC4

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ0__DQS_TX_IO_CMN_M1_R0_CFG

Address: 0x00120DC8

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ0__DQS_TX_IO_CMN_M1_R1_CFG

Address: 0x00120DCC

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ1__TOP_CFG

Address: 0x00130000

Description:

Registers

Name	Index	Type	Reset	Description
FIFO_CLR	[8]	RW	0x0	FIFO clear.
RCS_SW_OVR	[2]	RW	0x0	Read Chip Select Override.
RCS_SW_OVR_VAL	[3]	RW	0x0	Read Chip Select Override value.
TRAINING_MODE	[9]	RW	0x0	Training Mode.
WCS_SW_OVR	[0]	RW	0x0	Write Chip Select Override.
WCS_SW_OVR_VAL	[1]	RW	0x0	Write Chip Select Override value.

WAV_CH1_DQ1__TOP_STA

Address: 0x00130004

Description:

Name	Index	Type	Reset	Description
RCS	[1]	R	0x0	Read Chip Select status.
WCS	[0]	R	0x0	Write Chip Select status.

WAV_CH1_DQ1__DQ_RX_BSCAN_STA

Address: 0x00130008

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	R	0x000	Boundary Scan per-bit value.

WAV_CH1_DQ1__DQ_RX_M0_CFG

Address: 0x0013000C

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH1_DQ1__DQ_RX_M1_CFG

Address: 0x00130010

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_0

Address: 0x00130014

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_1

Address: 0x00130018

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_2

Address: 0x0013001C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_3

Address: 0x00130020

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_4

Address: 0x00130024

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_5

Address: 0x00130028

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_6

Address: 0x0013002C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_7

Address: 0x00130030

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH1_DQ1__DQ_RX_IO_M0_R0_CFG_8

Address: 0x00130034

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_0

Address: 0x00130038

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_1

Address: 0x0013003C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_2

Address: 0x00130040

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_3

Address: 0x00130044

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_4

Address: 0x00130048

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_5

Address: 0x0013004C

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_6

Address: 0x00130050

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_7

Address: 0x00130054

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M0_R1_CFG_8

Address: 0x00130058

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_0

Address: 0x0013005C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_1

Address: 0x00130060

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_2

Address: 0x00130064

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_3

Address: 0x00130068

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_4

Address: 0x0013006C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_5

Address: 0x00130070

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_6

Address: 0x00130074

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_7

Address: 0x00130078

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R0_CFG_8

Address: 0x0013007C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_0

Address: 0x00130080

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_1

Address: 0x00130084

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_2

Address: 0x00130088

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_3

Address: 0x0013008C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_4

Address: 0x00130090

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_5

Address: 0x00130094

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_6

Address: 0x00130098

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_7

Address: 0x0013009C

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_M1_R1_CFG_8

Address: 0x001300A0

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_DQ1__DQ_RX_IO_STA

Address: 0x001300A4

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_0

Address: 0x001300A8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_1

Address: 0x001300AC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_2

Address: 0x001300B0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_3

Address: 0x001300B4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_4

Address: 0x001300B8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_5

Address: 0x001300BC

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_6

Address: 0x001300C0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_7

Address: 0x001300C4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R0_CFG_8

Address: 0x001300C8

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_0

Address: 0x001300CC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_1

Address: 0x001300D0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_2

Address: 0x001300D4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_3

Address: 0x001300D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_4

Address: 0x001300DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_5

Address: 0x001300E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_6

Address: 0x001300E4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_7

Address: 0x001300E8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M0_R1_CFG_8

Address: 0x001300EC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_0

Address: 0x001300F0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_1

Address: 0x001300F4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_2

Address: 0x001300F8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_3

Address: 0x001300FC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_4

Address: 0x00130100

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_5

Address: 0x00130104

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_6

Address: 0x00130108

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_7

Address: 0x0013010C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R0_CFG_8

Address: 0x00130110

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_0

Address: 0x00130114

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_1

Address: 0x00130118

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_2

Address: 0x0013011C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_3

Address: 0x00130120

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_4

Address: 0x00130124

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_5

Address: 0x00130128

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_6

Address: 0x0013012C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_7

Address: 0x00130130

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_M1_R1_CFG_8

Address: 0x00130134

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_0

Address: 0x00130138

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_1

Address: 0x0013013C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_2

Address: 0x00130140

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_3

Address: 0x00130144

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH1_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_4

Address: 0x00130148

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_5

Address: 0x0013014C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_6

Address: 0x00130150

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M0_R0_CFG_7

Address: 0x00130154

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R0_CFG_8

Address: 0x00130158

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_0

Address: 0x0013015C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_1

Address: 0x00130160

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_2

Address: 0x00130164

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_3

Address: 0x00130168

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_4

Address: 0x0013016C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_5

Address: 0x00130170

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_6

Address: 0x00130174

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M0_R1_CFG_7

Address: 0x00130178

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M0_R1_CFG_8

Address: 0x0013017C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_0

Address: 0x00130180

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_1

Address: 0x00130184

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_2

Address: 0x00130188

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_3

Address: 0x0013018C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R0_CFG_4

Address: 0x00130190

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH1_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_5

Address: 0x00130194

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_6

Address: 0x00130198

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_7

Address: 0x0013019C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DLY_M1_R0_CFG_8

Address: 0x001301A0

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_0

Address: 0x001301A4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_1

Address: 0x001301A8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_2

Address: 0x001301AC

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_3

Address: 0x001301B0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_4

Address: 0x001301B4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_5

Address: 0x001301B8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_6

Address: 0x001301BC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_7

Address: 0x001301C0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_DL_Y_M1_R1_CFG_8

Address: 0x001301C4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_RX_SA_STA_0

Address: 0x001301C8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_RX_SA_STA_1

Address: 0x001301CC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_RX_SA_STA_2

Address: 0x001301D0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_RX_SA_STA_3

Address: 0x001301D4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

Registers

WAV_CH1_DQ1__DQ_RX_SA_STA_4

Address: 0x001301D8

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_RX_SA_STA_5

Address: 0x001301DC

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_RX_SA_STA_6

Address: 0x001301E0

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_RX_SA_STA_7

Address: 0x001301E4

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_RX_SA_STA_8

Address: 0x001301E8

Description:

Name	Index	Type	Reset	Description

Registers

SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_DQ1__DQ_TX_BSCAN_CFG

Address: 0x001301EC

Description:

Name	Index	Type	Reset	Description
VAL	[8:0]	RW	0x00	Boundary Scan per-bit value.

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_0

Address: 0x001301F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_1

Address: 0x001301F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_2

Address: 0x001301F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_3

Address: 0x001301FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_4

Address: 0x00130200

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_5

Address: 0x00130204

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00130208

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_7

Address: 0x0013020C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M0_CFG_8

Address: 0x00130210

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_0

Address: 0x00130214

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_1

Address: 0x00130218

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_2

Address: 0x0013021C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_3

Address: 0x00130220

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_4

Address: 0x00130224

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_5

Address: 0x00130228

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_6

Address: 0x0013022C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_7

Address: 0x00130230

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_ANA_M1_CFG_8

Address: 0x00130234

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_0

Address: 0x00130238

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_1

Address: 0x0013023C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_2

Address: 0x00130240

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_3

Address: 0x00130244

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_4

Address: 0x00130248

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_5

Address: 0x0013024C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_6

Address: 0x00130250

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_7

Address: 0x00130254

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M0_CFG_8

Address: 0x00130258

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_0

Address: 0x0013025C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_1

Address: 0x00130260

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_2

Address: 0x00130264

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_3

Address: 0x00130268

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_4

Address: 0x0013026C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_5

Address: 0x00130270

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_6

Address: 0x00130274

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_7

Address: 0x00130278

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_EGRESS_DIG_M1_CFG_8

Address: 0x0013027C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQ_TX_ODR_PI_M0_R0_CFG

Address: 0x00130280

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_ODR_PI_M0_R1_CFG

Address: 0x00130284

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_ODR_PI_M1_R0_CFG

Address: 0x00130288

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_ODR_PI_M1_R1_CFG

Address: 0x0013028C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00130290

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00130294

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00130298

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_QDR_PI_0_M1_R1_CFG

Address: 0x0013029C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ1__DQ_TX_QDR_PI_1_M0_R0_CFG

Address: 0x001302A0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_QDR_PI_1_M0_R1_CFG

Address: 0x001302A4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_QDR_PI_1_M1_R0_CFG

Address: 0x001302A8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_QDR_PI_1_M1_R1_CFG

Address: 0x001302AC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_DDR_PI_0_M0_R0_CFG

Address: 0x001302B0

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_DDR_PI_0_M0_R1_CFG

Address: 0x001302B4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_DDR_PI_0_M1_R0_CFG

Address: 0x001302B8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_DDR_PI_0_M1_R1_CFG

Address: 0x001302BC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_DDR_PI_1_M0_R0_CFG

Address: 0x001302C0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_PI_1_M0_R1_CFG

Address: 0x001302C4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_DDR_PI_1_M1_R0_CFG

Address: 0x001302C8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_DDR_PI_1_M1_R1_CFG

Address: 0x001302CC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_PI_RT_M0_R0_CFG

Address: 0x001302D0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_PI_RT_M0_R1_CFG

Address: 0x001302D4

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_PI_RT_M1_R0_CFG

Address: 0x001302D8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_PI_RT_M1_R1_CFG

Address: 0x001302DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQ_TX_RT_M0_R0_CFG

Address: 0x001302E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ1__DQ_TX_RT_M0_R1_CFG

Address: 0x001302E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ1__DQ_TX_RT_M1_R0_CFG

Address: 0x001302E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_RT_M1_R1_CFG

Address: 0x001302EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_0

Address: 0x001302F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_1

Address: 0x001302F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_2

Address: 0x001302F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.

Registers

PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_3

Address: 0x001302FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_4

Address: 0x00130300

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_5

Address: 0x00130304

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.

Registers

PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.
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WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_6

Address: 0x00130308

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_7

Address: 0x0013030C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R0_CFG_8

Address: 0x00130310

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_0

Address: 0x00130314

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_1

Address: 0x00130318

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_2

Address: 0x0013031C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_3

Address: 0x00130320

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_4

Address: 0x00130324

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_5

Address: 0x00130328

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_6

Address: 0x0013032C

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_7

Address: 0x00130330

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M0_R1_CFG_8

Address: 0x00130334

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_0

Address: 0x00130338

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_1

Address: 0x0013033C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_2

Address: 0x00130340

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_3

Address: 0x00130344

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_4

Address: 0x00130348

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_5

Address: 0x0013034C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_6

Address: 0x00130350

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_7

Address: 0x00130354

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R0_CFG_8

Address: 0x00130358

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_0

Address: 0x0013035C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_1

Address: 0x00130360

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_2

Address: 0x00130364

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_3

Address: 0x00130368

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_4

Address: 0x0013036C

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_5

Address: 0x00130370

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_6

Address: 0x00130374

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_7

Address: 0x00130378

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_M1_R1_CFG_8

Address: 0x0013037C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00130380

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x00130384

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00130388

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x0013038C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00130390

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x00130394

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00130398

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x0013039C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x001303A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x001303A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x001303A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x001303AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x001303B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x001303B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x001303B8

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x001303BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x001303C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x001303C4

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x001303C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x001303CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x001303D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x001303D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x001303D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x001303DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x001303E0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x001303E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x001303E8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x001303EC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x001303F0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x001303F4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x001303F8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x001303FC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x00130400

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x00130404

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x00130408

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x0013040C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00130410

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_1

Address: 0x00130414

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_2

Address: 0x00130418

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x0013041C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_4

Address: 0x00130420

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x00130424

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x00130428

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x0013042C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R0_CFG_8

Address: 0x00130430

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_0

Address: 0x00130434

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_1

Address: 0x00130438

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x0013043C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00130440

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_4

Address: 0x00130444

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_5

Address: 0x00130448

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_6

Address: 0x0013044C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_7

Address: 0x00130450

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00130454

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00130458

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x0013045C

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x00130460

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x00130464

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x00130468

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_5

Address: 0x0013046C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x00130470

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x00130474

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R0_CFG_8

Address: 0x00130478

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x0013047C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_1

Address: 0x00130480

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_2

Address: 0x00130484

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x00130488

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x0013048C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_5

Address: 0x00130490

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_6

Address: 0x00130494

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_7

Address: 0x00130498

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_SDR_FC_DL_Y_M1_R1_CFG_8

Address: 0x0013049C

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_0

Address: 0x001304A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_1

Address: 0x001304A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_2

Address: 0x001304A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_3

Address: 0x001304AC

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_4

Address: 0x001304B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_5

Address: 0x001304B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_6

Address: 0x001304B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_7

Address: 0x001304BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_M0_R0_CFG_8

Address: 0x001304C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_0

Address: 0x001304C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_1

Address: 0x001304C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_2

Address: 0x001304CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_3

Address: 0x001304D0

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_4

Address: 0x001304D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_5

Address: 0x001304D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_6

Address: 0x001304DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_7

Address: 0x001304E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_M0_R1_CFG_8

Address: 0x001304E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_0

Address: 0x001304E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_1

Address: 0x001304EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_2

Address: 0x001304F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_3

Address: 0x001304F4

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_4

Address: 0x001304F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_5

Address: 0x001304FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_6

Address: 0x00130500

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_7

Address: 0x00130504

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_M1_R0_CFG_8

Address: 0x00130508

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_0

Address: 0x0013050C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_1

Address: 0x00130510

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_2

Address: 0x00130514

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_3

Address: 0x00130518

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_4

Address: 0x0013051C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_5

Address: 0x00130520

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_6

Address: 0x00130524

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_7

Address: 0x00130528

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_M1_R1_CFG_8

Address: 0x0013052C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00130530

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x00130534

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00130538

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x0013053C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00130540

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x00130544

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00130548

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x0013054C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00130550

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00130554

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00130558

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x0013055C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00130560

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00130564

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00130568

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x0013056C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00130570

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00130574

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00130578

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x0013057C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00130580

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x00130584

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x00130588

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x0013058C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x00130590

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x00130594

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x00130598

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x0013059C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x001305A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x001305A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x001305A8

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x001305AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x001305B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x001305B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x001305B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x001305BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_0

Address: 0x001305C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_1

Address: 0x001305C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_2

Address: 0x001305C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_3

Address: 0x001305CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_4

Address: 0x001305D0

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_5

Address: 0x001305D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_6

Address: 0x001305D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_7

Address: 0x001305DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R0_CFG_8

Address: 0x001305E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_0

Address: 0x001305E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_1

Registers

Address: 0x001305E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_2

Address: 0x001305EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_3

Address: 0x001305F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_4

Address: 0x001305F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_5

Address: 0x001305F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_6

Address: 0x001305FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_7

Address: 0x00130600

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M0_R1_CFG_8

Address: 0x00130604

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_0

Address: 0x00130608

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_1

Address: 0x0013060C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_2

Address: 0x00130610

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_3

Address: 0x00130614

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_4

Address: 0x00130618

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_5

Address: 0x0013061C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_6

Address: 0x00130620

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_7

Address: 0x00130624

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R0_CFG_8

Address: 0x00130628

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_0

Address: 0x0013062C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_1

Address: 0x00130630

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_2

Address: 0x00130634

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_3

Address: 0x00130638

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_4

Address: 0x0013063C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_5

Address: 0x00130640

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_6

Registers

Address: 0x00130644

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_7

Address: 0x00130648

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_M1_R1_CFG_8

Address: 0x0013064C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00130650

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x00130654

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x00130658

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x0013065C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x00130660

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x00130664

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x00130668

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x0013066C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x00130670

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00130674

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x00130678

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x0013067C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x00130680

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x00130684

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x00130688

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x0013068C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x00130690

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x00130694

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00130698

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x0013069C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_2

Registers

Address: 0x001306A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x001306A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x001306A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x001306AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x001306B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x001306B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x001306B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x001306BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x001306C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x001306C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x001306C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x001306CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x001306D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x001306D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x001306D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x001306DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_0

Address: 0x001306E0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_1

Address: 0x001306E4

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_2

Address: 0x001306E8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_3

Address: 0x001306EC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_4

Address: 0x001306F0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_5

Address: 0x001306F4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_6

Address: 0x001306F8

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_7

Address: 0x001306FC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R0_CFG_8

Address: 0x00130700

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_0

Address: 0x00130704

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_1

Address: 0x00130708

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_2

Address: 0x0013070C

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_3

Address: 0x00130710

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_4

Address: 0x00130714

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_5

Address: 0x00130718

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_6

Address: 0x0013071C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_7

Address: 0x00130720

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M0_R1_CFG_8

Address: 0x00130724

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_0

Address: 0x00130728

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_1

Address: 0x0013072C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_2

Address: 0x00130730

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_3

Address: 0x00130734

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_4

Address: 0x00130738

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_5

Address: 0x0013073C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_6

Address: 0x00130740

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_7

Address: 0x00130744

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R0_CFG_8

Address: 0x00130748

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_0

Address: 0x0013074C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_1

Address: 0x00130750

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_2

Address: 0x00130754

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_3

Address: 0x00130758

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_4

Address: 0x0013075C

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_5

Address: 0x00130760

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_6

Address: 0x00130764

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_7

Address: 0x00130768

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_LPDE_M1_R1_CFG_8

Address: 0x0013076C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_0

Address: 0x00130770

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_1

Address: 0x00130774

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_2

Address: 0x00130778

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_3

Address: 0x0013077C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_4

Address: 0x00130780

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_5

Address: 0x00130784

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_6

Address: 0x00130788

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_7

Address: 0x0013078C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.

Registers

SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M0_CFG_8

Address: 0x00130790

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_0

Address: 0x00130794

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_1

Address: 0x00130798

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_2

Address: 0x0013079C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.

Registers

OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_3

Address: 0x001307A0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_4

Address: 0x001307A4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_5

Address: 0x001307A8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_6

Address: 0x001307AC

Registers

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_7

Address: 0x001307B0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQ_TX_IO_M1_CFG_8

Address: 0x001307B4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQS_RX_M0_CFG

Address: 0x001307B8

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH1_DQ1__DQS_RX_M1_CFG

Registers

Address: 0x001307BC

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH1_DQ1__DQS_RX_BSCAN_STA

Address: 0x001307C0

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	R	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH1_DQ1__DQS_RX_SDR_LPDE_M0_R0_CFG

Address: 0x001307C4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_RX_SDR_LPDE_M0_R1_CFG

Address: 0x001307C8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_RX_SDR_LPDE_M1_R0_CFG

Address: 0x001307CC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_RX_SDR_LPDE_M1_R1_CFG

Address: 0x001307D0

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_RX_REN_PI_M0_R0_CFG

Address: 0x001307D4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_REN_PI_M0_R1_CFG

Address: 0x001307D8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_REN_PI_M1_R0_CFG

Address: 0x001307DC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_REN_PI_M1_R1_CFG

Address: 0x001307E0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ1__DQS_RX_RCS_PI_M0_R0_CFG

Address: 0x001307E4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RCS_PI_M0_R1_CFG

Address: 0x001307E8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RCS_PI_M1_R0_CFG

Address: 0x001307EC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RCS_PI_M1_R1_CFG

Address: 0x001307F0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RDQS_PI_0_M0_R0_CFG

Address: 0x001307F4

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RDQS_PI_0_M0_R1_CFG

Address: 0x001307F8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RDQS_PI_0_M1_R0_CFG

Address: 0x001307FC

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RDQS_PI_0_M1_R1_CFG

Address: 0x00130800

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RDQS_PI_1_M0_R0_CFG

Address: 0x00130804

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ1__DQS_RX_RDQS_PI_1_M0_R1_CFG

Address: 0x00130808

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RDQS_PI_1_M1_R0_CFG

Address: 0x0013080C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_RDQS_PI_1_M1_R1_CFG

Address: 0x00130810

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_RX_PI_STA

Address: 0x00130814

Description:

Name	Index	Type	Reset	Description
RCS_PI_PHASE	[1]	R	0x0	Indicates the phase of RE_PI output clock wrt RCS.
REN_PI_PHASE	[0]	R	0x0	Indicates the phase of RE_PI output clock wrt REN.

WAV_CH1_DQ1__DQS_RX_IO_M0_R0_CFG_0

Address: 0x00130818

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

Registers

WAV_CH1_DQ1__DQS_RX_IO_M0_R0_CFG_1

Address: 0x0013081C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ1__DQS_RX_IO_M0_R1_CFG_0

Address: 0x00130820

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ1__DQS_RX_IO_M0_R1_CFG_1

Address: 0x00130824

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ1__DQS_RX_IO_M1_R0_CFG_0

Address: 0x00130828

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ1__DQS_RX_IO_M1_R0_CFG_1

Address: 0x0013082C

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ1__DQS_RX_IO_M1_R1_CFG_0

Address: 0x00130830

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.

Registers

DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.
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WAV_CH1_DQ1__DQS_RX_IO_M1_R1_CFG_1

Address: 0x00130834

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_DQ1__DQS_RX_IO_CMN_M0_R0_CFG

Address: 0x00130838

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for edge detect EN and IE.

WAV_CH1_DQ1__DQS_RX_IO_CMN_M0_R1_CFG

Address: 0x0013083C

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_DQ1__DQS_RX_IO_CMN_M1_R0_CFG

Address: 0x00130840

Registers

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_DQ1__DQS_RX_IO_CMN_M1_R1_CFG

Address: 0x00130844

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_DQ1__DQS_RX_IO_STA

Address: 0x00130848

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH1_DQ1__DQS_RX_SA_M0_R0_CFG_0

Address: 0x0013084C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.

Registers

CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQS_RX_SA_M0_R0_CFG_1

Address: 0x00130850

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQS_RX_SA_M0_R1_CFG_0

Address: 0x00130854

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQS_RX_SA_M0_R1_CFG_1

Address: 0x00130858

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.

Registers

CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQS_RX_SA_M1_R0_CFG_0

Address: 0x0013085C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQS_RX_SA_M1_R0_CFG_1

Address: 0x00130860

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQS_RX_SA_M1_R1_CFG_0

Address: 0x00130864

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.

Registers

CAL_DIR_90	[17]	RW	0x0	Calibration direction.
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WAV_CH1_DQ1__DQS_RX_SA_M1_R1_CFG_1

Address: 0x00130868

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_DQ1__DQS_RX_SA_CMN_CFG

Address: 0x0013086C

Description:

Name	Index	Type	Reset	Description
CAL_EN_0_180	[1]	RW	0x0	Calibration enable.
CAL_EN_90_270	[3]	RW	0x0	Calibration enable.
OVR_EN_0_180	[0]	RW	0x1	Software override value of SA_Enable.
OVR_EN_90_270	[2]	RW	0x1	Software override value of SA_Enable.
SW_OVR	[4]	RW	0x0	Software override for SA enable.

WAV_CH1_DQ1__DQS_TX_M0_CFG

Address: 0x00130870

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH1_DQ1__DQS_TX_M1_CFG

Address: 0x00130874

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

Registers

WAV_CH1_DQ1__DQS_TX_BSCAN_CTRL_CFG

Address: 0x00130878

Description:

Name	Index	Type	Reset	Description
IE	[0]	RW	0x0	Boundary Scan IE.
OE	[1]	RW	0x0	Boundary Scan OE.

WAV_CH1_DQ1__DQS_TX_BSCAN_CFG

Address: 0x0013087C

Description:

Name	Index	Type	Reset	Description
VAL	[3:0]	RW	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_0

Address: 0x00130880

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_1

Address: 0x00130884

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_2

Address: 0x00130888

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_3

Address: 0x0013088C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_4

Registers

Address: 0x00130890

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_5

Address: 0x00130894

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00130898

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_7

Address: 0x0013089C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M0_CFG_8

Address: 0x001308A0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_0

Address: 0x001308A4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_1

Address: 0x001308A8

Registers

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_2

Address: 0x001308AC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_3

Address: 0x001308B0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_4

Address: 0x001308B4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_5

Address: 0x001308B8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_6

Address: 0x001308BC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_7

Address: 0x001308C0

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_ANA_M1_CFG_8

Address: 0x001308C4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_0

Address: 0x001308C8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_1

Address: 0x001308CC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_2

Address: 0x001308D0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_3

Address: 0x001308D4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_4

Address: 0x001308D8

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_5

Address: 0x001308DC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_6

Address: 0x001308E0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_7

Address: 0x001308E4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M0_CFG_8

Address: 0x001308E8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_0

Address: 0x001308EC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_1

Address: 0x001308F0

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_2

Address: 0x001308F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_3

Address: 0x001308F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_4

Address: 0x001308FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_5

Address: 0x00130900

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_6

Address: 0x00130904

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_7

Address: 0x00130908

Description:

Registers

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_EGRESS_DIG_M1_CFG_8

Address: 0x0013090C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_DQ1__DQS_TX_ODR_PI_M0_R0_CFG

Address: 0x00130910

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_ODR_PI_M0_R1_CFG

Address: 0x00130914

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_ODR_PI_M1_R0_CFG

Address: 0x00130918

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_ODR_PI_M1_R1_CFG

Address: 0x0013091C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00130920

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00130924

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00130928

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_QDR_PI_0_M1_R1_CFG

Address: 0x0013092C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ1__DQS_TX_QDR_PI_1_M0_R0_CFG

Address: 0x00130930

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_QDR_PI_1_M0_R1_CFG

Address: 0x00130934

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_QDR_PI_1_M1_R0_CFG

Address: 0x00130938

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_QDR_PI_1_M1_R1_CFG

Address: 0x0013093C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DDR_PI_0_M0_R0_CFG

Address: 0x00130940

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DDR_PI_0_M0_R1_CFG

Address: 0x00130944

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DDR_PI_0_M1_R0_CFG

Address: 0x00130948

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DDR_PI_0_M1_R1_CFG

Address: 0x0013094C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DDR_PI_1_M0_R0_CFG

Address: 0x00130950

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ1__DQS_TX_DDR_PI_1_M0_R1_CFG

Address: 0x00130954

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DDR_PI_1_M1_R0_CFG

Address: 0x00130958

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DDR_PI_1_M1_R1_CFG

Address: 0x0013095C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_PI_RT_M0_R0_CFG

Address: 0x00130960

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_PI_RT_M0_R1_CFG

Address: 0x00130964

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_PI_RT_M1_R0_CFG

Address: 0x00130968

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_PI_RT_M1_R1_CFG

Address: 0x0013096C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_SDR_PI_M0_R0_CFG

Address: 0x00130970

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_SDR_PI_M0_R1_CFG

Address: 0x00130974

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_DQ1__DQS_TX_SDR_PI_M1_R0_CFG

Address: 0x00130978

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_SDR_PI_M1_R1_CFG

Address: 0x0013097C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DFI_PI_M0_R0_CFG

Address: 0x00130980

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DFI_PI_M0_R1_CFG

Address: 0x00130984

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DFI_PI_M1_R0_CFG

Address: 0x00130988

Description:

Name	Index	Type	Reset	Description

Registers

EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other PIs.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_DFI_PI_M1_R1_CFG

Address: 0x0013098C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other PIs.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_DQ1__DQS_TX_RT_M0_R0_CFG

Address: 0x00130990

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ1__DQS_TX_RT_M0_R1_CFG

Address: 0x00130994

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ1__DQS_TX_RT_M1_R0_CFG

Address: 0x00130998

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ1__DQS_TX_RT_M1_R1_CFG

Address: 0x0013099C

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[8:0]	RW	0x000	Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_0

Address: 0x001309A0

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_1

Address: 0x001309A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_2

Address: 0x001309A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_3

Address: 0x001309AC

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_4

Address: 0x001309B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_5

Address: 0x001309B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_6

Address: 0x001309B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_7

Address: 0x001309BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R0_CFG_8

Address: 0x001309C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_0

Address: 0x001309C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_1

Address: 0x001309C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_2

Address: 0x001309CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_3

Address: 0x001309D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_4

Address: 0x001309D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_5

Address: 0x001309D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_6

Address: 0x001309DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_7

Address: 0x001309E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M0_R1_CFG_8

Address: 0x001309E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_0

Address: 0x001309E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_1

Address: 0x001309EC

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_2

Address: 0x001309F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_3

Address: 0x001309F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_4

Address: 0x001309F8

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_5

Address: 0x001309FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_6

Address: 0x00130A00

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_7

Address: 0x00130A04

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R0_CFG_8

Address: 0x00130A08

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_0

Address: 0x00130A0C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_1

Address: 0x00130A10

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_2

Address: 0x00130A14

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_3

Address: 0x00130A18

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_4

Address: 0x00130A1C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_5

Address: 0x00130A20

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_6

Address: 0x00130A24

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_7

Address: 0x00130A28

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_DQ1__DQS_TX_SDR_M1_R1_CFG_8

Address: 0x00130A2C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00130A30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x00130A34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00130A38

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x00130A3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00130A40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x00130A44

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00130A48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x00130A4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x00130A50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x00130A54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x00130A58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x00130A5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x00130A60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x00130A64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x00130A68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x00130A6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x00130A70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x00130A74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x00130A78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x00130A7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x00130A80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x00130A84

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x00130A88

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x00130A8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x00130A90

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x00130A94

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x00130A98

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x00130A9C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x00130AA0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x00130AA4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x00130AA8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x00130AAC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x00130AB0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x00130AB4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x00130AB8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x00130ABC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00130AC0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_1

Address: 0x00130AC4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_2

Address: 0x00130AC8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_3

Address: 0x00130ACC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M0_R0_CFG_4

Address: 0x00130AD0

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x00130AD4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x00130AD8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x00130ADC

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R0_CFG_8

Address: 0x00130AE0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_0

Address: 0x00130AE4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_1

Address: 0x00130AE8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x00130AEC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00130AF0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x00130AF4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x00130AF8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x00130AFC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x00130B00

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00130B04

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00130B08

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x00130B0C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_2

Address: 0x00130B10

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_3

Address: 0x00130B14

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_4

Address: 0x00130B18

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DL_Y_M1_R0_CFG_5

Address: 0x00130B1C

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x00130B20

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x00130B24

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R0_CFG_8

Address: 0x00130B28

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x00130B2C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_1

Address: 0x00130B30

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_2

Address: 0x00130B34

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x00130B38

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x00130B3C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x00130B40

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x00130B44

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x00130B48

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x00130B4C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_0

Address: 0x00130B50

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_1

Address: 0x00130B54

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_2

Address: 0x00130B58

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_3

Address: 0x00130B5C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_4

Address: 0x00130B60

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_5

Address: 0x00130B64

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_6

Address: 0x00130B68

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_7

Address: 0x00130B6C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R0_CFG_8

Address: 0x00130B70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
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WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_0

Address: 0x00130B74

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_1

Address: 0x00130B78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_2

Address: 0x00130B7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_3

Address: 0x00130B80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_4

Address: 0x00130B84

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_5

Address: 0x00130B88

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_6

Address: 0x00130B8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_7

Address: 0x00130B90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M0_R1_CFG_8

Address: 0x00130B94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_0

Address: 0x00130B98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_1

Address: 0x00130B9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_2

Address: 0x00130BA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_3

Address: 0x00130BA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_4

Address: 0x00130BA8

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_5

Address: 0x00130BAC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_6

Address: 0x00130BB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_7

Address: 0x00130BB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R0_CFG_8

Address: 0x00130BB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_0

Address: 0x00130BBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_1

Address: 0x00130BC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_2

Address: 0x00130BC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_3

Address: 0x00130BC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_4

Address: 0x00130BCC

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_5

Address: 0x00130BD0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_6

Address: 0x00130BD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_7

Address: 0x00130BD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_DDR_M1_R1_CFG_8

Address: 0x00130BDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00130BE0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x00130BE4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00130BE8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x00130BEC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00130BF0

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x00130BF4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00130BF8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x00130BFC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00130C00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00130C04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00130C08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x00130C0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00130C10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00130C14

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00130C18

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x00130C1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00130C20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00130C24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00130C28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x00130C2C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00130C30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x00130C34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x00130C38

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x00130C3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x00130C40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x00130C44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x00130C48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x00130C4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x00130C50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x00130C54

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x00130C58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x00130C5C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x00130C60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x00130C64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x00130C68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_DQ1__DQS_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x00130C6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_0

Address: 0x00130C70

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_1

Address: 0x00130C74

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_2

Address: 0x00130C78

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_3

Address: 0x00130C7C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_4

Address: 0x00130C80

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_5

Address: 0x00130C84

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_6

Address: 0x00130C88

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_7

Address: 0x00130C8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R0_CFG_8

Address: 0x00130C90

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_0

Address: 0x00130C94

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_1

Address: 0x00130C98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_2

Address: 0x00130C9C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_3

Address: 0x00130CA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_4

Address: 0x00130CA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_5

Address: 0x00130CA8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_6

Address: 0x00130CAC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_7

Address: 0x00130CB0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M0_R1_CFG_8

Registers

Address: 0x00130CB4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_0

Address: 0x00130CB8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_1

Address: 0x00130CBC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_2

Address: 0x00130CC0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_3

Address: 0x00130CC4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_4

Address: 0x00130CC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_5

Address: 0x00130CCC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_6

Address: 0x00130CD0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_7

Address: 0x00130CD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R0_CFG_8

Address: 0x00130CD8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_0

Address: 0x00130CDC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_1

Address: 0x00130CEO

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_2

Address: 0x00130CE4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_3

Address: 0x00130CE8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_4

Address: 0x00130CEC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_5

Address: 0x00130CF0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_6

Address: 0x00130CF4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_7

Address: 0x00130CF8

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_M1_R1_CFG_8

Address: 0x00130CFC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00130D00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x00130D04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x00130D08

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x00130D0C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_4

Registers

Address: 0x00130D10

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x00130D14

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x00130D18

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x00130D1C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x00130D20

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00130D24

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x00130D28

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x00130D2C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x00130D30

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x00130D34

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x00130D38

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x00130D3C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x00130D40

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x00130D44

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00130D48

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x00130D4C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x00130D50

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x00130D54

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x00130D58

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x00130D5C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x00130D60

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x00130D64

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x00130D68

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_0

Registers

Address: 0x00130D6C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x00130D70

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x00130D74

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x00130D78

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x00130D7C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x00130D80

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x00130D84

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x00130D88

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x00130D8C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_DQ1__DQS_TX_LPDE_M0_R0_CFG_0

Address: 0x00130D90

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_LPDE_M0_R0_CFG_1

Address: 0x00130D94

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_LPDE_M0_R1_CFG_0

Address: 0x00130D98

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_LPDE_M0_R1_CFG_1

Address: 0x00130D9C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_LPDE_M1_R0_CFG_0

Address: 0x00130DA0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_LPDE_M1_R0_CFG_1

Address: 0x00130DA4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_LPDE_M1_R1_CFG_0

Address: 0x00130DA8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_LPDE_M1_R1_CFG_1

Address: 0x00130DAC

Description:

Registers

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_DQ1__DQS_TX_IO_M0_CFG_0

Address: 0x00130DB0

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQS_TX_IO_M0_CFG_1

Address: 0x00130DB4

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQS_TX_IO_M1_CFG_0

Address: 0x00130DB8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQS_TX_IO_M1_CFG_1

Address: 0x00130DBC

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_DQ1__DQS_TX_IO_CMN_M0_R0_CFG

Address: 0x00130DC0

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ1__DQS_TX_IO_CMN_M0_R1_CFG

Address: 0x00130DC4

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ1__DQS_TX_IO_CMN_M1_R0_CFG

Address: 0x00130DC8

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_DQ1__DQS_TX_IO_CMN_M1_R1_CFG

Address: 0x00130DCC

Description:

Registers

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_CA__TOP_CFG

Address: 0x00140000

Description:

Name	Index	Type	Reset	Description
FIFO_CLR	[8]	RW	0x0	FIFO clear.
RCS_SW_OVR	[2]	RW	0x0	Read Chip Select Override.
RCS_SW_OVR_VAL	[3]	RW	0x0	Read Chip Select Override value.
TRAINING_MODE	[9]	RW	0x0	Training Mode.
WCS_SW_OVR	[0]	RW	0x0	Write Chip Select Override.
WCS_SW_OVR_VAL	[1]	RW	0x0	Write Chip Select Override value.

WAV_CH1_CA__TOP_STA

Address: 0x00140004

Description:

Name	Index	Type	Reset	Description
RCS	[1]	R	0x0	Read Chip Select status.
WCS	[0]	R	0x0	Write Chip Select status.

WAV_CH1_CA__DQ_RX_BSCAN_STA

Address: 0x00140008

Description:

Name	Index	Type	Reset	Description
VAL	[10:0]	R	0x000	Boundary Scan per-bit value.

WAV_CH1_CA__DQ_RX_M0_CFG

Address: 0x0014000C

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH1_CA__DQ_RX_M1_CFG

Address: 0x00140010

Description:

Registers

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_0

Address: 0x00140014

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_1

Address: 0x00140018

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_2

Address: 0x0014001C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_3

Address: 0x00140020

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_4

Address: 0x00140024

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_5

Address: 0x00140028

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_6

Address: 0x0014002C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_7

Address: 0x00140030

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_8

Address: 0x00140034

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_9

Address: 0x00140038

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R0_CFG_10

Address: 0x0014003C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_0

Address: 0x00140040

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_1

Address: 0x00140044

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_2

Address: 0x00140048

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_3

Address: 0x0014004C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_4

Address: 0x00140050

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_5

Address: 0x00140054

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_6

Address: 0x00140058

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_7

Address: 0x0014005C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_8

Address: 0x00140060

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_9

Address: 0x00140064

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M0_R1_CFG_10

Address: 0x00140068

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_0

Address: 0x0014006C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_1

Address: 0x00140070

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_2

Address: 0x00140074

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_3

Address: 0x00140078

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_4

Address: 0x0014007C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_5

Address: 0x00140080

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_6

Address: 0x00140084

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_7

Address: 0x00140088

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_8

Address: 0x0014008C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_9

Address: 0x00140090

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R0_CFG_10

Address: 0x00140094

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

Registers

RESERVED	[7:0]	RW	0x0	TBD Configuration.
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WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_0

Address: 0x00140098

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_1

Address: 0x0014009C

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_2

Address: 0x001400A0

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_3

Address: 0x001400A4

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_4

Address: 0x001400A8

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_5

Address: 0x001400AC

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_6

Address: 0x001400B0

Registers

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_7

Address: 0x001400B4

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_8

Address: 0x001400B8

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_9

Address: 0x001400BC

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_M1_R1_CFG_10

Address: 0x001400C0

Description:

Name	Index	Type	Reset	Description
RESERVED	[7:0]	RW	0x0	TBD Configuration.

WAV_CH1_CA__DQ_RX_IO_STA

Address: 0x001400C4

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_0

Address: 0x001400C8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_1

Address: 0x001400CC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_2

Address: 0x001400D0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_3

Address: 0x001400D4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_4

Address: 0x001400D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_5

Address: 0x001400DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_6

Address: 0x001400E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_7

Address: 0x001400E4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_8

Address: 0x001400E8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_9

Address: 0x001400EC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH1_CA__DQ_RX_SA_M0_R0_CFG_10

Address: 0x001400F0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_0

Address: 0x001400F4

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_1

Address: 0x001400F8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_2

Address: 0x001400FC

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_3

Address: 0x00140100

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_4

Address: 0x00140104

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_5

Address: 0x00140108

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_6

Address: 0x0014010C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_7

Address: 0x00140110

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_8

Address: 0x00140114

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_9

Address: 0x00140118

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M0_R1_CFG_10

Address: 0x0014011C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_0

Address: 0x00140120

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_1

Address: 0x00140124

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_2

Address: 0x00140128

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_3

Address: 0x0014012C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.

Registers

CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_4

Address: 0x00140130

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_5

Address: 0x00140134

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_6

Address: 0x00140138

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

Registers

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_7

Address: 0x0014013C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_8

Address: 0x00140140

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_9

Address: 0x00140144

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R0_CFG_10

Address: 0x00140148

Registers

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_0

Address: 0x0014014C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_1

Address: 0x00140150

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_2

Address: 0x00140154

Description:

Name	Index	Type	Reset	Description

Registers

CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_3

Address: 0x00140158

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_4

Address: 0x0014015C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_5

Address: 0x00140160

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.

Registers

CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_6

Address: 0x00140164

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_7

Address: 0x00140168

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_8

Address: 0x0014016C

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.

Registers

CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_9

Address: 0x00140170

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_M1_R1_CFG_10

Address: 0x00140174

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_0

Address: 0x00140178

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_1

Address: 0x0014017C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_2

Address: 0x00140180

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_3

Address: 0x00140184

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_4

Address: 0x00140188

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_5

Address: 0x0014018C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_6

Address: 0x00140190

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_7

Address: 0x00140194

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_8

Address: 0x00140198

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_9

Address: 0x0014019C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R0_CFG_10

Address: 0x001401A0

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_0

Address: 0x001401A4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_1

Address: 0x001401A8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_2

Address: 0x001401AC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_3

Address: 0x001401B0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_4

Address: 0x001401B4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_5

Address: 0x001401B8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_6

Address: 0x001401BC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_7

Address: 0x001401C0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_8

Address: 0x001401C4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_9

Address: 0x001401C8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M0_R1_CFG_10

Address: 0x001401CC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_0

Address: 0x001401D0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_1

Address: 0x001401D4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_2

Address: 0x001401D8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_3

Address: 0x001401DC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_4

Address: 0x001401E0

Registers

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_5

Address: 0x001401E4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_6

Address: 0x001401E8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_7

Address: 0x001401EC

Description:

Name	Index	Type	Reset	Description

Registers

CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_8

Address: 0x001401F0

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_9

Address: 0x001401F4

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R0_CFG_10

Address: 0x001401F8

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.

Registers

CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_0

Address: 0x001401FC

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_1

Address: 0x00140200

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_2

Address: 0x00140204

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.

Registers

GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_3

Address: 0x00140208

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_4

Address: 0x0014020C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_5

Address: 0x00140210

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.

Registers

GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_6

Address: 0x00140214

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_7

Address: 0x00140218

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_8

Address: 0x0014021C

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

Registers

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_9

Address: 0x00140220

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_DLY_M1_R1_CFG_10

Address: 0x00140224

Description:

Name	Index	Type	Reset	Description
CTRL_0	[7:2]	RW	0x00	Programmable binary delay.
CTRL_180	[23:18]	RW	0x00	Programmable binary delay.
CTRL_270	[31:26]	RW	0x00	Programmable binary delay.
CTRL_90	[15:10]	RW	0x00	Programmable binary delay.
GEAR_0	[1:0]	RW	0x0	Performance calibration.
GEAR_180	[17:16]	RW	0x0	Performance calibration.
GEAR_270	[25:24]	RW	0x0	Performance calibration.
GEAR_90	[9:8]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_RX_SA_STA_0

Address: 0x00140228

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_1

Address: 0x0014022C

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.

Registers

SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_2

Address: 0x00140230

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_3

Address: 0x00140234

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_4

Address: 0x00140238

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_5

Address: 0x0014023C

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_6

Address: 0x00140240

Registers

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_7

Address: 0x00140244

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_8

Address: 0x00140248

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_9

Address: 0x0014024C

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.
SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.

WAV_CH1_CA__DQ_RX_SA_STA_10

Address: 0x00140250

Description:

Name	Index	Type	Reset	Description
SA_OUT_0	[0]	R	0x0	Phase 0 Sense Amp output.
SA_OUT_180	[2]	R	0x0	Phase 2 Sense Amp output.
SA_OUT_270	[3]	R	0x0	Phase 3 Sense Amp output.

Registers

SA_OUT_90	[1]	R	0x0	Phase 1 Sense Amp output.
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WAV_CH1_CA__DQ_TX_BSCAN_CFG

Address: 0x00140254

Description:

Name	Index	Type	Reset	Description
VAL	[10:0]	RW	0x00	Boundary Scan per-bit value.

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_0

Address: 0x00140258

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_1

Address: 0x0014025C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_2

Address: 0x00140260

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_3

Address: 0x00140264

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_4

Address: 0x00140268

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_5

Address: 0x0014026C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_6

Address: 0x00140270

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_7

Address: 0x00140274

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_8

Address: 0x00140278

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_9

Address: 0x0014027C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M0_CFG_10

Address: 0x00140280

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_0

Address: 0x00140284

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_1

Address: 0x00140288

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_2

Address: 0x0014028C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_3

Address: 0x00140290

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_4

Address: 0x00140294

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_5

Address: 0x00140298

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

Registers

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_6

Address: 0x0014029C

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_7

Address: 0x001402A0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_8

Address: 0x001402A4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_9

Address: 0x001402A8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_ANA_M1_CFG_10

Address: 0x001402AC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_0

Address: 0x001402B0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_1

Address: 0x001402B4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_2

Address: 0x001402B8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_3

Address: 0x001402BC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_4

Address: 0x001402C0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_5

Address: 0x001402C4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_6

Address: 0x001402C8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_7

Address: 0x001402CC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_8

Address: 0x001402D0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_9

Address: 0x001402D4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M0_CFG_10

Address: 0x001402D8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_0

Address: 0x001402DC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_1

Address: 0x001402E0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_2

Address: 0x001402E4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_3

Address: 0x001402E8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_4

Address: 0x001402EC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_5

Address: 0x001402F0

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_6

Address: 0x001402F4

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_7

Address: 0x001402F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

Registers

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_8

Address: 0x001402FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_9

Address: 0x00140300

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_EGRESS_DIG_M1_CFG_10

Address: 0x00140304

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3:ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQ_TX_ODR_PI_M0_R0_CFG

Address: 0x00140308

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_ODR_PI_M0_R1_CFG

Address: 0x0014030C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_ODR_PI_M1_R0_CFG

Address: 0x00140310

Registers

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_ODR_PI_M1_R1_CFG

Address: 0x00140314

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00140318

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_QDR_PI_0_M0_R1_CFG

Address: 0x0014031C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00140320

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH1_CA__DQ_TX_QDR_PI_0_M1_R1_CFG

Address: 0x00140324

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_QDR_PI_1_M0_R0_CFG

Address: 0x00140328

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_QDR_PI_1_M0_R1_CFG

Address: 0x0014032C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_QDR_PI_1_M1_R0_CFG

Address: 0x00140330

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_QDR_PI_1_M1_R1_CFG

Address: 0x00140334

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_DDR_PI_0_M0_R0_CFG

Address: 0x00140338

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_DDR_PI_0_M0_R1_CFG

Address: 0x0014033C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_DDR_PI_0_M1_R0_CFG

Address: 0x00140340

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_DDR_PI_0_M1_R1_CFG

Address: 0x00140344

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_CA__DQ_TX_DDR_PI_1_M0_R0_CFG

Address: 0x00140348

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_DDR_PI_1_M0_R1_CFG

Address: 0x0014034C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_DDR_PI_1_M1_R0_CFG

Address: 0x00140350

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_DDR_PI_1_M1_R1_CFG

Address: 0x00140354

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_PI_RT_M0_R0_CFG

Address: 0x00140358

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_PI_RT_M0_R1_CFG

Address: 0x0014035C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_PI_RT_M1_R0_CFG

Address: 0x00140360

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_PI_RT_M1_R1_CFG

Address: 0x00140364

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQ_TX_RT_M0_R0_CFG

Address: 0x00140368

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH1_CA__DQ_TX_RT_M0_R1_CFG

Address: 0x0014036C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH1_CA__DQ_TX_RT_M1_R0_CFG

Address: 0x00140370

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH1_CA__DQ_TX_RT_M1_R1_CFG

Address: 0x00140374

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[10:0]	RW	0x000	Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_RO_CFG_0

Address: 0x00140378

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_RO_CFG_1

Address: 0x0014037C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_2

Address: 0x00140380

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_3

Address: 0x00140384

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_4

Address: 0x00140388

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_5

Address: 0x0014038C

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_6

Address: 0x00140390

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_7

Address: 0x00140394

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_8

Address: 0x00140398

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_9

Address: 0x0014039C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R0_CFG_10

Address: 0x001403A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_0

Address: 0x001403A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_1

Address: 0x001403A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_2

Address: 0x001403AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_3

Address: 0x001403B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_4

Address: 0x001403B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_5

Address: 0x001403B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_6

Address: 0x001403BC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_7

Address: 0x001403C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_8

Address: 0x001403C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_9

Address: 0x001403C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_SDR_M0_R1_CFG_10

Address: 0x001403CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_0

Address: 0x001403D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_1

Address: 0x001403D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_2

Address: 0x001403D8

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_3

Address: 0x001403DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_4

Address: 0x001403E0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_5

Address: 0x001403E4

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_6

Address: 0x001403E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_7

Address: 0x001403EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_8

Address: 0x001403F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_9

Address: 0x001403F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R0_CFG_10

Address: 0x001403F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_0

Address: 0x001403FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_1

Address: 0x00140400

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_2

Address: 0x00140404

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_3

Address: 0x00140408

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.

Registers

PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_4

Address: 0x0014040C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_5

Address: 0x00140410

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_6

Address: 0x00140414

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_7

Address: 0x00140418

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_8

Address: 0x0014041C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_9

Address: 0x00140420

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_M1_R1_CFG_10

Address: 0x00140424

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00140428

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_1

Address: 0x0014042C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_2

Address: 0x00140430

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_3

Address: 0x00140434

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_4

Address: 0x00140438

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_5

Address: 0x0014043C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_6

Address: 0x00140440

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_7

Address: 0x00140444

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_8

Address: 0x00140448

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_9

Address: 0x0014044C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R0_CFG_10

Address: 0x00140450

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x00140454

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_1

Address: 0x00140458

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_2

Address: 0x0014045C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_3

Address: 0x00140460

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_4

Address: 0x00140464

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_5

Address: 0x00140468

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_6

Address: 0x0014046C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_7

Address: 0x00140470

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_8

Address: 0x00140474

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_9

Address: 0x00140478

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M0_R1_CFG_10

Address: 0x0014047C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x00140480

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_1

Address: 0x00140484

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_2

Address: 0x00140488

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_3

Address: 0x0014048C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_4

Address: 0x00140490

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_5

Address: 0x00140494

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.

Registers

X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_6

Address: 0x00140498

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_7

Address: 0x0014049C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_8

Address: 0x001404A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.

Registers

X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_9

Address: 0x001404A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R0_CFG_10

Address: 0x001404A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x001404AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_1

Address: 0x001404B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_2

Address: 0x001404B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_3

Address: 0x001404B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_4

Address: 0x001404BC

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_5

Address: 0x001404C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_6

Address: 0x001404C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_7

Address: 0x001404C8

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_8

Address: 0x001404CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_9

Address: 0x001404D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_X_SEL_M1_R1_CFG_10

Address: 0x001404D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_0

Address: 0x001404D8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_1

Address: 0x001404DC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_2

Address: 0x001404E0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_3

Address: 0x001404E4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_4

Address: 0x001404E8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_5

Address: 0x001404EC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_6

Address: 0x001404F0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_7

Address: 0x001404F4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R0_CFG_8

Address: 0x001404F8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_CA__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_9

Address: 0x001404FC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DL_Y_M0_R0_CFG_10

Address: 0x00140500

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_0

Address: 0x00140504

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DL_Y_M0_R1_CFG_1

Address: 0x00140508

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_2

Address: 0x0014050C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_3

Address: 0x00140510

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_4

Address: 0x00140514

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_5

Address: 0x00140518

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_6

Address: 0x0014051C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_7

Address: 0x00140520

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_8

Address: 0x00140524

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_9

Address: 0x00140528

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M0_R1_CFG_10

Address: 0x0014052C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00140530

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_1

Address: 0x00140534

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_2

Address: 0x00140538

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_3

Address: 0x0014053C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_4

Address: 0x00140540

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_5

Address: 0x00140544

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_6

Address: 0x00140548

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_7

Address: 0x0014054C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_8

Address: 0x00140550

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_9

Address: 0x00140554

Registers

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R0_CFG_10

Address: 0x00140558

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x0014055C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_1

Address: 0x00140560

Description:

Name	Index	Type	Reset	Description

Registers

DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_2

Address: 0x00140564

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_3

Address: 0x00140568

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_4

Address: 0x0014056C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.

Registers

DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_5

Address: 0x00140570

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_6

Address: 0x00140574

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_7

Address: 0x00140578

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.

Registers

DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_8

Address: 0x0014057C

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_9

Address: 0x00140580

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_SDR_FC_DLY_M1_R1_CFG_10

Address: 0x00140584

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.

Registers

DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_0

Address: 0x00140588

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_1

Address: 0x0014058C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_2

Address: 0x00140590

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_3

Address: 0x00140594

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_4

Address: 0x00140598

Registers

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_5

Address: 0x0014059C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_6

Address: 0x001405A0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_7

Address: 0x001405A4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_8

Address: 0x001405A8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
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WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_9

Address: 0x001405AC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R0_CFG_10

Address: 0x001405B0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_0

Address: 0x001405B4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_1

Address: 0x001405B8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_2

Address: 0x001405BC

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_3

Address: 0x001405C0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_4

Address: 0x001405C4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_5

Address: 0x001405C8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_6

Address: 0x001405CC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_7

Address: 0x001405D0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_8

Address: 0x001405D4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_9

Address: 0x001405D8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M0_R1_CFG_10

Address: 0x001405DC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_0

Address: 0x001405E0

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_1

Address: 0x001405E4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_2

Address: 0x001405E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_3

Address: 0x001405EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_4

Address: 0x001405F0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_5

Address: 0x001405F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_6

Address: 0x001405F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_7

Address: 0x001405FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_8

Address: 0x00140600

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_9

Address: 0x00140604

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R0_CFG_10

Address: 0x00140608

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_0

Address: 0x0014060C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_1

Address: 0x00140610

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_2

Address: 0x00140614

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_3

Address: 0x00140618

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_4

Address: 0x0014061C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_5

Address: 0x00140620

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_6

Address: 0x00140624

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_7

Address: 0x00140628

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_8

Address: 0x0014062C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_9

Address: 0x00140630

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_M1_R1_CFG_10

Address: 0x00140634

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00140638

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_1

Address: 0x0014063C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_2

Address: 0x00140640

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_3

Address: 0x00140644

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_4

Address: 0x00140648

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_5

Address: 0x0014064C

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_6

Address: 0x00140650

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_7

Address: 0x00140654

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_8

Address: 0x00140658

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_9

Address: 0x0014065C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R0_CFG_10

Address: 0x00140660

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00140664

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_1

Address: 0x00140668

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_2

Address: 0x0014066C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_3

Address: 0x00140670

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_4

Address: 0x00140674

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_5

Address: 0x00140678

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_6

Address: 0x0014067C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_7

Address: 0x00140680

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_8

Address: 0x00140684

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_9

Address: 0x00140688

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M0_R1_CFG_10

Address: 0x0014068C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00140690

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_1

Address: 0x00140694

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_2

Address: 0x00140698

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_3

Address: 0x0014069C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_4

Address: 0x001406A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_5

Address: 0x001406A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_6

Address: 0x001406A8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_7

Address: 0x001406AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_8

Address: 0x001406B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_9

Address: 0x001406B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R0_CFG_10

Address: 0x001406B8

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x001406BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_1

Address: 0x001406C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_2

Address: 0x001406C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_3

Address: 0x001406C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_4

Address: 0x001406CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_5

Address: 0x001406D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_6

Address: 0x001406D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_7

Address: 0x001406D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_8

Address: 0x001406DC

Description:

Name	Index	Type	Reset	Description

Registers

X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_9

Address: 0x001406E0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_DDR_X_SEL_M1_R1_CFG_10

Address: 0x001406E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_0

Address: 0x001406E8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_1

Address: 0x001406EC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_2

Address: 0x001406F0

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_3

Address: 0x001406F4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_4

Address: 0x001406F8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_5

Address: 0x001406FC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_6

Address: 0x00140700

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_7

Address: 0x00140704

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_8

Registers

Address: 0x00140708

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_9

Address: 0x0014070C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R0_CFG_10

Address: 0x00140710

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_0

Address: 0x00140714

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_1

Address: 0x00140718

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_2

Address: 0x0014071C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_3

Address: 0x00140720

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_4

Address: 0x00140724

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_5

Address: 0x00140728

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_6

Address: 0x0014072C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_7

Address: 0x00140730

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_8

Address: 0x00140734

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_9

Address: 0x00140738

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M0_R1_CFG_10

Address: 0x0014073C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_0

Address: 0x00140740

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_1

Address: 0x00140744

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_2

Address: 0x00140748

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_3

Address: 0x0014074C

Description:

Registers

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_4

Address: 0x00140750

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_5

Address: 0x00140754

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_6

Address: 0x00140758

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_7

Address: 0x0014075C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_8

Address: 0x00140760

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_9

Registers

Address: 0x00140764

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R0_CFG_10

Address: 0x00140768

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_0

Address: 0x0014076C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_1

Address: 0x00140770

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_2

Address: 0x00140774

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_3

Address: 0x00140778

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

Registers

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_4

Address: 0x0014077C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_5

Address: 0x00140780

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_6

Address: 0x00140784

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_7

Address: 0x00140788

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_8

Address: 0x0014078C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_9

Address: 0x00140790

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.

Registers

PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
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WAV_CH1_CA__DQ_TX_QDR_M1_R1_CFG_10

Address: 0x00140794

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00140798

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_1

Address: 0x0014079C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_2

Address: 0x001407A0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_3

Address: 0x001407A4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_4

Address: 0x001407A8

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_5

Address: 0x001407AC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_6

Address: 0x001407B0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_7

Address: 0x001407B4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_8

Address: 0x001407B8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_9

Address: 0x001407BC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R0_CFG_10

Registers

Address: 0x001407C0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x001407C4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_1

Address: 0x001407C8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_2

Address: 0x001407CC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_3

Address: 0x001407D0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_4

Address: 0x001407D4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_5

Address: 0x001407D8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_6

Address: 0x001407DC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_7

Address: 0x001407E0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_8

Address: 0x001407E4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_9

Address: 0x001407E8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M0_R1_CFG_10

Address: 0x001407EC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.

Registers

X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.
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WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x001407F0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_1

Address: 0x001407F4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_2

Address: 0x001407F8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_3

Address: 0x001407FC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_4

Address: 0x00140800

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_5

Address: 0x00140804

Description:

Registers

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_6

Address: 0x00140808

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_7

Address: 0x0014080C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_8

Address: 0x00140810

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_9

Address: 0x00140814

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R0_CFG_10

Address: 0x00140818

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_0

Registers

Address: 0x0014081C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_1

Address: 0x00140820

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_2

Address: 0x00140824

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_3

Address: 0x00140828

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_4

Address: 0x0014082C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_5

Address: 0x00140830

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

Registers

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_6

Address: 0x00140834

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_7

Address: 0x00140838

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_8

Address: 0x0014083C

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_9

Address: 0x00140840

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_QDR_X_SEL_M1_R1_CFG_10

Address: 0x00140844

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_0

Address: 0x00140848

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_1

Address: 0x0014084C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_2

Address: 0x00140850

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_3

Address: 0x00140854

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_4

Address: 0x00140858

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_5

Address: 0x0014085C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_6

Address: 0x00140860

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_7

Address: 0x00140864

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_8

Address: 0x00140868

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_9

Address: 0x0014086C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R0_CFG_10

Address: 0x00140870

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_0

Address: 0x00140874

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_1

Address: 0x00140878

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_2

Address: 0x0014087C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_3

Address: 0x00140880

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_4

Address: 0x00140884

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_5

Address: 0x00140888

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_6

Address: 0x0014088C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_7

Address: 0x00140890

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_8

Address: 0x00140894

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_9

Address: 0x00140898

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M0_R1_CFG_10

Address: 0x0014089C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_0

Address: 0x001408A0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_1

Address: 0x001408A4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_2

Address: 0x001408A8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_3

Address: 0x001408AC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_4

Address: 0x001408B0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_5

Address: 0x001408B4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_6

Address: 0x001408B8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_7

Address: 0x001408BC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_8

Address: 0x001408C0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_9

Address: 0x001408C4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R0_CFG_10

Address: 0x001408C8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_0

Address: 0x001408CC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_1

Address: 0x001408D0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_2

Address: 0x001408D4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_3

Address: 0x001408D8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_4

Address: 0x001408DC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_5

Address: 0x001408E0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_6

Address: 0x001408E4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_7

Address: 0x001408E8

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_8

Address: 0x001408EC

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_9

Address: 0x001408F0

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_LPDE_M1_R1_CFG_10

Address: 0x001408F4

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_0

Address: 0x001408F8

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_1

Address: 0x001408FC

Description:

Registers

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_2

Address: 0x00140900

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_3

Address: 0x00140904

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_4

Address: 0x00140908

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH1_CA__DQ_TX_IO_M0_CFG_5

Address: 0x0014090C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_6

Address: 0x00140910

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_7

Address: 0x00140914

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_8

Address: 0x00140918

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.

Registers

SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_9

Address: 0x0014091C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M0_CFG_10

Address: 0x00140920

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_0

Address: 0x00140924

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_1

Address: 0x00140928

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.

Registers

OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_2

Address: 0x0014092C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_3

Address: 0x00140930

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_4

Address: 0x00140934

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_5

Address: 0x00140938

Registers

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_6

Address: 0x0014093C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_7

Address: 0x00140940

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_8

Address: 0x00140944

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

Registers

WAV_CH1_CA__DQ_TX_IO_M1_CFG_9

Address: 0x00140948

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQ_TX_IO_M1_CFG_10

Address: 0x0014094C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x0	Override select.
OVRD_VAL	[3]	RW	0x0	Override value.
RESERVED	[4]	RW	0x0	Reserved.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQS_RX_M0_CFG

Address: 0x00140950

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH1_CA__DQS_RX_M1_CFG

Address: 0x00140954

Description:

Name	Index	Type	Reset	Description
FGB_MODE	[7:4]	RW	0x7	FIFO Gearbox Mode (see documentation).
PRE_FILTER_SEL	[13:12]	RW	0x0	Preamble filter select - 0: None, 1:One toggle, 2:Two toggle.
RGB_MODE	[2:0]	RW	0x4	Datapath Gearbox Mode (see documentation).
WCK_MODE	[8]	RW	0x0	WCK Clocking mode - 0: RDQS, 1: WCK Loopback.

WAV_CH1_CA__DQS_RX_BSCAN_STA

Registers

Address: 0x00140958

Description:

Name	Index	Type	Reset	Description
VAL	[1:0]	R	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH1_CA__DQS_RX_SDR_LPDE_M0_R0_CFG

Address: 0x0014095C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_RX_SDR_LPDE_M0_R1_CFG

Address: 0x00140960

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_RX_SDR_LPDE_M1_R0_CFG

Address: 0x00140964

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_RX_SDR_LPDE_M1_R1_CFG

Address: 0x00140968

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_RX_REN_PI_M0_R0_CFG

Address: 0x0014096C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_REN_PI_M0_R1_CFG

Address: 0x00140970

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_REN_PI_M1_R0_CFG

Address: 0x00140974

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_REN_PI_M1_R1_CFG

Address: 0x00140978

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RCS_PI_M0_R0_CFG

Address: 0x0014097C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_CA__DQS_RX_RCS_PI_M0_R1_CFG

Address: 0x00140980

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RCS_PI_M1_R0_CFG

Address: 0x00140984

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RCS_PI_M1_R1_CFG

Address: 0x00140988

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RDQS_PI_0_M0_R0_CFG

Address: 0x0014098C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RDQS_PI_0_M0_R1_CFG

Address: 0x00140990

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RDQS_PI_0_M1_R0_CFG

Address: 0x00140994

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RDQS_PI_0_M1_R1_CFG

Address: 0x00140998

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RDQS_PI_1_M0_R0_CFG

Address: 0x0014099C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RDQS_PI_1_M0_R1_CFG

Address: 0x001409A0

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_CA__DQS_RX_RDQS_PI_1_M1_R0_CFG

Address: 0x001409A4

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_RDQS_PI_1_M1_R1_CFG

Address: 0x001409A8

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_RX_PI_STA

Address: 0x001409AC

Description:

Name	Index	Type	Reset	Description
RCS_PI_PHASE	[1]	R	0x0	Indicates the phase of RE_PI output clock wrt RCS.
REN_PI_PHASE	[0]	R	0x0	Indicates the phase of RE_PI output clock wrt REN.

WAV_CH1_CA__DQS_RX_IO_M0_R0_CFG_0

Address: 0x001409B0

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_CA__DQS_RX_IO_M0_R1_CFG_0

Address: 0x001409B4

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_CA__DQS_RX_IO_M1_R0_CFG_0

Registers

Address: 0x001409B8

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_CA__DQS_RX_IO_M1_R1_CFG_0

Address: 0x001409BC

Description:

Name	Index	Type	Reset	Description
DLY_CTRL_C	[7:0]	RW	0x0	Binary delay control.
DLY_CTRL_T	[15:8]	RW	0x0	Binary delay control.

WAV_CH1_CA__DQS_RX_IO_CMN_M0_R0_CFG

Address: 0x001409C0

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for edge detect EN and IE.

WAV_CH1_CA__DQS_RX_IO_CMN_M0_R1_CFG

Address: 0x001409C4

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).

Registers

SW_OVR	[23]	RW	0x0	Software override for RE and IE.
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WAV_CH1_CA__DQS_RX_IO_CMN_M1_R0_CFG

Address: 0x001409C8

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_CA__DQS_RX_IO_CMN_M1_R1_CFG

Address: 0x001409CC

Description:

Name	Index	Type	Reset	Description
CAL_N_C	[11:8]	RW	0x7	Offset correction magnitude.
CAL_N_T	[15:12]	RW	0x7	Offset correction magnitude.
CAL_P_C	[3:0]	RW	0x7	Offset correction magnitude.
CAL_P_T	[7:4]	RW	0x7	Offset correction magnitude.
DCPATH_EN	[19]	RW	0x1	DC mode, active high. Unterminated clocking (<1GHz).
EN	[20]	RW	0x0	Enable. When deasserted then dqs_t=0 and dqs_c=1.
FB_EN	[18:16]	RW	0x2	Enable the feedback resistors based on frequency.
RXCAL_EN	[21]	RW	0x0	Enables the AC receiver offset correction.
SE_MODE	[22]	RW	0x1	Single-ended mode. Unterminated clocking (<1GHz).
SW_OVR	[23]	RW	0x0	Software override for RE and IE.

WAV_CH1_CA__DQS_RX_IO_STA

Address: 0x001409D0

Description:

Name	Index	Type	Reset	Description
CORE_IG	[31:0]	R	0x0	Core ingress data.

WAV_CH1_CA__DQS_RX_SA_M0_R0_CFG_0

Address: 0x001409D4

Description:

Registers

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQS_RX_SA_M0_R1_CFG_0

Address: 0x001409D8

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQS_RX_SA_M1_R0_CFG_0

Address: 0x001409DC

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.
CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQS_RX_SA_M1_R1_CFG_0

Address: 0x001409E0

Description:

Name	Index	Type	Reset	Description
CAL_CODE_0	[3:0]	RW	0x0	Calibration code.

Registers

CAL_CODE_180	[11:8]	RW	0x0	Calibration code.
CAL_CODE_270	[15:12]	RW	0x0	Calibration code.
CAL_CODE_90	[7:4]	RW	0x0	Calibration code.
CAL_DIR_0	[16]	RW	0x0	Calibration direction.
CAL_DIR_180	[18]	RW	0x0	Calibration direction.
CAL_DIR_270	[19]	RW	0x0	Calibration direction.
CAL_DIR_90	[17]	RW	0x0	Calibration direction.

WAV_CH1_CA__DQS_RX_SA_CMN_CFG

Address: 0x001409E4

Description:

Name	Index	Type	Reset	Description
CAL_EN_0_180	[1]	RW	0x0	Calibration enable.
CAL_EN_90_270	[3]	RW	0x0	Calibration enable.
OVR_EN_0_180	[0]	RW	0x1	Software override value of SA_Enable.
OVR_EN_90_270	[2]	RW	0x1	Software override value of SA_Enable.
SW_OVR	[4]	RW	0x0	Software override for SA enable.

WAV_CH1_CA__DQS_TX_M0_CFG

Address: 0x001409E8

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH1_CA__DQS_TX_M1_CFG

Address: 0x001409EC

Description:

Name	Index	Type	Reset	Description
CK2WCK_RATIO	[9:8]	RW	0x0	CK2WCK Ratio. Use in CA only. (see documentation).
TGB_MODE	[2:0]	RW	0x7	Datapath Gearbox mode (see documentation).
WGB_MODE	[7:4]	RW	0x8	Write Gearbox Mode (see documentation).

WAV_CH1_CA__DQS_TX_BSCAN_CTRL_CFG

Address: 0x001409F0

Description:

Name	Index	Type	Reset	Description
IE	[0]	RW	0x0	Boundary Scan IE.
OE	[1]	RW	0x0	Boundary Scan OE.

Registers

WAV_CH1_CA__DQS_TX_BSCAN_CFG

Address: 0x001409F4

Description:

Name	Index	Type	Reset	Description
VAL	[1:0]	RW	0x000	Boundary Scan per-bit value 2x for *_t and *_c.

WAV_CH1_CA__DQS_TX_EGRESS_ANA_M0_CFG_0

Address: 0x001409F8

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQS_TX_EGRESS_ANA_M1_CFG_0

Address: 0x001409FC

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[5:0]	RW	0x01	Egress mode (one-hot) - 0: BYPASS, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1

WAV_CH1_CA__DQS_TX_EGRESS_DIG_M0_CFG_0

Address: 0x00140A00

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQS_TX_EGRESS_DIG_M1_CFG_0

Address: 0x00140A04

Description:

Name	Index	Type	Reset	Description
EGRESS_MODE	[6:0]	RW	0x02	Egress mode (one-hot) - 0:SDR, 1:DDR_2to1, 2:QDR_2to1, 3: ODR_2to1, 4:QDR_4to1, 5:ODR_4to1, 6:BSCAN

WAV_CH1_CA__DQS_TX_ODR_PI_M0_R0_CFG

Address: 0x00140A08

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.

Registers

XCPL	[13:10]	RW	0x0	Analog - TBD.
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WAV_CH1_CA__DQS_TX_ODR_PI_M0_R1_CFG

Address: 0x00140A0C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_ODR_PI_M1_R0_CFG

Address: 0x00140A10

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_ODR_PI_M1_R1_CFG

Address: 0x00140A14

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_QDR_PI_0_M0_R0_CFG

Address: 0x00140A18

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_QDR_PI_0_M0_R1_CFG

Address: 0x00140A1C

Description:

Registers

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_QDR_PI_0_M1_R0_CFG

Address: 0x00140A20

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_QDR_PI_0_M1_R1_CFG

Address: 0x00140A24

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_QDR_PI_1_M0_R0_CFG

Address: 0x00140A28

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_QDR_PI_1_M0_R1_CFG

Address: 0x00140A2C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_CA__DQS_TX_QDR_PI_1_M1_R0_CFG

Address: 0x00140A30

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_QDR_PI_1_M1_R1_CFG

Address: 0x00140A34

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DDR_PI_0_M0_R0_CFG

Address: 0x00140A38

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DDR_PI_0_M0_R1_CFG

Address: 0x00140A3C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DDR_PI_0_M1_R0_CFG

Address: 0x00140A40

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DDR_PI_0_M1_R1_CFG

Address: 0x00140A44

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DDR_PI_1_M0_R0_CFG

Address: 0x00140A48

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DDR_PI_1_M0_R1_CFG

Address: 0x00140A4C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DDR_PI_1_M1_R0_CFG

Address: 0x00140A50

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_CA__DQS_TX_DDR_PI_1_M1_R1_CFG

Address: 0x00140A54

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_PI_RT_M0_R0_CFG

Address: 0x00140A58

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_PI_RT_M0_R1_CFG

Address: 0x00140A5C

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_PI_RT_M1_R0_CFG

Address: 0x00140A60

Description:

Name	Index	Type	Reset	Description
CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_PI_RT_M1_R1_CFG

Address: 0x00140A64

Description:

Name	Index	Type	Reset	Description

Registers

CODE	[5:0]	RW	0x00	6-bit code that will control 1/4th of the interpolator.
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_SDR_PI_M0_R0_CFG

Address: 0x00140A68

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_SDR_PI_M0_R1_CFG

Address: 0x00140A6C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_SDR_PI_M1_R0_CFG

Address: 0x00140A70

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_SDR_PI_M1_R1_CFG

Address: 0x00140A74

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

Registers

WAV_CH1_CA__DQS_TX_DFI_PI_M0_R0_CFG

Address: 0x00140A78

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DFI_PI_M0_R1_CFG

Address: 0x00140A7C

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DFI_PI_M1_R0_CFG

Address: 0x00140A80

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_DFI_PI_M1_R1_CFG

Address: 0x00140A84

Description:

Name	Index	Type	Reset	Description
EN	[14]	RW	0x0	Enable.
GEAR	[9:6]	RW	0x1	Performance calibration.
RSVD	[5:0]	RW	0x00	Reserved field added in place of CODE field in other Pls.
XCPL	[13:10]	RW	0x0	Analog - TBD.

WAV_CH1_CA__DQS_TX_RT_M0_R0_CFG

Address: 0x00140A88

Description:

Name	Index	Type	Reset	Description

Registers

PIPE_EN	[0:0]	RW	0x000	Pipeline enable.
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WAV_CH1_CA__DQS_TX_RT_M0_R1_CFG

Address: 0x00140A8C

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[0:0]	RW	0x000	Pipeline enable.

WAV_CH1_CA__DQS_TX_RT_M1_R0_CFG

Address: 0x00140A90

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[0:0]	RW	0x000	Pipeline enable.

WAV_CH1_CA__DQS_TX_RT_M1_R1_CFG

Address: 0x00140A94

Description:

Name	Index	Type	Reset	Description
PIPE_EN	[0:0]	RW	0x000	Pipeline enable.

WAV_CH1_CA__DQS_TX_SDR_M0_R0_CFG_0

Address: 0x00140A98

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQS_TX_SDR_M0_R1_CFG_0

Address: 0x00140A9C

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.

Registers

PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQS_TX_SDR_M1_R0_CFG_0

Address: 0x00140AA0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQS_TX_SDR_M1_R1_CFG_0

Address: 0x00140AA4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.
PIPE_EN_P4	[4]	RW	0x0	Phase 4 Pipeline enable.
PIPE_EN_P5	[5]	RW	0x0	Phase 5 Pipeline enable.
PIPE_EN_P6	[6]	RW	0x0	Phase 6 Pipeline enable.
PIPE_EN_P7	[7]	RW	0x0	Phase 7 Pipeline enable.

WAV_CH1_CA__DQS_TX_SDR_X_SEL_M0_R0_CFG_0

Address: 0x00140AA8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.

Registers

X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQS_TX_SDR_X_SEL_M0_R1_CFG_0

Address: 0x00140AAC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQS_TX_SDR_X_SEL_M1_R0_CFG_0

Address: 0x00140AB0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.
X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.

WAV_CH1_CA__DQS_TX_SDR_X_SEL_M1_R1_CFG_0

Address: 0x00140AB4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[2:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[6:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[10:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[14:12]	RW	0x0	Phase 3 X-ing select.
X_SEL_P4	[18:16]	RW	0x0	Phase 4 X-ing select.
X_SEL_P5	[22:20]	RW	0x0	Phase 5 X-ing select.
X_SEL_P6	[26:24]	RW	0x0	Phase 6 X-ing select.

Registers

X_SEL_P7	[30:28]	RW	0x0	Phase 7 X-ing select.
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WAV_CH1_CA__DQS_TX_SDR_FC_DLY_M0_R0_CFG_0

Address: 0x00140AB8

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQS_TX_SDR_FC_DLY_M0_R1_CFG_0

Address: 0x00140ABC

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQS_TX_SDR_FC_DLY_M1_R0_CFG_0

Address: 0x00140AC0

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

Registers

WAV_CH1_CA__DQS_TX_SDR_FC_DLY_M1_R1_CFG_0

Address: 0x00140AC4

Description:

Name	Index	Type	Reset	Description
DLY_P0	[1:0]	RW	0x0	Phase 0 Full Cycle Delay.
DLY_P1	[5:4]	RW	0x0	Phase 1 Full Cycle Delay.
DLY_P2	[9:8]	RW	0x0	Phase 2 Full Cycle Delay.
DLY_P3	[13:12]	RW	0x0	Phase 3 Full Cycle Delay.
DLY_P4	[17:16]	RW	0x0	Phase 4 Full Cycle Delay.
DLY_P5	[21:20]	RW	0x0	Phase 5 Full Cycle Delay.
DLY_P6	[25:24]	RW	0x0	Phase 6 Full Cycle Delay.
DLY_P7	[29:28]	RW	0x0	Phase 7 Full Cycle Delay.

WAV_CH1_CA__DQS_TX_DDR_M0_R0_CFG_0

Address: 0x00140AC8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQS_TX_DDR_M0_R1_CFG_0

Address: 0x00140ACC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQS_TX_DDR_M1_R0_CFG_0

Address: 0x00140AD0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQS_TX_DDR_M1_R1_CFG_0

Registers

Address: 0x00140AD4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.
PIPE_EN_P2	[2]	RW	0x0	Phase 2 Pipeline enable.
PIPE_EN_P3	[3]	RW	0x0	Phase 3 Pipeline enable.

WAV_CH1_CA__DQS_TX_DDR_X_SEL_M0_R0_CFG_0

Address: 0x00140AD8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQS_TX_DDR_X_SEL_M0_R1_CFG_0

Address: 0x00140ADC

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQS_TX_DDR_X_SEL_M1_R0_CFG_0

Address: 0x00140AE0

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.
X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQS_TX_DDR_X_SEL_M1_R1_CFG_0

Address: 0x00140AE4

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[1:0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[5:4]	RW	0x0	Phase 1 X-ing select.

Registers

X_SEL_P2	[9:8]	RW	0x0	Phase 2 X-ing select.
X_SEL_P3	[13:12]	RW	0x0	Phase 3 X-ing select.

WAV_CH1_CA__DQS_TX_QDR_M0_R0_CFG_0

Address: 0x00140AE8

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQS_TX_QDR_M0_R1_CFG_0

Address: 0x00140AEC

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQS_TX_QDR_M1_R0_CFG_0

Address: 0x00140AF0

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQS_TX_QDR_M1_R1_CFG_0

Address: 0x00140AF4

Description:

Name	Index	Type	Reset	Description
PIPE_EN_P0	[0]	RW	0x0	Phase 0 Pipeline enable.
PIPE_EN_P1	[1]	RW	0x0	Phase 1 Pipeline enable.

WAV_CH1_CA__DQS_TX_QDR_X_SEL_M0_R0_CFG_0

Address: 0x00140AF8

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQS_TX_QDR_X_SEL_M0_R1_CFG_0

Address: 0x00140AFC

Registers

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQS_TX_QDR_X_SEL_M1_R0_CFG_0

Address: 0x00140B00

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQS_TX_QDR_X_SEL_M1_R1_CFG_0

Address: 0x00140B04

Description:

Name	Index	Type	Reset	Description
X_SEL_P0	[0]	RW	0x0	Phase 0 X-ing select.
X_SEL_P1	[4]	RW	0x0	Phase 1 X-ing select.

WAV_CH1_CA__DQS_TX_LPDE_M0_R0_CFG_0

Address: 0x00140B08

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_TX_LPDE_M0_R1_CFG_0

Address: 0x00140B0C

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_TX_LPDE_M1_R0_CFG_0

Address: 0x00140B10

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.

Registers

EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_TX_LPDE_M1_R1_CFG_0

Address: 0x00140B14

Description:

Name	Index	Type	Reset	Description
CTRL_BIN	[5:0]	RW	0x0	Programmable binary delay.
EN	[8]	RW	0x1	Enable.
GEAR	[7:6]	RW	0x0	Performance calibration.

WAV_CH1_CA__DQS_TX_IO_M0_CFG_0

Address: 0x00140B18

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQS_TX_IO_M1_CFG_0

Address: 0x00140B1C

Description:

Name	Index	Type	Reset	Description
OVRD_SEL	[2:0]	RW	0x1	Override select.
OVRD_VAL_C	[3]	RW	0x0	Override value.
OVRD_VAL_T	[4]	RW	0x0	Override value.
RX_IMPD	[11:9]	RW	0x0	RX impedance code.
SW_OVR	[5]	RW	0x0	Software override enable for OE.
TX_IMPD	[8:6]	RW	0x1	TX impedance code.

WAV_CH1_CA__DQS_TX_IO_CMN_M0_R0_CFG

Address: 0x00140B20

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.

Registers

SE_MODE	[13]	RW	0x0	Single-ended mode.
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WAV_CH1_CA__DQS_TX_IO_CMN_M0_R1_CFG

Address: 0x00140B24

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_CA__DQS_TX_IO_CMN_M1_R0_CFG

Address: 0x00140B28

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

WAV_CH1_CA__DQS_TX_IO_CMN_M1_R1_CFG

Address: 0x00140B2C

Description:

Name	Index	Type	Reset	Description
BS_EN	[11]	RW	0x0	Boundary scan mode.
LPBK_EN	[12]	RW	0x0	Loopback enable.
NCAL	[4:0]	RW	0x01	N Calibration code. Value must be > 1 for TX driver enable.
PCAL	[10:5]	RW	0x00	P Calibration code.
SE_MODE	[13]	RW	0x0	Single-ended mode.

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How to request help?

Indices and tables

- genindex
- modindex
- search