



ECE 552 HWS

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state output
descriptions

EN: enables cache
comp: enables compare tags
c_write: write to cache
valid-in: valid input to cache
mem_wrt: write to mem
mem_rd: read from mem
mem_cache_wrt: write to cache data from mem
done: operation is complete or ready for next operation

Problem 1: Direct Mapped Cache Finite State Machine

fractional cistals description :

write: when there is a load instruction
 - start interpretation?

write when there is a store instruction

hit : Cache hit

valid : Cache line is valid

dirty: cache line is dirty

The access update to cache is done

rd-done: reading memory, writing to memory is done

ur-done: writing

Page 5: Does nothing seem right?