



ECE 552 HWS

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State outputs descriptions

EN: enables cache
comp: enables compare tags
C-write: write to cache
valid-in: valid input to cache
mem-wr: write to mem
mem-rd: read from mem
mem-cache-wr: write to cache data from mem
done: operation is complete or ready for next operation

Problem 1: Direct Mapped Cache Finite State Machine

transition signals description:

write: when there is a load instruction

write: when there is a store instruction

hit: Cache hit

valid: Cache line is valid

dirty: Cache line is dirty

rd-done: reading memory, writing to cache is done

wr-done: writing to memory is done

wr-done-c: done writing to cache

rd-done-c: done reading from cache