Terawins, Inc.

April, 02 ,2015

T582DB System CLK Reference Table

Revision Note

Revisions	Content	Date
1.00	First release	*Apr, 02, 2015*

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1 Change Log

Revisions	Page	Description of changes

2 T582DB System CLK Reference Table

Panel Model	Panel Size & Resolution	DCLK Typ.~Max. Range	Panel Type
MEX040HS	4 inch (480x272)	9M~12M	TTL RGB
MEX043CM	4.3 inch (480x272)	9M~15M	TTL RGB
A036QN01	3.6 inch (960x240)	19.4M~25M	Serial RGB
ZJ050NA-08C	5 inch (600x480)	25.2M~34.2M	TTL RGB
AT070TN92	7 inch (800x480)	33.3M~46.8M	TTL RGB
KD101N7	10 inch (1024x600)	52M~67M	TTL RGB

DCLK Range	Frequency(MHz)			PLL Setting Register		Page0 Register			
	DCLK	SD_CLK (≒50)	CPU_CLK (108~120)	B7C00104	B7C00110	C8h	C9h	CAh	CBh
9MHz ~ 15MHz	9	43.2	108	77541101	F1	9E	00	00	12
	9.98	47.93	119.81	77541101	A29	C5	02	00	12
	10.8	43.2	108	77441101	571	AE	01	00	12
	11.03	44.1	110.25	77441101	579	AF	01	00	12
	11.48	45.9	114.75	77441101	589	B1	01	00	12
	12.02	48.06	120.15	77441101	EB9	D7	03	00	12
	13.5	43.2	108	77741101	F1	9E	00	00	00
	13.92	44.55	111.38	77741101	F9	9F	00	00	00
	14.77	47.25	118.13	77741101	109	A1	00	00	00
19MHz ~ 25MHz	19.97	47.93	119.813	77541101	A29	C5	02	00	00
	20.25	48.6	121.5	77541101	111	A2	00	00	00
	21.16	43.2	108	77441101	F1	9E	00	00	00
	21.6	43.2	108	77441101	9F1	BE	02	00	00
	22.05	44.1	110.25	77441101	579	AF	01	00	00
	22.5	45	112.5	77441101	581	B0	01	00	00
	22.95	45.9	114.75	77441101	101	A0	00	00	00
	23.4	46.8	117	77441101	591	B2	01	00	00
	24.03	48.06	120.15	77441101	EB9	D7	03	00	00
25MHz ~ 34MHz	27	43.2	108	77341101	F1	9E	00	00	00
	27.56	44.1	110.25	77341101	579	AF	01	00	00
	28.12	45	112.5	77341101	581	B0	01	00	00
	28.69	45.9	114.75	77341101	101	A0	00	00	00
	29.11	46.58	116.44	77341101	A19	C3	02	00	00
	29.53	47.25	118.13	77341101	109	A1	00	00	00
	29.95	47.93	119.81	77341101	A29	C5	02	00	00
33MHz ~ 46MHz	36	43.2	108	77241101	F1	9E	00	00	00
	36.56	43.88	109.69	77241101	9F9	BF	02	00	00
	37.13	44.55	111.38	77241101	A01	C0	02	00	00
	37.5	45	112.5	77241101	581	B0	01	00	00
	38.25	45.9	114.75	77241101	589	B1	01	00	00
	39	46.8	117	77241101	591	B2	01	00	00

	39.6	47.52	118.8	77241101	EB1	D6	03	00	00
	40.05	48.06	120.15	77241101	EB9	D7	03	00	00
52M ~ 67M	54	43.2	108	77141101	F1	9E	00	00	00
	54.56	43.65	109.13	77141101	12F9	DF	04	00	00
	55.13	44.1	110.25	77141101	579	AF	01	00	00
	55.69	44.55	111.38	77141101	A01	C0	02	00	00
	56.03	44.82	112.05	77141101	E89	D1	03	00	00
	56.53	45.23	113.063	77141101	A09	C1	02	00	00
	57.38	45.9	114.75	77141101	589	B1	01	00	00
	58.05	46.44	116.1	77141101	EA1	D4	03	00	00
	58.5	46.8	117	77141101	591	B2	01	00	00
	59.06	47.25	118.13	77141101	A21	C4	02	00	00
	59.4	47.52	118.8	77141101	EB1	D6	03	00	00
	59.9	47.925	119.8125	77141101	A29	C5	02	00	00

※ [redacted] 為軟件人員設置項目

1. disp/sysclock.c 設定 B7C00104, B7C00110 的值

	由 MIPS 設定(sysclock.c)	
VAL_SYSMGM_CLK_DIV	= **B7C00104**	(Hex)
VAL_SYSMGM_AHB_PLL	= **B7C00110**	(Hex)
VAL_SYS_CLK_SRC	27000000	

2. disp/iml_cvbs.h 設定 CBh 的值

```
static const struct reg panel_init_p0[]={
        …….
    {0xC7,0x0D},
    {0xCB,CBh},
};
```