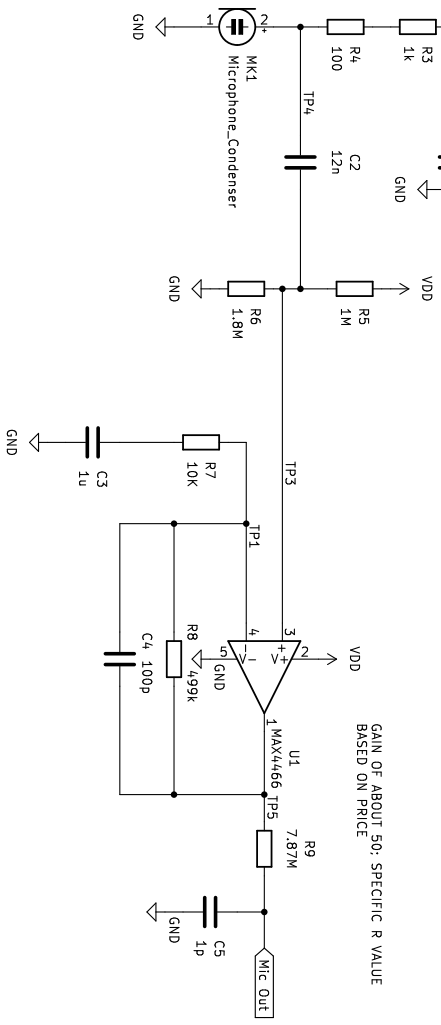


VDD = 5V AS PER FPGA POWER REQ

USE MAXIMUM POSSIBLE CAPACITOR HERE
IF NOISE PREVALENT FROM POWER SUPPLY CONSIDER ELECTROLYTIC CAP



***** REVISION TABLE *****		
DATE	AUTHOR	CHANGE DESCRIPTION
12/29/2023	EN	INITIAL DESIGN

AUTHOR: EVAN NEWELL		
LWVD		
Sheet: /		
File: Microphone.kicad_sch		
Title: MICROPHONE SCHEMATIC		
Size: A4	Date:	Rev: A
KiCad E.D.A. kicad 7.0.8		Id: 1/1