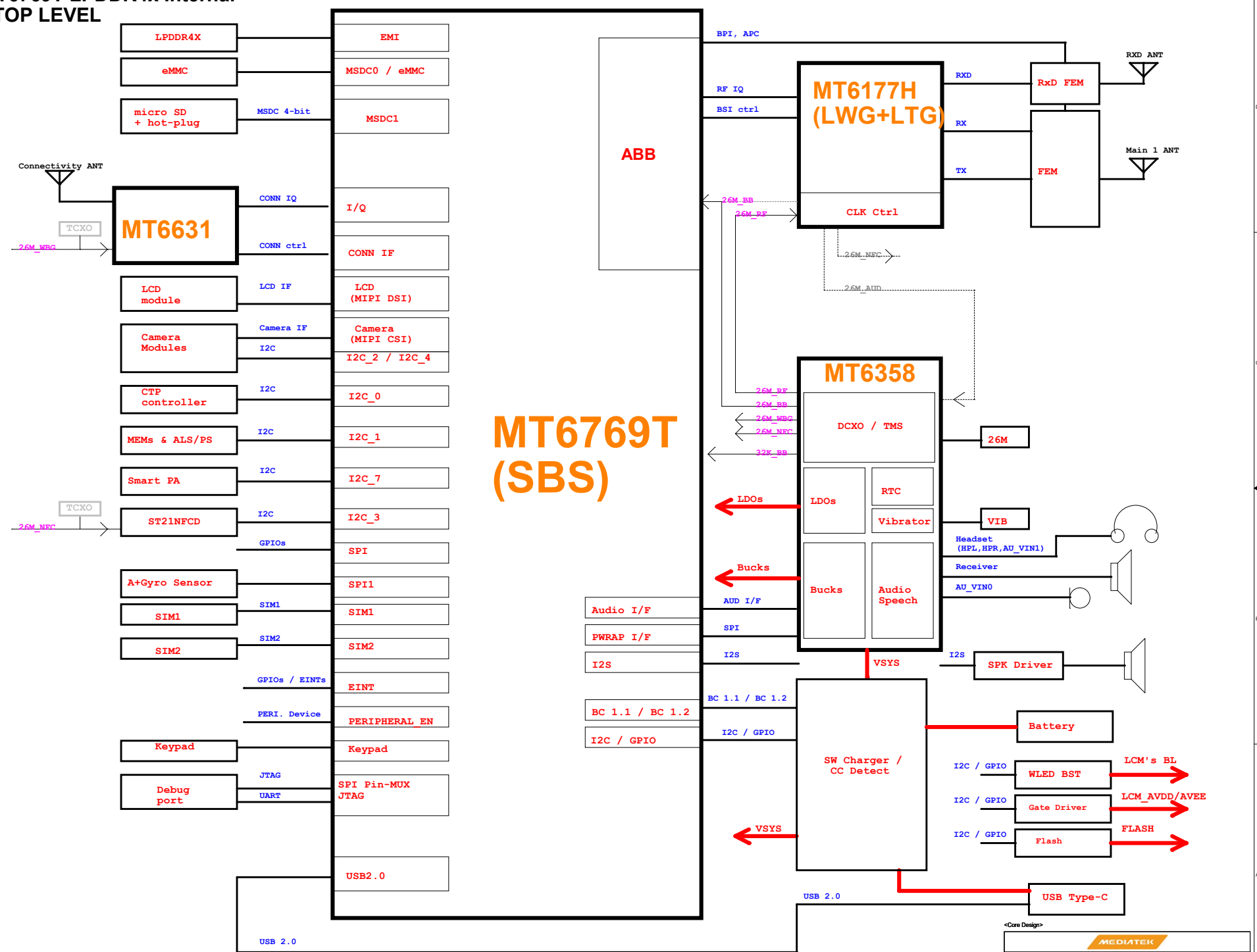


Project : MT6769T LPDDR4x Internal
REF_SCH TOP LEVEL



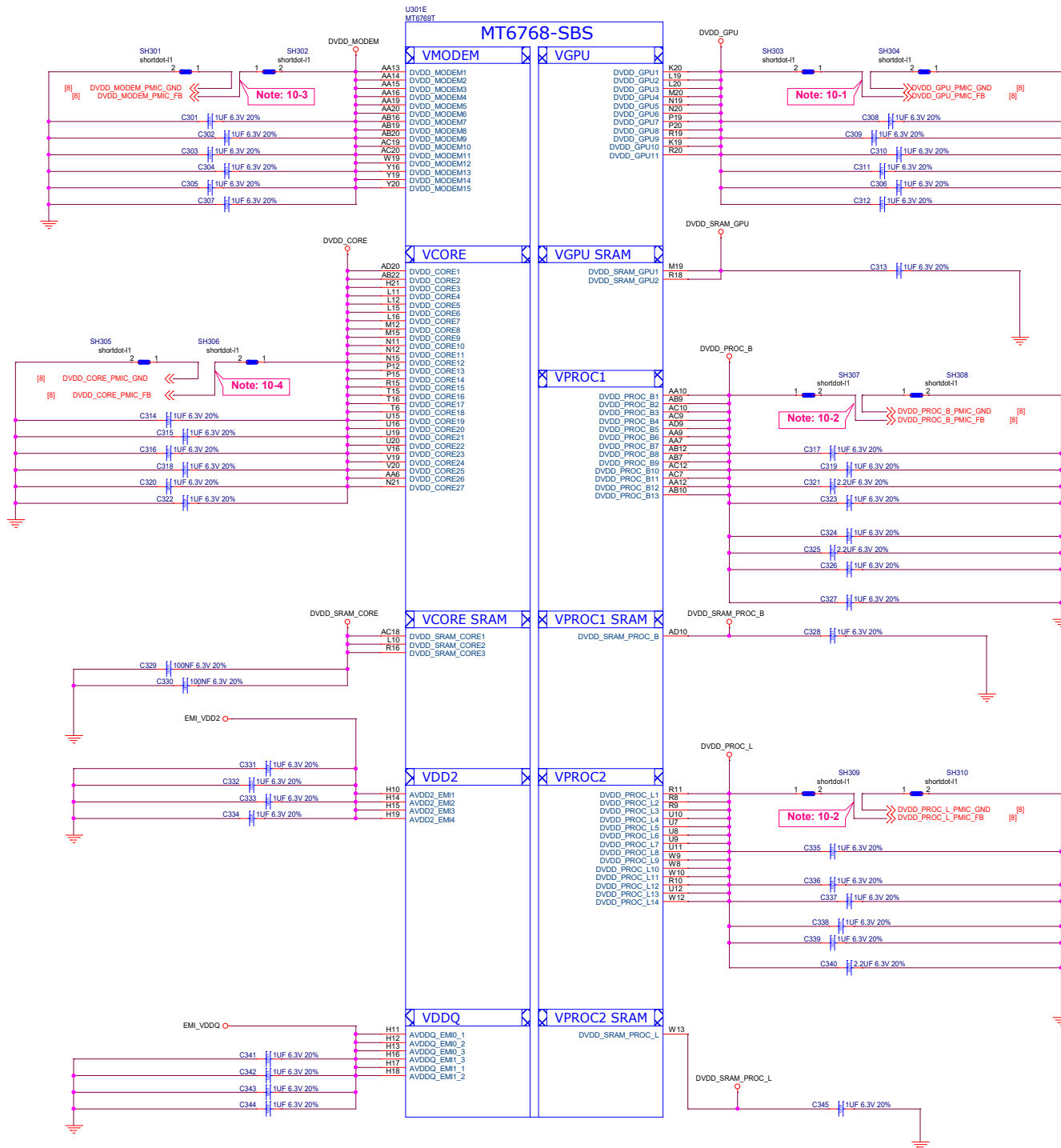
Schematic design notice of "10_BB_ POWER_PDN" page:

Note 10-1: Differential pair of DVDD_GPU remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

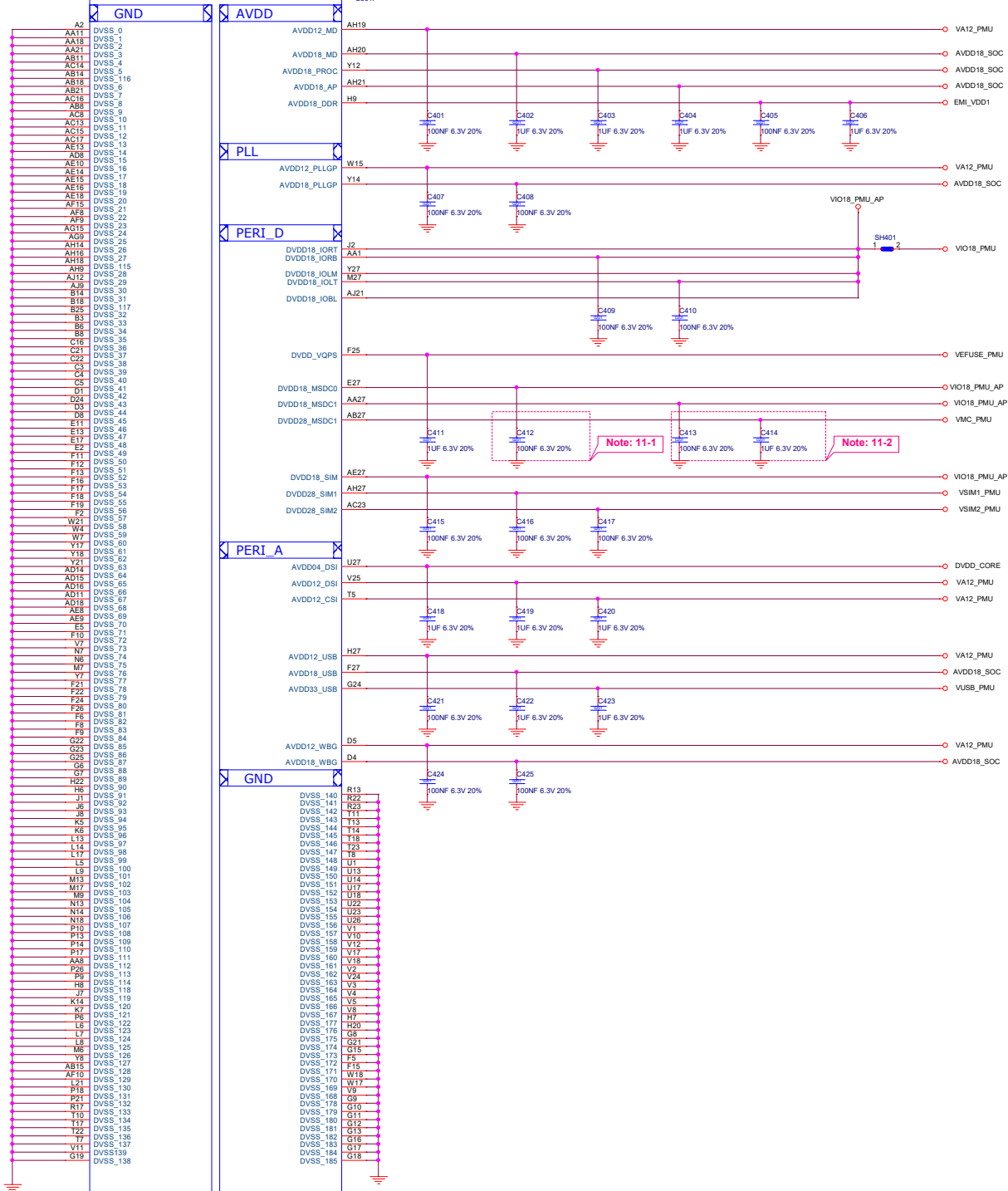
Note 10-2: Differential pair of DVDD_PROC remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Note 10-3: Differential pair of DVDD_MODEM remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Note 10-4: Differential pair of DVDD_CORE remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)



MT6768-SBS



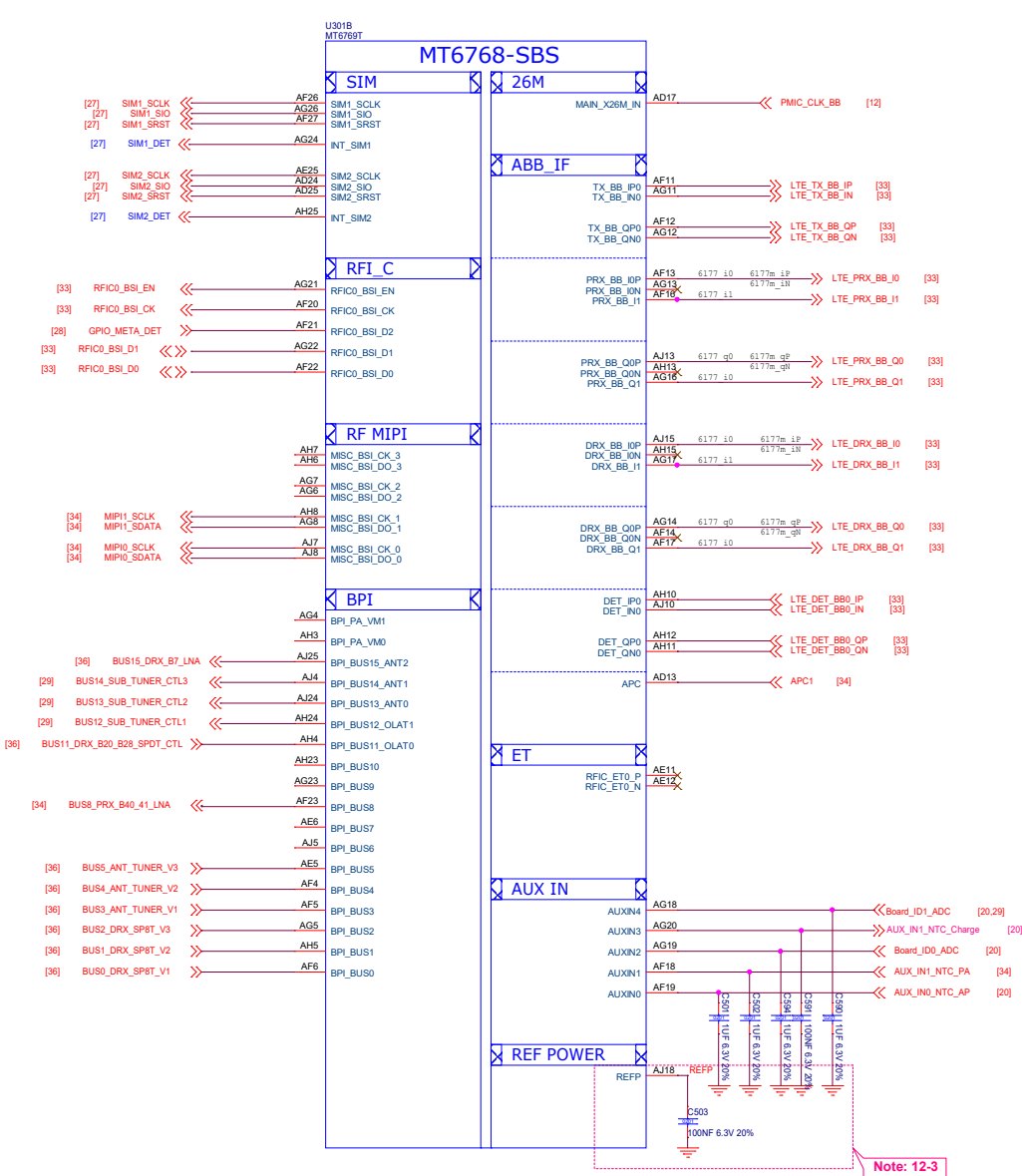
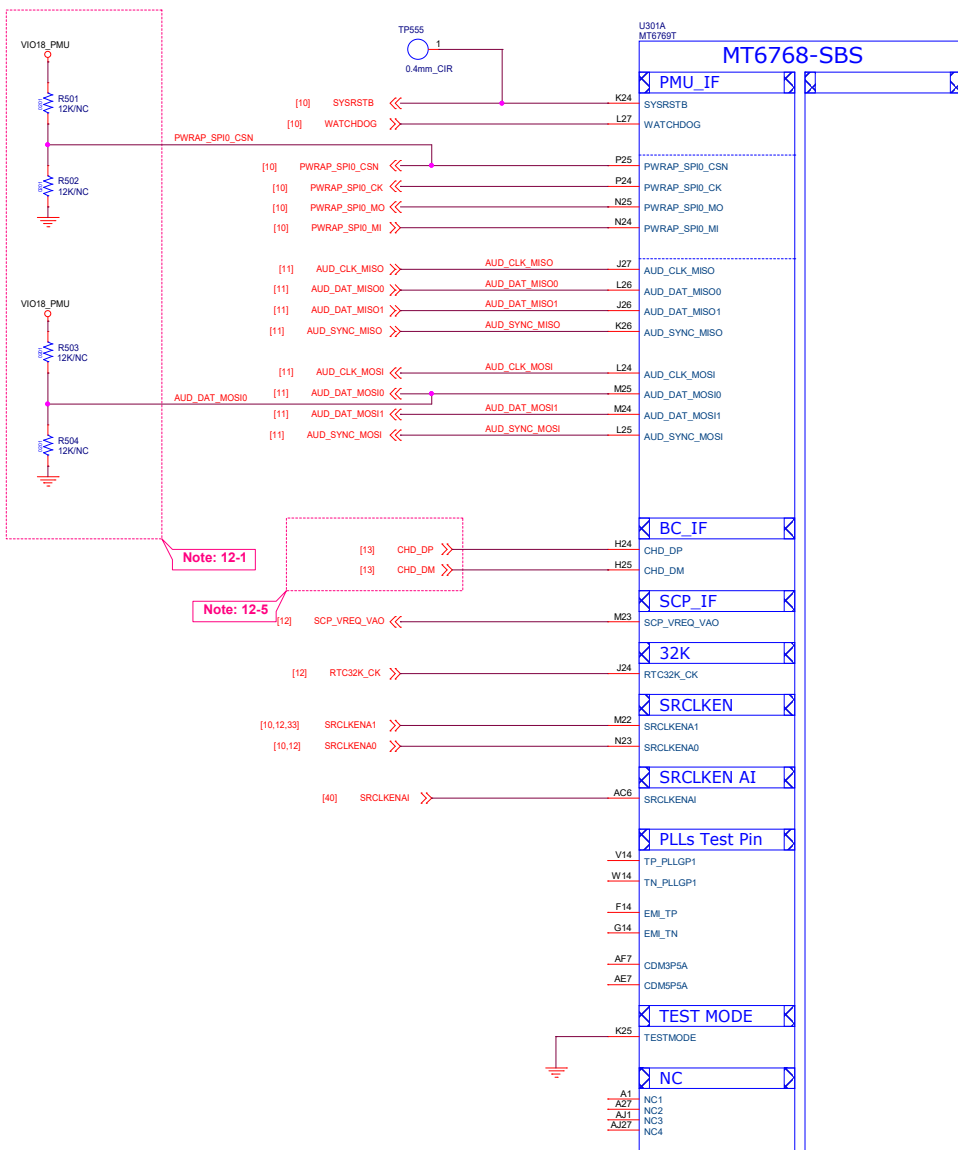
Schematic design notice of "11_BB_POWER_IO" page:

Note 11-1: C412 closed DVDD18_MSDC0 150mil

Note 11-2: C413 closed DVDD18_MSDC1 150mil
C414 closed DVDD28_MSDC1 150mil

<Core Design>

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Schematic design notice of "12_BB_1" page:

Note 12-1: PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out

PWRAP_SPI0_CSN default=PU	AUD_DAT_MOSI0 default=PD	JTAG Function	
		AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by ext. PU)	SPI0 + EINT8	SPI2 + SPI3
LO (by ext. PD)	LO	SPI0 + EINT8	N/A
LO (by ext. PD)	HI (by ext. PU)	N/A	N/A

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

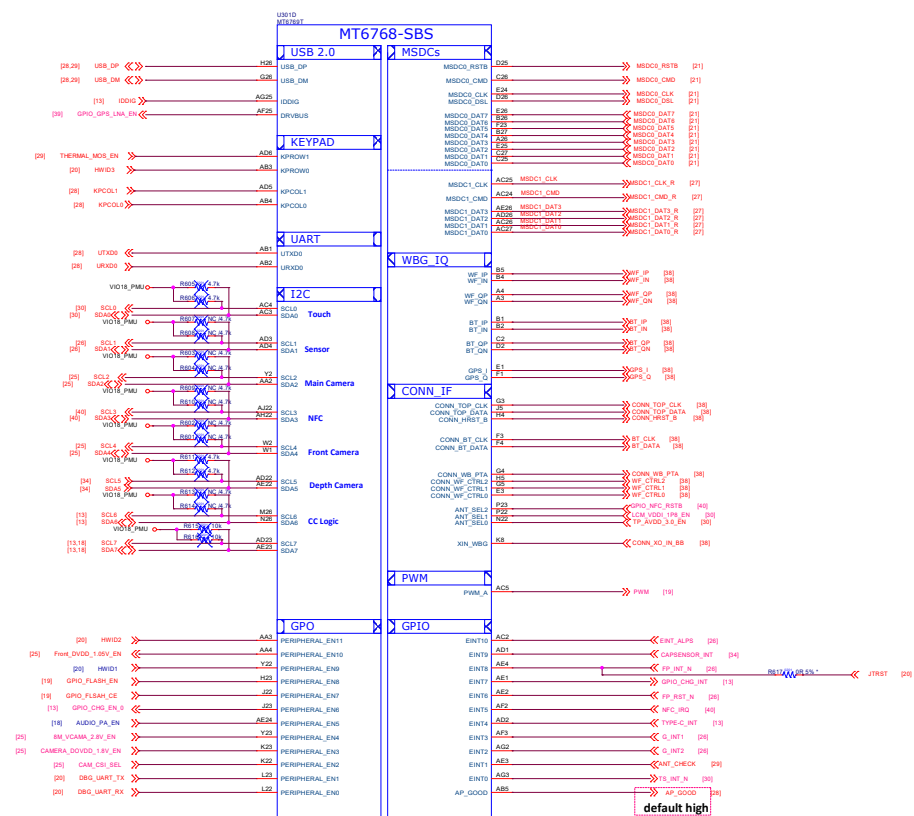
Note 12-3: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

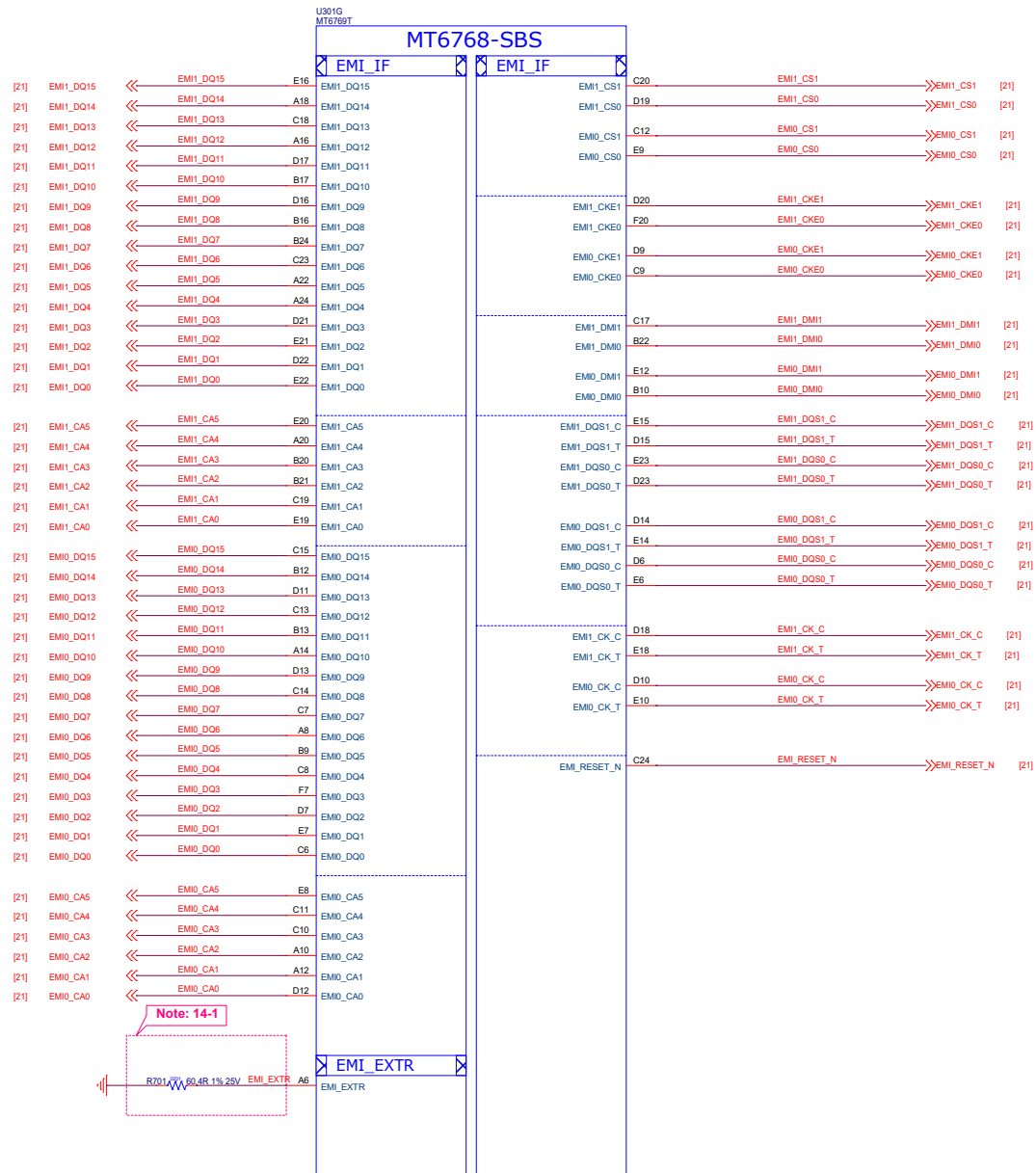
Note 12-4: HW pin for DDR type feature in bootstrap (refer to BB HW design Notice)

AUD_SYNC_MISO default=PD	AUD_CLK_MISO default=PD	CAM_PDN3 default=PD	PMIC 6358 voltage VDRAM1 / VDRAM2	DDR Type
No ext. pull	No ext. pull	No ext. pull	1.125v / 0.6v	LP4X eMCP
No ext. pull	12K pull to VIO18	No ext. pull	OFF / 1.8v	Reserved
12K pull to VIO18	No ext. pull	No ext. pull	1.225v / OFF	LP3 eMCP
12K pull to VIO18	12K pull to VIO18	No ext. pull	1.125v / 1.8v	Reserved

Note 12-5:

Charger must have D+/D- pin for charger type USB detection.
Charger must have at least 500mA USB current for All charger type.

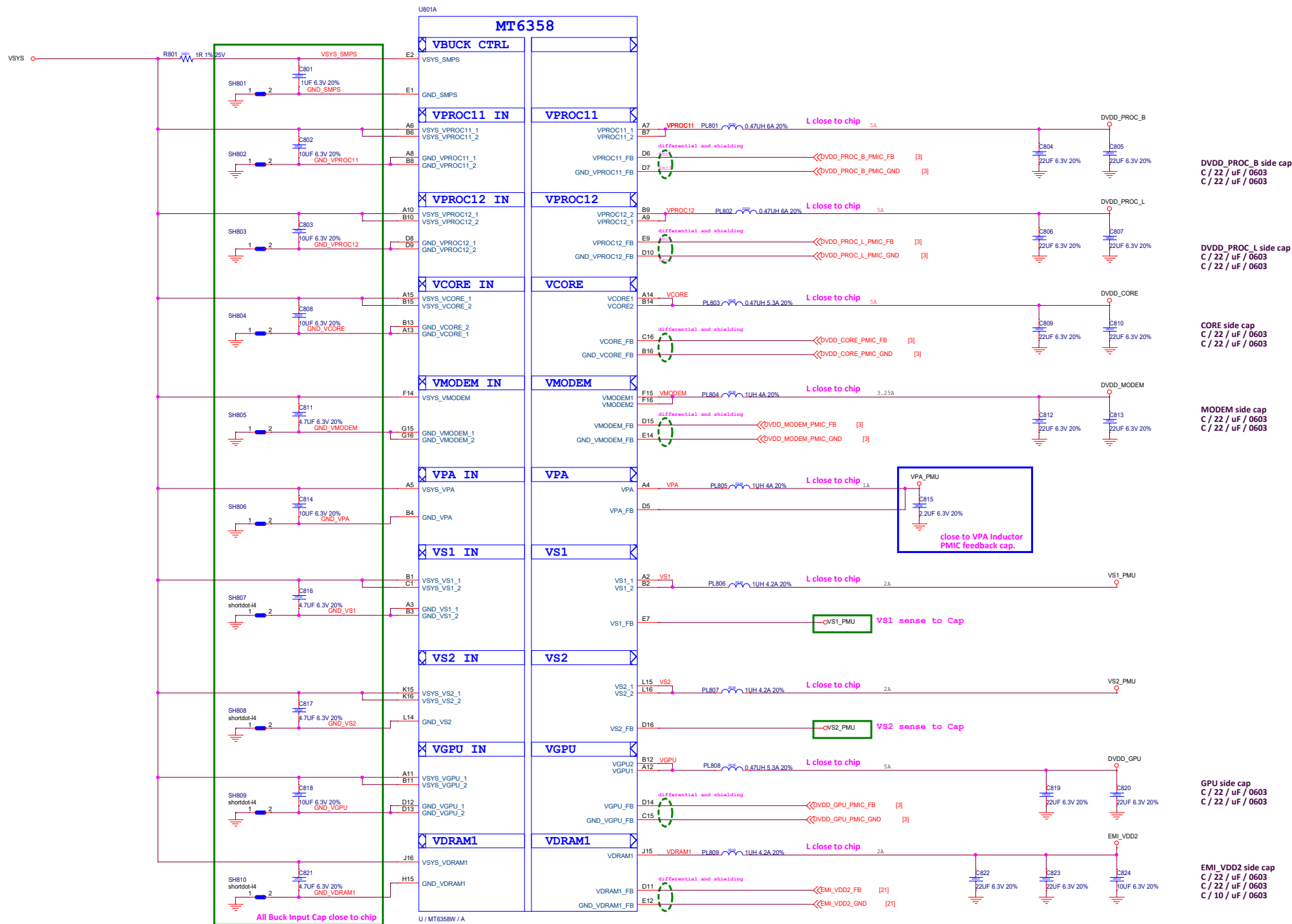


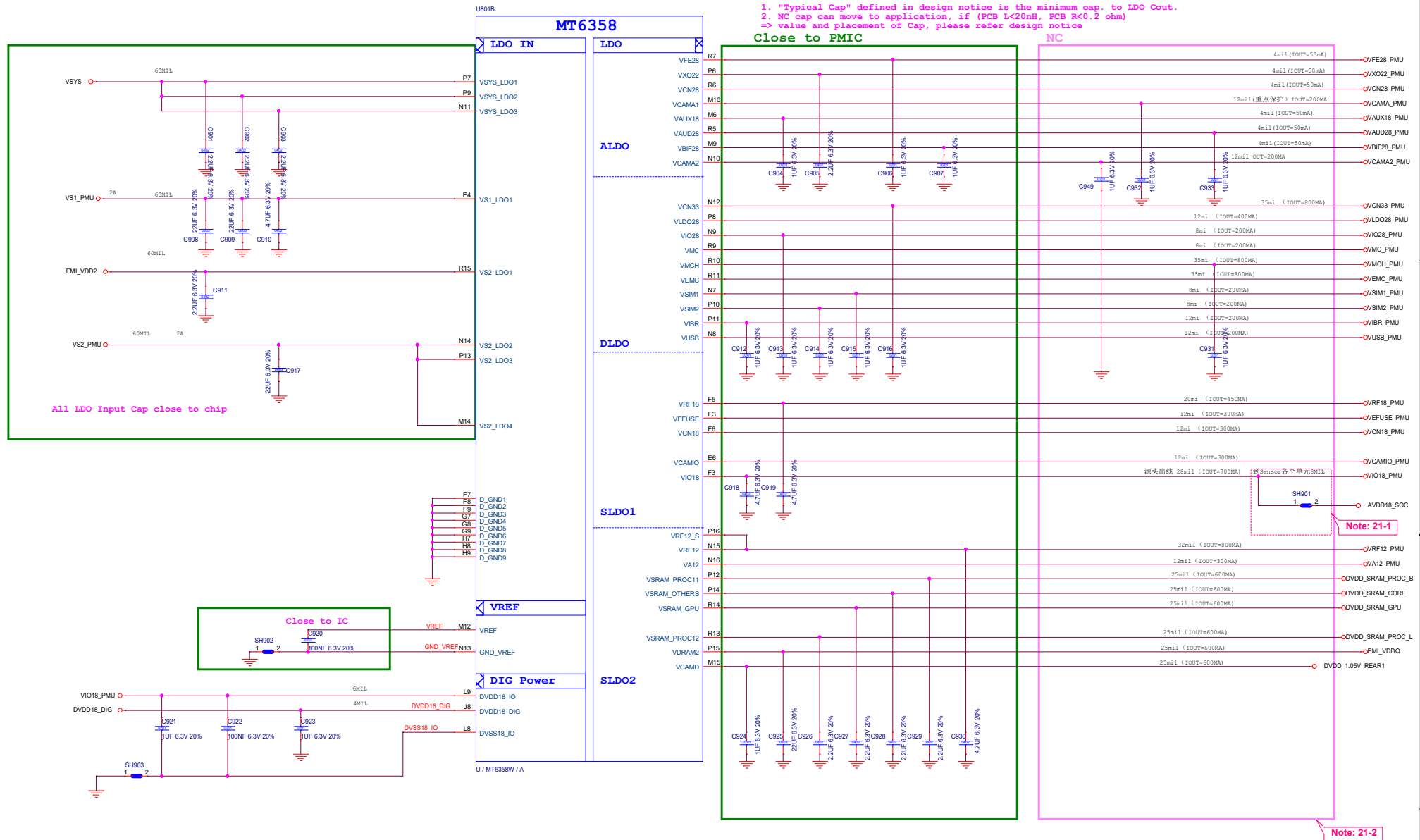


Schematic design notice of "14_BB_3" page.

Note 14-1: R701 please select 60.4 ohm (1%) resistor

<Core Design>

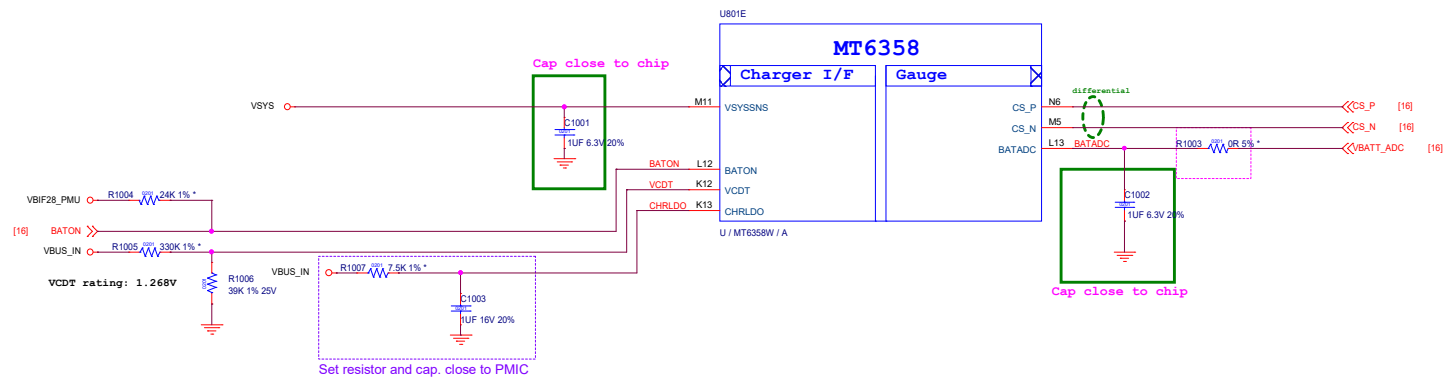
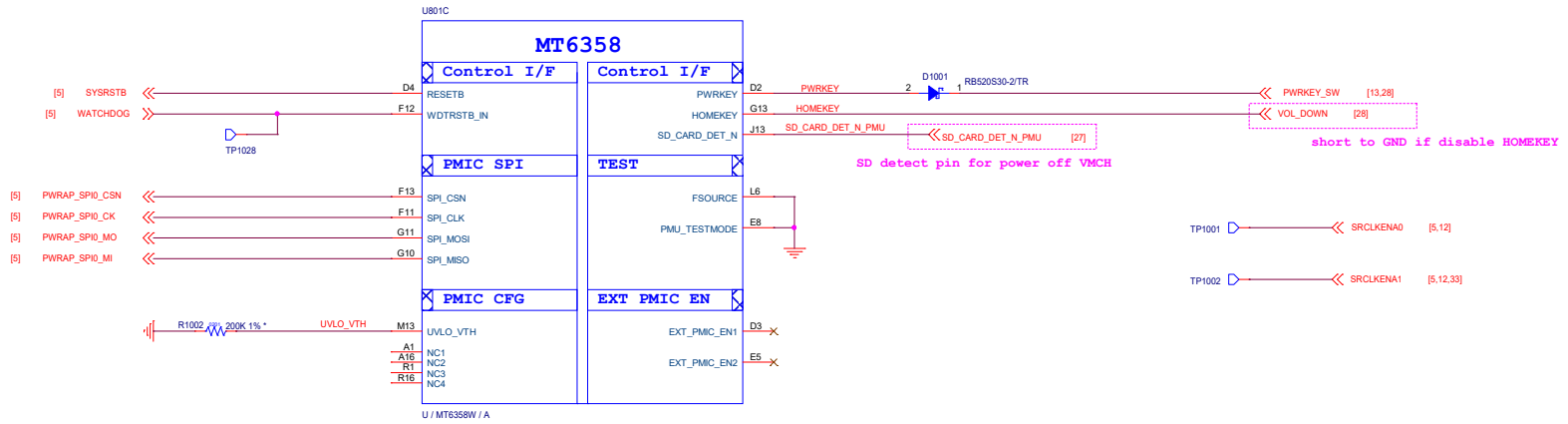




Schematic design notice of "21_POWER_MT6358-LDO" page.

Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
 Please also refer to MT6358 design notice for further detail design information

Note 21-2: If these power trace can meet LDO layout constraint, these CAP can be NC or removed.
 Please refer to MT6358 design notice.



<Core Design>

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Title	10_POWER_MT6358-IF
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UB01D
U / MT6358W / A

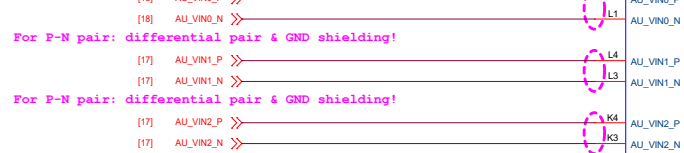
MT6358

AUDIO IF



AUDIO INPUT

For P-N pair: differential pair & GND shielding!

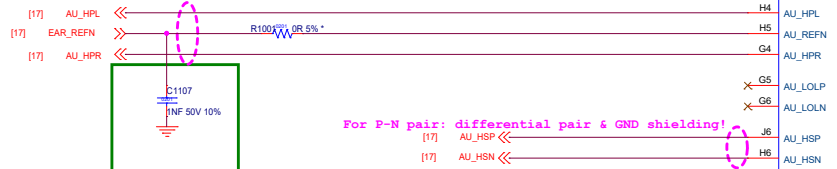


ACCDET



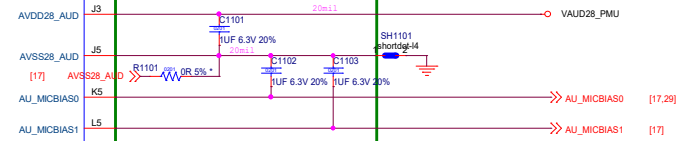
AUDIO OUTPUT

-AU_HPL and AU_HPR should be routed as single end signal and be guarded by GND, up and down, left and right respectively
-The suggested layout pattern of AU_HPL/ AU_HPR/ AU_REFN is " GND AU_HPL AU_REFN AU_HPR GND"



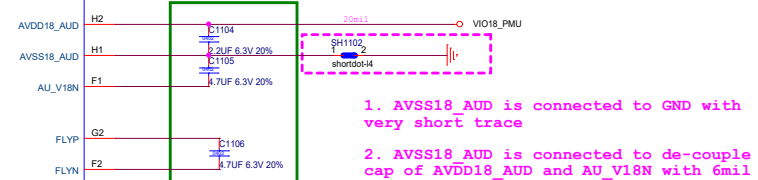
Close to Chip

UL POWER



Close to Chip

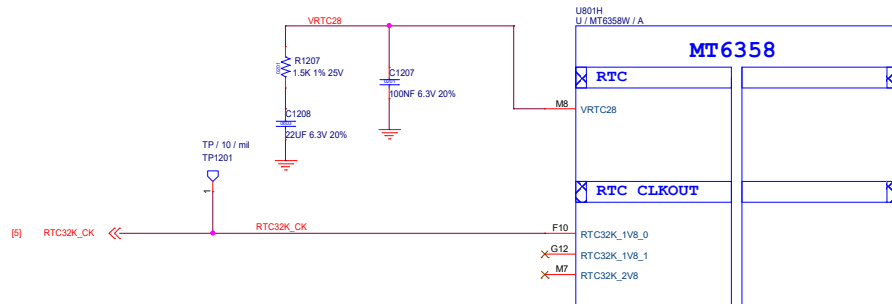
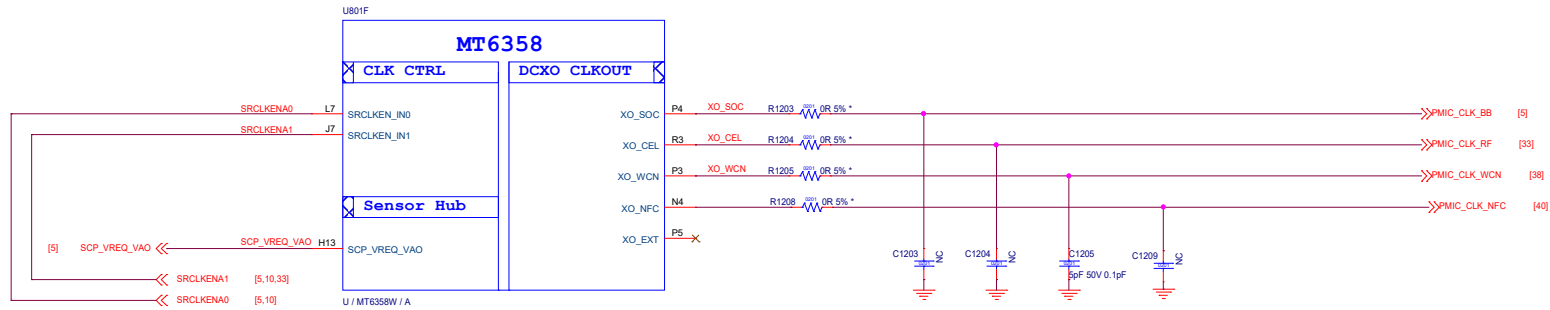
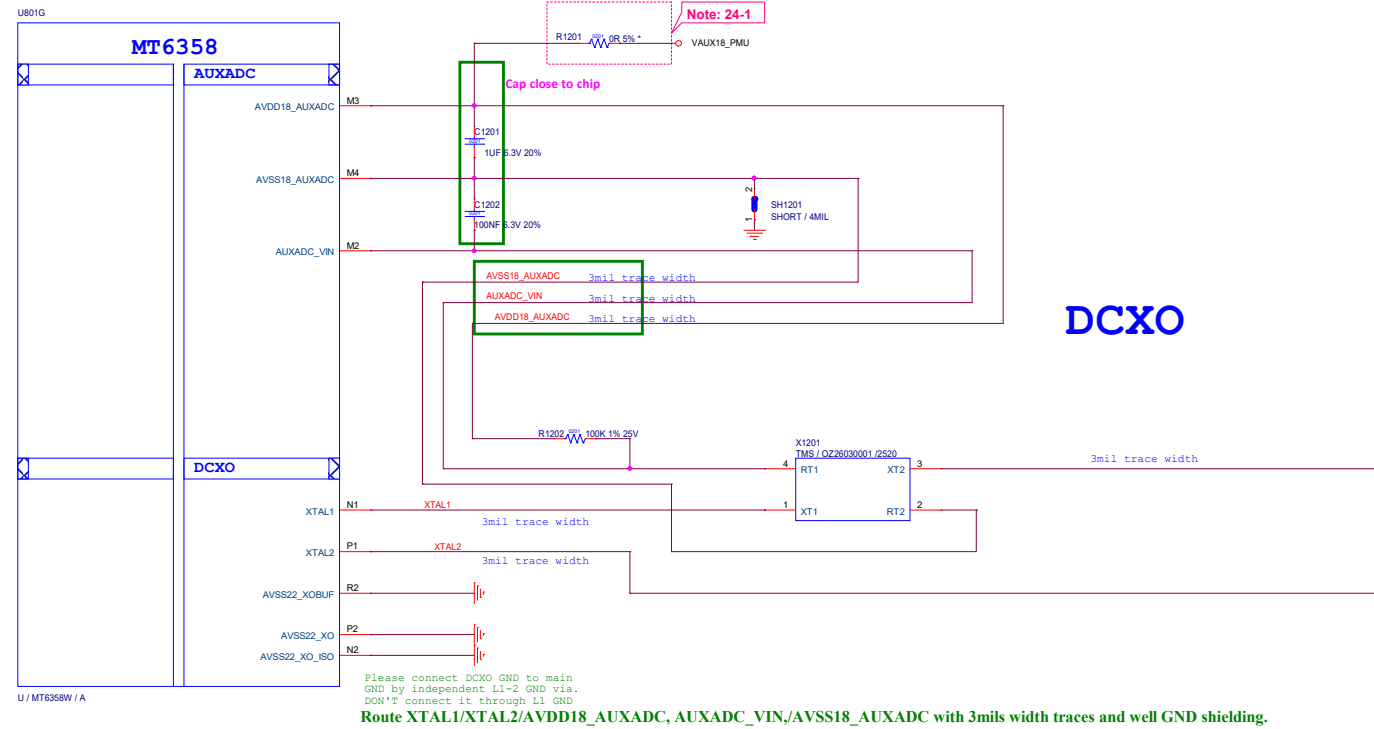
CHARGE PUMP



Close to Chip

1. AVSS18_AUD is connected to GND with very short trace
2. AVSS18_AUD is connected to de-couple cap of AVDD18_AUD and AU_V18N with 6mil trace respectively

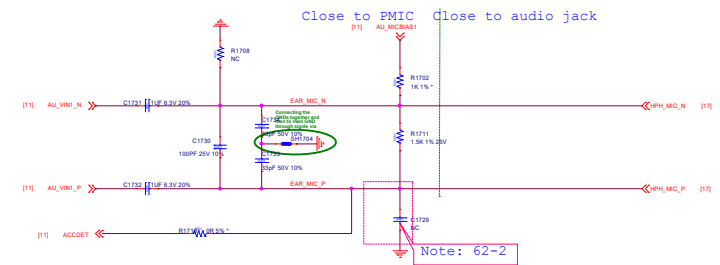
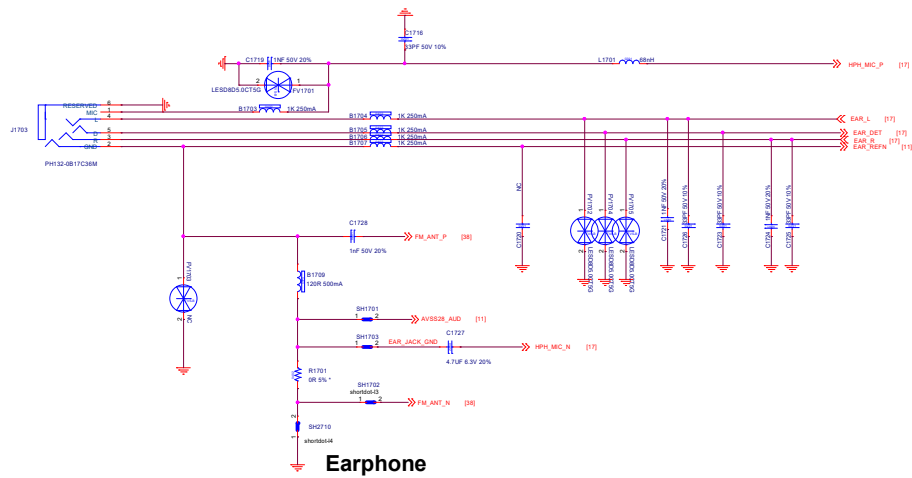
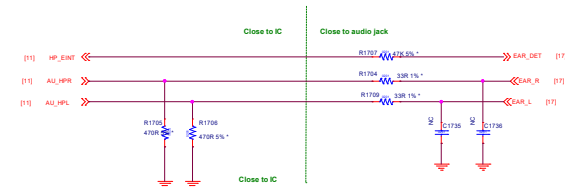
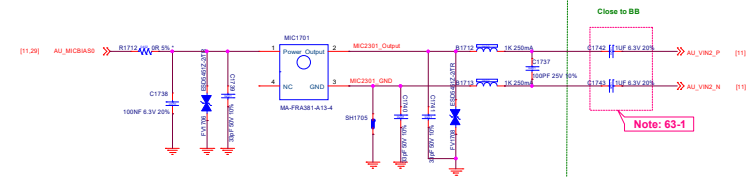
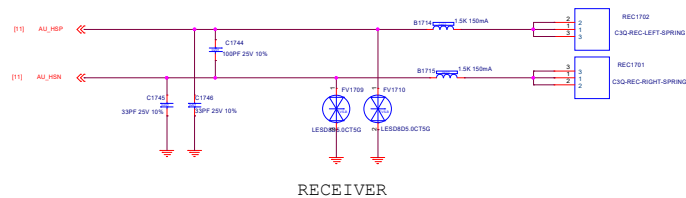
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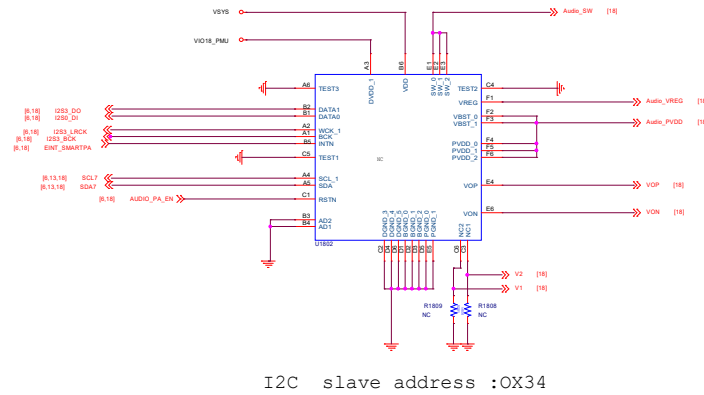
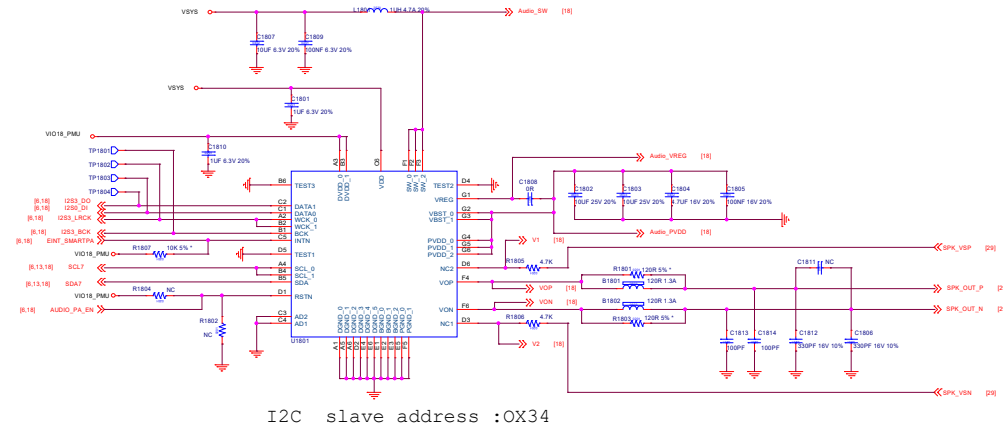


Schematic design notice of "24_POWER_MT6358_Clock"

Note 24-1: Please follow MT6768_MT6358 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD.

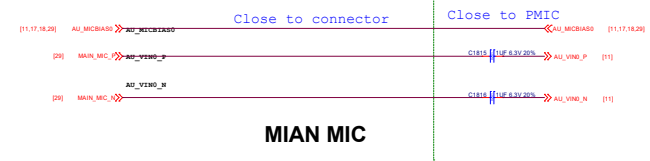


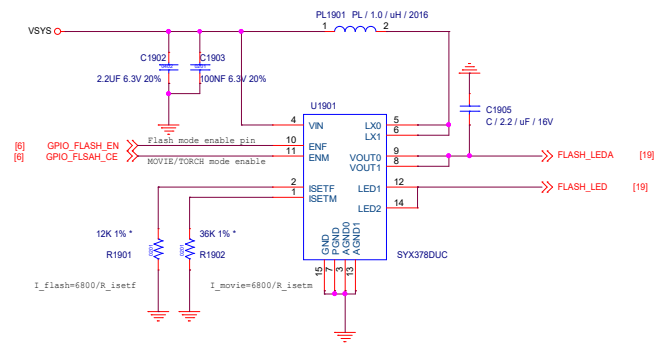




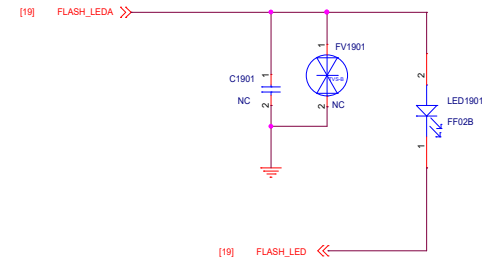
Smart PA

Audio PA兼容焊盘设计

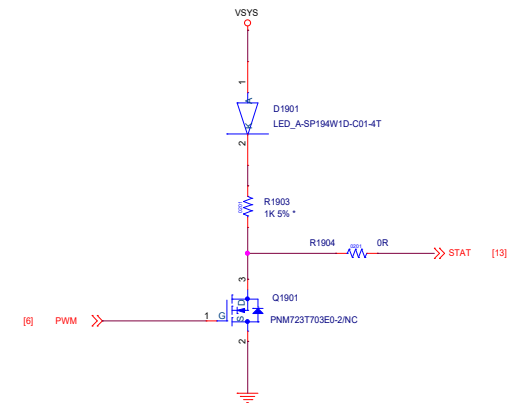




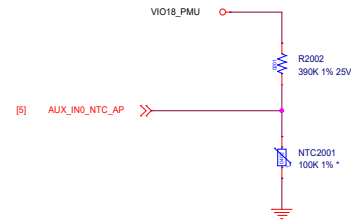
Flash LED Driver



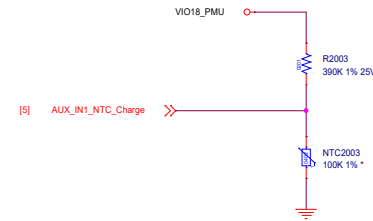
FLASH LED



Charger indicator

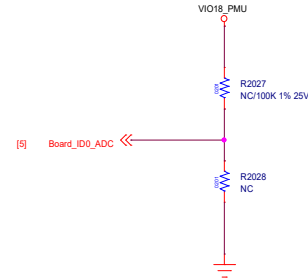
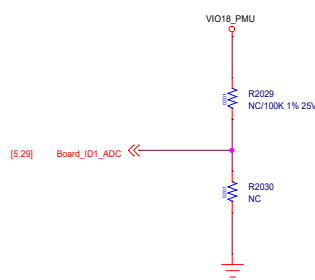


Thermistor to sense AP temperature

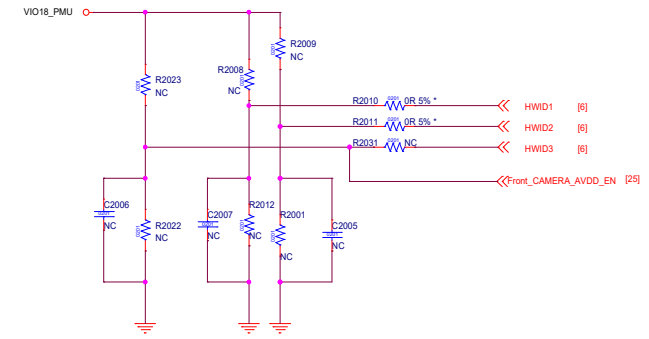


Thermistor to sense charge temperature

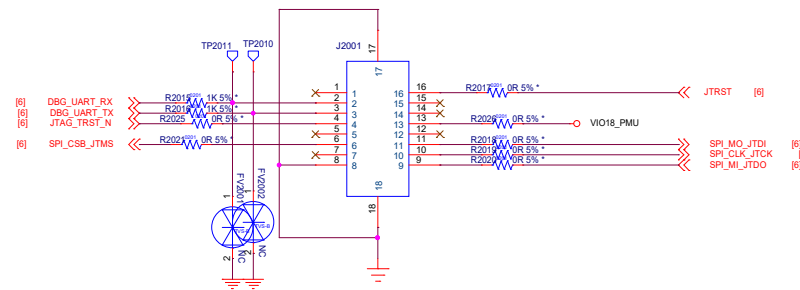
1. NTC2001 must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

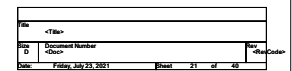
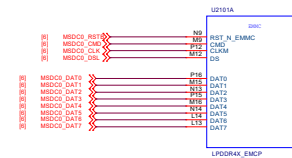
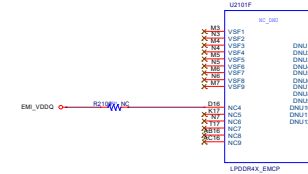
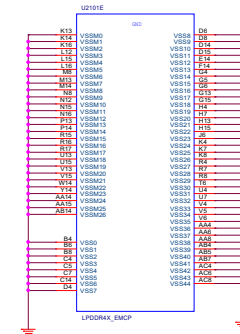
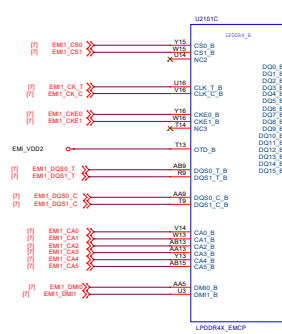


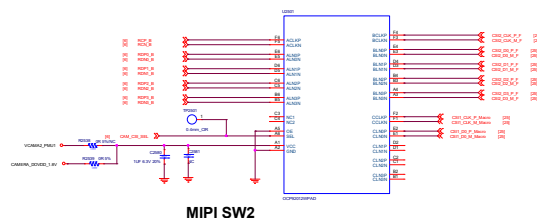
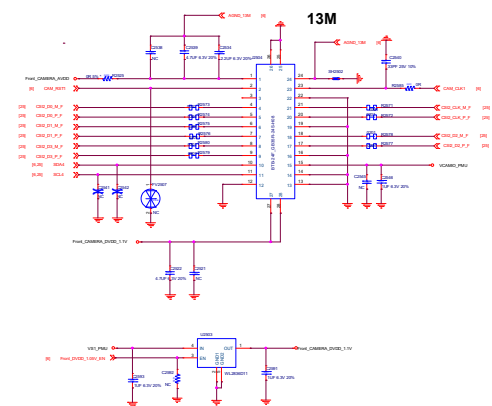
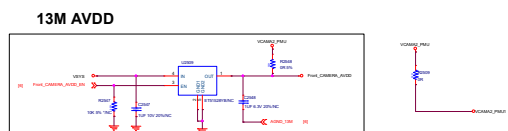
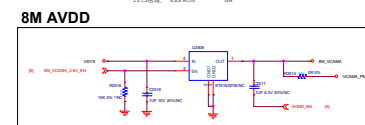
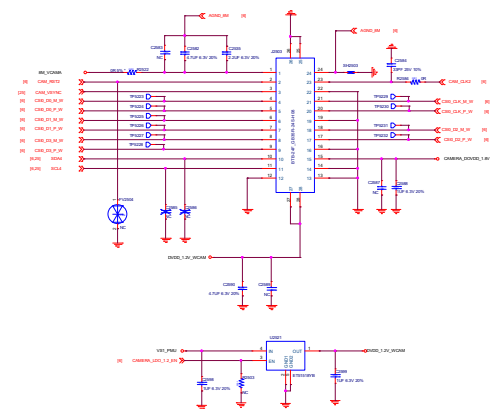
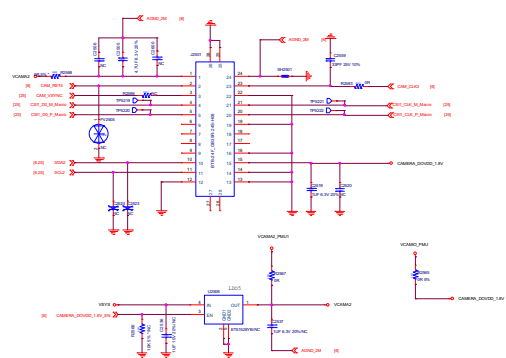
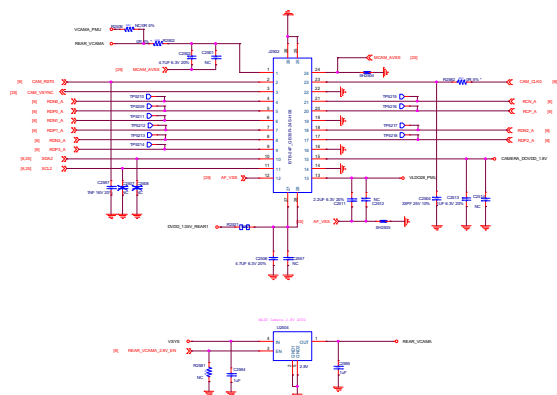
RF ADC SKU

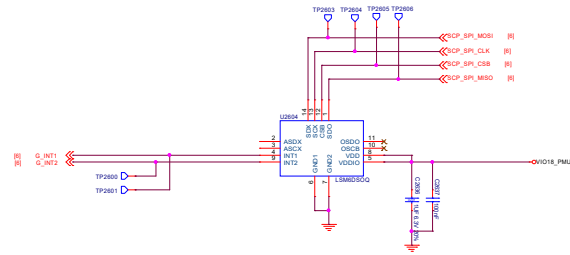


HWID



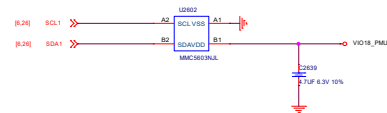




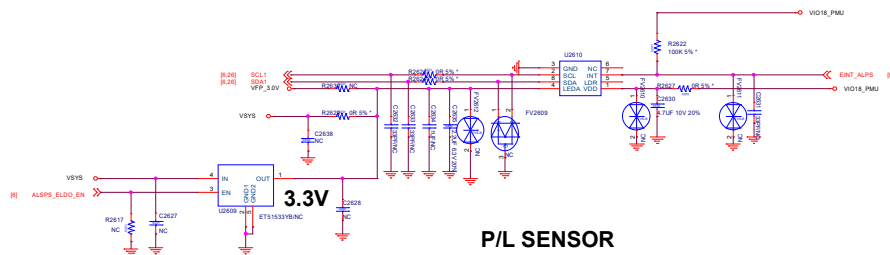


A+GYRO

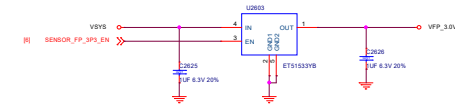
MMC5603NJL I2C slave address :0X30



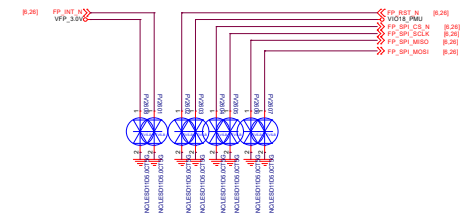
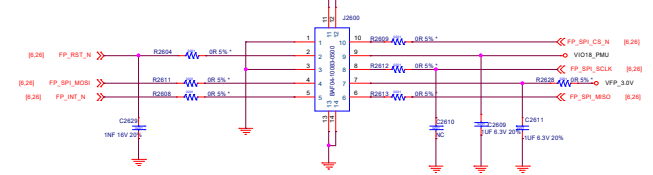
M SENSOR

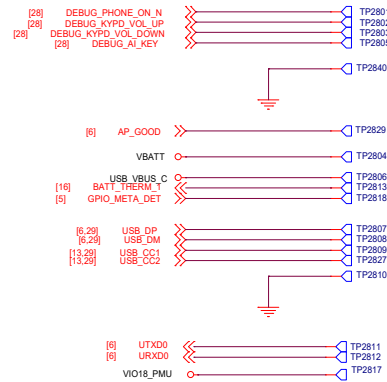
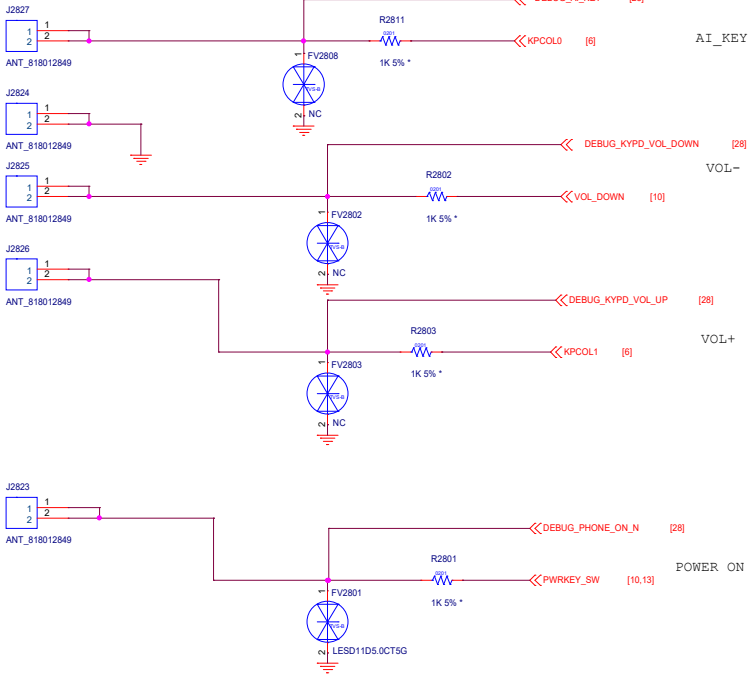


P/L SENSOR

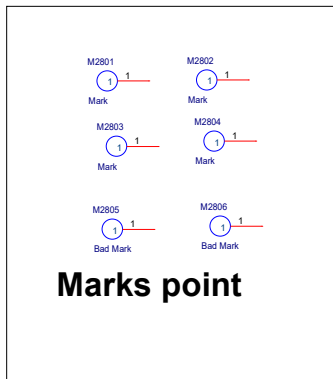
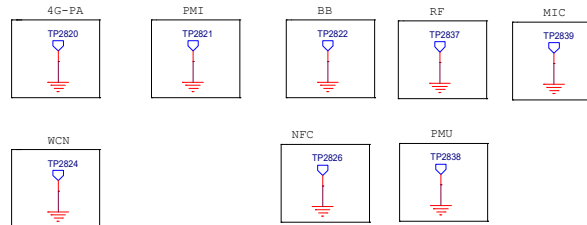


FP

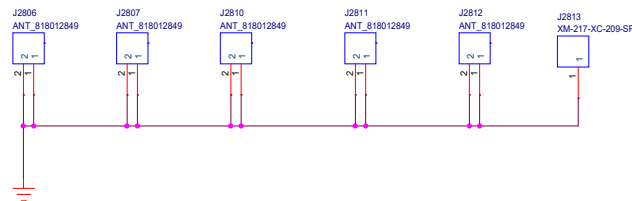




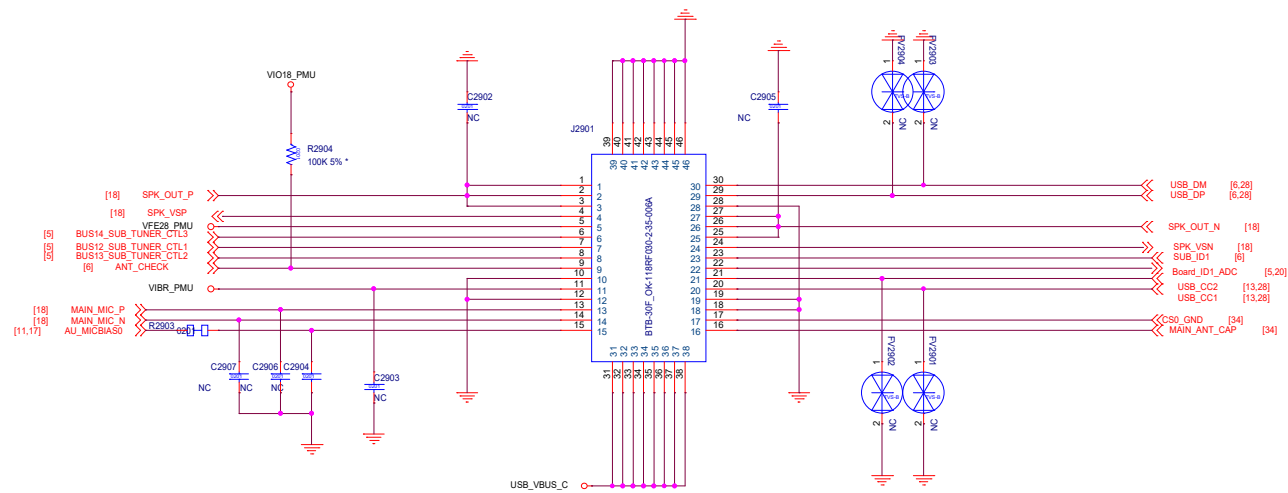
屏蔽盖



Marks point

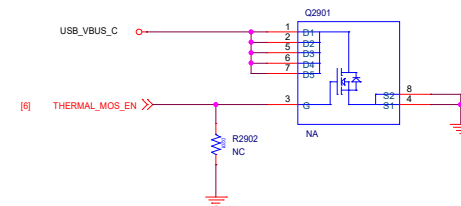


USE FOR GND



Sub Connector

10V 3A / 5V 2A



<Core Design>

MEDIATEK

File

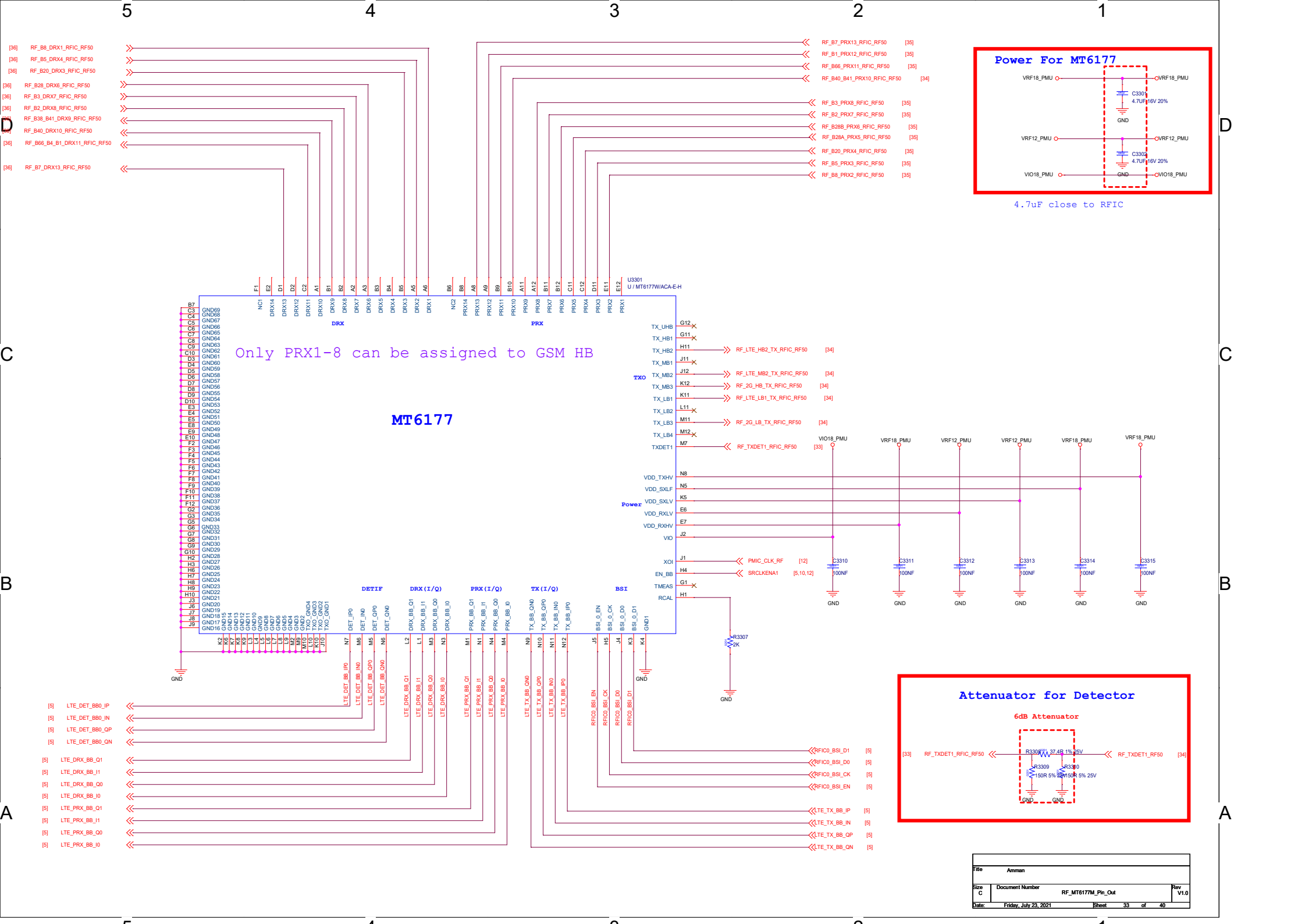
Size

C

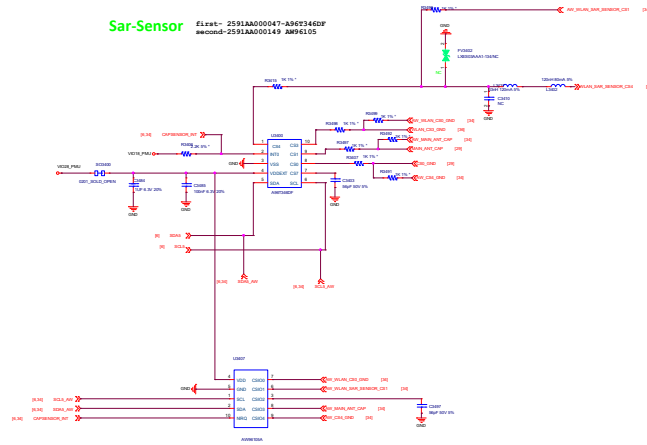
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Date: Friday, July 23, 2021

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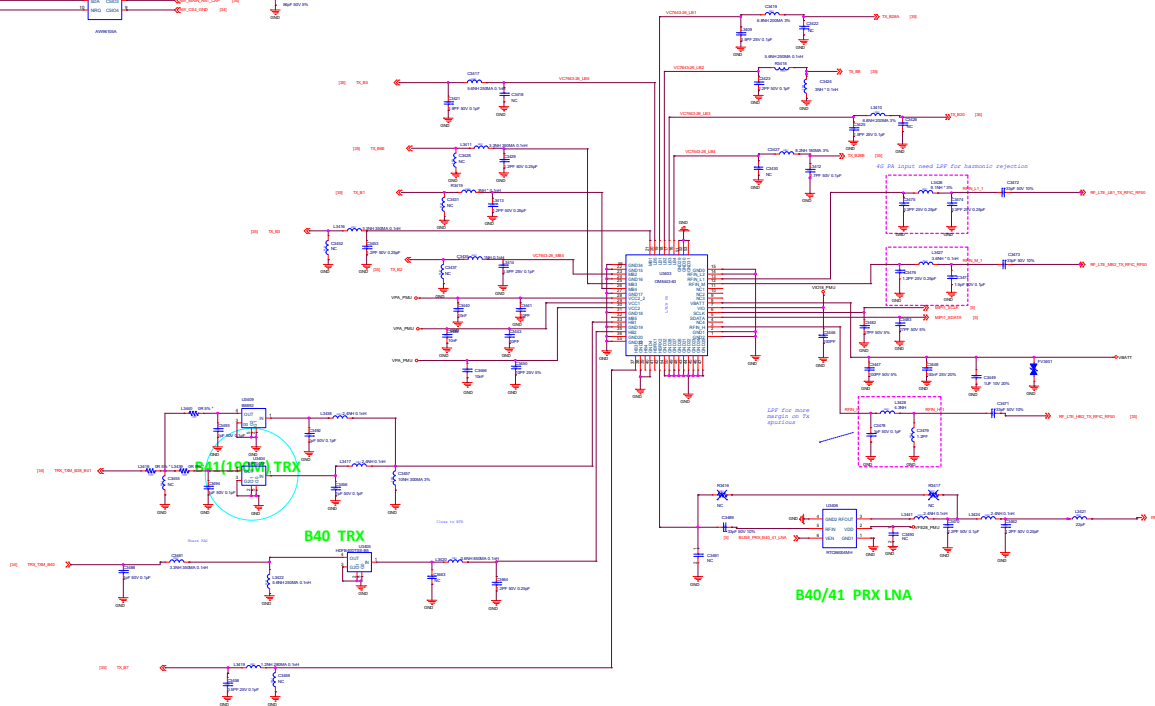
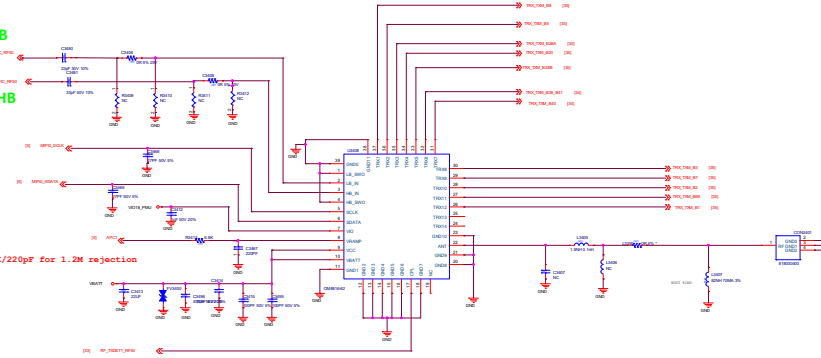
Sar-Sensor
 First- 2591AA00047-A9693460F
 second-2591AA000149 AM96105



2G_PAIN_LB

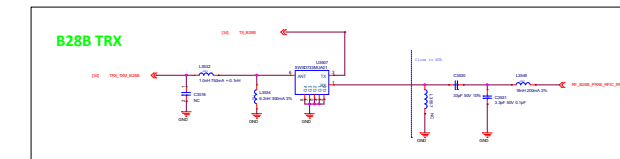
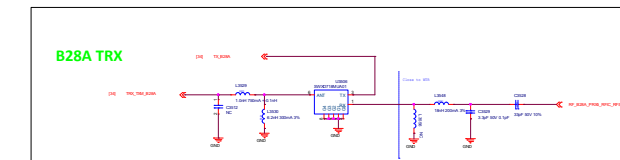
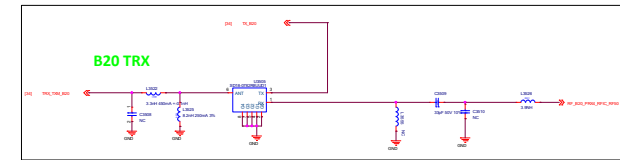
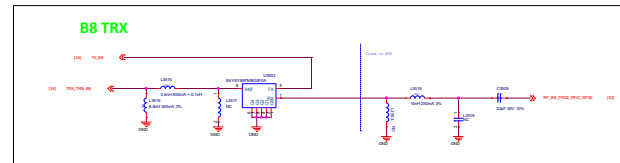
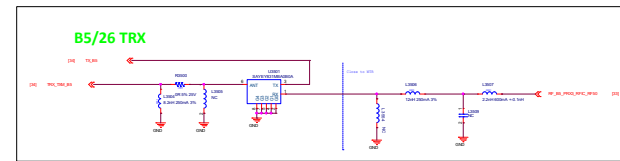
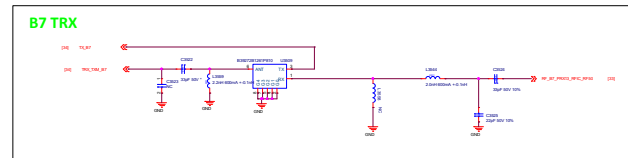
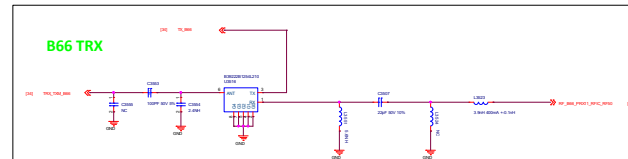
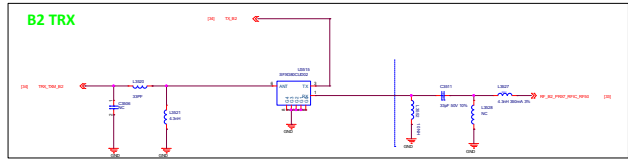
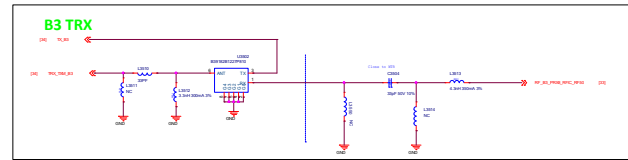
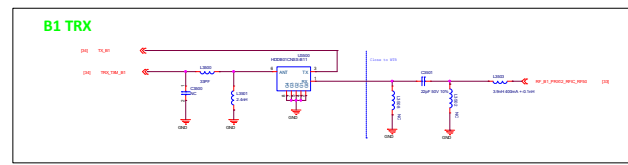
2G_PAIN_HB

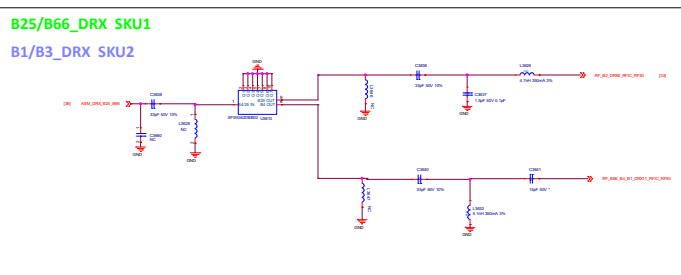
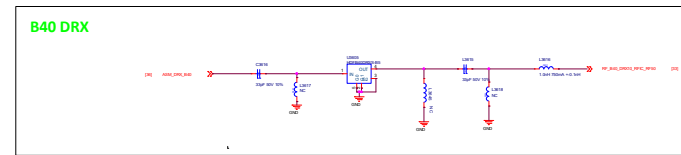
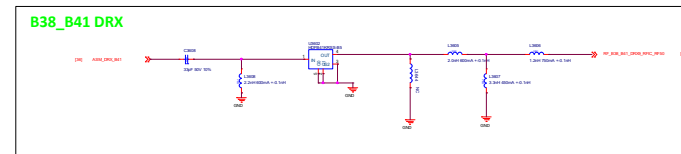
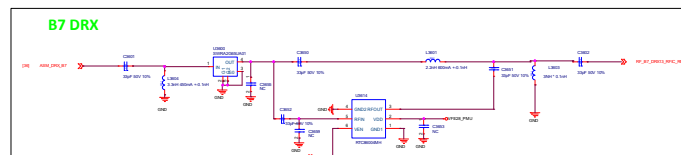
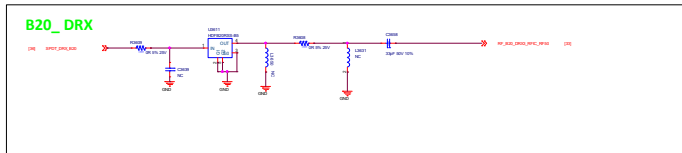
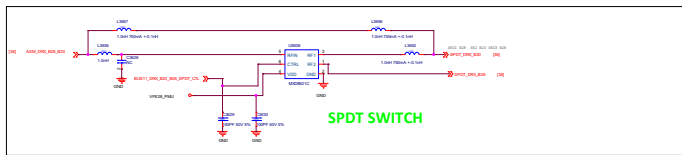
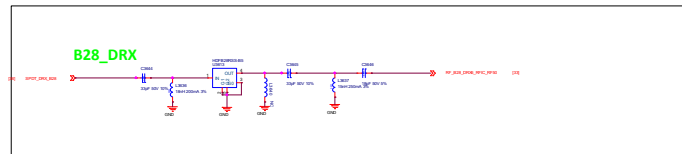
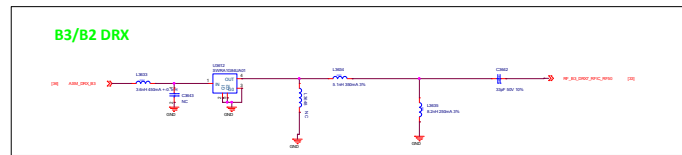
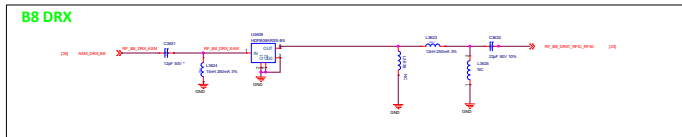
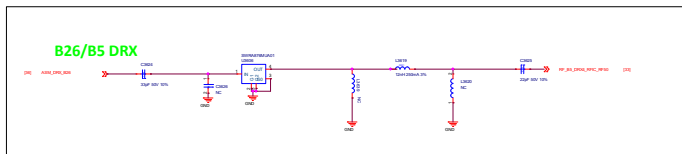
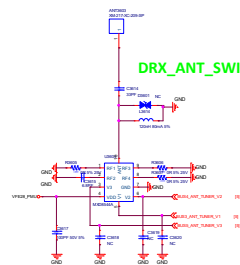
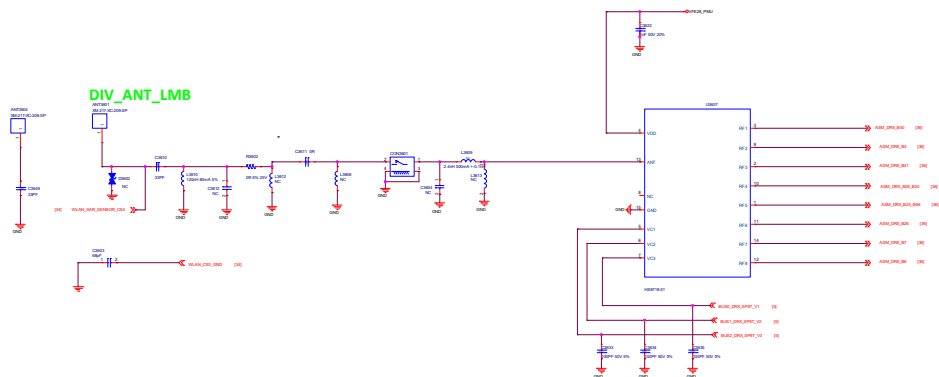
RC=6.98R/220pF for 1.2M rejection

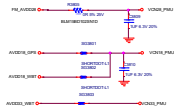


Note:
 Reserve one tuning cap. For PMIC VPA total cap requirement,
 the total cap at RP side should be in 6.2uF +/-10%.

RT3401 and C3493 close to PA, and located in the same layer

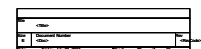






Note 51-4: Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

Name	
Animal	
Order	Discussion Number
8	CONNECTIVITY_COMBIS_MF0033



A

