SeDA: Secure and Efficient DNN Accelerators with Hardware/Software Synergy

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1. Background

Secure is important for DNN-based Applications:

Attacked auto-vehicles can disrupt critical functions and pose safety risks

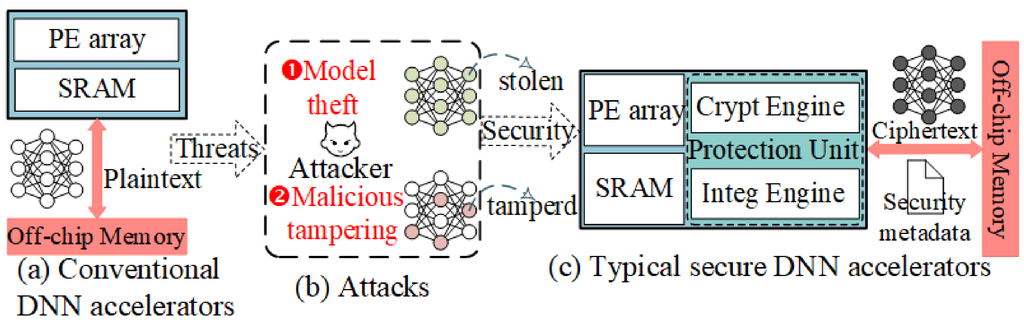
Healthcare cybersecurity endanger patient data, medical devices, and operations

Maliciously hacked AI robots may harm human interests

Malicious data alterations undermine financial market fairness and investor trust

Typical Secure DNN Accelerators:

Threat Model: unsecure off-chip memory and communication buses.
Memory Protection Mechanism: authentication encryption.



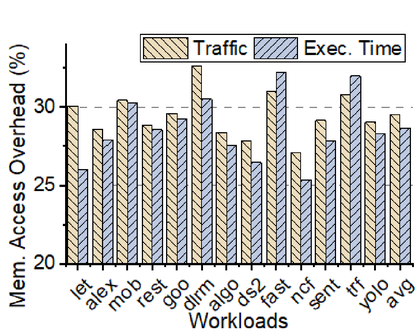
2. Motivations

Costly Off-Chip Memory Access Overhead for Integrity Verification

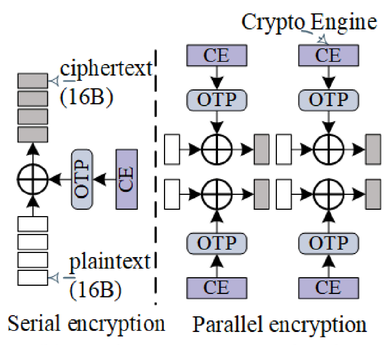
- Merkle Tree (MT) with its variants incurs extra off-chip data access, to defend replay attacks.
- Different cross-layer tiling patterns introduce redundant authentication data read and computation.
- XOR-based MAC scheme may lead to re-permutation attack.

High Hardware Overhead for Confidentiality Protection

- Serial encryption engine provides limited bandwidth.
- Parallel approach incurs amount of hardware overhead.
- Shared one-time pad (OTP) can be vulnerable to the single-element collision attacks.



(a) Memory access overhead

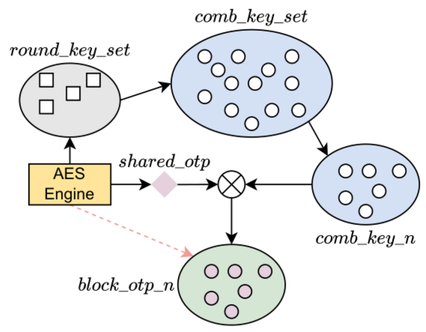


(b) Hardware crypto overhead

3. Proposed SeDA

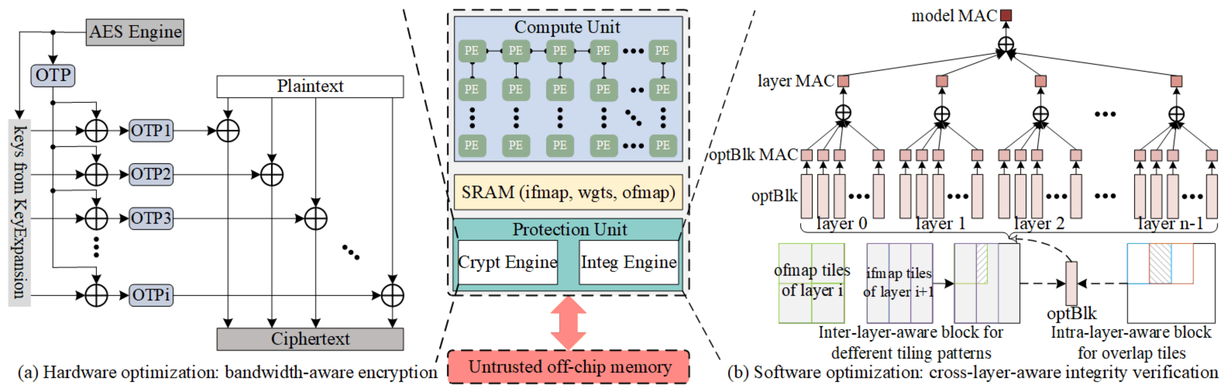
Bandwidth-Aware Encryption Scheme:

- Utilize KeyExpansion of AES to generate multiple unique OTPs
- It can en/decrypt all 128-bit sub-blocks by running one time of AES engine
- Improve the memory protection bandwidth to meet requirements



Multi-level Integrity Verification:

- Explore optimal block (optBlk) considering diverse cross-layer tiling patterns;
- Calculate message authentication code of each optBlk (optBlk MAC);
- Aggregate layer MAC (model MAC) by XORing all optBlk MACs (layer MACs);

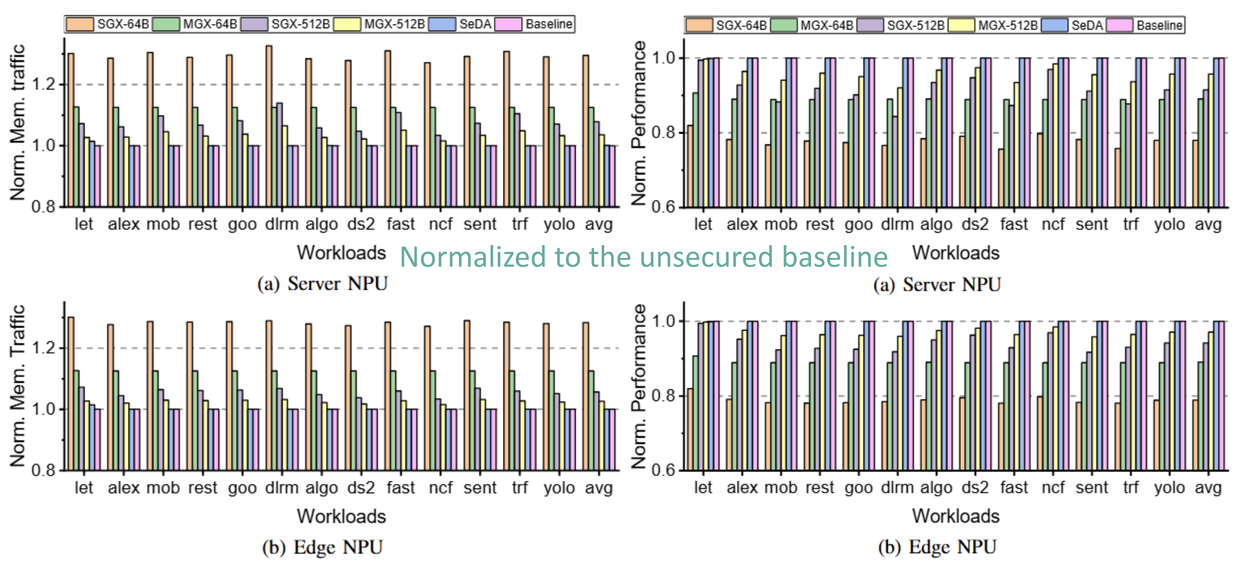


(a) Hardware optimization: bandwidth-aware encryption

(b) Software optimization: cross-layer-aware integrity verification

4. Evaluation

Through systematic experiments, SeDA is shown to mitigate performance overhead by over 12% for both server and edge NPUs, through the implementation of bandwidth-aware encryption and multi-level integrity verification framework.



Protection Scheme	Encryption Granularity	Integrity Granularity	Off-chip Memory Access	DNN Tiling Pattern	Encryption Scalability
SGX-64B	16B	64B	MAC,VN,IT	✗	✗
SGX-512B	16B	512B	MAC,VN,IT	✗	✗
MGX-64B	16B	64B	MAC	✗	✗
MGX-512B	16B	512B	MAC	✗	✗
SeDA	bandwidth-aware	multi-level	minimal to no cost	✓	✓

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