NCKU-ES
2020 IC contest
IC training

Lab 2

Multiply and Accumulation

Professor:Wen-Long Chin
TA: Jen-Hao Hsiao
、Kai-Chun Chang
、Yi-Teng Chang
、Yu-Tun Teng

VLSI signal processing LAB

Objectives

- To implement the basic circuits of DSP operation

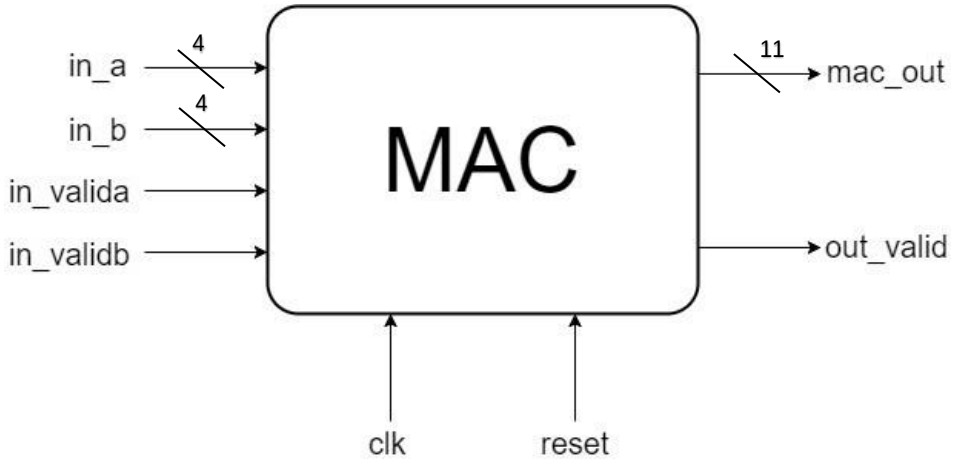
LAB contents

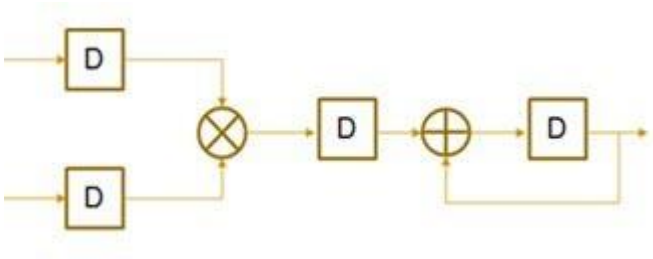
- LAB2: Multiply and Accumulation

Design Description

- Please design a Multiply and Accumulation(MAC) with two 4- bits inputs.

Block Diagram





Specifications

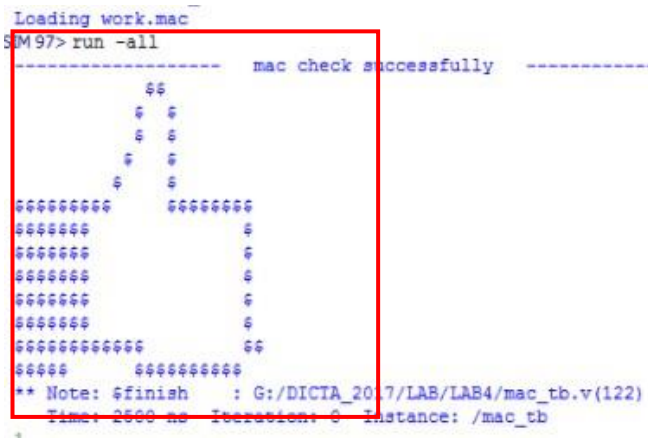
- Top module name : mac (File name: mac.v)
- Input pins: in_a[3:0], in_b[3:0], in_valida, in_validb, reset, clk
- Output pins: mac_out[10:0], out_valid
- All inputs and outputs are synchronized at clock positive edge.
- It is synchronous-reset architecture, both outs become 0 when the reset equal to 1.
- Note that in_a, in_b are 4-bits signed integer number. Please design the circuit without overflow.
- The two operands are valid when the control signals "in_valida" and "in_validb" are 1, respectively.
- After 8 MACs, output the result and assert the "out_valid" signal
- Note that two control signals are in a "one-to-one" manner, so you do not have to buffer the operands.

- In order to decrease the critical path, insert a retiming D-FF(introduce one more pipeline stage) at the output of the multiplier.

Note

- 本測驗提供測試程式(testbench)，各位同學之作業需能通過testbench的驗證

- 書面報告(report.doc）需包含：
  1. 設計原理(Design principle)
  2. 架構設計(Architecture)
  3. 波型(Waveform)分析
  4. 通過測試的截圖，如下



- 書面報告請勿手寫
- 評分標準依是否達到題目要求各事項，未達到要求依項扣分
- 繳交的作業資料夾組織與命名請與下頁圖示相同
- 作業繳交至 jfslmarco@gmail.com

- 截止日期: **2019/07/22(一)**

Directory Organization