

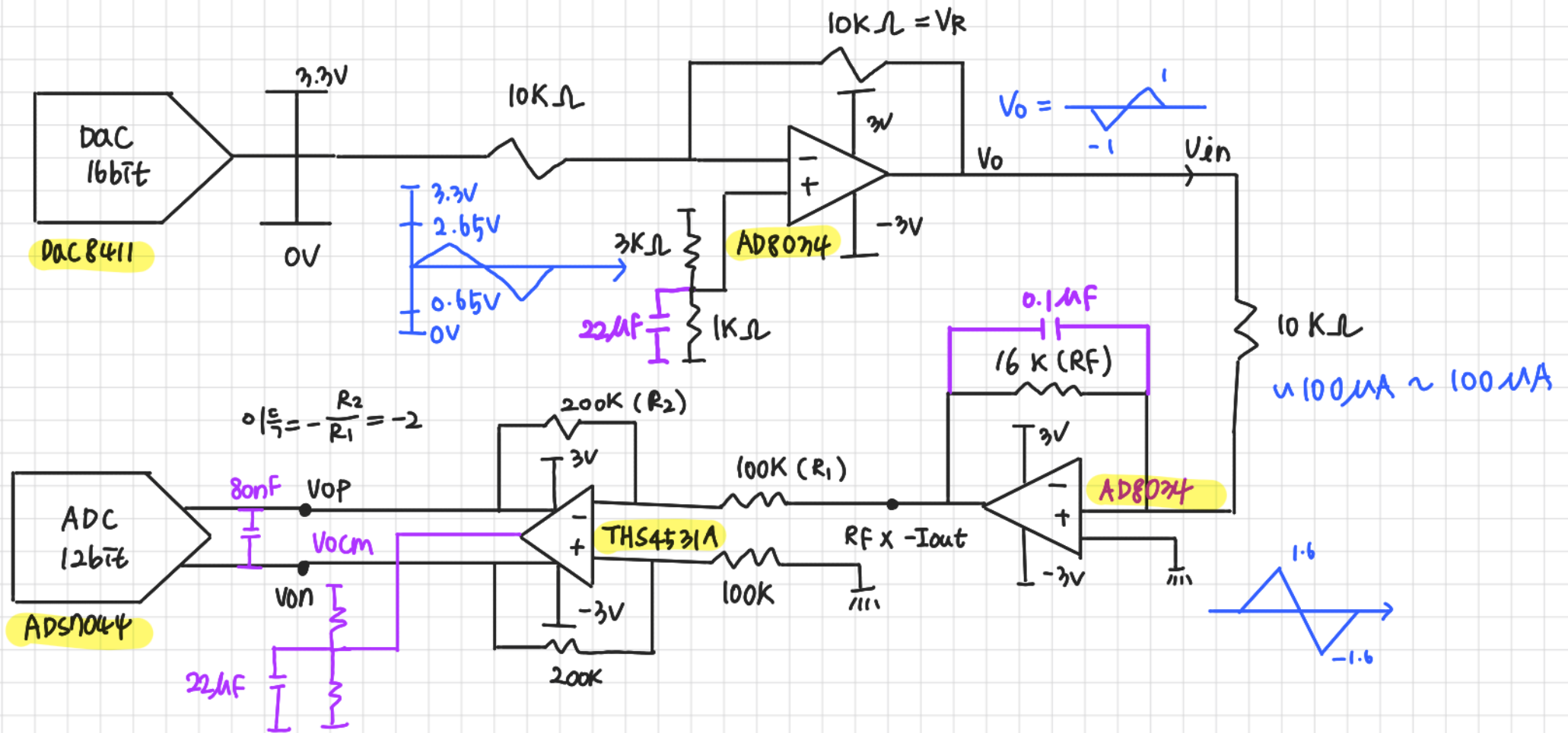
# C-mod bio-sensor 회로 정리

2025\_09\_02

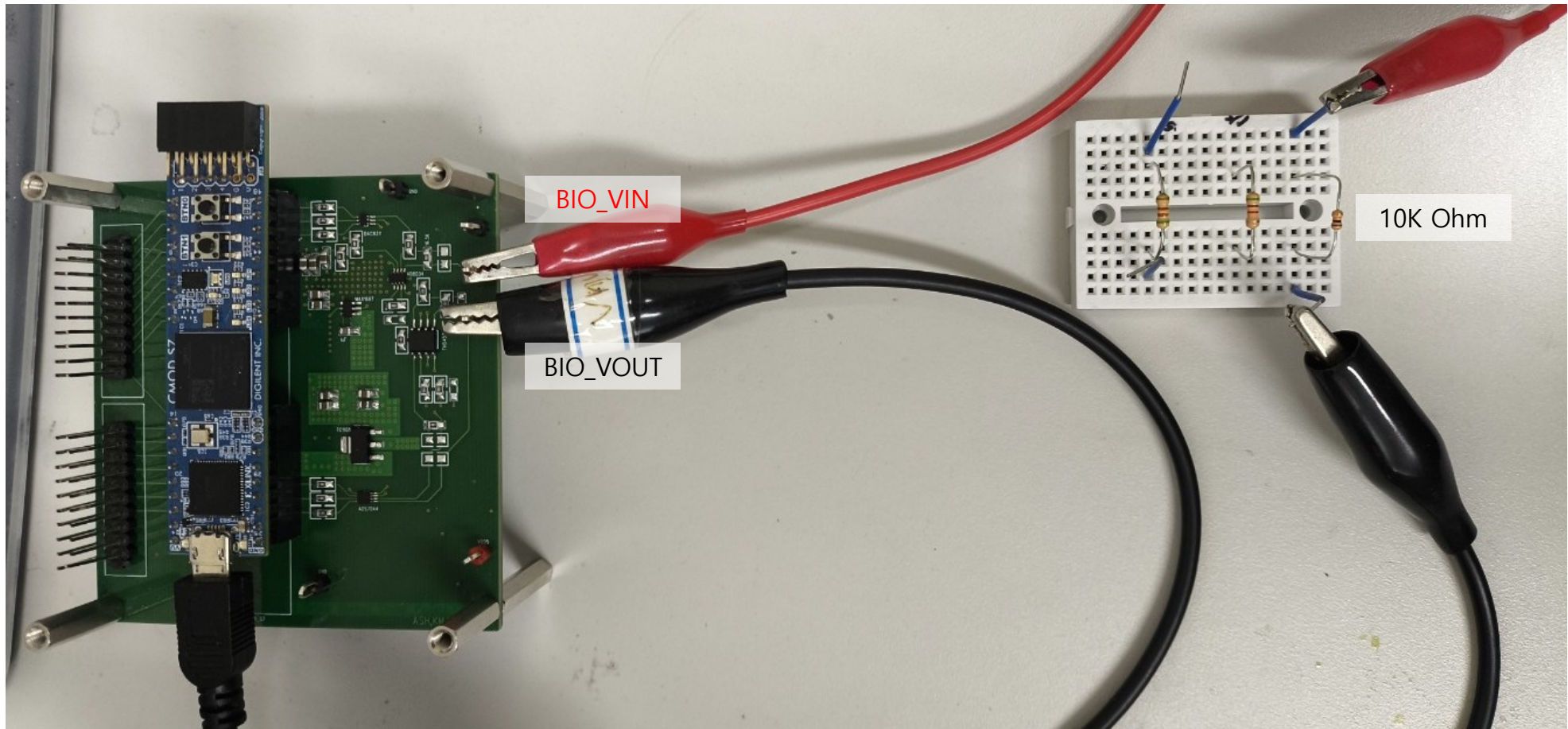
Verilog file : Project\_final0515

Python code : test\_CMOD\_UART FINAL0509.py

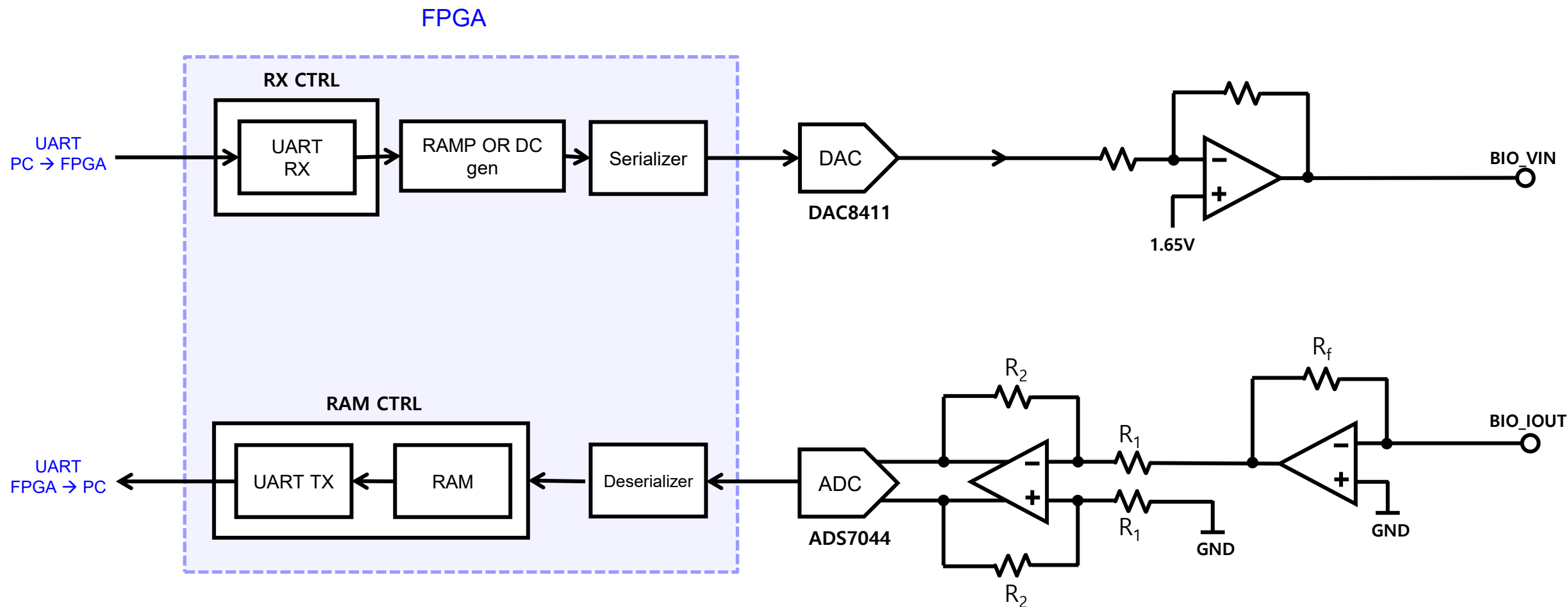
# 회로 구성



# 회로 연결



# Block diagram

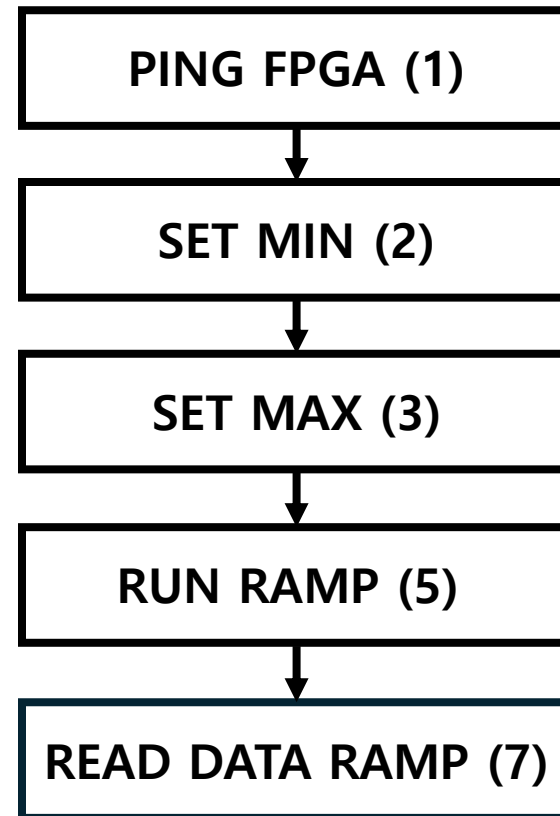


# 사용자 인터페이스 작동법

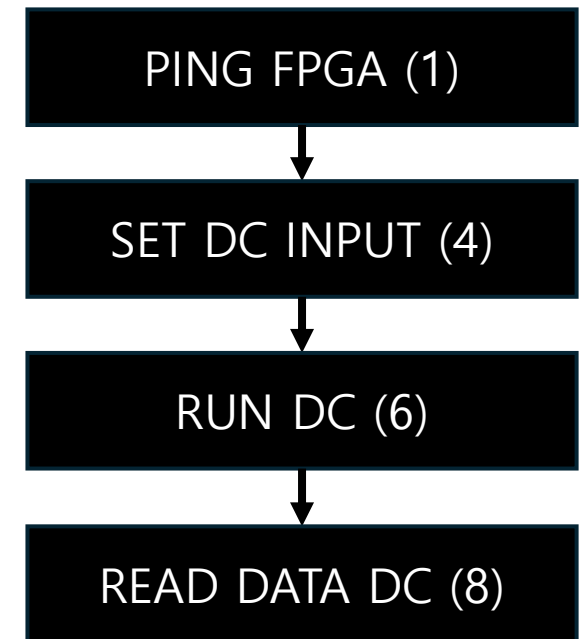
```
while True:
    try:
        menu = []
        while menu != 9 :
            print('#####')
            print('##### Menu #####')
            print('#####')
            print('1. Ping FPGA')
            print('2. Set min')
            print('3. Set max')
            print('4. Set DC Input')
            print('5. Run Ramp')
            print('6. Run DC')
            print('7. Read Data Ramp')
            print('8. Read Data DC')
            print('9. Exit')

            menu = int(input("Choose number: "))
```

RAMP 작동법 (파형)



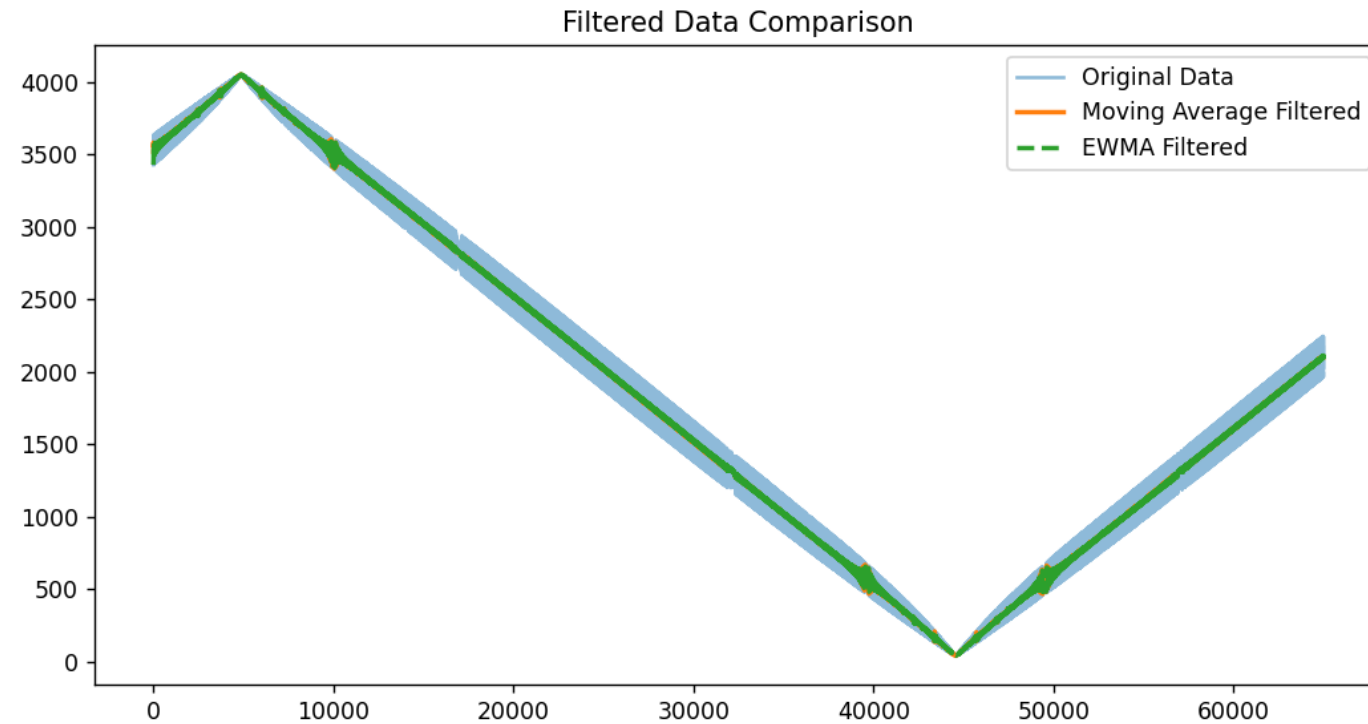
DC 작동법 (임피던스)



# 파이썬 결과

SET\_MIN 12900 →

SET\_MAX 52600



# 시뮬레이션으로 파형 보기 최적화

**SET\_MIN 30000 →**

**SET\_MAX 35000**

