toplevel Project Status			
Project File:	lissajous.xise	**Parser Errors:**	No Errors
Module Name:	toplevel	**Implementation State:**	Synthesized
Target Device:	xc3s500e-4fg320	• **Errors:**	No Errors
Product Version:	ISE 13.4	• **Warnings:**	18 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	197	4656	4%
Number of Slice Flip Flops	144	9312	1%
Number of 4 input LUTs	334	9312	3%
Number of bonded IOBs	15	232	6%
Number of BRAMs	4	20	20%
Number of MULT18X18SIOs	2	20	10%
Number of GCLKs	1	24	4%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Aug 28 00:18:26 2012	0	18 Warnings (0 new)	3 Infos (0 new)
Translation Report	Out of Date	Mon Aug 20 22:21:54 2012	0	0	0
Map Report	Out of Date	Mon Aug 20 22:22:09 2012	0	0	3 Infos (3 new)
Place and Route Report	Out of Date	Mon Aug 20 22:22:38 2012	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing	Out of	Mon Aug 20 22:22:43	0	0	6 Infos (6

Report	Date	2012			new)
Bitgen Report	Out of Date	Mon Aug 20 22:22:52 2012	0	0	0

Secondary Reports		[-]
Report Name	**Status**	**Generated**
WebTalk Report	Out of Date	Mon Aug 20 22:22:53 2012
WebTalk Log File	Out of Date	Mon Aug 20 22:23:42 2012

Date Generated: 08/28/2012 - 00:22:05