

# Will Buziak

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## Education

**Colorado School of Mines**  
M.S. Computer Science

Expected Graduation:  
May 2026

**University of Tennessee, Knoxville**  
B.S. Mechanical Engineering  
Minor Computer Science

Graduation Date:  
May 2024

## Experience

**Computer Architecture Design**  
**Bahar Lab**  
**Graduate Research Assistant**

Golden, CO  
**Aug 2024 - Present**

- Secure Memory Architecture Design and Development for RISC-V Trusted Execution Environments
- Modify, implement and verify RISC-V instructions within a simulated environment

**Neuromorphic**  
**Computing (TENNLab)**

**Undergraduate Research Assistant**

Knoxville, TN  
**Dec 2022 – Aug 2024**

- Mathematical Modeling for Dual Fuel Diesel-Ammonia Combustion Engines in a collaborative project with Oak Ridge National Research Lab (ORNL)
- Embedded computing and control applications using spiking neural networks within the TENNLab neuromorphic framework
- Robotic design for swarming robotics applications

**Electrochemical Energy**  
**Conversion and Storage Lab (EESCL)**

**Undergraduate Research Assistant**

Knoxville, TN  
**Aug 2022 – May 2024**

- Computational Fluid Dynamics (CFD) Modeling of two-phase flow for hydrogen electrolyzer research applications
- Web development for interactive dynamic data visualization tools
- Design a user interface for energy storage and power delivery system requirements

**Eck-Lectric Ind.**  
**Mechanical Engineering Intern**

Knoxville, TN  
**Oct 2022-Dec 2022**

- Assist in original product design for patent development

**Shaw Ind.**  
**Process Engineering Co-op**

Dalton, GA  
**May 2022 – Aug 2022**

- Process improvement projects in a manufacturing environment focusing on waste management, safety and process optimization

## Awards

EnergyTech University Prize 2023 Bonus Prize finalist (Eck-Lectric)

## Computer Skills

C/C++ | Python | Java | MATLAB | Solidworks/Onshape | Linux/Unix | Git | Raspberry Pi | Shell Scripting  
HTML/CSS | RISC-V | SLURM | SIMD | gem5 | QEMU | Qiskit | Verilog / SystemVerilog | Rust