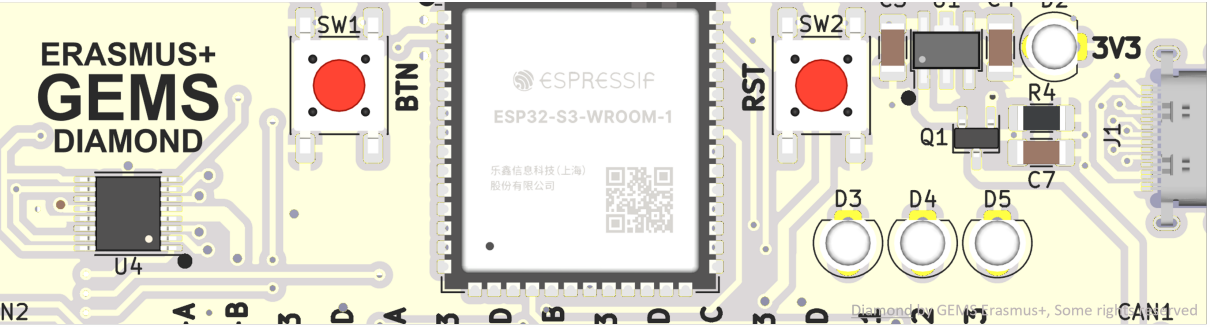

Tutorial 4

Design Considerations for Power Converters

Dr. ir. Sachin Yadav
DCE&S, ESE, TU Delft

TU Delft

1. Parasitics Influencing Switching in a Half Bridge
2. Gate Driver Circuits
3. PCB layout - good practices

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A Typical DC Motor Drive

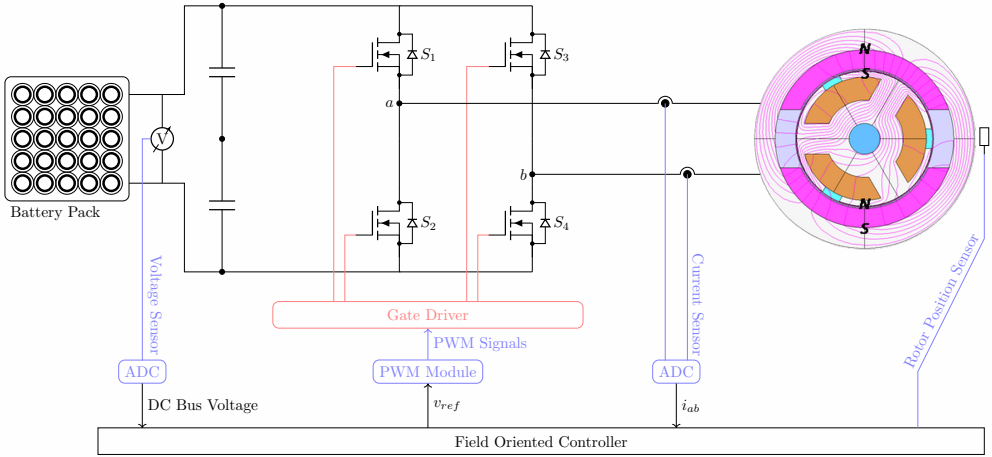


Figure: A typical DC motor drive.

Parasitics in a half-bridge

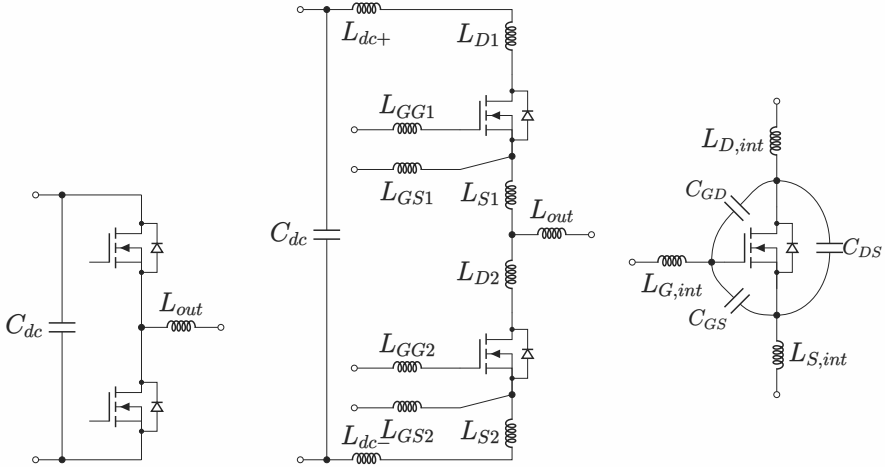


Figure: Parasitics in a half bridge.

Layout dependent inductance

Several sources of layout dependent parasitic inductances:

- DC link capacitors to the switches.
- Connection between the switches.
- Gate source connection with gate drivers.

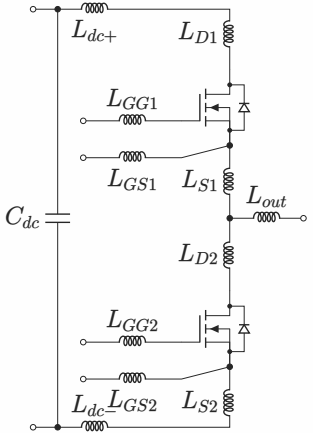


Figure: Layout dependent parasitics in a half bridge.

Layout dependent inductance

Reducing $\mathrm{L_{dc+}}$ and $\mathrm{L_{dc-}}$ using decoupling capacitors place close to the half bridge stage.

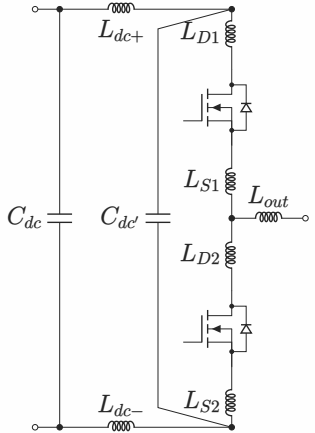
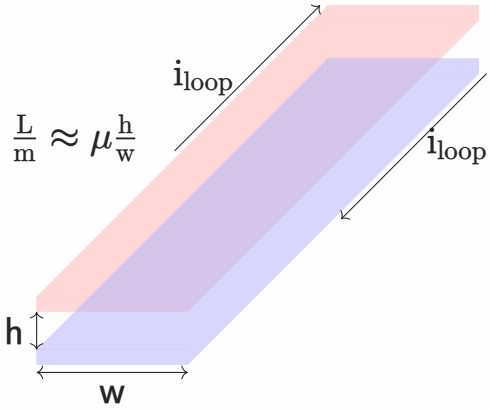


Figure: Using decoupling capacitors to reduce impact of $\mathrm{L_{dc+}}$ and $\mathrm{L_{dc-}}$.

Layout dependent inductance



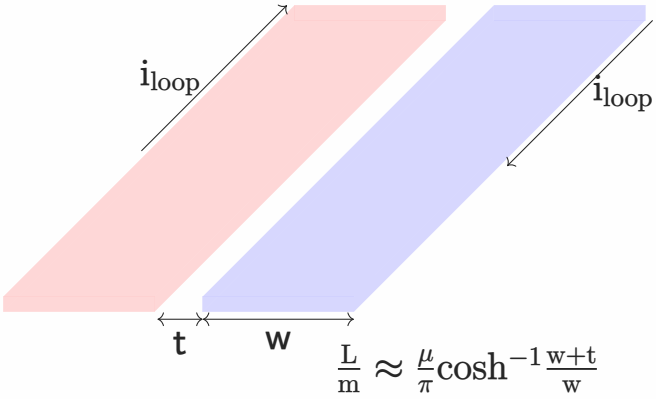


Figure: Parallel plate vs co-planar inductance [1].

Package dependent parasitics

- Parasitic capacitances
- Parasitic inductances

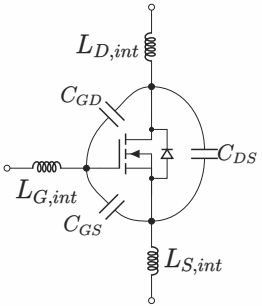


Figure: Parasitics in a typical MOSFET package.

Package dependent parasitics

Module

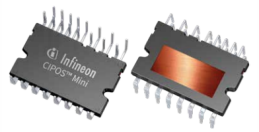


Figure: Semiconductor modules. Source: [2].

Discrete

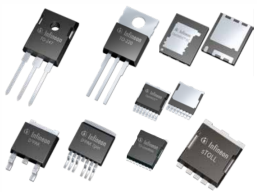


Figure: Discrete semiconductor packages. Source: [2].

Integrated

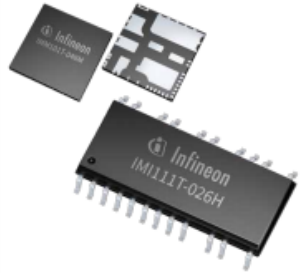


Figure: Intelligent power modules. Source: [2].

Package dependent parasitics

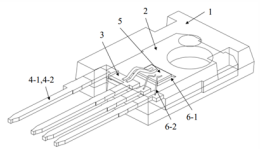


Figure: TO-247-4L [3].

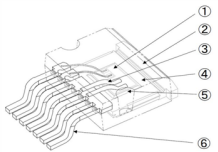


Figure: TO-263-7L [4].

Table: Loop inductance for different packages [5].

Package	Loop inductace [nH]
TO-247-4	≈15
TO-263-7	≈9

Parasitic capacitances

- C_{GS} determines how fast the switch starts conducting current.
- C_{GD} determines how fast the switch voltage changes.
- C_{DS} determines the losses incurred at turn-on. The energy stored in C_{DS} is lost when switch is shorted at turn on.

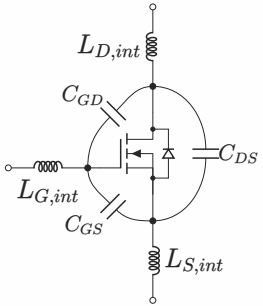


Figure: Package parasitics.

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3. PCB layout - good practices

HB gate driver - common elements

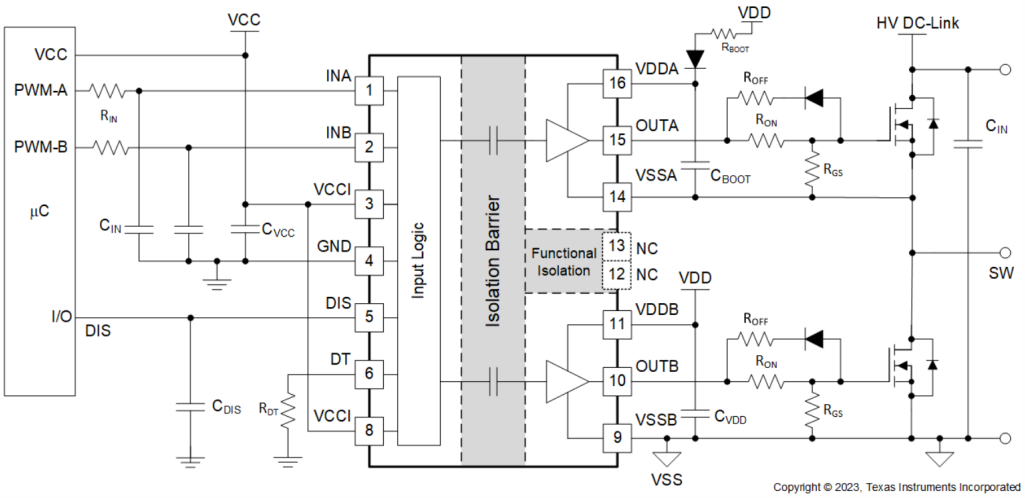

Figure: Common elements in a gate driver circuit. Source: [6].

HB gate driver - supply types

- Isolated supply.

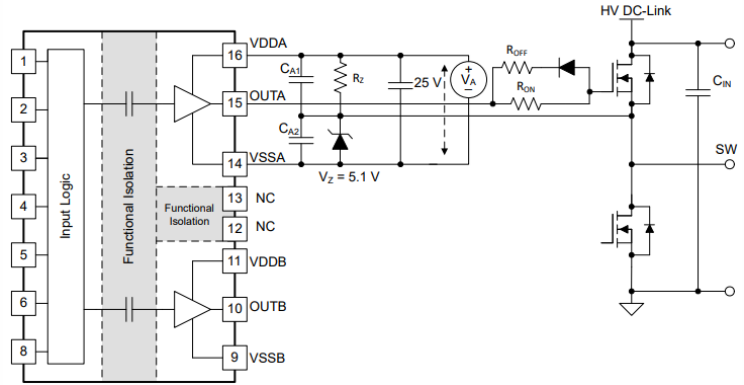

Figure: Gate driver using isolated supply. Source: [6].

HB gate driver - supply types

- Isolated supply.
- Bootstrap supply.

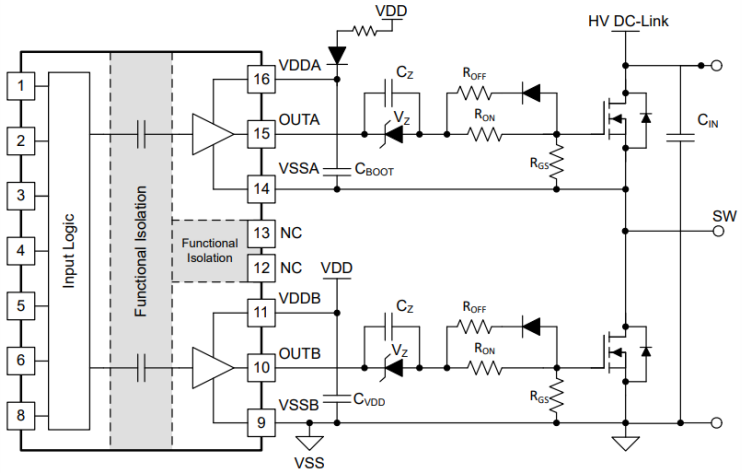

Figure: Gate driver using bootstrap supply. Source: [6].

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PCB layout - good practices

Some practices to improve circuit performance and EMI [7]:

- For high-frequency designs, try to use at least four layers.

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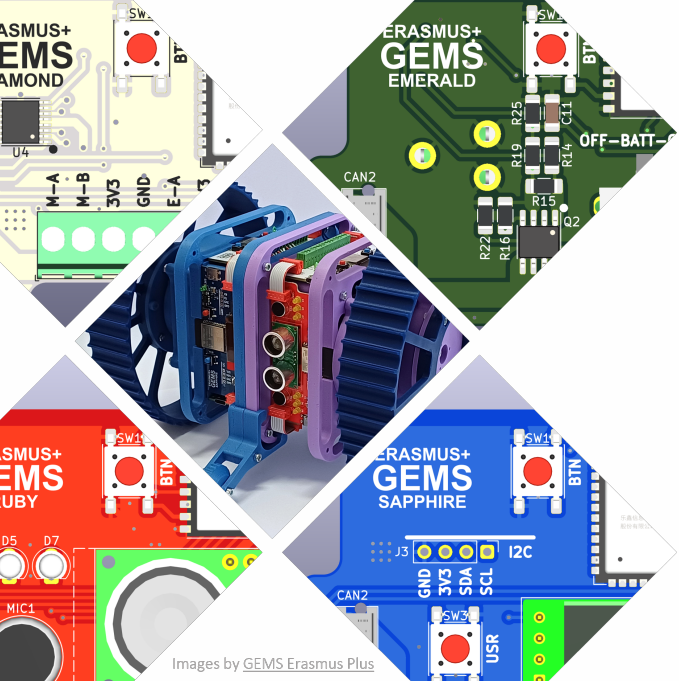
- Reduce loop area as much as possible -> Keep high di/dt components close.
- Place bypass capacitors as close as possible to the components.
- Never cut ground below/above a signal/power path. More info -> [9].

Conclusion

- Parasitics in a half bridges.
- Gate driver circuits.
- Review of good layouting practices.



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