A09 Softcore Processor

Episode 8b

Final Sequencer

Control Matrix

Episode 8a

Sequencer

- What guides us in our Model
  - ISA
- The instructions are the Key
  - Define the sequences
- Instruction Fetch Cycle

Episode 8a

Chores

- Modify **Memory** Initialization
  - Program loading
- Write Programs
  - **NOP**, **HLT**…
- **Decode** statement

Episode 8a

Everything

- CPU
- Test Bench
- Assembly Code
- Makefile
- Decode case with
  - NOP
  - HLT

Episode 8b

Synthesis

- Finish Instructions
- **Synthesis**

Episode 8b

Review

- Build **CPU** module
- Build **Top** module
- rom_memory.v (**new**)
  - No stuff -- no memory
    - yosys log
    - next-pnr log
- Makefile
- pin.pcf

Episode 8b

Backtracking in the woods

- Add a “**reg**” variable
- Assign a default value
- Route signal to output

Episode 8b

Instructions

- Branch not Equal (**BNE**)
- Shift Left Logical (**SHL**)
- Shift Right Logical (**SHR**)
- Addition (**ADD**)
- Subtraction (**SUB**)
- Compare (**CMP**)

Episode 9

End of the Road

- Source on Github
- Wrapup
- The Future

Episode Finale

The roads ahead