**Odd Counter code**

module odd\_counter(

input wire clk,

input wire reset,

output logic [7:0] od\_counter

);

logic [7:0]next\_cnt;

always\_ff @(posedge clk or posedge reset)

if(reset)

od\_counter <= 8'h1;

else

od\_counter <= next\_cnt;

assign next\_cnt= od\_counter + 2'h2;

endmodule

**Test Bench Code**

module tb\_od\_counter();

logic clk,reset;

logic [7:0] od\_counter;

odd\_counter day5(.\*);

always begin

clk= 1'b0;

#5;

clk=1'b1;

#5;

end

initial begin

reset <= 1'b1;

@(posedge clk);

@(posedge clk);

reset <= 1'b0;

for (int i=0;i<128;i++)

@(posedge clk);

$finish();

end

initial begin

$dumpfile("day5.vcd");

$dumpvars(0, tb\_od\_counter);

end

endmodule