**LFSR code**

module lfsr(

input wire clk,

input wire reset,

output wire [3:0]lfsr\_o

);

logic [3:0]lfsr\_ff;

logic [3:0]nxt\_lfsr;

always\_ff @(posedge clk)

if(reset)

lfsr\_ff <= 4'hE;

else

lfsr\_ff <= nxt\_lfsr;

assign nxt\_lfsr = {lfsr\_ff[2:0], lfsr\_ff[1]^lfsr\_ff[3]};

assign lfsr\_o=lfsr\_ff;

endmodule

**Test Bench Code**

module tb\_lfsr();

logic clk;

logic reset;

logic [3:0] lfsr\_o;

lfsr DAY7 (.\*);

always begin

clk = 1'b1;

#5;

clk = 1'b0;

#5;

end

initial begin

reset <= 1'b1;

@(posedge clk);

reset <= 1'b0;

for (int i=0; i<32; i=i+1)

@(posedge clk);

$finish();

end

initial begin

$dumpfile("day7.vcd");

$dumpvars(2, tb\_lfsr);

end

endmodule

**Simulation**

