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Time Warp Simulation on Multi-core Processors and Clusters

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Discrete Event Simulation

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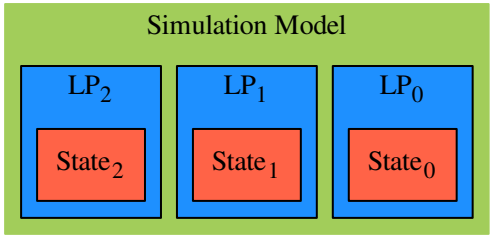
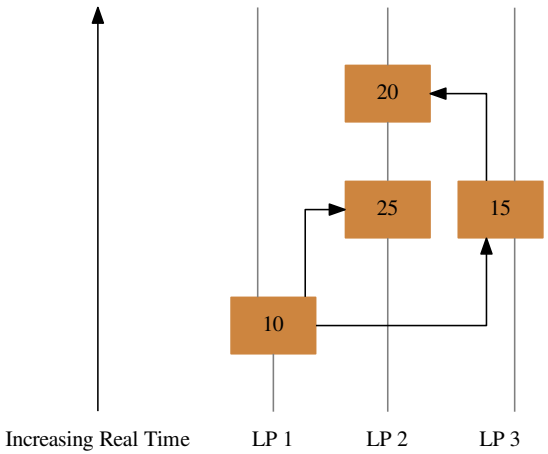
- Three main components
  - State variables
  - Simulation clock
  - Pending event set
- Unprocessed events stored in pending event set
- Events processed in time stamp order
- Simulation clock and state variables updated only when event occurs

Parallel Discrete Event Simulation



- Model system as a set of Logical Processes (LPs)
- No shared state between LPs
- Events exchanged between LPs

Possible Causality Violations



- Events can be received & processed out of order
- Two solutions
  - Conservative and Optimistic

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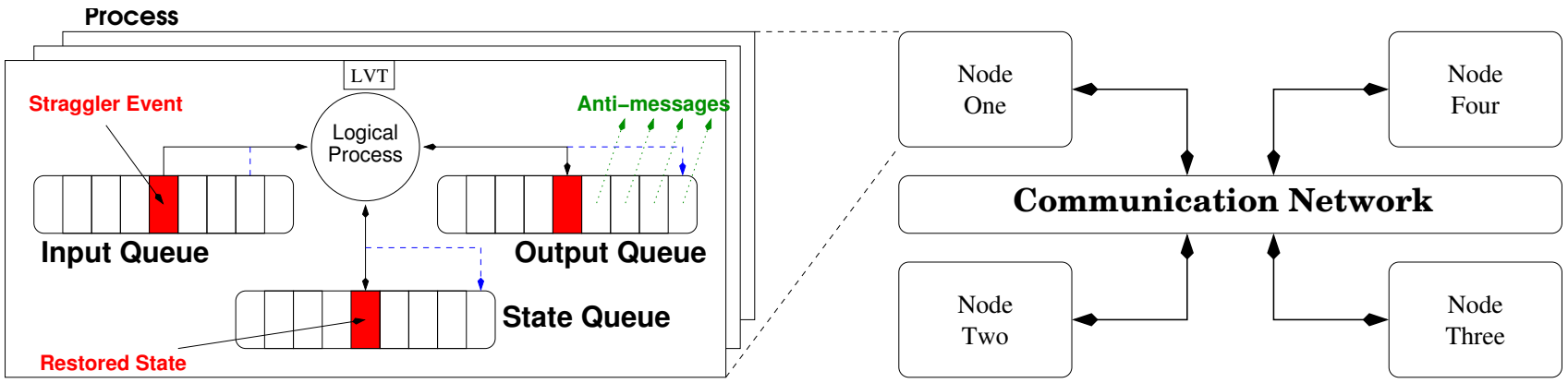
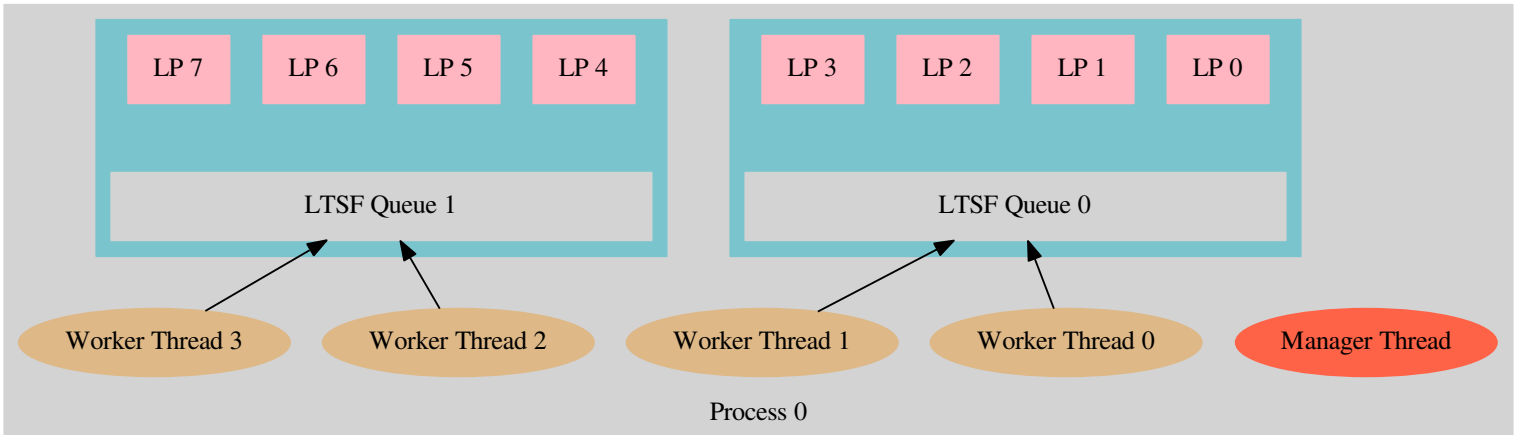
Optimistic Mechanism



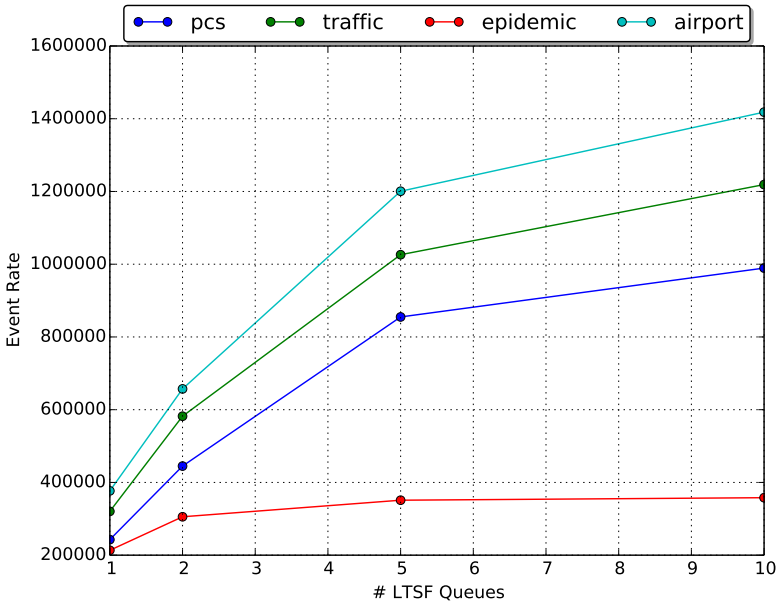
- Rollback Mechanism
  - State Restoration, Anti-Messages
- Local Virtual Time (LVT) & Global Virtual Time (GVT)
- Fossil Collection

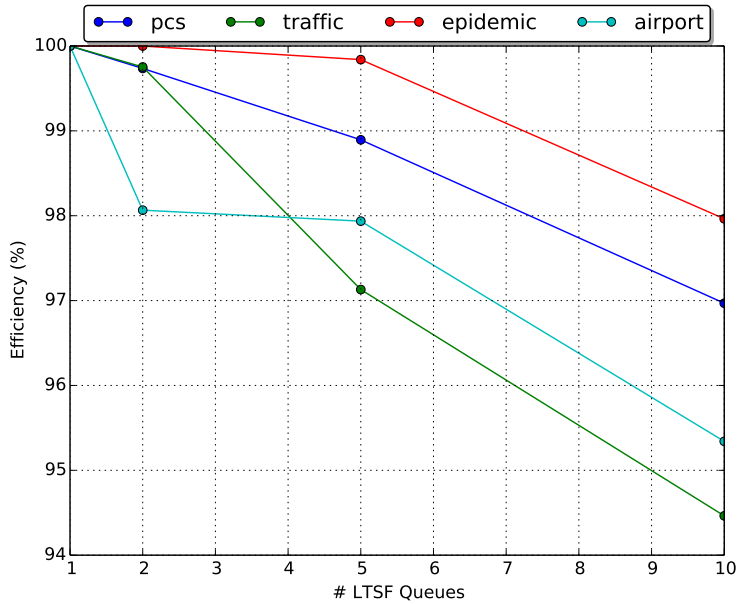
WARPED2 Process



- Worker Threads and Manager Thread
- LTSF Queues
- LP Partitioning
  - Processes
  - LTSF Queues

Sharing LTSF Queues





$$EventRate = \frac{CommitedEvents}{Runtime} \quad Efficiency = \frac{CommittedEvents}{ProcessedEvents} * 100\%$$

Reducing contention more important than reducing rollbacks

Partitioning

Round-Robin

Block

Periodic State Saving

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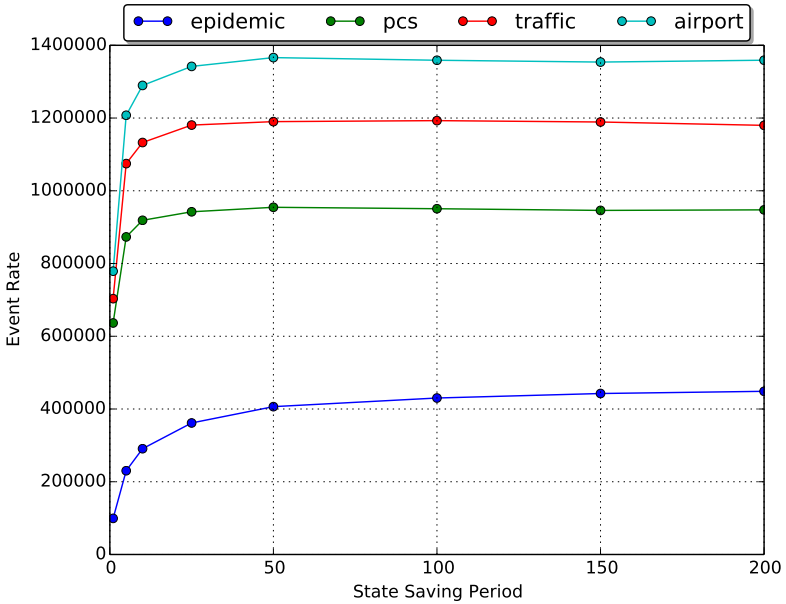
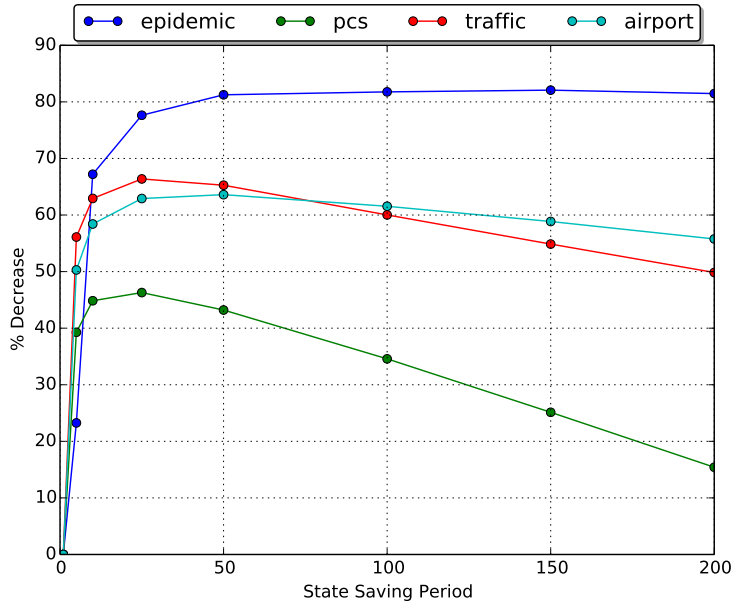
Save state only once every *N* events

- Not all states available to roll back to
- Must ”Coast Forward” to reproduce state
- Decrease time to copy states and reduce memory footprint
- Increase rollback time

SMP Machine - Intel® Xeon® X5675





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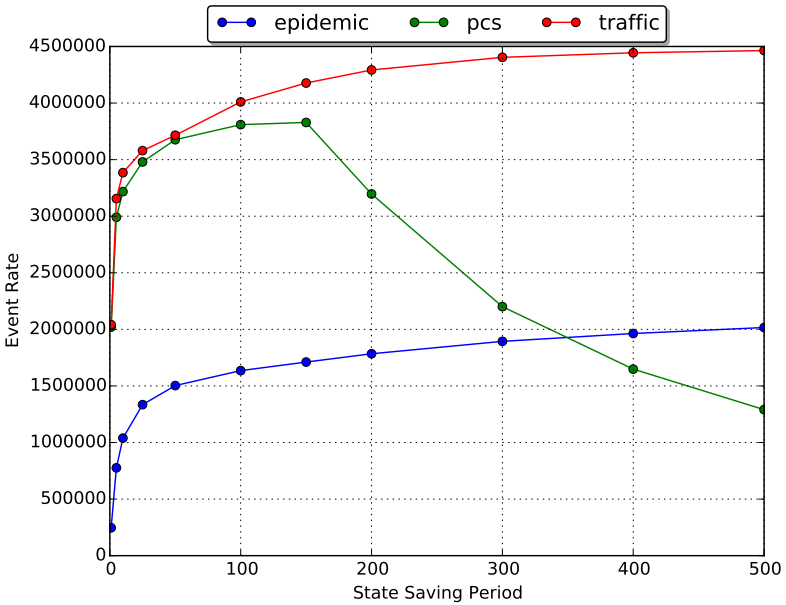
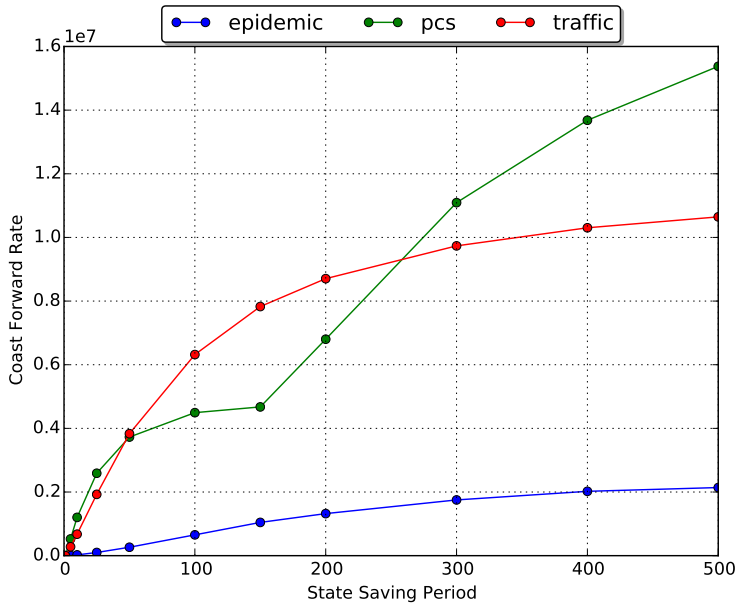
8 Node Cluster - Intel® Xeon® E5410





$$CoastForwardRate = \frac{CoastForwardEvents}{Rollbacks} * RollbackRate$$

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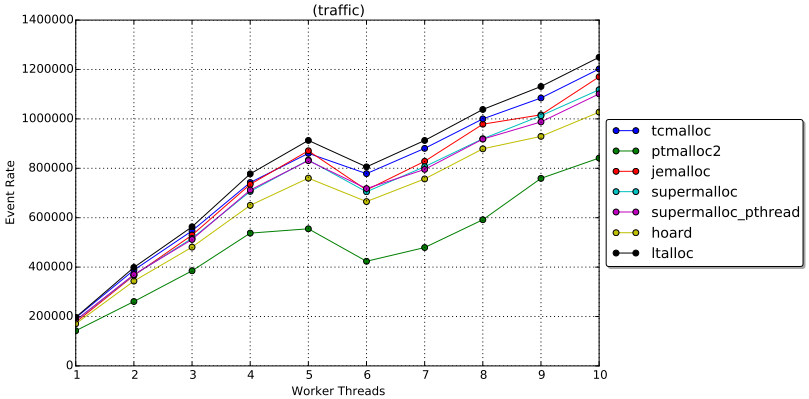

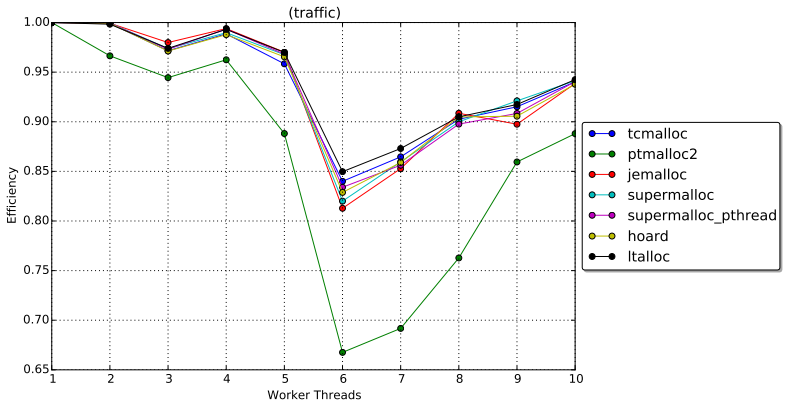

- ptmalloc2 default in GLIBC

Message Aggregation