Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal(M.P.)

Scheme of Examination

Third Semester- Master of Engineering

(Embedded System and VLSI Design,Micro electronics and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End. Sem. Exam.	Tests (Two)	Assign ments /Quiz	End. Sem. Practical /Viva	Practical Record/ Assignm ent/Quiz /Present ation	
1.	MEVD-301	Elective I	3	1	-	4	70	20	10	-	-	100
2.	MEVD-302	Elective II	3	1	-	4	70	20	10	-	-	100
3.	MEVD-303	Seminar	-	-	4	4	-	-	-	-	100	100
4.	MEVD-304	Preliminary Dissertation cum Synopsis	-	-	8	8	-	-	-	120	80	200
		Total	6	2	12	20	140	40	20	120	180	500

L: Lecture - T: Tutorial - P: Practical

w.e.f. July-2010

MEVD 301 Elective -I	
(A)	Opto-Electronics Integrated Circuits
(B)	System On Chip (SOC) Design

MEVD 302 Elective -II	
(A)	Communication RF IC Design
(B)	Embedded System Programming