

Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal (M.P.)

Scheme of Examination

Second Semester- Master of Engineering

(Embedded System and VLSI Design, Micro electronics and VLSI Design)

S.No.	Subject	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
	Code											
							End.	Tests	Assign	End.	Practical	
							Sem.	(Two)	ments	Sem.	Record/A	
			L	Т	P		Exam.		/Quiz	Practical/	ssignmen	
				1	•					Viva	t/Quiz/Pr	
											esentatio	
1	MEMO	VI CI Ta alama la mi	2	1		4	70	20	10		n	100
1.	MEVD- 201	VLSI Technology	3	1	ı	4	70	20	10	-	-	100
2.	MEVD-	Real Time	3	1	-	4	70	20	10	-	-	100
	202	Operating System										
3.	MEVD-	VLSI Test and	3	1	-	4	70	20	10	-	-	100
	203	Testability										
4.	MEVD- 204	Microelectronics	3	1	-	4	70	20	10	-	-	100
5.	MEVD-	Embedded	3	1	-	4	70	20	10	-	-	100
	205	Computing System Design										
6.	MEVD-	Lab-III	-	-	6	6	-	-	-	90	60	150
	206	Real Time										
		Operative System										
7.	MEVD-	Lab-IV	-	-	6	6	-	-	-	90	60	150
	207	VLSI Technology										
		Total	15	5	12	32	350	100	50	180	120	800