

Design a Mealy sequential circuit which investigates an input sequence X and which will produce an output of $Z = 1$ for any input sequence ending in 1010, provided that the sequence 001 has occurred at least once.

Example:

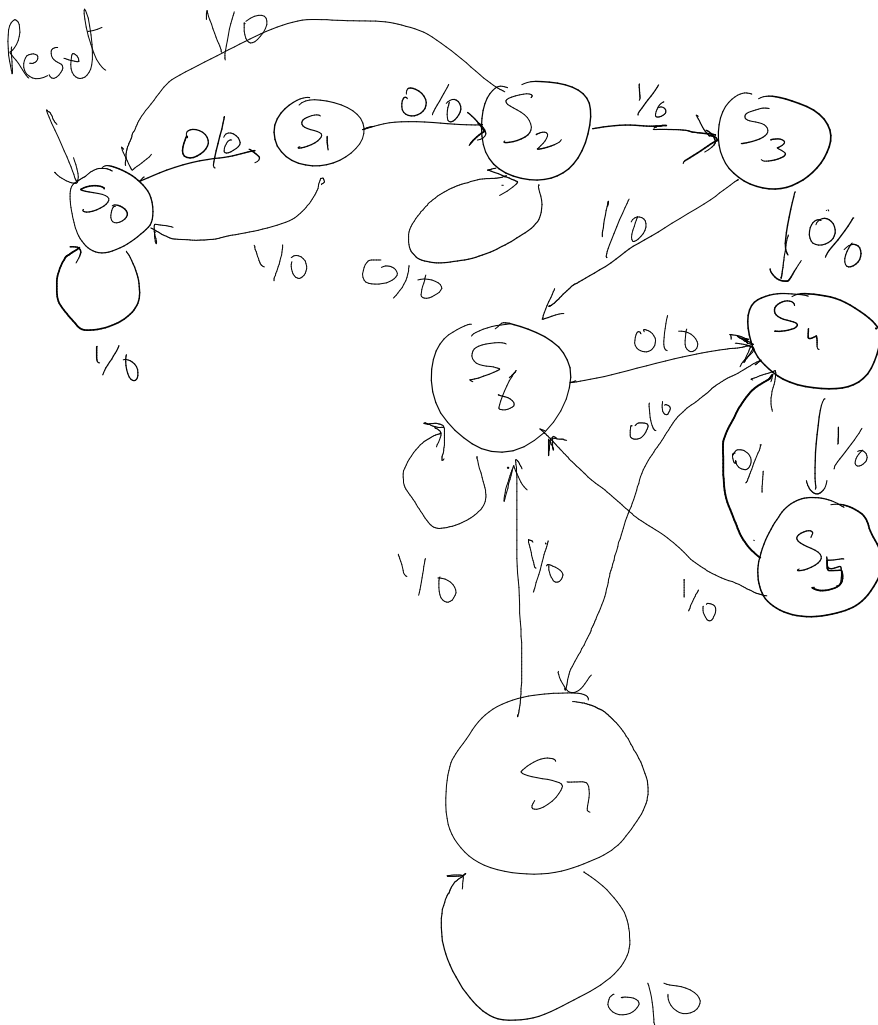
$X = 10100101010$
 $Z = 00000000101$

Notice that the circuit does not reset to the start state when an output of $Z = 1$ occurs.

Problem 1. Complete the following state diagram. You can also choose to draw state diagram from scratch. Also fill the state transition table. (20 marks)

$x \rightarrow x$
 $xx \rightarrow 1$
 $x10$
 101

$A=0$ "001" has not occurred
 $A=1$ "001" has occurred



$S_0 = \{A=0, () \text{ empty seq}\}$

$S_1 = \{A=0, "0"\}$

$S_2 = \{A=0, "00"\}$

$S_3 = \{A=1, "001"\}$

$S_4 = \{A=1, "x10"\}$

$S_5 = \{A=1, "101"\}$

$S_6 = \{A=1, "xx1"\}$

$S_7 = \{A=1, "xxx"\}$

	Present State	Next State		Output (z)	
		X=0	X=1	X=0	X=1
"xx"	S_0	S_1	S_0	0	0
"x0"	S_1	S_2	S_0	0	0
"x00"	S_2	S_2	S_3	0	0
"xx1"	S_3	S_4	S_3	0	0
"x10"	S_4	S_7	S_5	0	0
"101"	S_5	S_4	S_3	1	0
"xx1"	S_6	S_4	S_3	0	0
"x00"	S_7	S_7	S_3	0	0

1	S_0						
2	S_1	1					
3	S_2	1	2				
4	S_3	X	X	X			
5	S_4	X	X	X	X		
6	S_5	X	X	X	X	X	
7	S_7	1	2	2	X	X	X
		S_0	S_1	S_2	S_3	S_4	S_5

$S_3 \equiv$ because
 $S_4 \neq$ because
 $S_5 \neq$

Problem 2. The above state table can be reduced to only 7 states instead of 8 states. Reduce the states by row-reduction method. You can also use implication table but that will take longer. Only specify which states are equivalent to each other. You do not need to write the state table again. (10 marks)

$$S_3 \equiv S_6$$

Present State		Next State		Output(z)	
		X=0	X=1	X=0	X=1
"xx"	S_0	S_1	S_0	0	0
"x0"	S_1	S_2	S_0	0	0
"x00"	S_2	S_2	S_3	0	0
"xx1"	S_3	S_4	S_3	0	0
"x10"	S_4	S_7	S_5	0	0
"101"	S_5	S_4	S_3	1	0
"xx1"	S_6	S_4	S_3	0	0
"x00"	S_7	S_7	S_3	0	0

1	S_0						
2	S_1	X					
3	S_2	X	X				
4	S_3	X	X	X			
5	S_4	X	X	X	X		
6	S_5	X	X	X	X	X	
7	S_7	X	X	X	X	X	X
		S_0	S_1	S_2	S_3	S_4	S_5

$S_3 \equiv S_6$ because
 $S_4 \not\equiv S_5$ because
 $S_5 \not\equiv S_7$

Problem 3. (State assignment).

Using the guideline method find the groups of states that should be grouped together. Draw the state assignment map. Assign a 3-bit state encoding to the 7 states in the reduced state table derived in Problem 2. (20 marks).

$$G1: (s_0, s_7), (s_3, s_5, s_7), (s_3, s_5), (s_1, s_2)$$

$$G2: (s_0, s_1), (s_0, s_2), (s_2, s_3), (s_3, s_4)^{\times 2}, (s_5, s_7), (s_3, s_7)$$

y_2			
s_1 ⁰	s_0 ²	s_7 ⁶	s_4 ⁴
s_2 ¹	s_3 ³	s_5 ⁷	s_6 ⁵
y_1			

y_2	y_1	y_0	
0	0	0	s_1
0	0	1	s_2
0	1	0	s_0
0	1	1	
1	0	0	s_4
1	0	1	s_3
1	1	0	s_7
1	1	1	s_5

Problem 4. The following state-assigned table is given. Find the boolean expressions for inputs J_2 and K_2 to a J-K flip flop that implements the transition from Present state y_2 to Next state Y_2 . Express J_2 and K_2 in terms of input X and present state y_2 , y_1 and y_0 (20 marks).

Present State			Next state						Output	
			X=0			X=1			X=0	X=1
y_2	y_1	y_0	Y_2	Y_1	Y_0	Y_2	Y_1	Y_0	Z	Z
0	0	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	1	1	0	1	0
0	1	1	d	d	d	d	d	d	d	d
1	0	0	1	1	0	1	1	1	1	0
1	0	1	1	0	0	1	0	0	1	0
1	1	0	1	1	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0

y_2 X

0	1	1	0
0	1	1	0
d	1	1	d
0	1	1	1

y_1 y_0

y_2 Y_2 J_2 K_2

0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

$J_2 = x y_1$

y_2 X

0	d	d	0
0	d	d	0
d	d	d	d
0	d	d	1

y_1 y_0

$K_2 = 0$

y_2 X

d	0	0	d
d	0	0	d
d	0	0	d
d	0	0	d

y_1 y_0