Logic minimization: Minimum-cost circuits

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1 A few more Boolean problems

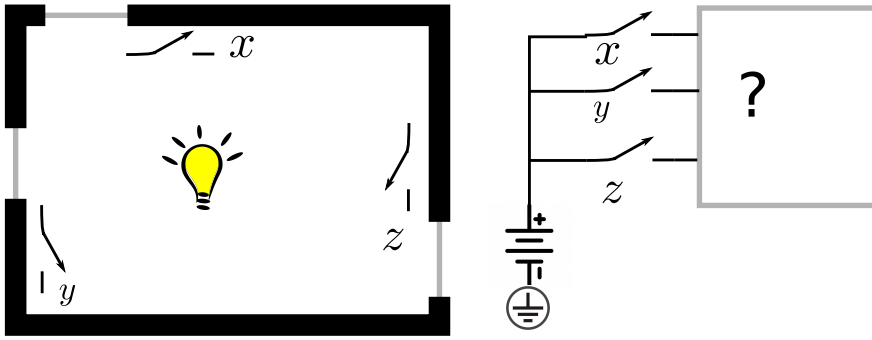
Example 1. *Simplify the following Boolean expression:*

$$f = x_1\bar{x}_3\bar{x}_4 + x_2\bar{x}_3\bar{x}_4 + x_1\bar{x}_2\bar{x}_3$$

Example 2. *Using algebraic manipulation to prove that:*

$$x + yz = (x + y)(y + z)$$

Example 3. *Design a three-way light control*



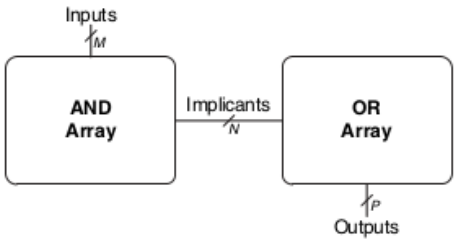
2 Logic minimization

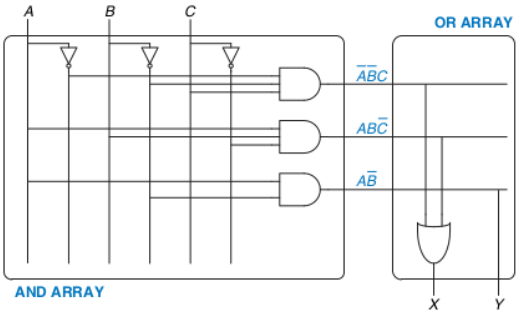
A general optimization criteria for multi-level logic are to Minimize some combination of:

1. Area occupied by the logic gates and interconnect;
2. the Critical Path Delay of the longest path through the logic;
3. the Degree of Testability of the circuit, measured in terms of the percentage of faults covered by a specified set of test vectors, for an appropriate fault model (Eg., single stuck faults, multiple stuck faults, etc.);
4. Power consumed by the logic gates.

In this course, we will start with two-level multi-input circuits and a criteria based on the number of gates/transistors/diodes.

3 Programmable Logic Arrays





4 Two-level circuits

The cost that we are going to consider in this class depend upon:

1. Number of gates.
2. Number of input to the gates.

More gates need more transistors, more area on the chip. More-inputs the gate need more transistors within each gate. Number of gate inputs can be considered secondary criterion to the number of gates.

Example 4. *Find the cost of the following Boolean expression* $X = \bar{A}\bar{B}C + AB\bar{C} + A\bar{B}$.