1 Syllabus covered

- ☑ Binary numbers, Hexadecimal, Sign-magnitude, One's-complement and Two's complement. Conversions between them.
    1. Homework 1 and Lectures 08/31 and 09/02.
- ☑ Generate minterms, maxterms, SOP canonical form and POS canonical forms and convert between them
    1. Lecture 09/09
- ☑ Understand and use the laws and theorems of Boolean Algebra
    1. Homework 2 and Lectures 09/16-09/19
- ☑ Perform algebraic simplification using Boolean algebra
    1. Homework 2 and Lectures 09/16-09/19
- ☑ Simplification using K-maps
    1. Homework 2 and 3 and Lectures 09/12-09/14
- ☑ Derive sum of product and product of sums expressions for a combinational circuit
    1. Homework 2 and 3 and Lectures 09/12-09/23
- ☑ Convert combinational logic to NAND-NAND and NOR-NOR forms
    1. Homework 3 and Lecture 09/28
- ☑ Simplification using Quine-McCluskey method
    1. Lecture 09/28
- ☑ Design combinational circuits for positive and negative logic
    1. For Negative logic is H = 0, L = 0. See Example 6, on lecture 10/19
- ☑ Design Hazard-free two level circuits.
    1. See Example 14, on lecture 10/24
- ☑ Compute noise margin of one device
    1. See Section 2 of lecture 10/17
- ☑ Describe how tri-state and open-collector outputs are different from totem-pole outputs.

1. See Definitions 11-13 covered in lecture 10/21

☑ Different between and limitations of level-triggered latches and edge-triggered flip-flops.

1. See lecture 10/26-10/28

☑ Analyze a sequential circuit and derive a state-table and a state-graph

☑ Understand the difference between synchronous and asynchronous inputs

☑ Derive a state graph or state table from a word description of the problem

☑ Implement a design using JK, SR, D or T flip-flops

☐ Compute fan out and noise margin of one device driving the same time

☐ Know the differences and similarities between PAL, PLA, and ROMs and can use each for logic design

☐ Design combinational circuits using multiplexers and decoders

☐ Reduce the number of states in a state table using row reduction and implication tables

☐ Perform a state assignment using the guideline method

☐ Analyse and design both Mealy and Moore sequential circuits with multiple inputs and multiple outputs

☐ Convert between Mealy and Moore designs

☐ Partition a system into multiple state machines