

# Sequential logic design

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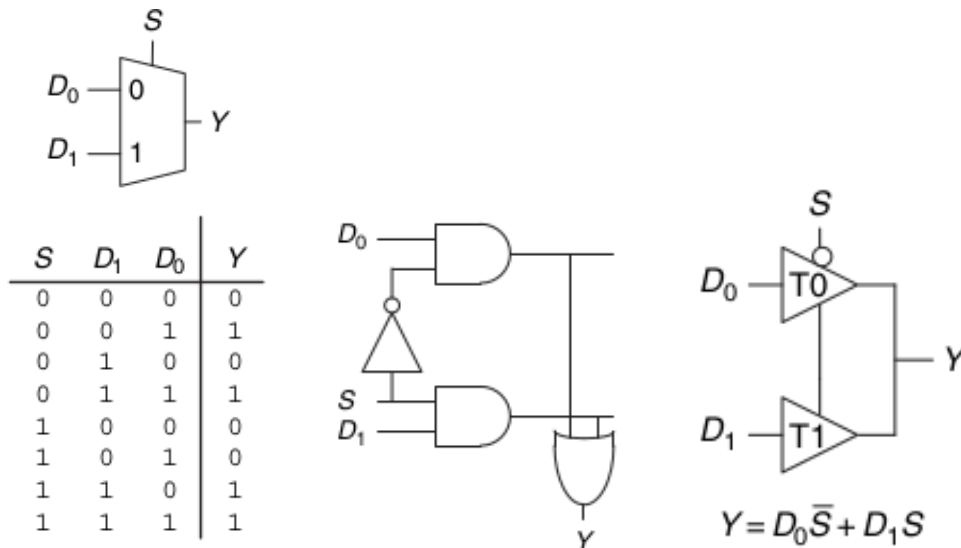
December 5, 2022

## 1 Objectives

1. Design combinational circuits using multiplexers and decoders

## 2 Design combinational circuit using multiplexers [1, Section 2.8.1]

### 2.1 Review: 2to1 Multiplexer (MUX)



### 2.2 Wider multiplexers

Draw the symbol for a 4:1 MUX, an 8:1 MUX and a  $2^N : 1$  MUX and write corresponding Boolean expressions.

**Example 1.** Design a circuit for  $Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$  using a 8:1 MUX.

**Remark 1.** A  $2^N : 1$  MUX can be used to program any  $N$ -input logic function.

**Example 2.** Design a circuit for  $Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$  using a 4:1 MUX and NOT gates only.

**Remark 2.** A  $2^{N-1} : 1$  MUX can be used to program any  $N$ -input logic function, if we use literals on the input side.

**Example 3.** Design a circuit for  $Y = \bar{A}C + \bar{A}B + B\bar{D}$  using a 8:1 MUX and NOT gates only. Also design using 4:1 MUX and other gates. fewest gates.

### 3 Encoders and Decoders

**Example 4.** Draw the symbol and the truth table for 2:4 decoder. Also write the logic expressions.

**Example 5.** Draw the symbol and the truth table for 3:8 decoder, 4:16 decoder and  $N : 2^N$  decoder. Also write the logic expressions.

**Example 6.** *Design a circuit for a XOR gate using a 2:4 decoder and an OR gate.*

**Example 7.** *Design a circuit for  $Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$  using a 3:8 decoder and an OR gate.*

### 3.1 Encoders

**Example 8.** *Draw symbol and truth table for a 4:2 priority encoder.*

**Example 9.** *Draw symbol and truth table for a 8:3 priority encoder.*

## References

- [1] Sarah L Harris and David Harris. *Digital design and computer architecture*. Morgan Kaufmann, 2022.