Homework 6

Max marks: 50 marks

Due on Oct 25th, 2021, 9 AM, before class.

Problem 1 *Show how the function* $f(w_1, w_2, w_3) = \sum m(0, 2, 3, 4, 5, 7)$ *can be implemented using a 3-to-8 binary decoder and an OR gate. [1, Prob 4.1] (10 marks)*

Problem 2 *Consider the function* $f = \bar{w}_2\bar{w}_3 + w_1w_2$*. Derive a circuit for* f *that uses only one 2-to-1 multiplexer and no other gates (assuming inputs are available in both uncomplemented and complemented form). [1, Prob 4.4](10 marks)*

Problem 3 *Figure 1 shows the notation for a BCD to 7-segment display and Table 1 shows the corresponding truth table. The inputs corresponding to the missing rows in the truth table should be considered as don't care.*

1. *implement segment "a" using an 8:1 mux and no other logic gate, (10 marks)*

2. *implement segment "a" using a 4:1 mux and one other gate, (10 marks)*

3. *implement segment "f" with 4:1 mux and no other logic gate. Assume inputs are available in both uncomplemented and complemented form. (Hint: There are* $({}^4C_2 = 6)$ *possible pairs of control inputs:* (w_3, w_2)*,* (w_2, w_1)*,* (w_1, w_0)*,* (w_0, w_3)*,* (w_0, w_2)*,* (w_1, w_3)*. There are 6 don't care conditions. With two control inputs of the multiplexer and one input allowed, you can represent an expression with upto 4-SOP-terms of size three-literals or less. You might the arrive at the answer sooner, if you try to write the minimal SOP expression first and find the two inputs that occur most often in all the terms. Those two inputs are most likely to the control inputs.) (10 marks)*

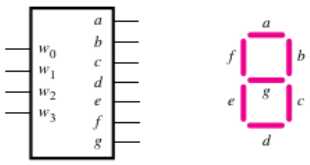

Figure 1: Seven segment display and BCD-to-7-segment display converter. When $a = 1$ the corresponding segment of the display lights up. To display the number 8, you will turn on all the seven segments, while to display 1, you will turn on $b = 1, c = 1$ and turn off $= 0$ the rest. The full truth-table for the seven-segment display is shown in Table 1.

Row	w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 1: Truth table for BCD to seven-segment display as shown in Figure 1. The missing combinations of inputs should be considered as dont care.

References

[1] S. Brown and Z. Vranesic. *Fundamentals of Digital Logic with Verilog Design: Third Edition.* McGraw-Hill Higher Education, 2013.