Homework 8

Max marks:

Due on Nov 10th, 2021, 9 AM, before class.

Problem 1 *Derive a minimal state table for an FSM that acts as a three-bit parity generator. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates the parity bit p = 1 if and only if the number of 1s in the three-bit sequence is odd (10 marks) [1, Prob 6.12].*

Problem 2 *Design a modulo-6 counter, which counts in the sequence 0, 1, 2, 3, 4, 5, 0, 1, ... The counter counts the clock pulses if its enable input, w, is equal to 1. Use D flip-flops in your circuit (20 marks) [1, Prob 6.23].*

Problem 3 *Design a three-bit counterlike circuit controlled by the input w. If w = 1, then the counter adds 2 to its contents, wrapping around if the count reaches 8 or 9. Thus if the present state is 8 or 9, then the next state becomes 0 or 1, respectively. If w = 0, then the counter subtracts 1 from its contents, acting as a normal down-counter. Use J-K flip-flops in your circuit (20 marks) [1, Prob 6.26].*

State Reduction

Problem 4 *Reduce the following state table to a minimum number of states:*

Present State	Next State $X=0$	Next State 1	Present Output (Z)
a	e	e	1
b	c	e	1
c	i	h	0
d	h	a	1
e	i	f	0
f	e	g	0
g	h	b	1
h	c	d	0
i	f	b	1

(10 marks).

Problem 5 *Digital engineer B. I. Nary has just completed the design of a sequential circuit which has the following state table:*

Present State	Next State $X=0$	Next State 1	Output 0	Output 1
S_0	S_5	S_1	0	0
S_1	S_5	S_6	0	0
S_2	S_2	S_6	0	0
S_3	S_0	S_1	1	0
S_4	S_4	S_3	0	0
S_5	S_0	S_1	0	0
S_6	S_5	S_1	1	0

His assistant, F. L. Ipflop, who has just completed this course, claims that his design can be used to replace Mr. Nary's circuit. Mr. Ipflop's design has the following state table:

	Next State $X=0$	Next State 1	Output 0	Output 1
a	a	b	0	0
b	a	c	0	0
c	a	b	1	0

1. *Is Mr. Ipflop correct? (Prove your answer.)(10 marks)*
2. *If Mr. Nary's circuit is always started in state S_0 , is Mr. Ipflop correct? (Prove your answer by showing equivalent states, etc.)*

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State Reduction

Problem 6 *1. Reduce the following state table to a minimum number of states using implica- tion charts (10 marks).*

2. *Use the guideline method to determine a suitable state assignment for the reduced table (10 marks).*

3. *Realize the table using D flip-flops (10 marks).*

4. *Realize the table using J-K flip-flops (10 marks).*

	$X = 0$	1	Z
A	A	B	1
B	C	E	0
C	F	G	1
D	C	A	0
E	I	G	1
F	H	I	1
G	C	F	0
H	F	B	1
I	C	E	0

References

[1] S. Brown and Z. Vranesic. *Fundamentals of Digital Logic with Verilog Design: Third Edition.* McGraw-Hill Higher Education, 2013.