Sequential logic design

Vikas Dhiman for ECE275

November 21, 2022

1 Objectives

1. Analyse and design both Mealy and Moore sequential circuits with multiple inputs and multiple outputs
2. Convert between Mealy and Moore designs

2 Mealy vs Moore Finite State Machines

Definition 1 (Finite State Machines (FSM))**.** *[1, Sec 3.4]*

Definition 2 (Mealy FSM)**.** *[1, Sec 3.4.3]*

Definition 3 (Moore FSM)**.** *[1, Sec 3.4.3]*

Example 1. *A sequential circuit has one input (X) and one output (Z). The circuit examines groups of four consecutive inputs and produces an output Z=1 if the input sequence 0010 or 0001 occurs. The sequences can overlap. Draw both Mealy and Moore timing diagrams. Find the Mealy and Moore state graph.*

Practice Problem 1. *A sequential circuit has one input (X) and one output (Z). The circuit examines groups of four consecutive inputs and produces an output Z=1 if the input sequence 0101 or 1001 occurs. The circuit resets after every four inputs. Draw both Mealy and Moore timing diagrams. Find the Mealy and Moore state graph.*

References

[1] Sarah L Harris and David Harris. *Digital design and computer architecture*. Morgan Kaufmann, 2022.