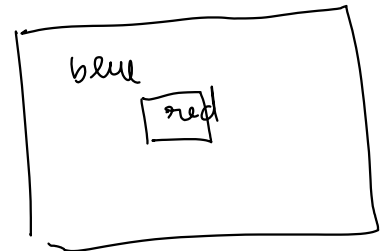


ECE275 Lab Final Project Kickoff

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1 VGA module

Watch the tutorial below and replicate it on the Altera FPGA board,

- VGA Video Tutorial (Must be logged in to your Umaine account to view) : **Video Tutorial**. There is a mistake in the video when instantiating the make_box module, it should be make_box make_first_player_paddle(and not module make_first_player make_box(
- Example simple top level : **VGA_top.v**
- DE0 VGA Driver Module : **DE0_VGA.v**
- PLL (Phase Locked Loop) Verilog File : **PLL_PIXEL_CLK.v**
- QSF File : **VGA_top.qsf**

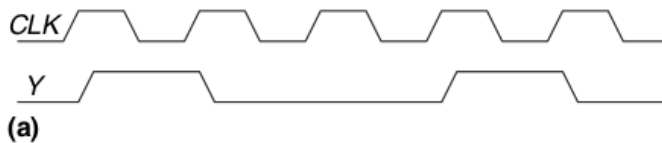
modified

read only

2 Breaking application into smaller parts

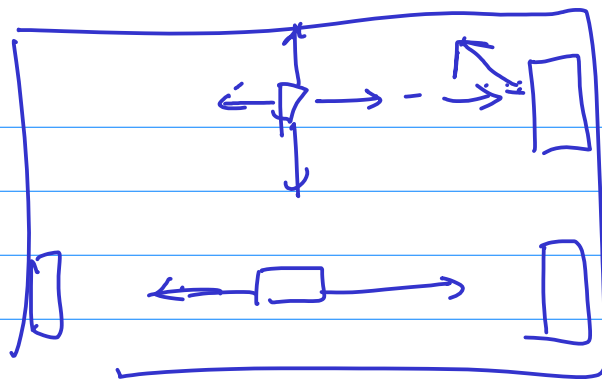
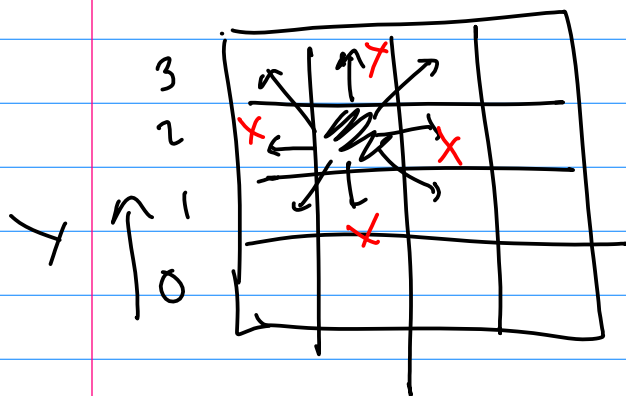
2.1 Slow clock

Problem 1. A divide-by- N counter has one output and no inputs. The output Y is HIGH for one clock cycle out of every N . In other words, the output divides the frequency of the clock by N . The waveform for a divide-by-3 counter is shown here:



Sketch circuit designs for such a counter

Problem 2. Repeat the above problem in Verilog and show a clock being reduced from 50 MHz to 10 Hz in ModelSim simulator. Example files covered in class, **testslowclock.v** **slowclock.v**



$\begin{matrix} & X \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 2 & 0 & 1 & 0 \\ 3 & 0 & 1 & 1 \end{matrix}$

State space

$\begin{matrix} X & Y & V_x & V_y \\ X_1 X_0 & Y_1 Y_0 & & \end{matrix}$

NE 00
 NW 01
 SE 10
 SW 11

Next state

$X^+ \ Y^+ \ V_x^+ \ V_y^+$

6 bits

2.2 Bouncing Ball

Problem 3. Design a circuit for a 1 pixel bouncing ball on a 4x4 pixel screen. You cannot design this circuit by hand (Why?). How will you design it using Verilog? Write verilog code and test it using a testbench?

Problem 4. Once you have the VGA example working, extend the above problem to 640x480 resolution and ball represented by a box your chosen size. Connect this module's output to the VGA module.

2.3 Moving paddle

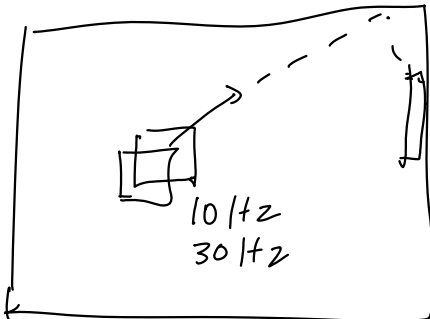
Problem 5. Design a circuit for 1 pixel paddle on a 4x4 pixel screen. Assume that it can take two inputs from BUTTONs, one for moving up and another one for moving down. You can design this circuit by hand (Why)?

Problem 6. Design the above circuit using Verilog.

Problem 7. Once you have the VGA example working, extend the above problem to 640x480 resolution with you

2.4 Ball paddle collision

Problem 8. Combine the bouncing ball problem with the moving paddle problem and bounce the ball only if the ball is about to hit the paddle, otherwise game is over. If the ball hits the paddle increment a score counter by 1.



① VGA module

② Slow clock

CLOCK 50 MHz
input