1 Syllabus covered

- ☑ Binary numbers, Hexadecimal, Sign-magnitude, One's-complement and Two's complement. Conversions between them.
- ☑ Generate minterms, maxterms, SOP canonical form and POS canonical forms and convert between them
- ☑ Understand and use the laws and theorems of Boolean Algebra
- ☑ Perform algebraic simplification using Boolean algebra
- ☑ Simplification using K-maps
- ☑ Derive sum of product and product of sums expressions for a combinational circuit
- ☑ Convert combinational logic to NAND-NAND and NOR-NOR forms
- ☑ Simplification using Quine-McCluskey method, PI tables and Petrick's method
- ☐ Design combinational circuits for positive and negative logic
- ☐ Design Hazard-free two level circuits and understand Hazards in multi-level circuits
- ☐ Compute noise margin of one device
- ☐ Describe how tri-state and open-collector outputs are different from totem-pole outputs.
- ☐ Different between and limitations of master-slave and edge-triggered flip-flops.
- ☐ Compute fan out and noise margin of one device driving the same time
- ☐ Know the differences and similarities between PAL, PLA, and ROMs and can use each for logic design
- ☐ Design combinational circuits using multiplexers and decoders
- ☐ Analyze a sequential circuit and derive a state-table and a state-graph
- ☐ Understand the difference between synchronous and asynchronous inputs
- ☐ Derive a state graph or state table from a word description of the problem
- ☐ Reduce the number of states in a state table using row reduction and implication tables
- ☐ Perform a state assignment using the guideline method
- ☐ Implement a design using JK, SR, D or T flip-flops
- ☐ Analyse and design both Mealy and Moore sequential circuits with multiple inputs and multiple outputs
- ☐ Convert between Mealy and Moore designs
- ☐ Partition a system into multiple state machines

1.1 Labs (not questioned in exams)

- ☐ Use computer tools to enter designs graphically and HDL
- ☐ Simulate designs using computer tools
- ☐ Use computer tools to program gate arrays logic and debug and test

ECE275 (sample) Midterm 1 Fall 2023

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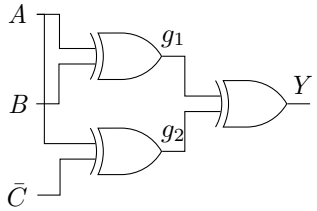
2 Instructions

- Time allowed is 50 minutes. (This sample exam might be lengthier than the actual exam.)
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book. One 8x11in cheatsheet is allowed.
- Non-programmable calculators are permitted.
- The maximum number of marks is 100, as indicated; the midterm examination amounts 10% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.

Problem 1. *Number conversions:*

1. *Use repeated division to convert* 230_{10} *to octal representation (5 marks).*
2. *What is the value of* $19D_{16}$ *in base 10 (5 marks).*
3. *A 6-bit two's complement number is* 100011_2*. Convert it to (signed) decimal (5 marks).*
4. *Represent* -23_{10} *in two's complement binary notation (5 marks).*

Problem 2. *Consider the circuit below*



By algebraic manipulation, prove or disprove that $Y = \bar{B}\bar{C} + BC$ *(10 marks).*

Problem 3. *Use the following 5-variable K-map for F (A, B, C, D, E), and find a minimal SOP expression for F (15 marks)*

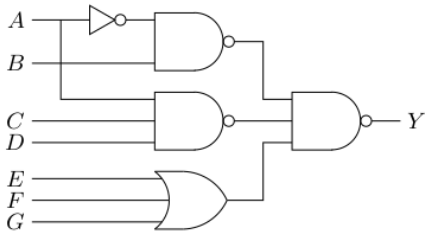
DE \ BC	00	01	11	10
00	1			1
01	1	1		1
11		1		
10		1	1	

A=0

DE \ BC	00	01	11	10
00		1	1	
01	1	1		1
11		1		
10		1	1	

A=1

Problem 4. *Use bubble-pushing and/or algebra to find an SOP expression for Y in the circuit below. If you use bubble-pushing, draw an equivalent circuit beside the given circuit (5 marks).*



Problem 5. *Consider the function Y given below.*

$$Y(A,B,C,D) = \sum m(0,3,5,7,8,14) + d(2,12,15)$$

1. *Draw a K-maps to derive a minimum SOP and POS expressions for Y . Indicate all essential prime implicants for Y or $\bar{Y}$ in your K-maps (20 marks).*
2. *Sketch a two-level NOR-NOR circuit for Y. Assume that A, B, C, and D are available in true end complimentary forms (5 marks).*
3. *Write Y in Product of sums (POS)* canonical *form (5 marks).*

Problem 6. *Design a minimal SOP circuit to add two two-bit unsigned numbers. Denote the two bits of first number as A_1A_0 and the two bits of second number as B_1B_0. The result will be a 2-bit sum S_1S_0 and a carry C. Start with filling out the following truth table (3 example rows are provided) and then use K-maps to find minimal SOP for S_1, S_0 and a single carry bit C_1 (20 marks).*

A_1	A_0	B_1	B_0	C_1	S_1	S_0
0	*0*	*0*	*0*			
0	*0*	*0*	*1*			
0	*0*	*1*	*0*			
0	*0*	*1*	*1*			
0	*1*	*0*	*0*			
0	*1*	*0*	*1*	*0*	*1*	*0*
0	*1*	*1*	*0*			
0	*1*	*1*	*1*			
1	*0*	*0*	*0*			
1	*0*	*0*	*1*			
1	*0*	*1*	*0*			
1	*0*	*1*	*1*			
1	*1*	*0*	*0*			
1	*1*	*0*	*1*	*1*	*0*	*0*
1	*1*	*1*	*0*			
1	*1*	*1*	*1*	*1*	*1*	*0*