Homework 4

Max marks: 100

Due on Nov 1st, 2023, 12 noon, before class.

Problem 1 *Consider the timing diagram in Figure 1. Assuming that the D and Clock inputs shown are applied to the circuit in Figure 2, draw waveforms for the Q_a , Q_b , and Q_c signals. (10 marks) [1, Prob 5.1]*

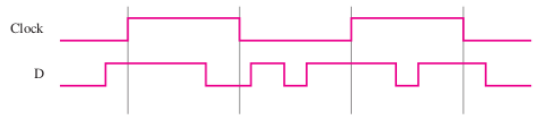

Figure 1: Inputs for Prob 1

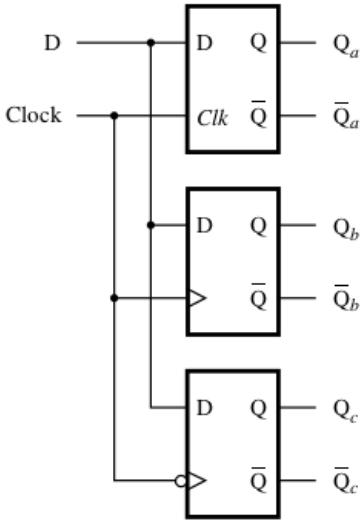

Figure 2: Circuit for Prob 1. Recall that *Clk* with a "▷" symbol indicates rising-edge (positive-edge) triggered flip-flop. *Clk* without "▷" symbol indicates a level-triggered latch. *Clk* with "○▷" symbol indicates a falling-edge (negative-edge) triggered flip-flop.

Problem 2 *An SR flip-flop is a flip-flop that has set and reset inputs like a gated SR latch. Show how an SR flip-flop can be constructed using a D flip-flop and other logic gates. (10 marks) [1, Prob 5.5]*

Problem 3 *Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates (10 marks) [1, Prob 5.7].*

Problem 4 *Design a three-bit up/down counter using T flip-flops. It should include a control input called Up/Down. If Up/Down = 0, then the circuit should behave as an up-counter. If Up/Down = 1, then the circuit should behave as a down-counter. (10 marks) [1, Prob 5.15].*

Problem 5 *The circuit in Figure 3 looks like a counter. What is the counting sequence of this circuit (10 marks) [1, Prob 5.17]?*

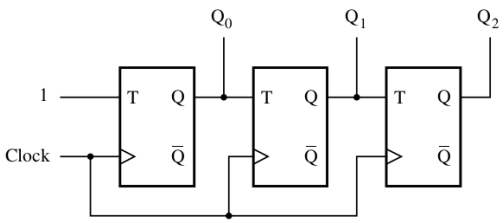

Figure 3: Circuit for Problem 5.

Problem 6 *Derive a minimal state table for an FSM (Finite-state machine) that acts as a three-bit parity generator. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates the parity bit p = 1 if and only if the number of 1s in the three-bit sequence is odd (10 marks) [1, Prob 6.12].*

Problem 7 *Design a modulo-6 counter, which counts in the sequence 0, 1, 2, 3, 4, 5, 0, 1, ... The counter counts the clock pulses if its enable input, w, is equal to 1. Use D flip-flops in your circuit (20 marks) [1, Prob 6.23].*

Problem 8 *Design a three-bit counterlike circuit controlled by the input w. If w = 1, then the counter adds 2 to its contents, wrapping around if the count reaches 8 or 9. Thus if the present state is 8 or 9, then the next state becomes 0 or 1, respectively. If w = 0, then the counter subtracts 1 from its contents, acting as a normal down-counter. Use J-K flip-flops in your circuit (20 marks) [1, Prob 6.26].*

References

[1] S. Brown and Z. Vranesic. *Fundamentals of Digital Logic with Verilog Design: Third Edition.* McGraw-Hill Higher Education, 2013.