Homework 4

Max marks: 60

Due on Nov 1st, 2023, 12 noon, before class.

Problem 1 *Consider the timing diagram in Figure 1. Assuming that the D and Clock inputs shown are applied to the circuit in Figure 2, draw waveforms for the Q_a , Q_b , and Q_c signals. (10 marks) [1, Prob 5.1]*

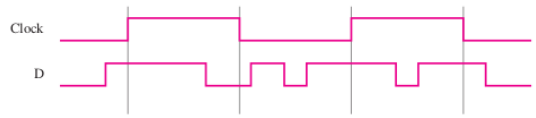

Figure 1: Inputs for Prob 1

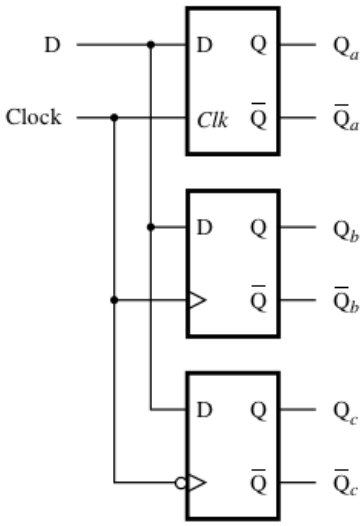

Figure 2: Circuit for Prob 1. Recall that *Clk* with a "▷" symbol indicates rising-edge (positive-edge) triggered flip-flop. *Clk* without "▷" symbol indicates a level-triggered latch. *Clk* with "○▷" symbol indicates a falling-edge (negative-edge) triggered flip-flop.

Problem 2 *Figure 3 shows a S-R latch built with NOR gates. Draw a similar latch using NAND gates. Derive its characteristic table and show its timing diagram. Assume that $\bar{S}$ and $\bar{R}$ are available. (10 marks) [1, Prob 5.2].*

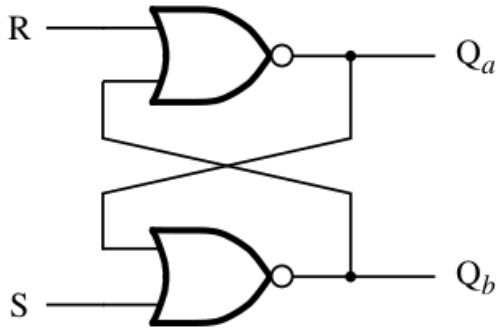

Figure 3: Circuit for Prob 2

Problem 3 *An SR flip-flop is a flip-flop that has set and reset inputs like a gated SR latch. Show how an SR flip-flop can be constructed using a D flip-flop and other logic gates. (10 marks) [1, Prob 5.5]*

Problem 4 *Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates (10 marks) [1, Prob 5.7].*

Problem 5 *Design a three-bit up/down counter using T flip-flops. It should include a control input called Up/Down. If Up/Down = 0, then the circuit should behave as an up-counter. If Up/Down = 1, then the circuit should behave as a down-counter. (10 marks) [1, Prob 5.15].*

Problem 6 *The circuit in Figure 4 looks like a counter. What is the counting sequence of this circuit (10 marks) [1, Prob 5.17]?*

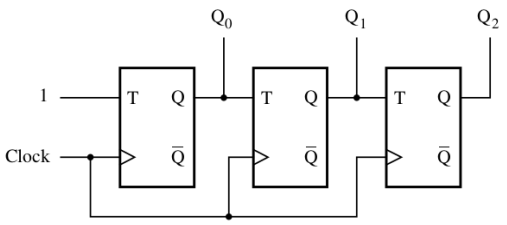

Figure 4: Circuit for Problem 6.

References

[1] S. Brown and Z. Vranesic. *Fundamentals of Digital Logic with Verilog Design: Third Edition.* McGraw-Hill Higher Education, 2013.