ECE275 Practice problems for Final Fall 2023

Instructor: Vikas Dhiman (vikas.dhiman@maine.edu)

December 6, 2023

Student Name: Student Email:

1 Instructions

- Time allowed is ∞ minutes.
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book. One 8×11 in two-sided cheatsheet is allowed.
- Non-programmable calculators are permitted.
- The maximum number of marks is 160, as indicated; the midterm examination amounts 10% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility. Colored pens/pencils are recommended for K-map grouping.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.
- If you are behind on grades, you may submit the solutions to this on brightspace before Dec 15th exam for extra homework grades.

Problem 1. *Use the following 5-variable K-map for F (A, B, C, D, E), and find a minimal SOP expression for F (15 marks)*

DE \ BC	00	01	11	10
00	1			1
01	1	1		1
11		1		
10		1	1	

A=0

DE \ BC	00	01	11	10
00		1	1	
01	1	1		1
11		1		
10		1	1	

A=1

Problem 2. *A sequential circuit has two inputs and two outputs. The inputs (X_1 and X_0) represent a 2-bit binary number, N. If the present value of N is greater than the previous value, then Z_1 is 1. If the present value of N is less than the previous value, then Z_2 is 1.* ***Otherwise****, Z_1 and Z_2 are 0. When the first pair of inputs is received, there is no previous value of N, so we*

cannot determine whether the present N is greater than or less than the previous value; therefore, the "otherwise" category applies.

Find a Mealy state table for the circuit (minimum number of states, including starting state, is five) (30 marks).

(Hint: The header for Mealy State table will look something like this:)

Present State	Next State				Outputs (Z_1Z_2)			
	Inputs $X_1X_0 = 00$	01	10	11	$X_1X_0 = 00$	01	10	11
S_0	S_1	S_2	S_3	S_4	00	00	00	00

Problem 3. *Reduce the following state table to minimum number of states (30 marks)*

PS	NS $X=0$	NS 1	Output 0	Output 1
a	*b*	*c*	1	0
b	*e*	*d*	1	0
c	*g*	*d*	1	1
d	*e*	*b*	1	0
e	*f*	*g*	1	0
f	*h*	*b*	1	1
g	*h*	*i*	0	1
h	*g*	*i*	0	1
i	*a*	*a*	0	1

Problem 4. *1. Use the guideline method (Highest priority and Medium priority only) to determine a suitable* ***state assignment*** *for the state table (20 marks).*

2. Realize the least significant bit of the encoding table using J-K flip-flops (30 marks).

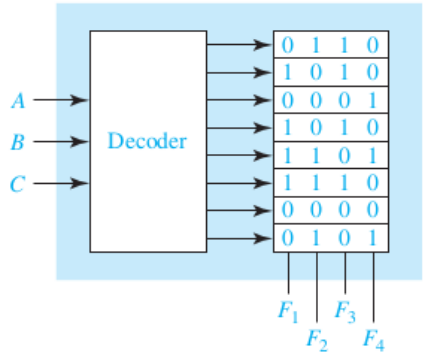
Present State	*Next State* $X=0$	*Next State* 1	*Output (Z)*
A	*A*	*B*	*1*
B	*C*	*E*	*0*
C	*F*	*G*	*1*
D	*C*	*A*	*0*
E	*B*	*G*	*1*
F	*F*	*B*	*1*
G	*C*	*F*	*0*

Problem 5. *A 4:2 priority encoder takes 4 inputs y_0, y_1, y_2, y_3 and has three outputs, w_1, w_0 and IST. Find boolean expressions for w_1 and w_0 using K-maps for the priority encoder. The priority encoder truth table is given for reference ("*" indicates all possible input combinations and "d" indicates don't care output). (10 marks)*

Inputs				*Outputs*		
y_0	y_1	y_2	y_3	w_1	w_0	*IST*
0	*0*	*0*	*0*	*d*	*d*	*0*
1	*	*	*	*0*	*0*	*1*
0	*1*	*	*	*0*	*1*	*1*
0	*0*	*1*	*	*1*	*0*	*1*
0	*0*	*0*	*1*	*1*	*1*	*1*

Problem 6. *(Optional for extra credit) The following diagram shows the pattern of 0's and 1's stored in a ROM with eight words and four bits per word. What will be the values of $F_1, F_2, F_3, and F_4$*

if $A = B = 0$ and $C = 1$? Also give the minterm expansions for F_1 and F_2 (20 marks).



Problem 7. *The following prime implicant table is for a four variable function $f(A, B, C, D)$. Give the algebraic expression of each of the essential prime implicants. Find the minimal sum of products expression for f by PI table reduction. (10 marks)*

minterms \ PIs:	$\bar{B}D$	$\bar{B}C$	CD	AD
2		×		
3	×	×	×	
7			×	
9	×			×
11	×	×	×	×
13				×

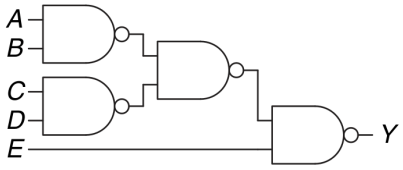
Problem 8. *Packages arrive at the stockroom and are delivered on carts to offices and laboratories by student employees.The carts and packages are various sizes and shapes.The students are paid according to the carts used. There are five carts and the pay for their use is*
Cart C1: \$2
Cart C2: \$1
Cart C3: \$4
Cart C4: \$2
Cart C5: \$2
On a particular day, seven packages arrive, and they can be delivered using the five carts as follows:
C1 can be used for packages P1, P3, and P4.
C2 can be used for packages P2, P5, and P6.
C3 can be used for packages P1, P2, P5, P6, and P7.
C4 can be used for packages P3, P6, and P7.
C5 can be used for packages P2 and P4.
The stockroom manager wants the packages delivered at minimum cost. Using minimization techniques described in this class, present a systematic procedure for finding the minimum cost solution. (20 marks)

Problem 9. *(a) For $V_{IH} = 4$ V, $V_{OH} = 4.5$ V, $V_{IL} = 1$ V, $V_{OL} = 0.3$ V, and $V_{DD} = 5$ V, calculate the noise margins NM_H and NM_L (5 marks).*
(b) Draw an eight-input NAND gate built using NMOS technology and pull-up resistor (5 marks).
(c) In the above circuit, if the voltage drop across each transistor is 0.1 V, what is V_{OL} ? What is the corresponding NM_L using the other parameters from part (a) (10 marks).

Problem 10. *What is the difference between positive logic and negative logic? Design a CMOS complex gate for $f = x_1\bar{x}_2 + \bar{x}_1x_2$ under negative logic (10 marks).*

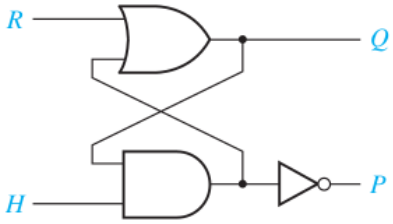
Problem 11. *Find the propagation delay and contamination delay of the following circuit (5*

marks):

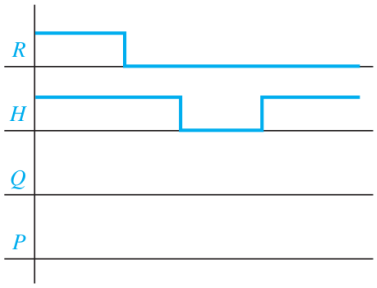


Problem 12. *Describe how tri-state and open-collector outputs are different from totem- pole outputs using NMOS NOR gate as an example (10 marks).*

Problem 13. *A latch can be constructed from an OR gate, an AND gate, and an inverter connected as follows:*



1. *What restriction must be placed on R and H so that P will always equal Q (under steady-state conditions) (10 marks)?*
2. *Construct a characteristic (next-state) table and derive the corresponding characteristic equation for the latch (5 marks).*
3. *Complete the following timing diagram for the latch (10 marks)*



Problem 14. *Figure 1 shows the notation for a BCD to 7-segment display and Table 1 shows the corresponding truth table. The inputs corresponding to the missing rows in the truth table should be considered as don't care.*

1. *implement segment "a" using an 8:1 mux and no other logic gate, (10 marks)*
2. *implement segment "a" using a 4:1 mux and one other gate, (10 marks)*
3. *implement segment "f" with 4:1 mux and no other logic gate. Assume inputs are available in both uncomplemented and complemented form. (Hint: There are* $({}^4C_2 = 6)$ *possible pairs of control inputs:* (w_3, w_2), (w_2, w_1), (w_1, w_0), (w_0, w_3), (w_0, w_2), (w_1, w_3). *There are 6 don't care conditions. With two control inputs of the multiplexer and one input, you can represent an expression with up to 4-SOP-terms of size three-literals or less. You might the arrive at the*

answer sooner, if you try to write the minimal SOP expression first and find the two inputs that occur most often in all the terms. Those two inputs are most likely to be the chosen pair of control inputs.) (10 marks)

Row	w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 1: Truth table for BCD to seven-segment display as shown in Figure 1. The missing combinations of inputs should be considered as dont care.

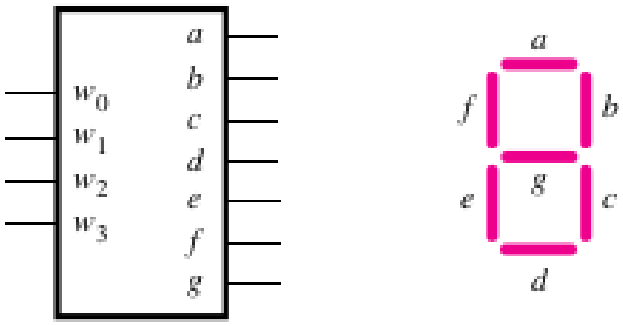


Figure 1: Seven segment display and BCD-to-7-segment display converter. When $a = 1$ the corresponding segment of the display lights up. To display the number 8, you will turn on all the seven segments, while to display 1, you will turn on $b = 1, c = 1$ and turn off $= 0$ the rest. The full truth-table for the seven-segment display is shown in Table 1.

Problem 15. *Design a 3-bit modulo 8 Gray counter that counts from 000, to 111 and then loops back to 0000. (A modulo N counter counts from 0 to $N - 1$) (20 marks).*

1. *Draw its state transition table*
2. *Design the circuit using a D flip-flop.*