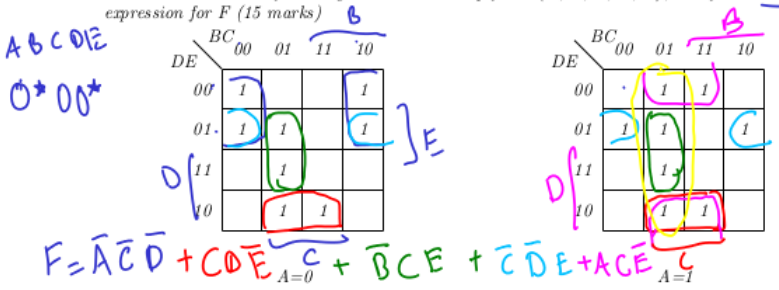
Problem 1. *Use the following 5-variable K-map for F (A, B, C, D, E), and find a minimal SOP expression for F (15 marks)*



$$F = \bar{A}\bar{C}\bar{D} + CD\bar{E} + \bar{B}CE + \bar{C}\bar{D}E + AC\bar{E}$$

Problem 2

Example

X_1	0	0	1	1	1	0	1
X_0	0	1	0	1	0	1	1
Z_1	0	1	1	1	0	0	1
Z_2	0	0	0	0	1	1	0

PS	NS				Outputs ($Z_1 Z_2$)			
	$X_1 X_0$ = 00	01	10	11	$X_1 X_0$ = 00	01	10	11
S_0	S_1	S_2	S_3	S_4	00	00	00	00
S_1	S_1	S_2	S_3	S_4	00	10	10	10
S_2	S_1	S_2	S_3	S_4	01	00	10	10
S_3	S_1	S_2	S_3	S_4	01	01	00	10
S_4	S_1	S_2	S_3	S_4	01	01	01	00

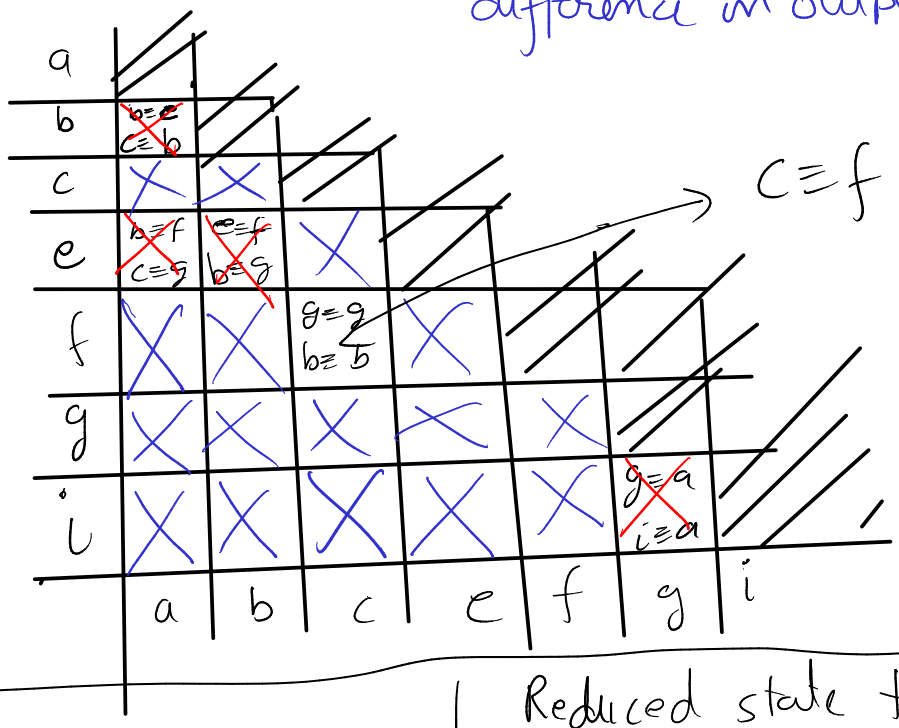
Problem 3

PS	NS X = 0	1	Output 0	1
a	b	c	1	0
b	e	d, b	1	0
c	g	d, b	1	1
d	e	b	1	0
e	f	g	1	0
f	h, g	b	1	1
g	h, g	i	0	1
h	g	i	0	1
i	a	a	0	1

State reduction ① if $g \equiv h$ and $i \equiv i$ then $g \equiv h$

② if $c \equiv e$ and $b \equiv d$ then $b \equiv d$

Implication chart - $x \equiv$ cannot be same due to difference in output



Replace h with g

d with b

f with c

Reduced state table

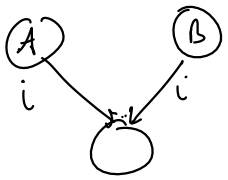
PS	NS X=0	1	Output 0	1
a	b	c	1	0
b	e	b	1	0
c	g	b	1	1
e	c	g	1	0
g	g	i	0	1
i	a	a	0	1

Problem 4. *1. Use the guideline method (Highest priority and Medium priority only) to determine a suitable* ***state assignment*** *for the state table (20 marks).*

2. Realize the least significant bit of the encoding table using J-K flip-flops (30 marks).

Present State	*Next State* $X=0$	1	*Output (Z)*
A	A	B	1
B	C	D	0
C	F	G	1
D	C	A	0
E	B	G	1
F	F	B	1
G	C	F	0

Highest priority

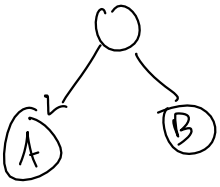


(B, D, G) (C, F) (G, E) (A, F)

leads to C when X = 0

F

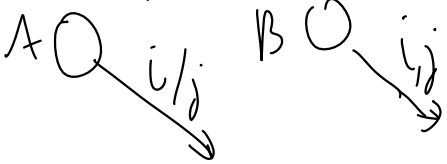
Medium priority



(A, B), (C, E) (F, G), (C, A), (B, G)

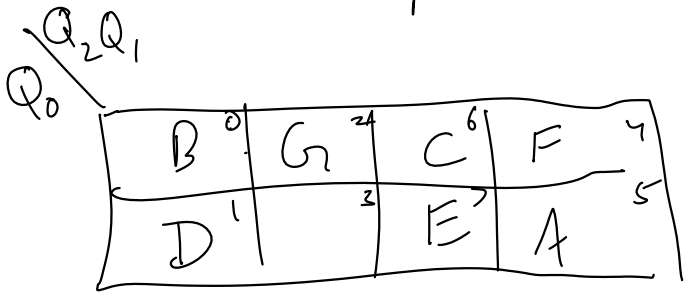
(F, B), (C, F)

Lowest priority



	Q_2	Q_1	Q_0
A	1	0	1
B	0	0	0
C	1	1	0
D	0	0	1
E	1	1	1
F	1	0	0
G	0	1	0

State map



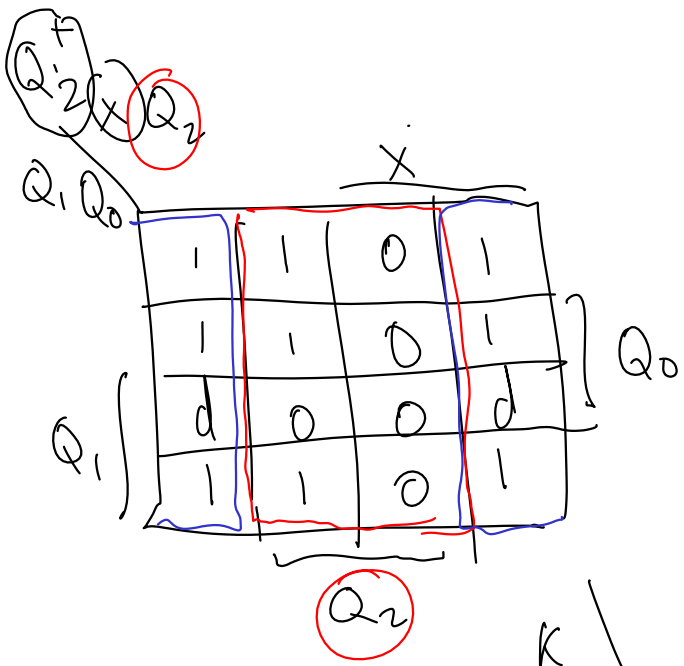
Present State	Next State $X=0$	Next State 1	Output (Z)
A	A	B	1
B	C	D	0
C	F	G	1
D	C	A	0
E	B	G	1
F	F	B	1
G	C	F	0

	Q_2	Q_1	Q_0
A	1	0	1
B	0	0	0
C	1	1	0
D	0	0	1
E	1	1	1
F	1	0	0
G	Output	1	0

NS

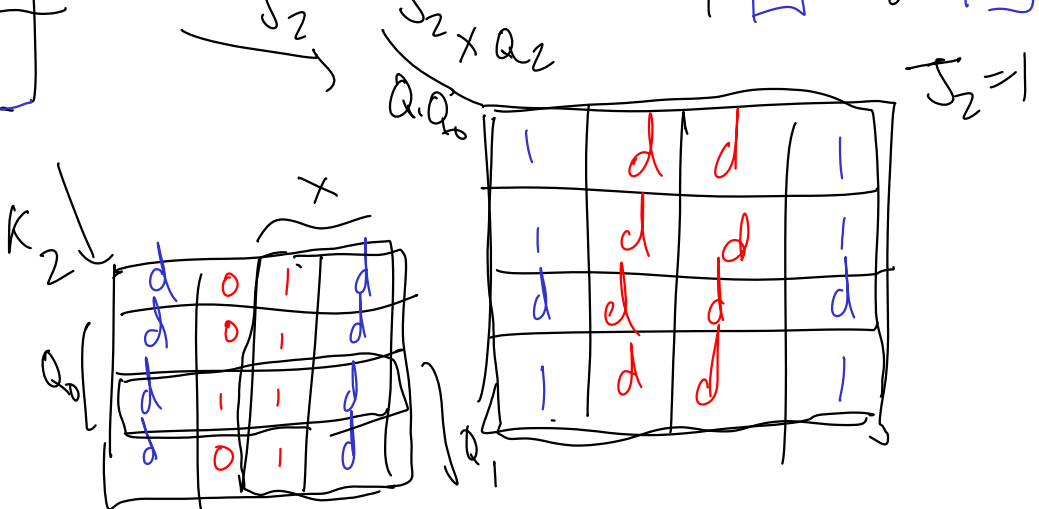
PS

PS $Q_2\ Q_1\ Q_0$				$X=0$ $Q_2^+\ Q_1^+\ Q_0$				$X=1$ $Q_2^+\ Q_1^+\ Q_0^+$				
0	0	0	B	0	1	1	0	8	1	1	1	0
0	0	1	D	1	1	1	0	9	1	0	1	0
0	1	0	G	2	1	1	0	10	1	0	0	0
0	1	1		3	d	d	d	11	d	d	d	d
1	0	0	F	4	1	0	0	12	0	0	0	1
1	0	1	A	5	1	0	1	13	0	0	0	1
1	1	0	C	6	1	0	0	14	0	1	0	1
1	1	1	E	7	0	0	0	15	0	1	0	0

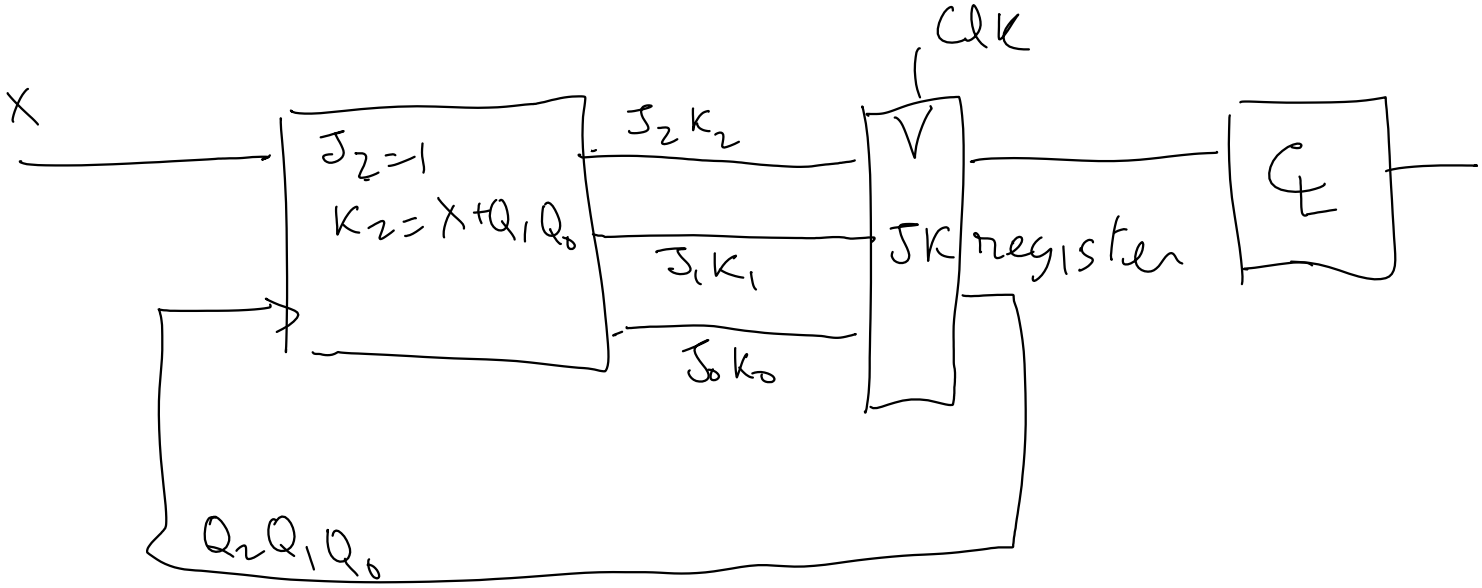


encoded state table

Q_2	Q_2^+	J_2	K_2
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0



$K_2 = X + Q_1 Q_0$



PS $Q_2\ Q_1\ Q_0$		NS $X=0$ $Q_2^+\ Q_1^+\ Q_0^+$	NS $X=1$ $Q_2^+\ Q_1^+\ Q_0^+$	Output Z
0 0 0	B	1 1 0	1 1 1	0
0 0 1	D	1 1 0	1 0 1	0
0 1 0	G	1 1 0	1 0 0	0
0 1 1		d d d	d d d	d
1 0 0	F	1 0 0	0 0 0	1
1 0 1	A	1 0 1	0 0 0	1
1 1 0	C	1 0 0	0 1 0	1
1 1 1	E	0 0 0	0 1 0	0

Q_2	Q_2^+	J_2	K_2
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

Q_1^+ — XQ_2 / Q_1Q_0 — X / Q_0 / Q_2

Q_1Q_0 \ XQ_2	00	01	11	10
00	1	0	0	1
01	1	0	0	0
11	d	0	1	d
10	1	0	1	0

J_1 — XQ_2 / Q_1Q_0

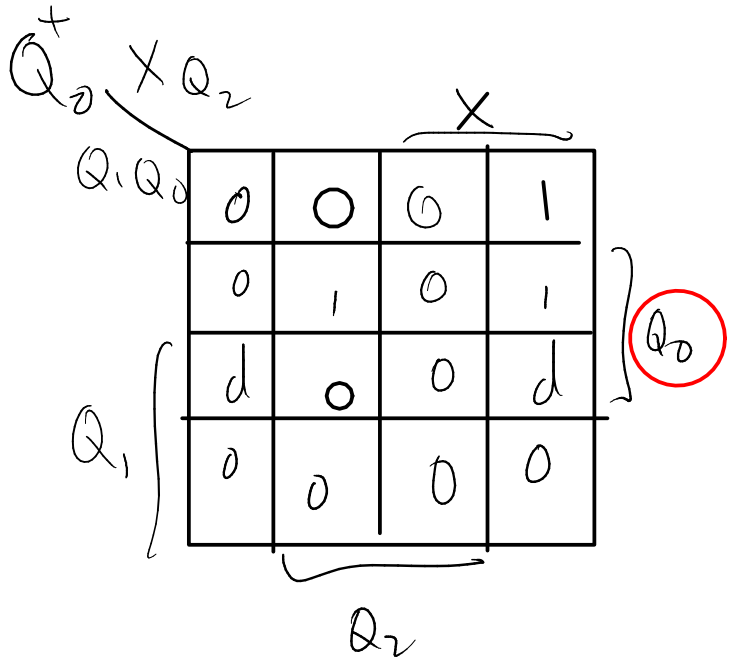
Q_1Q_0 \ XQ_2	00	01	11	10
00	1	0	0	1
01	1	0	0	0
11	d	d	d	d
10	d	d	d	d

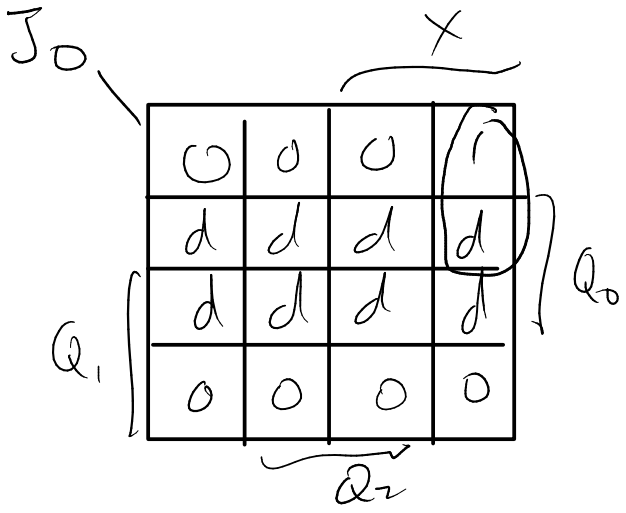
$J_1 = \bar{X}\bar{Q}_2 + \bar{Q}_2\bar{Q}_0$

$K_1 = \bar{X}Q_2 + X\bar{Q}_2$

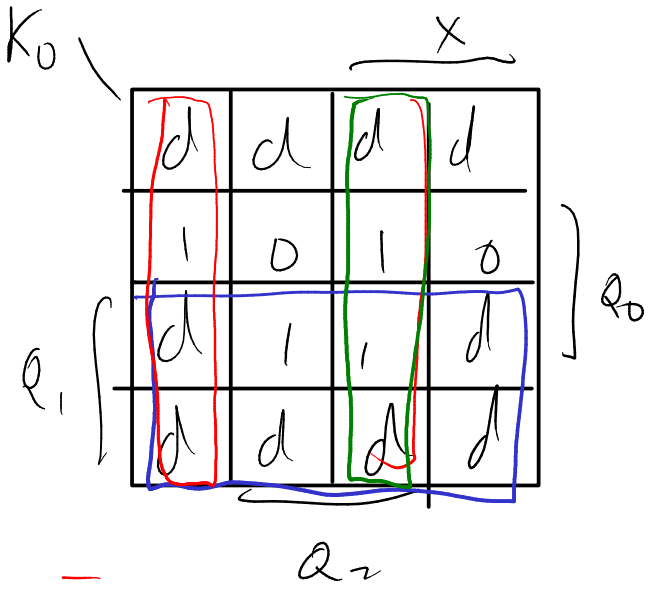
K_1 — XQ_2 / Q_1Q_0

Q_1Q_0 \ XQ_2	00	01	11	10
00	d	d	d	d
01	d	d	d	d
11	d	1	0	d
10	0	1	0	1





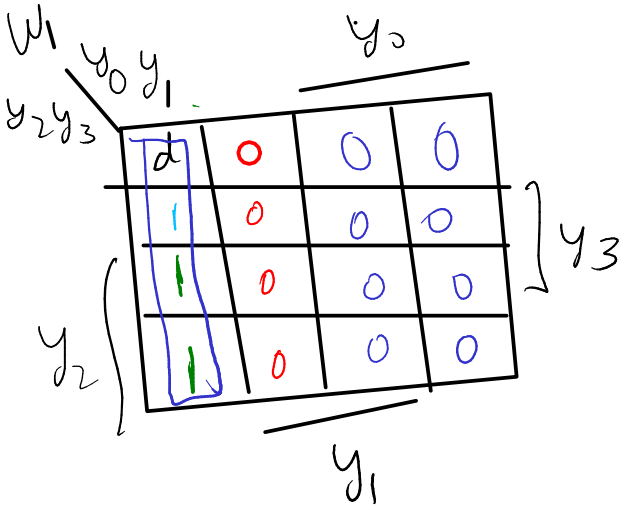
$$J_0 = X\bar{Q}_2\bar{Q}_1$$

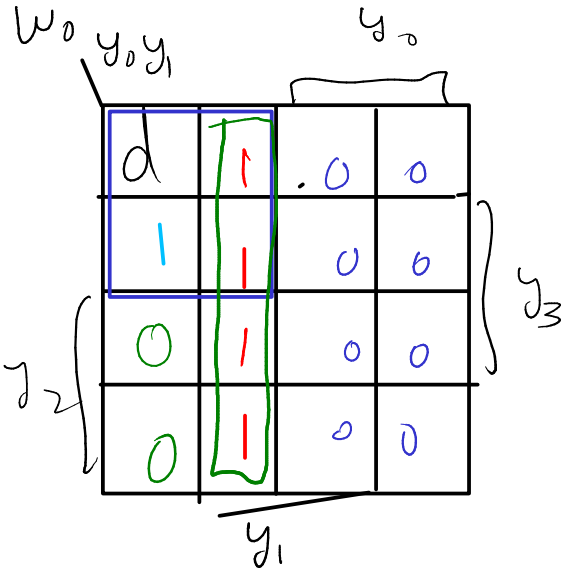


$$K_0 = Q_1 + \bar{X}\bar{Q}_2 + XQ_2$$

Problem 5. *A 4:2 priority encoder takes 4 inputs y_0, y_1, y_2, y_3 and has three outputs, w_1, w_0 and IST. Find boolean expressions for w_1 and w_0 using K-maps for the priority encoder. The priority encoder truth table is given for reference ("*" indicates all possible input combinations and "d" indicates don't care output). (10 marks)*

Inputs				Outputs		
y_0	y_1	y_2	y_3	w_1	w_0	IST
0	0	0	0	d	d	0
1	*	*	*	0	0	1
0	1	*	*	0	1	1
0	0	1	*	1	0	1
0	0	0	1	1	1	1





$$w_1 = \overline{y_0}\,\overline{y_1}$$

$$w_0 = \overline{y_0}\,y_1 + \overline{y_0}\,\overline{y_2}$$

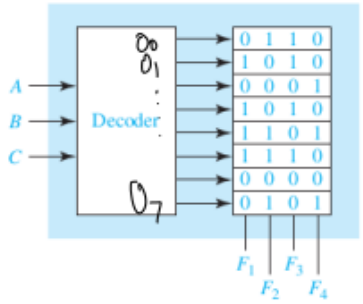
Problem 6

when ABC = 001

then $F_1 F_2 F_3 F_4$ = 1010

$F_1 = \sum m(1, 3, 4, 5)$

$F_2 = \sum m(0, 4, 5, 7)$



Problem 7. *The following prime implicant table is for a four variable function $f(A, B, C, D)$. Give the algebraic expression of each of the essential prime implicants. Find the minimal sum of products expression for f by PI table reduction. (10 marks)*

minterms \ *PIs:*	$\bar{B}D$	$\bar{B}C$	CD	AD
2				
3	×	×	×	
7			×	
9	×			×
11	×	×	×	×
13				×

EPI = { $\bar{B}C$, AD, CD }

Problem 8. *Packages arrive at the stockroom and are delivered on carts to offices and laboratories by student employees. The carts and packages are various sizes and shapes. The students are paid according to the carts used. There are five carts and the pay for their use is*

Cart C1: $2
Cart C2: $1
Cart C3: $4
Cart C4: $2
Cart C5: $2

On a particular day, seven packages arrive, and they can be delivered using the five carts as follows:
C1 can be used for packages P1, P3, and P4.
C2 can be used for packages P2, P5, and P6.
C3 can be used for packages P1, P2, P5, P6, and P7.
C4 can be used for packages P3, P6, and P7.
C5 can be used for packages P2 and P4.
The stockroom manager wants the packages delivered at minimum cost. Using minimization techniques described in this class, present a systematic procedure for finding the minimum cost solution. (20 marks)

Carts → / Packages	C_1	C_2	C_3	C_4	C_5
P_1	×		×		
P_2		×	×		×
P_3	×			×	
P_4	×				×
P_5		×	×		
P_6		×	×		×
P_7			×	×	

If P_5 is delivered, P_7 will always be delivered

Package P1 is delivered if C1 OR C3 is used.

Package P2 is delivered if C2 OR C3 OR C5 is used

All packages are delivered if the following boolean expression is true

$$= \underbrace{(C_1 + C_3)}_{P_1}\underbrace{(C_2 + C_3 + C_5)}_{P_2}\underbrace{(C_1 + C_4)}_{P_3}\underbrace{(C_1 + C_5)}_{P_4}$$

$$\underbrace{(C_2 + C_3)}_{P_5}\underbrace{(C_3 + C_4)}_{P_7}$$

$= C_1 C_2 C_4$ ✓

Cost = 5

C_1 occurs in most brackets and $C_1 \cdot C_1 = C_1$

$+ C_1 C_3$

cost = 6

$+ C_1 C_4$

cost = 8

$+ C_1 C_3 C_5$

cost = 8

$+ C_3 C_4 C_5$

cost = 8

$+ C_3 C_2 C_4 C_5$

$+ \ldots\ldots$

Pick cuts

C_1 and C_2 and C_4

for cost 5.

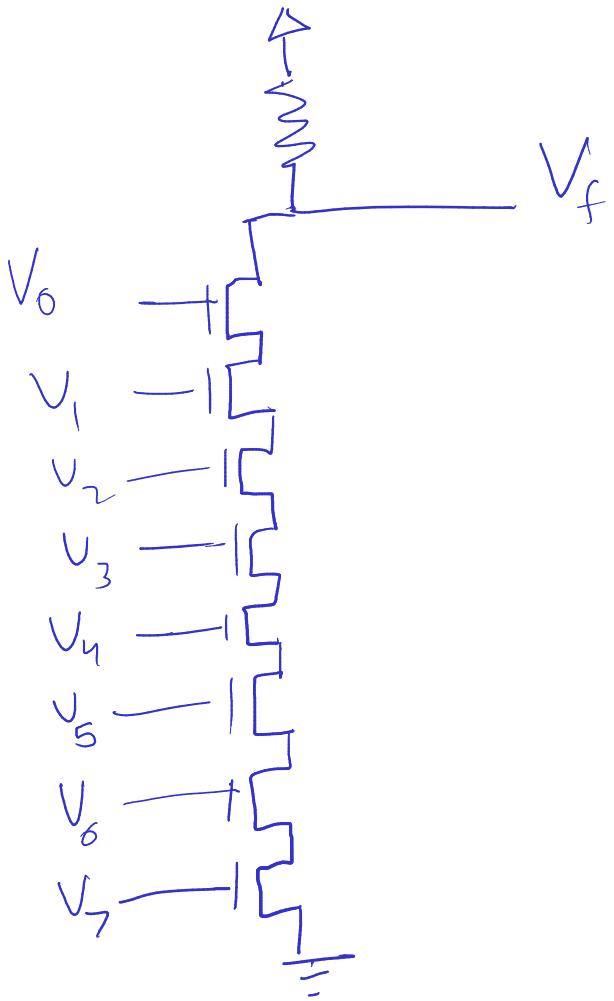
That covers all packages

Problem 9. *(a) For $V_{IH} = 4$ V, $V_{OH} = 4.5$ V, $V_{IL} = 1$ V, $V_{OL} = 0.3$ V, and $V_{DD} = 5$ V, calculate the noise margins NM_H and NM_L (5 marks).*
(b) Draw an eight-input NAND gate built using NMOS technology and pull-up resistor (5 marks).
(c) In the above circuit, if the voltage drop across each transistor is 0.1 V, what is V_{OL} ? What is the corresponding NM_L using the other parameters from part (a) (10 marks).

(a) $NM_H = V_{OH} - V_{IH} = 4.5 - 4 = 0.5\,V$

$NM_L = V_{IL} - V_{OL} = 1 - 0.3 = 0.7\,V$

(b)



$V_f = L$ if and only if all $V_0, V_1, \ldots, V_7$ are H

(c) Above circuit is not given

Problem 10 Under positive logic, high voltage (H) is treated as boolean 1 while low voltage is boolean 0

Under negative logic H = 0
L = 1

$f = x_1\bar{x}_2 + \bar{x}_1 x_2$

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

Negative logic →

V_{x_1}	V_{x_2}	V_f
H	H	H
H	L	L
H	L	L
L	L	H

↓ Positive logic

x_1	x_2	g
1	1	1
1	0	0
0	1	0
0	0	1

←

$g = \sum m(0,3)$

$= \bar{x}_1\bar{x}_2 + x_1 x_2$

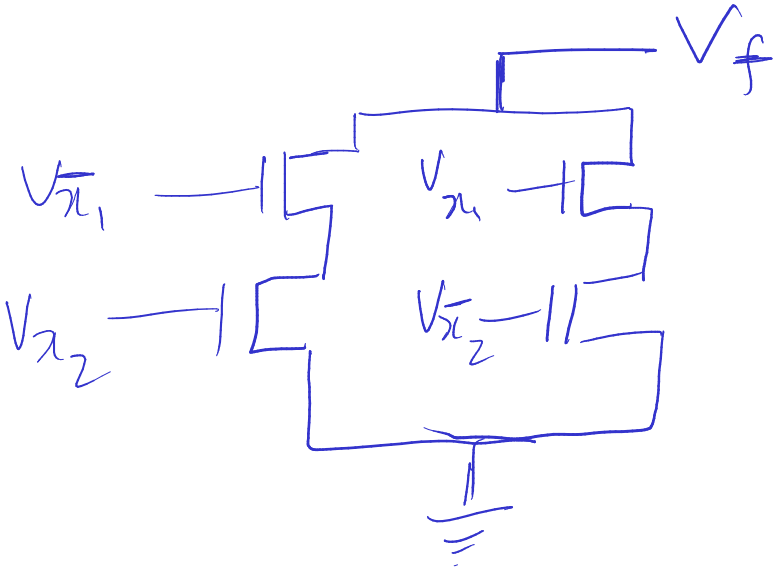
Designing $f = \bar{x}_1 x_2 + x_1 \bar{x}_2$ under negative logic

is same as designing $g = \bar{x}_1 \bar{x}_2 + x_1 x_2$ under +ve logic

nMOS block design

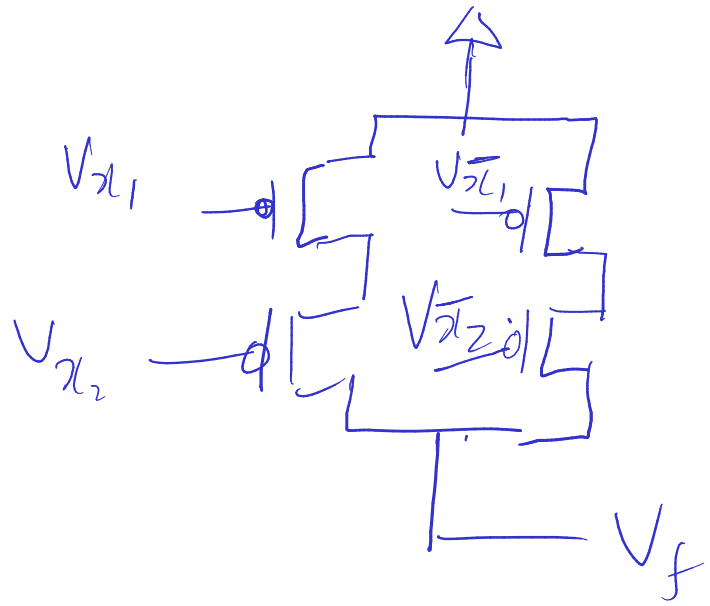
Design for $\bar{g} = \overline{\bar{x}_1 \bar{x}_2 + x_1 x_2}$

$= \bar{x}_1 x_2 + x_1 \bar{x}_2$

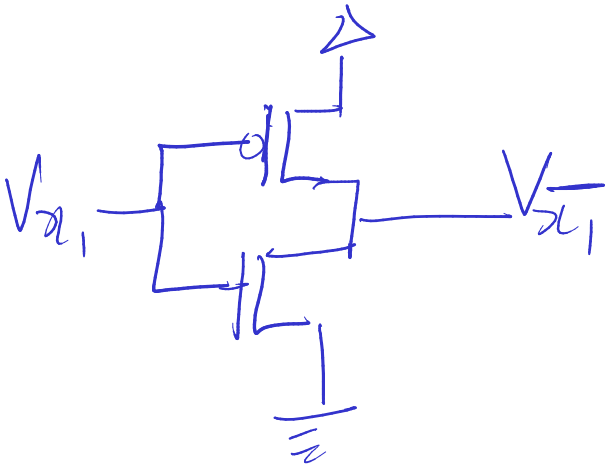


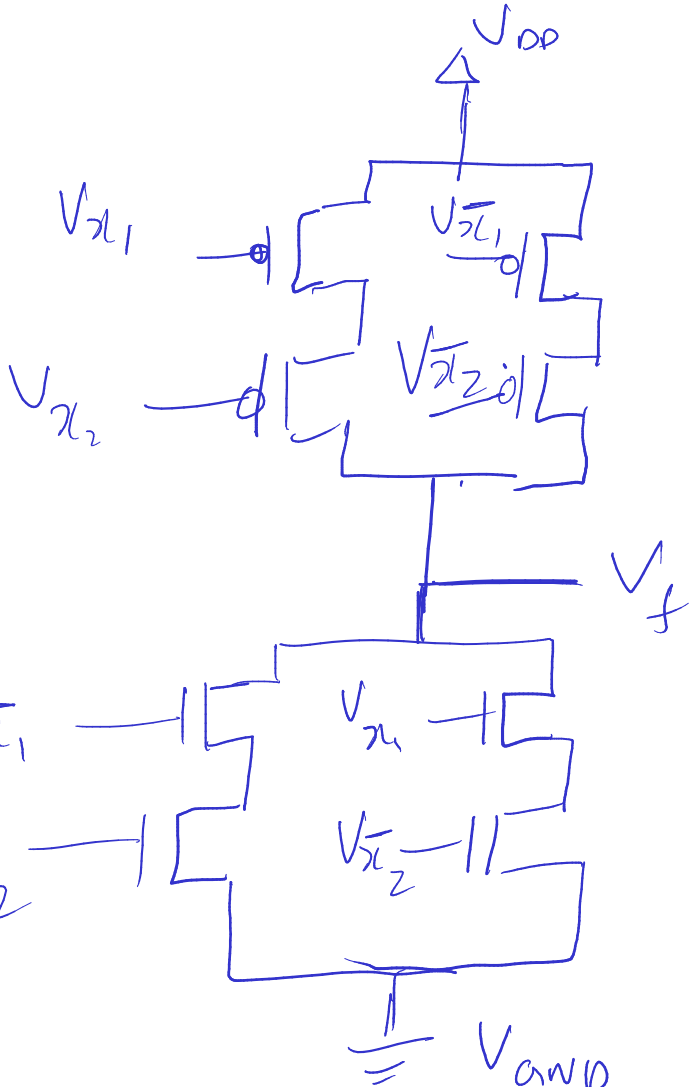
pMOS block design

Design for $g = \bar{x}_1 \bar{x}_2 + x_1 x_2$



$V_{\bar{x}_1}$ and $V_{\bar{x}_2}$ can be obtained from CMOS NOT gates using 2 transistor each





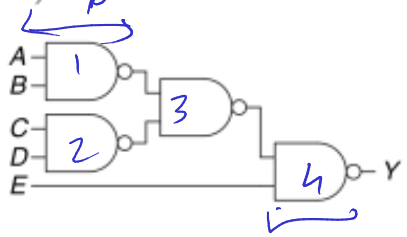
CMOS

Total transistors

$2+2+4+4 = 12$

Problem 11. *Find the propagation delay and contamination delay of the following circuit (5*

marks): t_p



t_{cd_4}

Let the propagation delay of each gate be t_{p_1}, t_{p_2} t_{p_3} t_{p_4} respectively

then

total propagation delay

$= t_{p_4} + t_{p_3} + \max(t_{p_1}, t_{p_2})$

Total contamination delay

$= t_{cd_4}$

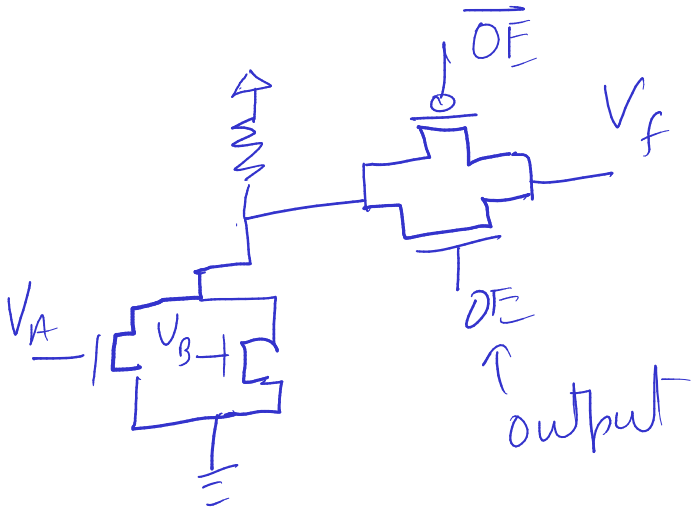
Problem 12

Tristate has 3 possible outputs:
High, Low, high impedance
1, 0, Z

Open collector has 2 possible outputs:
High impedance
Z
and Low = 0

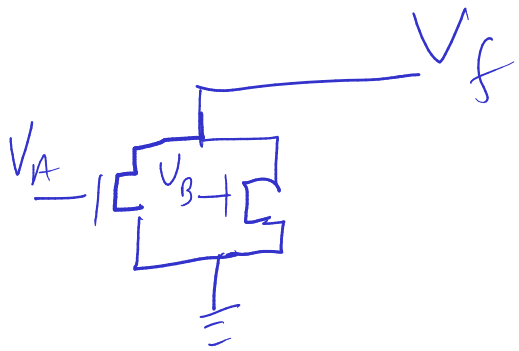
Totem pole has 2 possible outputs:
High and Low
1 0

Tristate NMOS NOR gate



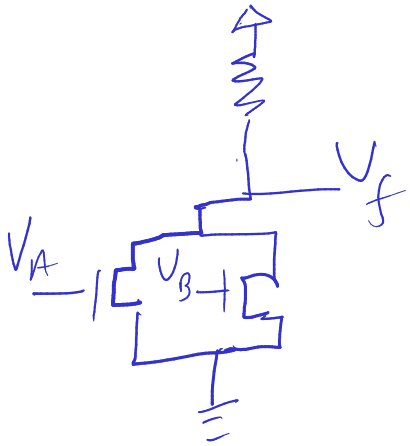
V_A	V_B	$\overline{OE}$	V_f
*	*	L	Z
L	L	H	L
L	H	H	H
H	L	H	H
H	H	H	H

Open collector



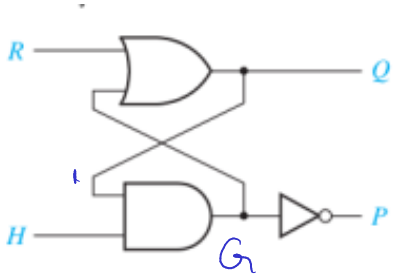
V_A	V_B	V_f
L	L	L
L	H	Z
H	L	Z
H	H	Z

Totem pole



V_A	V_B	V_f
L	L	L
L	H	H
H	L	H
H	H	H

Problem 13

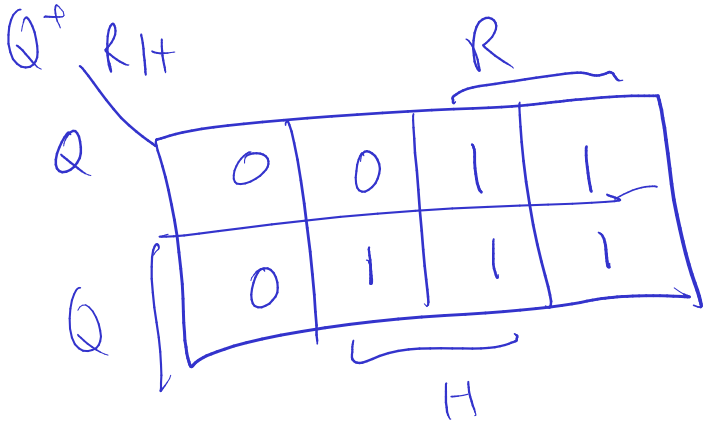


R	H	Q	G	Q^+	G^+
0	0	*	*	0	0
0	1	0/1	0/1	Q	Q
1	0	*	*	1	0
1	1	*	*	1	1

(1) P=Q y R=1, H=0

(2)

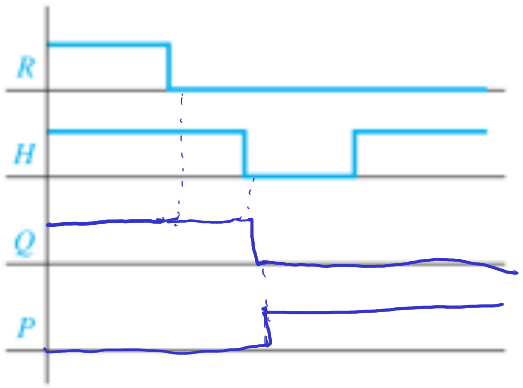
R	H	Q	G	Q^+	G^+
0	0	*	*	0	0
0	1	0/1	0/1	Q	Q
1	0	*	*	1	0
1	1	*	*	1	1



$Q^+ = R + HQ$

characteristic equation

(3)

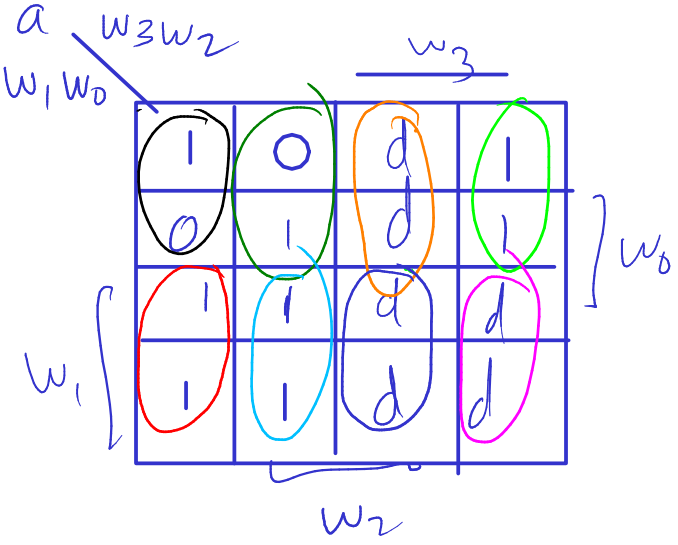


Problem 14. *Figure 1 shows the notation for a BCD to 7-segment display and Table 1 shows the corresponding truth table. The inputs corresponding to the missing rows in the truth table should be considered as don't care.*

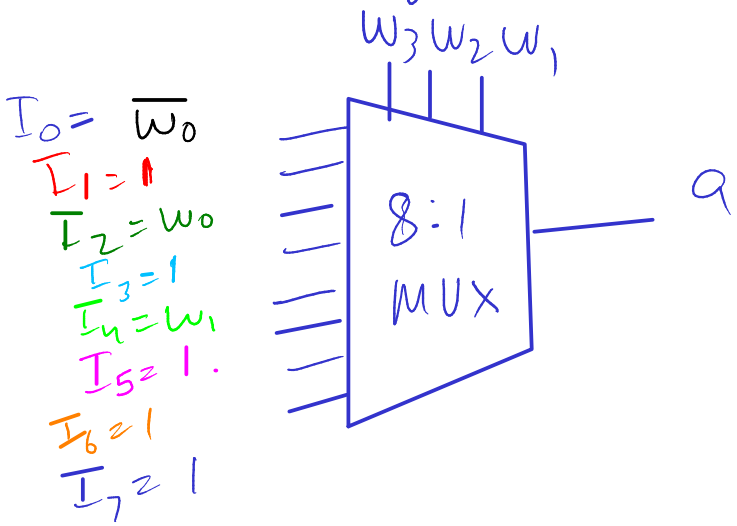
1. *implement segment "a" using an 8:1 mux and no other logic gate, (10 marks)*
2. *implement segment "a" using a 4:1 mux and one other gate, (10 marks)*
3. *implement segment "f" with 4:1 mux and no other logic gate. Assume inputs are available in both uncomplemented and complemented form. (Hint: There are $({}^4C_2 = 6)$ possible pairs of control inputs: (w_3, w_2), (w_2, w_1), (w_1, w_0), (w_0, w_3), (w_0, w_2), (w_1, w_3). There are 6 don't care conditions. With two control inputs of the multiplexer and one input, you can represent an expression with up to 4-SOP-terms of size three-literals or less. You might the arrive at the*

Row	w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

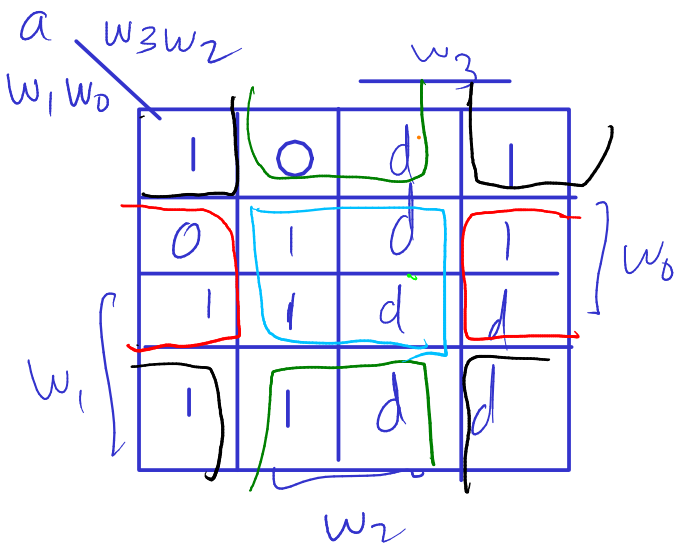
(1) a



Picking $w_3 w_2 w_1$ as the selection lines

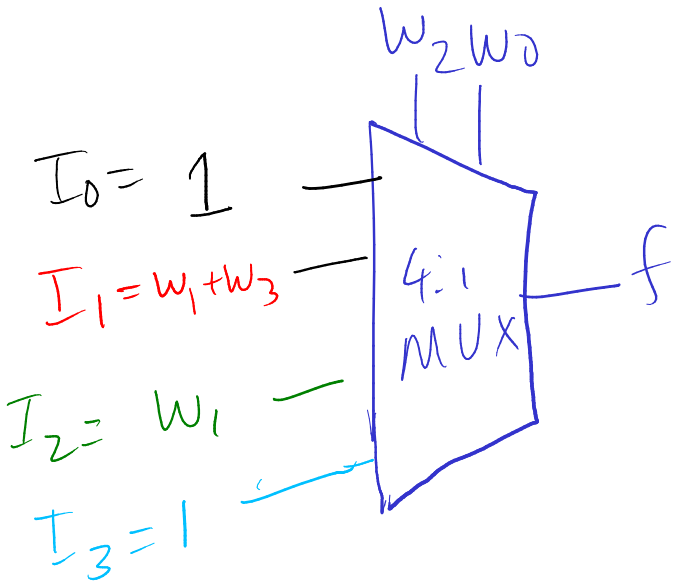


(b)



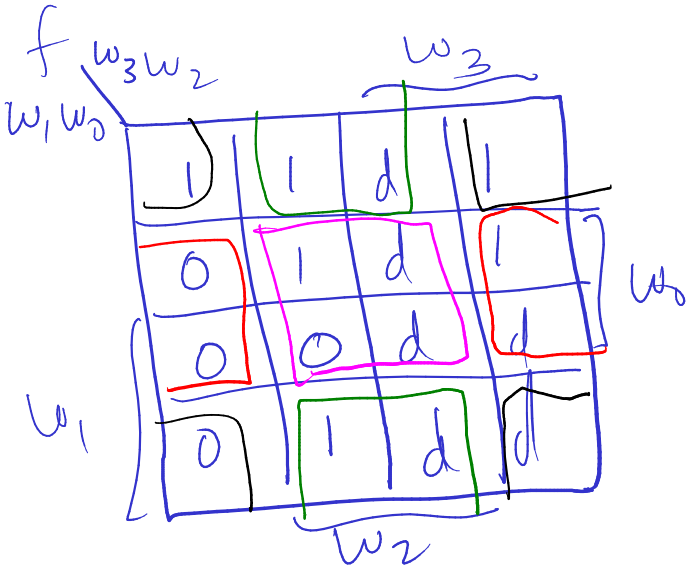
$$a = w_3 + w_1 + \overline{w_0}\,\overline{w_2} + w_0 w_2$$

Picking w_0 and w_2 as selection bits



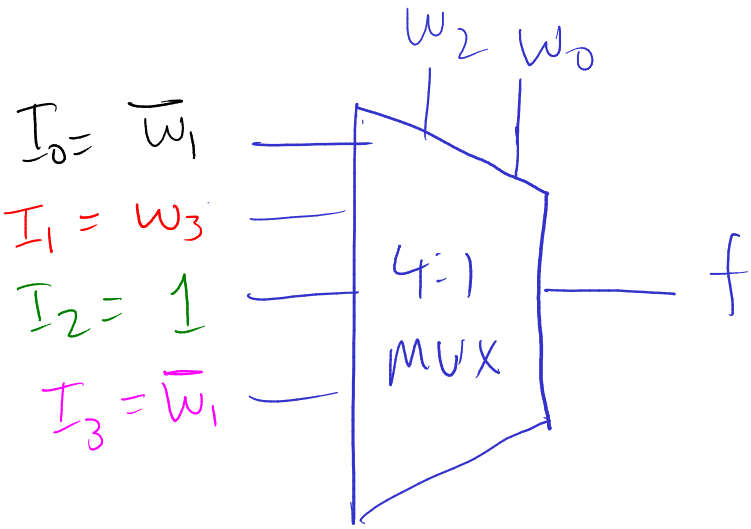
Uses only one other logic gate for $I_1 = w_1 + w_3$

(c)



$$f = w_3 + \bar{w}_0\bar{w}_1 + w_2\bar{w}_0 + w_2\bar{w}_1$$

Pick w_2 and w_0 as the selection bits



This uses no other logic gates.

Problem 15

Not covered in syllabus

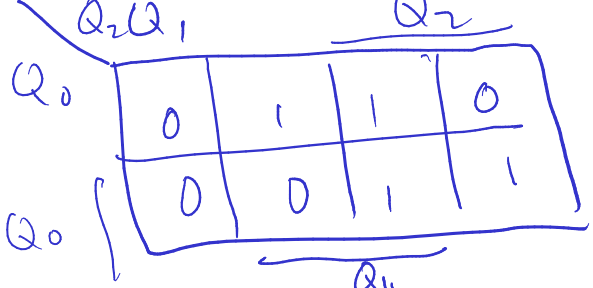
A **gray counter** is one that changes only one bit at a time

	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0

↓ Gray code counting

Q_2 Q_1 Q_0	Q_2^+ Q_1^+ Q_0^+
0 0 0	0 0 1
0 0 1	0 1 1
0 1 0	1 1 0
0 1 1	0 1 0
1 0 0	0 0 0
1 0 1	1 0 0
1 1 0	1 1 1
1 1 1	1 0 1

$D_2 = Q_2^+$



$$D_2 = Q_1\overline{Q_0} + Q_2Q_0$$

$D_1 = Q_1^+$

Q_2Q_1 \ Q_0	00	01	11	10
0	0	1	1	0
1	1	1	0	0

$$D_1 = Q_1\bar{Q}_0 + \bar{Q}_2 Q_0$$

D_0

Q_2Q_1 \ Q_0	00	01	11	10
0	1	0	1	0
1	1	0	1	0

$$D_0 = Q_2Q_1 + \bar{Q}_2\bar{Q}_1$$