

Analog details behind the digital abstraction

Vikas Dhiman for ECE275

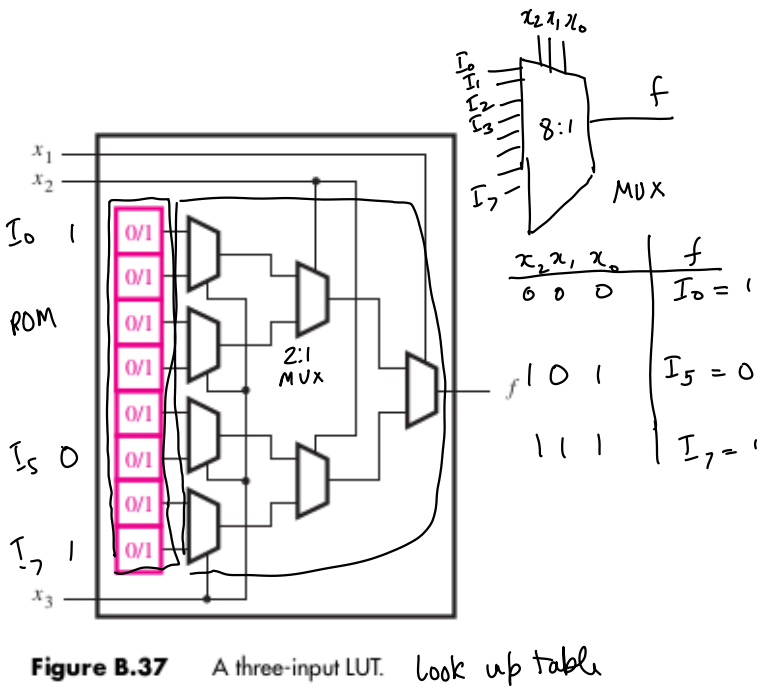
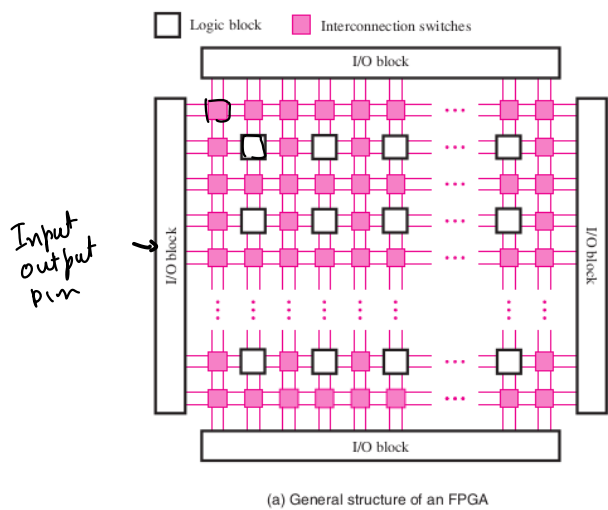
November 17, 2023

Some of the material is out of the textbook. Additional resources include Appendix B of Brown and Vranesic book, “Fundamentals of digital logic.”

1 Objectives

1. Describe how tri-state and open-collector outputs are different from totem-pole outputs
2. Compute noise margin of one device driving the same time

2 FPGA [1, Section B.6.5]



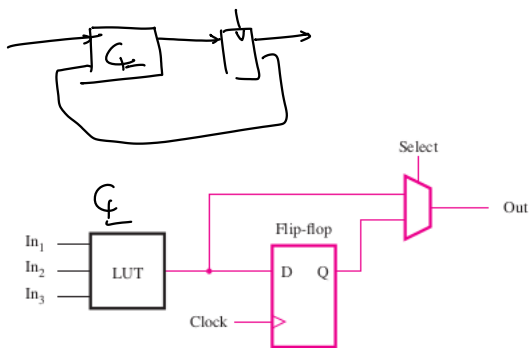


Figure B.38 Inclusion of a flip-flop in an FPGA logic element.

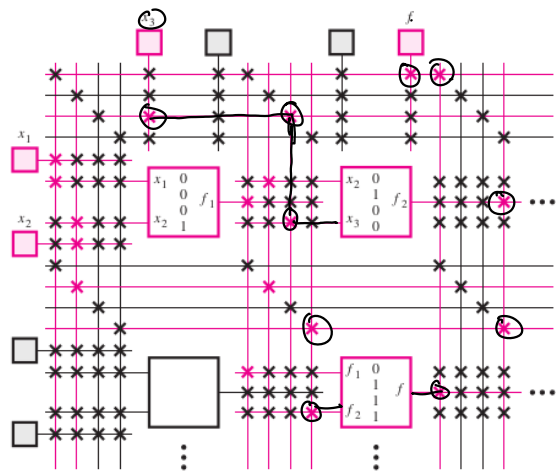


Figure B.39 A section of a programmed FPGA.

Definition 1 (Random Access Memory (RAM)). *Structure of a RAM is as follows:*

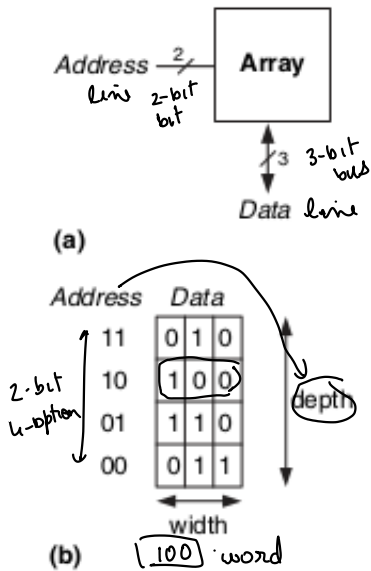


Figure 5.39 4 × 3 memory array: (a) symbol, (b) function

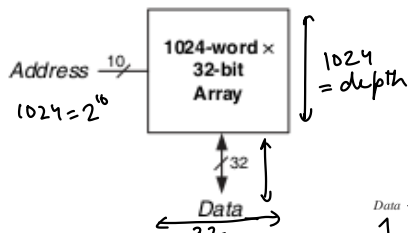


Figure 5.40 32 Kb array: depth = $2^{10} = 1024$ words, width = 32 bits

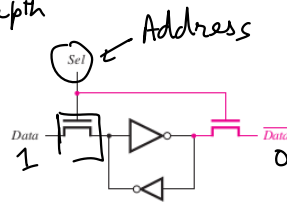
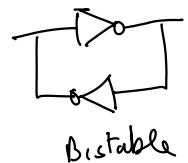


Figure B.64 An SRAM cell.



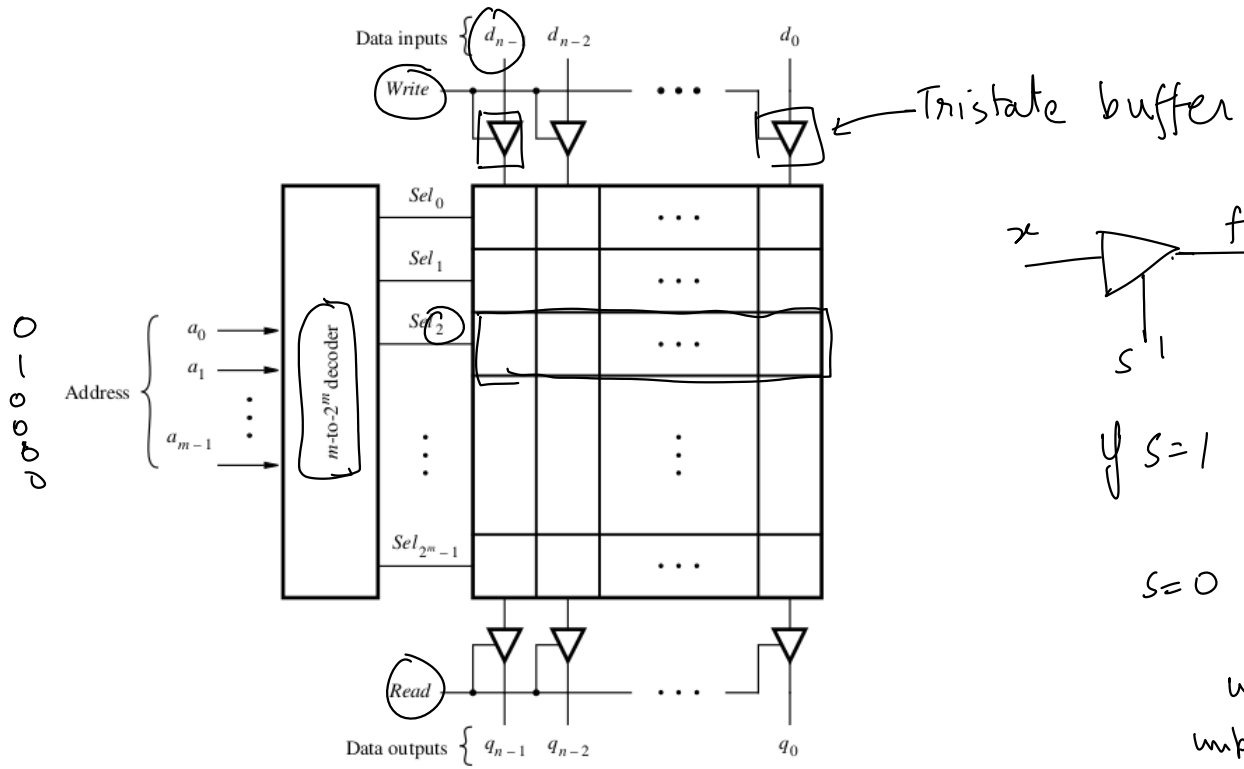
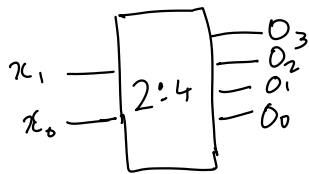


Figure B.66 A $2^m \times n$ SRAM block.

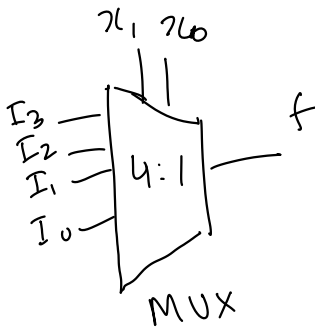
Definition 2 (Read Only Memory (ROM)). Structure of a ROM is as follows:

Decoder



Decoder

3:8, 4:16



x_1	x_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

x_1	x_0	f
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

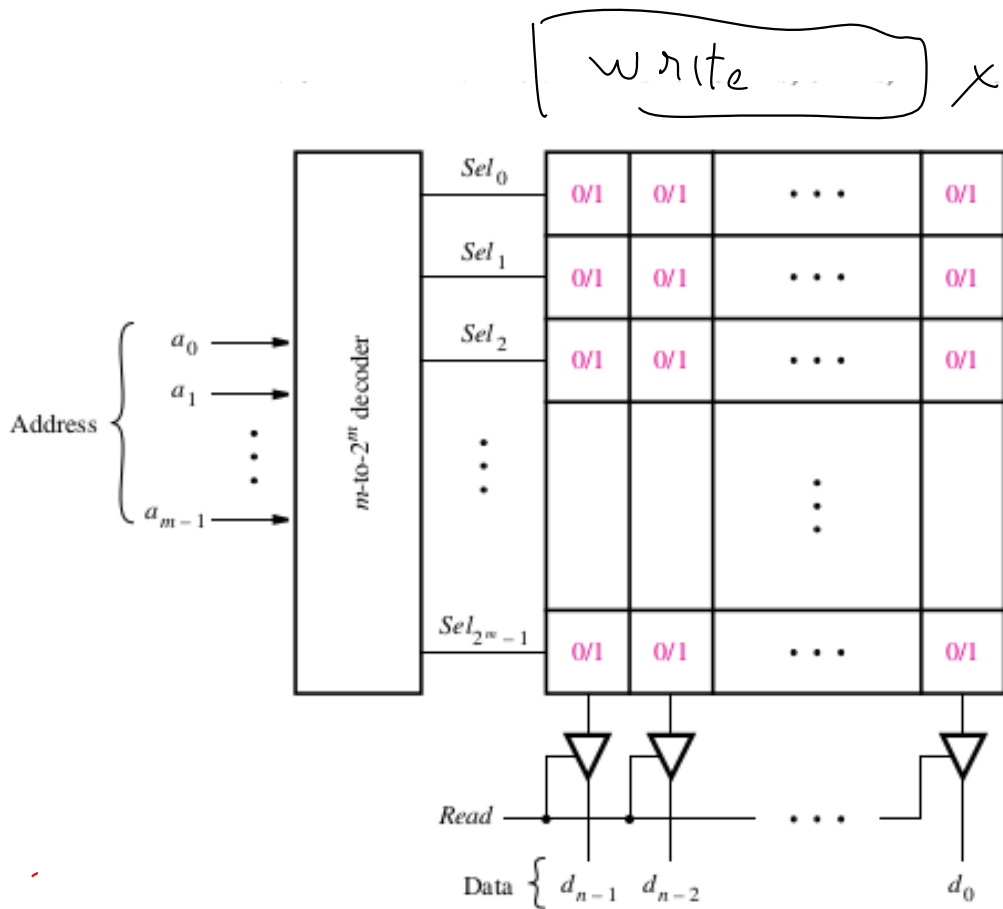
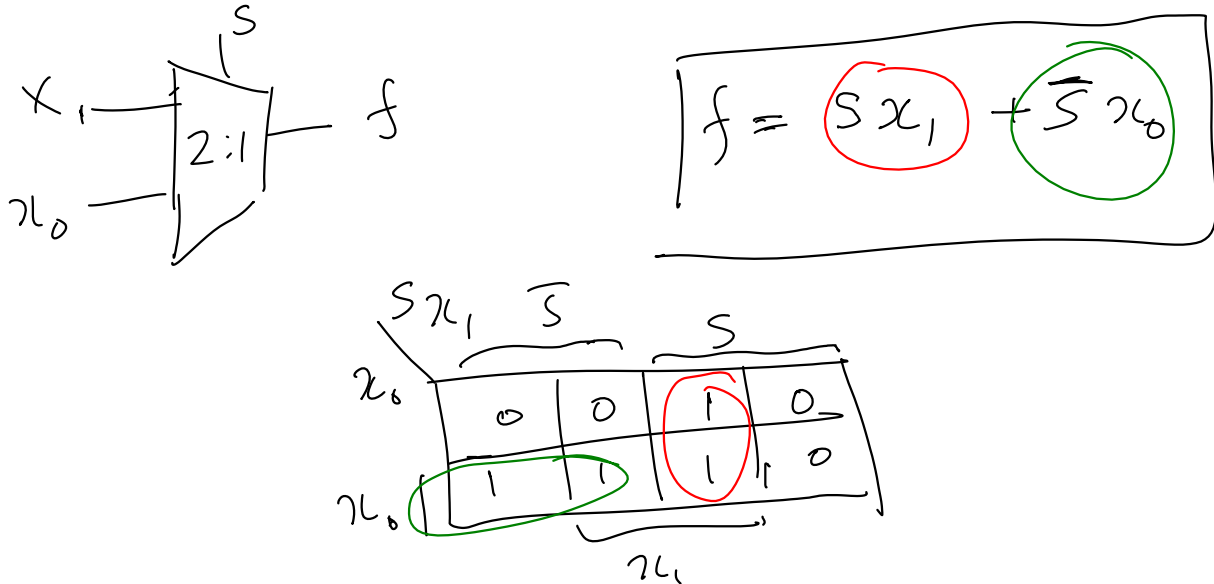
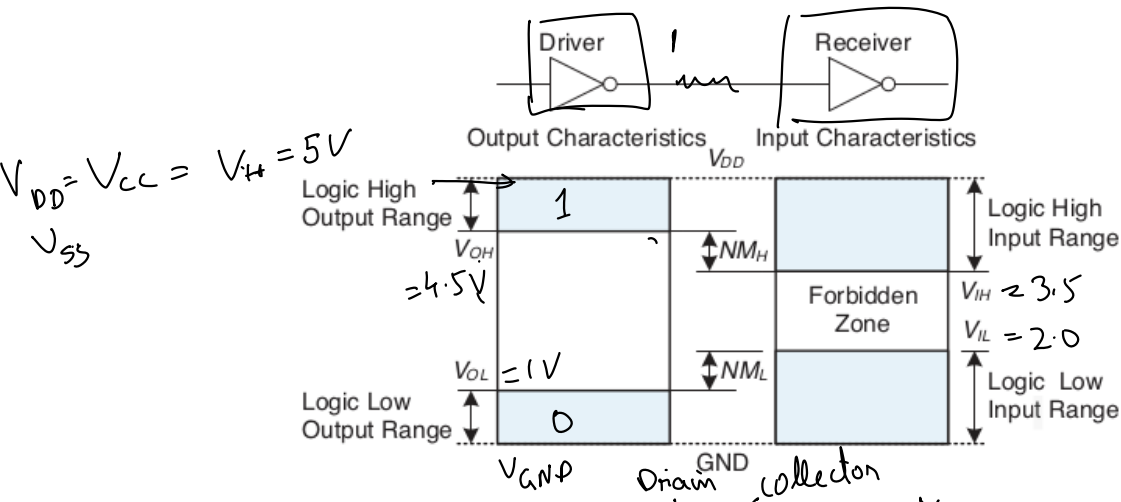


Figure B.72 A $2^m \times n$ read-only memory (ROM) block.

Example 1. Draw a Multiplexer using sum of products form.



3 Logic levels and Noise Margins



Boolean	Voltage
1	5V - 4.5V
0	0V - 1.0V

Positive logic

$$V_{IH} = 3.5V$$

$$V_{IL} = 2.0V$$

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

Definition 3 (Supply Voltage ($V_{DD}/V_{CC}/V_{SS}$)).

The highest voltage a circuit can output

Definition 4 (Ground Voltage (V_{GND})).

The lowest

Definition 5 (Input high (V_{IH}) and Input Low (V_{IL}) of a gate).

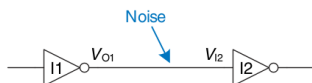
Definition 6 (Output high (V_{OH}) and Output low (V_{OL}) of a gate).

Assume positive logic | for boolean output 1, $V_{OH} \leq V \leq V_{CC}$ | for '1'
Boolean 1 | V_{OH} is the lowest acceptable output voltage for boolean 1
0 | V_{OL} is the highest acceptable output voltage for boolean 0

Definition 7 (Positive logic and Negative logic).

Pos Logic: V_{CC} for 1, V_{GND} for 0
Neg Logic: V_{GND} for 1, V_{CC} for 0

Definition 8 (Noise margins (NM_L and NM_H) of a channel).



Example 2.

If $V_{DD} = 5V$, $V_{IL} = 1.35V$, $V_{IH} = 3.15V$, $V_{OL} = 0.33V$ and $V_{OH} = 3.84V$ for both the "inverters", then what are the low and high noise margins? Can the circuit tolerate 1V of noise at the channel?

$$NM_H = 0.69 = V_{OH} - V_{IH} = 3.84 - 3.15$$

$$NM_L = 1.02 = V_{IH} - V_{IL}$$

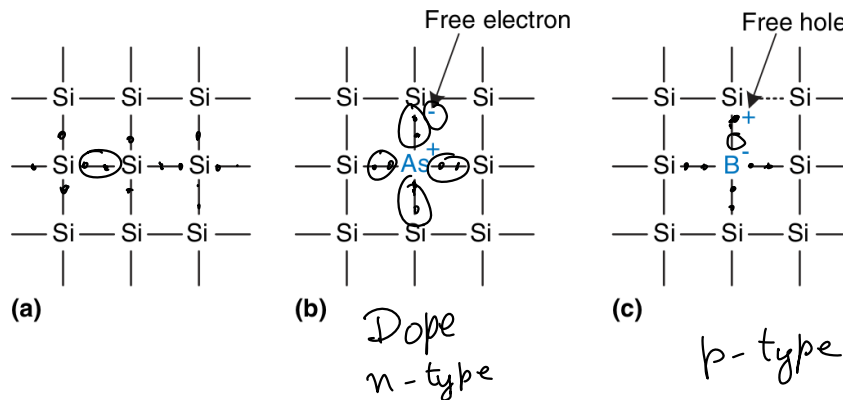
4 Semiconductors and Doping

Not in syllabus but good to know

Elements recognized as metalloids V • T • E

	13	14	15	16	17
2	B Boron	C Carbon	N Nitrogen	O Oxygen	F Fluorine
3	Al Aluminium	Si Silicon	P Phosphorus	S Sulfur	Cl Chlorine
4	Ga Gallium	Ge Germanium	As Arsenic	Se Selenium	Br Bromine
5	In Indium	Sn Tin	Sb Antimony	Te Tellurium	I Iodine
6	Tl Thallium	Pb Lead	Bi Bismuth	Po Polonium	At Astatine

Commonly recognized (86–99%): B, Si, Ge, As, Sb, Te
Irregularly recognized (40–49%): Po, At
Less commonly recognized (24%): Se
Rarely recognized (8–10%): C, Al
(All other elements cited in less than 6% of sources)
 Arbitrary metal-nonmetal dividing line: between Be and B, Al and Si, Ge and As, Sb and Te, Po and At



ECE 341
Nuri

5 MOSFET: Metal Oxide Field Effect Transistors

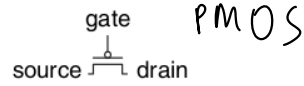
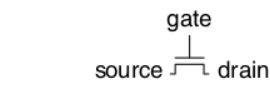
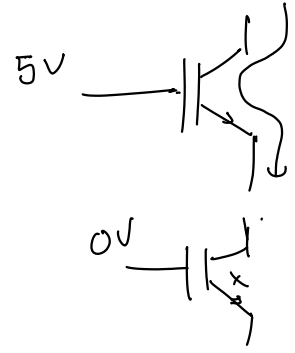
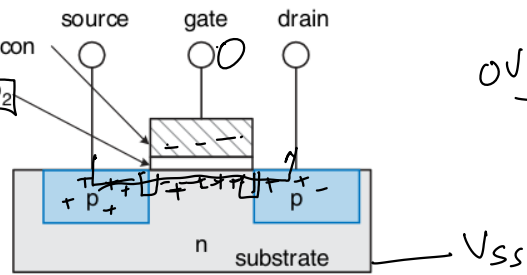
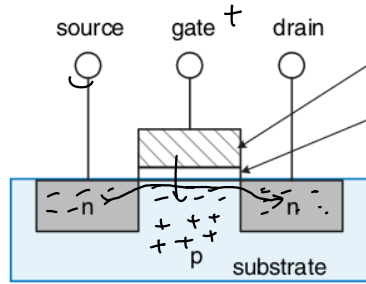
Not in syllabus but good to know

MOSFET

nMOS

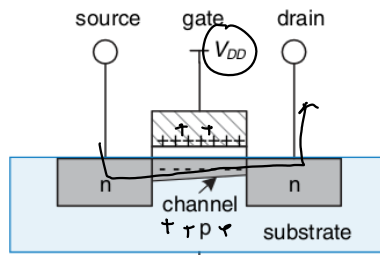
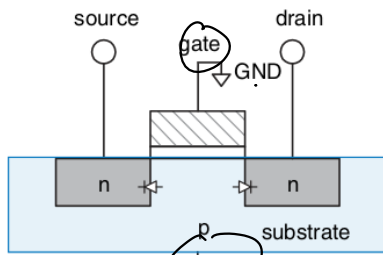
pMOS

Field



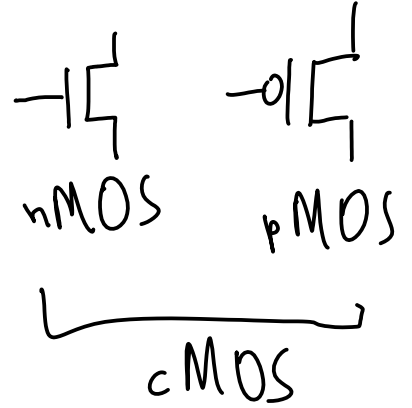
(a) nMOS

(b) pMOS

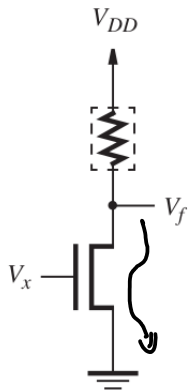


(a)

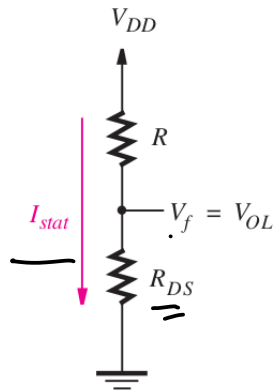
(b)



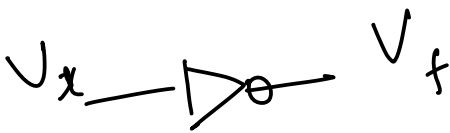
6 DC Transfer characteristic



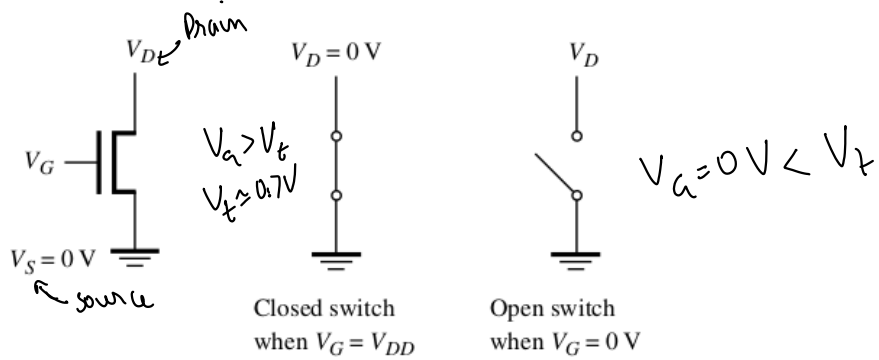
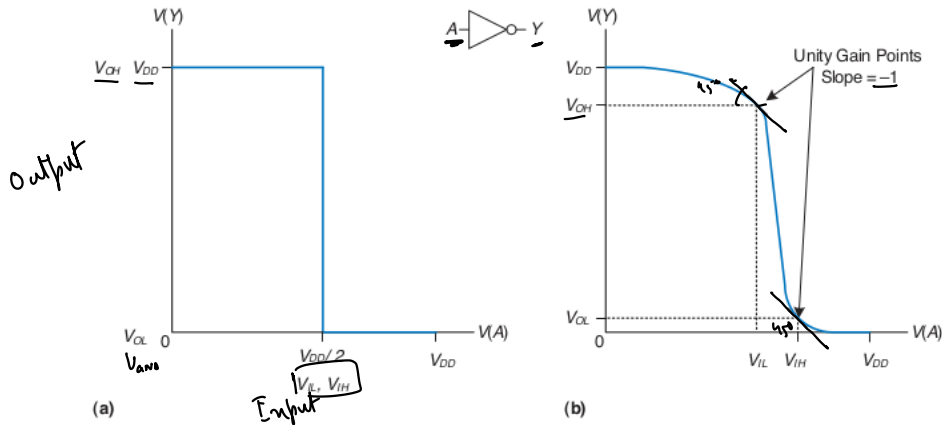
(a) NMOS NOT gate



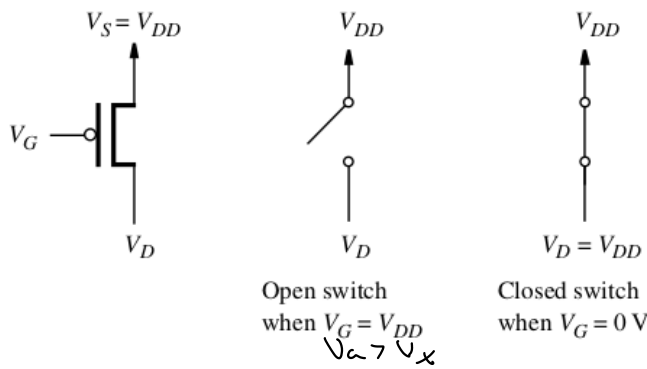
(b) $V_x = 5\text{ V}$



Ideal gate

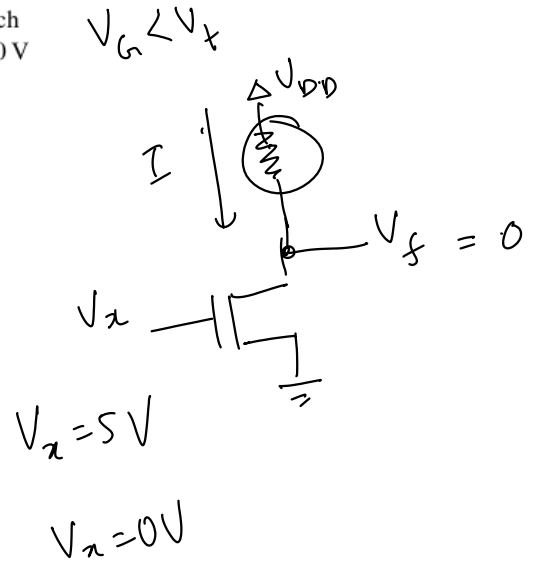


(a) NMOS transistor



(b) PMOS transistor

Example 3. Draw a NOT gate using nMOS transistors.

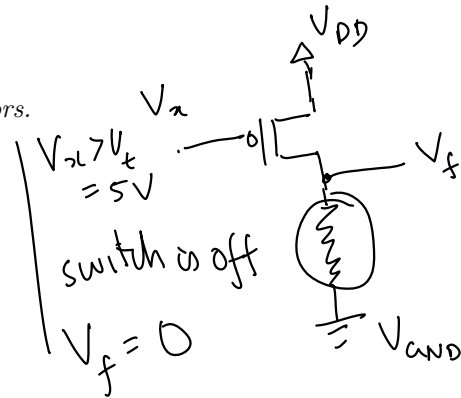


Example 4. Draw a NOT gate using pMOS transistors.

When $V_x < V_t = 0$

the transistor switch is ON

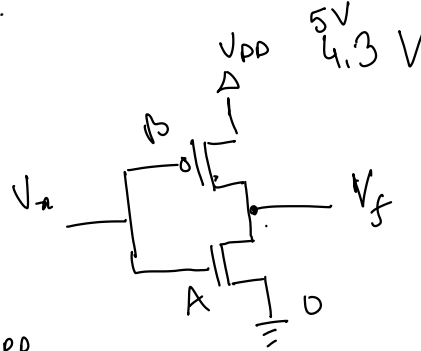
$$V_f = V_{DD} = 5V$$



Remark 1. nMOS transistors pass 0's well (output between 0 and $V_{DD} - V_t$). pMOS transistors pass 1's well (output between V_t and V_{DD}).

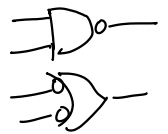
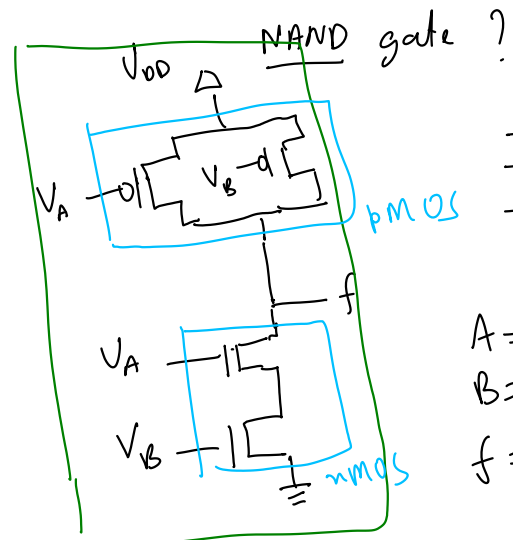
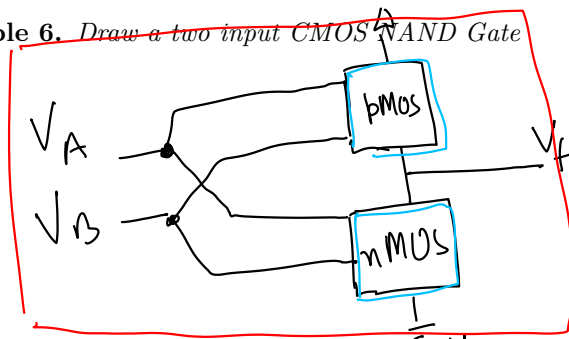
Example 5. Draw CMOS NOT Gate.

Complementary MOS gates



$V_x > V_t = 5V$
nMOS switch (A)
is turned on
pMOS switch (B)
is OFF

Example 6. Draw a two input CMOS NAND Gate



$$A = 1$$

$$B = 1$$

$$f = \overline{A \cdot B}$$

$$= 0$$

Definition 9 (Negative logic).

Boolean	Positive logic	Negative logic
0	Low	High
1	High	Low

Example 7. Analyze the above circuit under negative logic.

V_A	V_B	V_f
L	L	H
L	H	H
H	L	H
H	H	L

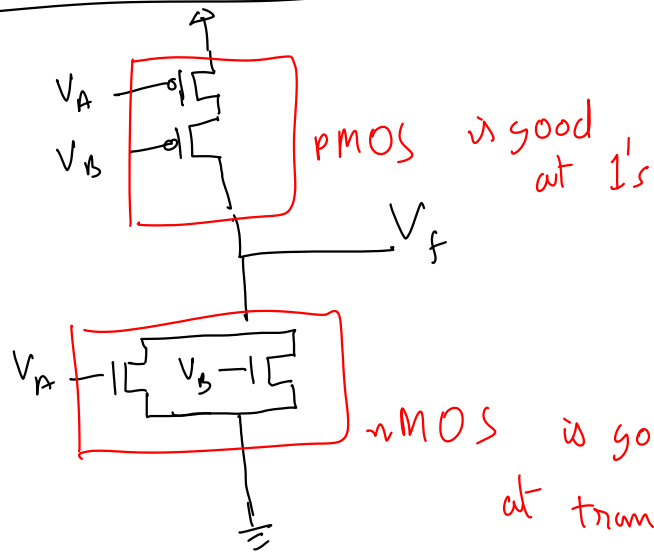
A	B	F
1	1	0
1	0	0
0	1	0
0	0	1

NOR gate

Example 8. Draw a three input NAND using CMOS.

Draw a CMOS NOR gate

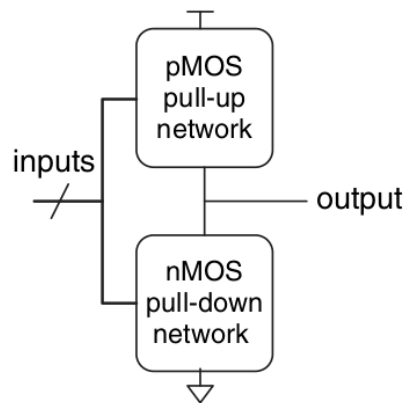
$H = 5V$
 $L = 0V$



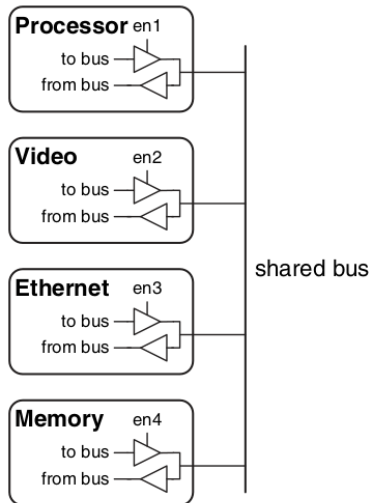
V_A	V_B	V_f
L	L	H
L	H	L
H	L	L
H	H	L

Example 9. Draw a three input NOR using CMOS.

Example 10. Draw a two input AND gate using CMOS.



6.1 Gates with floating output



Definition 10 (Transmission gate). *Draw a schematic of transmission gate and truth table for transmission gate. What is its commonly used symbol?*

Definition 11 (Tristate buffer). *What is tristate buffer? Draw its symbol and truth table? Where is it used?*

Example 11. *Draw a Multiplexer using transmission gates.*

Example 12. *Draw a Multiplexer using tristate buffers.*

Definition 12 (Totem-pole). *Draw a Push-pull (or Totem-pole) output NAND gate using CMOS. Can you connect this gate to a shared bus?*

Definition 13 (Tristate). *Draw a Tristate output NAND gate using CMOS with an output enable (OE) input. Can you connect this gate to a shared bus?*

Definition 14 (Open-collector). *Draw a open-collector output NAND gate. Can you connect this gate to a shared bus?*

7 Verilog truth tables

Table 11-11—Bitwise binary AND operator

&	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

Table 11-12—Bitwise binary OR operator

	0	1	x	z
0	0	1	x	x
1	1	1	1	1
x	x	1	x	x
z	x	1	x	x

References

- [1] Brown Stephen and Vranesic Zvonko. *Fundamentals of digital Logic with Verilog design*. McGraw Hill, 2022.