Sequential logic design: More terminology

Vikas Dhiman for ECE275

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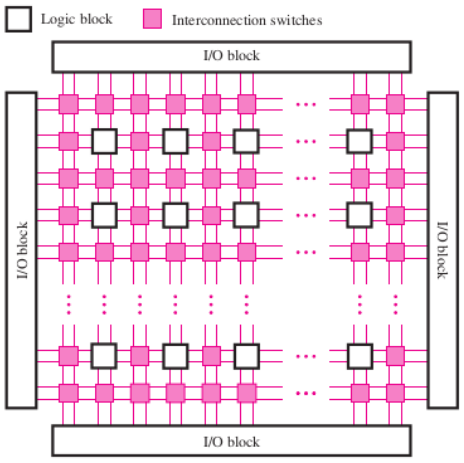
1 FPGA [2, Section B.6.5]



(a) General structure of an FPGA

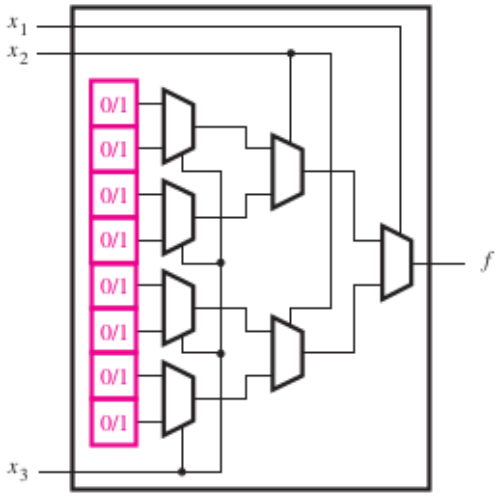


Figure B.37 A three-input LUT.

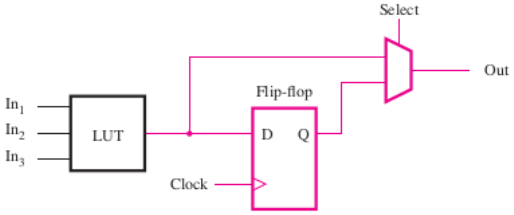


Figure B.38 Inclusion of a flip-flop in an FPGA logic element.

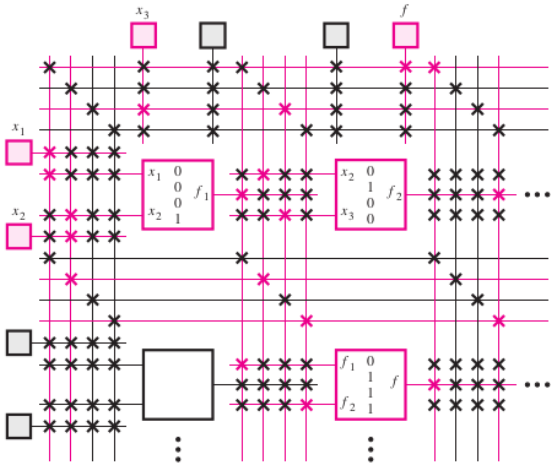
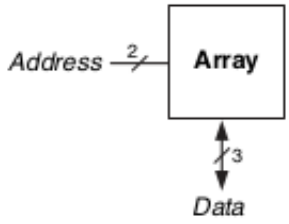


Figure B.39 A section of a programmed FPGA.

Definition 1 (Random Access Memory (RAM))**.** *Structure of a RAM is as follows:*



(a)

(b)

Figure 5.39 4 × 3 memory array: (a) symbol, (b) function

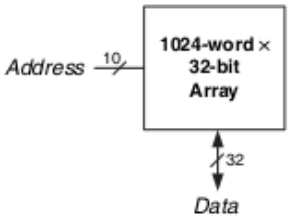


Figure 5.40 32 Kb array: depth = 2^{10} = 1024 words, width = 32 bits

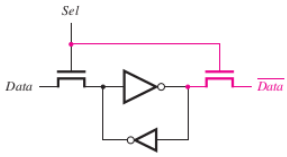


Figure B.64 An SRAM cell.

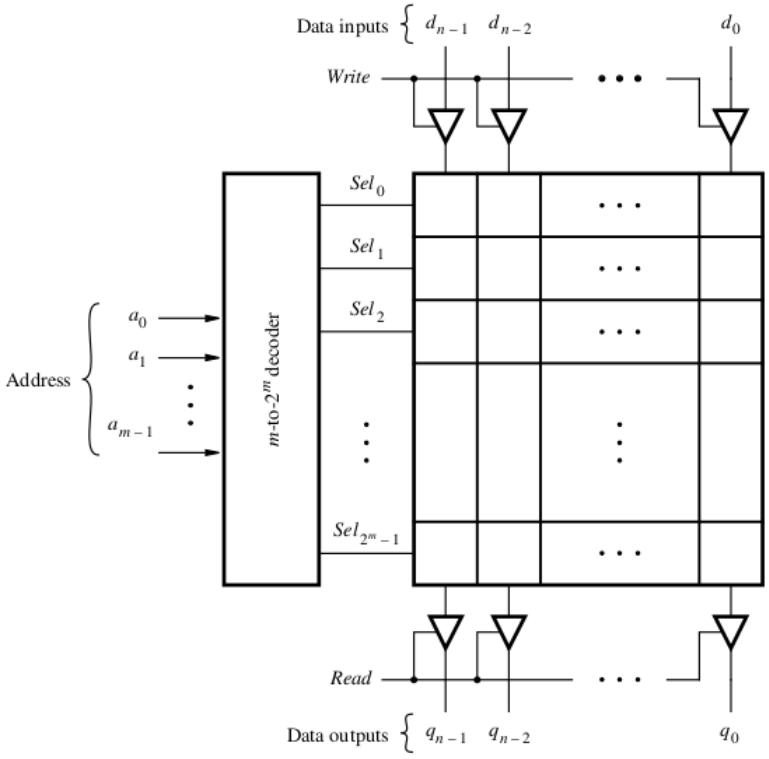


Figure B.66 A $2^m \times n$ SRAM block.

Definition 2 (Read Only Memory (ROM))**.** *Structure of a ROM is as follows:*

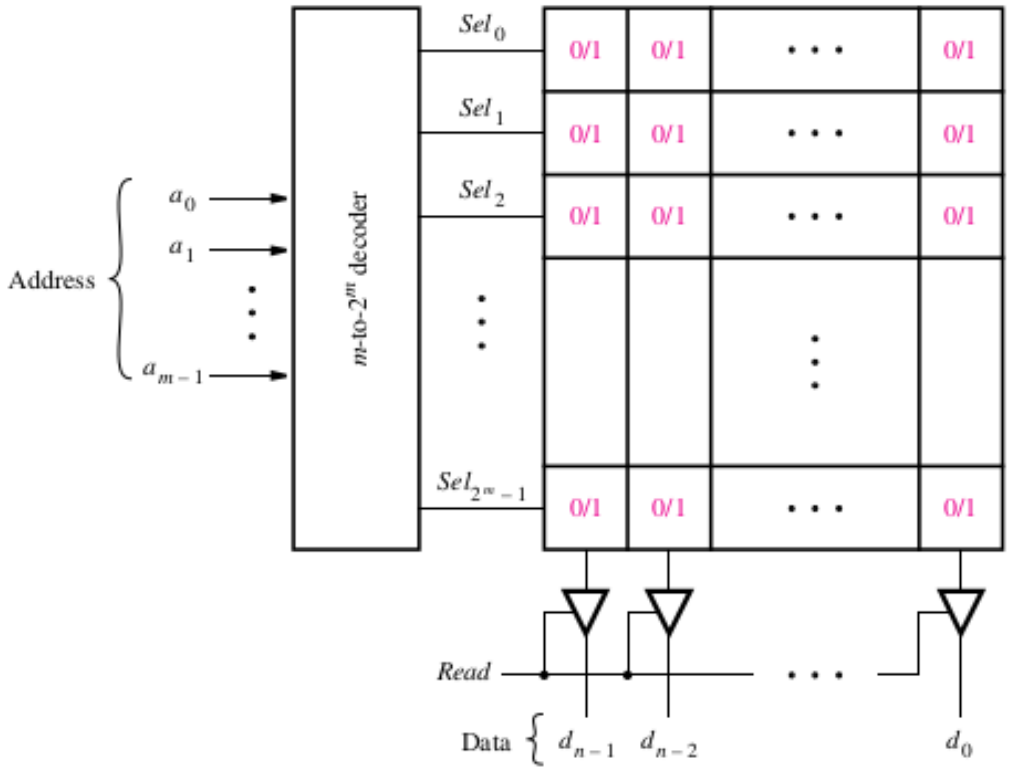
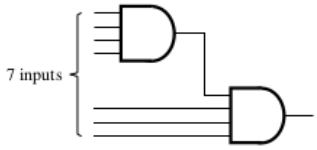


Figure B.72 A $2^m \times n$ read-only memory (ROM) block.

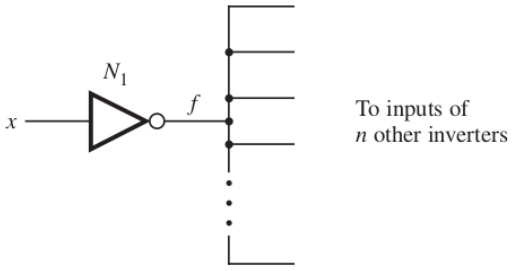
Definition 3 (Fan-in)**.** *The fan-in of a logic gate is number of inputs to a logic gate. [2, Section B.8.9]*



Remark 1 (Fan-in)**.** *The fan-in of a gate is limited by the propagation delay t_p. Higher the fan-in, higher the t_p. The output voltage thresholds like V_{OL} and V_{OH} also limit fan-in. Higher the fan-in, higher is V_{OL} (and lower is the V_{OH}).*

Example 1. *Implement an OR gate with fan-in of 7 using OR gates with fan-in of 3.*

Definition 4 (Fan-out)**.** *The fan-out of a logic gate is the maximum number of other gates that can be connected to output of a gate. [2, Section B.8.9]*



Definition 5 (Programmable Logic Array (PLA)). *Structure of a PLA:*

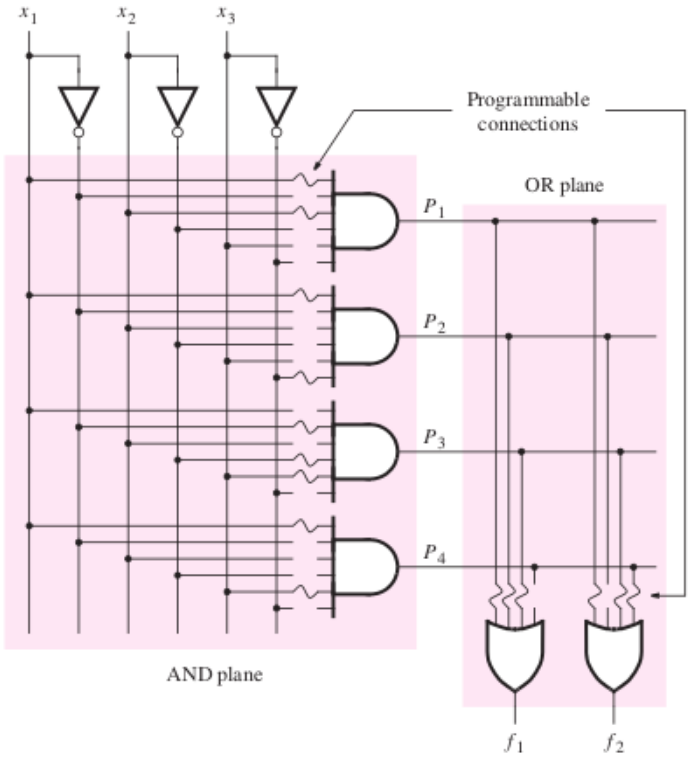


Figure B.26 Gate-level diagram of a PLA. *[2, Section B.6.1]*

Definition 6 (Programmable Array Logic (PAL)). *Structure of a PAL:*

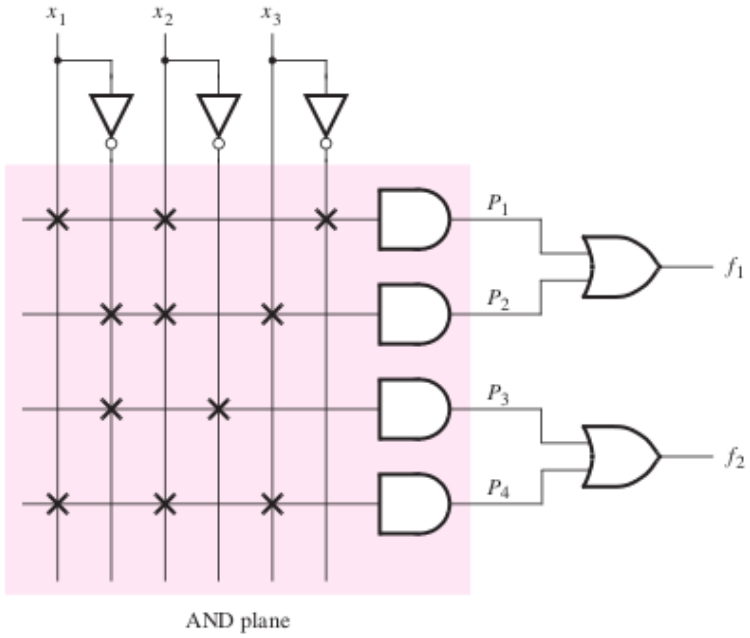
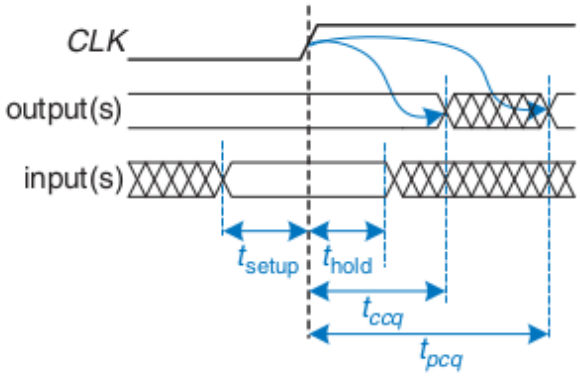


Figure B.28 An example of a PAL.

[2, Section B.6.2]

Example 2. *What is the difference between PLA and PAL?*

2 Timing parameters for sequential circuit [1, Section 3.5]



Definition 7 (Setup time t_{su} of a latch/flip-flop)**.** *Time for which input must be stable before the clock edge.*

Definition 8 (Hold time t_h of a latch/flip-flop)**.** *Time for which input must be stable after the clock edge.*

Definition 9 (Clock-to-Q contamination delay t_{ccq} of a latch/flip-flop)**.** *Time taken to influence (contaminate) the Q output after the clock edge.*

Definition 10 (Clock-to-Q propagation delay t_{ccq} of a latch/flip-flop)**.** *Time taken for Q output to stabalize after the clock edge.*

References

[1] Sarah L Harris and David Harris. *Digital design and computer architecture*. Morgan Kaufmann, 2022.

[2] Brown Stephen and Vranesic Zvonko. *Fundamentals of digital Logic with Verilog design*. McGraw Hill, 2022.