MUX/DEC Sequential logic design

Vikas Dhiman for ECE275
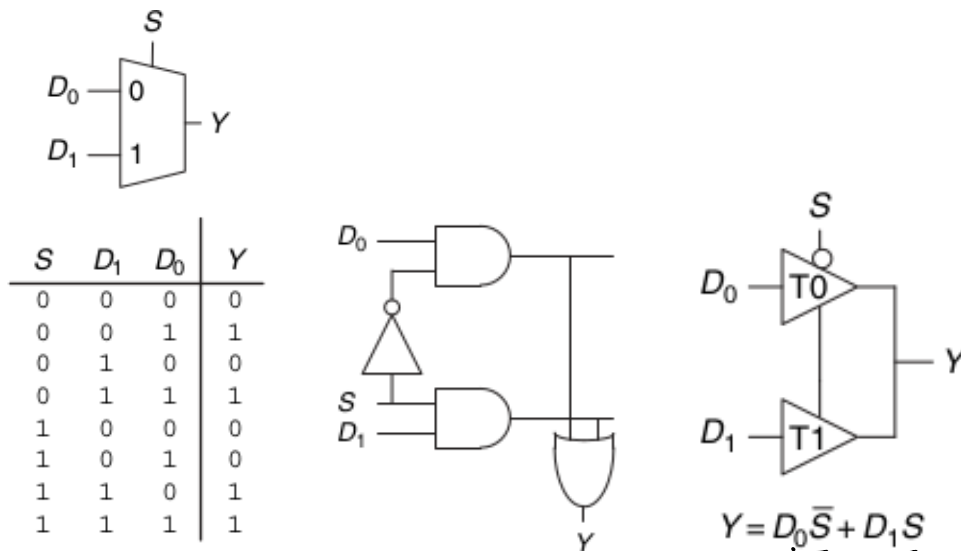
December 1, 2023

1 Objectives

1. Design combinational circuits using multiplexers and decoders
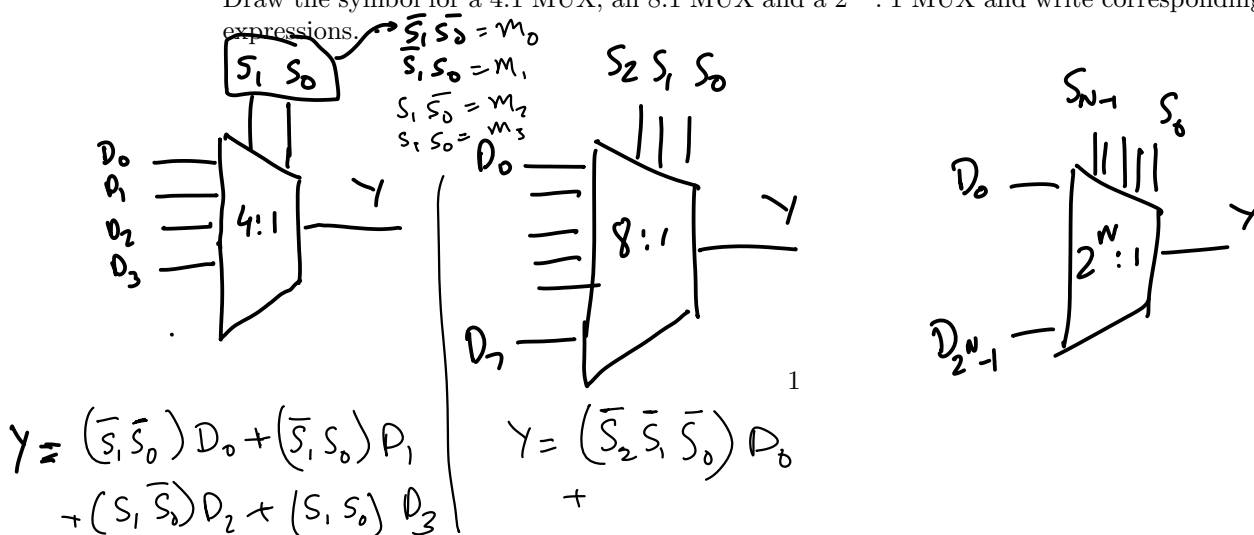
2 Design combinational circuit using multiplexers [1, Section 2.8.1]

2.1 Review: 2to1 Multiplexer (MUX)

S	D_1	D_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$$Y = D_0\bar{S} + D_1 S$$

2.2 Wider multiplexers

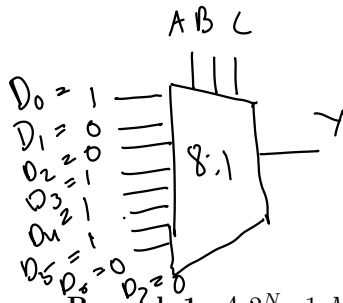Draw the symbol for a 4:1 MUX, an 8:1 MUX and a $2^N : 1$ MUX and write corresponding Boolean expressions.

$\bar{S_1}\,\bar{S_0} = M_0$
$\bar{S_1}S_0 = M_1$
$S_1\bar{S_0} = M_2$
$S_1 S_0 = M_3$

$$Y = (\bar{S_1}\bar{S_0})D_0 + (\bar{S_1}S_0)D_1 + (S_1\bar{S_0})D_2 + (S_1 S_0)D_3$$

$$Y = (\bar{S_2}\bar{S_1}\bar{S_0})D_0 +$$

1

$m_5 \quad m_4$

$A\bar{B}C + A\bar{B}\bar{C}$ usms 4:1 MUX + gate

$\underset{m_3}{\underbrace{}}$

Example 1. *Design a circuit for* $Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$ *using a 8:1 MUX.*

$\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$
$m_0 \qquad m_4$

A B C

$D_0 = 1$
$D_1 = 0$
$D_2 = 1$
$D_3 = 1$
$D_4 = 1$
$D_5 = 0 \quad D_6 = 0 \quad D_7 = 0$

8:1 → Y

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

$Y = D_0$
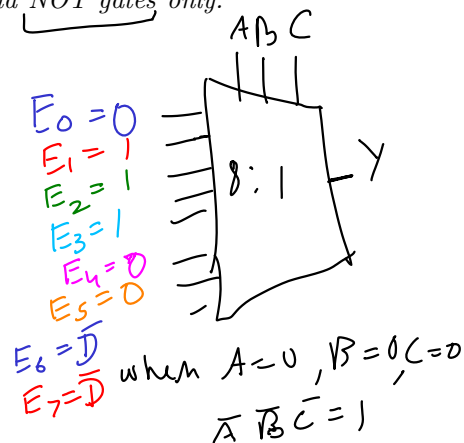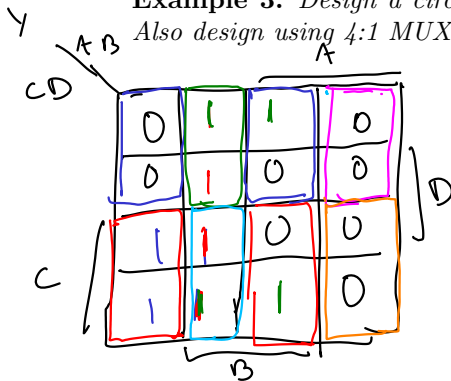$Y = D_1$
$Y = D_7$

Remark 1. *A* $2^N : 1$ *MUX can be used to program any N-input logic function.*

Example 2. *Design a circuit for* $Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$ *using a 4:1 MUX and NOT gates only.*

A B   BC   CA
C   A   B

Y   AB $\bar{A}\bar{B}$ A

$\bar{C}$	00	01	11	01
	1	0	0	1
C	0	1	0	1

$D_0 = \bar{C}$

A B

4:1
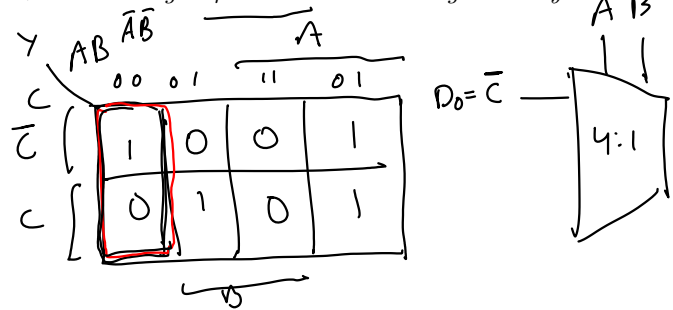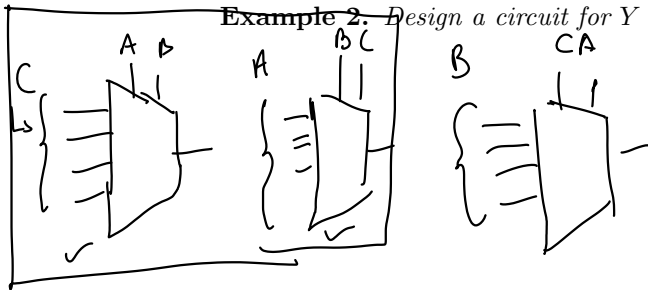
Remark 2. *A* $2^{N-1} : 1$ *MUX can be used to program any N-input logic function, if we use literals on the input side.*
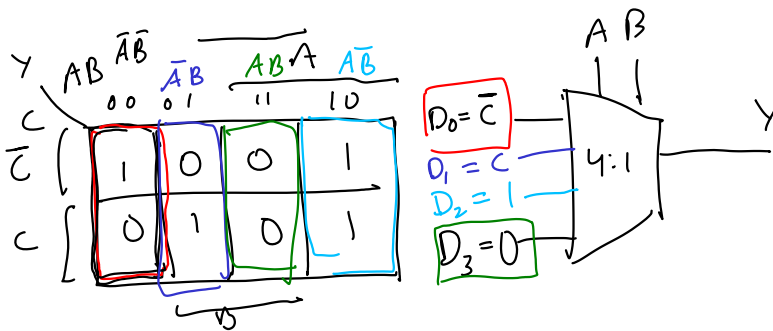
Example 3. *Design a circuit for* $Y = \bar{A}C + \bar{A}B + B\bar{D}$ *using a 8:1 MUX and NOT gates only. Also design using 4:1 MUX and other gates. fewest gates.*

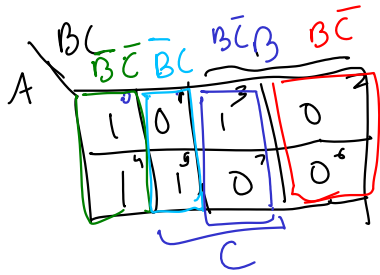4 var

Y
AB
CD

A

0	1	1	0
0	1	0	0
1	1	0	0
1	1	1	0

D

C

B

ABC

$E_0 = 0$
$E_1 = 1$
$E_2 = 1$
$E_3 = 1$
$E_4 = 0$
$E_5 = 0$
$E_6 = \bar{D}$
$E_7 = \bar{D}$

8:1 → Y

when $A=0$, $B=0$ $C=0$
$\bar{A}\bar{B}\bar{C} = 1$

3 Encoders and Decoders

Example 4. *Draw the symbol and the truth table for 2:4 decoder. Also write the logic expressions.*

Example 5. *Draw the symbol and the truth table for 3:8 decoder, 4:16 decoder and* $N : 2^N$ *decoder. Also write the logic expressions.*
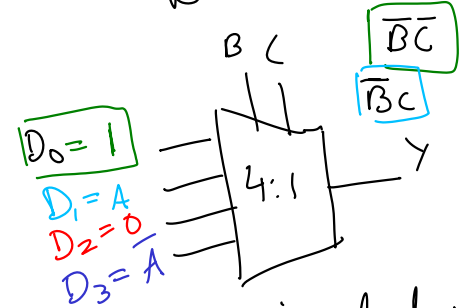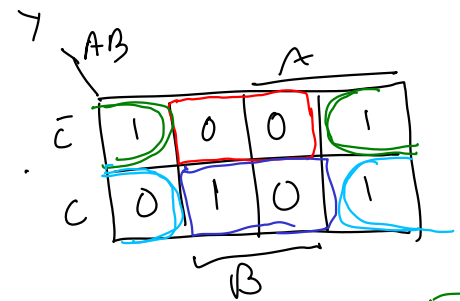
Top-left K-map:

Y $\quad$ AB $\bar{A}\bar{B}$	$\bar{A}B$	AB A	$A\bar{B}$
C $\bar{C}$	00 01	11	10
$\bar{C}$	1	0	0	1
C	0	1	0	1

$D_0 = \bar{C}$
$D_1 = C$
$D_2 = 1$
$D_3 = 0$

4:1 MUX with select A B, output Y

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + AB\cdot 0 + A\cdot\bar{B}\cdot 1$$

$$Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$$

Bottom-left K-map:

A $\quad$ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC B	$B\bar{C}$
	1	0	1	0
	1	1	0	0

Truth table:

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Top-right K-map:

Y $\quad$ AB		A	
$\bar{C}$	1	0	0	1
C	0	1	0	1

B

Right MUX:

$D_0 = 1$
$D_1 = A$
$D_2 = 0$
$D_3 = A$

4:1 MUX with select B C, output Y

$\overline{B}\overline{C}$
$\overline{B}C$

$Y = D_0$ is selected
when $B=0$, $C=0$
when $\bar{B}\bar{C} = 1$

$B=0$ $\quad C=1$
$\bar{B}C = 1$

Example 6. *Design a circuit for a XOR gate using a 2:4 decoder and an OR gate.*

Example 7. *Design a circuit for $Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$ using a 3:8 decoder and an OR gate.*

3.1   (Priority) Encoders

Example 8. *Draw symbol and truth table for a 4:2 priority encoder.*

Example 9. *Draw symbol and truth table for a 8:3 priority encoder.*

References

[1] Sarah L Harris and David Harris. *Digital design and computer architecture*. Morgan Kaufmann, 2022.