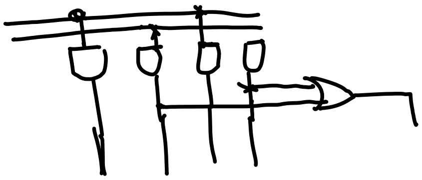
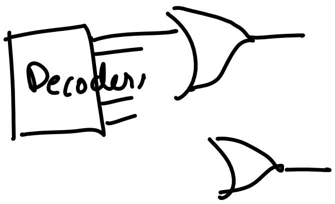
1980s-90s PLA



Chapter 6

Muxes and Decoders

Sometimes building blocks of circuit can be larger than simple gates.
Having larger building blocks reduces the number of inter-connection switches.

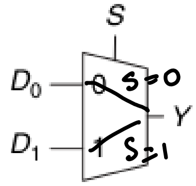


6.1 Objectives

1. Design combinational circuits using multiplexers and decoders

6.2 Design combinational circuit using multiplexers [1, Section 2.8.1]

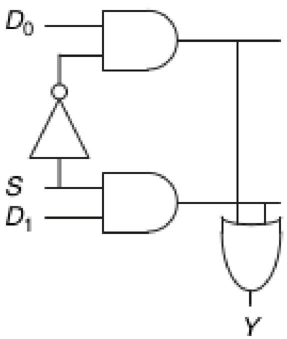
6.2.1 Review: 2to1 Multiplexer (MUX)

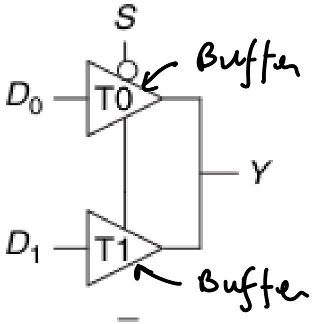


S	Y
0	D_0
0	D_1

S_0	D_1	D_0	Y
0	0	0	0
0	0	1	1
	⋮		0
			1
			0
			0
			1
1	1	1	1

S	D_1	D_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



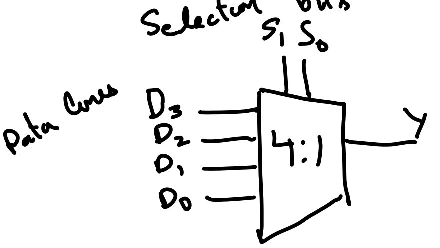


$Y = D_0\overline{S} + D_1 S$

$$Y = S D_1 + \overline{S} D_0$$

6.2.2 Wider multiplexers

Draw the symbol for a 4:1 MUX, an 8:1 MUX and a 2^N : 1 MUX and write corresponding Boolean expressions.

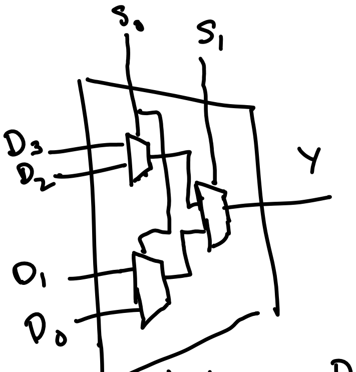


S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$Y = \underbrace{\overline{S}_1 \overline{S}_0}_{m_0} D_0 + \underbrace{\overline{S}_1 S_0}_{m_1} D_1 + S_1 \overline{S}_0 D_2 + S_1 S_0 D_3$$

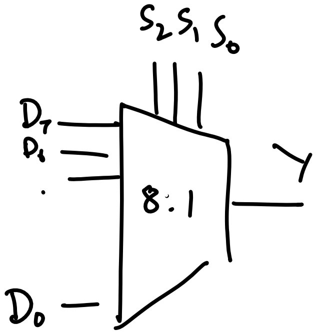
$2 = \log_2(4)$

$2^2 = 4$

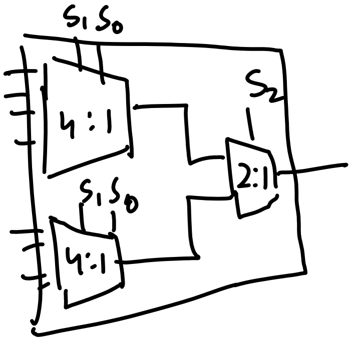


4:1

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



$3 = \log_2(8) \Leftrightarrow 2^3 = 8$

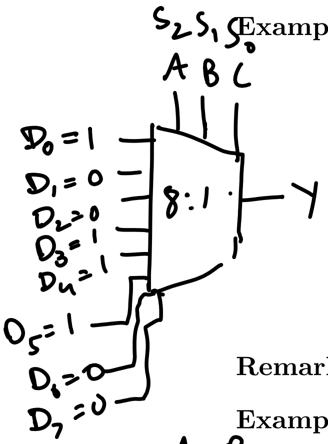


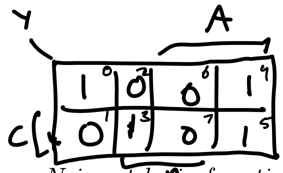
8:1

3 $2^3:1$

Example 6.1. *Design a circuit for* $Y = \underline{A\bar{B} + \bar{B}\bar{C}} + \bar{A}BC$ *using a 8:1 MUX.*

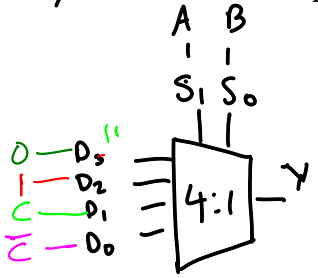
A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	





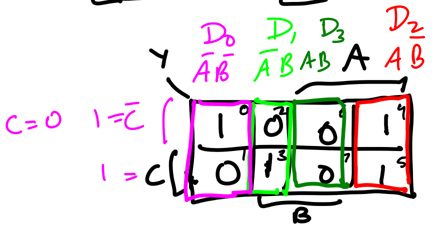
Remark 6.1. *A* $2^N : 1$ *MUX can be used to program any N-input logic function.*

Example 6.2. *Design a circuit for* $Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$ *using a* *4:1 MUX and NOT gates only.*



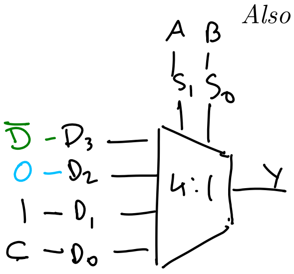
S_1	S_0	
0	0	D_0

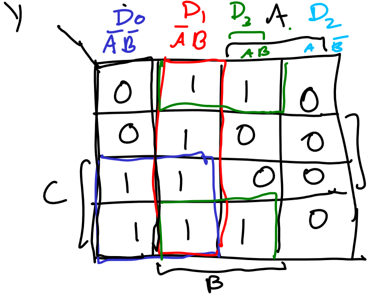
$$Y = \bar{S}_1\bar{S}_0 D_0 + \bar{S}_1 S_0 D_1 + S_1\bar{S}_0 D_2 + S_1 S_0 D_3$$



Remark 6.2. *A* $2^{N-1} : 1$ *MUX can be used to program any N-input logic function, if we use literals on the input side.*

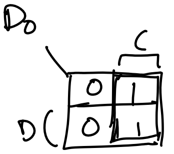
Example 6.3. *Design a circuit for* $Y = \bar{A}C + \bar{A}B + B\bar{D}$ *using a 8:1 MUX and NOT gates only. Also design using 4:1 MUX and other gates.* fewest gates.





Y= when AB=00

D_0

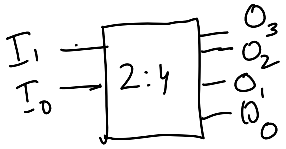


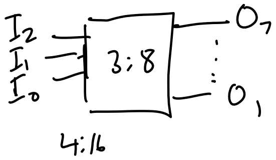
Problem 6.1. *(15 marks [1, Ex-2.42]) Implement the function* $Y = BC + \bar{A}\bar{B}\bar{C} + B\bar{C}$ *using*

1. *an 8:1 multiplexer*
2. *a 4:1 multiplexer and no other gates*
3. *a 2:1 multiplexer, one OR gate, and an inverter*

6.3 Encoders and Decoders

Example 6.4. *Draw the symbol and the truth table for 2:4 decoder. Also write the logic expressions.*

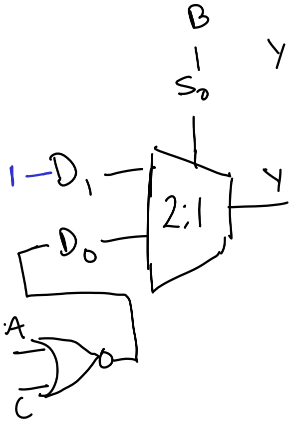




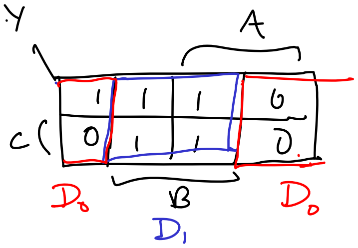
I_1	I_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$O_3 = m_3 = I_1 I_0$ $O_1 = \bar{I}_1 I_0$

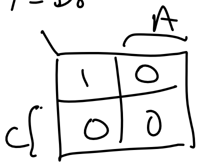
$O_2 = m_2 = I_1 \bar{I}_0$ $O_0 = \bar{I}_1 \bar{I}_0$



$Y = BC + \bar{A}\bar{B}\bar{C} + B\bar{C}$

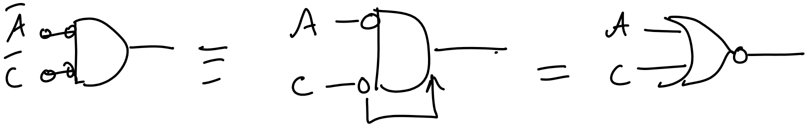


$Y = D_0$ when $B=0$



$$D_0 = \bar{A}\bar{C}$$
$$= (\overline{\overline{\bar{A}\bar{C}}})$$
$$= \overline{A+C}$$

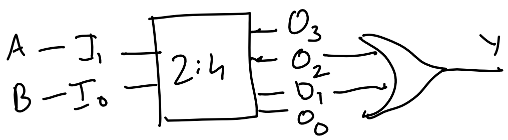
$$f = \bar{\bar{f}}$$



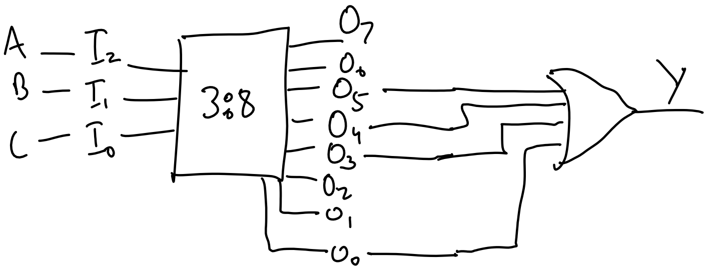
Example 6.5. *Draw the symbol and the truth table for 3:8 decoder, 4:16 decoder and* $N : 2^N$ *decoder. Also write the logic expressions.*

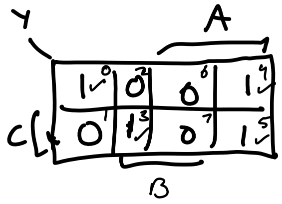
Example 6.6. *Design a circuit for a XOR gate using a 2:4 decoder and an OR gate.*

$$Y = \underset{m_2}{A\bar{B}} + \underset{m_1}{\bar{A}B}$$



Example 6.7. *Design a circuit for* $\underbrace{Y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC}$ *using a 3:8 decoder and an OR gate.*

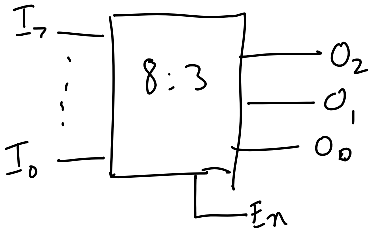




1^{0} ✓	0^{2}	0^{6}	1^{4} ✓
0^{1}	1^{3} ✓	0^{7}	1^{5} ✓

6.3.1 (Priority) Encoders

Example 6.8. *Draw symbol and truth table for a 4:2 priority encoder.*



$I_7 > \dots > I_0$	O_2	O_1	O_0	En
1 x x x --- x	1	1	1	1
0 1 x x -- x	1	1	0	1
⋮				⋮
0 0 ---- 1	0	0	0	1
0 · 0		0		En=0

Example 6.9. *Draw symbol and truth table for a 8:3 priority encoder.*