Sequential logic design

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1 Objectives

1. Analyse and design both Mealy and Moore sequential circuits with multiple inputs and multiple outputs
2. Convert between Mealy and Moore designs

2 Mealy vs Moore Finite State Machines

Definition 1 (Finite State Machines (FSM)). *[1, Sec 3.4]*

Definition 2 (Mealy FSM). *[1, Sec 3.4.3]*

Definition 3 (Moore FSM). *[1, Sec 3.4.3]*

3 State reduction via Implication tables

To minimize the number of states, we will identify "equivalent states" and eliminate any redundancy found. Two states are equivalent if they have equivalent next states and the same output for each possible input condition. To find equivalent states we will create an "implication table" which looks at pairs of states and identifies which states have to be equivalent if this pair is to be equivalent. We can use a table to hold information about each pair.

To investigate all possible pairs, we could use a square table such as this to record information about pairs of

PS	NS		Z	
	X=0	X=1	X=0	X=1
A	B	C	0	1
B	A	E	1	0
C	D	A	0	1
D	C	E	1	0
E	A	F	1	0
F	E	F	0	1

states. But note every pair represented in the upper right "triangle" of the table is also listed in the lower left "triangle" of the table. Furthermore, the diagonal of the table will only present information about a state being equivalent to itself. Only the part of the table in bold is needed to investigate all possible pairs of states:

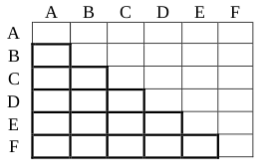

Figure 2: Implication table

4 State assignment

References

[1] Sarah L Harris and David Harris. *Digital design and computer architecture*. Morgan Kaufmann, 2022.

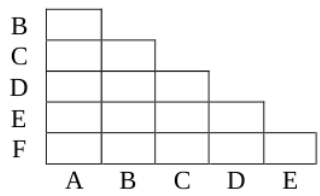

Figure 3: Selected implication table