ECE275 Practice problems for Final Spring 2025

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April 28, 2025

Student Name: Student Email:

1 Instructions

- Time allowed is ∞ minutes.
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book. One 8×11 in two-sided cheatsheet is allowed.
- Non-programmable calculators are permitted.
- The maximum number of marks is XXX, as indicated; the final examination amounts 10% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility. Colored pens/pencils are recommended for K-map grouping.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.
- If you are behind on grades, you may submit the solutions to this on brightspace before the May 5th exam for (makeup) grades. If you are already ahead, then these grades won't push you beyond hundred in homework+midterm grades.

Problem 1. *Use the following 5-variable K-map for F (B, C, D, E), and find a minimal SOP expression for F (15 marks)*

DE \ BC	00	01	11	10
00	1			1
01	1	1		1
11		1		
10		1	1	

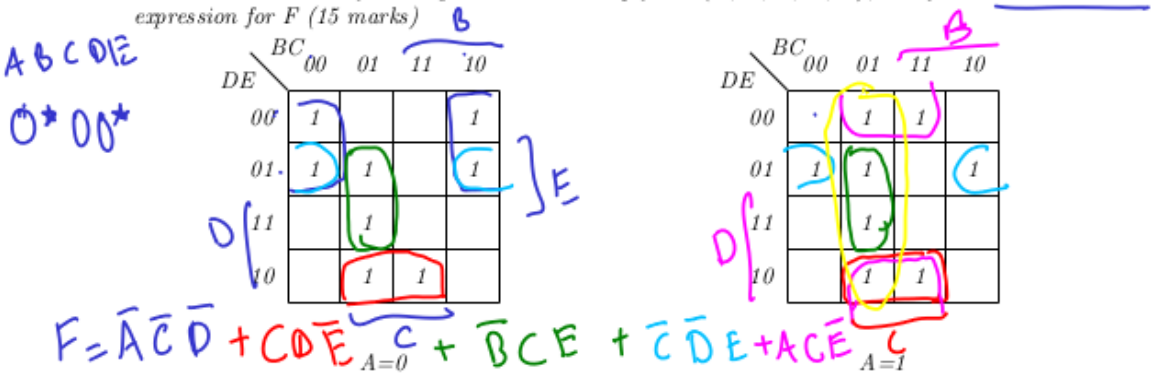
A=0

DE \ BC	00	01	11	10
00		1	1	
01	1	1		1
11		1		
10		1	1	

A=1

Problem 2. *A sequential circuit has two inputs and two outputs. The inputs (X_1 and X_0) represent a 2-bit binary number, N. If the present value of N is greater than the previous value, then Z_1 is 1. If the present value of N is less than the previous value, then Z_2 is 1.* ***Otherwise,***

Problem 1. *Use the following 5-variable K-map for F (A, B, C, D, E), and find a minimal SOP expression for F (15 marks)*



Problem 2

Example

X_1	0	0	1	1	1	0	1
X_0	0	1	0	1	0	1	1
Z_1	0	1	1	1	0	0	1
Z_2	0	0	0	0	1	1	0

PS	NS				Outputs (Z_1 Z_2)			
	X_1X_0 = 00	01	10	11	X_1X_0 = 00	01	10	11
S_0	S_1	S_2	S_3	S_4	00	00	00	00
S_1	S_1	S_2	S_3	S_4	00	10	10	10
S_2	S_1	S_2	S_3	S_4	01	00	10	10
S_3	S_1	S_2	S_3	S_4	01	01	00	10
S_4	S_1	S_2	S_3	S_4	01	01	01	00

Z_1 and Z_2 are 0. When the first pair of inputs is received, there is no previous value of N, so we cannot determine whether the present N is greater than or less than the previous value; therefore, the "otherwise" category applies.

Find a Mealy state table for the circuit (minimum number of states, including starting state, is five) (30 marks).

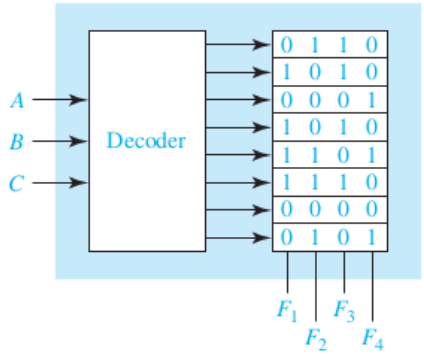
(Hint: The header for Mealy State table will look something like this:)

Present State	Next State				Outputs (Z_1Z_2)			
	Inputs $X_1X_0 = 00$	01	10	11	$X_1X_0 = 00$	01	10	11
S_0	S_1	S_2	S_3	S_4	00	00	00	00

Problem 3. *A 4:2 priority encoder takes 4 inputs y_0, y_1, y_2, y_3 and has three outputs, w_1, w_0 and IST. Find boolean expressions for w_1 and w_0 using K-maps for the priority encoder. The priority encoder truth table is given for reference ("*" indicates all possible input combinations and "d" indicates don't care output). (10 marks)*

Inputs				*Outputs*		
y_0	y_1	y_2	y_3	w_1	w_0	*IST*
0	0	0	0	d	d	0
1	*	*	*	0	0	1
0	1	*	*	0	1	1
0	0	1	*	1	0	1
0	0	0	1	1	1	1

Problem 4. *The following diagram shows the pattern of 0's and 1's stored in a ROM with eight words and four bits per word. What will be the values of $F_1, F_2, F_3, and F_4$ if $A = B = 0$ and $C = 1$? Also give the minterm expansions for F_1 and F_2 (20 marks).*



F_1 F_2 F_3 F_4 = 1010

F1 = ∑ m(1, 3, 4, 5)
F2 = ∑ m(0, 4, 5, 7)

Problem 5. *The following prime implicant table is for a four variable function $f(A, B, C, D)$. Give the algebraic expression of each of the essential prime implicants. Find the minimal sum of products expression for f by PI table reduction. (10 marks)*

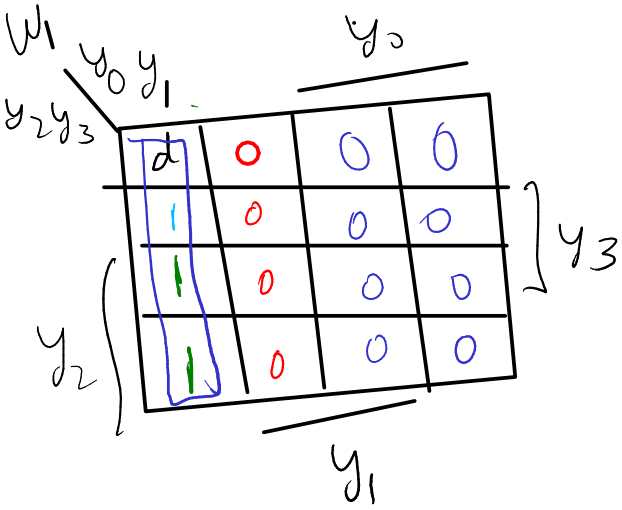
minterms \PIs:	$\bar{B}D$	$\bar{B}C$	CD	AD
2		×		
3	×	×	×	
7			×	
9	×			×
11	×	×	×	×
13				×

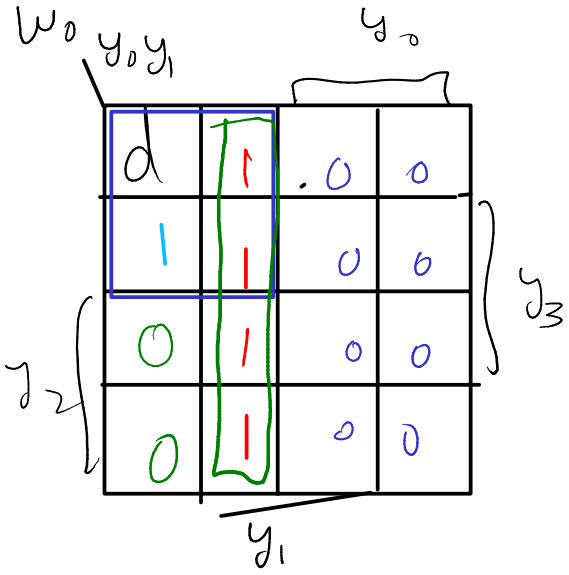
Problem 6. *Packages arrive at the stockroom and are delivered on carts to offices and laboratories by student employees.The carts and packages are various sizes and shapes.The students are paid*

3

Problem 5. *A 4:2 priority encoder takes 4 inputs y_0, y_1, y_2, y_3 and has three outputs, w_1, w_0 and IST. Find boolean expressions for w_1 and w_0 using K-maps for the priority encoder. The priority encoder truth table is given for reference ("*" indicates all possible input combinations and "d" indicates don't care output). (10 marks)*

Inputs				Outputs		
y_0	y_1	y_2	y_3	w_1	w_0	IST
0	0	0	0	d	d	0
1	*	*	*	0	0	1
0	1	*	*	0	1	1
0	0	1	*	1	0	1
0	0	0	1	1	1	1





Problem 5. *The following prime implicant table is for a four variable function $f(A, B, C, D)$. Give the algebraic expression of each of the essential prime implicants. Find the minimal sum of products expression for f by PI table reduction. (10 marks)*

minterms \PIs:	$\bar{B}D$	$\bar{B}C$	CD	AD
2		×		
3	×	×	×	
7			×	
9	×			×
11	×	×	×	×
13				×

EPIs = (~B)C, CD

Column dominance: AD > (~B)D.

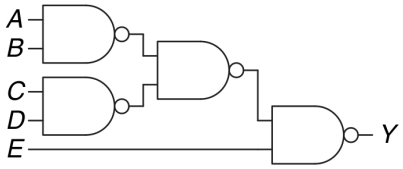
Minimal sum of product expression f = AD +(~B)C + CD

according to the carts used. There are five carts and the pay for their use is
Cart C1: $2
Cart C2: $1
Cart C3: $4
Cart C4: $2
Cart C5: $2
On a particular day, seven packages arrive, and they can be delivered using the five carts as follows:
C1 can be used for packages P1, P3, and P4.
C2 can be used for packages P2, P5, and P6.
C3 can be used for packages P1, P2, P5, P6, and P7.
C4 can be used for packages P3, P6, and P7.
C5 can be used for packages P2 and P4.
The stockroom manager wants the packages delivered at minimum cost. Using minimization techniques described in this class, present a systematic procedure for finding the minimum cost solution. (20 marks)

Problem 7. *(a) For $V_{IH} = 4$ V, $V_{OH} = 4.5$ V, $V_{IL} = 1$ V, $V_{OL} = 0.3$ V, and $V_{DD} = 5$ V, calculate the noise margins NM_H and NM_L (5 marks).*
(b) Draw an eight-input NAND gate built using NMOS technology and pull-up resistor (5 marks).
(c) In the above circuit, if the voltage drop across each transistor is 0.1 V, what is V_{OL} ? What is the corresponding NM_L using the other parameters from part (a) (10 marks).

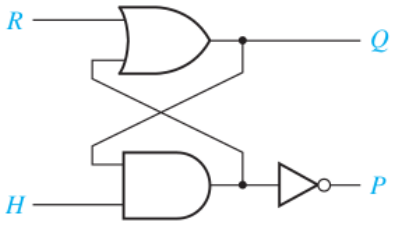
Problem 8. *What is the difference between positive logic and negative logic? Design a CMOS complex gate for $f = x_1\bar{x}_2 + \bar{x}_1x_2$ under negative logic (10 marks).*

Problem 9. *Find the propagation delay and contamination delay of the following circuit (5 marks):*



Problem 10. *Describe how tri-state and open-collector outputs are different from totem- pole outputs using NMOS NOR gate as an example (10 marks).*

Problem 11. *A latch can be constructed from an OR gate, an AND gate, and an inverter connected as follows:*



1. *What restriction must be placed on R and H so that P will always equal Q (under steady-state conditions) (10 marks)?*
2. *Construct a characteristic (next-state) table and derive the corresponding characteristic equation for the latch (5 marks).*

Problem 6. *Packages arrive at the stockroom and are delivered on carts to offices and laboratories by student employees. The carts and packages are various sizes and shapes. The students are paid according to the carts used. There are five carts and the pay for their use is*

Cart C1: $2
Cart C2: $1
Cart C3: $4
Cart C4: $2
Cart C5: $2

On a particular day, seven packages arrive, and they can be delivered using the five carts as follows:
C1 can be used for packages P1, P3, and P4.
C2 can be used for packages P2, P5, and P6.
C3 can be used for packages P1, P2, P5, P6, and P7.
C4 can be used for packages P3, P6, and P7.
C5 can be used for packages P2 and P4.
The stockroom manager wants the packages delivered at minimum cost. Using minimization techniques described in this class, present a systematic procedure for finding the minimum cost solution. (20 marks)

Carts → / Packages	C_1	C_2	C_3	C_4	C_5
P_1	×		×		
P_2		×	×		×
P_3	×			×	
P_4	×				×
P_5		×	×		
P_6		×	×	×	
P_7			×	×	

If P_5 is delivered, P_2 will always be delivered

Package P1 is delivered if C1 OR C3 is used.
Package P2 is delivered if C2 OR C3 OR C5 is used

All packages are delivered if the following boolean expression is true

$P_1 \quad P_2 \quad P_3 \quad P_4$

$= (C_1 + C_3)(C_2 + C_3 + C_5)(C_1 + C_4)(C_1 + C_5)$

$P_5 \quad P_7$

$(C_2 + C_3)(C_3 + C_4)$

$= C_1 C_2 C_4$

Cost = 5 ✓

C_1 occurs in most brackets and $C_1 \cdot C_1 = C_1$

$+ C_1 C_3$

cost = 6

$+ C_1 C_4$

cost = 8

$+ C_1 C_3 C_5$

cost = 8

$+ C_3 C_4 C_5$

cost = 8

$+ C_3 C_2 C_4 C_5$

$+ \ldots\ldots$

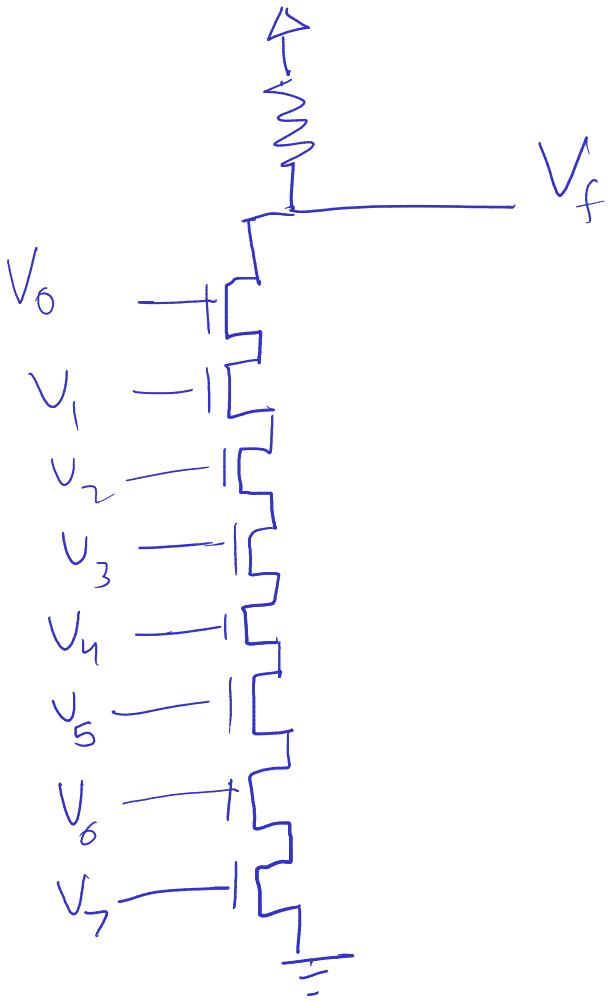
Pick carts C_1 and C_2 and C_4 for cost 5. That covers all packages

Problem ~~5.~~ 7. *(a) For $V_{IH} = 4$ V, $V_{OH} = 4.5$ V, $V_{IL} = 1$ V, $V_{OL} = 0.3$ V, and $V_{DD} = 5$ V, calculate the noise margins NM_H and NM_L (5 marks).*
(b) Draw an eight-input NAND gate built using NMOS technology and pull-up resistor (5 marks).
(c) In the above circuit, if the voltage drop across each transistor is 0.1 V, what is V_{OL} ? What is the corresponding NM_L using the other parameters from part (a) (10 marks).

(a) $NM_H = V_{OH} - V_{IH} = 4.5 - 4 = 0.5\ V$

$NM_L = V_{IL} - V_{OL} = 1 - 0.3 = 0.7\ V$

(b)



$V_f = L$ if and only if all $V_0, V_1 \ldots V_7$ are H

(C) V_oL = 0.8

Problem 8

Under positive logic, high voltage (H) is treated as boolean 1 while low voltage is boolean 0

Under negative logic H = 0, L = 1

$f = x_1\bar{x}_2 + \bar{x}_1 x_2$

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

Negative logic →

V_{x_1}	V_{x_2}	V_f
H	H	H
H	L	L
H	L	L
L	L	H

↓ Positive logic

x_1	x_2	g
1	1	1
1	0	0
0	1	0
0	0	1

←

$g = \sum m(0,3)$

$= \bar{x}_1\bar{x}_2 + x_1 x_2$

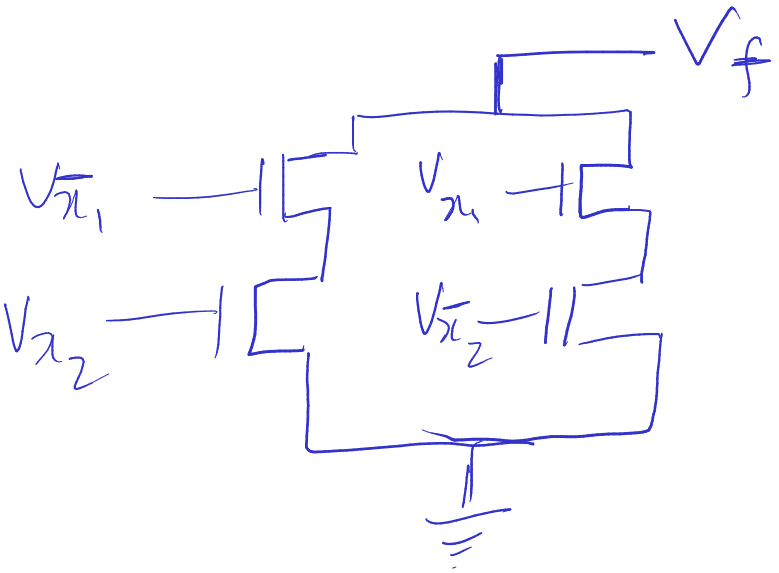
Designing $f = \bar{x}_1 x_2 + x_1 \bar{x}_2$ under negative logic

is same as designing $g = \bar{x}_1 \bar{x}_2 + x_1 x_2$ under +ve logic

nMOS block design

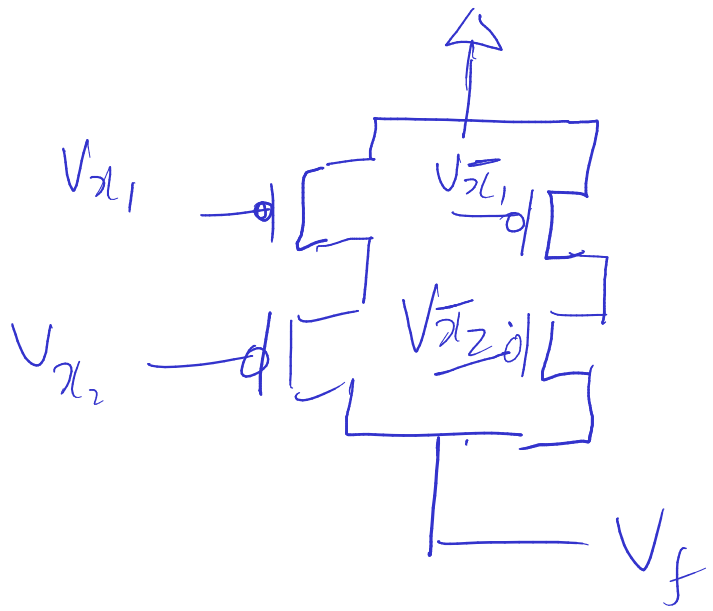
Design for $\bar{g} = \overline{\bar{x}_1 \bar{x}_2 + x_1 x_2}$

$= \bar{x}_1 x_2 + x_1 \bar{x}_2$

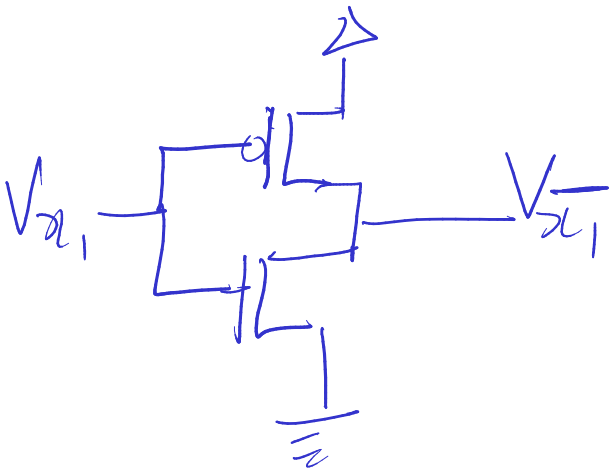


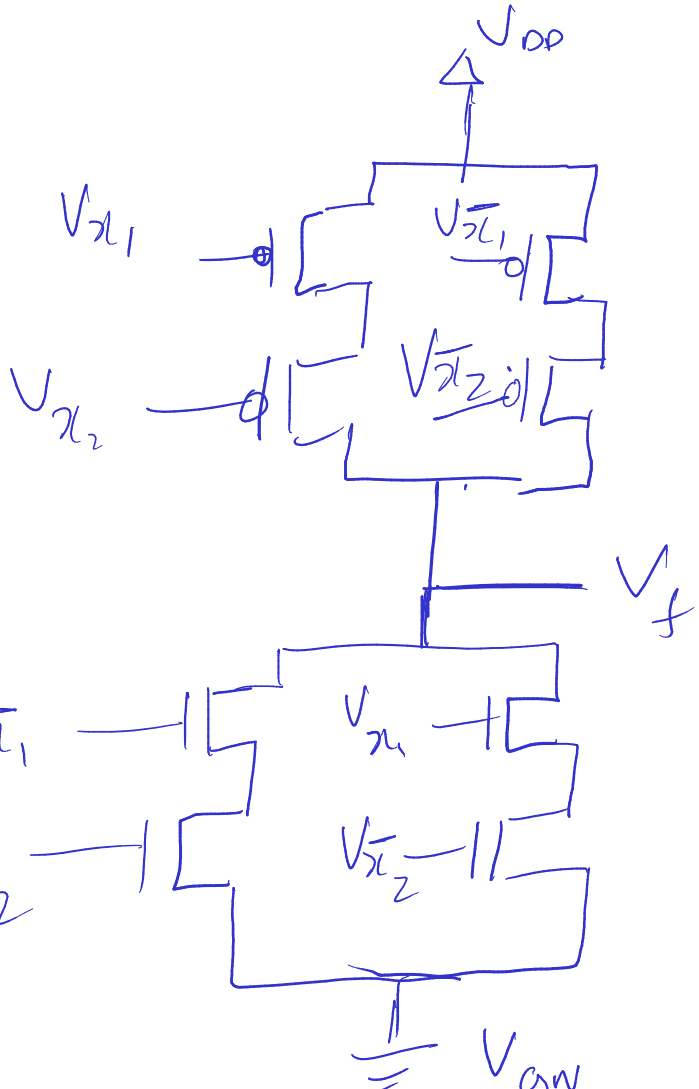
pMOS block design

Design for $g = \bar{x}_1 \bar{x}_2 + x_1 x_2$



$V_{\bar{x}_1}$ and $V_{\bar{x}_2}$ can be obtained from CMOS NOT gates using 2 transistor each



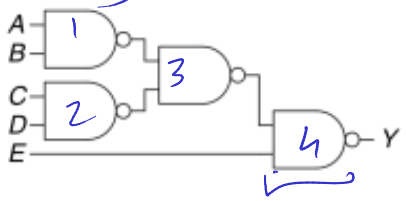


CMOS

Total transistors

$2+2+4+4 = 12$

Problem 5. *Find the propagation delay and contamination delay of the following circuit (5 marks):*



Let the propagation delay of each gate be t_{p_1}, t_{p_2} t_{p_3} t_{p_4} respectively

t_{cd_4}

then

total propagation delay

$= t_{p_4} + t_{p_3} + \max(t_{p_1}, t_{p_2})$

Total contamination delay

$= t_{cd_4}$

Problem 10

Tristate has 3 possible outputs:

High, Low, high impedance

1, 0, Z

Open collector has 2 possible outputs:

High impedance

Z

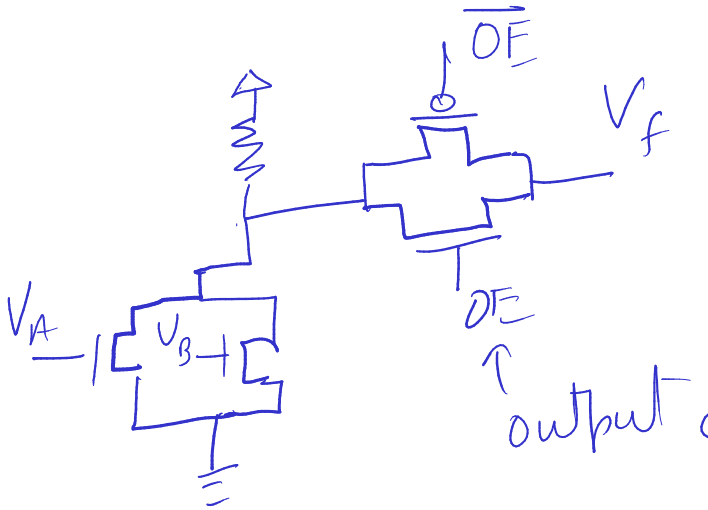
and Low = 0

Totem pole has 2 possible outputs:

High and Low

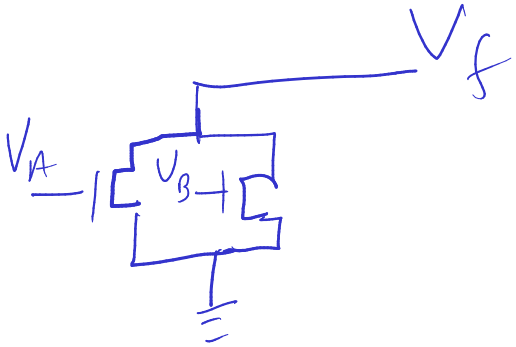
1 0

Tristate NMOS NOR gate



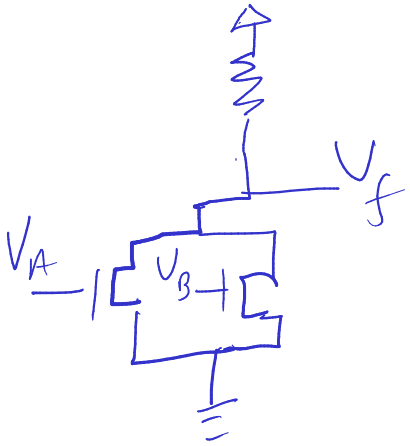
V_A	V_B	$\overline{OE}$	V_f
*	*	L	Z
L	L	H	L
L	H	H	H
H	L	H	H
H	H	H	H

Open collector



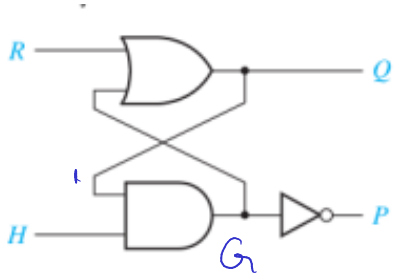
V_A	V_B	V_f
L	L	L
L	H	Z
H	L	Z
H	H	Z

Totem pole



V_A	V_B	V_f
L	L	L
L	H	H
H	L	H
H	H	H

Problem 11

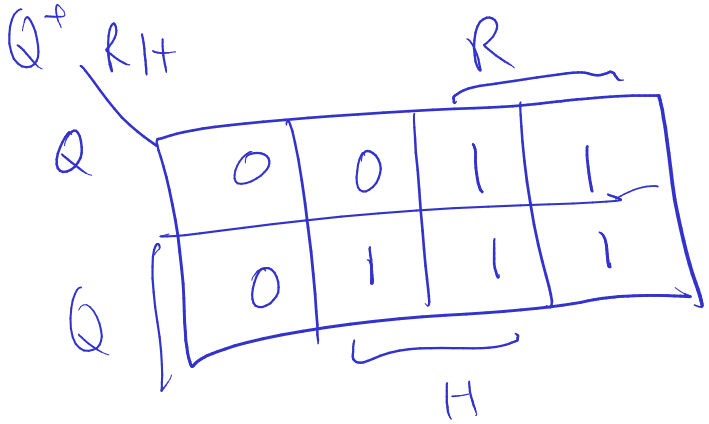


R	H	Q	G	Q^+	G^+
0	0	*	*	0	0
0	1	0/1	0/1	Q	Q
1	0	*	*	1	0
1	1	▷	*	1	1

(1) P=Q y R=1, H=0

(2)

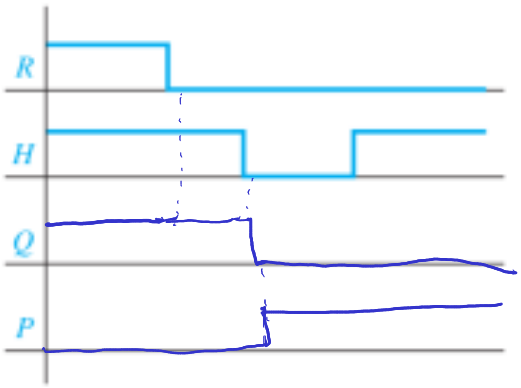
R	H	Q	G	Q^+	G^+
0	0	*	*	0	0
0	1	0/1	0/1	Q	Q
1	0	*	*	1	0
1	1	▷	*	1	1



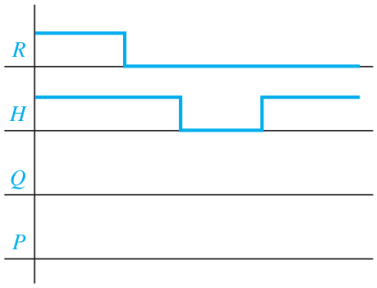
$Q^+ = R + HQ$

characteristic equation

(3)



3. *Complete the following timing diagram for the latch (10 marks)*



Problem 12. *Figure 1 shows the notation for a BCD to 7-segment display and Table 1 shows the corresponding truth table. The inputs corresponding to the missing rows in the truth table should be considered as don't care.*

1. *implement segment "a" using an 8:1 mux and no other logic gate, (10 marks)*
2. *implement segment "a" using a 4:1 mux and one other gate, (10 marks)*
3. *implement segment "f" with 4:1 mux and no other logic gate. Assume inputs are available in both uncomplemented and complemented form. (Hint: There are ($^4C_2 = 6$) possible pairs of control inputs: (w_3, w_2), (w_2, w_1), (w_1, w_0), (w_0, w_3), (w_0, w_2), (w_1, w_3). There are 6 don't care conditions. With two control inputs of the multiplexer and one input, you can represent an expression with up to 4-SOP-terms of size three-literals or less. You might the arrive at the answer sooner, if you try to write the minimal SOP expression first and find the two inputs that occur most often in all the terms. Those two inputs are most likely to be the chosen pair of control inputs.) (10 marks)*

Row	w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 1: Truth table for BCD to seven-segment display as shown in Figure 1. The missing combinations of inputs should be considered as dont care.

Problem 13. *Design a 3-bit modulo 8 counter that counts from 000, to 111 and then loops back to 0000. (A modulo N counter counts from 0 to $N-1$) (20 marks).*

1. *Draw its state transition table*
2. *Design the circuit using a D flip-flop.*

Problem 14. *Draw Mealy state transition diagram which investigates an input sequence X and will produce an output of $Z = 1$ for any input sequence ending in 0011 or 110.*
Example:

Problem 12. *Figure 1 shows the notation for a BCD to 7-segment display and Table 1 shows the corresponding truth table. The inputs corresponding to the missing rows in the truth table should be considered as don't care.*

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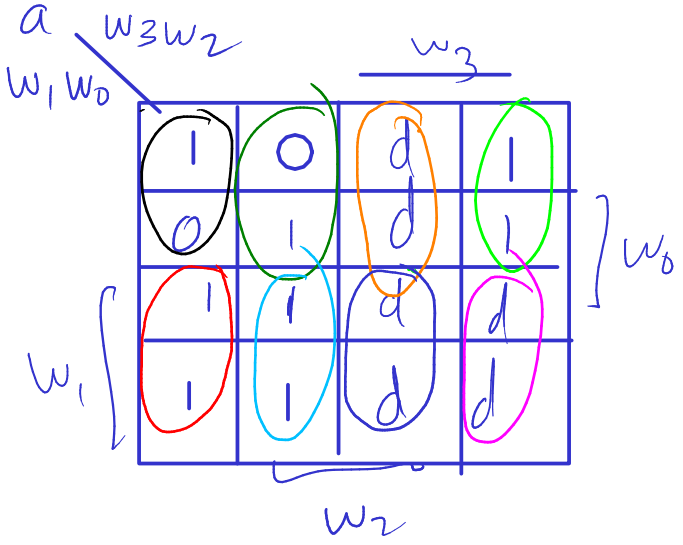
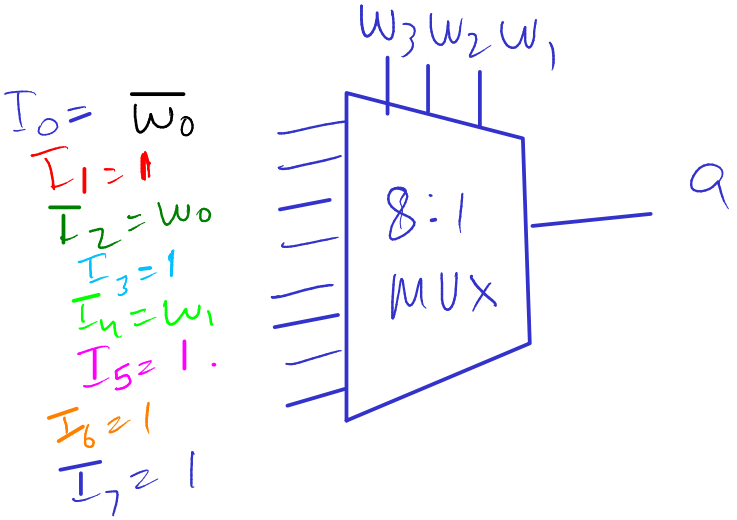
2. *implement segment "a" using a 4:1 mux and one other gate, (10 marks)*
3. *implement segment "f" with 4:1 mux and no other logic gate. Assume inputs are available in both uncomplemented and complemented form. (Hint: There are ($^4C_2 = 6$) possible pairs of control inputs: (w_3, w_2), (w_2, w_1), (w_1, w_0), (w_0, w_3), (w_0, w_2), (w_1, w_3). There are 6 don't care conditions. With two control inputs of the multiplexer and one input, you can represent an expression with up to 4-SOP-terms of size three-literals or less. You might the arrive at the*

Row	w_3	w_2	w_1	w_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

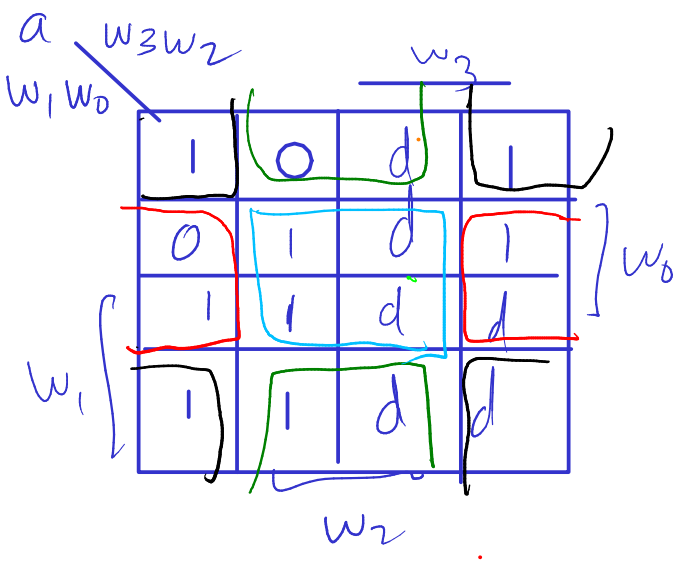
(1)



Picking $w_3 w_2 w_1$ as the selection lines

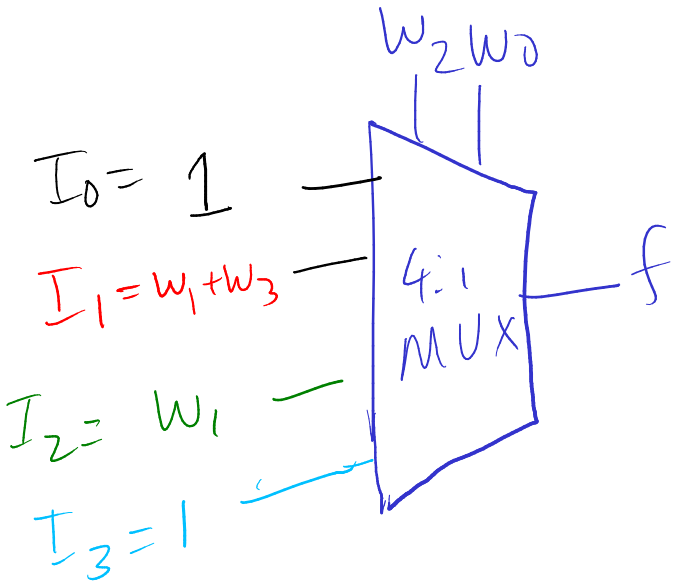


(b)



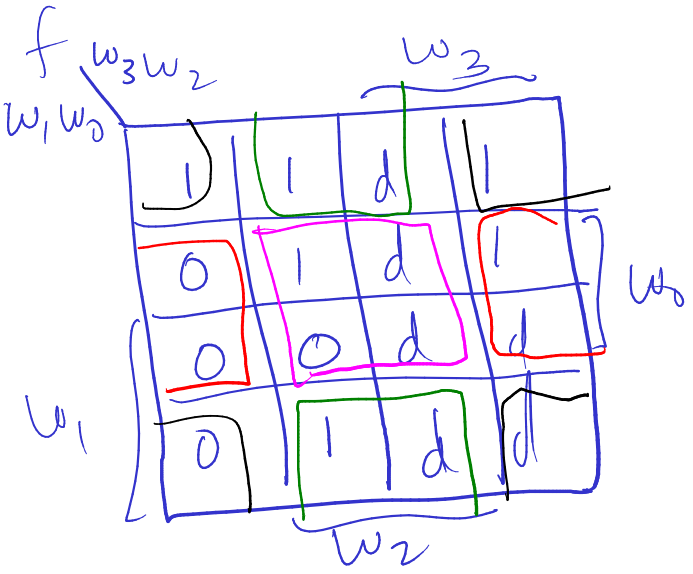
$a = w_3 + w_1 + \overline{w_0}\,\overline{w_2} + w_0 w_2$

Picking w_0 and w_2 as selection bits



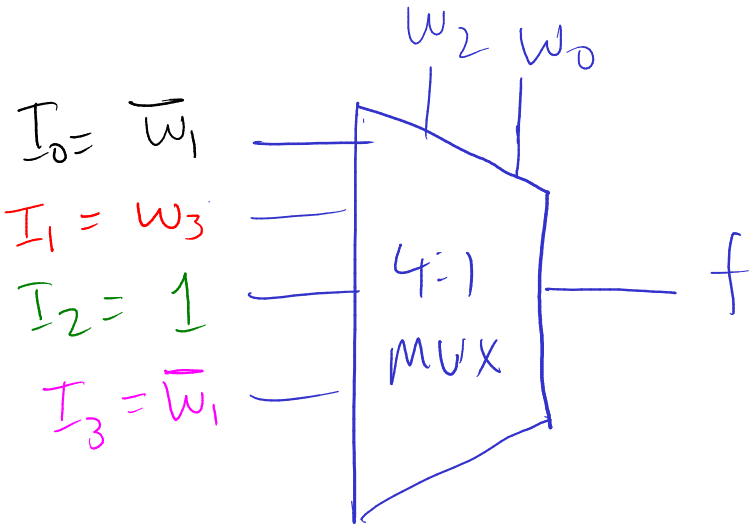
Uses only one other logic gate for $I_1 = w_1 + w_3$

(c)



$$f = w_3 + \bar{w}_0\bar{w}_1 + w_2\bar{w}_0 + w_2\bar{w}_1$$

Pick w_2 and w_0 as the selection bits



This uses no other logic gates.

Problem 13

Not covered in syllabus

A gray counter is one that changes only one bit at a time

	Q_2 Q_1 Q_0
0	0 0 0
1	0 0 1
2	0 1 1
3	0 1 0
4	1 1 0
5	1 1 1
6	1 0 1
7	1 0 0

↓ Gray code counting

Q_2 Q_1 Q_0	Q_2^+ Q_1^+ Q_0^+
0 0 0	0 0 1
0 0 1	0 1 1
0 1 0	1 1 0
0 1 1	0 1 0
1 0 0	0 0 0
1 0 1	1 0 0
1 1 0	1 1 1
1 1 1	1 0 1

$D_2 = Q_2^+$

Q_2Q_1 / Q_0	00	01	11	10
0	0	1	1	0
1	0	0	1	1

$D_2 = Q_1 \bar{Q}_0 + Q_2 Q_0$

$D_1 = Q_1^+$

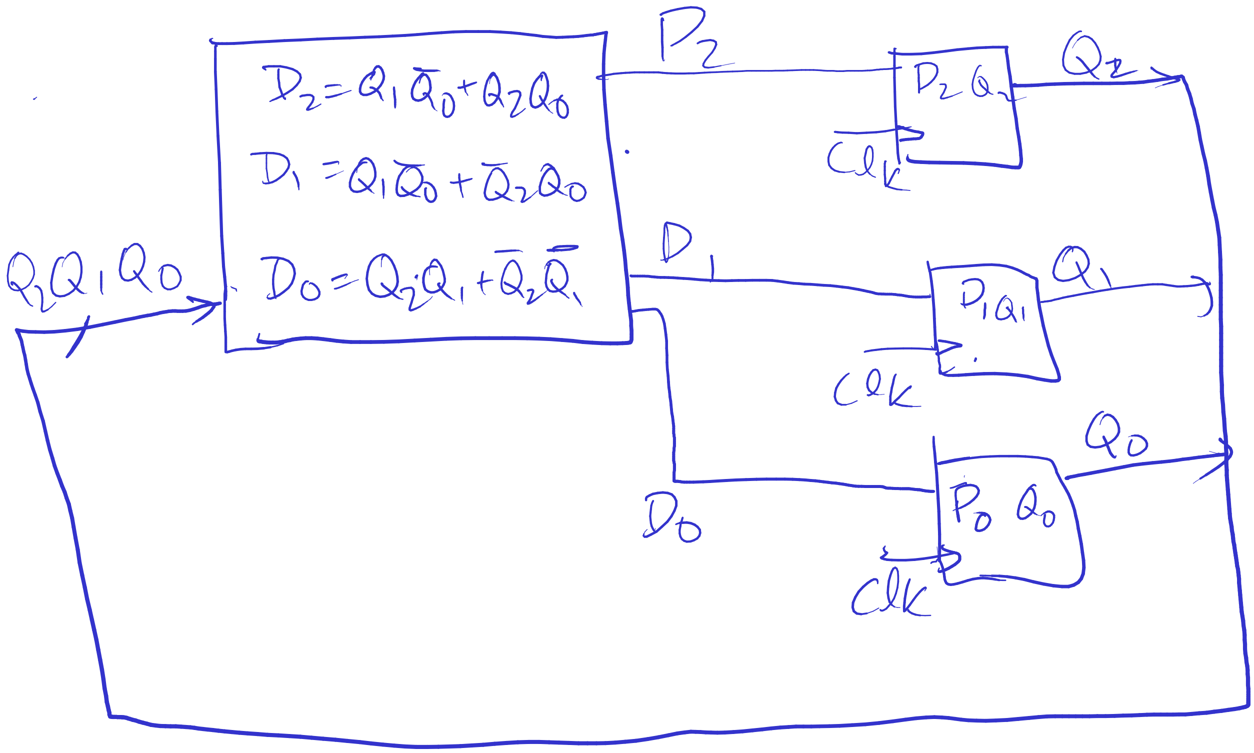
Q_2Q_1				
$\overline{Q_0}$	0	1	1	0
Q_0	1	1	0	0

$$D_1 = Q_1\overline{Q_0} + \overline{Q_2}Q_0$$

D_0

Q_2Q_1				
$\overline{Q_0}$	1	0	1	0
Q_0	1	0	1	0

$$D_0 = Q_2Q_1 + \overline{Q_2}\,\overline{Q_1}$$



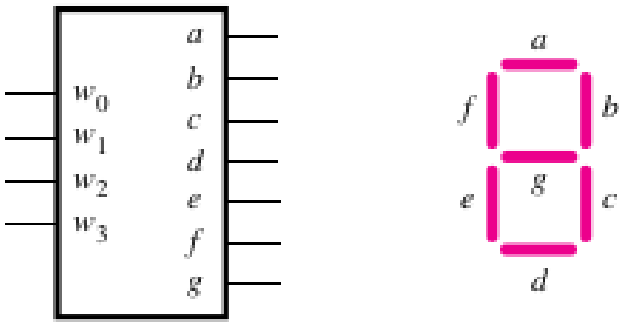


Figure 1: Seven segment display and BCD-to-7-segment display converter. When $a = 1$ the corresponding segment of the display lights up. To display the number 8, you will turn on all the seven segments, while to display 1, you will turn on $b = 1, c = 1$ and turn off $= 0$ the rest. The full truth-table for the seven-segment display is shown in Table 1.

$X =$	*1*	*1*	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*1*	*0*	*1*
$Z =$	*0*	*0*	*0*	*1*	*0*	*1*	*1*	*0*	*1*	*0*	*0*	*1*	*0*	*1*	*0*

Notice that the circuit does not reset to the start state when an output of $Z = 1$ occurs. A minimum solution requires six states. Assign 000 to the start state. (20 marks).

Problem 15. *Find the expression for J_0 and K_0 assuming that J_0 and K_0 are inputs to the J-K flip flop that capture the state of the second most significant bit Q_0 of the following state encoded table. The state encoding table given with state encoding denoted as $Q_2Q_1Q_0$. (20 marks).*

Present State	*Next State*		*Output*	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
$Q_2Q_1Q_0$	$Q_2^+Q_1^+Q_0^+$	$Q_2^+Q_1^+Q_0^+$	Z	Z
000	*100*	*101*	*1*	*0*
001	*100*	*101*	*0*	*1*
010	*000*	*000*	*1*	*0*
011	*000*	*000*	*0*	*1*
100	*111*	*110*	*1*	*0*
101	*110*	*110*	*0*	*1*
110	*011*	*010*	*1*	*0*
111	*011*	*011*	*0*	*1*

Problem 14. *Draw Mealy state transition diagram which investigates an input sequence X and will produce an output of $Z = 1$ for any input sequence ending in 0011 or 110.*
Example:

$X =$	1	1	0	0	1	0	0	1	0	1	0	0	1	0	1
$Z =$	0	0	0	1	0	1	1	0	1	0	0	1	0	1	0

Notice that the circuit does not reset to the start state when an output of $Z = 1$ occurs. A minimum solution requires six states. Assign 000 to the start state. (20 marks).

Here's a table, make a diagram instead

State	Next state		Output (Z)	
	X = 0	X = 1	X = 0	X= 1
S0	S1	S4	0	0
S1	S2	S4	0	0
S2	S2	S3	0	1
S4	S1	S5	0	0
S5	S1	S5	1	0

State meaning
S0 = *** # have seen nothing
S1 = **0 # have seen a zero
S2 = *00 # have seen two zeros
S3 = 001 # have seen two zeros and a 1
S4 = **1 # have seen a zero
S5 = *11 # have seen two ones

Problem 15. *Find the expression for J_0 and K_0 assuming that J_0 and K_0 are inputs to the J-K flip flop that capture the state of the second most significant bit Q_0 of the following state encoded table. The state encoding table given with state encoding denoted as $Q_2Q_1Q_0$. (20 marks).*

Present State	*Next State*		*Output*	
	$X=0$	$X=1$	$X=0$	$X=1$
$Q_2Q_1Q_0$	$Q_2^+Q_1^+Q_0^+$	$Q_2^+Q_1^+Q_0^+$	Z	Z
000	*100*	*101*	*1*	*0*
001	*100*	*101*	*0*	*1*
010	*000*	*000*	*1*	*0*
011	*000*	*000*	*0*	*1*
100	*111*	*110*	*1*	*0*
101	*110*	*110*	*0*	*1*
110	*011*	*010*	*1*	*0*
111	*011*	*011*	*0*	*1*