AC6381A Datasheet

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AC6381A Features

High performance 32-bit RISC CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 160MHz programmable processor
- 64 Vectored interrupts
- 8 Levels interrupt priority

Flexible I/O

- 24 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level schmitt triggered input
- External wake up/interrupt on all GPIOs

Peripheral Feature

- One Full Speed USB OTG controller
- Six Multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, support DMA mode
- Two SPI interface supports host and device mode
- One hardware IIC interface supports host and device mode
- Two Built-in low power Cap Sense Keys
- Built-in Cap Sense Key controller
- 10-bit ADC for analog sampling
- Power-on reset

Bluetooth Feature

- Compliant with Bluetooth V5.1+BR+EDR+BLE specification
- Meet class1 class2 and class3 transmitting power requirement
- Support GFSK and π/4 DQPSK all packet types
- Provides maximum +8dbm@BDR, +6dbm@EDR transmitting power
- receiver with -94dBm@EDR sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap gatt\rfcomm\sdp\l2cap profile
- a2dp 1.3\avctp 1.4\avdtp 1.3\avrcp 1.5\ hfp 1.5 \spp 1.0\rfcomm 1.2\pnp 1.3\ hid 1.0\sdp core4.2\l2cap core 4.2

Power Supply

- Low voltage LDO for internal digital and analog circuit supply
- 2uA current consumption in the soft-off mode
- Built-in LDO for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 5.5V
  VDDIO is 2.2V to 3.4V

Packages

- QFN32(4x4mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

1. Pin Definition

1.1 Pin Assignment

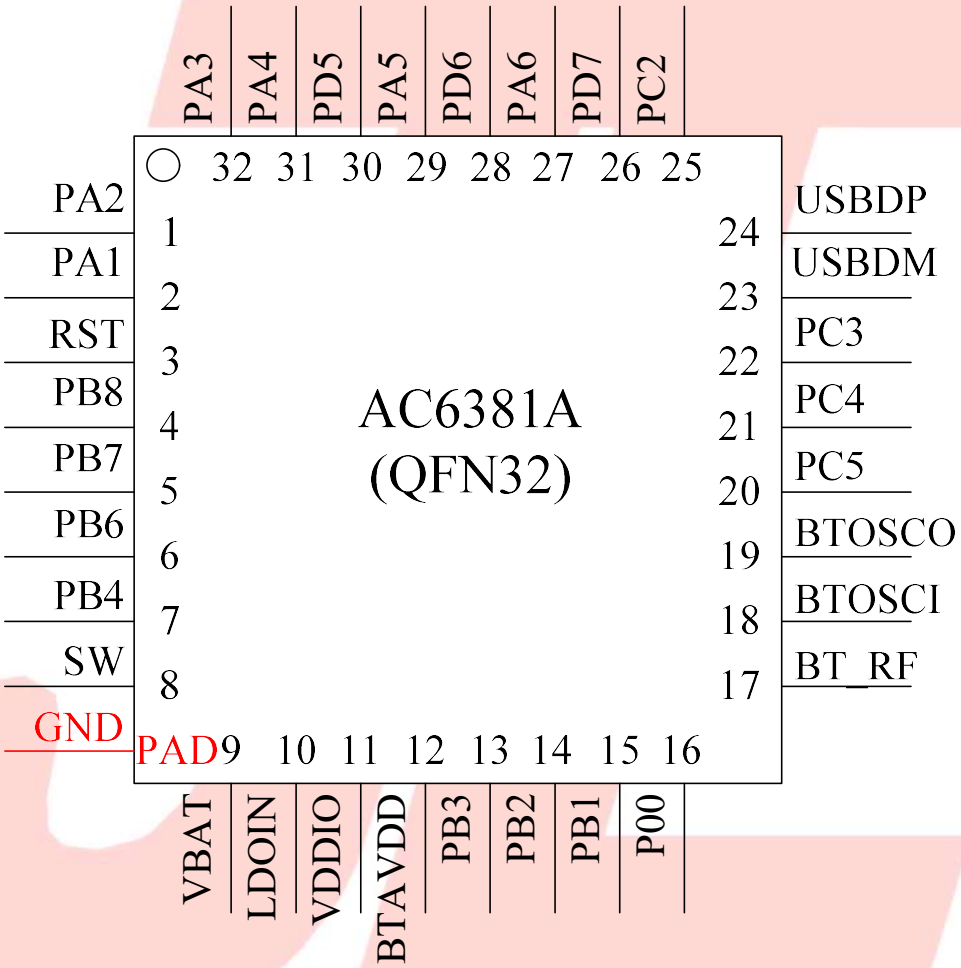


Figure 1-1 AC6381A_QFN32 Package Diagram

1.2 Pin Description

Table 1-1 AC6381A_QFN32 Pin Description

PIN NO.	Name	I/O Type	Function	Other Function
1	PA2	I/O	GPIO	CAP3: Timer3 Capture; UART1_RXC: Uart1 Data In(C);
2	PA1	I/O	GPIO	SPI1_DIC: SPI1 Data In(C); PWM0: Timer0 PWM Output; UART1_TXC: Uart1 Data Out(C);
3	RST	I	GPIO	RESET:Hight Active;
4	PB8	I/O	GPIO (High Voltage)	UART0_RXB: Uart0 Data In(B); CAP4: Timer4 Capture;
5	PB7	I/O	GPIO	SPI1_DOA: SPI1 Data Out(A); SD0CLKB：SD0 Clock(B); Q-decoder1; TOUCH1:Touch Input Channel 6 ADC8: ADC Channel 8; UART0_TXB: Uart0 Data Out(B);
6	PB6	I/O	GPIO	SPI1_CLKA: SPI1 Clock(A) ; Q-decoder0; SD0CMDB：SD0 Command(B); ADC9: ADC Channel 9; TOUCH7:Touch Input Channel 7; UART1_RXA: Uart1 Data In(A); PWM2: Timer2 PWM Output;
7	PB4	I/O	GPIO	CLKOUT0; LVD:Low Voltage Detect; SD0DAT0B：SD0 Data0(B); SPI1_DIA: SPI1 Data In(A); ADC12: ADC Channel 12; TOUCH6:Touch Input Channel 6; UAR1_TXA: Uart1 Data Out(A); TMR2: Timer2 Clock In;
8	SW	P	DC-DC Switch Pin	-
9	VBAT	P	LDO Power	-

10	LDOIN	P	Charge Power 5V	PWM3: Timer3 PWM Output; UART0_TXC: Uart0 Data Out(C); UART0_RXC: Uart0 Data In(C);
11	VDDIO	P	IO Power 3.3V	-
12	BTAVDD	P	Core Power 1.3V	-
13	PB3	I/O	GPIO	SPI2_DIC: SPI2 Data In(C); UART1_TXB: Uart1 Data Out(B); UART1_RXB: Uart1 Data In(B); TMR4: Timer4 Clock In;
14	PB2	I/O	GPIO	SPI2_DOC: SPI2 Data Out(C); ADC7: ADC Channel 7; UART2_RXC: Uart2 Data In(C); CAP5: Timer5 Capture; LP_TH1：Low Power Touch Channel 1;
15	PB1	I/O	GPIO (pull up)	Long Press Reset; UART2_TXC: Uart2 Data Out(C); ADC6: ADC Channel 6; LP_TH0：Low Power Touch Channel 0;
16	P00	I/O	GPIO (High Voltage)	
17	BT_RF	-	RF Antenna	-
18	BTOSCI	I	BTOSCI	-
19	BTOSCO	O	BTOSCO	-
20	PC5	I/O	GPIO	SD0CLKA：SD0 Clock(A); SPI1_DOB: SPI1 Data Out(B); IIC_SDA_B: IIC SDA(B); ADC5: ADC Channel 5; UART2_RXD: Uart2 Data In(D);
21	PC4	I/O	GPIO	SD0CMDA：SD0 Command(A); SPI1_CLKB: SPI1 Clock(B) ; IIC_SCL_B: IIC SCL(B); ADC4: ADC Channel 4; UART2_TXD: Uart2 Data Out(D); PWM4: Timer4 PWM Output;
22	PC3	I/O	GPIO	SD0DAT0A：SD0 Data0(A); SPI1_DIB: SPI1 Data In(B); IIC_SDA_C: IIC SDA(C); ADC3: ADC Channel 3; TOUCH5:Touch Input Channel 5; UART0_RXD: Uart0 Data In(D); TMR3: Timer3 Clock In;

23	USBDM	I/O	GPIO (pull down)	SPI2_DOB: SPI2 Data Out(B); IIC_SDA_A: IIC SDA(A); ADC11: ADC Channel 11; UART1_RXD: Uart1 Data In(D);
24	USBDP	I/O	GPIO (pull down)	SPI2_CLKB: SPI2 Clock(B); IIC_SCL_A: IIC SCL(A); ADC10: ADC Channel 10; UART1_TXD: Uart1 Data Out(D);
25	PC2	I/O	GPIO	SPI2_DIB: SPI2 Data In(B); IIC_SCL_C: IIC SCL(C); TOUCH4:Touch Input Channel 4; UART0_TXD: Uart0 Data Out(D); TMR1: Timer1 Clock In;
26	PD7	I/O	GPIO	UART2_RXB: Uart2 Data In(B); TMR5: Timer5 Clock In;
27	PA6	I/O	GPIO	UART1_RTS; SPI2_DOA: SPI2 Data Out(A); IIC_SDA_D: IIC SDA(D); ADC2: ADC Channel 2; TOUCH3:Touch Input Channel 3; UART0_RXA: Uart0 Data In(A); CAP0: Timer0 Capture;
28	PD6	I/O	GPIO	UART2_TXB: Uart2 Data Out(B); TMR0: Timer0 Clock In;
29	PA5	I/O	GPIO	UART1_CTS; SPI2_CLKA: SPI2 Clock(A); IIC_SCL_D: IIC SCL(D); ADC1: ADC Channel 1; TOUCH2:Touch Input Channel 2; UART0_TXA: Uart0 Data Out(A); PWM5: Timer5 PWM Output;
30	PD5	I/O	GPIO (Output 0)	
31	PA4	I/O	GPIO (High Voltage)	SPI2_DIA: SPI2 Data In(A); UART2_RXA: Uart2 Data In(A); CAP2: Timer2 Capture;
32	PA3	I/O	GPIO	SPI1_DOC: SPI1 Data Out(C); ADC0: ADC Channel 0; TOUCH0:Touch Input Channel 0; UART2_TXA: Uart2 Data Out(A); PWM1: Timer1 PWM Output;
PAD		P	GND	-

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	5.5	V
LDOIN	Charge Input Voltage	-0.3	6	V
VDDIO	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 Recommended Operating Conditions

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	_
LDOIN	Voltage Input	4.5	5.0	5.5	V	_
Normal mode						
VDDIO	Voltage output	-	3.0	-	V	VBAT= 4.2V, 10mA loading
	Loading current	-	-	100	mA	VDDIO=3V@VBAT = 4.2V
BTAVDD	Voltage output	-	1.25	-	V	VDDIO=3V,10mA loading
	Loading current	-	-	60	mA	BTAVDD=1.25V@VDDIO = 3V
LP mode						
VDDIO	Loading current	-	-	5	mA	VDDIO=3V@VBAT = 4.2V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDOIN	Charge Input Voltage	4.5	5	5.5	V	_
V_{Charge}	Charge Voltage	4.15	4.2	4.25	V	_
I_{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode

I_{Trikl}	Trickle Charge Current	20	45	70	mA	V_{BAT} <V_{Trikl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* VDDIO	V	VDDIO = 3.0V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	–	VDDIO+0.3	V	VDDIO = 3.0V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.33	V	VDDIO = 3.0V
V_{OH}	High-Level Output Voltage	2.7	–	–	V	VDDIO = 3.0V

2.5 Internal Resistor Characteristics

Table 2-5

Port	**Drive Strength**	**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
PA1-PA8, PB1-PB7, PC1-PC5, PD5-PD7	drive_select[11] 64mA drive_select[10] 26.4mA drive_select[01] 8mA drive_select[00] 2.4mA	10K	10K	1. PB1 default pull up 2. USBDM&USBDP default pull down 3. Internal pull-up/pull-down resistance | accuracy ±20% 4. PB8,P00 can pull-up resistance to 5V
PB8,P00	8mA	10K	10K	
USBDP	4mA	1.5K	15K	
USBDM	4mA	180K	15K	

2.6 BT Characteristics

2.6.1 Transmitter

Basic Data Rate **Table 2-6**

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power			6	8	dBm	25℃, Power Supply VBAT=3.7V 2441MHZ
RF Power Control Range			20		dB	
20dB Bandwidth			950		KHz	
Adjacent Channel Transmit Power	+2MHz		-40		dBm	
	-2MHz		-38		dBm	
	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

Enhanced Data Rate **Table 2-7**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1	-3	dB	25℃, Power Supply VBAT=3.7V 2441MHz
π/4 DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		10		%	
	DEVM Peak		15		%	
Adjacent Channel Transmit Power	+2MHz		-40		dBm	
	-2MHz		-38		dBm	
	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

2.6.2 Receiver

Basic Data Rate **Table 2-8**

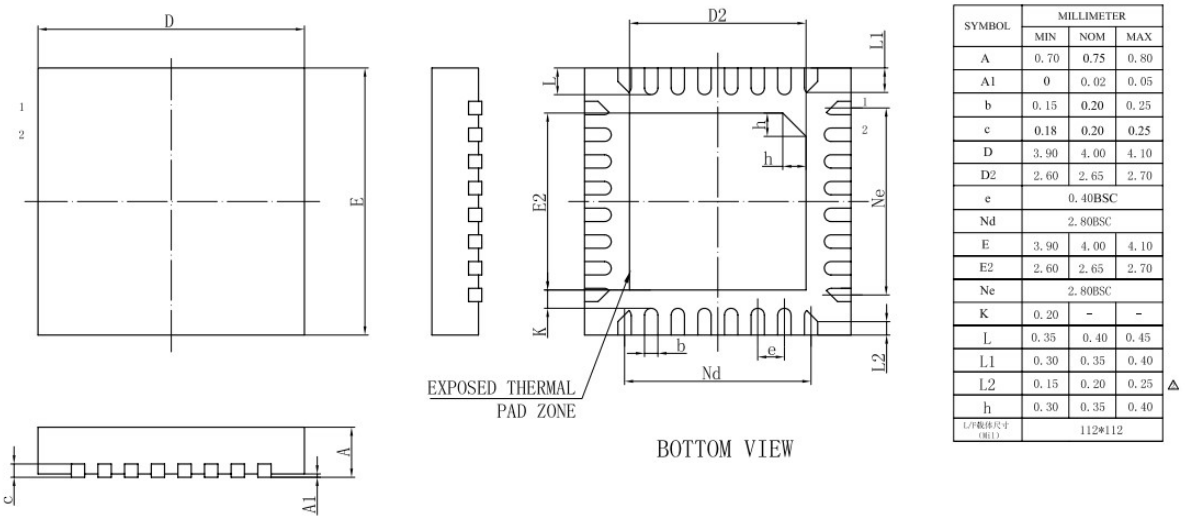
Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25℃, Power Supply VBAT=3.7V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate **Table 2-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25℃, Power Supply VBAT=3.7V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

3. Package Information

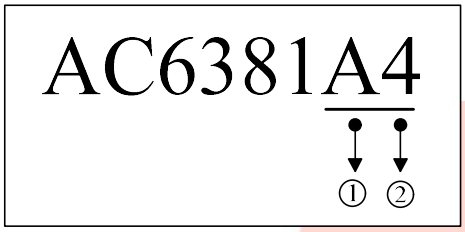
4.1 QFN32(4mm*4mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	112*112		

Figure 4-1 AC6381A_QFN32 Package

4. Package Type Specification



①Represents different packages

②Represents different memory sizes

4: 4Mbit Flash

5. Revision History

Date	Revision	Description
2021.05.19	V1.0	Initial Release