AC6311A Datasheet

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AC6311A Features

High performance 32-bit RISC CPU

- RISC 32-bit CPU
- DC-120MHz operation
- 56KB data RAM
- 8KB Icache 4way
- 64 Vectored interrupts
- 4 Levels interrupt priority

Flexible I/O

- 23 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

Peripheral Feature

- Two Full Speed USB OTG controller
- Four Multi-function 32-bit timers, support capture and PWM mode
- One full-duplex basic UART
- Two full-duplex advanced UART(DMA)
- Three SPI interface supports host and device mode
- One IIC interface supports host and device mode
- RTC,with alarm clock and time base to wake up the chip
- 16-bit PWM generator for motor driving
- Three IQ Encoder
- 16 channels 10-bit ADC
- 1 channel 8 levels Low Power Detector
- Embedded PMU support low power mode
- 2 Crystal Oscillator
- Watchdog
- Power-on reset

Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V5.1+BR+EDR+BLE specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and π/4 DQPSK all paket types
- Provides +8dbm transmitting power
- Receiver with -92dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile

Power Supply

- VBAT is 1.8V to4.5V
- VDDIO is 1.8V to 3.4V

Packages

- QFN32(4x4mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

1. Pin Definition

1.1 Pin Assignment

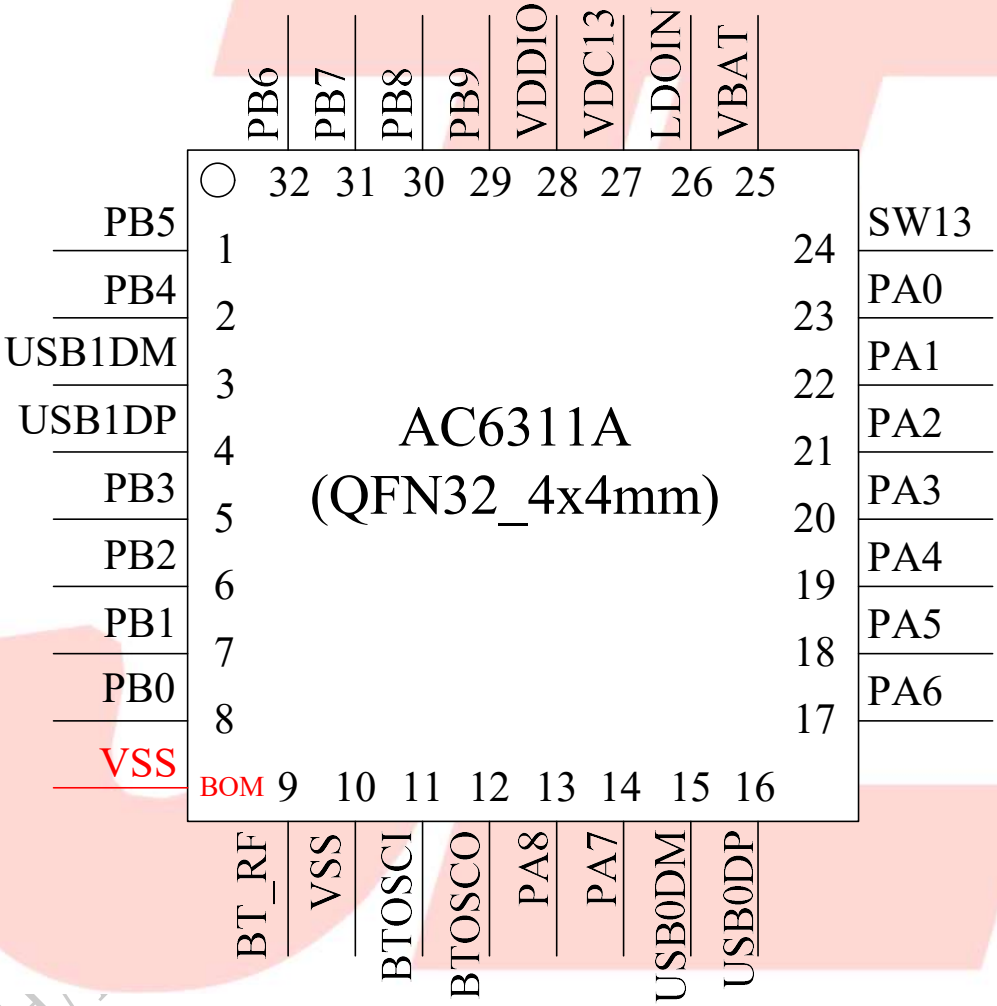


Figure 1-1 AC6311A_QFN32 Package Diagram

1.2 Pin Description

Table 1-1 AC6311A_QFN32 Pin Description

PIN NO.	Name	I/O Type	Function	Other Function
1	PB5	I/O	GPIO (High Voltage Resistance)	SPI2_DIA: SPI2 Data In(A) UART1_RXA: Uart1 Data In(A) PWMCH3L Q-decoder2_1
2	PB4	I/O	GPIO	TMR2: Timer2 Clock In SPI1_DIB: SPI1 Data In(B) Q-decoder2_0 ADC9: ADC Channel 9 UART1_TXA: Uart1 Data Out(A) PWMCH3H
3	USB1DM	I/O	GPIO (pull down)	SPI1_DOB: SPI1 Data Out(B) IIC_SDA_B: IIC SDA(B) ADC6: ADC Channel 6 UART2_RXD: Uart2 Data In(D)
4	USB1DP	I/O	GPIO (pull down)	SPI1_CLKB: SPI1 Clock(B) IIC_SCL_B: IIC SCL(B) ADC5: ADC Channel 5 UART2_TXD: Uart2 Data Out(D)
5	PB3	I/O	GPIO (High Voltage Resistance)	CAP1: Timer1 Capture Q-decoder1_1 UART0_RXB: Uart0 Data In(B) PWMCH2L
6	PB2	I/O	GPIO (pull up)	MCLR Q-decoder1_0 ADC8: ADC Channel 8 UART0_TXB: Uart0 Data Out(B) PWMCH2H
7	PB1	I/O	GPIO (pull up)	PWM2: Timer2 PWM Output ADC7: ADC Channel 7 UART1_RXB: Uart1 Data In(B) Long Press Reset
8	PB0	I/O	GPIO (High Voltage Resistance)	CLKOUT0: Clock Out0 UART1_TXB: Uart1 Data Out(B) TMR2CK
9	BT_RF	-	RF Antenna	-

10	VSS	P	Ground	-
11	BTOSCI	I	BTOSCI	-
12	BTOSCO	O	BTOSCO	-
13	PA8	I/O	GPIO	TMR3: Timer3 Clock In SPI1_DOA: SPI1 Data Out(A) IIC_SDA_C: IIC SDA(C) ADC4: ADC Channel 4 UART1_RXC: Uart1 Data In(C) PWMCH1L
14	PA7	I/O	GPIO	TMR1: Timer1 Clock In SPI1_CLKA: SPI1 Clock(A) IIC_SCL_C: IIC SCL(C) ADC3: ADC Channel 3 UART1_TXC: Uart1 Data Out(C) PWMCH1H
15	USB0DM	I/O	GPIO (pull down)	SPI2_DOB: SPI2 Data Out(B) IIC_SDA_A: IIC SDA(A) ADC11: ADC Channel 11 UART1_RXD: Uart1 Data In(D)
16	USB0DP	I/O	GPIO (pull down)	SPI2_CLKB: SPI2 Clock(B) IIC_SCL_A: IIC SCL(A) ADC10: ADC Channel 10 UART1_TXD: Uart1 Data Out(D)
17	PA6	I/O	GPIO	CAP0: Timer0 Capture SPI1_DIA: SPI1 Data In(A) UART0_RXA: Uart0 Data In(A) TMR1CK
18	PA5	I/O	GPIO	TMR0: Timer0 Clock In SPI2_DIB: SPI2 Data In(B) ADC2: ADC Channel 2 UART0_TXA: Uart0 Data Out(A) TMR0CK
19	PA4	I/O	GPIO	PWM1: Timer1 PWM Output IIC_SDA_D: IIC SDA(D) UART2_RXA: Uart2 Data In(A)
20	PA3	I/O	GPIO	CAP2: Timer2 Capture IIC_SCL_D: IIC SCL(D) ADC1: ADC Channel 1 UART2_TXA: Uart2 Data Out(A) PWMCH0L

21	PA2	I/O	GPIO	CAP3: Timer3 Capture Q-decoder0_1 32K_OSCI UART0_RXC: Uart0 Data In(C) UART1_RTS
22	PA1	I/O	GPIO	PWM0: Timer0 PWM Output Q-decoder0_0 32K_OSCO ADC0: ADC Channel 0 UART0_TXC: Uart0 Data Out(C) UART1_CTS
23	PA0	I/O	GPIO	CLKOUT1 UART2_TXB: Uart2 Data Out(B) UART2_RXB: Uart2 Data In(B) PWMCH0H
24	SW13	P	DC-DC Switch Pin	-
25	VBAT	P	LDO Power	-
26	LDOIN	P	Charge Power 5V	-
27	VDC13	P	Core Power 1.3V	-
28	VDDIO	P	IO Power 3.3V	-
29	PB9	I/O	GPIO	SPI0_DAT2A(2): SPI0 Data2 In(A) UART0_RXD: Uart0 Data In(D) LVD: Low Power Detector
30	PB8	I/O	GPIO	SPI0_DAT3A(3): SPI0 Data3 In(A) UART0_TXD: Uart0 Data Out(D)
31	PB7	I/O	GPIO (High Voltage Resistance)	SPI2_DOA: SPI2 Data Out(A) UART2_RXC: Uart2 Data In(C)
32	PB6	I/O	GPIO	PWM3: Timer3 PWM Output SPI2_CLKA: SPI2 Clock(A) ADC12: ADC Channel 12 UART2_TXC: Uart2 Data Out(C) TMR3CK
Substrate		P	GND	-

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	4.5	V
LDO_IN	Charge Input Voltage	-0.3	6	V
$V_{3.3IO}$	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 Recommended Operating Conditions

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	1.8	3.7	4.5	V	_
LDOIN	Voltage Input	4.5	5.0	5.5	V	_
VDDIO	Voltage output	1.8	3.0	3.4	V	VBAT= 4.2V, 60mA loading
VDC13	Voltage output	1	1.3	1.4	V	DC-DC mode: 40mA loading
IL3.3	Loading current	_	_	60	mA	VBAT = 4.2V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Charge Input Voltage	4.5	5	5.5	V	_
V_{Charge}	Charge Voltage	4.15	4.2	4.25	V	_
I_{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode
I_{Trikl}	Trickle Charge Current	20	45	70	mA	$V_{BAT} < V_{Trikl}$

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	–	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	2.7	–	–	V	VDDIO = 3.3V

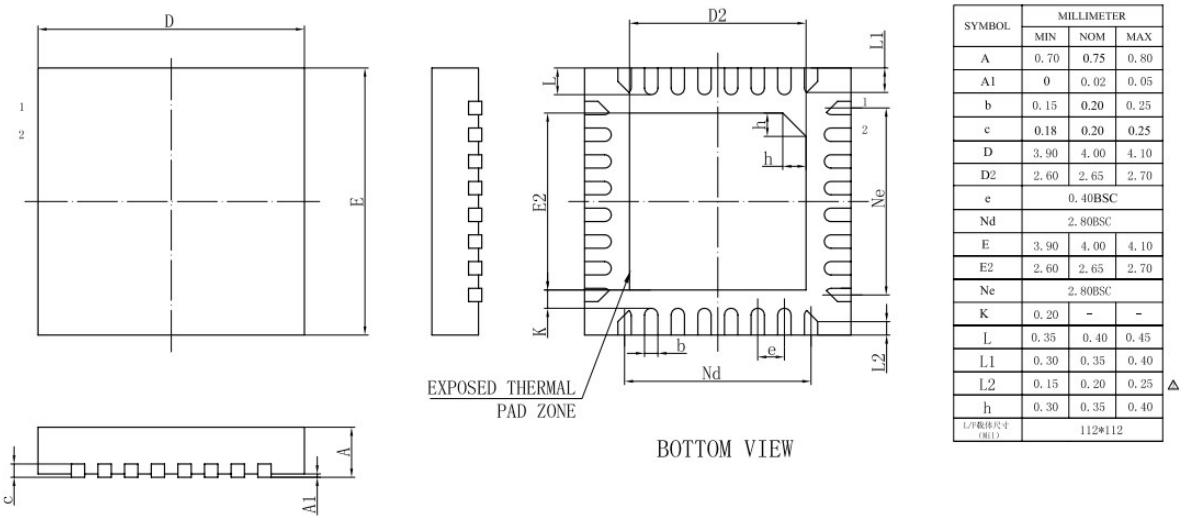
2.5 Internal Resistor Characteristics

Table 2-5

Port	Drive Strength	**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
PA1-PA8, PB1-PB2, PB4,PB6, PB8,PB9	drive_select[11] 24mA drive_select[10] 16mA drive_select[01] 8mA drive_select[00] 2.4mA (with 120ohm res)	10K	10K	1. PB1&PB2 default pull up 2. USB0DM&USB0DP default pull down 3. USB1DM&USB1DP default pull down 4. Internal pull-up/pull-down resistance | accuracy ±20% 5.PA0,PB0,PB3,PB5,PB7 can pull-up resistance to 5V
PA0,PB0, PB3,PB5, PB7	8mA	10K	10K	
USB0DP USB1DP	4mA	1.5K	15K	
USB0DM USB1DM	4mA	180K	15K	

3. Package Information

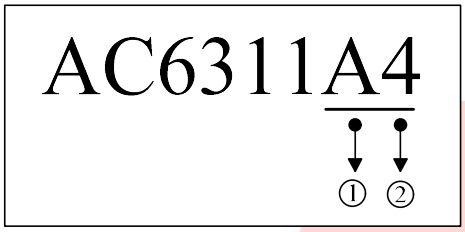
3.1 QFN32(4mm*4mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	112*112		

Figure 3-1. AC6311A_QFN32 Package

4. Package Type Specification



①Represents different packages

②Represents different memory sizes

0: No memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

5. Revision History

Date	Revision	Description
2020.06.06	V1.0	Initial Release
2020.07.13	V1.1	Update I/O Description