Table 7-62 Physical Layer 16.0 GT/s Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 16.0 GT/s Capability is 0026h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.7.5.2 16.0 GT/s Capabilities Register (Offset 04h)

Figure 7-80 16.0 GT/s Capabilities Register

Table 7-63 16.0 GT/s Capabilities Register

Bit Location	Register Description	Attributes
31:0	RsvdP	RsvdP

7.7.5.3 16.0 GT/s Control Register (Offset 08h)

Figure 7-81 16.0 GT/s Control Register

Table 7-64 16.0 GT/s Control Register

Bit Location	Register Description	Attributes
31:0	RsvdP	RsvdP

7.7.5.4 16.0 GT/s Status Register (Offset 0Ch)

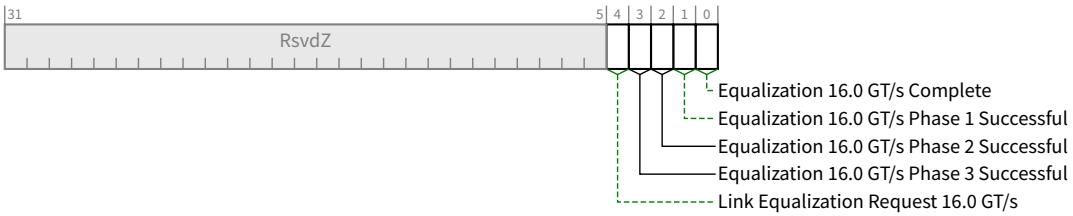

Figure 7-82 16.0 GT/s Status Register

Table 7-65 16.0 GT/s Status Register

Bit Location	Register Description	Attributes
0	***Equalization 16.0 GT/s Complete*** - When Set, this bit indicates that the 16.0 GT/s Transmitter Equalization procedure has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
1	***Equalization 16.0 GT/s Phase 1 Successful*** - When set to 1b, this bit indicates that Phase 1 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
2	***Equalization 16.0 GT/s Phase 2 Successful*** - When set to 1b, this bit indicates that Phase 2 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
3	***Equalization 16.0 GT/s Phase 3 Successful*** - When set to 1b, this bit indicates that Phase 3 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
4	***Link Equalization Request 16.0 GT/s*** - This bit is Set by hardware to request the 16.0 GT/s Link equalization process to be performed on the Link. Refer to Section 4.2.3 and Section 4.2.6.4.2 for details. The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	RW1CS/RsvdZ

7.7.5.5 16.0 GT/s Local Data Parity Mismatch Status Register (Offset 10h)

The Local Data Parity Mismatch Status register is a 32-bit vector where each bit indicates if the local receiver detected a Data Parity mismatch on the Lane with the corresponding Lane number. This Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

This register collects parity errors for 16.0 GT/s and higher data rates. When tracking errors for a specific Link Speed, software should clear this register on speed changes.

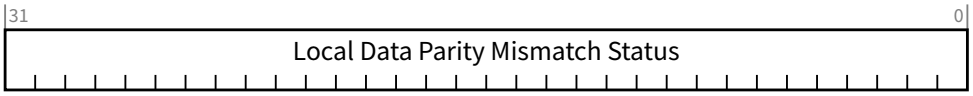

Figure 7-83 16.0 GT/s Local Data Parity Mismatch Status Register

Table 7-66 16.0 GT/s Local Data Parity Mismatch Status Register

Bit Location	Register Description	Attributes
31:0	***Local Data Parity Mismatch Status*** - Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. See Section 4.2.7.2 for more information. The default value of each bit is 0b. For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ.	RW1CS/RsvdZ

7.7.5.6 16.0 GT/s First Retimer Data Parity Mismatch Status Register (Offset 14h)

The First Retimer Data Parity Status register is a 32-bit vector where each bit indicates if the first Retimer of a Path (see Figure 4-36 for more information) detected a Data Parity mismatch on the Lane with the corresponding Lane number. This Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

This register collects parity errors for 16.0 GT/s and higher data rates. When tracking errors for a specific Link Speed, software should clear this register on speed changes.

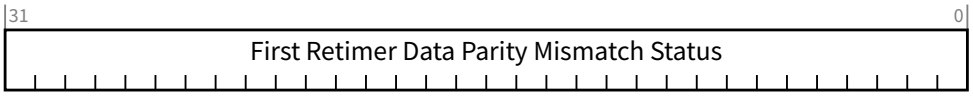

Figure 7-84 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Table 7-67 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Bit Location	Register Description	Attributes
31:0	***First Retimer Data Parity Mismatch Status*** - Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. See Section 4.2.7.2 for more information. The default value of each bit is 0b. The value of this field is undefined when no Retimers are present. For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ.	RW1CS/RsvdZ

7.7.5.7 16.0 GT/s Second Retimer Data Parity Mismatch Status Register (Offset 18h)

The 16.0 GT/s Second Retimer Data Parity Mismatch Status Register is a 32-bit vector where each bit indicates if the second Retimer of a Path (see Figure 4-36 for more information) detected a Data Parity mismatch on the Lane with the corresponding Lane number. This Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

This register collects parity errors for 16.0 GT/s and higher data rates. When tracking errors for a specific Link Speed, software should clear this register on speed changes.

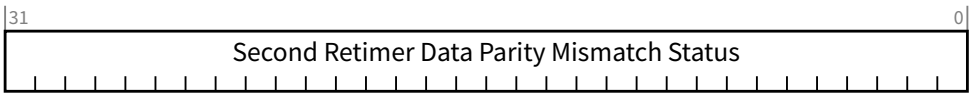

Figure 7-85 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

Table 7-68 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

Bit Location	Register Description	Attributes
31:0	***Second Retimer Data Parity Mismatch Status*** - Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. See Section 4.2.7.2 for more information. The default value of each bit is 0b. The value of this field is undefined when no Retimers are present or only one Retimer is present. For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ.	RW1CS/RsvdZ

7.7.5.8 Physical Layer 16.0 GT/s Reserved (Offset 1Ch)

This register is RsvdP.

7.7.5.9 16.0 GT/s Lane Equalization Control Register (Offsets 20h to 3Ch)

The Equalization Control register consists of control fields required for per-Lane 16.0 GT/s equalization. It contains entries for at least the number of Lanes defined by the Maximum Link Width (see Section 7.5.3.6 or Section 7.9.9.2), must be implemented in whole DW granularity (e.g., if the Maximum Link Width is x1, the register will still contain entries for 4 Lanes with the entries for Lanes 1, 2 and 3 being undefined), and it is permitted to contain up to 32 entries regardless of the Maximum Link Width. The value of entries beyond the Maximum Link Width is undefined.

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

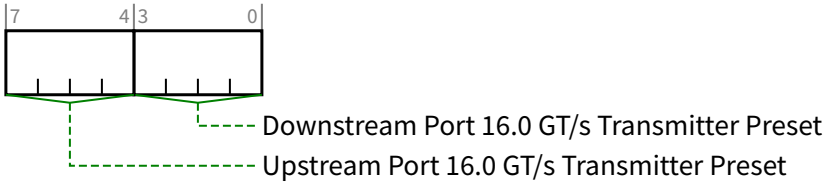

Figure 7-86 16.0 GT/s Lane Equalization Control Register Entry

Table 7-69 ***16.0 GT/s Lane Equalization Control Register Entry***

<table>
<tr><th>Bit Location</th><th>Register Description</th><th>Attributes</th></tr>
<tr><td>3:0</td><td>Downstream Port 16.0 GT/s Transmitter Preset - Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. See Chapter 8 for details. The field encodings are defined in Section 4.2.3.2 .

For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. See Section 7.5.3.18 .

The default value is 1111b.</td><td>HwInit/RsvdP (see description)</td></tr>
<tr><td>7:4</td><td>Upstream Port 16.0 GT/s Transmitter Preset - Field contains the Transmit Preset value sent or received during 16.0 GT/s Link Equalization. Field usage varies as follows:
<table>
<tr><th></th><th>Operating Port Direction</th><th>Crosslink Supported</th><th>Usage</th></tr>
<tr><td>A</td><td>Downstream Port</td><td>Any</td><td>Field contains the value sent on the associated Lane during Link Equalization.

Field is HwInit.</td></tr>
<tr><td>B</td><td>Upstream Port</td><td>0b</td><td>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.

Field is RO.

When crosslinks are supported, case C (below) applies and this captured information is not visible to software.</td></tr>
</table></td><td>HwInit/RO (see description)</td></tr>
</table>

<table>
<tr><th>Bit Location</th><th>Register Description</th><th>Attributes</th></tr>
<tr><td></td><td>
<table>
<tr><th></th><th>Operating Port Direction</th><th>Crosslink Supported</th><th>Usage</th></tr>
<tr><td></td><td></td><td></td><td>Vendors are encouraged to provide an alternate mechanism to obtain this information.</td></tr>
<tr><td>C</td><td>Upstream Port</td><td>1b</td><td>Field is not used or affected by the current Link Equalization.

Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A (above) applies.

Field is HwInit.</td></tr>
</table>
See Section 4.2.3 and Chapter 8 for details. The field encodings are defined in Section 4.2.3.2 .

The default value is 1111b.
</td><td></td></tr>
</table>

7.7.6 Physical Layer 32.0 GT/s Extended Capability

The Physical Layer 32.0 GT/s Extended Capability structure must be implemented in Ports where one or more of the following features are supported:

- The Supported Link Speeds Vector field indicates support for a Link speed of 32.0 GT/s.
- The Function supports sending and/or receiving Modified TS1/TS2 Ordered Sets.

When implemented, this structure must be implemented in:

- A Function associated with a Downstream Port
- A Function of a single-Function Device associated with an Upstream Port
- Function 0 (and only Function 0) of a Multi-Function Device associated with an Upstream Port

This capability is permitted to be implemented in any of the Functions listed above even if the 32.0 GT/s Link speed is not supported. When the 32.0 GT/s Link speed is not supported, the behavior of registers other than the Capability Header is undefined.

Figure 7-87 details allocation of register fields in the Physical Layer 32.0 GT/s Extended Capability structure.

Note that parity errors for 32.0 GT/s are recorded in 16.0 GT/s Local Data Parity Mismatch Status Register, 16.0 GT/s First Retimer Data Parity Mismatch Status Register, and 16.0 GT/s Second Retimer Data Parity Mismatch Status Register. When tracking errors for a specific Link Speed, software should clear those registers on speed changes.

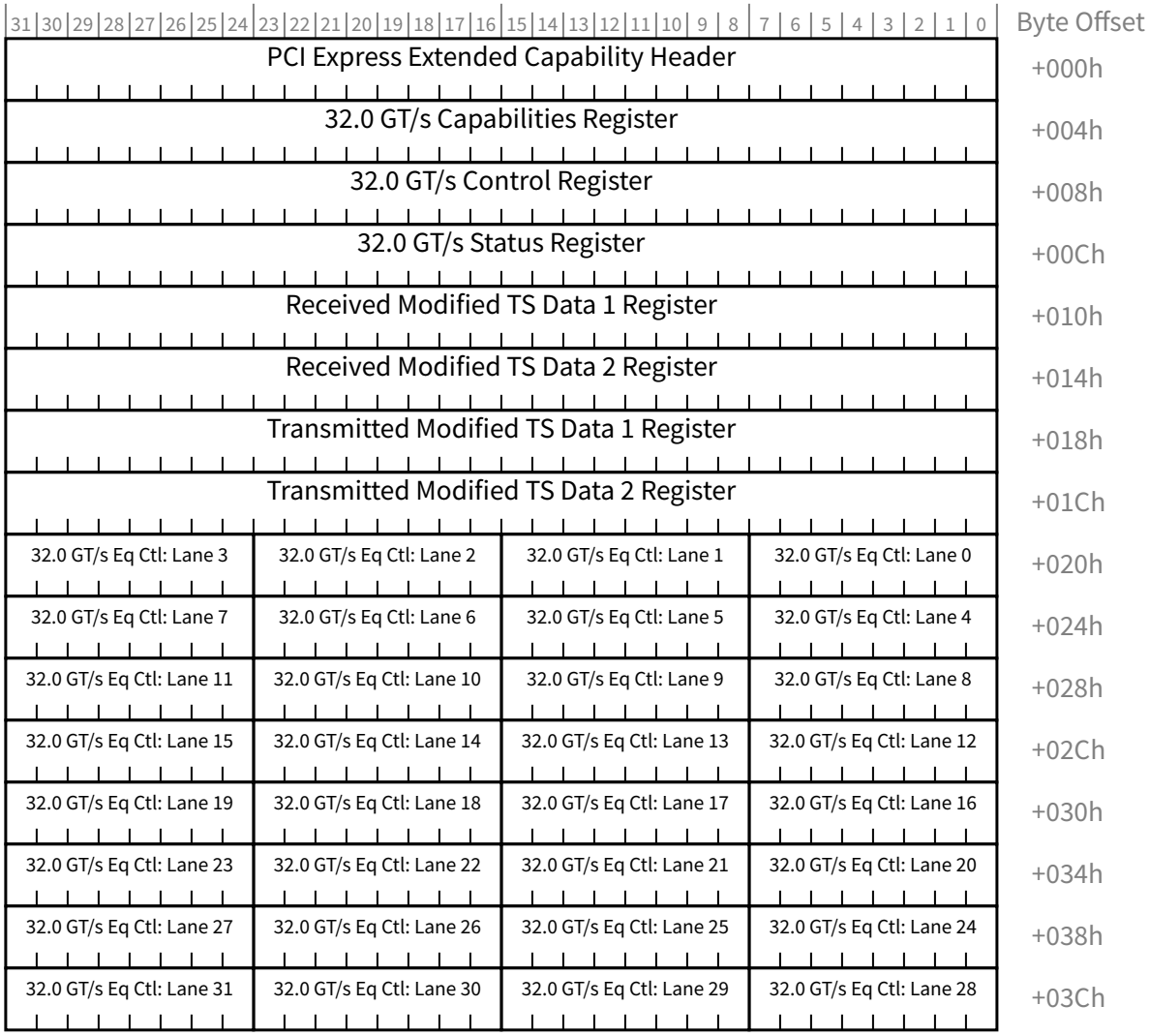

Figure 7-87 Physical Layer 32.0 GT/s Extended Capability

7.7.6.1 Physical Layer 32.0 GT/s Extended Capability Header (Offset 00h)

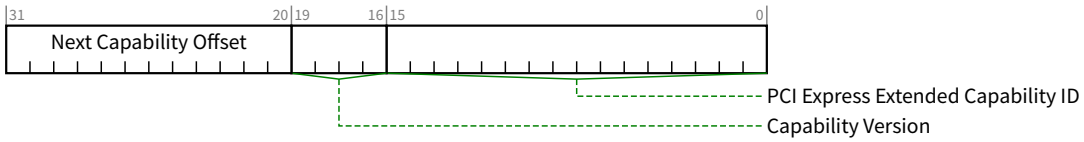

Figure 7-88 Physical Layer 32.0 GT/s Extended Capability Header

Table 7-70 Physical Layer 32.0 GT/s Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 32.0 GT/s Capability is 002Ah.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.7.6.2 32.0 GT/s Capabilities Register (Offset 04h)

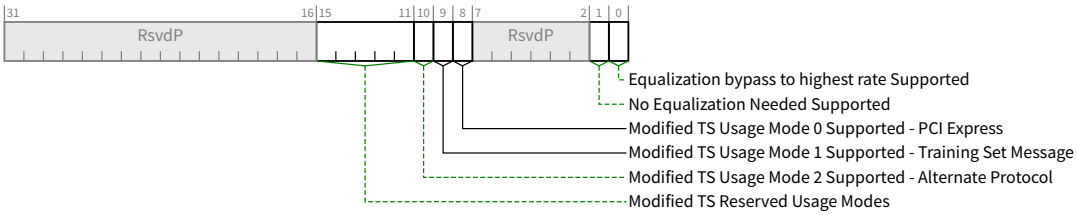

Figure 7-89 32.0 GT/s Capabilities Register

Table 7-71 32.0 GT/s Capabilities Register

Bit Location	Register Description	Attributes
0	***Equalization bypass to highest rate Supported*** - When Set, this Port supports controlling whether the Port negotiates to skip equalization for speeds other than the highest common supported speed. See Section Section 4.2.3 for details. Must be 1b for Ports that support 32.0 GT/s or higher data rates.	HwInit
1	***No Equalization Needed Supported*** - When Set, this Port supports controlling whether or not Equalization is needed.	HwInit
8	***Modified TS Usage Mode 0 Supported - PCI Express*** - This bit indicates that this Port supports PCI Express (Modified TS Usage 000b). This bit must be 1b.	RO
9	***Modified TS Usage Mode 1 Supported - Training Set Message*** - This bit indicates that this Port supports sending and recieving vendor specific Training Set Messages (Modified TS Usage 001b). See Section 4.2.4.2 for details.	HwInit
10	***Modified TS Usage Mode 2 Supported - Alternate Protocol*** - This bit indicates that this Port supports negotiating to use alternate protocols (Modified TS Usage 010b). See Section 4.2.4.2 for details.	HwInit
15:11	***Modified TS Reserved Usage Modes*** - Reserved bits for future Usage Modes defined by the PCISIG. Must be 0 0000b.	RO

7.7.6.3 32.0 GT/s Control Register (Offset 08h)

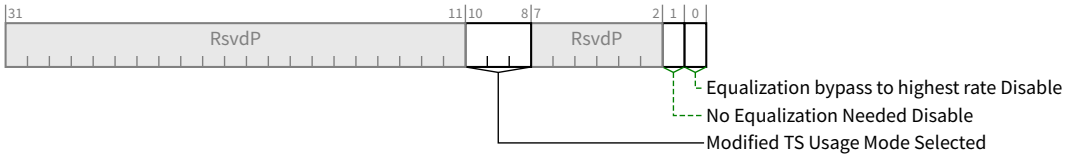

Figure 7-90 32.0 GT/s Control Register

Table 7-72 32.0 GT/s Control Register

Bit Location	Register Description	Attributes
0	***Equalization bypass to highest rate Disable*** - When Clear, this Port indicates during Link Training that is wishes to train to the highest common link data rate and skip equalization of intermediate data rates. See Section 4.2.3 for details. If Equalization bypass to highest rate Supported is Set, this bit is RWS with a default value of 0b. If Equalization bypass to highest rate Supported is Clear, this bit is permitted to be hardwired to 0b.	RWS/RO
1	***No Equalization Needed Disable*** - When Clear, this Port is permitted to indicate that it does not require equalization. When Set, this Port must always indicate that it requires equalization. See Section 4.2.3 for details. If No Equalization Needed Supported is Set, this bit is RWS with a default value of 0b. If No Equalization Needed Supported is Clear, this bit is permitted to be hardwired to 0b.	RWS/RO
10:8	***Modified TS Usage Mode Selected*** - Thie field indicates which Usage Mode will be used by this Downstream Port the next time the Link enters L0 LTSSM State. See Section 4.2.4.2 for details. Behavior is undefined if this field indicates a Usage Mode that is not supported (i.e., associated Modified TS Usage Mode Supported bit is Clear). Unused bits in this field are permitted to be hardwired to 0b. If the only supported usage mode is PCI Express, this field is permitted to he hardwired to 000b. This field is present in Downstream Ports. In Upstream Ports, this field is RsvdP. Default is 000b.	RWS/RO/RsvdP

7.7.6.4 32.0 GT/s Status Register (Offset 0Ch)

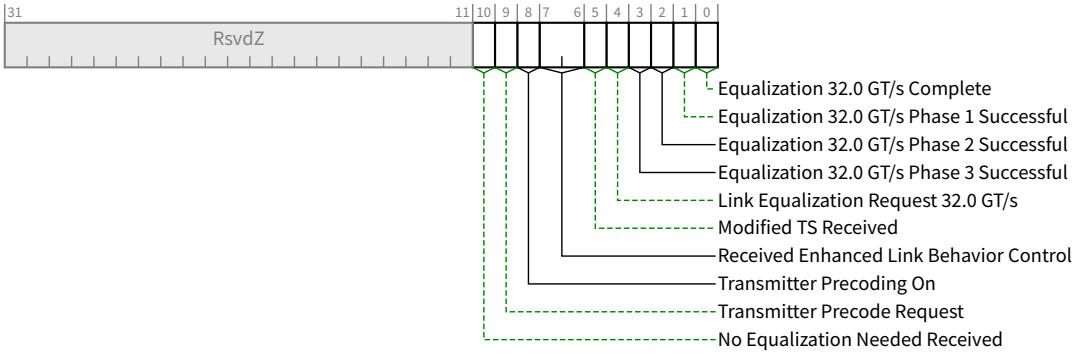

Figure 7-91 32.0 GT/s Status Register

Table 7-73 32.0 GT/s Status Register

Bit Location	Register Description	Attributes
0	***Equalization 32.0 GT/s Complete*** - When Set, this bit indicates that the 32.0 GT/s Transmitter Equalization procedure has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
1	***Equalization 32.0 GT/s Phase 1 Successful*** - When set to 1b, this bit indicates that Phase 1 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
2	***Equalization 32.0 GT/s Phase 2 Successful*** - When set to 1b, this bit indicates that Phase 2 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ
3	***Equalization 32.0 GT/s Phase 3 Successful*** - When set to 1b, this bit indicates that Phase 3 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2 . The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	ROS/RsvdZ

Bit Location	Register Description	Attributes
4	***Link Equalization Request 32.0 GT/s*** - This bit is Set by hardware to request the 32.0 GT/s Link equalization process to be performed on the Link. Refer to Section 4.2.3 and Section 4.2.6.4.2 for details. The default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.	RW1CS/RsvdZ
5	***Modified TS Received*** - If Set, Received Modified TS Data 1 Register and Received Modified TS Data 2 Register contain meaningful data. This bit is Cleared when the Link is Down. This bit is Set when the Modified TS1/TS2 Ordered Set is received (See Section 4.2.6.3.3). Default is 0b.	RO
7:6	***Received Enhanced Link Behavior Control*** - This field contains the Enhanced Link Behavior Control bits from the most recent TS1 or TS2 received in the Polling or Configuration states. See Section 4.2.4.1 , Table 4-6 and Table 4-7 . This field is Cleared on DL_Down. Default is 00b.	RO
8	***Transmitter Precoding On*** - This field indicates whether the Receiver asked this transmitter to enable Precoding. See Section 4.2.2.5 . This bit is cleared on DL_Down. Default is 0b.	RO>
9	***Transmitter Precode Request*** - When Set, this Port will request the transmitter to use Precoding by setting the Transmitter Precode Request bit in the TS1s/TS2s it transmits prior to entry to Recovery.Speed (see Section 4.2.2.5). Default is Implementation Specific.	RO
10	***No Equalization Needed Received*** - When Set, this Port either received a Modified TS1/TS2 with the No Equalization Needed bit Set or received a non-modified TS1/TS2 was recieved with the No Equalization Needed encoding (also reported in the Received Enhanced Link Behavior Control field). Default is 0b.	RO

7.7.6.5 Received Modified TS Data 1 Register (Offset 10h)

This register contains the values received in the Modified TS1/TS2 Ordered Set (see Table 4-8).

If PCI Express (Usage Mode 0) is the only one supported by a Port, this register is permitted to be hardwired to 0000 0000h.

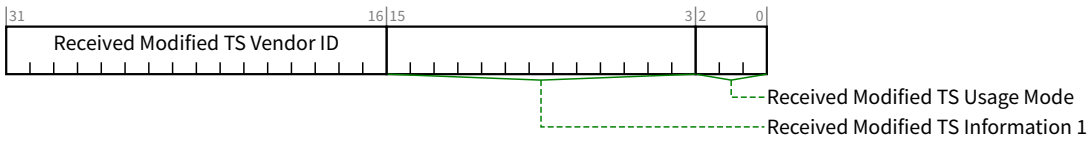

Figure 7-92 Received Modified TS Data 1 Register

Table 7-74 Received Modified TS Data 1 Register

Bit Location	Description	Attributes
2:0	***Received Modified TS Usage Mode*** - If Modified TS Received is Set, this field contains the Modified TS Usage field from the Modified TS1/TS2 Ordered Set (see Section 4.2.6.3.6). If Modified TS Received is Clear, this field contains 000b. Unused bits in this field are permitted to he hardwired to 0b. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 000b. Default is 000b.	RO
15:3	***Received Modified TS Information 1*** - If Modified TS Received is Set, this field contains the Modified TS Information 1 field from the Modified TS1/TS2 Ordered Set (see Section 4.2.6.3.6). If Modified TS Received is Clear, this field contains 0 0000 0000 0000b. Bits 15:8 contain the value of Symbol 9. Bits 7:3 contain bits 7:3 of Symbol 8. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0 0000 0000 0000b. Default is 0 0000 0000 0000b.	RO
31:16	***Received Modified TS Vendor ID*** - If Modified TS Received is Set, this field contains the Training Set Message Vendor ID or Alternate Protocol Vendor ID field from the Modified TS1/TS2 Ordered Set received (see Section 4.2.6.3.6). If Modified TS Received is Clear, this field contains 0000h. Bits 15:8 contain the value of Symbol 11. Bits 7:0 contain the value of Symbol 10. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0000h. Default is 0000h.	RO

7.7.6.6 Received Modified TS Data 2 Register (Offset 14h)

This register contains the values received in Symbols 12 through 14 of the Modified TS1/TS2 (see Table 4-8).

If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h.

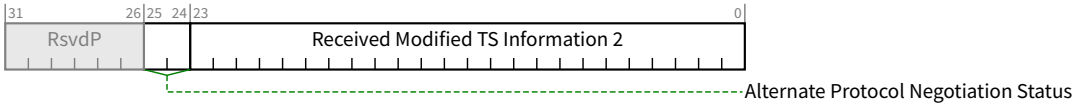

Figure 7-93 Received Modified TS Data 2 Register

Table 7-75 Received Modified TS Data 2 Register

Bit Location	Description	Attributes
23:0	***Received Modified TS Information 2*** - If Modified TS Received is Set, this field contains the Modified TS Information 2 field from the received Modified TS1/TS2 Ordered Set (Section 4.2.6.3.6). If Modified TS Received is Clear, this field contains 00 0000h. Bits 23:16 contain the value of Symbol 14. Bits 16:8 contain the value of Symbol 13. Bits 7:0 contain the value of Symbol 12. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 00 0000h. Default is 00 0000h.	RO
25:24	***Alternate Protocol Negotiation Status*** - Indicates the status of the Alternate Protocol Negotiation. Encodings are: **00b** Alternate Protocol Negotiation not supported - Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear. **01b** Alternate Protocol Negotiation disabled - Modified TS Usage Mode 2 Supported - Alternate Protocol is Set but Modified TS Usage Mode Selected was not 2 during the appropriate LTSSM State. **10b** Alternate Protocol Negotiation failed - Alternate Protocol Negotiation was attempted and did not locate a protocol that was supported on both ends of the Link. **11b** Alternate rotocol Negotiation succeeded - Alternate Protocol Negotiation located one or more protocols that were supported on both ends of the Link and the Downstream Port selected one of those protocols for use. If Set, Alternate Protocol Negotiation completed succesfully. If Clear, Alternate Protocol Negotiation negotiation has not completed succesfully. If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h. If Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear, this bit is hardwired to 0b. If Modified TS Usage Mode Selected does not equal 2, this bit contains 0b. This bit is Cleared on Detect LTSSM State. Default is 0b.	RO

7.7.6.7 Transmitted Modified TS Data 1 Register (Offset 18h)

This register contains the values transmitted in the Modified TS1/TS2 Ordered Set (see Table 4-8).

If PCI Express (Usage Mode 0) is the only one supported by a Port, this register is permitted to be hardwired to 0000 0000h.

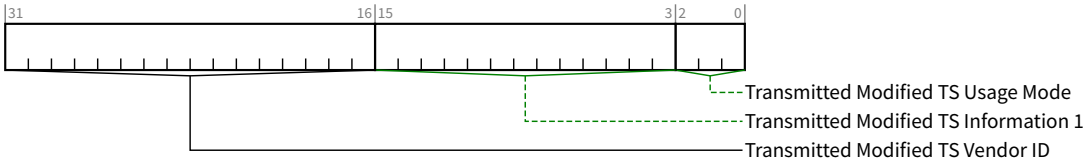

Figure 7-94 Transmitted Modified TS Data 1 Register

Table 7-76 Transmitted Modified TS Data 1 Register

Bit Location	Description	Attributes
2:0	***Transmitted Modified TS Usage Mode*** - If Modified TS Received is Set, this field contains the Modified TS Usage field from the Modified TS2 Ordered Set transmitted during the Configuration.Complete LTSSM State (see Section 4.2.6.3.6). Unused bits in this field are permitted to he hardwired to 0b. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 000b. Default is 000b.	RO
15:3	***Transmitted Modified TS Information 1*** - If Modified TS Received is Set, this field contains the Modified TS Information 1 field from Modified TS2 Ordered Set transmitted during the Configuration.Complete LTSSM State (see Section 4.2.6.3.6). Bits 15:8 contain the value of Symbol 9. Bits 7:3 contain bits 7:3 of Symbol 8. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0 0000 0000 0000b. Default is 0 0000 0000 0000b.	RO
31:16	***Transmitted Modified TS Vendor ID*** - If Modified TS Received is Set, this field contains the Training Set Message Vendor ID or Alternate Protocol Vendor IDfield from the Modified TS2 Ordered Set transmitted during the Configuration.Complete LTSSM State (see Section 4.2.6.3.6). Bits 15:8 contain the value of Symbol 11. Bits 7:0 contain the value of Symbol 10. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0000h. Default is 0000h.	RO

7.7.6.8 Transmitted Modified TS Data 2 Register (Offset 1Ch)

This register contains the values received in Symbols 12 through 14 of the Modified TS1/TS2 (see Table 4-8).

If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h.

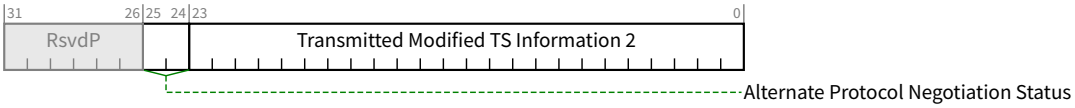

Figure 7-95 Transmitted Modified TS Data 2 Register

Table 7-77 Transmitted Modified TS Data 2 Register

Bit Location	Description	Attributes
23:0	***Transmitted Modified TS Information 2*** - If Modified TS Received is Set, this field contains the Modified TS Information 2 field from the Modified TS2 Ordered Set transmitted during the Configuration.Complete LTSSM State (see Section 4.2.6.3.6). Bits 23:16 contain the value of Symbol 14. Bits 16:8 contain the value of Symbol 13. Bits 7:0 contain the value of Symbol 12. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 00 0000h. Default is 00 0000h.	RO
25:24	***Alternate Protocol Negotiation Status*** - Indicates the status of the Alternate Protocol Negotiation. Encodings are: **00b** Alternate Protocol Negotiation not supported - Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear. **01b** Alternate Protocol Negotiation disabled - Modified TS Usage Mode 2 Supported - Alternate Protocol is Set but Modified TS Usage Mode Selected was not 2 during the appropriate LTSSM State. **10b** Alternate Protocol Negotiation failed - Alternate Protocol Negotiation was attempted and did not locate a protocol that was supported on both ends of the Link. **11b** Alternate rotocol Negotiation succeeded - Alternate Protocol Negotiation located one or more protocols that were supported on both ends of the Link and the Downstream Port selected one of those protocols for use. If Set, Alternate Protocol Negotiation completed succesfully. If Clear, Alternate Protocol Negotiation negotiation has not completed succesfully. If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h. If Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear, this bit is hardwired to 0b. If Modified TS Usage Mode Selected does not equal 2, this bit contains 0b. This bit is Cleared on Detect LTSSM State. Default is 0b.	RO

7.7.6.9 32.0 GT/s Lane Equalization Control Register (Offset 20h)

The 32.0 GT/s Equalization Control register consists of control fields required for per-Lane 32.0 GT/s equalization. It contains entries for at least the number of Lanes defined by the Maximum Link Width (see Section 7.5.3.6 or Section 7.9.9.2), must be implemented in whole DW DW granularity (e.g., if the Maximum Link Width is x1, the register will still

contain entries for 4 Lanes with the entries for Lanes 1, 2 and 3 being undefined), and it is permitted to contain up to 32 entries regardless of the Maximum Link Width. The value of entries beyond the Maximum Link Width is undefined.

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

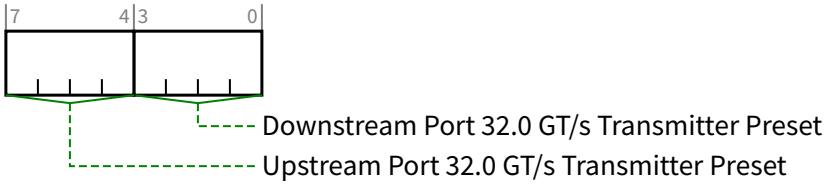

Figure 7-96 32.0 GT/s Lane Equalization Control Register Entry

Table 7-78 ***32.0 GT/s Lane Equalization Control Register Entry***

<table>
<tr><th>Bit Location</th><th>Register Description</th><th>Attributes</th></tr>
<tr><td>3:0</td><td>Downstream Port 32.0 GT/s Transmitter Preset - Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. See Chapter 8 for details. The field encodings are defined in Section 4.2.3.2 .

For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. See Section 7.5.3.18 .

The default value is 1111b.</td><td>HwInit/RsvdP (see description)</td></tr>
<tr><td>7:4</td><td>Upstream Port 32.0 GT/s Transmitter Preset - Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows:
<table>
<tr><th></th><th>Operating Port Direction</th><th>Crosslink Supported</th><th>Usage</th></tr>
<tr><td>A</td><td>Downstream Port</td><td>Any</td><td>Field contains the value sent on the associated Lane during Link Equalization.

Field is HwInit.</td></tr>
<tr><td>B</td><td>Upstream Port</td><td>0b</td><td>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.

Field is RO.

When crosslinks are supported, case C (below) applies and this captured information is not visible to software. Vendors are encouraged to provide an alternate mechanism to obtain this information.</td></tr>
<tr><td>C</td><td>Upstream Port</td><td>1b</td><td>Field is not used or affected by the current Link Equalization.

Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A (above) applies.</td></tr>
</table></td><td>HwInit/RO (see description)</td></tr>
</table>

Bit Location	Register Description	Attributes
	<table><tr><th></th><th>Operating Port Direction</th><th>Crosslink Supported</th><th>Usage</th></tr><tr><td></td><td></td><td></td><td>Field is HwInit.</td></tr></table> See Section 4.2.3 and Chapter 8 for details. The field encodings are defined in Section 4.2.3.2 . The default value is 1111b.	

7.7.7 Lane Margining at the Receiver Extended Capability

The Lane Margining at the Receiver Extended Capability structure must be implemented in:

- A Function associated with a Downstream Port where the Supported Link Speeds Vector field indicates support for a Link speed of 16.0 GT/s or higher.
- A Function of a single-Function Device associated with an Upstream Port where the Supported Link Speeds Vector field indicates support for a Link speed of 16.0 GT/s or higher.
- Function 0 (and only Function 0) of a Multi-Function Device associated with an Upstream Port where the Supported Link Speeds Vector field indicates support for a Link speed of 16.0 GT/s or higher.

Figure 7-97 shows the layout of the Margining Extended Capability. This capability contains a pair of per-Port registers followed by a set of per-Lane registers.

The number of per-Lane entries is determined by the Maximum Link Width (see Section 7.5.3.6 or Section 7.9.9.2). Up to 32 entries are permitted regardless of the Maximum Link Width. The value of entries beyond the Maximum Link Width is undefined.

Each per-Lane entry contains the values for that Lane. Lane numbering uses the default Lane number and is thus invariant to Link width and Lane reversal negotiation that occurs during Link training.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Byte Offset
PCI Express Extended Capability Header		+000h
Margining Port Status Register	Margining Port Capabilities Register	+004h
Margining Lane Status: Lane 0	Margining Lane Control: Lane 0	+008h
Margining Lane Status: Lane 1 (Optional)	Margining Lane Control: Lane 1 (Optional)	+00Ch
Margining Lane Status: Lane 2 (Optional)	Margining Lane Control: Lane 2 (Optional)	+010h
Margining Lane Status: Lane 3 (Optional)	Margining Lane Control: Lane 3 (Optional)	+014h
Margining Lane Status: Lane 4 (Optional)	Margining Lane Control: Lane 4 (Optional)	+018h
Margining Lane Status: Lane 5 (Optional)	Margining Lane Control: Lane 5 (Optional)	+01Ch
Margining Lane Status: Lane 6 (Optional)	Margining Lane Control: Lane 6 (Optional)	+020h
Margining Lane Status: Lane 7 (Optional)	Margining Lane Control: Lane 7 (Optional)	+024h
Margining Lane Status: Lane 8 (Optional)	Margining Lane Control: Lane 8 (Optional)	+028h
Margining Lane Status: Lane 9 (Optional)	Margining Lane Control: Lane 9 (Optional)	+02Ch
Margining Lane Status: Lane 10 (Optional)	Margining Lane Control: Lane 10 (Optional)	+030h
Margining Lane Status: Lane 11 (Optional)	Margining Lane Control: Lane 11 (Optional)	+034h
Margining Lane Status: Lane 12 (Optional)	Margining Lane Control: Lane 12 (Optional)	+038h
Margining Lane Status: Lane 13 (Optional)	Margining Lane Control: Lane 13 (Optional)	+03Ch
Margining Lane Status: Lane 14 (Optional)	Margining Lane Control: Lane 14 (Optional)	+040h
Margining Lane Status: Lane 15 (Optional)	Margining Lane Control: Lane 15 (Optional)	+044h
Margining Lane Status: Lane 16 (Optional)	Margining Lane Control: Lane 16 (Optional)	+048h
Margining Lane Status: Lane 17 (Optional)	Margining Lane Control: Lane 17 (Optional)	+04Ch
Margining Lane Status: Lane 18 (Optional)	Margining Lane Control: Lane 18 (Optional)	+050h
Margining Lane Status: Lane 19 (Optional)	Margining Lane Control: Lane 19 (Optional)	+054h
Margining Lane Status: Lane 20 (Optional)	Margining Lane Control: Lane 20 (Optional)	+058h
Margining Lane Status: Lane 21 (Optional)	Margining Lane Control: Lane 21 (Optional)	+05Ch
Margining Lane Status: Lane 22 (Optional)	Margining Lane Control: Lane 22 (Optional)	+060h
Margining Lane Status: Lane 23 (Optional)	Margining Lane Control: Lane 23 (Optional)	+064h
Margining Lane Status: Lane 24 (Optional)	Margining Lane Control: Lane 24 (Optional)	+068h
Margining Lane Status: Lane 25 (Optional)	Margining Lane Control: Lane 25 (Optional)	+06Ch
Margining Lane Status: Lane 26 (Optional)	Margining Lane Control: Lane 26 (Optional)	+070h
Margining Lane Status: Lane 27 (Optional)	Margining Lane Control: Lane 27 (Optional)	+074h
Margining Lane Status: Lane 28 (Optional)	Margining Lane Control: Lane 28 (Optional)	+078h
Margining Lane Status: Lane 29 (Optional)	Margining Lane Control: Lane 29 (Optional)	+07Ch
Margining Lane Status: Lane 30 (Optional)	Margining Lane Control: Lane 30 (Optional)	+080h
Margining Lane Status: Lane 31 (Optional)	Margining Lane Control: Lane 31 (Optional)	+084h

Figure 7-97 Lane Margining at the Receiver Extended Capability

7.7.7.1 Lane Margining at the Receiver Extended Capability Header (Offset 00h)

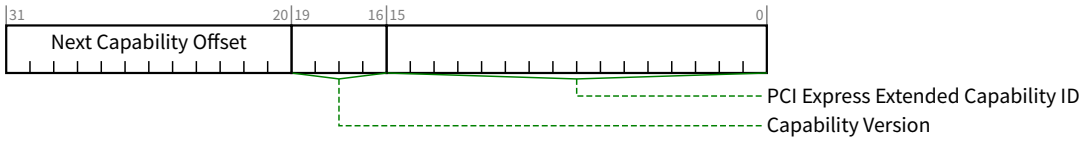

Figure 7-98 Lane Margining at the Receiver Extended Capability Header

Table 7-79 Lane Margining at the Receiver Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 16.0 GT/s Margining Extended Capability is 0027h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.7.7.2 Margining Port Capabilities Register (Offset 04h)

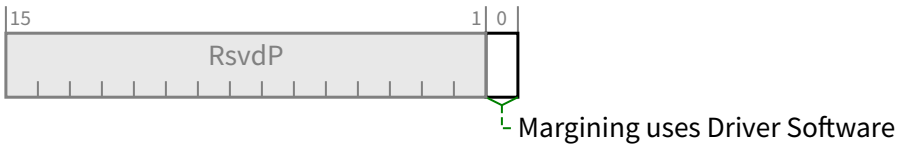

Figure 7-99 Margining Port Capabilities Register

Table 7-80 Margining Port Capabilities Register

Bit Location	Register Description	Attributes
0	***Margining uses Driver Software*** - If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining	HwInit

Bit Location	Register Description	Attributes
	does not require device driver software. In this case the value read from Margining Software Ready is undefined.	

7.7.7.3 Margining Port Status Register (Offset 06h)

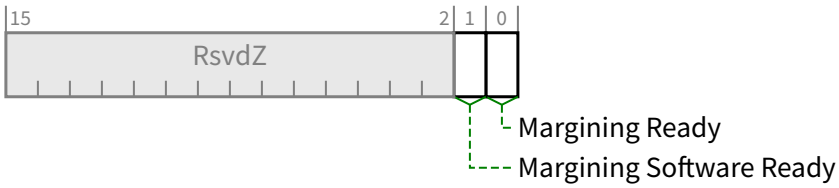

Figure 7-100 Margining Port Status Register

Table 7-81 Margining Port Status Register

Bit Location	Register Description	Attributes
0	***Margining Ready***. - Indicates when the Margining feature is ready to accept margining commands. Behavior is undefined if this bit is Clear and, for any Lane, any of the Receiver Number, Margin Type, Usage Model, or Margin Payload fields are written (see Section 7.7.7.4). If Margining uses Driver Software is Set, Margining Ready must be Set no later than 100 ms after the later of Margining Software Ready becoming Set or the link training to 16.0 GT/s. If Margining uses Driver Software is Clear, Margining Ready must be Set no later than 100 ms after the Link trains to 16.0 GT/s. Default value is implementation specific.	RO
1	***Margining Software Ready*** - When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is undefined if Margining uses Driver Software is Clear. The default value of this bit is implementation specific.	RO

7.7.7.4 Margining Lane Control Register (Offset 08h)

The Margining Lane Control Register consists of control fields required for per-Lane margining.

The number of entries in this register are sized by Maximum Link Width (see Section 7.5.3.6).

See Section 4.2.7.2 for details of this register.

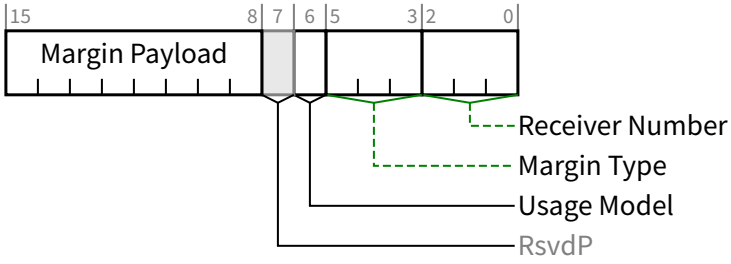

Figure 7-101 Lane N: Margining Control Register Entry

Table 7-82 ***Lane N: Margining Control Register Entry***

Bit Location	Register Description	Attributes
2:0	***Receiver Number*** - See Section 8.4.4 for details. The default value is 000b. This field must be reset to the default value if the Port goes to DL_Down status.	RW (see description)
5:3	***Margin Type*** - See Section 8.4.4 for details. The default value is 111b. This field must be reset to the default value if the Port goes to DL_Down status.	RW (see description)
6	***Usage Model*** - See Section 8.4.4 for details. The default value is 0b. This field must be reset to the default value if the Port goes to DL_Down status.	RW (see description)
15:8	***Margin Payload*** - See Section 8.4.4 for details. This field's value is used in conjunction with the Margin Type field, as described in Section 8.4.4 . The default value is 9Ch. This field must be reset to the default value if the Port goes to DL_Down status.	RW (see description)

7.7.7.5 Margining Lane Status Register (Offset 0Ah)

The Margining Lane Status register consists of status fields required for per-Lane margining. The number of entries in this register are sized by Maximum Link Width (see Section 7.5.3.6). See Section 4.2.7.2 for details of this register.

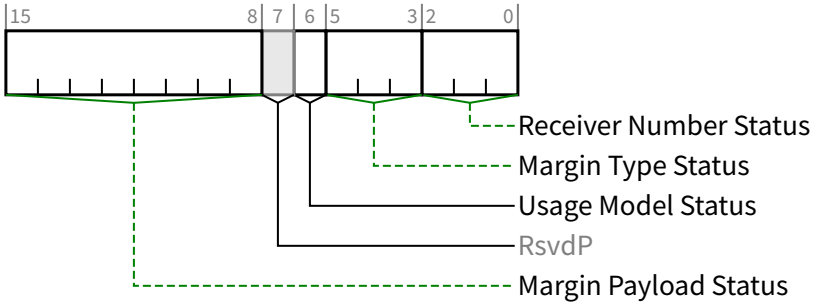

Figure 7-102 Lane N: Margining Lane Status Register Entry

Table 7-83 ***Lane N: Margining Lane Status Register Entry***

Bit Location	Register Description	Attributes
		Control Fields
2:0	***Receiver Number Status*** - See Section 8.4.4 for details. The default value is 000b. For Downstream Ports, this field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)
5:3	***Margin Type Status*** - See Section 8.4.4 for details. The default value is 000b. This field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)
6	***Usage Model Status*** - See Section 8.4.4 for details. The default value is 0b. This field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)
15:8	***Margin Payload Status*** - See Section 8.4.4 for details. This field is only meaningful, when the Margin Type is a defined encoding other than 'No Command'. The default value is 00h. This field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)

7.7.8 ACS Extended Capability

The ACS Extended Capability is an optional capability that provides enhanced access controls (see Section 6.12). This capability may be implemented by a Root Port, a Switch Downstream Port, or a Multi-Function Device Function. It is never applicable to a PCI Express to PCI Bridge or Root Complex Event Collector. It is not applicable to a Switch Upstream Port unless that Switch Upstream Port is a Function in a Multi-Function Device.

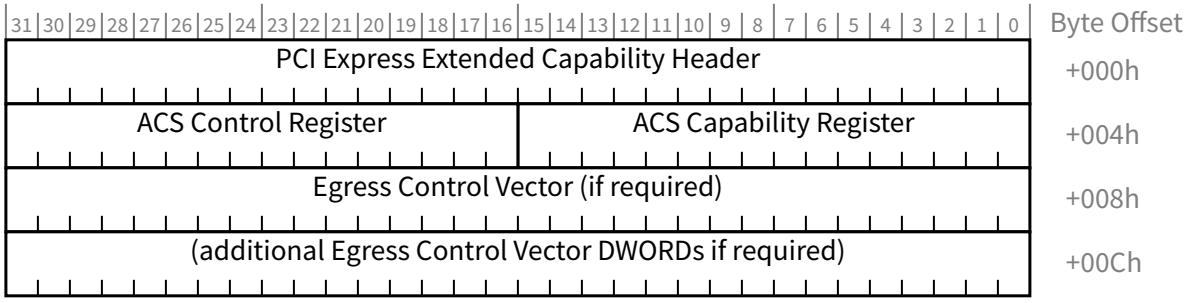

Figure 7-103 ACS Extended Capability

7.7.8.1 ACS Extended Capability Header (Offset 00h)

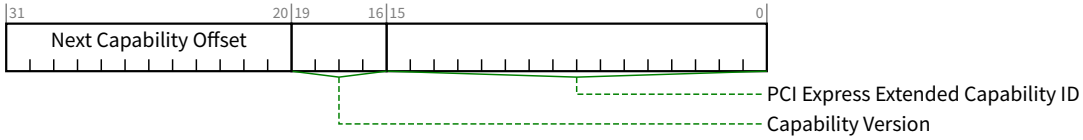

Figure 7-104 ACS Extended Capability Header

Table 7-84 ACS Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the ACS Extended Capability is 000Dh.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.7.8.2 ACS Capability Register (Offset 04h)

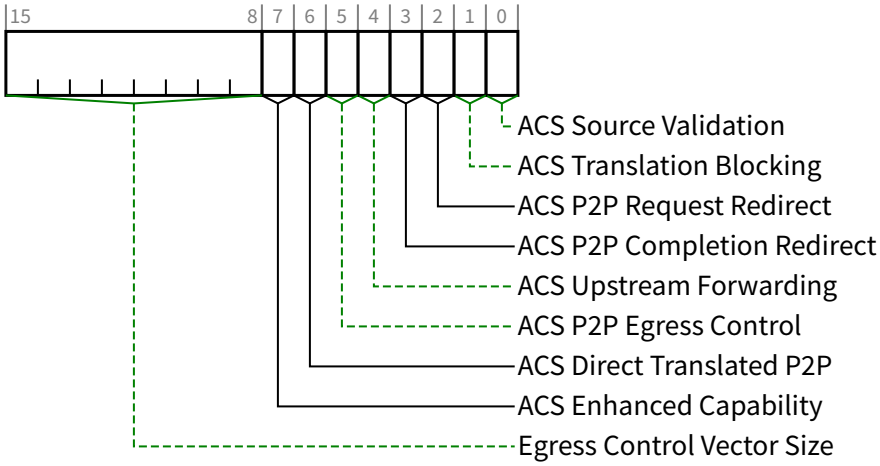

Figure 7-105 ACS Capability Register

Table 7-85 ACS Capability Register

Bit Location	Register Description	Attributes
0	***ACS Source Validation*** - Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.	RO
1	***ACS Translation Blocking*** - Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.	RO
2	***ACS P2P Request Redirect*** - Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for Multi-Function Device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.	RO
3	***ACS P2P Completion Redirect*** - Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.	RO
4	***ACS Upstream Forwarding*** - Required for Root Ports if the RC supports Redirected Request Validation; required for Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Upstream Forwarding.	RO
5	***ACS P2P Egress Control*** - Optional for Root Ports, Switch Downstream Ports, and Multi-Function Device Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Egress Control.	RO
6	***ACS Direct Translated P2P*** - Required for Root Ports that support Address Translation Services (ATS) and also support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for Multi-Function Device Functions that support Address Translation Services (ATS) and also support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Direct Translated P2P.	RO

Bit Location	Register Description	Attributes
7	***ACS Enhanced Capability*** - Required for Root Ports and Switch Downstream Ports that support the ACS Enhanced Capability mechanisms. If Set, indicates that the component supports any of the following mechanisms: • ACS I/O Request Blocking • ACS DSP Memory Target Access • ACS USP Memory Target Access • ACS Unclaimed Request Redirect	RO
15:8	***Egress Control Vector Size*** - Encodings 01h-FFh directly indicate the number of applicable bits in the Egress Control Vector; the encoding 00h indicates 256 bits. If the ACS P2P Egress Control bit is 0b, the value of the size field is undefined, and the Egress Control Vector Register is not required to be present.	HwInit

7.7.8.3 ACS Control Register (Offset 06h)

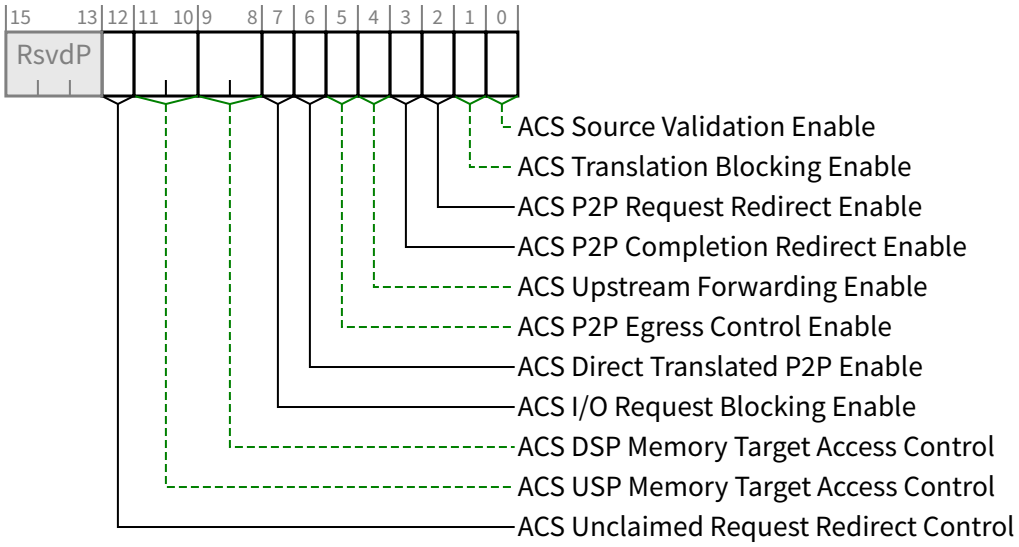

Figure 7-106 ACS Control Register

Table 7-86 ACS Control Register

Bit Location	Register Description	Attributes
0	***ACS Source Validation Enable*** - When Set, the component validates the Bus Number from the Requester ID of Upstream Requests against the secondary/subordinate Bus Numbers. Default value of this bit is 0b. Must be hardwired to 0b if the ACS Source Validation functionality is not implemented.	RW

Bit Location	Register Description	Attributes
1	***ACS Translation Blocking Enable*** - When Set, the component blocks all Upstream Memory Requests whose Address Type (AT) field is not set to the default value. Default value of this bit is 0b. Must be hardwired to 0b if the ACS Translation Blocking functionality is not implemented.	RW
2	***ACS P2P Request Redirect Enable*** - In conjunction with ACS P2P Egress Control and ACS Direct Translated P2P mechanisms, determines when the component redirects peer-to-peer Requests Upstream (see Section 6.12.3). Note that with Downstream Ports, this bit only applies to Upstream Requests arriving at the Downstream Port, and whose normal routing targets a different Downstream Port. Default value of this bit is 0b. Must be hardwired to 0b if the ACS P2P Request Redirect functionality is not implemented.	RW
3	***ACS P2P Completion Redirect Enable*** - Determines when the component redirects peer-to-peer Completions Upstream; applicable only to Completions[146] whose Relaxed Ordering Attribute is clear. Default value of this bit is 0b. Must be hardwired to 0b if the ACS P2P Completion Redirect functionality is not implemented.	RW
4	***ACS Upstream Forwarding Enable*** - When Set, the component forwards Upstream any Request or Completion TLPs it receives that were redirected Upstream by a component lower in the hierarchy. Note that this bit only applies to Upstream TLPs arriving at a Downstream Port, and whose normal routing targets the same Downstream Port. Default value of this bit is 0b. Must be hardwired to 0b if the ACS Upstream Forwarding functionality is not implemented.	RW
5	***ACS P2P Egress Control Enable*** - In conjunction with the Egress Control Vector plus the ACS P2P Request Redirect and ACS Direct Translated P2P mechanisms, determines when to allow, disallow, or redirect peer-to-peer Requests (see Section 6.12.3). Default value of this bit is 0b. Must be hardwired to 0b if the ACS P2P Egress Control functionality is not implemented.	RW
6	***ACS Direct Translated P2P Enable*** - When Set, overrides the ACS P2P Request Redirect and ACS P2P Egress Control mechanisms with peer-to-peer Memory Requests whose Address Type (AT) field indicates a Translated address (see Section 6.12.3). This bit is ignored if ACS Translation Blocking Enable is 1b. Default value of this bit is 0b. Must be hardwired to 0b if the ACS Direct Translated P2P functionality is not implemented.	RW
7	***ACS I/O Request Blocking Enable*** - if Set, Upstream I/O Requests received by the Downstream Port must be handled as ACS Violations. This bit is required for Root Ports and Switch Downstream Ports if the ACS Enhanced Capability bit is Set; otherwise it must be RsvdP. The default value of this bit is 0b.	RW/RsvdP
9:8	***ACS DSP Memory Target Access Control*** - This field controls how a Downstream Port handles Upstream Memory Requests attempting to access any Memory BAR Space on an applicable Root Port or Switch Downstream Port (including the Ingress Port). See Section 6.12.1.1 . Defined Encodings are: **00b** Direct Request access enabled **01b** Request blocking enabled **10b** Request redirect enabled	RW/RsvdP

146. This includes Read Completions, AtomicOp Completions, and other Completions with or without Data.

Bit Location	Register Description	Attributes
	11b Reserved This field is required for Root Ports and Switch Downstream Ports if the ACS Enhanced Capability bit is Set and there is applicable Memory BAR Space to protect; otherwise it must be RsvdP. The default value of this field is 00b.	
11:10	***ACS USP Memory Target Access Control*** - This field controls how a Switch Downstream Port handles Upstream Memory Requests attempting to access any Memory BAR Space on the Switch Upstream Port. See Section 6.12.1.1 . Defined Encodings are: **00b** Direct Request access enabled **01b** Request blocking enabled **10b** Request redirect enabled **11b** Reserved This field is required for Root Ports and Switch Downstream Ports if the ACS Enhanced Capability bit is Set and there is applicable Memory BAR Space to protect; otherwise it must be RsvdP. The default value of this field is 00b.	RW/RsvdP
12	***ACS Unclaimed Request Redirect Control*** - Controls how a Switch Downstream Port handles incoming Requests targeting Memory Space within the Memory aperture of the Switch Upstream Port that is not within a Memory aperture or Memory BAR Space of any Downstream Port within the Switch. When Set, the Switch must forward such Requests Upstream out of the Switch. When Clear, the Switch Downstream Port must handle such Requests as an Unsupported Request (UR). This bit is required for Switch Downstream Ports if the ACS Enhanced Capability bit is Set; otherwise it must be RsvdP. The default value of this bit is 0b.	RW/RsvdP

7.7.8.4 Egress Control Vector Register (Offset 08h)

The Egress Control Vector is a read-write register that contains a bit-array. The number of bits in the register is specified by the Egress Control Vector Size field, and the register spans multiple DWORDs if required. If the ACS P2P Egress Control bit in the ACS Capability Register is 0b, the Egress Control Vector Size field is undefined and the Egress Control Vector Register is not required to be present.

For the general case of an Egress Control Vector spanning multiple DWORDs, the DWORD offset and bit number within that DWORD for a given arbitrary bit *K* are specified by the formulas[147] :

$$\text{DWORD offset} = 08\text{h} + (K \text{ div } 32) \times 4$$

$$\text{DWORD bit\#} = K \bmod 32$$

Equation 7-4 Egress Control Vector Access

Bits in a DWORD beyond those specified by the Egress Control Vector Size field are RsvdP.

For Root Ports and Switch Downstream Ports, each bit in the bit-array always corresponds to a Port Number. Otherwise, for Functions[148] within a Multi-Function Device, each bit in the bit-array corresponds to one or more Function Numbers, or a Function Group Number. For example, access to Function 2 is controlled by bit number 2 in the bit-array. For both

147. Div is an integer divide with truncation. Mod is the remainder from an integer divide.
148. Including Switch Upstream Ports.

Port Number cases and Function Number cases, the bit corresponding to the Function that implements this Extended Capability structure must be hardwired to 0b.[149]

If an ARI Device implements ACS Function Groups (ACS Function Groups Capability is Set), its Egress Control Vector Size is required to be a power-of-2 from 8 to 256, and all of its implemented Egress Control Vector bits must be RW. With ARI Devices, multiple Functions can be associated with a single bit, so for each Function, its associated bit determines how Requests from it targeting other Functions (if any) associated with the same bit are handled.

If ACS Function Groups are enabled in an ARI Device (ACS Function Groups Enable is Set), the first 8 Egress Control Vector bits in each Function are associated with Function Group Numbers instead of Function Numbers. In this case, access control is enforced between Function Groups instead of Functions, and any implemented Egress Control Vector bits beyond the first 8 are unused.

Independent of whether an ARI Device implements ACS Function Groups, its Egress Control Vector Size is not required to cover the entire Function Number range of all Functions implemented by the Device. If ACS Function Groups are not enabled, Function Numbers are mapped to implemented Egress Control Vector bits by taking the modulo of the Egress Control Vector Size, which is constrained to be a power-of-2.

With RCs, some Port Numbers may refer to internal Ports instead of Root Ports. For Root Ports in such RCs, each bit in the bit-array that corresponds to an internal Port must be hardwired to 0b.

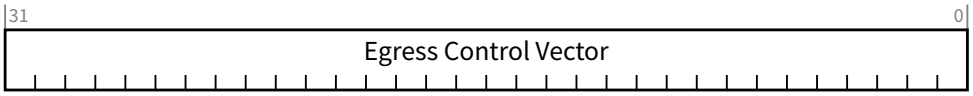

Figure 7-107 Egress Control Vector Register

Table 7-87 Egress Control Vector Register

Bit Location	Register Description	Attributes
31:0	***Egress Control Vector*** - An N-bit bit-array configured by software, where N is given by the value in the Egress Control Vector Size field. When a given bit is set, peer-to-peer Requests targeting the associated Port, Function, or Function Group are blocked or redirected (if enabled) (see Section 6.12.3). Figure 7-107 shows a single DWORD register. This register is always an integral number of DWORDs. Default value of each bit is 0b.	RW

The following examples illustrate how the vector might be configured:

- For an 8-Port Switch, each Port will have a separate vector indicating which Downstream Egress Ports it may forward Requests to.
  Port 1 being not allowed to communicate with any other Downstream Ports would be configured as:
  1111 1100b with bit 0 corresponding to the Upstream Port (hardwired to 0b) and bit 1 corresponding to the Ingress Port (hardwired to 0b).

  Port 2 being allowed to communicate with Ports 3, 5, and 7 would be configured as: 0101 0010b.

- For a 4-Function device, each Function will have a separate vector that indicates which Function it may forward Requests to.
  Function 0 being not allowed to communicate with any other Functions would be configured as: 1110b with bit 0 corresponding to Function 0 (hardwired to 0b).

149. For ARI Devices, the bit must be RW. See subsequent description.

Function 1 being allowed to communicate with Functions 2 and 3 would be configured as: 0001b with bit 1 corresponding to Function 1 (hardwired to 0b).

7.8 Common PCI and PCIe Capabilities

This section, contains a description of common PCI and PCIe capabilities that are individually optional in this but may be required by other PCISIG specifications.

7.8.1 *Power Budgeting Extended Capability*

The Power Budgeting Extended Capability allows the system to allocate power to devices that are added to the system at runtime. Through this Capability, a device can report the power it consumes on a variety of power rails, in a variety of device power-management states, in a variety of operating conditions. The system can use this information to ensure that the system is capable of providing the proper power and cooling levels to the device. Failure to indicate proper device power consumption may risk device or system failure.

Implementation of the Power Budgeting Extended Capability is optional for PCI Express devices that are implemented either in a form factor which does not require Hot-Plug support, or that are integrated on the system board. PCI Express form factor specifications may require support for power budgeting. Figure 7-108 details allocation of register fields in the Power Budgeting Extended Capability.

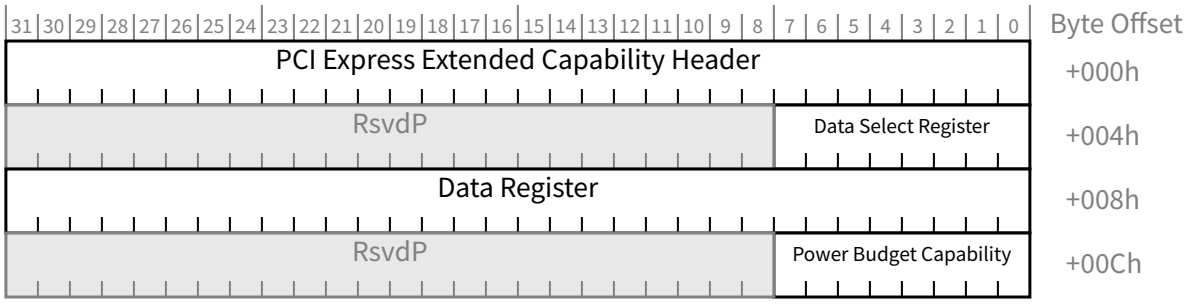

Figure 7-108 Power Budgeting Extended Capability

7.8.1.1 *Power Budgeting Extended Capability Header (Offset 00h)*

Figure 7-109 details allocation of register fields in the Power Budgeting Extended Capability Header; Table 7-88 provides the respective bit definitions. Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. The Extended Capability ID for the Power Budgeting Extended Capability is 0004h.

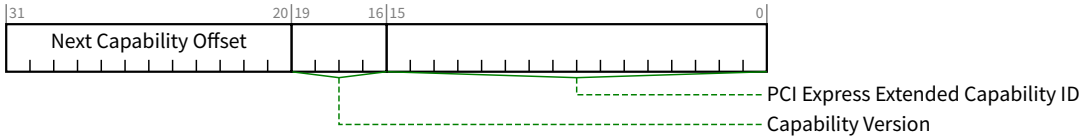

Figure 7-109 Power Budgeting Extended Capability Header

Table 7-88 Power Budgeting Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Power Budgeting Extended Capability is 0004h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.8.1.2 Power Budgeting Data Select Register (Offset 04h)

The Power Budgeting Data Select Register is an 8-bit read-write register that indexes the Power Budgeting Data reported through the Power Budgeting Data Register and selects the DWORD of Power Budgeting Data that is to appear in the Power Budgeting Data Register. Values for this register start at zero to select the first DWORD of Power Budgeting Data; subsequent DWORDs of Power Budgeting Data are selected by increasing index values. The default value of this register is undefined.

7.8.1.3 Power Budgeting Data Register (Offset 08h)

This read-only register returns the DWORD of Power Budgeting Data selected by the Power Budgeting Data Select Register. Each DWORD of the Power Budgeting Data describes the power usage of the device in a particular operating condition. Power Budgeting Data for different operating conditions is not required to be returned in any particular order, as long as incrementing the Power Budgeting Data Select Register causes information for a different operating condition to be returned. If the Power Budgeting Data Select Register contains a value greater than or equal to the number of operating conditions for which the device provides power information, this register must return all zeros. The default value of this register is undefined. Figure 7-110 details allocation of register fields in the Power Budgeting Data Register; Table 7-89 provides the respective bit definitions.

The Base Power and Data Scale fields describe the power usage of the device; the Power Rail, Type, PM State, and PM Sub State fields describe the conditions under which the device has this power usage.

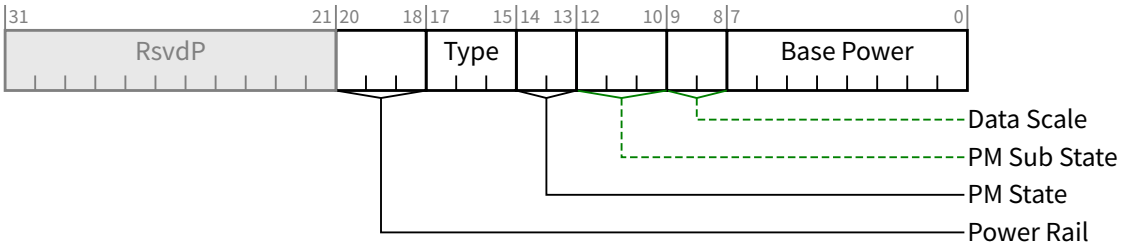

Figure 7-110 Power Budgeting Data Register

Table 7-89 Power Budgeting Data Register

Bit Location	Register Description	Attributes
7:0	***Base Power*** - Specifies in watts the base power value in the given operating condition. This value must be multiplied by the data scale to produce the actual power consumption value except when the Data Scale field equals 00b (1.0x) and Base Power exceeds EFh, the following alternative encodings are used: **F0h** greater than 239 W and less than or equal to 250 W Slot Power Limit **F1h** greater than 250 W and less than or equal to 275 W Slot Power Limit **F2h** greater than 275 W and less than or equal to 300 W Slot Power Limit **F3h to FFh** Reserved for values greater than 300 W	RO
9:8	***Data Scale*** - Specifies the scale to apply to the Base Power value. The power consumption of the device is determined by multiplying the contents of the Base Power field with the value corresponding to the encoding returned by this field, except as noted above. Defined encodings are: **00b** 1.0x **01b** 0.1x **10b** 0.01x **11b** 0.001x	RO
12:10	***PM Sub State*** - Specifies the power management sub state of the operating condition being described. Defined encodings are: **000b** Default Sub State **001b - 111b** Device Specific Sub State	RO
14:13	***PM State*** - Specifies the power management state of the operating condition being described. Defined encodings are: **00b** D0 **01b** D1 **10b** D2 **11b** D3 A device returns 11b in this field and Aux or PME Aux in the Type field to specify the $D3_{Cold}$ PM State. An encoding of 11b along with any other Type field value specifies the $D3_{Hot}$ state.	RO

Bit Location	Register Description	Attributes
17:15	***Type*** - Specifies the type of the operating condition being described. Defined encodings are: **000b** PME Aux **001b** Auxiliary **010b** Idle **011b** Sustained **100b** Sustained - Emergency Power Reduction State (see Section 6.25) **101b** Maximum - Emergency Power Reduction State (see Section 6.25) **111b** Maximum **Others** All other encodings are Reserved.	RO
20:18	***Power Rail*** - Specifies the thermal load or power rail of the operating condition being described. Defined encodings are: **000b** Power (12V) **001b** Power (3.3V) **010b** Power (1.5V or 1.8V) **111b** Thermal **Others** All other encodings are Reserved.	RO

A device that implements the Power Budgeting Extended Capability is required to provide data values for the D0 Maximum and D0 Sustained PM State and Type combinations for every power rail from which it consumes power; data for the D0 Maximum and D0 Sustained for Thermal must also be provided if these values are different from the sum of the values for an operating condition reported for D0 Maximum and D0 Sustained on the power rails.

Devices that support auxiliary power or PME from auxiliary power must provide data for the appropriate power Type (Auxiliary or PME Aux).

If a device implements Emergency Power Reduction State, it must report Power Budgeting values for the following:

- Maximum Emergency Power Reduction State, PM State D0, all power rails used by the device
- Maximum Emergency Power Reduction State, PM State D0, Thermal (if different from the sum of the preceding values)
- Sustained Emergency Power Reduction State, PM State D0, all power rails used by the device
- Sustained Emergency Power Reduction State, PM State: D0, Thermal (if different from the sum of the preceding values)

7.8.1.4 Power Budgeting Capability Register (Offset 0Ch)

This register indicates the power budgeting capabilities of a device. Figure 7-111 details allocation of register fields in the Power Budgeting Capability Register; Table 7-90 provides the respective bit definitions.

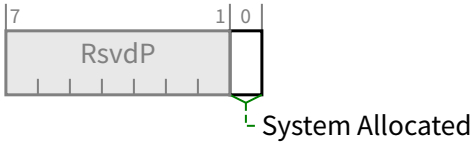

Figure 7-111 Power Budgeting Capability Register

Table 7-90 Power Budgeting Capability Register

Bit Location	Register Description	Attributes
0	***System Allocated*** - When Set, this bit indicates that the power budget for the device is included within the system power budget. Reported Power Budgeting Data for this device must be ignored by software for power budgeting decisions if this bit is Set.	HwInit

7.8.2 *Latency Tolerance Reporting (LTR) Extended Capability*

The PCI Express Latency Tolerance Reporting (LTR) Extended Capability is an optional Extended Capability that allows software to provide platform latency information to components with Upstream Ports (Endpoints and Switches), and is required for Switch Upstream Ports and Endpoints if the Function supports the LTR mechanism. It is not applicable to Root Ports, Bridges, or Switch Downstream Ports.

For a Multi-Function Device associated with the Upstream Port of a component that implements the LTR mechanism, this Capability structure must be implemented only in Function 0, and must control the component's Link behavior on behalf of all the Functions of the Device.

RCiEPs implemented as Multi-Function Devices are permitted to implement this Capability structure in more than one Function of the Multi-Function Device.

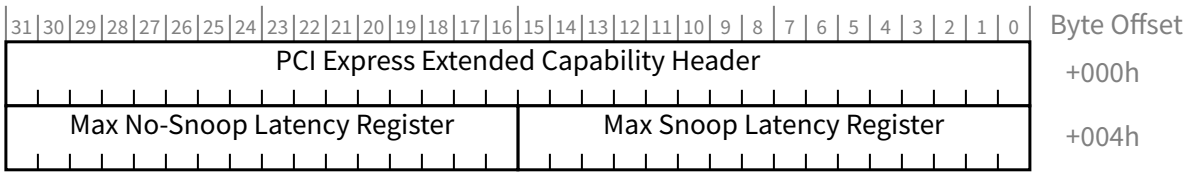

Figure 7-112 LTR Extended Capability Structure

7.8.2.1 LTR Extended Capability Header (Offset 00h)

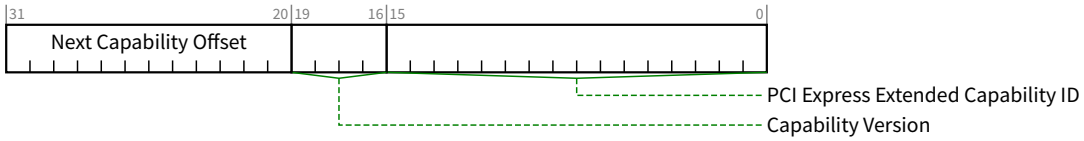

Figure 7-113 LTR Extended Capability Header

Table 7-91 LTR Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability for the LTR Extended Capability is 0018h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.8.2.2 Max Snoop Latency Register (Offset 04h)

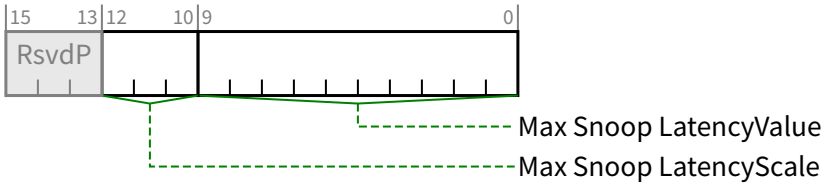

Figure 7-114 Max Snoop Latency Register

Table 7-92 Max Snoop Latency Register

Bit Location	Register Description	Attributes
9:0	***Max Snoop LatencyValue*** - Along with the Max Snoop LatencyScale field, this register specifies the maximum snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. The default value for this field is 00 0000 0000b.	RW

Bit Location	Register Description	Attributes
12:10	***Max Snoop LatencyScale*** - This register provides a scale for the value contained within the Max Snoop LatencyValue field. Encoding is the same as the LatencyScale fields in the LTR Message. See Section 6.18 . It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. The default value for this field is 000b. Hardware operation is undefined if software writes a Not Permitted value to this field.	RW

7.8.2.3 Max No-Snoop Latency Register (Offset 06h)

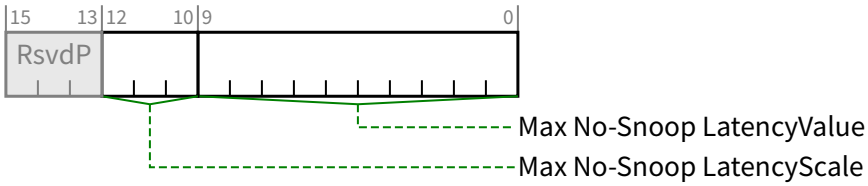

Figure 7-115 Max No-Snoop Latency Register

Table 7-93 Max No-Snoop Latency Register

Bit Location	Register Description	Attributes
9:0	***Max No-Snoop LatencyValue*** - Along with the Max No-Snoop LatencyScale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. The default value for this field is 00 0000 0000b.	RW
12:10	***Max No-Snoop LatencyScale*** - This register provides a scale for the value contained within the Max No-Snoop LatencyValue field. Encoding is the same as the LatencyScale fields in the LTR Message. See Section 6.18 . It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. The default value for this field is 000b. Hardware operation is undefined if software writes a Not Permitted value to this field.	RW

7.8.3 L1 PM Substates Extended Capability

The L1 PM Substates Extended Capability is an optional Extended Capability, that is required if L1 PM Substates is implemented at a Port. The L1 PM Substates Extended Capability structure is defined as shown in Figure 7-116 .

For a Multi-Function Device associated with an Upstream Port implementing L1 PM Substates, this Extended Capability Structure must be implemented only in Function 0, and must control the Upstream Port's Link behavior on behalf of all the Functions of the device.

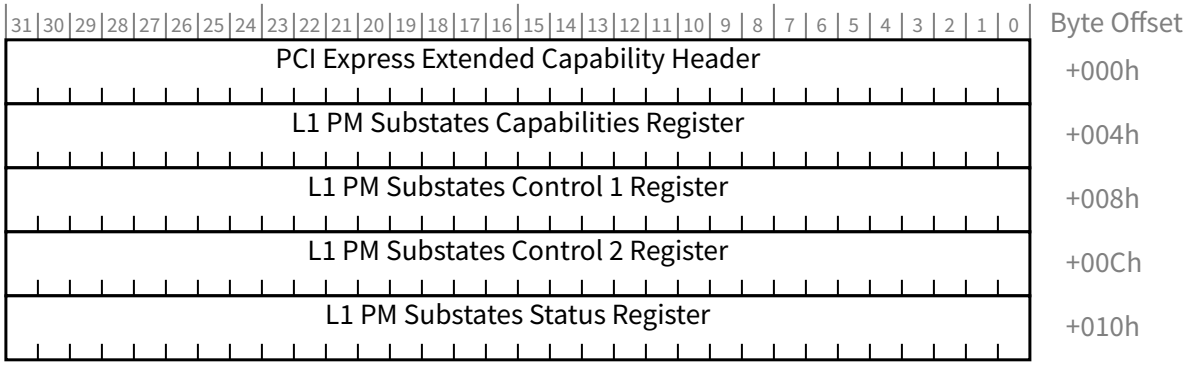

Figure 7-116 L1 PM Substates Extended Capability

7.8.3.1 L1 PM Substates Extended Capability Header (Offset 00h)

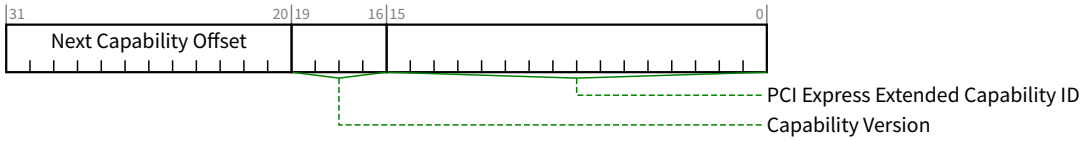

Figure 7-117 L1 PM Substates Extended Capability Header

Table 7-94 L1 PM Substates Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 PM Substates is 001Eh.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the L1 PM Substates Status Register is implemented and must be 1h otherwise.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.	RO

7.8.3.2 L1 PM Substates Capabilities Register (Offset 04h)

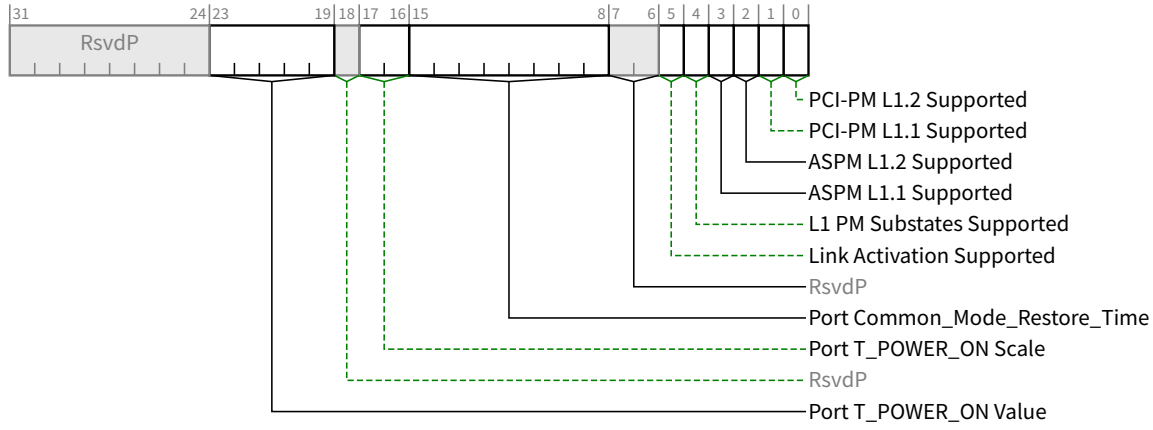

Figure 7-118 L1 PM Substates Capabilities Register

Table 7-95 L1 PM Substates Capabilities Register

Bit Location	Register Description	Attributes
0	***PCI-PM L1.2 Supported*** - When Set this bit indicates that PCI-PM L1.2 is supported.	HwInit
1	***PCI-PM L1.1 Supported*** - When Set this bit indicates that PCI-PM L1.1 is supported, and must be Set by all Ports implementing L1 PM Substates.	HwInit
2	***ASPM L1.2 Supported*** - When Set this bit indicates that ASPM L1.2 is supported.	HwInit
3	***ASPM L1.1 Supported*** - When Set this bit indicates that ASPM L1.1 is supported.	HwInit
4	***L1 PM Substates Supported*** - When Set this bit indicates that this Port supports L1 PM Substates.	HwInit
5	***Link Activation Supported*** - For Downstream Ports, when Set, this bit indicates that this Port supports Link Activation. See Section 5.5.6 for details. This bit is of type RsvdP for Upstream Ports.	HwInit/RsvdP
15:8	***Port Common_Mode_Restore_Time*** - Time (in µs) required for this Port to re-establish common mode as described in Table 5-11 . Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP.	HwInit/RsvdP (See description)
17:16	***Port T_POWER_ON Scale*** - Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities Register. Range of Values **00b** 2 µs **01b** 10 µs **10b** 100 µs **11b** Reserved	HwInit/RsvdP

Bit Location	Register Description	Attributes
	Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Default value is 00b	
23:19	***Port T_POWER_ON Value*** - Along with the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities Register sets the time (in µs) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities Register. Default value is 00101b Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP.	HwInit/RsvdP

7.8.3.3 L1 PM Substates Control 1 Register (Offset 08h)

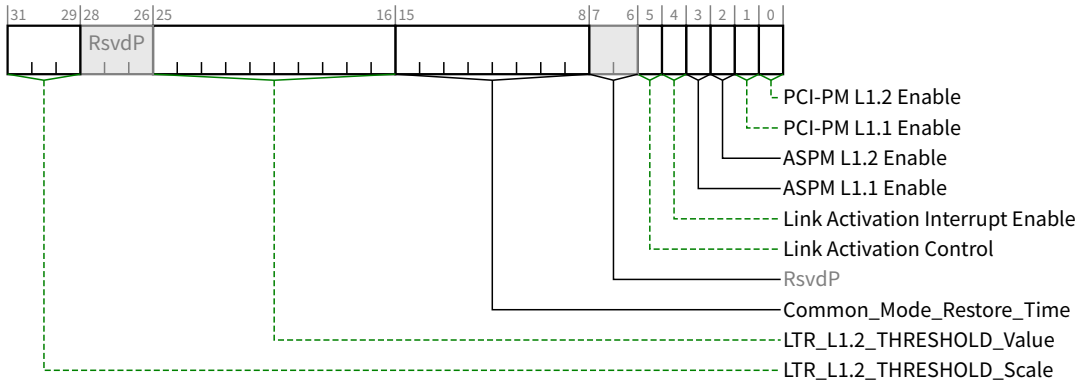

Figure 7-119 L1 PM Substates Control 1 Register

Table 7-96 L1 PM Substates Control 1 Register

Bit Location	Register Description	Attributes
0	***PCI-PM L1.2 Enable*** - When Set this bit enables PCI-PM L1.2. Required for both Upstream and Downstream Ports. For Ports for which the PCI-PM L1.2 Supported bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW
1	***PCI-PM L1.1 Enable*** - When Set this bit enables PCI-PM L1.1. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW

Bit Location	Register Description	Attributes
2	***ASPM L1.2 Enable*** - When Set this bit enables ASPM L1.2. Required for both Upstream and Downstream Ports. For Ports for which the ASPM L1.2 Supported bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW
3	***ASPM L1.1 Enable*** - When Set this bit enables ASPM L1.1. Required for both Upstream and Downstream Ports. For Ports for which the ASPM L1.1 Supported bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW
4	***Link Activation Interrupt Enable*** - When set this bit enables the generation of an interrupt to indicate the completion of the Link Activation process. See Section 5.5.6 for details. Required for Downstream Ports when the Link Activation Supported bit is Set, otherwise it is permitted to be hardwired to 0b. Must be RsvdP for Upstream Ports. Default value is 0b.	RW/RsvdP
5	***Link Activation Control*** - When this bit is Set, the Port must initiate the Link Activation process. See Section 5.5.6 for details. Required for Downstream Ports when the Link Activation Supported bit is Set, otherwise it is permitted to be hardwired to 0b. Must be RsvdP for Upstream Ports. Default value is 0b.	RW/RsvdP
15:8	***Common_Mode_Restore_Time*** - Sets value of $T_{COMMONMODE}$ (in µs), which must be used by the Downstream Port for timing the re-establishment of common mode, as described in Table 5-11 . This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are Set. Required for Downstream Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. This field is of type RsvdP for Upstream Ports. Default value is implementation specific.	RW/RsvdP (See Description)
25:16	***LTR_L1.2_THRESHOLD_Value*** - Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled). The default value for this field is 00 0000 0000b. This field must only be modified when the ASPM L1.2 Enable bit is Clear. The Port behavior is undefined if this field is modified when the ASPM L1.2 Enable bit is Set. Required for all Ports for which the ASPM L1.2 Supported bit is Set, otherwise this field is of type RsvdP.	RW/RsvdP (See Description)

Bit Location	Register Description	Attributes
31:29	***LTR_L1.2_THRESHOLD_Scale*** - This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. Encoding is the same as the LatencyScale fields in the LTR Message (see Section 6.18). The default value for this field is 000b. Hardware operation is undefined if software writes a Not-Permitted value to this field. This field must only be modified when the ASPM L1.2 Enable bit is Clear. The Port behavior is undefined if this field is modified when the ASPM L1.2 Enable bit is Set. Required for all Ports Ports for which the ASPM L1.2 Supported bit is Set, otherwise this field is of type RsvdP.	RW/RsvdP (See description)

7.8.3.4 L1 PM Substates Control 2 Register (Offset 0Ch)

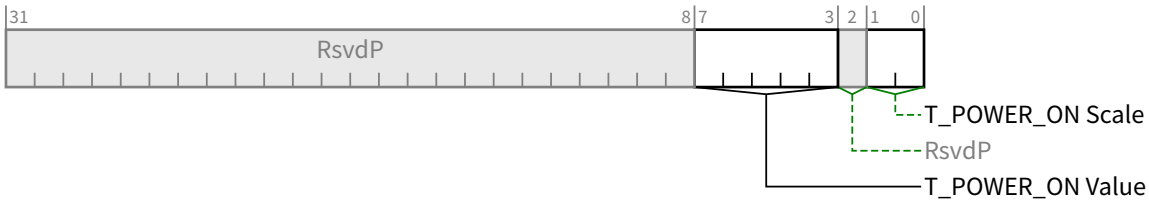

Figure 7-120 L1 PM Substates Control 2 Register

Table 7-97 L1 PM Substates Control 2 Register

Bit Location	Register Description	Attributes
1:0	***T_POWER_ON Scale*** - Specifies the scale used for T_POWER_ON Value. Range of Values: **00b** 2 µs **01b** 10 µs **10b** 100 µs **11b** Reserved Required for all Ports that support L1.2, otherwise this field is of type RsvdP. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are Set. Default value is 00b	RW/RsvdP
7:3	***T_POWER_ON Value*** - Along with the T_POWER_ON Scale sets the minimum amount of time (in µs) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON Scale field. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are Set.	RW/RsvdP

Bit Location	Register Description	Attributes
	Default value is 00101b Required for all Ports that support L1.2, otherwise this field is of type RsvdP.	

7.8.3.5 L1 PM Substates Status Register (Offset 10h)

Hardware must implement this register if the Capability Version in the L1 PM Substates Extended Capability Header is 2h or greater. This register is not present if the Capability Version is 1h.

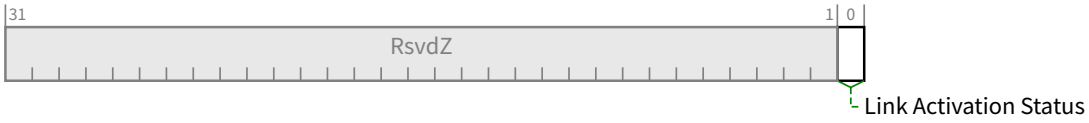

Figure 7-121 L1 PM Substates Status Register

Table 7-98 L1 PM Substates Status Register

Bit Location	Register Description	Attributes
0	***Link Activation Status*** - Indicates the status of Link Activation. See Section 5.5.6 for details. Required for Downstream Ports when the Link Activation Supported bit is Set, otherwise it is hardwired to 0b. Must be RsvdZ for Upstream Ports. Default value is 0b.	RW1C/RsvdZ

7.8.4 Advanced Error Reporting Extended Capability

The PCI Express Advanced Error Reporting Capability is an optional Extended Capability that may be implemented by PCI Express device Functions supporting advanced error control and reporting. The Advanced Error Reporting Capability structure definition has additional interpretation for Root Ports and Root Complex Event Collectors; software must interpret the Device/Port Type field in the PCI Express Capabilities register to determine the availability of additional registers for Root Ports and Root Complex Event Collectors.

Figure 7-122 shows the PCI Express Advanced Error Reporting Extended Capability structure.

Note that if an error reporting bit field is marked as optional in the error registers, the bits must be implemented or not implemented as a group across the Status, Mask and Severity registers. In other words, a Function is required to implement the same error bit fields in corresponding Status, Mask and Severity registers. Bits corresponding to bit fields that are not implemented must be hardwired to 0, unless otherwise specified.

Except for Root Ports and Root Complex Event Collectors, if the End-End TLP Prefix Supported bit is Set, the Root Error Command and Error Source Identification Registers must be RsvdP and the Root Error Status Register must be RsvdZ.

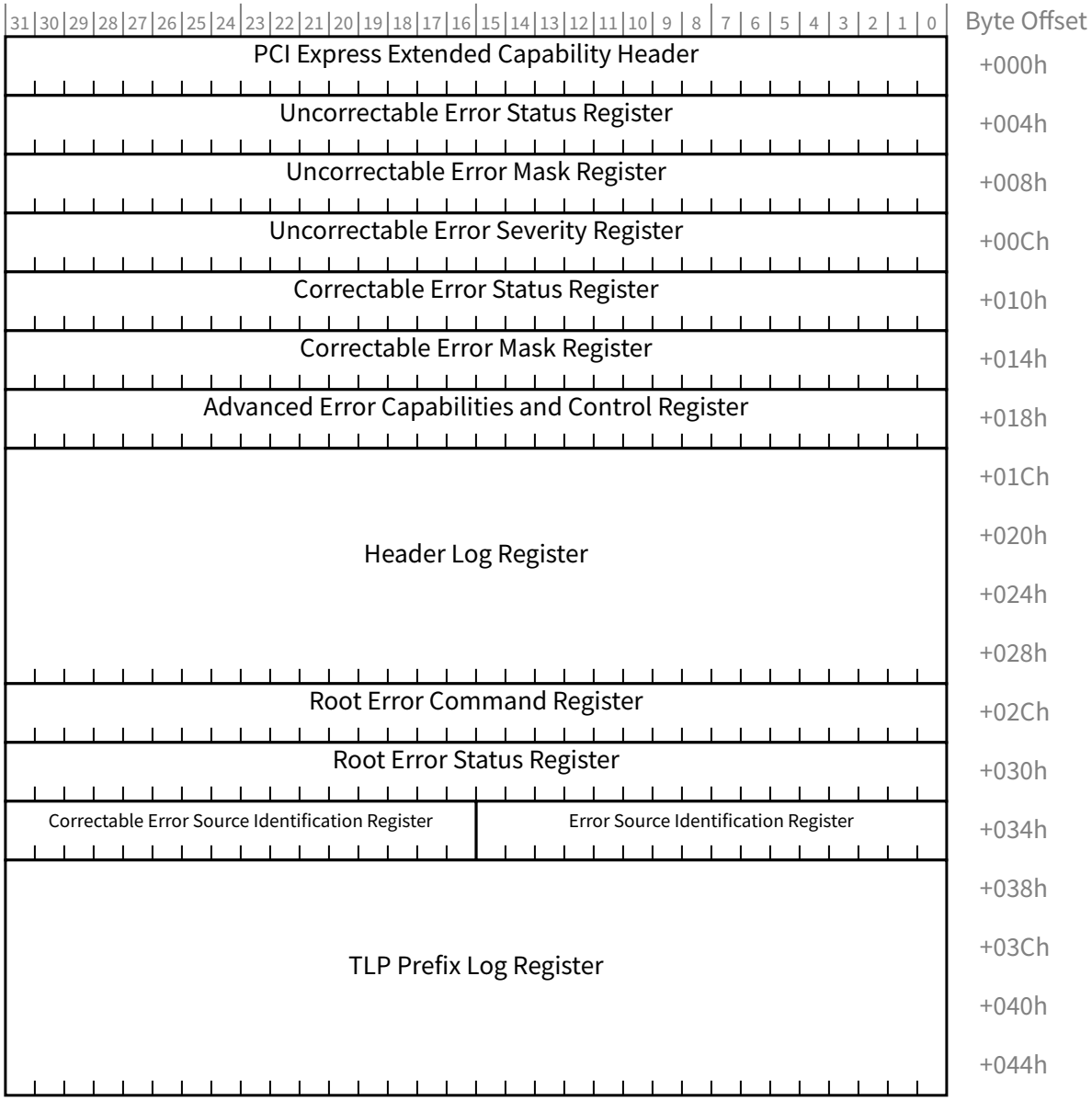

Figure 7-122 Advanced Error Reporting Extended Capability Structure

7.8.4.1 Advanced Error Reporting Extended Capability Header (Offset 00h)

Figure 7-123 details the allocation of register fields of an Advanced Error Reporting Extended Capability header; Table 7-99 provides the respective bit definitions.

Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h.

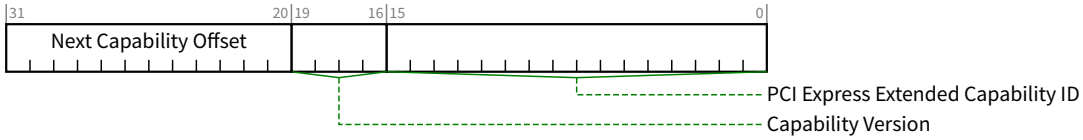

Figure 7-123 Advanced Error Reporting Extended Capability Header

Table 7-99 Advanced Error Reporting Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the End-End TLP Prefix Supported bit (see Section 7.5.3.15) is Set and must be 1h or 2h otherwise.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.8.4.2 Uncorrectable Error Status Register (Offset 04h)

The Uncorrectable Error Status Register indicates error detection status of individual errors on a PCI Express device Function. An individual error status bit that is Set indicates that a particular error was detected; software may clear an error status by writing a 1b to the respective bit. Refer to Section 6.2 for further details. Register bits not implemented by the Function are hardwired to 0b. Figure 7-124 details the allocation of register fields of the Uncorrectable Error Status Register; Section 7.8.4.2 provides the respective bit definitions.

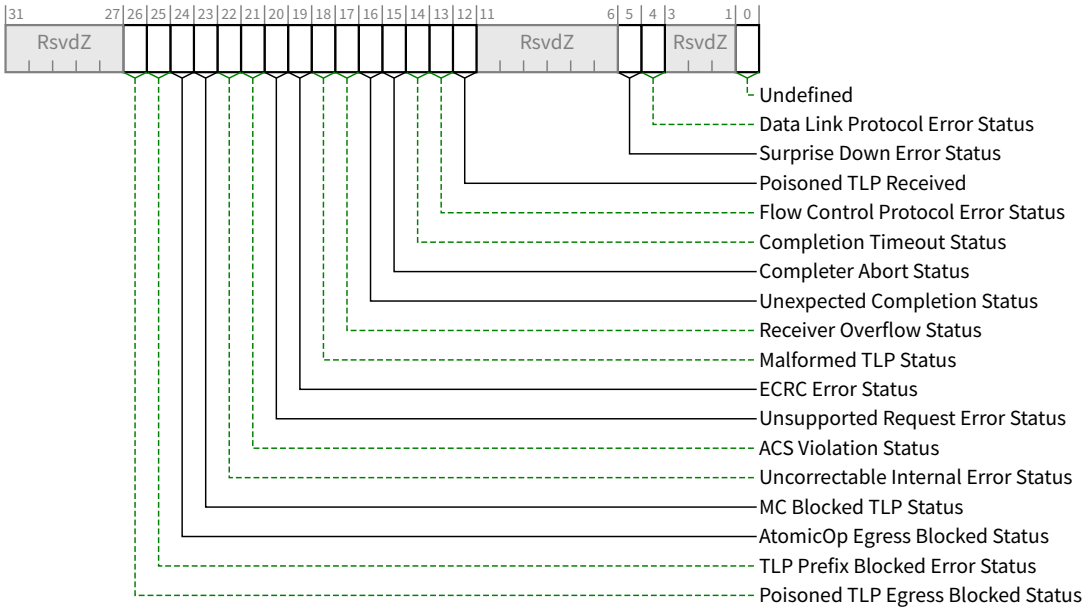

Figure 7-124 Uncorrectable Error Status Register

Table 7-100 Uncorrectable Error Status Register

Bit Location	Register Description	Attributes	Default
0	**Undefined** - The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.	Undefined	Undefined
4	***Data Link Protocol Error Status***	RW1CS	0b
5	***Surprise Down Error Status*** (Optional)	RW1CS	0b
12	***Poisoned TLP Received*** Status	RW1CS	0b
13	***Flow Control Protocol Error Status*** (Optional)	RW1CS	0b
14	***Completion Timeout Status***[150]	RW1CS	0b
15	***Completer Abort Status*** (Optional)	RW1CS	0b
16	***Unexpected Completion Status***	RW1CS	0b
17	***Receiver Overflow Status*** (Optional)	RW1CS	0b
18	***Malformed TLP Status***	RW1CS	0b
19	***ECRC Error Status*** (Optional)	RW1CS	0b
20	***Unsupported Request Error Status***	RW1CS	0b

150. For Switch Ports, required if the Switch Port issues Non-Posted Requests on its own behalf (vs. only forwarding such Requests generated by other devices). If the Switch Port does not issue such Requests, then the Completion Timeout mechanism is not applicable and this bit must be hardwired to 0b.

Bit Location	Register Description	Attributes	Default
21	***ACS Violation Status*** (Optional)	RW1CS	0b
22	***Uncorrectable Internal Error Status*** (Optional)	RW1CS	0b
23	***MC Blocked TLP Status*** (Optional)	RW1CS	0b
24	***AtomicOp Egress Blocked Status*** (Optional)	RW1CS	0b
25	***TLP Prefix Blocked Error Status*** (Optional)	RW1CS	0b
26	***Poisoned TLP Egress Blocked Status*** (Optional)	RW1CS	0b

7.8.4.3 Uncorrectable Error Mask Register (Offset 08h)

The Uncorrectable Error Mask Register controls reporting of individual errors by the device Function to the PCI Express Root Complex via a PCI Express error Message. A masked error (respective bit Set in the mask register) is not recorded or reported in the Header Log, TLP Prefix Log, or First Error Pointer, and is not reported to the PCI Express Root Complex by this Function. Refer to Section 6.2 for further details. There is a mask bit per error bit of the Uncorrectable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b. Figure 7-125 details the allocation of register fields of the Uncorrectable Error Mask Register; Table 7-101 provides the respective bit definitions.

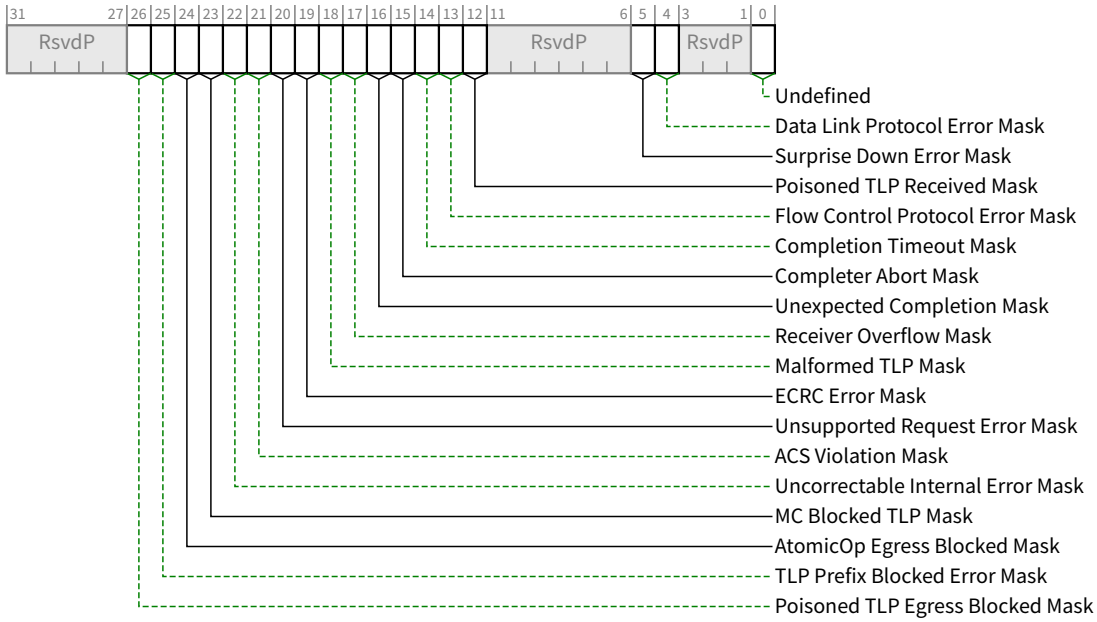

Figure 7-125 Uncorrectable Error Mask Register

Table 7-101 Uncorrectable Error Mask Register

Bit Location	Register Description	Attributes	Default
0	**Undefined** - The value read from this bit is undefined. In previous versions of this specification, this bit was used to mask a Link Training Error. System software must ignore the value read from this bit. System software must only write a value of 1b to this bit.	Undefined	Undefined
4	***Data Link Protocol Error Mask***	RWS	0b
5	***Surprise Down Error Mask*** (Optional)	RWS	0b
12	***Poisoned TLP Received Mask***	RWS	0b
13	***Flow Control Protocol Error Mask*** (Optional)	RWS	0b
14	***Completion Timeout Mask***[151]	RWS	0b
15	***Completer Abort Mask*** (Optional)	RWS	0b
16	***Unexpected Completion Mask***	RWS	0b
17	***Receiver Overflow Mask*** (Optional)	RWS	0b
18	***Malformed TLP Mask***	RWS	0b
19	***ECRC Error Mask*** (Optional)	RWS	0b
20	***Unsupported Request Error Mask***	RWS	0b
21	***ACS Violation Mask*** (Optional)	RWS	0b
22	***Uncorrectable Internal Error Mask*** (Optional)	RWS	1b
23	***MC Blocked TLP Mask*** (Optional)	RWS	0b
24	***AtomicOp Egress Blocked Mask*** (Optional)	RWS	0b
25	***TLP Prefix Blocked Error Mask*** (Optional)	RWS	0b
26	***Poisoned TLP Egress Blocked Mask*** (Optional)	RWS	1b

7.8.4.4 Uncorrectable Error Severity Register (Offset 0Ch)

The Uncorrectable Error Severity Register controls whether an individual error is reported as a Non-fatal or Fatal error. An error is reported as fatal when the corresponding error bit in the severity register is Set. If the bit is Clear, the corresponding error is considered non-fatal. Refer to Section 6.2 for further details. Register fields for bits not implemented by the Function are hardwired to an implementation specific value. Figure 7-126 details the allocation of register fields of the Uncorrectable Error Severity Register; Table 7-102 provides the respective bit definitions.

151. For Switch Ports, required if the Switch Port issues Non-Posted Requests on its own behalf (vs. only forwarding such Requests generated by other devices). If the Switch Port does not issue such Requests, then the Completion Timeout mechanism is not applicable and this bit must be hardwired to 0b.

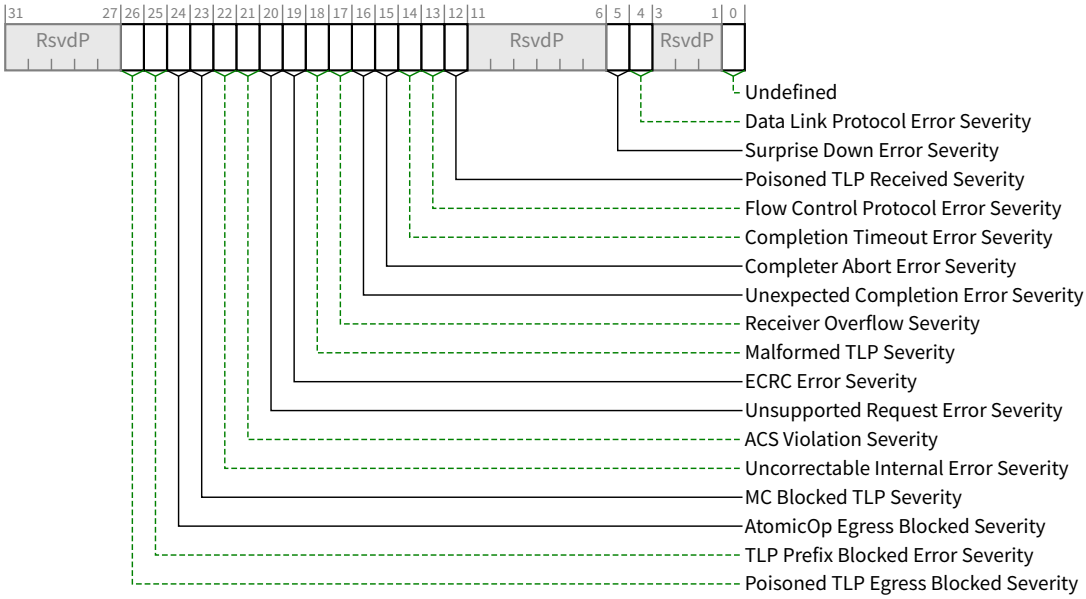

Figure 7-126 Uncorrectable Error Severity Register

Table 7-102 Uncorrectable Error Severity Register

Bit Location	Register Description	Attributes	Default
0	**Undefined** - The value read from this bit is undefined. In previous versions of this specification, this bit was used to Set the severity of a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.	Undefined	Undefined
4	***Data Link Protocol Error Severity***	RWS	1b
5	***Surprise Down Error Severity*** (Optional)	RWS	1b
12	***Poisoned TLP Received Severity***	RWS	0b
13	***Flow Control Protocol Error Severity*** (Optional)	RWS	1b
14	***Completion Timeout Error Severity***[152]	RWS	0b
15	***Completer Abort Error Severity*** (Optional)	RWS	0b
16	***Unexpected Completion Error Severity***	RWS	0b
17	***Receiver Overflow Severity*** (Optional)	RWS	1b
18	***Malformed TLP Severity***	RWS	1b
19	***ECRC Error Severity*** (Optional)	RWS	0b
20	***Unsupported Request Error Severity***	RWS	0b

152. For Switch Ports, required if the Switch Port issues Non-Posted Requests on its own behalf (vs. only forwarding such Requests generated by other devices). If the Switch Port does not issue such Requests, then the Completion Timeout mechanism is not applicable and this bit must be hardwired to 0b.

Bit Location	Register Description	Attributes	Default
21	***ACS Violation Severity*** (Optional)	RWS	0b
22	***Uncorrectable Internal Error Severity*** (Optional)	RWS	1b
23	***MC Blocked TLP Severity*** (Optional)	RWS	0b
24	***AtomicOp Egress Blocked Severity*** (Optional)	RWS	0b
25	***TLP Prefix Blocked Error Severity*** (Optional)	RWS	0b
26	***Poisoned TLP Egress Blocked Severity*** (Optional)	RWS	0b

7.8.4.5 Correctable Error Status Register (Offset 10h)

The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device Function. When an individual error status bit is Set, it indicates that a particular error occurred; software may clear an error status by writing a 1b to the respective bit. Refer to Section 6.2 for further details. Register bits not implemented by the Function are hardwired to 0b. Figure 7-127 details the allocation of register fields of the Correctable Error Status register; Table 7-103 provides the respective bit definitions.

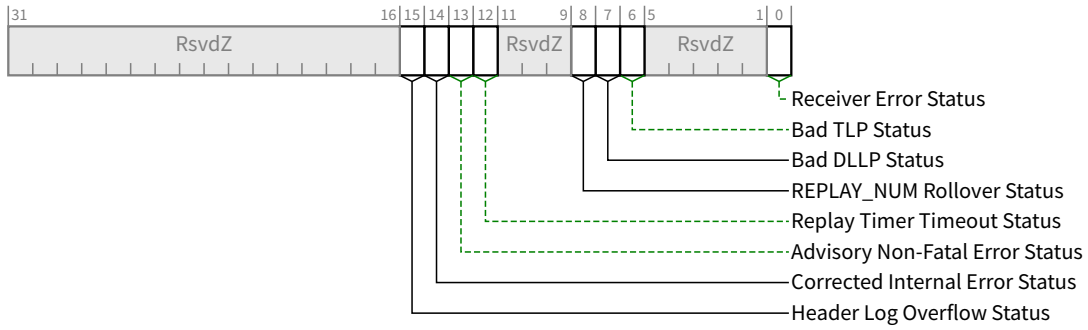

Figure 7-127 Correctable Error Status Register

Table 7-103 Correctable Error Status Register

Bit Location	Register Description	Attributes	Default
0	***Receiver Error Status***[153]	RW1CS	0b
6	***Bad TLP Status***	RW1CS	0b
7	***Bad DLLP Status***	RW1CS	0b
8	***REPLAY_NUM Rollover Status***	RW1CS	0b
12	***Replay Timer Timeout Status***	RW1CS	0b
13	***Advisory Non-Fatal Error Status***	RW1CS	0b

153. For historical reasons, implementation of this bit is optional. If not implemented, this bit must be RsvdZ, and bit 0 of the Correctable Error Mask Register must also not be implemented. Note that some checking for Receiver Errors is required in all cases (see Section 4.2.1.1.3 , Section 4.2.4.8 , and Section 4.2.6).

Bit Location	Register Description	Attributes	Default
14	***Corrected Internal Error Status*** (Optional)	RW1CS	0b
15	***Header Log Overflow Status*** (Optional)	RW1CS	0b

7.8.4.6 Correctable Error Mask Register (Offset 14h)

The Correctable Error Mask Register controls reporting of individual correctable errors by this Function to the PCI Express Root Complex via a PCI Express error Message. A masked error (respective bit Set in the mask register) is not reported to the PCI Express Root Complex by this Function. Refer to Section 6.2 for further details. There is a mask bit per error bit in the Correctable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b. Figure 7-128 details the allocation of register fields of the Correctable Error Mask Register; Table 7-104 provides the respective bit definitions.

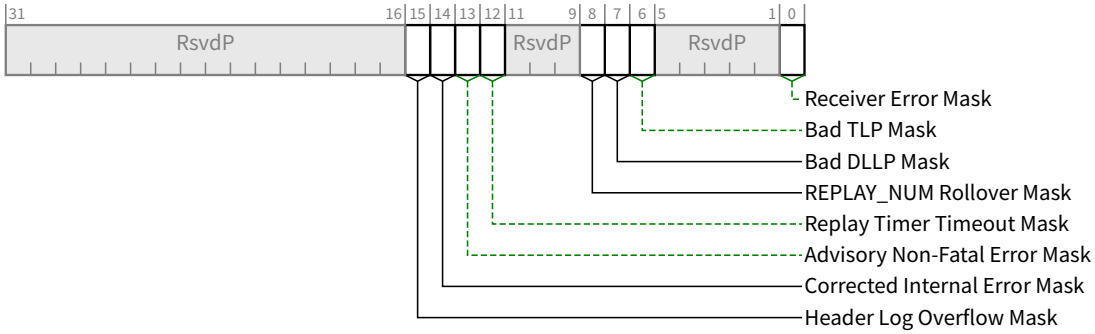

Figure 7-128 Correctable Error Mask Register

Table 7-104 Correctable Error Mask Register

Bit Location	Register Description	Attributes	Default
0	***Receiver Error Mask***[154]	RWS	0b
6	***Bad TLP Mask***	RWS	0b
7	***Bad DLLP Mask***	RWS	0b
8	***REPLAY_NUM Rollover Mask***	RWS	0b
12	***Replay Timer Timeout Mask***	RWS	0b
13	***Advisory Non-Fatal Error Mask*** - This bit is Set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.	RWS	1b
14	***Corrected Internal Error Mask*** (Optional)	RWS	1b
15	***Header Log Overflow Mask*** (Optional)	RWS	1b

154. For historical reasons, implementation of this bit is optional. If not implemented, this bit must be RsvdP, and bit 0 of the Correctable Error Status register must also not be implemented. Note that some checking for Receiver Errors is required in all cases (see Sections 4.2.1.1.3, 4.2.4.7, and 4.2.6).

7.8.4.7 Advanced Error Capabilities and Control Register (Offset 18h)

Figure 7-129 details allocation of register fields in the Advanced Error Capabilities and Control register; Table 7-105 provides the respective bit definitions. Handling of multiple errors is discussed in Section 6.2.4.2 .

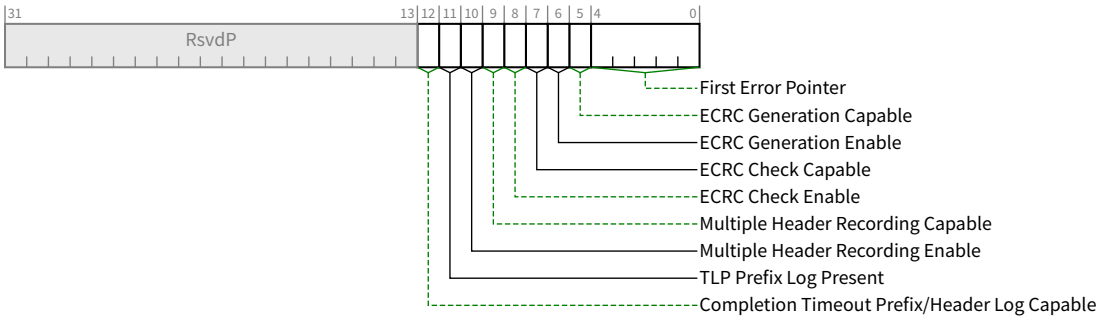

Figure 7-129 Advanced Error Capabilities and Control Register

Table 7-105 Advanced Error Capabilities and Control Register

Bit Location	Register Description	Attributes
4:0	***First Error Pointer*** - The First Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. Refer to Section 6.2 for further details.	ROS
5	***ECRC Generation Capable*** - If Set, this bit indicates that the Function is capable of generating ECRC (see Section 2.7).	RO
6	***ECRC Generation Enable*** - When Set, ECRC generation is enabled (see Section 2.7). Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RWS
7	***ECRC Check Capable*** - If Set, this bit indicates that the Function is capable of checking ECRC (see Section 2.7).	RO
8	***ECRC Check Enable*** - When Set, ECRC checking is enabled (see Section 2.7). Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RWS
9	***Multiple Header Recording Capable*** - If Set, this bit indicates that the Function is capable of recording more than one error header. Refer to Section 6.2 for further details.	RO
10	***Multiple Header Recording Enable*** - When Set, this bit enables the Function to record more than one error header. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RWS
11	***TLP Prefix Log Present*** - If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is Clear.	ROS

Bit Location	Register Description	Attributes
12	***Completion Timeout Prefix/Header Log Capable*** - If Set, this bit indicates that the Function records the prefix/header of Request TLPs that experience a Completion Timeout error.	RO

7.8.4.8 Header Log Register (Offset 1Ch)

The Header Log Register contains the header for the TLP corresponding to a detected error; refer to Section 6.2 for further details. Section 6.2 also describes the conditions where the packet header is recorded. This register is 16 bytes and adheres to the format of the headers defined throughout this specification.

The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in this document. Therefore, byte 0 of the header is located in byte 3 of the Header Log Register, byte 1 of the header is in byte 2 of the Header Log Register and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log Register are used and values in bytes 12 through 15 are undefined.

In certain cases where a Malformed TLP is reported, the Header Log Register may contain TLP Prefix information. See Section 6.2.4.4 for details.

Figure 7-130 details allocation of register fields in the Header Log Register; Table 7-106 provides the respective bit definitions.

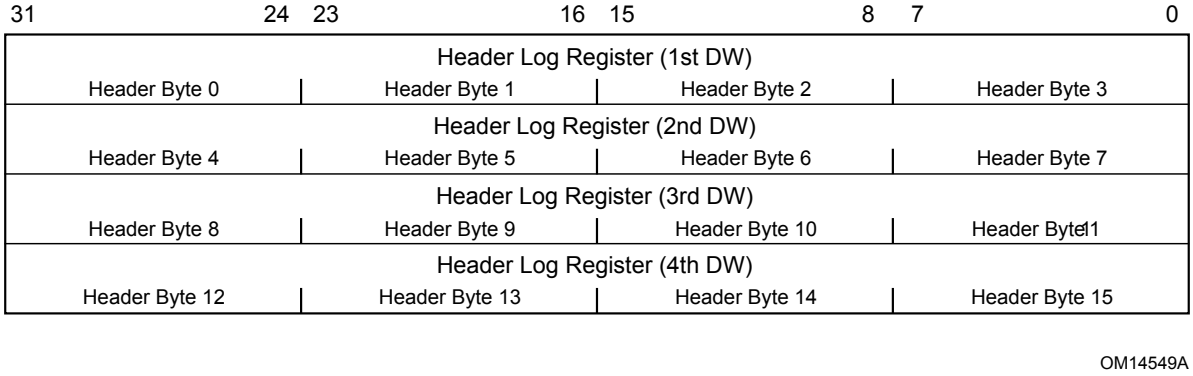

Figure 7-130 Header Log Register

Table 7-106 Header Log Register

Bit Location	Register Description	Attributes	Default
127:0	Header of TLP associated with error	ROS	0

7.8.4.9 Root Error Command Register (Offset 2Ch)

The Root Error Command Register allows further control of Root Complex response to Correctable, Non-Fatal, and Fatal error Messages than the basic Root Complex capability to generate system errors in response to error Messages (either received or internally generated). Bit fields (see Figure 7-131) enable or disable generation of interrupts (claimed by the Root Port or Root Complex Event Collector) in addition to system error Messages according to the definitions in Table 7-107 .

For both Root Ports and Root Complex Event Collectors, in order for a received error Message or an internally generated error Message to generate an interrupt enabled by this register, the error Message must be enabled for “transmission” by the Root Port or Root Complex Event Collector (see Section 6.2.4.1 and Section 6.2.8.1).

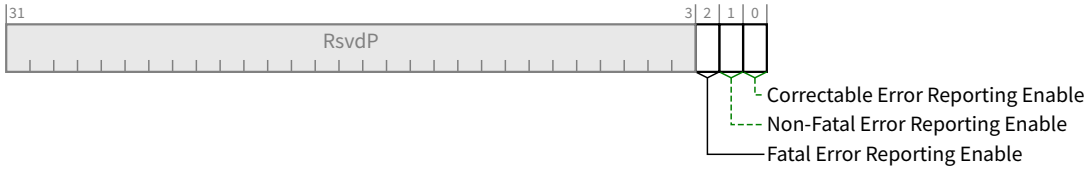

Figure 7-131 Root Error Command Register

Table 7-107 Root Error Command Register

Bit Location	Register Description	Attributes	Default
0	***Correctable Error Reporting Enable*** - When Set, this bit enables the generation of an interrupt when a correctable error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs. Refer to Section 6.2 for further details.	RW	0b
1	***Non-Fatal Error Reporting Enable*** - When Set, this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs. Refer to Section 6.2 for further details.	RW	0b
2	***Fatal Error Reporting Enable*** - When Set, this bit enables the generation of an interrupt when a Fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs. Refer to Section 6.2 for further details.	RW	0b

System error generation in response to PCI Express error Messages may be turned off by system software using the PCI Express Capability structure described in Section 7.5.3 when advanced error reporting via interrupts is enabled. Refer to Section 6.2 for further details.

7.8.4.10 Root Error Status Register (Offset 30h)

The Root Error Status Register reports status of error Messages (ERR_COR, ERR_NONFATAL, and ERR_FATAL) received by the Root Port, and of errors detected by the Root Port itself (which are treated conceptually as if the Root Port had sent an error Message to itself). In order to update this register, error Messages received by the Root Port and/or internally generated error Messages must be enabled for “transmission” by the primary interface of the Root Port. ERR_NONFATAL and ERR_FATAL Messages are grouped together as uncorrectable. Each correctable and uncorrectable (Non-fatal and Fatal) error source has a first error bit and a next error bit associated with it respectively. When an error is received by a Root Complex, the respective first error bit is Set and the Requester ID is logged in the Error Source Identification

Register. A Set individual error status bit indicates that a particular error category occurred; software may clear an error status by writing a 1b to the respective bit. If software does not clear the first reported error before another error Message is received of the same category (correctable or uncorrectable), the corresponding next error status bit will be set but the Requester ID of the subsequent error Message is discarded. The next error status bits may be cleared by software by writing a 1b to the respective bit as well. Refer to Section 6.2 for further details. This register is updated regardless of the settings of the Root Control register and the Root Error Command Register. Figure 7-132 details allocation of register fields in the Root Error Status Register; Table 7-108 provides the respective bit definitions. Root Complex Event Collectors provide support for the above-described functionality for RCiEPs (and for the Root Complex Event Collector itself). In order to update this register, error Messages received by the Root Complex Event Collector from its associated RCiEPs and/or internally generated error Messages must be enabled for “transmission” by the Root Complex Event Collector.

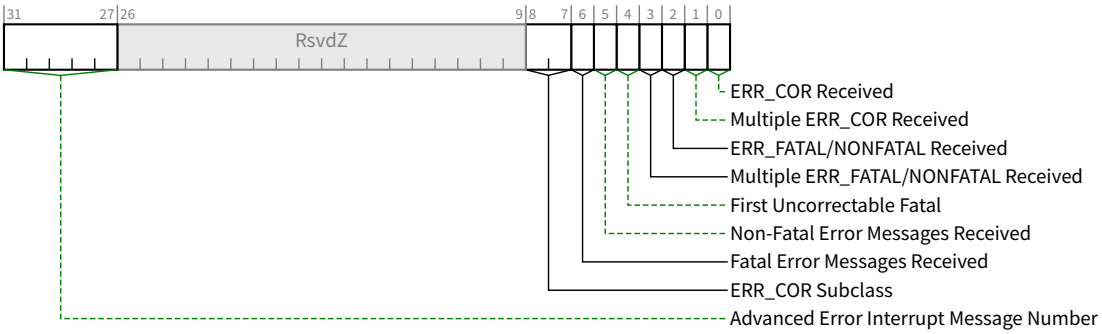

Figure 7-132 Root Error Status Register

Table 7-108 Root Error Status Register

Bit Location	Register Description	Attributes
0	***ERR_COR Received*** - Set when a Correctable error Message is received and this bit is not already Set. Default value of this bit is 0b.	RW1CS
1	***Multiple ERR_COR Received*** - Set when a Correctable error Message is received and ERR_COR Received is already Set. Default value of this bit is 0b.	RW1CS
2	***ERR_FATAL/NONFATAL Received*** - Set when either a Fatal or a Non-fatal error Message is received and this bit is not already Set. Default value of this bit is 0b.	RW1CS
3	***Multiple ERR_FATAL/NONFATAL Received*** - Set when either a Fatal or a Non-fatal error is received and ERR_FATAL/NONFATAL Received is already Set. Default value of this bit is 0b.	RW1CS
4	***First Uncorrectable Fatal*** - Set when the first Uncorrectable error Message received is for a Fatal error. Default value of this field is 0b.	RW1CS
5	***Non-Fatal Error Messages Received*** - Set when one or more Non-Fatal Uncorrectable error Messages have been received. Default value of this bit is 0b.	RW1CS

Bit Location	Register Description	Attributes
6	***Fatal Error Messages Received*** - Set when one or more Fatal Uncorrectable error Messages have been received. Default value of this bit is 0b.	RW1CS
8:7	***ERR_COR Subclass*** - If the Function is ERR_COR Subclass capable and the ERR_COR Received bit is not already Set, this field is loaded with the value of the ERR_COR Subclass field in the received ERR_COR Message. See Section 2.2.8.3 . The value in this field is only valid when the ERR_COR Received bit is Set. If the Function is not ERR_COR Subclass capable, this field is Reserved. If the Function is ERR_COR Subclass capable and a SIG_SFW ERR_COR Message is received, system firmware should be signaled using a system-specific mechanism. Default value of this field is 00b.	ROS/RsvdZ
31:27	***Advanced Error Interrupt Message Number*** - This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability. For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the Message Control Register for MSI. For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined.	RO

7.8.4.11 Error Source Identification Register (Offset 34h)

The Error Source Identification Register identifies the source (Requester ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status Register. Refer to Section 6.2 for further details. This register is updated regardless of the settings of the Root Control register and the Root Error Command Register. Figure 7-133 details allocation of register fields in the Error Source Identification Register; Table 7-109 provides the respective bit definitions.

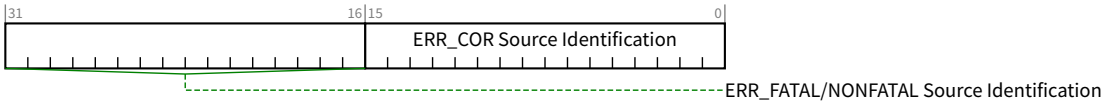

Figure 7-133 Error Source Identification Register

Table 7-109 Error Source Identification Register

Bit Location	Register Description	Attributes
15:0	***ERR_COR Source Identification*** - Loaded with the Requester ID indicated in the received ERR_COR Message when the ERR_COR Received bit is not already set.	ROS

Bit Location	Register Description	Attributes
	Default value of this field is 0000h.	
31:16	***ERR_FATAL/NONFATAL Source Identification*** - Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received bit is not already set. Default value of this field is 0000h.	ROS

7.8.4.12 TLP Prefix Log Register (Offset 38h)

The TLP Prefix Log Register captures the End-End TLP Prefix(s) for the TLP corresponding to the detected error; refer to Section 6.2 for further details. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set (see Section 7.8.4.7).

The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described. Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth.

The First TLP Prefix Log Register contains the first End-End TLP Prefix from the TLP (see Section 6.2.4.4). The Second TLP Prefix Log Register contains the second End-End TLP Prefix and so forth. If the TLP contains fewer than four End-End TLP Prefixes, the remaining TLP Prefix Log Registers contain zero. A TLP that contains more End-End TLP Prefixes than are indicated by the Function's Max End-End TLP Prefixes field must be handled as an error (see Section 2.2.10.2 for specifics). To allow software to detect this condition, the supported number of End-End TLP Prefixes are logged in this register, the first overflow End-End TLP Prefix is logged in the first DW of the Header Log register and the remaining DWs of the Header Log register are undefined (see Section 6.2.4.4).

The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero. For example, if a Functions, Max End-End TLP Prefixes field contains 10b (indicating 2 DW of buffering) then the third and fourth TLP Prefix Log Registers are hardwired to zero. If the End-End TLP Prefix Supported bit (Section 7.5.3.15) is Clear, the TLP Prefix Log Register is not required to be implemented.

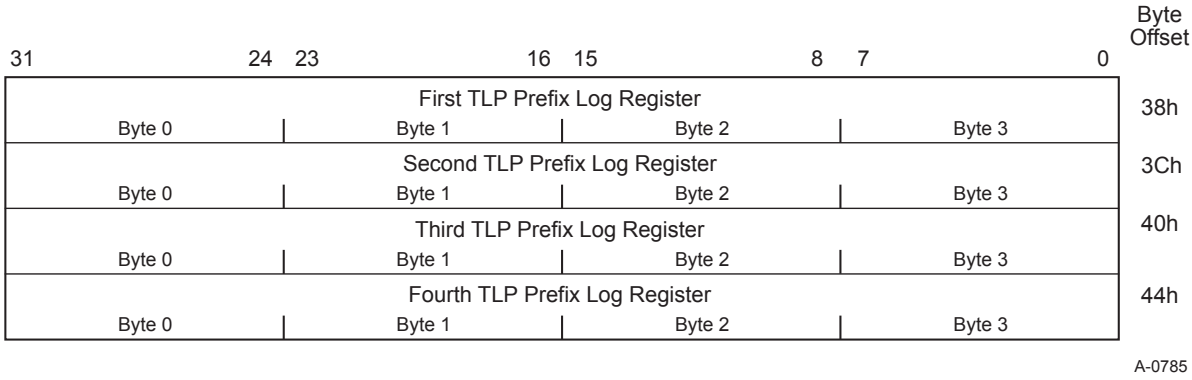

Figure 7-134 TLP Prefix Log Register

Table 7-110 TLP Prefix Log Register

Bit Location	Register Description	Attributes	Default
127:0	TLP Prefix Log	ROS	0

7.8.5 *Enhanced Allocation Capability* Structure (EA)

Each function that supports the Enhanced Allocation mechanism must implement the Enhanced Allocation capability structure.

Each field is defined in the following sections. Reserved registers must return 0 when read and write operations must have no effect. Read-only registers return valid data when read, and write operations must have no effect.

7.8.5.1 Enhanced Allocation Capability First DW (Offset 00h)

The first DW of the Enhanced Allocation capability is illustrated in Figure 7-135 , and is documented in Table 7-111 .

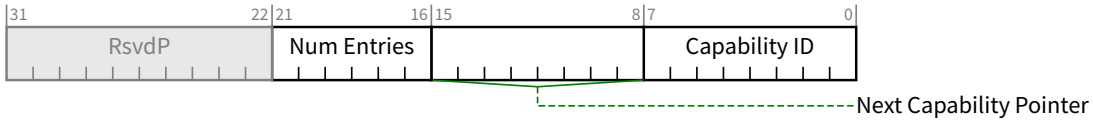

Figure 7-135 First DW of Enhanced Allocation Capability

Table 7-111 First DW of Enhanced Allocation Capability

Bit Location	Register Description	Attributes
7:0	***Capability ID*** - Must be set to 14h to indicate Enhanced Allocation capability. This field is read only.	HwInit
15:8	***Next Capability Pointer*** - Pointer to the next item in the capabilities list. Must be NULL for the final item in the list. This field is read only.	HwInit
21:16	***Num Entries*** - Number of entries following the first DW of the capability. Value of 00 0000b is permitted and means there are no entries. This field is read only.	HwInit

7.8.5.2 Enhanced Allocation Capability Second DW (Offset 04h) [Type 1 Functions Only]

For Type 1 Functions only, there is a second DW in the capability, preceding the first entry. This second DW must be included in the Enhanced Allocation Capability whenever this capability is implemented in a Type 1 Function. The second DW of the Enhanced Allocation capability is illustrated in Figure 7-136 , and is documented in Table 7-112 .

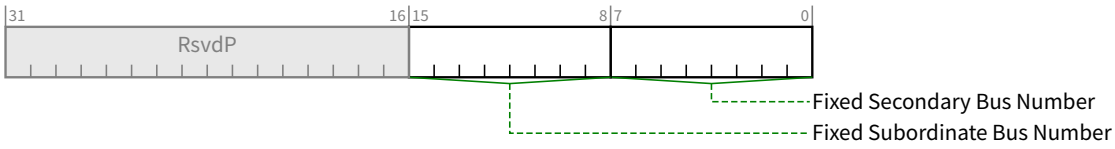

Figure 7-136 Second DW of Enhanced Allocation Capability

Table 7-112 Second DW of Enhanced Allocation Capability

Bit Location	Register Description	Attributes
7:0	***Fixed Secondary Bus Number*** - If at least one Function that uses EA is located behind this Function, then this field must be set to indicate the Bus Number for the secondary interface of this Function. If no Function that uses EA is located behind this Function, then this field must be set to 00h.	HwInit
15:8	***Fixed Subordinate Bus Number*** - If at least one Function that uses EA is located behind this Function, then this field must be set to indicate the the highest Bus Number below this Function. If no Function that uses-EA is located behind this Function, then this field must be set to 00h.	HwInit

7.8.5.3 Enhanced Allocation Per-Entry Format (Offset 04h or 08h)

An Enhanced Allocation Entry consists of a First DW followed by between 2 and 4 DW of Base / MaxOffset information.

- For Type 0 Functions, Enhanced Allocation Entries start at offset 04h of this capability.
- For Type 1 Functions, Enhanced Allocation Entries start at offset 08h of this capability.
- Subsequent Enhanced Allocation Entries immediately follow each other.

The first DW of each entry in the Enhanced Allocation capability is illustrated in Figure 7-137 , and is defined in Table 7-113 .

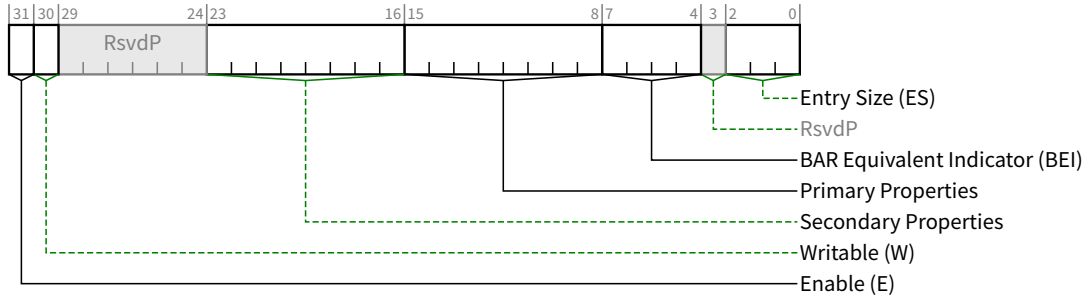

Figure 7-137 First DW of Each Entry for Enhanced Allocation Capability

Table 7-113 First DW of Each Entry for Enhanced Allocation Capability

<table>
<tr><th>Bit Location</th><th>Register Description</th><th>Attributes</th></tr>
<tr><td>2:0</td><td>Entry Size (ES) - Number of DW following the initial DW in this entry.
When processing this capability, software is required to use the value in this field to determine the size of this entry, and if this entry is not the final entry, the start of the following entry in the capability. This requirement must be strictly followed by software, even if the indicated entry size does not correspond to any entry defined in this specification.
Value of 000b indicates only the first DW (containing the Entry Size field) is included in the entry.</td><td>HwInit</td></tr>
<tr><td>7:4</td><td>BAR Equivalent Indicator (BEI) - This field indicates the equivalent BAR for this entry.
Specific rules for use of this field are given in the text following this table.
<table>
<tr><th>BEI Value</th><th>Description</th></tr>
<tr><td>0</td><td>Entry is equivalent to BAR at location 10h</td></tr>
<tr><td>1</td><td>Entry is equivalent to BAR at location 14h</td></tr>
<tr><td>2</td><td>Entry is equivalent to BAR at location 18h</td></tr>
<tr><td>3</td><td>Entry is equivalent to BAR at location 1Ch</td></tr>
<tr><td>4</td><td>Entry is equivalent to BAR at location 20h</td></tr>
<tr><td>5</td><td>Entry is equivalent to BAR at location 24h</td></tr>
<tr><td>6</td><td>Permitted to be used by a Function with a Type 1 Configuration Space Header only, optionally used to indicate a resource that is located behind the Function</td></tr>
<tr><td>7</td><td>Equivalent Not Indicated</td></tr>
<tr><td>8</td><td>Expansion ROM Base Address</td></tr>
<tr><td>9-14</td><td>Entry relates to VF BARs 0-5 respectively</td></tr>
<tr><td>15</td><td>Reserved - Software must treat values in this range as “Equivalent Not Indicated”</td></tr>
</table></td><td>HwInit</td></tr>
<tr><td>15:8</td><td>Primary Properties - Indicates the entry properties as defined in Table 7-114 .</td><td>HwInit</td></tr>
<tr><td>23:16</td><td>Secondary Properties - Optionally used to indicate a different but compatible entry property, using properties as defined in Table 7-114 .</td><td>HwInit</td></tr>
<tr><td>30</td><td>Writable (W) - The value 1b indicates that the Base and MaxOffset fields for this entry are RW and that the Field Size bits for this entry are either RW or HwInit. The value 0b indicates those fields are HwInit.
See Table 7-114 for additional requirements on the value of this field.</td><td>HwInit</td></tr>
<tr><td>31</td><td>Enable (E) - 1b indicates this entry is enabled, 0b indicates this entry is disabled.
If system software disables this entry, the resource indicated must still be associated with this function, and it is not permitted to reallocate this resource to any other entity.
This field is permitted to be implemented as HwInit for functions that require the allocation of the associated resource, or as RW for functions that can allow system software to disable this resource, for example if BAR mechanisms are to be used instead of this resource.</td><td>RW/HwInit</td></tr>
</table>

Rules for use of BEI field:

- A Type 0 Function is permitted to use EA to allocate resources for itself, and such resources must indicate a BEI value of 0-5, 7 or 8.
- A Physical Function (Type 0 Function that supports SR-IOV) is permitted to use EA to allocate resources for its associated Virtual Functions, and such resources must indicate a BEI value of 9-14.
- A Type 1 Function (bridge) is permitted to use EA to allocate resources for itself, and such resources must indicate a BEI value of 0, 1 or 7.
- A Type 1 Function is permitted but not required to indicate resources mapped behind that Function, but if such resources are indicated by the Type 1 Function, the entry must indicate a BEI value of 6.
- For a 64-bit Base Address Register, the BEI indicates the equivalent BAR location for lower DWORD.
- For Memory BARs where the Primary or Secondary Properties is 00h or 01h, it is permitted to assign the same BEI in the range of 0 to 5 once for a range where Base + MaxOffset is below 4 GB, and again for a range where Base + MaxOffset is greater than 4 GB; It is not otherwise permitted to assign the same BEI in the range 0 to 5 for more than one entry.
- For Virtual Function BARs where the Primary or Secondary Properties is 03h or 04h it is permitted to assign the same BEI in the range of 9 to 14 once for a range where Base + MaxOffset is below 4 GB, and again for a range where Base + MaxOffset is greater than 4 GB; It is not otherwise permitted to assign the same BEI in the range 9 to 14 for more than one VF entry.
- For all cases where two entries with the same BEI are permitted, Software must enable use of only one of the two ranges at a time for a given Function.
- It is permitted for an arbitrary number of entries to assign a BEI of 6 or 7.
- At most one entry is permitted with a BEI of 8; if such an entry is present, behavior of the Expansion ROM Base Address Register is changed (see Section 7.5.1.2.4).
- For Type 1 Functions, BEI values 2 through 5 are reserved.

Figure 7-138 illustrates the format of a complete Enhanced Allocation entry for a Type 0 Function. For the Base and MaxOffset fields, bit 1 indicates if the field is a 32b (0) or 64b (1) field.

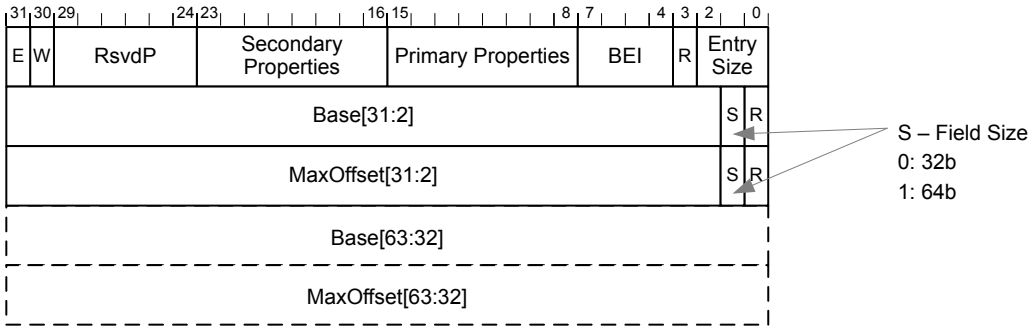

Figure 7-138 Format of Entry for Enhanced Allocation Capability

The value in the ***Base*** field ([63:2] or [31:2]) indicates the DW address of the start of the resource range. Bits [1:0] of the address are not included in the Base field, and must always be interpreted as 00b.

The value in the Base field plus the value in the ***MaxOffset*** field ([63:2] or [31:2]) indicates the address of the last included DW of the resource range. Bits [1:0] of the MaxOffset are not included in the MaxOffset field, and must always be interpreted as 11b.

For the Base and MaxOffset fields, when bits [63:32] are not provided then those bits must be interpreted as all 0's.

Although it is permitted for a Type 0 Function to indicate the use of a range that is not naturally aligned and/or not a power of two in size, some system software may fail if this is done. Particularly for ranges that are mapped to legacy BARs by indicating a BEI in the range of 0 to 5, it is strongly recommended that the Base and MaxOffset fields for a Type 0 Function indicate a naturally aligned region.

The Primary Properties[7:0] field must be set by hardware to identify the type of resource indicated by the entry. It is strongly recommended that hardware set the Secondary Properties[7:0] to indicate an alternate resource type which can be used by software when the Primary Properties[7:0] field value is not comprehended by that software, for example when older system software is used with new hardware that implements resources using a value for Primary Properties that was reserved at the time the older system software was implemented. When this is done, hardware must ensure that software operating using the resource according to the value indicated in the Secondary Properties field will operate in a functionally correct way, although it is not required that this operation will result in optimal system performance or behavior.

The Primary Properties[7:0] and Secondary Properties[7:0] fields are defined in Table 7-114 . This table also defines whether or not the entry is permitted to be writeable. The Writeable bit in any entry must be 0b unless both the Primary and Secondary properties of that entry allow otherwise.

Table 7-114 Enhanced Allocation Entry Field Value Definitions for both the Primary Properties and Secondary Properties Fields

Value (h)	Resource Definition	Writeable permitted
00	Memory Space, Non-Prefetchable.	No
01	Memory Space, Prefetchable.	No
02	I/O Space.	No
03	For use only by Physical Functions to indicate resources for Virtual Function use, Memory Space, Prefetchable.	No
04	For use only by Physical Functions to indicate resources for Virtual Function use, Memory Space, Non-Prefetchable.	No
05	For use only by Type 1 Functions to indicate Memory, Non-Prefetchable, for Allocation Behind that Bridge.	No
06	For use only by Type 1 Functions to indicate Memory, Prefetchable, for Allocation Behind that Bridge.	No
07	For use only by Type 1 Functions to indicate I/O Space for Allocation Behind that Bridge.	No
08-FC	Reserved for future use; System firmware/software must not write to this entry, and must not attempt to interpret this entry or to use this resource. When software reads a Primary Properties value that is within this range, is it strongly recommended that software treat this resource according to the value in the Secondary Properties field, if that field contains a non-reserved value.	Yes
FD	Memory Space Resource Unavailable For Use - - System firmware/software must not write to this entry, and must not attempt to use the resource described by this entry for any purpose.	No

Value (h)	Resource Definition	Writeable permitted
FE	I/O Space Resource Unavailable For Use - - System firmware/software must not write to this entry, and must not attempt to use the resource described by this entry for any purpose.	No
FF	Entry Unavailable For Use - System firmware/software must not write to this entry, and must not attempt to interpret this entry as indicating any resource. It is strongly recommended that hardware use this value in the Secondary Properties field to indicate that for proper operation, the hardware requires the use of the resource definition indicated in the Primary Properties field .	No

The following figures illustrate the layout of Enhanced Allocation entries for various cases.

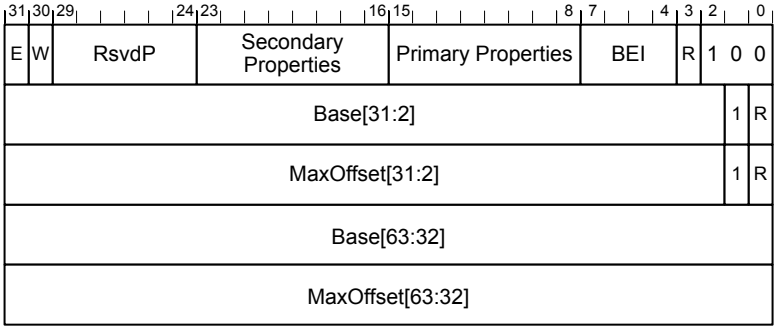

Figure 7-139 Example Entry with 64b Base and 64b MaxOffset

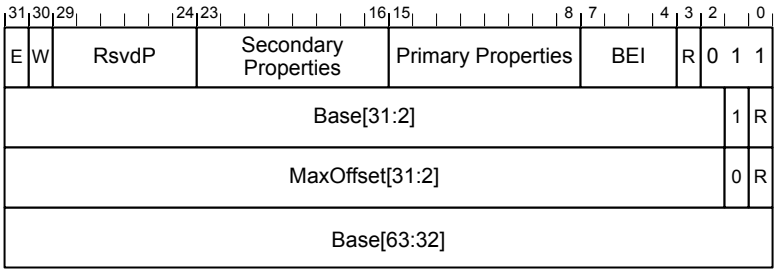

Figure 7-140 Example Entry with 64b Base and 32b MaxOffset

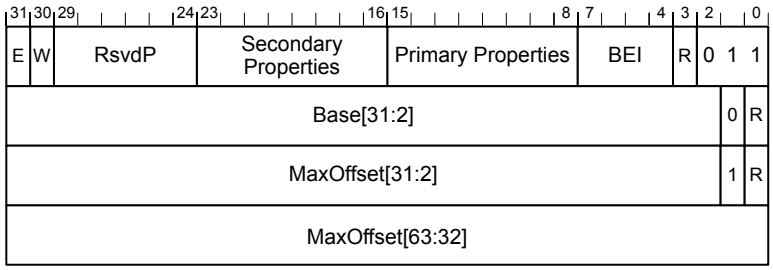

Figure 7-141 Example Entry with 32b Base and 64b MaxOffset

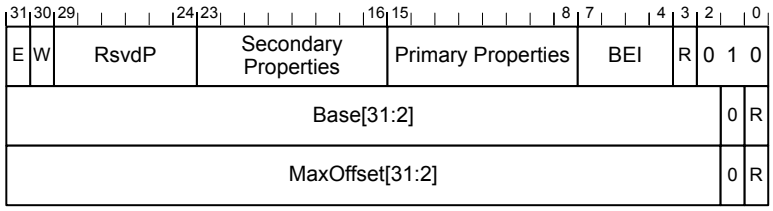

Figure 7-142 Example Entry with 32b Base and 32b MaxOffset

7.8.6 *Resizable BAR Extended Capability*

The Resizable BAR Extended Capability is an optional capability that allows hardware to communicate resource sizes, and system software, after determining the optimal size, to communicate this optimal size back to the hardware. Hardware communicates the resource sizes that are acceptable for operation via the Resizable BAR Capability and Control registers. Hardware must support at least one size in the range from 1 MB to 512 GB.

IMPLEMENTATION NOTE
Resizable BAR Backward Compatibility With Software

The Resizable BAR Extended Capability initially supported 20 sizes, ranging from 1 MB to 512 GB, and was later expanded with 16 larger sizes. The hardware requirement to support at least one of the initial sizes ensures backward compatibility with software that comprehends only the initial sizes.

Software determines, through a proprietary mechanism, what the optimal size is for the resource, and programs that size via the BAR Size field of the Resizable BAR Control register. Hardware immediately reflects the size inference in the read-only bits of the appropriate Base Address register. Hardware must Clear any bits that change from RW to read-only, so that subsequent reads return zero. Software must clear the Memory Space Enable bit in the Command register before

writing the BAR Size field. After writing the BAR Size field, the contents of the corresponding BAR are undefined. To ensure that it contains a valid address after resizing the BAR, system software must reprogram the BAR, and Set the Memory Space Enable bit (unless the resource is not allocated).

The Resizable BAR Capability and Control registers are permitted to indicate the ability to operate at 4 GB or greater only if the associated BAR is a 64-bit BAR.

This capability is applicable to Functions that have Base Address registers only. It is strongly recommended that a Function not advertise any supported BAR sizes that are larger than the space it would effectively utilize if allocated.

IMPLEMENTATION NOTE

Using the Capability During Resource Allocation

System software that allocates resources can use this capability to resize the resources inferred by the Function's BAR's read-only bits. Previous versions of this software determined the resource size by writing FFFFh to the BAR, reading back the value, and determining the size by the number of bits that are Set. Following this, the base address is written to the BAR.

System software uses this capability in place of the above mentioned method of determining the resource size, and prior to assigning the base address to the BAR. Potential usable resource sizes are reported by the Function via its Resizable BAR Capability and Control registers. It is intended that the software allocate the largest of the reported sizes that it can, since allocating less address space than the largest reported size can result in lower performance. Software then writes the size to the Resizable BAR Control register for the appropriate BAR for the Function. Following this, the base address is written to the BAR.

For interoperability reasons, it is possible that hardware will set the default size of the BAR to a low size; that is, a size lower than the largest reported in the Resizable BAR Capability and Control registers. Software that does not use this capability to size resources will likely result in sub-optimal resource allocation, where the resources are smaller than desirable, or not allocatable because there is no room for them.

With the Resizable BAR capability, the amount of address space consumed by a device can change. In a resource constrained environment, the allocation of more address space to a device may result in allocation of less of the address space to other memory-mapped hardware, like system RAM. System software responsible for allocating resources in this kind of environment is recommended to distribute the limited address space appropriately.

The Resizable BAR Capability structure defines a PCI Express Extended Capability, which is located in PCI Express Extended Configuration Space, that is, above the first 256 bytes, and is shown below in Figure 7-143 . This structure allows devices with this capability to be identified and controlled. A Capability and a Control register is implemented for each BAR that is resizable. Since a maximum of six BARs may be implemented by any Function, the Resizable BAR Capability structure can range from 12 bytes long (for a single BAR) to 52 bytes long (for all six BARs).

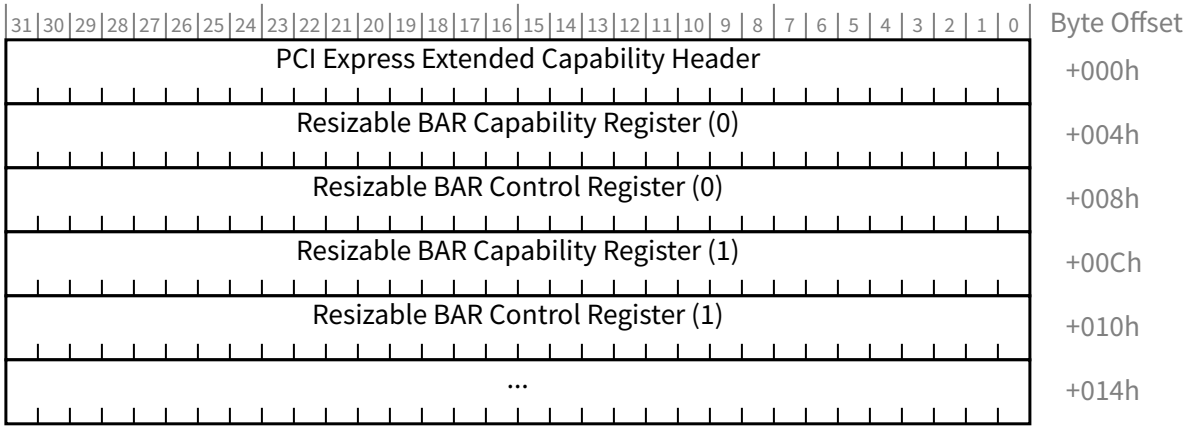

Figure 7-143 Resizable BAR Extended Capability

7.8.6.1 Resizable BAR Extended Capability Header (Offset 00h)

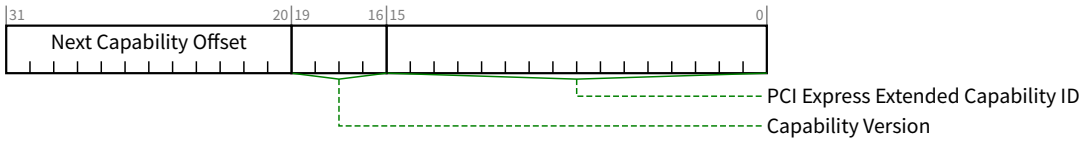

Figure 7-144 Resizable BAR Extended Capability Header

Table 7-115 Resizable BAR Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. The PCI Express Extended Capability ID for the Resizable BAR Capability is 0015h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.8.6.2 Resizable BAR Capability Register

For backward compatibility with software, hardware must Set at least one bit in the range from 4 to 23. See the associated Implementation Note in Section 7.8.6 .

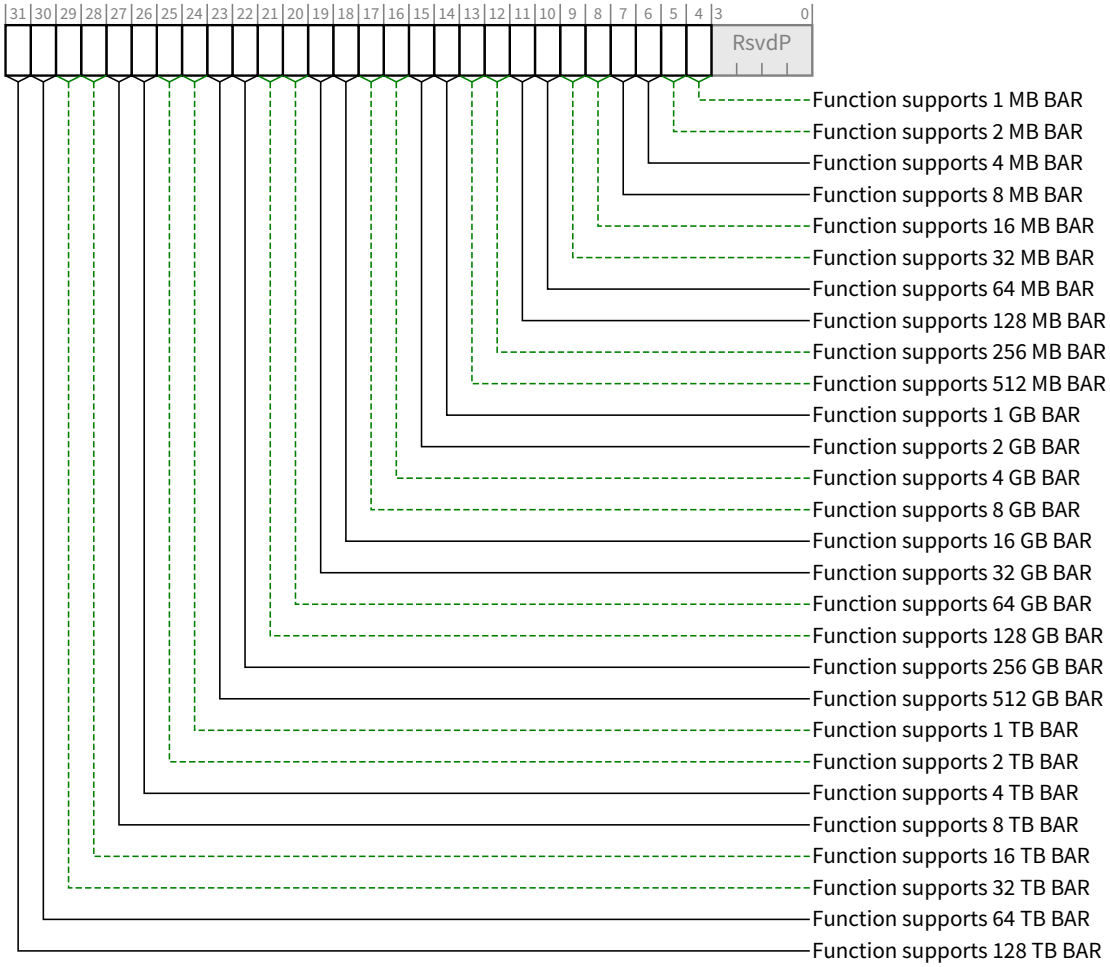

Figure 7-145 Resizable BAR Capability Register

Table 7-116 Resizable BAR Capability Register

Bit Location	Register Description	Attributes
4	***Function supports 1 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 1 MB (2^{20} bytes)	RO
5	***Function supports 2 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 2 MB (2^{21} bytes)	RO
6	***Function supports 4 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 4 MB (2^{22} bytes)	RO
7	***Function supports 8 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 8 MB (2^{23} bytes)	RO
8	***Function supports 16 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 16 MB (2^{24} bytes)	RO

Bit Location	Register Description	Attributes
9	***Function supports 32 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 32 MB (2^{25} bytes)	RO
10	***Function supports 64 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 64 MB (2^{26} bytes)	RO
11	***Function supports 128 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 128 MB (2^{27} bytes)	RO
12	***Function supports 256 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 256 MB (2^{28} bytes)	RO
13	***Function supports 512 MB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 512 MB (2^{29} bytes)	RO
14	***Function supports 1 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 1 GB (2^{30} bytes)	RO
15	***Function supports 2 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 2 GB (2^{31} bytes)	RO
16	***Function supports 4 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 4 GB (2^{32} bytes)	RO
17	***Function supports 8 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 8 GB (2^{33} bytes)	RO
18	***Function supports 16 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 16 GB (2^{34} bytes)	RO
19	***Function supports 32 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 32 GB (2^{35} bytes)	RO
20	***Function supports 64 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 64 GB (2^{36} bytes)	RO
21	***Function supports 128 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 128 GB (2^{37} bytes)	RO
22	***Function supports 256 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 256 GB (2^{38} bytes)	RO
23	***Function supports 512 GB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 512 GB (2^{39} bytes)	RO
24	***Function supports 1 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 1 TB (2^{40} bytes)	RO
25	***Function supports 2 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 2 TB (2^{41} bytes)	RO
26	***Function supports 4 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 4 TB (2^{42} bytes)	RO

Bit Location	Register Description	Attributes
27	***Function supports 8 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 8 TB (2^{43} bytes)	RO
28	***Function supports 16 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 16 TB (2^{44} bytes)	RO
29	***Function supports 32 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 32 TB (2^{45} bytes)	RO
30	***Function supports 64 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 64 TB (2^{46} bytes)	RO
31	***Function supports 128 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 128 TB (2^{47} bytes)	RO

7.8.6.3 Resizable BAR Control Register

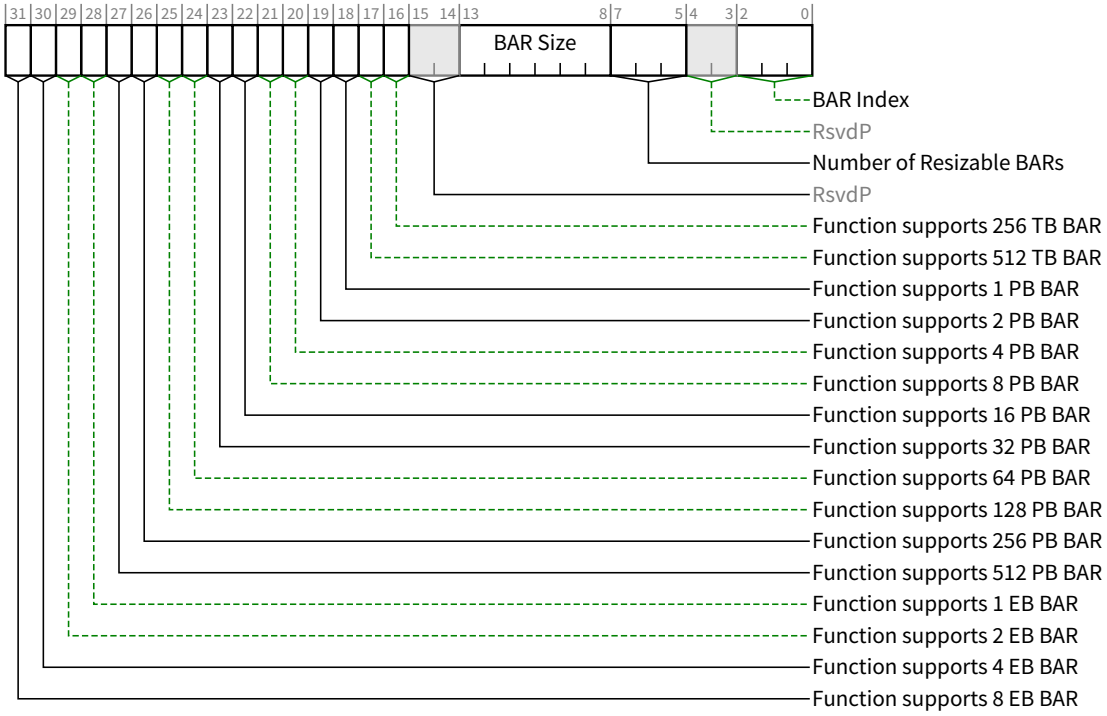

Figure 7-146 Resizable BAR Control Register

Table 7-117 Resizable BAR Control Register

Bit Location	Register Description	Attributes
2:0	***BAR Index*** - This encoded value points to the beginning of the BAR. **0** BAR located at offset 10h	RO

Bit Location	Register Description	Attributes
	1 BAR located at offset 14h **2** BAR located at offset 18h **3** BAR located at offset 1Ch **4** BAR located at offset 20h **5** BAR located at offset 24h **Others** All other encodings are Reserved. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size.	
7:5	***Number of Resizable BARs*** - Indicates the total number of resizable BARs in the capability structure for the Function. See Figure 7-143 . The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR Control register (0) (at offset 008h), and is RsvdP for all others.	RO/RsvdP
13:8	***BAR Size*** - This is an encoded value. **0** 1 MB (2^{20} bytes) **1** 2 MB (2^{21} bytes) **2** 4 MB (2^{22} bytes) **3** 8 MB (2^{23} bytes) … **43** 8 EB (2^{63} bytes) The default value of this field is equal to the default size of the address space that the BAR resource is requesting via the BAR's read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19. When this register field is programmed, the value is immediately reflected in the size of the resource, as encoded in the number of read-only bits in the BAR. Software must only write values that correspond to those indicated as supported in the Resizable BAR Capability and Control registers. Writing an unsupported value will produce undefined results. BAR Size bits that never need to be Set in order to indicate every supported size are permitted to be hardwired to 0.	RW
16	***Function supports 256 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 256 TB (2^{48} bytes)	RO
17	***Function supports 512 TB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 512 TB (2^{49} bytes)	RO
18	***Function supports 1 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 1 PB (2^{50} bytes)	RO
19	***Function supports 2 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 2 PB (2^{51} bytes)	RO
20	***Function supports 4 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 4 PB (2^{52} bytes)	RO

Bit Location	Register Description	Attributes
21	***Function supports 8 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 8 PB (2^{53} bytes)	RO
22	***Function supports 16 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 16 PB (2^{54} bytes)	RO
23	***Function supports 32 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 32 PB (2^{55} bytes)	RO
24	***Function supports 64 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 64 PB (2^{56} bytes)	RO
25	***Function supports 128 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 128 PB (2^{57} bytes)	RO
26	***Function supports 256 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 256 PB (2^{58} bytes)	RO
27	***Function supports 512 PB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 512 PB (2^{59} bytes)	RO
28	***Function supports 1 EB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 1 EB (2^{60} bytes)	RO
29	***Function supports 2 EB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 2 EB (2^{61} bytes)	RO
30	***Function supports 4 EB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 4 EB (2^{62} bytes)	RO
31	***Function supports 8 EB BAR*** - When Set, indicates that the Function supports operating with the BAR sized to 8 EB (2^{63} bytes)	RO

7.8.7 ARI Extended Capability

ARI is an optional capability. This capability must be implemented by each Function in an ARI Device. It is not applicable to a Root Port, a Switch Downstream Port, an RCiEP, or a Root Complex Event Collector.

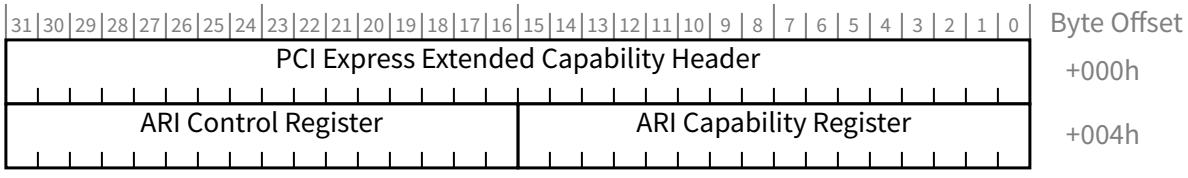

Figure 7-147 ARI Extended Capability

7.8.7.1 ARI Extended Capability Header (Offset 00h)

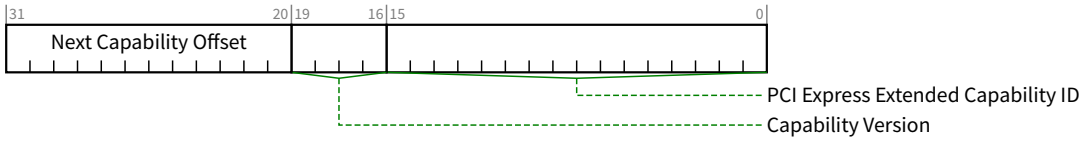

Figure 7-148 ARI Extended Capability Header

Table 7-118 ARI Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. PCI Express Extended Capability ID for the ARI Extended Capability is 000Eh.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.8.7.2 ARI Capability Register (Offset 04h)

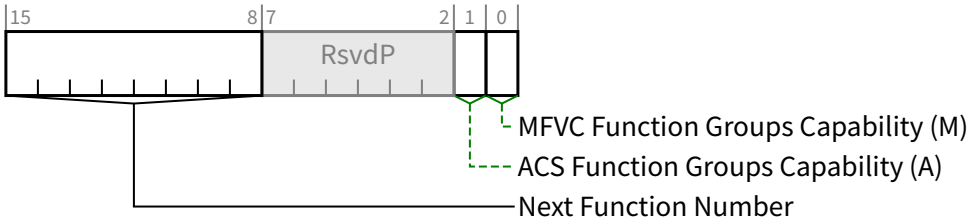

Figure 7-149 ARI Capability Register

Table 7-119 ARI Capability Register

Bit Location	Register Description	Attributes
0	***MFVC Function Groups Capability (M)*** - Applicable only for Function 0; must be 0b for all other Functions. If 1b, indicates that the ARI Device supports Function Group level arbitration via its Multi-Function Virtual Channel (MFVC) Capability structure.	RO
1	***ACS Function Groups Capability (A)*** - Applicable only for Function 0; must be 0b for all other Functions. If 1b, indicates that the ARI Device supports Function Group level granularity for ACS P2P Egress Control via its ACS Capability structures.	RO

Bit Location	Register Description	Attributes
15:8	***Next Function Number*** - This field indicates the Function Number of the next higher numbered Function in the Device, or 00h if there are no higher numbered Functions. Function 0 starts this linked list of Functions.	RO

7.8.7.3 ARI Control Register (Offset 06h)

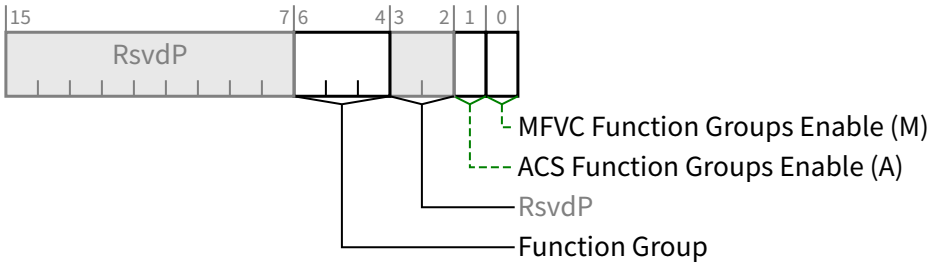

Figure 7-150 ARI Control Register

Table 7-120 ARI Control Register

Bit Location	Register Description	Attributes
0	***MFVC Function Groups Enable (M)*** - Applicable only for Function 0; must be hardwired to 0b for all other Functions. When set, the ARI Device must interpret entries in its Function Arbitration Table as Function Group Numbers rather than Function Numbers. Default value of this bit is 0b. Must be hardwired to 0b if the MFVC Function Groups Capability bit is 0b.	RW
1	***ACS Function Groups Enable (A)*** - Applicable only for Function 0; must be hardwired to 0b for all other Functions. When set, each Function in the ARI Device must associate bits within its Egress Control Vector with Function Group Numbers rather than Function Numbers. Default value of this bit is 0b. Must be hardwired to 0b if the ACS Function Groups Capability bit is 0b.	RW
6:4	***Function Group*** - Assigns a Function Group Number to this Function. Default value of this field is 000b. Must be hardwired to 000b if in Function 0, the MFVC Function Groups Capability bit and ACS Function Groups Capability bit are both 0b.	RW

7.8.8 *PASID Extended Capability* Structure

The presence of a PASID Extended Capability indicates that the Endpoint supports sending and receiving TLPs containing a PASID TLP Prefix. Separate support and enables are provided for the various optional features.

This capability is applicable to Endpoints and RCiEPs. For Root Ports, support and control is outside the scope of this specification.

This capability is independent of both the ATS and PRI features defined in Chapter 10 . Endpoints that contain a PASID Extended Capability need not support ATS or PRI. Endpoints that support ATS or PRI need not support PASID.

Figure 7-151 details allocation of the register bits in the PASID Extended Capability structure.

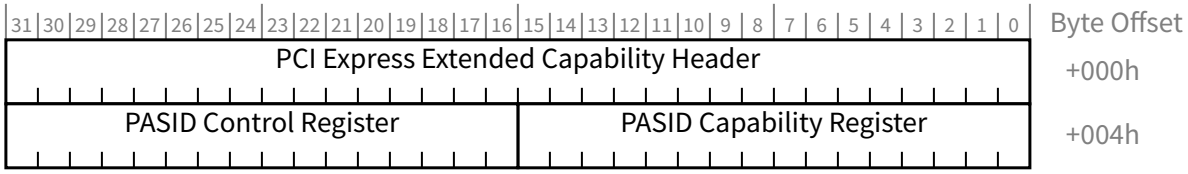

Figure 7-151 PASID Extended Capability Structure

7.8.8.1 PASID Extended Capability Header (Offset 00h)

Figure 7-152 details allocation of the register fields in the PASID Extended Capability Header; Table 7-121 provides the respective bit definitions.

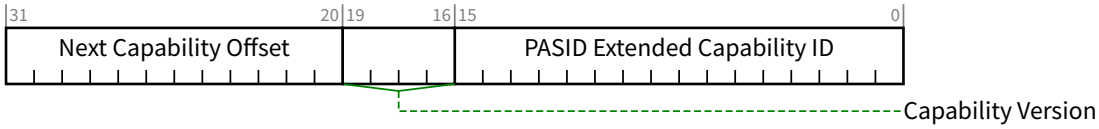

Figure 7-152 PASID Extended Capability Header

Table 7-121 PASID Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PASID Extended Capability ID*** - Indicates the PASID Extended Capability structure. This field must return a Capability ID of 001Bh indicating that this is a PASID Extended Capability structure.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - The offset to the next PCI Extended Capability structure or 000h if no other items exist in the linked list of capabilities.	RO

7.8.8.2 PASID Capability Register (Offset 04h)

Figure 7-153 details the allocation of register bits of the PASID Capability register; Table 7-122 provides the respective bit definitions.

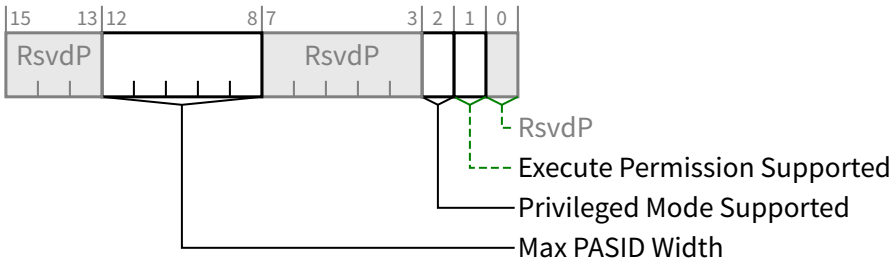

Figure 7-153 PASID Capability Register

Table 7-122 PASID Capability Register

Bit Location	Register Description	Attributes
1	***Execute Permission Supported*** - If Set, the Endpoint supports sending TLPs that have the Execute Requested bit Set. If Clear, the Endpoint will never Set the Execute Requested bit.	RO
2	***Privileged Mode Supported*** - If Set, the Endpoint supports operating in Privileged and Non-Privileged modes, and supports sending requests that have the Privileged Mode Requested bit Set. If Clear, the Endpoint will never Set the Privileged Mode Requested bit.	RO
12:8	***Max PASID Width*** - Indicates the width of the PASID field supported by the Endpoint. The value n indicates support for PASID values 0 through 2^n-1 (inclusive). The value 0 indicates support for a single PASID (0). The value 20 indicates support for all PASID values (20 bits). This field must be between 0 and 20 (inclusive).	RO

7.8.8.3 PASID Control Register (Offset 06h)

Figure 7-154 details the allocation of register bits of the PASID Control register; Table 7-123 provides the respective bit definitions.

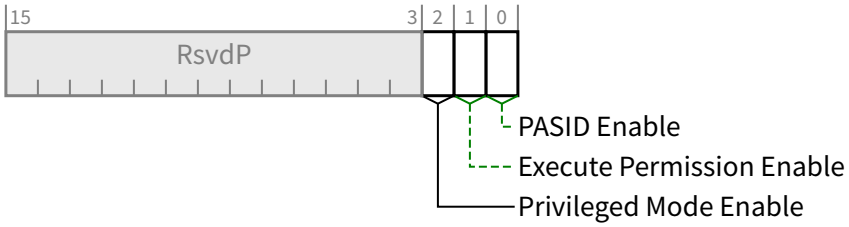

Figure 7-154 PASID Control Register

Table 7-123 PASID Control Register

Bit Location	Register Description	Attributes
0	***PASID Enable*** - If Set, the Endpoint is permitted to send and receive TLPs that contain a PASID TLP Prefix. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if the Endpoint supports ATS and this bit changes value when the Enable (E) bit in the ATS Control register is Set (see Section 10.5.1.3). Default is 0b.	RW
1	***Execute Permission Enable*** - If Set, the Endpoint is permitted to send Requests that have the Execute Requested bit Set. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if the Endpoint supports ATS and this bit changes value when the Enable bit in the ATS Control register is Set (see Section 10.5.1.3). If Execute Permission Supported is Clear, this bit is RsvdP. Default is 0b.	RW/RsvdP (see description)
2	***Privileged Mode Enable*** - If Set, the Endpoint is permitted to send Requests that have the Privileged Mode Requested bit Set. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if the Endpoint supports ATS and this bit changes value when the Enable bit in the ATS Control register is Set (see TSection 10.5.1.3). If Privileged Mode Supported is Clear, this bit is RsvdP. Default is 0b.	RW/RsvdP (see description)

7.8.9 *FRS Queueing Extended Capability*

The FRS Queueing Extended Capability is required for Root Ports and Root Complex Event Collectors that support the optional normative FRS Queueing capability. See Section 6.23 . This extended capability is only permitted in Root Ports and Root Complex Event Collectors.

If this capability is present in a Function, that Function must also implement either MSI, MSI-X, or both.

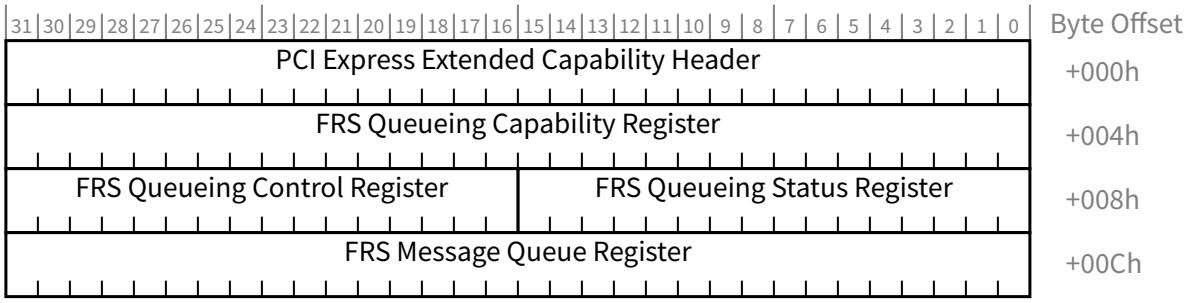

Figure 7-155 FRS Queueing Extended Capability

7.8.9.1 FRS Queueing Extended Capability Header (Offset 00h)

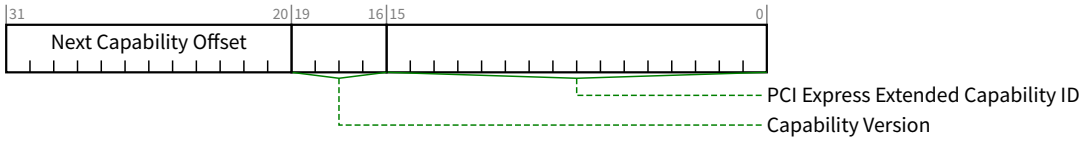

Figure 7-156 FRS Queueing Extended Capability Header

Table 7-124 FRS Queueing Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. PCI Express Extended Capability ID for the FRS Queueing Extended Capability is 0021h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of capabilities.	RO

7.8.9.2 FRS Queueing Capability Register (Offset 04h)

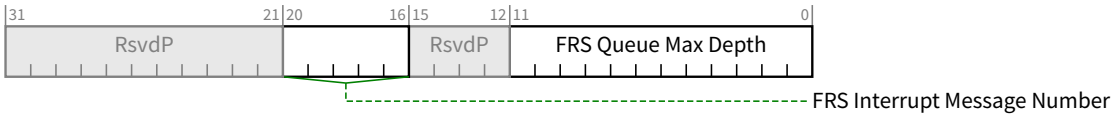

Figure 7-157 FRS Queueing Capability Register

Table 7-125 FRS Queueing Capability Register

Bit Location	Register Description	Attributes
11:0	***FRS Queue Max Depth*** - Indicates the implemented queue depth, with valid values ranging from 001h (queue depth of 1) to FFFh (queue depth of 4095) The value of FRS Message Queue Depth must not exceed this value. The value 000h is Reserved.	HwInit
20:16	***FRS Interrupt Message Number*** - This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with FRS Message Received or FRS Message Overflow. For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of	RO

Bit Location	Register Description	Attributes
	MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the Message Control Register for MSI. For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined.	

7.8.9.3 FRS Queueing Status Register (Offset 08h)

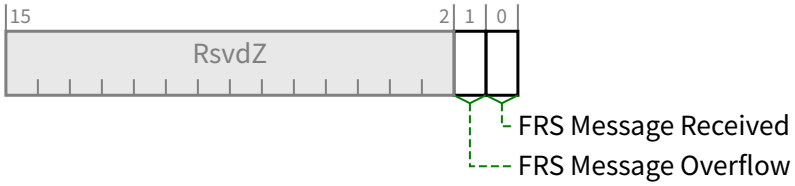

Figure 7-158 FRS Queueing Status Register

Table 7-126 FRS Queueing Status Register

Bit Location	Register Description	Attributes
0	***FRS Message Received*** - This bit is Set when a new FRS Message is Received or generated by this Root Port or Root Complex Event Collector. Root Ports must Clear this bit when the Link is DL_Down. Default value of this bit is 0b.	RW1C
1	***FRS Message Overflow*** - This bit is set if the FRS Message queue is full and a new FRS Message is received or generated by this Root Port or Root Complex Event Collector. Root Ports must Clear this bit when the Link is DL_Down. Default value of this bit is 0b.	RW1C

7.8.9.4 FRS Queueing Control Register (Offset 0Ah)

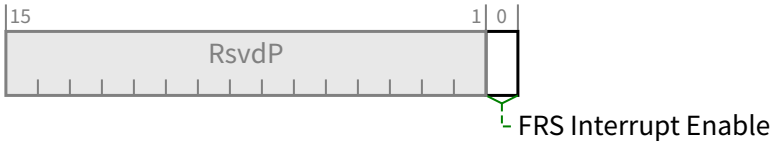

Figure 7-159 FRS Queueing Control Register

Table 7-127 FRS Queueing Control Register

Bit Location	Register Description	Attributes
0	***FRS Interrupt Enable*** - When Set and MSI or MSI-X is enabled, the Port must issue an MSI/MSI-X interrupt to indicate the 0b to 1b transition of either the FRS Message Received or the FRS Message Overflow bits. Default value of this bit is 0b.	RW

7.8.9.5 FRS Message Queue Register (Offset 0Ch)

The FRS Message Queue Register contains fields from the oldest FRS message in the queue. It also indicates the number of FRS messages in the queue.

A write of any value that includes byte 0 to this register removes the oldest FRS Message from the queue and updates these fields. A write to this register when the queue is empty has no effect.

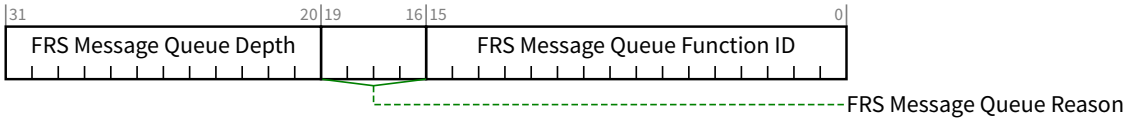

Figure 7-160 FRS Message Queue Register

Table 7-128 FRS Message Queue Register

Bit Location	Register Description	Attributes
15:0	***FRS Message Queue Function ID*** - Recorded from the Requester ID of the oldest FRS Message Received or generated by this Root Port or Root Complex Event Collector and still in the queue. Undefined if FRS Message Queue Depth is 000h.	RO
19:16	***FRS Message Queue Reason*** - Recorded from the FRS Reason of the oldest FRS Message Received or generated by this Root Port or Root Complex Event Collector and still in the queue. Undefined if FRS Message Queue Depth is 000h.	RO
31:20	***FRS Message Queue Depth*** - indicates the current number of FRS Messages in the queue.	RO

Bit Location	Register Description	Attributes
	The value of 000h indicates an empty queue. Default value of this field is 000h.	

7.8.10 *Flattening Portal Bridge (FPB) Capability*

The Flattening Portal Bridge (FPB) Capability is an optional Capability that is required for any bridge Function that implements FPB. The FPB Capability structure is shown in Figure 7-161 .

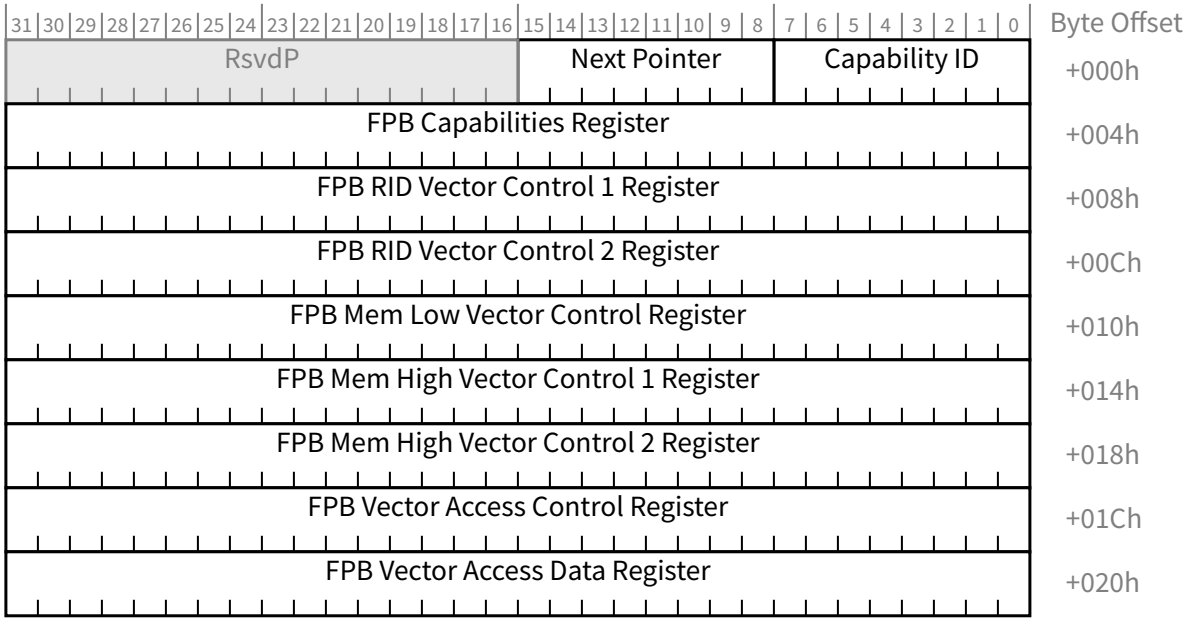

Figure 7-161 FPB Capability Structure

If a Switch implements FPB then each of its Ports of the Switch must implement an FPB Capability Structure. A Root Complex is permitted to implement the FPB Capability Structure on some or on all of its Root Ports. A Root Complex is permitted to implement the FPB Capability for internal logical busses.

7.8.10.1 FPB Capability Header (Offset 00h)

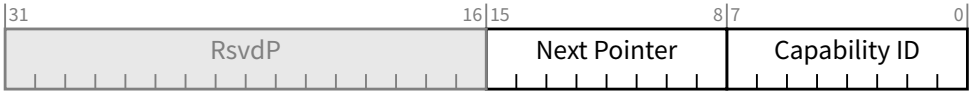

Figure 7-162 FPB Capability Header

Table 7-129 FPB Capability Header

Bit Location	Register Description	Attributes
7:0	***Capability ID*** - Must be set to 15h	RO
15:8	***Next Pointer*** - Pointer to the next item in the capabilities list. Must be 00h for the final item in the list.	RO

7.8.10.2 FPB Capabilities Register (Offset 04h)

Figure 7-163 details allocation of register fields for FPB Capabilities register and Table 7-130 describes the requirements for this register.

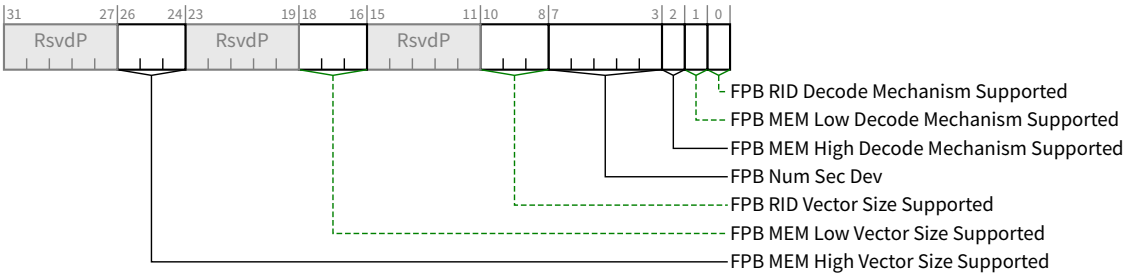

Figure 7-163 FPB Capabilities Register

Table 7-130 FPB Capabilities Register

Bit Location	Register Description	Attributes
0	***FPB RID Decode Mechanism Supported*** - If Set, indicates that the FPB RID Vector mechanism is supported.	HwInit
1	***FPB MEM Low Decode Mechanism Supported*** - If Set, indicates that the FPB MEM Low Vector mechanism is supported.	HwInit
2	***FPB MEM High Decode Mechanism Supported*** - If Set, indicates that the FPB Mem High mechanism is supported.	HwInit
7:3	***FPB Num Sec Dev*** - For Upstream Ports of Switches only, this field indicates the quantity of Device Numbers associated with the Secondary Side of the Upstream Port bridge. The quantity is determined by adding one to the numerical value of this field. Although it is recommended that Switch implementations assign Downstream Ports using all 8 allowed Functions per allocated Device Number, such that all Downstream Ports are assigned within a contiguous range of Device and Function Numbers, it is, however, explicitly permitted to assign Downstream Ports to Function Numbers that are not contiguous within the indicated range of Device Numbers, and system software is required to scan for Switch Downstream Ports at every Function Number within the indicated quantity of Device Numbers associated with the Secondary Side of the Upstream Port. This field is Reserved for Downstream Ports.	HwInit/RsvdP
10:8	***FPB RID Vector Size Supported*** - Indicates the size of the FPB RID Vector implemented in hardware, and constrains the allowed values software is permitted to write to the FPB RID Vector Granularity field.	HwInit

<table>
<tr><th>Bit Location</th><th>Register Description</th><th>Attributes</th></tr>
<tr><td></td><td>Defined encodings are:<table><tr><th>Value</th><th>Size</th><th>Allowed Granularities in RID units</th></tr><tr><td>000b</td><td>256 bits</td><td>8, 64, 256</td></tr><tr><td>010b</td><td>1 K bits</td><td>8, 64</td></tr><tr><td>101b</td><td>8 K bits</td><td>8</td></tr></table>All other encodings are Reserved.
If the FPB RID Decode Mechanism Supported bit is Clear, then the value in this field is undefined and must be ignored by software.</td><td></td></tr>
<tr><td>18:16</td><td>FPB MEM Low Vector Size Supported - Indicates the size of the FPB MEM Low Vector implemented in hardware, and constrains the allowed values software is permitted to write to the FPB MEM Low Vector Start field.
Defined encodings are:<table><tr><th>Value</th><th>Size</th><th>Allowed Granularities in MB units</th></tr><tr><td>000b</td><td>256 bits</td><td>1, 2, 4, 8, 16</td></tr><tr><td>001b</td><td>512 bits</td><td>1, 2, 4, 8</td></tr><tr><td>010b</td><td>1 K bits</td><td>1, 2, 4</td></tr><tr><td>011b</td><td>2 K bits</td><td>1, 2</td></tr><tr><td>100b</td><td>4 K bits</td><td>1</td></tr></table>All other encodings are Reserved.
If the FPB MEM Low Decode Mechanism Supported bit is Clear, then the value in this field is undefined and must be ignored by software.</td><td>HwInit</td></tr>
<tr><td>26:24</td><td>FPB MEM High Vector Size Supported - Indicates the size of the FPB MEM High Vector implemented in hardware.
Defined encodings are:<table><tr><th>Value</th><th>Size</th></tr><tr><td>000b</td><td>256 bits</td></tr><tr><td>001b</td><td>512 bits</td></tr><tr><td>010b</td><td>1 K bits</td></tr><tr><td>011b</td><td>2 K bits</td></tr><tr><td>100b</td><td>4 K bits</td></tr><tr><td>101b</td><td>8 K bits</td></tr></table>All other encodings are Reserved.
All defined Granularities are allowed for all defined vector sizes.</td><td>HwInit</td></tr>
</table>

Bit Location	Register Description	Attributes
	If the FPB MEM High Decode Mechanism Supported bit is Clear, then the value in this field is undefined and must be ignored by software.	

7.8.10.3 FPB RID Vector Control 1 Register (Offset 08h)

Figure 7-164 details allocation of register fields for FPB RID Control 1 register and Table 7-131 describes the requirements for this register.

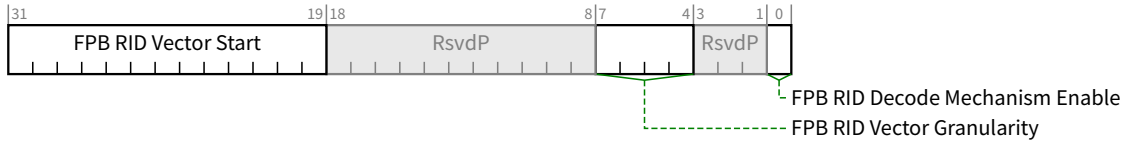

Figure 7-164 FPB RID Vector Control 1 Register

Table 7-131 FPB RID Vector Control 1 Register

Bit Location	Register Description	Attributes
0	***FPB RID Decode Mechanism Enable*** - When Set, enables the FPB RID Decode mechanism If the FPB RID Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this bit as RO, and in this case the value in this field is undefined. Default value of this bit is 0b.	RW/RO
7:4	***FPB RID Vector Granularity*** - The value written by software to this field controls the granularity of the FPB RID Vector and the required alignment of the FPB RID Vector Start field (below). Defined encodings are: Value / Granularity: 0000b / 8 RIDs; 0011b / 64 RIDs; 0101b / 256 RIDs All other encodings are Reserved. Based on the implemented FPB RID Vector size, hardware is permitted to implement as RW only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0. If the FPB RID Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. For Downstream Ports, if the ARI Forwarding Enable bit in the Device Control 2 Register and the FPB RID Decode Mechanism Enable bit are Set, then software must program 0101b into this field, if this field is programmable. Default value for this field is 0000b.	RW/RO

Bit Location	Register Description	Attributes
31:19	***FPB RID Vector Start*** - The value written by software to this field controls the offset at which the FPB RID Vector is applied. The value represents a RID offset in units of 8 RIDs, such that bit 0 of the FPB RID Vector represents the range of RIDs starting from the value represented in this register up to that value plus the FPB RID Vector Granularity minus 1, and bit 1 represents range from this register value plus granularity up to that value plus FPB RID Vector Granularity minus 1, etc. Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0's) according to the value in the FPB RID Vector Granularity Field as indicated here: FPB RID Vector Granularity / Start Alignment Constraint 0000b / <no constraint> 0011b / …00 0b 0101b / …0000 0b All other encodings are Reserved. If this requirement is violated, the hardware behavior is undefined. For Downstream Ports, if the ARI Forwarding Enable bit in the Device Control 2 Register and the FPB RID Decode Mechanism Enable bit are Set, then software must program bits 23:19 of this field to a value of 0000 0b, and the hardware behavior is undefined if any other value is programmed. If the FPB RID Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0000 0000 0000 0b.	RW/RO

7.8.10.4 FPB RID Vector Control 2 Register (Offset 0Ch)

Figure 7-165 details allocation of register fields for FPB RID Vector Control 2 register and Table 7-132 describes the requirements for this register

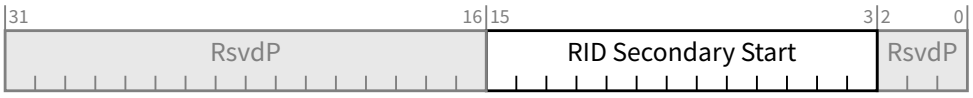

Figure 7-165 FPB RID Vector Control 2 Register

Table 7-132 FPB RID Vector Control 2 Register

Bit Location	Register Description	Attributes
15:3	***RID Secondary Start*** - The value written by software to this field controls the RID offset at which Type 1 Configuration Requests passing downstream through the bridge must be converted to Type 0. Bits[2:0] of the RID offset are fixed by hardware as 000b and cannot be modified. For Downstream Ports, if the ARI Forwarding Enable bit in the Device Control 2 register is Set, then software must write bits 7:3 of this field to 0 0000b.	RW/RO

Bit Location	Register Description	Attributes
	If the FPB RID Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0000 0000 0000 0b.	

7.8.10.5 FPB MEM Low Vector Control Register (Offset 10h)

Figure 7-166 details allocation of register fields for FPB MEM Low Vector Control Register and Table 7-133 describes the requirements for this register.

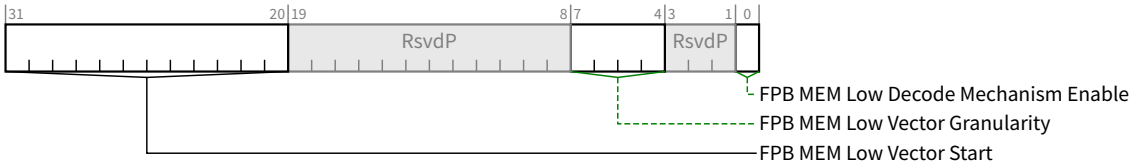

Figure 7-166 FPB MEM Low Vector Control Register

Table 7-133 FPB MEM Low Vector Control Register

Bit Location	Register Description	Attributes
0	***FPB MEM Low Decode Mechanism Enable*** - When Set, enables the FPB MEM Low Decode mechanism. If the FPB MEM Low Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this bit as RO, and in this case the value in this field is undefined. Default value of this bit is 0b.	RW/RO
7:4	***FPB MEM Low Vector Granularity*** - The value written by software to this field controls the granularity of the FPB MEM Low Vector, and the required alignment of the FPB MEM Low Vector Start field (below). Defined encodings are: Value / Granularity: 0000b = 1 MB; 0001b = 2 MB; 0010b = 4 MB; 0011b = 8 MB; 0100b = 16 MB All other encodings are Reserved. Based on the implemented FPB MEM Low Vector size, hardware is permitted to implement as RW only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0. If the FPB MEM Low Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined.	RW/RO

Bit Location	Register Description	Attributes
	Default value for this field is 0000b.	
31:20	***FPB MEM Low Vector Start*** - The value written by software to this field sets bits 31:20 of the base address at which the FPB MEM Low Vector is applied. Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0's) according to the value in the FPB MEM Low Vector Granularity field as indicated here: FPB MEM Low Vector Granularity / Constraint: 0000b — <no constraint> 0001b — …0b 0010b — …00b 0011b — …000b 0100b — …0000b If this requirement is violated, the hardware behavior is undefined. If the FPB MEM Low Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 000h.	RW/RO

7.8.10.6 FPB MEM High Vector Control 1 Register (Offset 14h)

Figure 7-167 details allocation of register fields for FPB MEM High Vector Control 1 Register and Table 7-134 describes the requirements for this register.

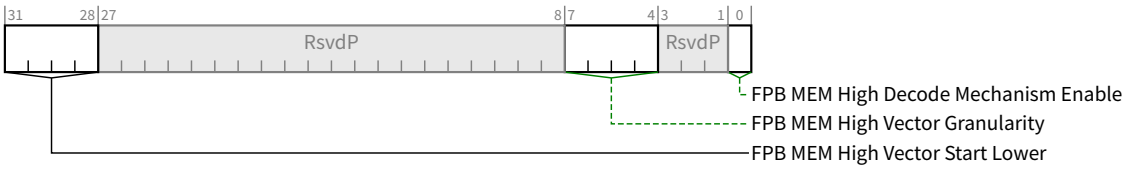

Figure 7-167 FPB MEM High Vector Control 1 Register

Table 7-134 FPB MEM High Vector Control 1 Register

Bit Location	Register Description	Attributes
0	***FPB MEM High Decode Mechanism Enable*** - When Set, enables the FPB MEM High Decode mechanism. If the FPB MEM High Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this bit as RO, and in this case the value in this field is undefined. Default value of this bit is 0b.	RW/RO

<table>
<tr><th>Bit Location</th><th>Register Description</th><th>Attributes</th></tr>
<tr><td>7:4</td><td>FPB MEM High Vector Granularity - The value written by software to this field controls the granularity of the FPB MEM High Vector, and the required alignment of the FPB MEM High Vector Start Lower field (below).

Software is permitted to select any allowed Granularity from the table below regardless of the value in the FPB MEM High Vector Size Supported field.

Defined encodings are:

<table>
<tr><th>Value</th><th>Granularity</th></tr>
<tr><td>0000b</td><td>256 MB</td></tr>
<tr><td>0001b</td><td>512 MB</td></tr>
<tr><td>0010b</td><td>1 GB</td></tr>
<tr><td>0011b</td><td>2 GB</td></tr>
<tr><td>0100b</td><td>4 GB</td></tr>
<tr><td>0101b</td><td>8 GB</td></tr>
<tr><td>0110b</td><td>16 GB</td></tr>
<tr><td>0111b</td><td>32 GB</td></tr>
</table>
All other encodings are Reserved.

Based on the implemented FPB MEM High Vector size, hardware is permitted to implement as RW only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0.

If the FPB MEM High Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined.

Default value for this field is 0000b.</td><td>RW/RO</td></tr>
<tr><td>31:28</td><td>FPB MEM High Vector Start Lower - The value written by software to this field sets the lower bits of the base address at which the FPB MEM High Vector is applied.

Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0’s) according to the value in the FPB MEM High Vector Granularity Field as indicated here:

<table>
<tr><th>FPB MEM High Vector Granularity</th><th>Constraint</th></tr>
<tr><td>0000b</td><td><no constraint></td></tr>
<tr><td>0001b</td><td>…0b</td></tr>
<tr><td>0010b</td><td>…00b</td></tr>
<tr><td>0011b</td><td>…000b</td></tr>
<tr><td>0100b</td><td>…0000b</td></tr>
<tr><td>0101b</td><td>…0 0000b</td></tr>
<tr><td>0110b</td><td>…00 0000b</td></tr>
<tr><td>0111b</td><td>…000 0000b</td></tr>
</table></td><td>RW/RO</td></tr>
</table>

Bit Location	Register Description	Attributes
	If this requirement is violated, the hardware behavior is undefined. If the FPB MEM High Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0h.	

7.8.10.7 FPB MEM High Vector Control 2 Register (Offset 18h)

Figure 7-168 details allocation of register fields for FPB MEM High Vector Control 2 Register and Table 7-135 describes the requirements for this register.

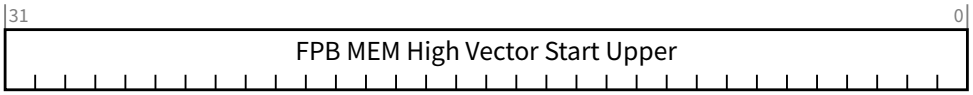

Figure 7-168 FPB MEM High Vector Control 2 Register

Table 7-135 FPB MEM High Vector Control 2 Register

Bit Location	Register Description	Attributes
31:0	***FPB MEM High Vector Start Upper*** - The value written by software to this field sets bits 63:32 of the base address at which the FPB MEM High Vector is applied. Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0's) according to the value in the FPB MEM High Vector Granularity Field as indicated here: **FPB MEM High Vector Granularity** / **Constraint** 0000b — <no constraint> 0001b — <no constraint> 0010b — <no constraint> 0011b — <no constraint> 0100b — <no constraint> 0101b — …0b 0110b — …00b 0111b — …000b If this requirement is violated, the hardware behavior is undefined If the FPB MEM High Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined. Default value for this field is 0000 0000h.	RW/RO

7.8.10.8 FPB Vector Access Control Register (Offset 1Ch)

Figure 7-169 details allocation of register fields for FPB Vector Access Control register and Table 7-136 describes the requirements for this register.

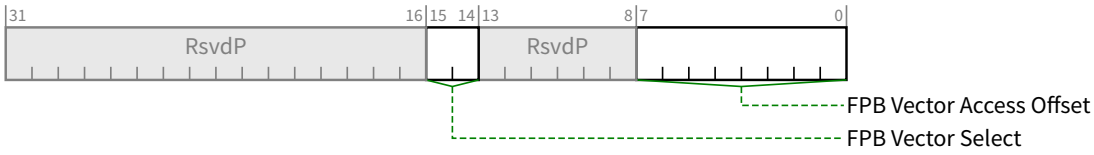

Figure 7-169 FPB Vector Access Control Register

Table 7-136 FPB Vector Access Control Register

Bit Location	Register Description	Attributes
7:0	***FPB Vector Access Offset*** - The value in this field indicates the offset of the DWORD portion of the FPB RID, MEM Low or MEM High, Vector that can be read or written by means of the FPB Vector Access Data register. The selection of RID, MEM Low or MEM High is made by the value written to the FPB Vector Select field. The bits of this field map to the offset according to the value in the corresponding FPB RID, MEM Low, or MEM High Vector Size Supported field as shown here: **Vector Size Supported / Offset Bits / Vector Access Offset** 000b — 2:0 — 2:0 (7:3 unused) 001b — 3:0 — 3:0 (7:4 unused) 010b — 4:0 — 4:0 (7:5 unused) 011b — 5:0 — 5:0 (7:6 unused) 100b — 6:0 — 6:0 (7 unused) 101b — 7:0 — 7:0 All other encodings are Reserved. Bits in this field that are unused per the table above must be written by software as 0b, and are permitted but not required to be implemented as RO. Default value for this field is 00h	RW/RO
15:14	***FPB Vector Select*** - The value written to this field selects the Vector to be accessed at the indicated FPB Vector Access Offset. Software must only write this field with values that correspond to supported FPB mechanisms, otherwise the results are undefined. Defined encodings are: **00b** RID **01b** MEM Low **10b** MEM High	RW

Bit Location	Register Description	Attributes
	11b Reserved Default value for this field is 00b	

7.8.10.9 FPB Vector Access Data Register (Offset 20h)

Figure 7-170 details allocation of register fields for FPB Vector Access Data Register and Table 7-137 describes the requirements for this register.

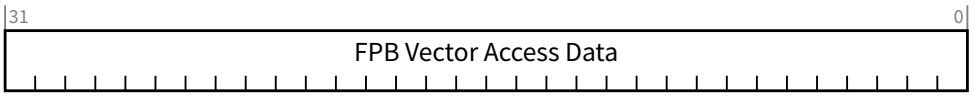

Figure 7-170 FPB Vector Access Data Register

Table 7-137 FPB Vector Access Data Register

Bit Location	Register Description	Attributes
31:0	***FPB Vector Access Data*** - Reads from this register return the DW of data from the FPB Vector at the location determined by the value in the FPB Vector Access Offset Register. Writes to this register replace the DW of data from the FPB Vector at the location determined by the value in the FPB Vector Access Offset Register. Behavior of this field is undefined if software programs unsupported values for FPB Vector Select or FPB Vector Access Offset fields, however hardware is required to complete the access to this register normally. Default value for this field is 0000 0000h	RW

7.9 Additional PCI and PCIe Capabilities

This section, contains a description of additional PCI and PCIe capabilities that are individually optional in this but may be required by other PCISIG specifications.

7.9.1 Virtual Channel Extended Capability

The Virtual Channel Extended Capability (***VC Capability***) is an optional Extended Capability required for devices that have Ports (or for individual Functions) that support functionality beyond the default Traffic Class (TC0) over the default Virtual Channel (VC0). This may apply to devices with only one VC that support TC filtering or to devices that support multiple VCs. Note that a PCI Express device that supports only TC0 over VC0 does not require VC Extended Capability and associated registers. Figure 7-171 provides a high level view of the Virtual Channel Extended Capability structure. This structure controls Virtual Channel assignment for PCI Express Links and may be present in any device (or RCRB) that contains (controls) a Port, or any device that has a Multi-Function Virtual Channel (MFVC) Capability structure. Some registers/fields in the Virtual Channel Extended Capability structure may have different interpretation for Endpoints,

Switch Ports, Root Ports and RCRB. Software must interpret the Device/Port Type field in the PCI Express Capabilities register to determine the availability and meaning of these registers/fields.

The number of (extended) Virtual Channels is indicated by the Extended VC Count field in the Port VC Capability Register 1. Software must interpret this field to determine the availability of extended VC Resource registers.

The VC Capability structure is permitted in the Extended Configuration Space of all single-Function devices or in RCRBs.

A Multi-Function Device at an Upstream Port is permitted to optionally contain a Multi-Function Virtual Channel (MFVC) Capability structure (see Section 7.9.2). If a Multi-Function Device contains an MFVC Capability structure, any or all of its Functions are permitted to contain a VC Capability structure. Per-Function VC Capability structures are also permitted for devices inside a Switch that contain only Switch Downstream Port Functions, or for RCiEPs. Otherwise, only Function 0 is permitted to contain a VC Capability structure.

To preserve software backward compatibility, two Extended Capability IDs are permitted for VC Capability structures: 0002h and 0009h. Any VC Capability structure in a device that also contains an MFVC Capability structure must use the Extended Capability ID 0009h. A VC Capability structure in a device that does not contain an MFVC Capability structure must use the Extended Capability ID 0002h.

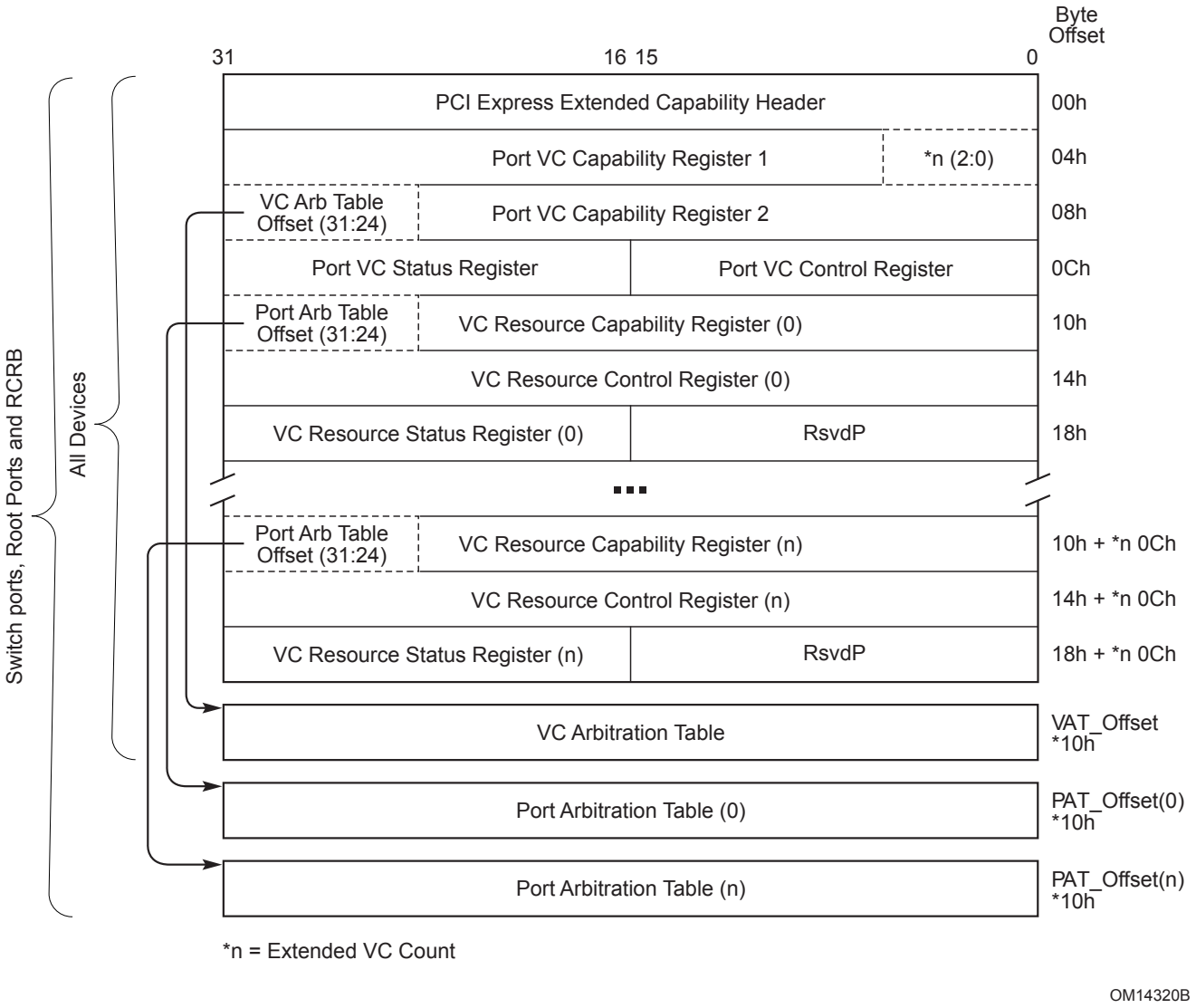

Figure 7-171 Virtual Channel Extended Capability Structure

The following sections describe the registers/fields of the Virtual Channel Extended Capability structure.

7.9.1.1 Virtual Channel Extended Capability Header (Offset 00h)

Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. A Virtual Channel Extended Capability must use one of two Extended Capability IDs: 0002h or 0009h. Refer to Section 7.9.1 for rules governing when each should be used. Figure 7-172 details allocation of register fields in the Virtual Channel Extended Capability Header; Table 7-138 provides the respective bit definitions.

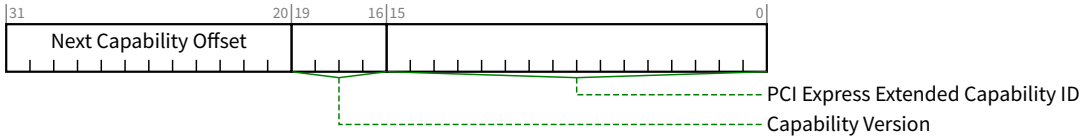

Figure 7-172 Virtual Channel Extended Capability Header

Table 7-138 Virtual Channel Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Virtual Channel Extended Capability is either 0002h or 0009h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.1.2 Port VC Capability Register 1 (Offset 04h)

The Port VC Capability Register 1 describes the configuration of the Virtual Channels associated with a PCI Express Port. Figure 7-173 details allocation of register fields in the Port VC Capability Register 1; Table 7-139 provides the respective bit definitions.

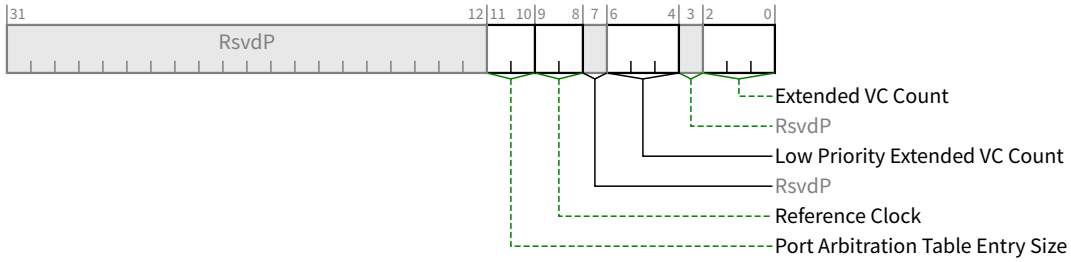

Figure 7-173 Port VC Capability Register 1

Table 7-139 Port VC Capability Register 1

Bit Location	Register Description	Attributes
2:0	***Extended VC Count*** - Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all Functions. This value indicates the number of (extended) VC Resource Capability, Control, and Status registers that are present in Configuration Space in addition to the required VC Resource registers for the default VC. The minimum value of this field is 0 (for devices that only support the default VC and only have 1 set of VC Resource Registers for that VC). The maximum value is 7.	RO
6:4	***Low Priority Extended VC Count*** - Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. This field is valid for all Functions. The minimum value of this field is 000b and the maximum value is Extended VC Count.	RO
9:8	***Reference Clock*** - Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. This field is valid for RCRBs, Switch Ports, and Root Ports that support peer-to-peer traffic. It is not valid for Root Ports that do not support peer-to-peer traffic, Endpoints, and Switches or Root Complexes not implementing WRR, and must be hardwired to 00b. Defined encodings are: **00b** 100 ns reference clock **01b - 11b** Reserved	RO
11:10	***Port Arbitration Table Entry Size*** - Indicates the size (in bits) of Port Arbitration table entry in the Function. This field is valid only for RCRBs, Switch Ports, and Root Ports that support peer-to-peer traffic. It is not valid and must be hardwired to 00b for Root Ports that do not support peer-to-peer traffic and Endpoints. Defined encodings are: **00b** The size of Port Arbitration table entry is 1 bit. **01b** The size of Port Arbitration table entry is 2 bits. **10b** The size of Port Arbitration table entry is 4 bits. **11b** The size of Port Arbitration table entry is 8 bits.	RO

7.9.1.3 Port VC Capability Register 2 (Offset 08h)

The Port VC Capability Register 2 provides further information about the configuration of the Virtual Channels associated with a PCI Express Port. Figure 7-174 details allocation of register fields in the Port VC Capability Register 2; Table 7-140 provides the respective bit definitions.

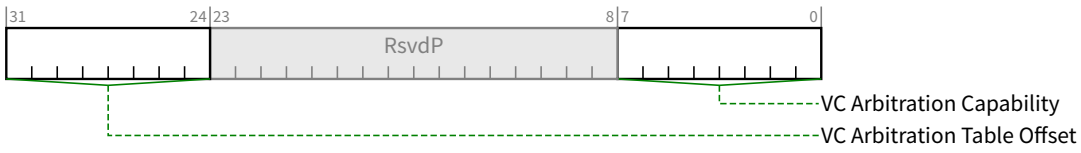

Figure 7-174 Port VC Capability Register 2

Table 7-140 Port VC Capability Register 2

Bit Location	Register Description	Attributes
7:0	***VC Arbitration Capability*** - Indicates the types of VC Arbitration supported by the Function for the LPVC group. This field is valid for all Functions that report a Low Priority Extended VC Count field greater than 0. For all other Functions, this field must be hardwired to 00h. Each Bit Location within this field corresponds to a VC Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the Port can be configured to provide different VC arbitration services. Defined bit positions are: **Bit 0** Hardware fixed arbitration scheme, e.g., Round Robin **Bit 1** Weighted Round Robin (WRR) arbitration with 32 phases **Bit 2** WRR arbitration with 64 phases **Bit 3** WRR arbitration with 128 phases **Bits 4-7** Reserved	RO
31:24	***VC Arbitration Table Offset*** - Indicates the location of the VC Arbitration Table. This field is valid for all Functions. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Extended Capability structure. A value of 0 indicates that the table is not present.	RO

7.9.1.4 Port VC Control Register (Offset 0Ch)

Figure 7-175 details allocation of register fields in the Port VC Control Register; Table 7-141 provides the respective bit definitions.

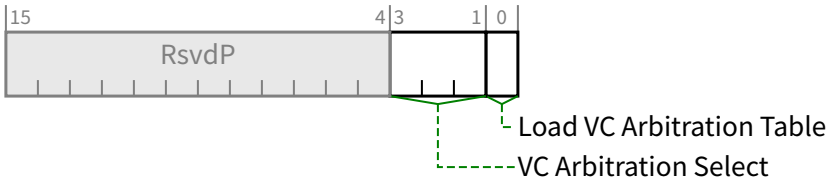

Figure 7-175 Port VC Control Register

Table 7-141 Port VC Control Register

Bit Location	Register Description	Attributes
0	***Load VC Arbitration Table*** - Used by software to update the VC Arbitration Table. This bit is valid for all Functions when the selected VC Arbitration uses the VC Arbitration Table. Software sets this bit to request hardware to apply new values programmed into VC Arbitration Table; clearing this bit has no effect. Software checks the VC Arbitration Table Status bit to confirm that new values stored in the VC Arbitration Table are latched by the VC arbitration logic. This bit always returns 0b when read.	RW

Bit Location	Register Description	Attributes
3:1	***VC Arbitration Select*** - Used by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability Register 2. This field is valid for all Functions. The permissible values of this field are numbers corresponding to one of the asserted bits in the VC Arbitration Capability field. This field cannot be modified when more than one VC in the LPVC group is enabled.	RW

7.9.1.5 Port VC Status Register (Offset 0Eh)

The Port VC Status Register provides status of the configuration of Virtual Channels associated with a Port. Figure 7-176 details allocation of register fields in the Port VC Status Register; Table 7-142 provides the respective bit definitions.

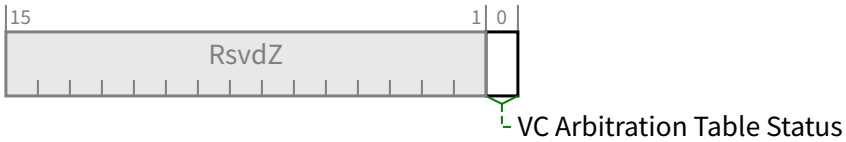

Figure 7-176 Port VC Status Register

Table 7-142 Port VC Status Register

Bit Location	Register Description	Attributes
0	***VC Arbitration Table Status*** - Indicates the coherency status of the VC Arbitration Table. This bit is valid for all Functions when the selected VC uses the VC Arbitration Table. This bit is Set by hardware when any entry of the VC Arbitration Table is written by software. This bit is Cleared by hardware when hardware finishes loading values stored in the VC Arbitration Table after software sets the Load VC Arbitration Table bit in the Port VC Control Register. Default value of this bit is 0b.	RO

7.9.1.6 VC Resource Capability Register

The VC Resource Capability Register describes the capabilities and configuration of a particular Virtual Channel resource. Figure 7-177 details allocation of register fields in the VC Resource Capability Register; Table 7-143 provides the respective bit definitions.

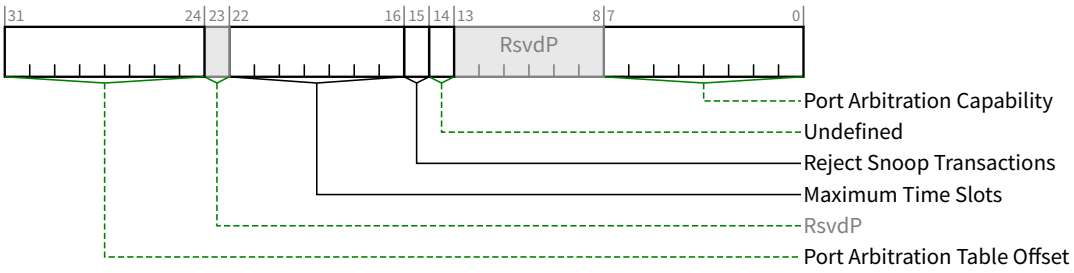

Figure 7-177 VC Resource Capability Register

Table 7-143 VC Resource Capability Register

Bit Location	Register Description	Attributes
7:0	***Port Arbitration Capability*** - Indicates types of Port Arbitration supported by the VC resource. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but not for Endpoints or Root Ports that do not support peer-to-peer traffic. Each Bit Location within this field corresponds to a Port Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Port Arbitration Select field (see Section 7.9.1.7). Defined bit positions are: **Bit 0** Non-configurable hardware-fixed arbitration scheme, e.g., Round Robin (RR) **Bit 1** Weighted Round Robin (WRR) arbitration with 32 phases **Bit 2** WRR arbitration with 64 phases **Bit 3** WRR arbitration with 128 phases **Bit 4** Time-based WRR with 128 phases **Bit 5** WRR arbitration with 256 phases **Bits 6-7** Reserved	RO
14	**Undefined** - The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate Advanced Packet Switching. System software must ignore the value read from this bit.	RO
15	***Reject Snoop Transactions*** - When Clear, transactions with or without the No Snoop bit Set within the TLP header are allowed on this VC. When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP header is permitted to be rejected as an Unsupported Request. Refer to Section 2.2.6.5 for information on where the No Snoop attribute is applicable. This bit is valid for Root Ports and RCRB; it is not valid for Endpoints or Switch Ports.	HwInit
22:16	***Maximum Time Slots*** - Indicates the maximum number of time slots (minus one) that the VC resource is capable of supporting when it is configured for time-based WRR Port Arbitration. For example, a value 000 0000b in this field indicates the supported maximum number of time slots is 1 and a value of 111 1111b indicates the supported maximum number of time slots is 128. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. In addition, this field is valid only when the Port Arbitration Capability field indicates that the VC resource supports time-based WRR Port Arbitration.	HwInit

Bit Location	Register Description	Attributes
31:24	***Port Arbitration Table Offset*** - Indicates the location of the Port Arbitration Table associated with the VC resource. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Extended Capability structure. A value of 00h indicates that the table is not present.	RO

7.9.1.7 VC Resource Control Register

Figure 7-178 details allocation of register fields in the VC Resource Control Register; Table 7-144 provides the respective bit definitions.

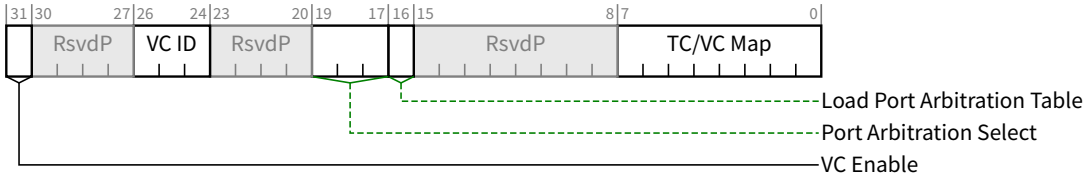

Figure 7-178 VC Resource Control Register

Table 7-144 VC Resource Control Register

Bit Location	Register Description	Attributes
7:0	***TC/VC Map*** - This field indicates the TCs that are mapped to the VC resource. This field is valid for all Functions. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be Set for the default VC0 and Clear for all other enabled VCs.	RW (see the note for exceptions)
16	***Load Port Arbitration Table*** - When Set, this bit updates the Port Arbitration logic from the Port Arbitration Table for the VC resource. This bit is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. In addition, this bit is only valid when the Port Arbitration Table is used by the selected Port Arbitration scheme (that is indicated by a Set bit in the Port Arbitration Capability field selected by Port Arbitration Select). Software sets this bit to signal hardware to update Port Arbitration logic with new values stored in Port Arbitration Table; clearing this bit has no effect. Software uses the Port Arbitration Table Status bit to confirm whether the new values of Port Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.	RW

Bit Location	Register Description	Attributes
19:17	***Port Arbitration Select*** - This field configures the VC resource to provide a particular Port Arbitration service. This field is valid for RCRBs, Root Ports that support peer-to-peer traffic, and Switch Ports, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. The permissible value of this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.	RW
26:24	***VC ID*** - This field assigns a VC ID to the VC resource (see note for exceptions). This field is valid for all Functions. This field cannot be modified when the VC is already enabled. Note: For the first VC resource (default VC), this field is read-only and must be hardwired to 000b.	RW
31	***VC Enable*** - This bit, when Set, enables a Virtual Channel (see note 1 for exceptions). The Virtual Channel is disabled when this bit is cleared. This bit is valid for all Functions. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. Default value of this bit is 1b for the first VC resource and is 0b for other VC resource(s). Notes: 1. This bit is hardwired to 1b for the default VC (VC0), i.e., writing to this bit has no effect for VC0. 2. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Set in both components on a Link. 3. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both components on a Link. 4. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 5. Software must fully disable a Virtual Channel in both components on a Link before re-enabling the Virtual Channel.	RW

7.9.1.8 VC Resource Status Register

Figure 7-179 details allocation of register fields in the VC Resource Status Register; Table 7-145 provides the respective bit definitions.

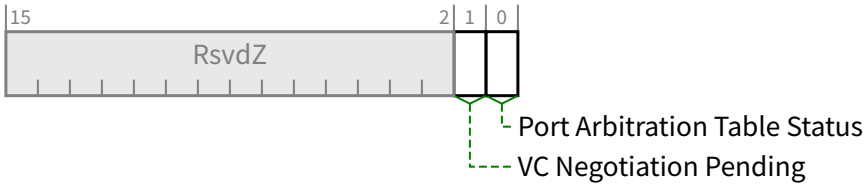

Figure 7-179 VC Resource Status Register

Table 7-145 VC Resource Status Register

Bit Location	Register Description	Attributes
0	***Port Arbitration Table Status*** - This bit indicates the coherency status of the Port Arbitration Table associated with the VC resource. This bit is valid for RCRBs, Root Ports that support peer-to-peer traffic, and Switch Ports, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. In addition, this bit is valid only when the Port Arbitration Table is used by the selected Port Arbitration for the VC resource. This bit is Set by hardware when any entry of the Port Arbitration Table is written to by software. This bit is Cleared by hardware when hardware finishes loading values stored in the Port Arbitration Table after software sets the Load Port Arbitration Table bit. Default value of this bit is 0b.	RO
1	***VC Negotiation Pending*** -This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. This bit is valid for all Functions. The value of this bit is defined only when the Link is in the DL_Active state and the Virtual Channel is enabled (its VC Enable bit is Set). When this bit is Set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is Cleared by hardware after the VC negotiation is complete (on exit from the FC_INIT2 state). For VC0, this bit is permitted to be hardwired to 0b. Before using a Virtual Channel, software must check whether the VC Negotiation Pending bits for that Virtual Channel are Clear in both components on the Link.	RO

7.9.1.9 VC Arbitration Table

The VC Arbitration Table is a read-write register array that is used to store the arbitration table for VC Arbitration. This register array is valid for all Functions when the selected VC Arbitration uses a WRR table. Functions that do not support WRR VC arbitration are not required to implement a VC Arbitration Table. If it exists, the VC Arbitration Table is located by the VC Arbitration Table Offset field.

The VC Arbitration Table is a register array with fixed-size entries of 4 bits. Figure 7-180 depicts the table structure of an example VC Arbitration Table with 32 phases. Each 4-bit table entry corresponds to a phase within a WRR arbitration period. The definition of table entry is depicted in Table 7-146 . The lower 3 bits (bits 0-2) contain the VC ID value, indicating that the corresponding phase within the WRR arbitration period is assigned to the Virtual Channel indicated by the VC ID (must be a valid VC ID that corresponds to an enabled VC).

The highest bit (bit 3) of the table entry is Reserved. The length of the table depends on the selected VC Arbitration as shown in Table 7-147 .

When the VC Arbitration Table is used by the default VC Arbitration method, the default values of the table entries must be all zero to ensure forward progress for the default VC (with VC ID of 0).

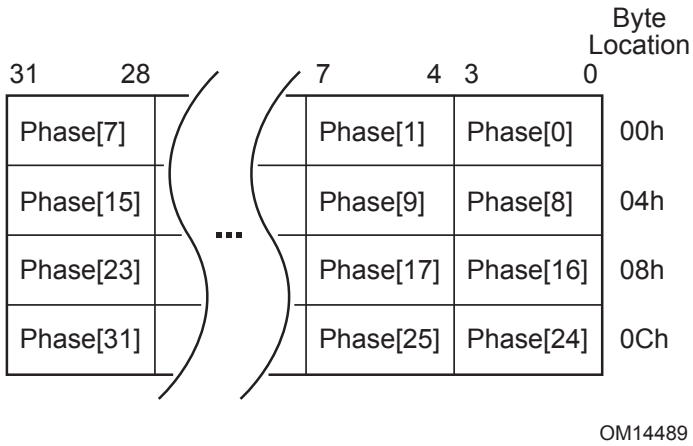

Figure 7-180 Example VC Arbitration Table with 32 Phases

Table 7-146 Definition of the 4-bit Entries in the VC Arbitration Table

Bit Location	Description	Attributes
2:0	VC ID	RW
3	RsvdP	RW

Table 7-147 Length of the VC Arbitration Table

VC Arbitration Select	VC Arbitration Table Length
001b	32 entries
010b	64 entries
011b	128 entries

7.9.1.10 Port Arbitration Table

The Port Arbitration Table register is a read-write register array that is used to store the WRR or time-based WRR arbitration table for Port Arbitration for the VC resource. This register array is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. It is only present when one or more asserted bits in the Port Arbitration Capability field indicate that the component supports a Port Arbitration scheme that uses a programmable arbitration table. Furthermore, it is only valid when one of the above-mentioned bits in the Port Arbitration Capability field is selected by the Port Arbitration Select field.

The Port Arbitration Table represents one Port arbitration period. Figure 7-181 shows the structure of an example Port Arbitration Table with 128 phases and 2-bit table entries. Each table entry containing a Port Number corresponds to a phase within a Port arbitration period. For example, a table with 2-bit entries can be used by a Switch component with up to four Ports. A Port Number written to a table entry indicates that the phase within the Port Arbitration period is assigned to the selected PCI Express Port (the Port Number must be a valid one).

- When the WRR Port Arbitration is used for a VC of any Egress Port, at each arbitration phase, the Port Arbiter serves one transaction from the Ingress Port indicated by the Port Number of the current phase. When

finished, it immediately advances to the next phase. A phase is skipped, i.e., the Port Arbiter simply moves to the next phase immediately if the Ingress Port indicated by the phase does not contain any transaction for the VC (note that a phase cannot contain the Egress Port's Port Number).

- When the Time-based WRR Port Arbitration is used for a VC of any given Port, at each arbitration phase aligning to a virtual timeslot, the Port Arbiter serves one transaction from the Ingress Port indicated by the Port Number of the current phase. It advances to the next phase at the next virtual timeslot. A phase indicates an “idle” timeslot, i.e., the Port Arbiter does not serve any transaction during the phase, if:
  - the phase contains the Egress Port's Port Number, or
  - the Ingress Port indicated by the phase does not contain any transaction for the VC.
  - The Port Arbitration Table Entry Size field in the Port VC Capability Register 1 determines the table entry size. The length of the table is determined by the Port Arbitration Select field as shown in Table 7-148 .
  - When the Port Arbitration Table is used by the default Port Arbitration for the default VC, the default values for the table entries must contain at least one entry for each of the other PCI Express Ports of the component to ensure forward progress for the default VC for each Port. The table may contain RR or RR-like fair Port Arbitration for the default VC.

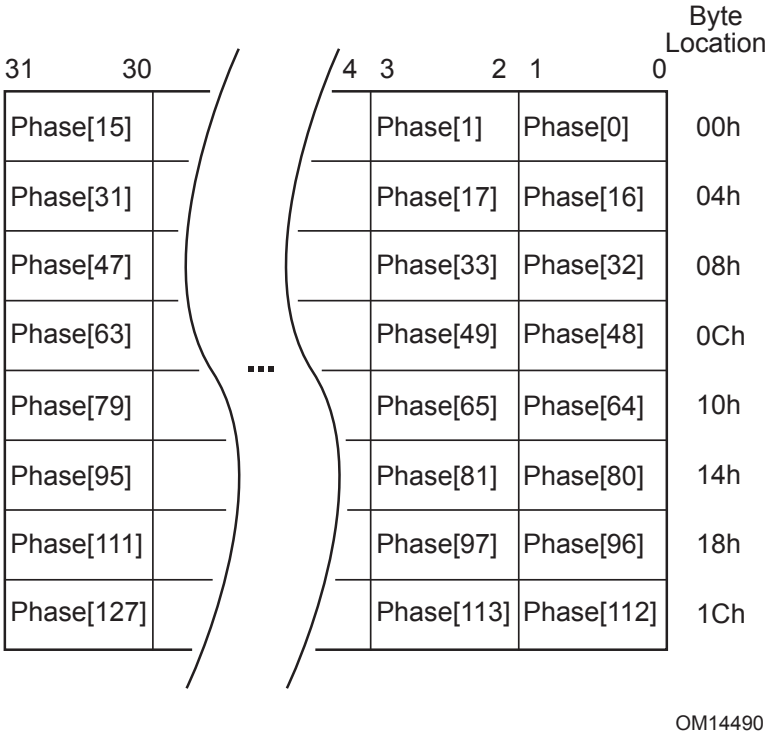

Figure 7-181 Example Port Arbitration Table with 128 Phases and 2-bit Table Entries

Table 7-148 Length of Port Arbitration Table

Port Arbitration Select	Port Arbitration Table Length
001b	32 entries
010b	64 entries
011b	128 entries

Port Arbitration Select	Port Arbitration Table Length
100b	128 entries
101b	256 entries

7.9.2 *Multi-Function Virtual Channel Extended Capability*

The Multi-Function Virtual Channel Extended Capability (***MFVC Capability***) is an optional Extended Capability that permits enhanced QoS management in a Multi-Function Device, including TC/VC mapping, optional VC arbitration, and optional Function arbitration for Upstream Requests. When implemented, the MFVC Capability structure must be present in the Extended Configuration Space of Function 0 of the Multi-Function Device's Upstream Port. Figure 7-182 provides a high level view of the MFVC Capability structure. This MFVC Capability structure controls Virtual Channel assignment at the PCI Express Upstream Port of the Multi-Function Device, while a VC Capability structure, if present in a Function, controls the Virtual Channel assignment for that individual Function.

The number of (extended) Virtual Channels is indicated by the Extended VC Count field in the Port VC Capability Register 1. Software must interpret this field to determine the availability of extended VC Resource registers.

A Multi-Function Device is permitted to have an MFVC Capability structure even if none of its Functions have a VC Capability structure. However, an MFVC Capability structure is permitted only in Function 0 in the Upstream Port of a Multi-Function Device.

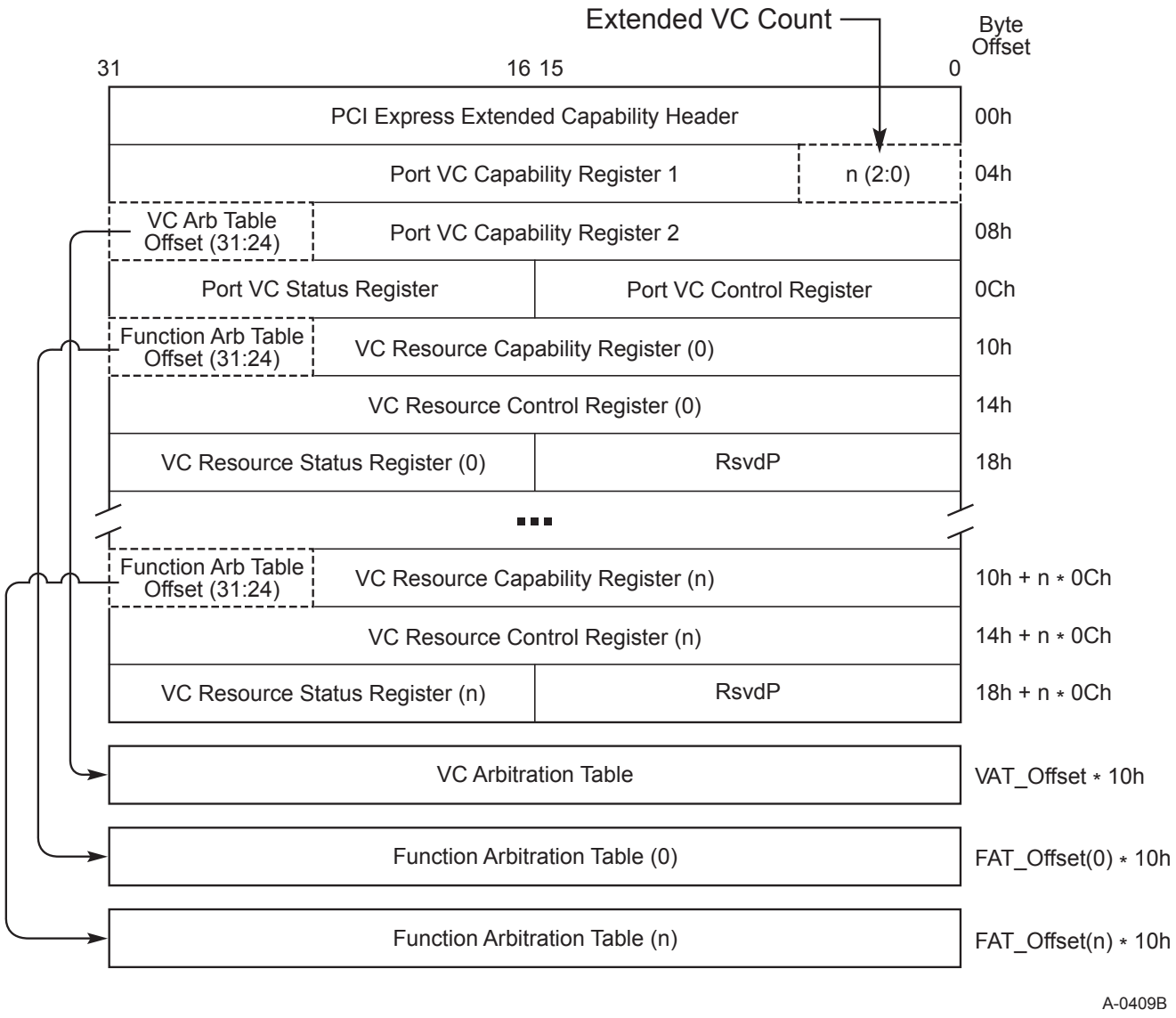

Figure 7-182 MFVC Capability Structure

The following sections describe the registers/fields of the MFVC Capability structure.

7.9.2.1 MFVC Extended Capability Header (Offset 00h)

Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. The Extended Capability ID for the MFVC Capability is 0008h. Figure 7-183 details allocation of register fields in the MFVC Extended Capability header; Table 7-149 provides the respective bit definitions.

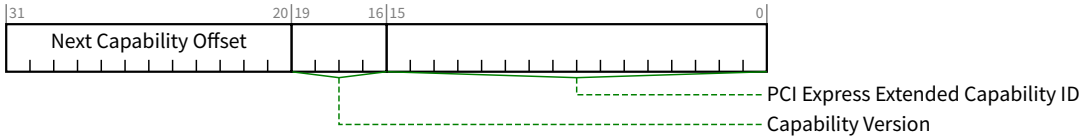

Figure 7-183 MFVC Extended Capability Header

Table 7-149 MFVC Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the MFVC Capability is 0008h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.2.2 MFVC Port VC Capability Register 1 (Offset 04h)

The MFVC Port VC Capability Register 1 describes the configuration of the Virtual Channels associated with a PCI Express Port of the Multi-Function Device. Figure 7-184 details allocation of register fields in the MFVC Port VC Capability Register 1; Table 7-150 provides the respective bit definitions.

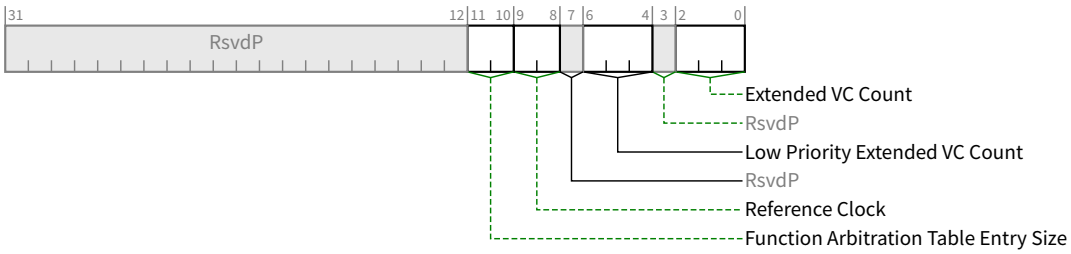

Figure 7-184 MFVC Port VC Capability Register 1

Table 7-150 MFVC Port VC Capability Register 1

Bit Location	Register Description	Attributes
2:0	***Extended VC Count*** - Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This value indicates the number of (extended) VC Resource Capability, Control, and Status registers that are present in Configuration Space in addition to the required VC Resource registers for the default VC. The minimum value of this field is 0 (for devices that only support the default VC and only have 1 set of VC Resource Registers for that VC). The maximum value is 7.	RO
6:4	***Low Priority Extended VC Count*** - Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The minimum value of this field is 000b and the maximum value is Extended VC Count.	RO
9:8	***Reference Clock*** - Indicates the reference clock for Virtual Channels that support time-based WRR Function Arbitration. Defined encodings are: **00b** 100 ns reference clock **01b - 11b** Reserved	RO
11:10	***Function Arbitration Table Entry Size*** - Indicates the size (in bits) of Function Arbitration table entry in the device. Defined encodings are: **00b** Size of Function Arbitration table entry is 1 bit **01b** Size of Function Arbitration table entry is 2 bits **10b** Size of Function Arbitration table entry is 4 bits **11b** Size of Function Arbitration table entry is 8 bits	RO

7.9.2.3 MFVC Port VC Capability Register 2 (Offset 08h)

The MFVC Port VC Capability Register 2 provides further information about the configuration of the Virtual Channels associated with a PCI Express Port of the Multi-Function Device. Figure 7-185 details allocation of register fields in the MFVC Port VC Capability Register 2; Table 7-151 provides the respective bit definitions.

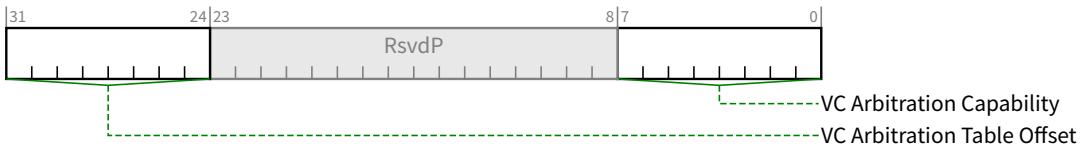

Figure 7-185 MFVC Port VC Capability Register 2

Table 7-151 MFVC Port VC Capability Register 2

Bit Location	Register Description	Attributes
7:0	***VC Arbitration Capability*** - Indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid for all devices that report a Low Priority Extended VC Count greater than 0. Each Bit Location within this field corresponds to a VC Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the device can be configured to provide different VC arbitration services. Defined bit positions are: **Bit 0** Hardware fixed arbitration scheme, e.g., Round Robin **Bit 1** Weighted Round Robin (WRR) arbitration with 32 phases **Bit 2** WRR arbitration with 64 phases **Bit 3** WRR arbitration with 128 phases **Bits 4-7** Reserved	RO
31:24	***VC Arbitration Table Offset*** - Indicates the location of the MFVC VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.	RO

7.9.2.4 MFVC Port VC Control Register (Offset 0Ch)

Figure 7-186 details allocation of register fields in the Port VC Control register; Table 7-152 provides the respective bit definitions.

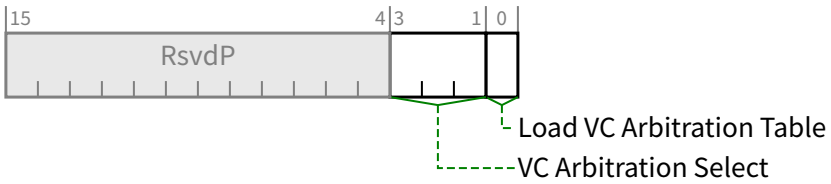

Figure 7-186 MFVC Port VC Control Register

Table 7-152 MFVC Port VC Control Register

Bit Location	Register Description	Attributes
0	***Load VC Arbitration Table*** - Used by software to update the MFVC VC Arbitration Table. This bit is valid when the selected VC Arbitration uses the MFVC VC Arbitration Table. Software Sets this bit to request hardware to apply new values programmed into MFVC VC Arbitration Table; Clearing this bit has no effect. Software checks the VC Arbitration Table Status bit to confirm that new values stored in the MFVC VC Arbitration Table are latched by the VC arbitration logic. This bit always returns 0b when read.	RW
3:1	***VC Arbitration Select*** - Used by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the MFVC Port VC Capability Register 2.	RW

Bit Location	Register Description	Attributes
	The permissible values of this field are numbers corresponding to one of the asserted bits in the VC Arbitration Capability field. This field cannot be modified when more than one VC in the LPVC group is enabled.	

7.9.2.5 MFVC Port VC Status Register (Offset 0Eh)

The MFVC Port VC Status Register provides status of the configuration of Virtual Channels associated with a Port of the Multi-Function Device. Figure 7-187 details allocation of register fields in the MFVC Port VC Status Register; Table 7-153 provides the respective bit definitions.

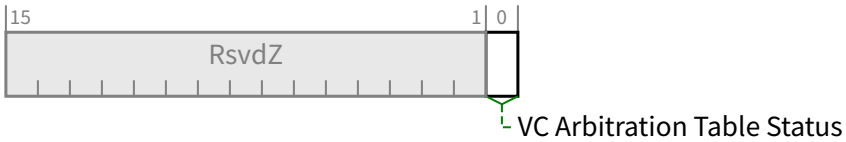

Figure 7-187 MFVC Port VC Status Register

Table 7-153 MFVC Port VC Status Register

Bit Location	Register Description	Attributes
0	***VC Arbitration Table Status*** - Indicates the coherency status of the MFVC VC Arbitration Table. This bit is valid when the selected VC uses the MFVC VC Arbitration Table. This bit is Set by hardware when any entry of the MFVC VC Arbitration Table is written by software. This bit is Cleared by hardware when hardware finishes loading values stored in the MFVC VC Arbitration Table after software sets the Load VC Arbitration Table bit in the MFVC Port VC Control Register. Default value of this bit is 0b.	RO

7.9.2.6 MFVC VC Resource Capability Register

The MFVC VC Resource Capability Register describes the capabilities and configuration of a particular Virtual Channel resource. Figure 7-188 details allocation of register fields in the MFVC VC Resource Capability Register; Table 7-154 provides the respective bit definitions.

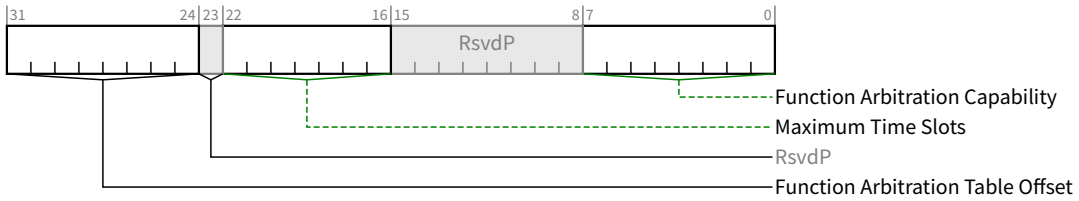

Figure 7-188 MFVC VC Resource Capability Register

Table 7-154 MFVC VC Resource Capability Register

Bit Location	Register Description	Attributes
7:0	***Function Arbitration Capability*** - Indicates types of Function Arbitration supported by the VC resource. Each Bit Location within this field corresponds to a Function Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Function Arbitration Select field (see Section 7.9.2.7). Defined bit positions are: **Bit 0** Non-configurable hardware-fixed arbitration scheme, e.g., Round Robin (RR) **Bit 1** Weighted Round Robin (WRR) arbitration with 32 phases **Bit 2** WRR arbitration with 64 phases **Bit 3** WRR arbitration with 128 phases **Bit 4** Time-based WRR with 128 phases **Bit 5** WRR arbitration with 256 phases **Bits 6-7** Reserved	RO
22:16	***Maximum Time Slots*** - Indicates the maximum number of time slots (minus 1) that the VC resource is capable of supporting when it is configured for time-based WRR Function Arbitration. For example, a value of 000 0000b in this field indicates the supported maximum number of time slots is 1 and a value of 111 1111b indicates the supported maximum number of time slots is 128. This field is valid only when the Function Arbitration Capability indicates that the VC resource supports time-based WRR Function Arbitration.	HwInit
31:24	***Function Arbitration Table Offset*** - Indicates the location of the Function Arbitration Table associated with the VC resource. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.	RO

7.9.2.7 MFVC VC Resource Control Register

Figure 7-189 details allocation of register fields in the MFVC VC Resource Control Register; Table 7-155 provides the respective bit definitions.

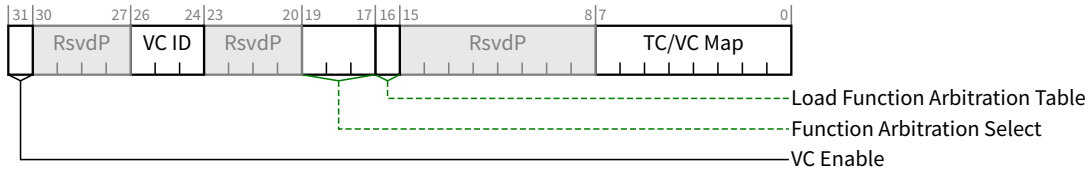

Figure 7-189 MFVC VC Resource Control Register

Table 7-155 MFVC VC Resource Control Register

Bit Location	Register Description	Attributes
7:0	***TC/VC Map*** - This field indicates the TCs that are mapped to the VC resource. Bit Locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.	RW (see the note for exceptions)
16	***Load Function Arbitration Table*** - When Set, this bit updates the Function Arbitration logic from the Function Arbitration Table for the VC resource. This bit is only valid when the Function Arbitration Table is used by the selected Function Arbitration scheme (that is indicated by a Set bit in the Function Arbitration Capability field selected by Function Arbitration Select). Software sets this bit to signal hardware to update Function Arbitration logic with new values stored in the Function Arbitration Table; clearing this bit has no effect. Software uses the Function Arbitration Table Status bit to confirm whether the new values of Function Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.	RW
19:17	***Function Arbitration Select*** - This field configures the VC resource to provide a particular Function Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Function Arbitration Capability field of the VC resource.	RW
26:24	***VC ID*** - This field assigns a VC ID to the VC resource (see note for exceptions). This field cannot be modified when the VC is already enabled. Note: For the first VC resource (default VC), this field is a read-only field that must be hardwired to 000b.	RW
31	***VC Enable*** - When Set, this bit enables a Virtual Channel (see note 1 for exceptions). The Virtual Channel is disabled when this bit is cleared. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. Default value of this bit is 1b for the first VC resource and 0b for other VC resource(s).	RW

Bit Location	Register Description	Attributes
	Notes: 1. This bit is hardwired to 1b for the default VC (VC0), i.e., writing to this field has no effect for VC0. 2. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Set in both components on a Link. 3. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Cleared in both components on a Link. 4. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 5. Software must fully disable a Virtual Channel in both components on a Link before re-enabling the Virtual Channel.	

7.9.2.8 MFVC VC Resource Status Register

Figure 7-190 details allocation of register fields in the MFVC VC Resource Status Register; Table 7-156 provides the respective bit definitions.

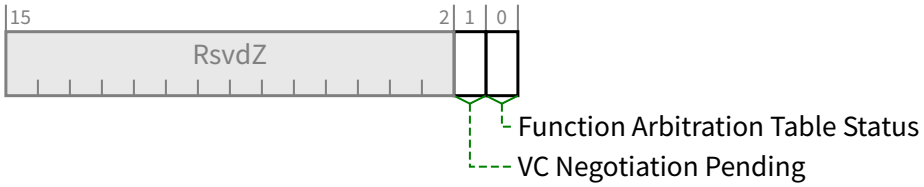

Figure 7-190 MFVC VC Resource Status Register

Table 7-156 MFVC VC Resource Status Register

Bit Location	Register Description	Attributes
0	***Function Arbitration Table Status*** - This bit indicates the coherency status of the Function Arbitration Table associated with the VC resource. This bit is valid only when the Function Arbitration Table is used by the selected Function Arbitration for the VC resource. This bit is Set by hardware when any entry of the Function Arbitration Table is written to by software. This bit is Cleared by hardware when hardware finishes loading values stored in the Function Arbitration Table after software sets the Load Function Arbitration Table bit. Default value of this bit is 0b.	RO
1	***VC Negotiation Pending*** - This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. When this bit is Set by hardware, it indicates that the VC resource is still in the process of negotiation. This bit is Cleared by hardware after the VC negotiation is complete. For a non-default Virtual Channel, software may use this bit when enabling or disabling the VC. For the default VC, this bit indicates the status of the process of Flow Control initialization.	RO

Bit Location	Register Description	Attributes
	Before using a Virtual Channel, software must check whether the VC Negotiation Pending bits for that Virtual Channel are Clear in both components on a Link.	

7.9.2.9 MFVC VC Arbitration Table

The definition of the MFVC VC Arbitration Table in the MFVC Capability structure is identical to that in the VC Capability structure (see Section 7.9.1.9).

7.9.2.10 Function Arbitration Table

The Function Arbitration Table register in the MFVC Capability structure takes the same form as the Port Arbitration Table register in the VC Capability structure (see Section 7.9.1.10).

The Function Arbitration Table register is a read-write register array that is used to store the WRR or time-based WRR arbitration table for Function Arbitration for the VC resource. It is only present when one or more asserted bits in the Function Arbitration Capability field indicate that the Multi-Function Device supports a Function Arbitration scheme that uses a programmable arbitration table. Furthermore, it is only valid when one of the above-mentioned bits in the Function Arbitration Capability field is selected by the Function Arbitration Select field.

The Function Arbitration Table represents one Function arbitration period. Each table entry containing a Function Number or Function Group[155] Number corresponds to a phase within a Function Arbitration period. The table entry size requirements are as follows:

- The table entry size for non-ARI devices must support enough values to specify all implemented Functions plus at least one value that does not correspond to an implemented Function. For example, a table with 2-bit entries can be used by a Multi-Function Device with up to three Functions.
- The table entry size for ARI Devices must be either 4 bits or 8 bits.
  - If MFVC Function Groups are enabled, each entry maps to a single Function Group. Arbitration between multiple Functions within a Function Group is implementation specific, but must guarantee forward progress.
  - If MFVC Function Groups are not enabled and 4-bit entries are implemented, a given entry maps to all Functions whose Function Number modulo 8 matches its value. Similarly, if 8-bit entries are implemented, a given entry maps to all Functions whose Function Number modulo 128 matches its value. If a given entry maps to multiple Functions, arbitration between those Functions is implementation specific, but must guarantee forward progress.

A Function Number or Function Group Number written to a table entry indicates that the phase within the Function Arbitration period is assigned to the selected Function or Function Group (the Function Number or Function Group Number must be a valid one).

- When the WRR Function Arbitration is used for a VC of the Egress Port of the Multi-Function Device, at each arbitration phase the Function Arbiter serves one transaction from the Function or Function Group indicated by the Function Number or Function Group Number of the current phase. When finished, it immediately advances to the next phase. A phase is skipped, i.e., the Function Arbiter simply moves to the next phase immediately if the Function or Function Group indicated by the phase does not contain any transaction for the VC.

155. If an ARI Device supports MFVC Function Groups capability and ARI-aware software enables it, arbitration is based on Function Groups instead of Functions. See Section 7.8.7 .

- When the Time-based WRR Function Arbitration is used for a VC of the Egress Port of the Multi-Function Device, at each arbitration phase aligning to a virtual timeslot, the Function Arbiter serves one transaction from the Function or Function Group indicated by the Function Number or Function Group Number of the current phase. It advances to the next phase at the next virtual timeslot. A phase indicates an “idle” timeslot, i.e., the Function Arbiter does not serve any transaction during the phase, if:
  - the phase contains the Number of a Function or a Function Group that does not exist, or
  - the Function or Function Group indicated by the phase does not contain any transaction for the VC.

The Function Arbitration Table Entry Size field in the MFVC Port VC Capability Register 1 determines the table entry size. The length of the table is determined by the Function Arbitration Select field as shown in Table 7-157 .

When the Function Arbitration Table is used by the default Function Arbitration for the default VC, the default values for the table entries must contain at least one entry for each of the active Functions or Function Groups in the Multi-Function Device to ensure forward progress for the default VC for the Multi-Function Device’s Upstream Port. The table may contain RR or RR-like fair Function Arbitration for the default VC.

Table 7-157 Length of Function Arbitration Table

Function Arbitration Select	Function Arbitration Table Length
001b	32 entries
010b	64 entries
011b	128 entries
100b	128 entries
101b	256 entries

7.9.3 Device Serial Number Extended Capability

The Device Serial Number Extended Capability is an optional Extended Capability that may be implemented by any PCI Express device Function. The Device Serial Number is a read-only 64-bit value that is unique for a given PCI Express device. Figure 7-191 details allocation of register fields in the Device Serial Number Extended Capability structure.

It is permitted but not recommended for RCiEPs to implement this Capability.

RCiEPs that implement this Capability are permitted but not required to return the same Device Serial Number value as that reported by other RCiEPs of the same Root Complex.

All Multi-Function DeviceDevices other than RCiEPs that implement this Capability must implement it for Function 0; other Functions that implement this Capability must return the same Device Serial Number value as that reported by Function 0.

RCiEPs are permitted to implement or not implement this Capability on an individual basis, independent of whether they are part of a Multi-Function Device.

A PCI Express component other than a Root Complex containing multiple Devices such as a PCI Express Switch that implements this Capability must return the same Device Serial Number for each device.

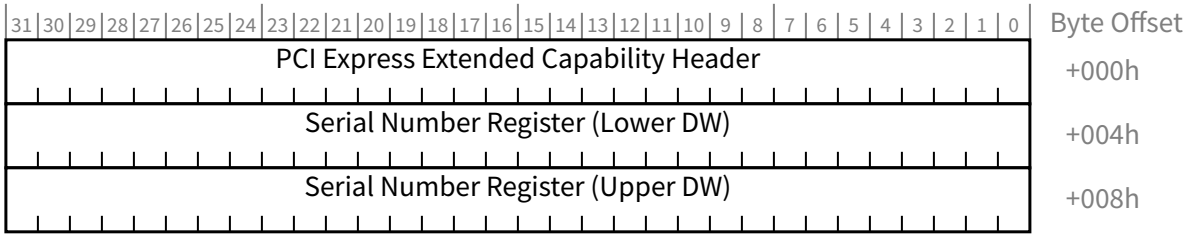

Figure 7-191 Device Serial Number Extended Capability Structure

7.9.3.1 Device Serial Number Extended Capability Header (Offset 00h)

Figure 7-192 details allocation of register fields in the Device Serial Number Extended Capability Header; Table 7-158 provides the respective bit definitions. Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. The Extended Capability ID for the Device Serial Number Extended Capability is 0003h.

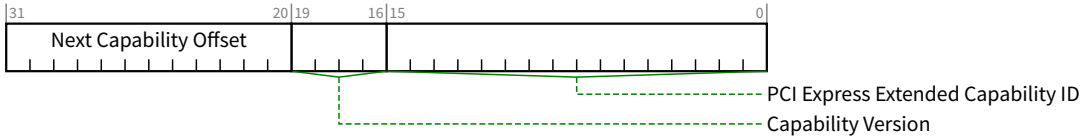

Figure 7-192 Device Serial Number Extended Capability Header

Table 7-158 Device Serial Number Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Device Serial Number Extended Capability is 0003h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.3.2 Serial Number Register (Offset 04h)

The Serial Number register is a 64-bit field that contains the IEEE defined 64-bit extended unique identifier [EUI-64]. Figure 7-193 details allocation of register fields in the Serial Number register; Table 7-159 provides the respective bit definitions.

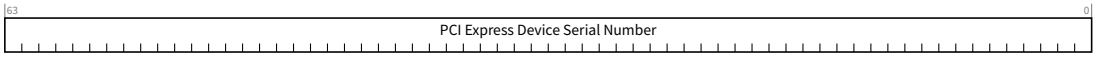

Figure 7-193 Serial Number Register

Table 7-159 Serial Number Register

Bit Location	Register Description	Attributes
63:0	***PCI Express Device Serial Number*** - This field contains the IEEE defined 64-bit Extended Unique Identifier [EUI-64]. This identifier includes a 24-bit company id value assigned by IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. PCI Express Device Serial Number[07:00] = EUI[63:56] PCI Express Device Serial Number[15:08] = EUI[55:48] PCI Express Device Serial Number[23:16] = EUI[47:40] PCI Express Device Serial Number[31:24] = EUI[39:32] PCI Express Device Serial Number[39:32] = EUI[31:24] PCI Express Device Serial Number[47:40] = EUI[23:16] PCI Express Device Serial Number[55:48] = EUI[15:08] PCI Express Device Serial Number[63:56] = EUI[07:00]	RO

7.9.4 Vendor-Specific Capability

The Vendor-Specific Capability is a capability structure in PCI-compatible Configuration Space (first 256 bytes) as shown in Figure 7-194 .

The Vendor-Specific Capability allows device vendors to use the Capability mechanism for vendor-specific information. The layout of the information is vendor-specific, except for the first three bytes, as explained below.

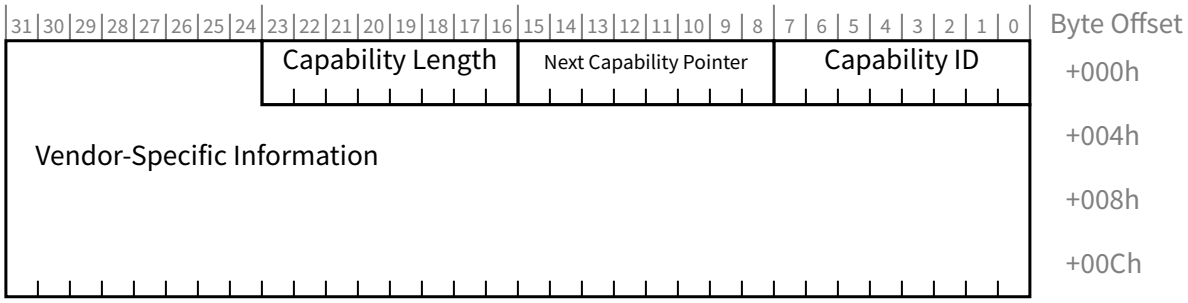

Figure 7-194 Vendor-Specific Capability

Table 7-160 Vendor-Specific Capability

Bit Location	Register Description	Attributes
7:0	***Capability ID*** - Indicates the PCI Express Capability structure. This field must return a Capability ID of 09h indicating that this is a Vendor-Specific Capability structure.	RO
15:8	***Next Capability Pointer*** - This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities.	RO
23:16	***Capability Length*** - This field provides the number of bytes in the Capability structure (including the three bytes consumed by the Capability ID, Next Capability Pointer, and Capability Length field).	RO
31:24	***Vendor Specific Information***	Vendor Specific

7.9.5 *Vendor-Specific Extended Capability*

The Vendor-Specific Extended Capability (***VSEC Capability***) is an optional Extended Capability that is permitted to be implemented by any PCI Express Function or RCRB. This allows PCI Express component vendors to use the Extended Capability mechanism to expose vendor-specific registers.

A single PCI Express Function or RCRB is permitted to contain multiple VSEC structures.

An example usage is a set of vendor-specific features that are intended to go into an on-going series of components from that vendor. A VSEC structure can tell vendor-specific software which features a particular component supports, including components developed after the software was released.

Figure 7-195 details allocation of register fields in the VSEC structure. The structure of the Vendor-Specific Extended Capability Header and the Vendor-Specific Header is architected by this specification.

With a PCI Express Function, the structure and definition of the vendor-specific Registers area is determined by the vendor indicated by the Vendor ID field located at byte offset 00h in PCI-compatible Configuration Space. With an RCRB, a VSEC is permitted only if the RCRB also contains an RCRB Header Extended Capability structure, which contains a Vendor ID field indicating the vendor.

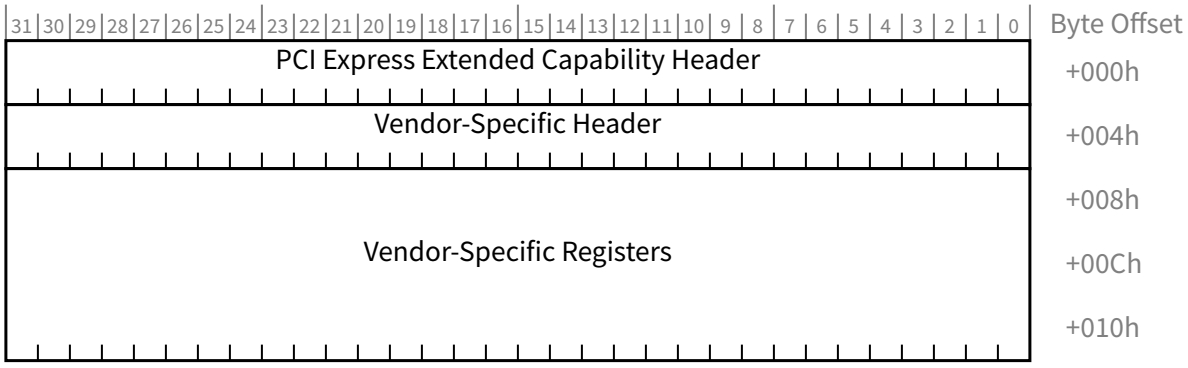

Figure 7-195 VSEC Capability Structure

7.9.5.1 Vendor-Specific Extended Capability Header (Offset 00h)

Figure 7-196 details allocation of register fields in the Vendor-Specific Extended Capability Header; Table 7-161 provides the respective bit definitions. Refer to Section 7.6.3 for a description of the PCI Express Extended Capability Header. The Extended Capability ID for the Vendor-Specific Extended Capability is 000Bh.

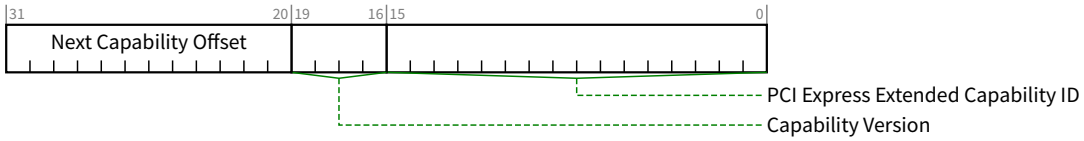

Figure 7-196 Vendor-Specific Extended Capability Header

Table 7-161 Vendor-Specific Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Vendor-Specific Extended Capability is 000Bh.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.5.2 Vendor-Specific Header (Offset 04h)

Figure 7-197 details allocation of register fields in the Vendor-Specific Header; Table 7-162 provides the respective bit definitions.

Vendor-specific software must qualify the associated Vendor ID of the PCI Express Function or RCRB before attempting to interpret the values in the VSEC ID or VSEC Rev fields.

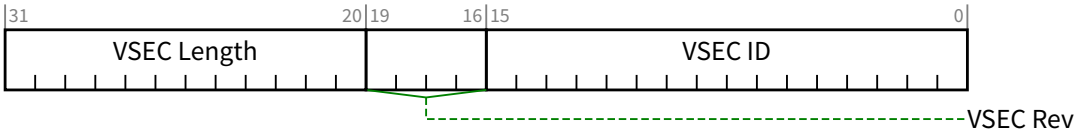

Figure 7-197 Vendor-Specific Header

Table 7-162 Vendor-Specific Header

Bit Location	Register Description	Attributes
15:0	***VSEC ID*** - This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.	RO
19:16	***VSEC Rev*** - This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.	RO
31:20	***VSEC Length*** - This field indicates the number of bytes in the entire VSEC structure, including the Vendor-Specific Extended Capability Header, the Vendor-Specific Header, and the vendor-specific registers.	RO

7.9.6 *Designated Vendor-Specific Extended Capability* (DVSEC)

The Designated Vendor-Specific Extended Capability (***DVSEC Capability***) is an optional Extended Capability that is permitted to be implemented by any PCI Express Function or RCRB. This allows PCI Express component vendors to use the Extended Capability mechanism to expose vendor-specific registers that can be present in components by a variety of vendors.

A single PCI Express Function or RCRB is permitted to contain multiple DVSEC Capability structures.

An example usage is a set of vendor-specific features that are intended to go into an on-going series of components from a collection of vendors. A DVSEC Capability structure can tell vendor-specific software which features a particular component supports, including components developed after the software was released.

Figure 7-198 details allocation of register fields in the DVSEC Capability structure. The structure of the PCI Express Extended Capability Header and the Designated Vendor-Specific header is architected by this specification.

The DVSEC Vendor-Specific Register area begins at offset 0Ah.

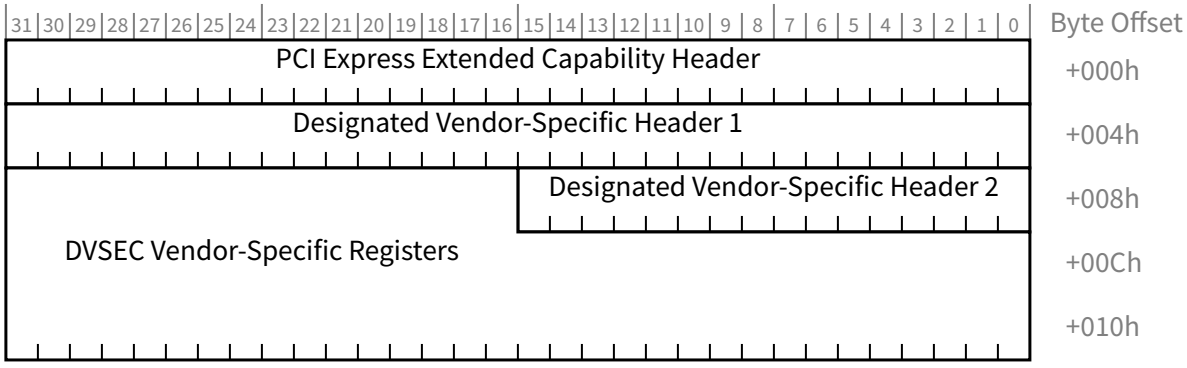

Figure 7-198 Designated Vendor-Specific Extended Capability

7.9.6.1 Designated Vendor-Specific Extended Capability Header (Offset 00h)

Figure 7-199 details allocation of register fields in the Designated Vendor-Specific Extended Capability Header; Table 7-163 provides the respective bit definitions. Refer to Section 7.9.3 for a description of the PCI Express Extended Capability Header. The Extended Capability ID for the Designated Vendor-Specific Extended Capability is 0023h.

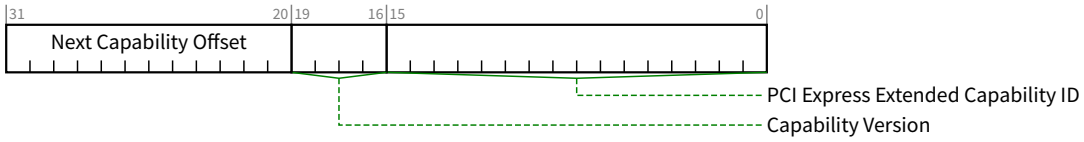

Figure 7-199 Designated Vendor-Specific Extended Capability Header

Table 7-163 Designated Vendor-Specific Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Designated Vendor-Specific Extended Capability is 0023h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.6.2 Designated Vendor-Specific Header 1 (Offset 04h)

Figure 7-200 details allocation of register fields in the Designated Vendor-Specific Header 1; Table 7-164 provides the respective bit definitions.

Vendor-specific software must qualify the DVSEC Vendor ID before attempting to interpret the DVSEC Revision field.

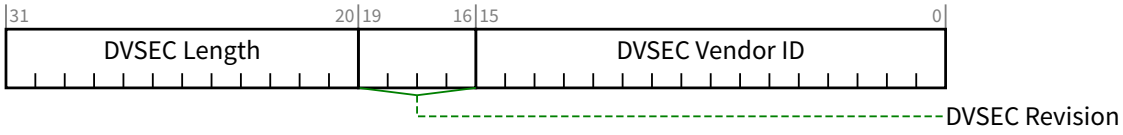

Figure 7-200 Designated Vendor-Specific Header 1

Table 7-164 Designated Vendor-Specific Header 1

Bit Location	Register Description	Attributes
15:0	***DVSEC Vendor ID*** - This field is the Vendor ID associated with the vendor that defined the contents of this capability.	RO
19:16	***DVSEC Revision*** - This field is a vendor-defined version number that indicates the version of the DVSEC structure. Software must qualify the DVSEC Vendor ID and DVSEC ID before interpreting this field.	RO
31:20	***DVSEC Length*** - This field indicates the number of bytes in the entire DVSEC structure, including the PCI Express Extended Capability Header, the DVSEC Header 1, DVSEC Header 2, and DVSEC vendor-specific registers.	RO

7.9.6.3 Designated Vendor-Specific Header 2 (Offset 08h)

Figure 7-201 details allocation of register fields in the Designated Vendor-Specific Header 2; Table 7-165 provides the respective bit definitions.

Vendor-specific software must qualify the DVSEC Vendor ID before attempting to interpret the DVSEC ID field.

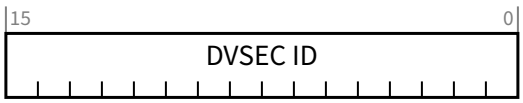

Figure 7-201 Designated Vendor-Specific Header 2

Table 7-165 Designated Vendor-Specific Header 2

Bit Location	Register Description	Attributes
15:0	***DVSEC ID*** - This field is a vendor-defined ID that indicates the nature and format of the DVSEC structure. Software must qualify the DVSEC Vendor ID before interpreting this field.	RO

7.9.7 RCRB Header Extended Capability

The PCI Express RCRB Header Extended Capability is an optional Extended Capability that may be implemented in an RCRB to provide a Vendor ID and Device ID for the RCRB and to permit the management of parameters that affect the behavior of Root Complex functionality associated with the RCRB.

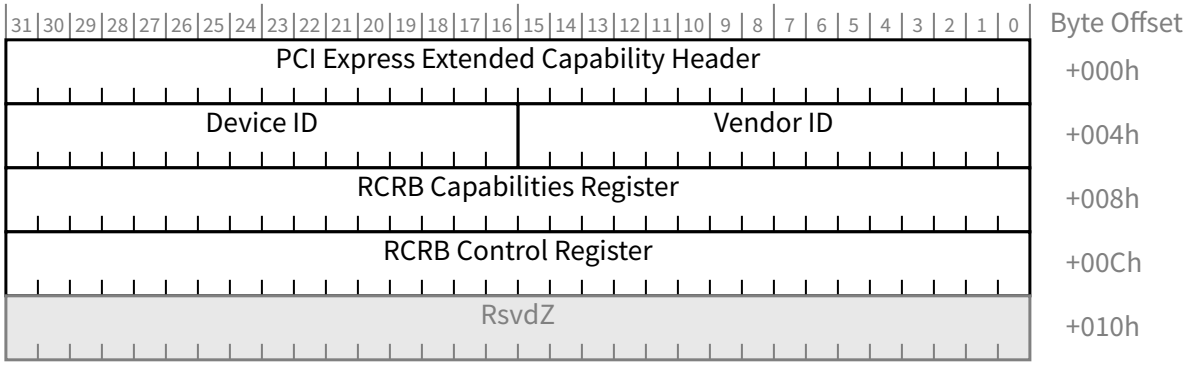

Figure 7-202 RCRB Header Extended Capability Structure

7.9.7.1 RCRB Header Extended Capability Header (Offset 00h)

Figure 7-203 details allocation of register fields in the RCRB Header Extended Capability Header. Table 7-166 provides the respective bit definitions. Refer to Section 7.6.3 for a description of the PCI Express Enhanced Capabilities header. The Extended Capability ID for the RCRB Header Extended Capability is 000Ah.

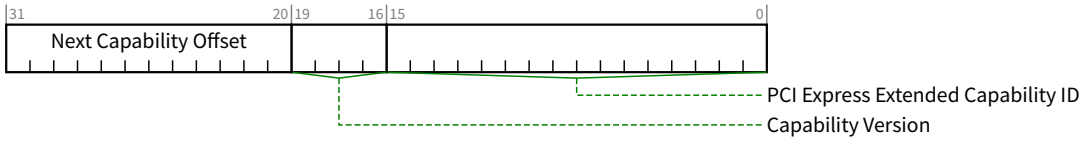

Figure 7-203 RCRB Header Extended Capability Header

Table 7-166 RCRB Header Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the RCRB Header Extended Capability is 000Ah.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.7.2 RCRB Vendor ID and Device ID register (Offset 04h)

Figure 7-204 details allocation of register fields in the RCRB Vendor ID and Device ID register; Table 7-167 provides the respective bit definitions.

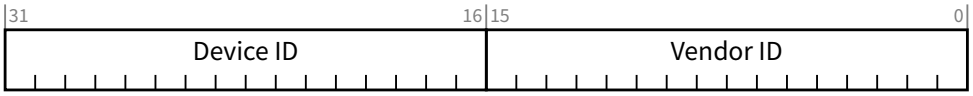

Figure 7-204 RCRB Vendor ID and Device ID register

Table 7-167 RCRB Vendor ID and Device ID register

Bit Location	Register Description	Attributes
15:0	***Vendor ID*** - PCI-SIG assigned. Analogous to the equivalent field in PCI-compatible Configuration Space. This field provides a means to associate an RCRB with a particular vendor.	RO
31:16	***Device ID*** - Vendor assigned. Analogous to the equivalent field in PCI-compatible Configuration Space. This field provides a means for a vendor to classify a particular RCRB.	RO

7.9.7.3 RCRB Capabilities register (Offset 08h)

Figure 7-205 details allocation of register fields in the RCRB Capabilities register; Table 7-168 provides the respective bit definitions.

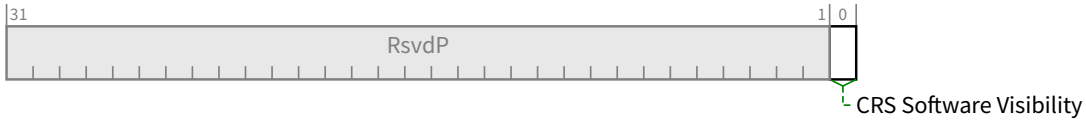

Figure 7-205 RCRB Capabilities register

Table 7-168 RCRB Capabilities register

Bit Location	Register Description	Attributes
0	***CRS Software Visibility*** - When Set, this bit indicates that the Root Complex is capable of returning Configuration Request Retry Status (CRS) Completion Status to software for all Root Ports and integrated devices associated with this RCRB (see Section 2.3.1).	RO

7.9.7.4 RCRB Control register (Offset 0Ch)

Figure 7-206 details allocation of register fields in the RCRB Control register; Table 7-169 provides the respective bit definitions.

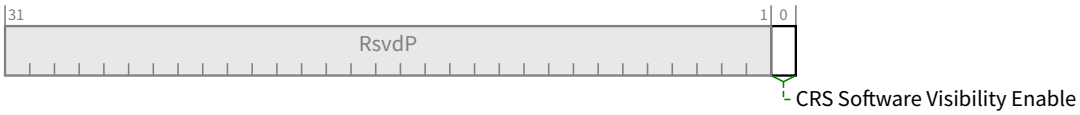

Figure 7-206 RCRB Control register

Table 7-169 RCRB Control register

Bit Location	Register Description	Attributes
0	***CRS Software Visibility Enable*** - When Set, this bit enables the Root Complex to return Configuration Request Retry Status (CRS) Completion Status to software for all Root Ports and integrated devices associated with this RCRB (see Section 2.3.1). RCRBs that do not implement this capability must hardwire this bit to 0b. Default value of this bit is 0b.	RW

7.9.8 Root Complex Link Declaration Extended Capability

The Root Complex Link Declaration Extended Capability is an optional Capability that is permitted to be implemented by Root Ports, RCiEPs, or RCRBs to declare a Root Complex's internal topology.

A Root Complex consists of one or more following elements:

- PCI Express Root Port
- A default system Egress Port or an internal sink unit such as memory (represented by an RCRB)
- Internal Data Paths/Links (represented by an RCRB on either side of an internal Link)
- Integrated devices
- Functions

A Root Complex Component is a logical aggregation of the above described Root Complex elements. No single element can be part of more than one Root Complex Component. Each Root Complex Component must have a unique Component ID.

A Root Complex is represented either as an opaque Root Complex or as a collection of one or more Root Complex Components.

The Root Complex Link Declaration Extended Capability is permitted to be present in a Root Complex element's Configuration Space or RCRB. It declares Links from the respective element to other elements of the same Root Complex Component or to an element in another Root Complex Component. The Links are required to be declared bidirectional such that each valid data path from one element to another has corresponding Link Entries in the Configuration Space (or RCRB) of both elements.

The Root Complex Link Declaration Extended Capability is permitted to also declare an association between a Configuration Space element (Root Port or RCiEP) and an RCRB Header Extended Capability (see Section 7.9.7) contained in an RCRB that affects the behavior of the Configuration Space element. Note that an RCRB Header association is not declared bidirectional; the association is only declared by the Configuration Space element and not by the target RCRB.

IMPLEMENTATION NOTE
Topologies to Avoid

Topologies that create more than one data path between any two Root Complex elements (either directly or through other Root Complex elements) may not be able to support bandwidth allocation in a standard manner. The description of how traffic is routed through such a topology is implementation specific, meaning that general purpose-operating systems may not have enough information about such a topology to correctly support bandwidth allocation. In order to circumvent this problem, these operating systems may require that a single RCRB element (of type Internal Link) not declare more than one Link to a Root Complex Component other than the one containing the RCRB element itself.

The Root Complex Link Declaration Extended Capability, as shown in Figure 7-207 , consists of the PCI Express Extended Capability header and Root Complex Element Self Description followed by one or more Root Complex Link Entries.

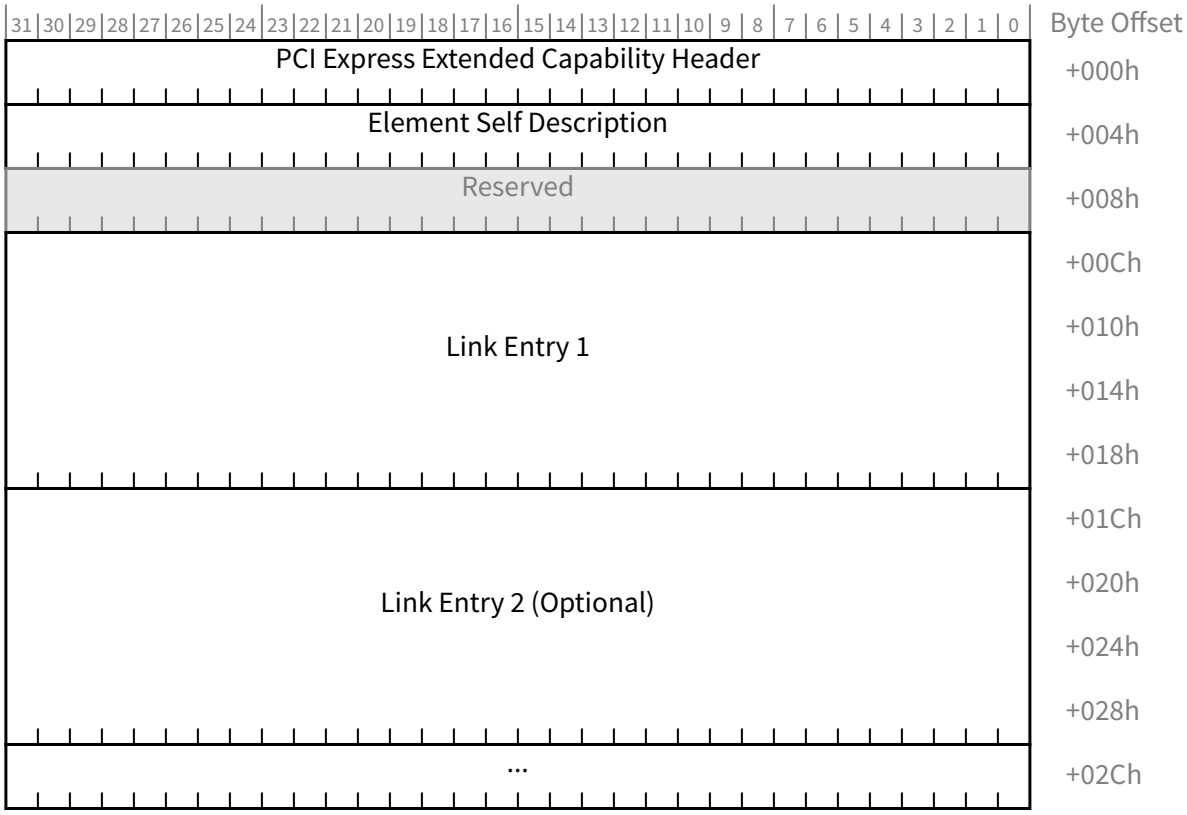

Figure 7-207 Root Complex Link Declaration Extended Capability

7.9.8.1 Root Complex Link Declaration Extended Capability Header (Offset 00h)

The Extended Capability ID for the Root Complex Link Declaration Extended Capability is 0005h.

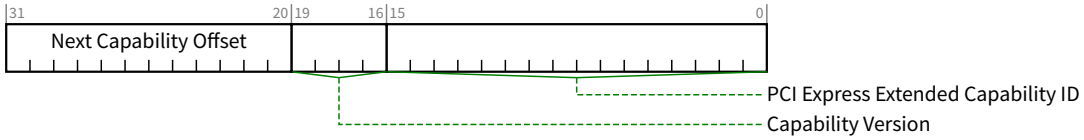

Figure 7-208 Root Complex Link Declaration Extended Capability Header

Table 7-170 Root Complex Link Declaration Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Root Complex Link Declaration Extended Capability is 0005h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.	RO

7.9.8.2 Element Self Description Register (Offset 04h)

The Element Self Description Register provides information about the Root Complex element containing the Root Complex Link Declaration Extended Capability.

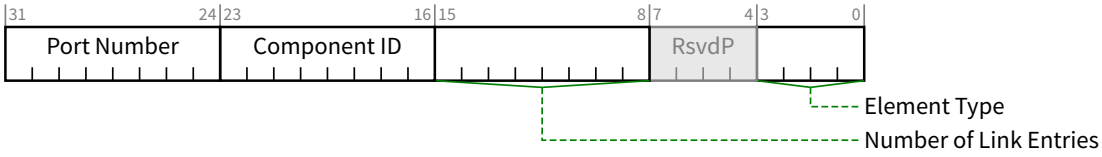

Figure 7-209 Element Self Description Register

Table 7-171 Element Self Description Register

Bit Location	Register Description	Attributes
3:0	***Element Type*** - This field indicates the type of the Root Complex Element. Defined encodings are:	RO

Bit Location	Register Description	Attributes
	0h Configuration Space Element **1h** System Egress Port or internal sink (memory) **2h** Internal Root Complex Link **3h-Fh** Reserved	
15:8	***Number of Link Entries*** - This field indicates the number of Link Entries following the Element Self Description. This field must report a value of 01h or higher.	HwInit
23:16	***Component ID*** - This field identifies the Root Complex Component that contains this Root Complex Element. Component IDs must start at 01h, as a value of 00h is Reserved.	HwInit
31:24	***Port Number*** - This field specifies the Port Number associated with this element with respect to the Root Complex Component that contains this element. An element with a Port Number of 00h indicates the default Egress Port to configuration software.	HwInit

7.9.8.3 Link Entries

Link Entries start at offset 10h of the Root Complex Link Declaration Extended Capability structure. Each Link Entry consists of a Link description followed by a 64-bit Link Address at offset 08h from the start of Link Entry identifying the target element for the declared Link. A Link Entry declares an internal Link to another Root Complex Element.

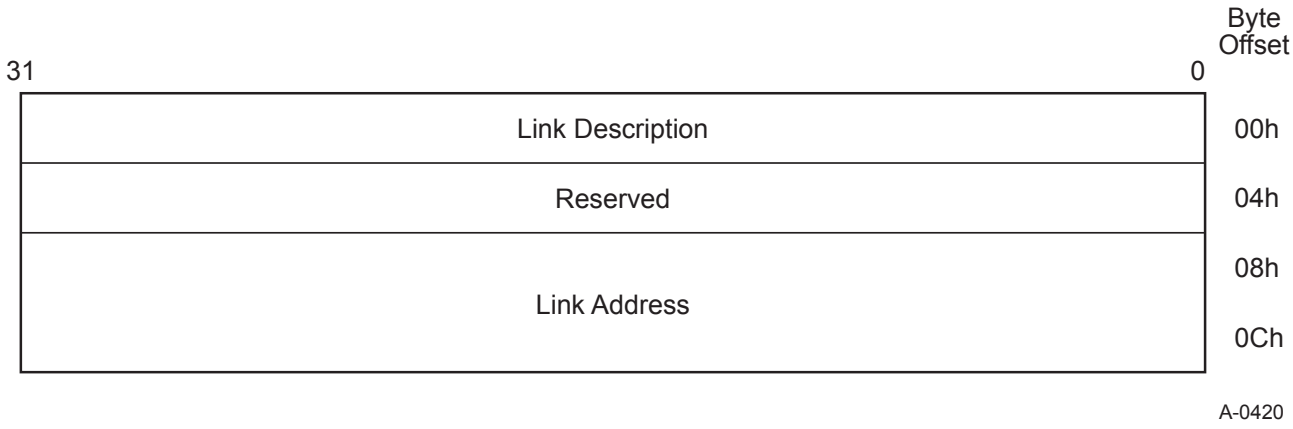

Figure 7-210 Link Entry

7.9.8.3.1 Link Description Register

The Link Description Register is located at offset 00h from the start of a Link Entry and is defined as follows:

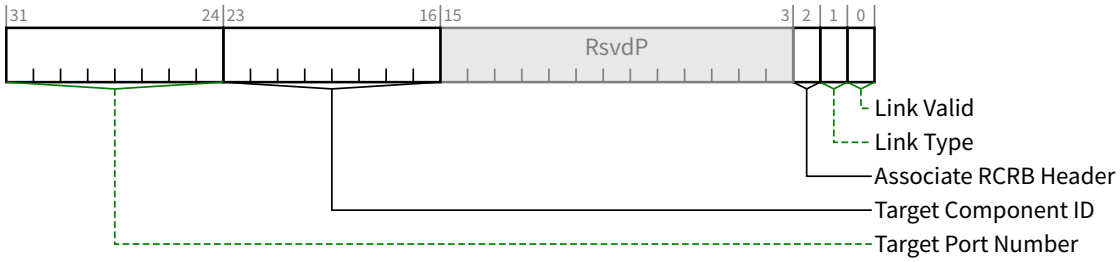

Figure 7-211 Link Description Register

Table 7-172 Link Description Register

Bit Location	Register Description	Attributes
0	***Link Valid*** - When Set, this bit indicates that the Link Entry specifies a valid Link. Link Entries that do not have either this bit Set or the Associate RCRB Header bit Set (or both) are ignored by software.	HwInit
1	***Link Type*** - This bit indicates the target type of the Link and defines the format of the Link Address field. Defined Link Type values are: **0b** Link points to memory-mapped space[156] (for RCRB). The Link Address specifies the 64-bit base address of the target RCRB. **1b** Link points to Configuration Space (for a Root Port or RCiEP). The Link Address specifies the configuration address (PCI Segment Group, Bus, Device, Function) of the target element.	HwInit
2	***Associate RCRB Header*** - When Set, this bit indicates that the Link Entry associates the declaring element with an RCRB Header Extended Capability in the target RCRB. Link Entries that do not have either this bit Set or the Link Valid bit Set (or both) are ignored by software. The Link Type bit must be Clear when this bit is Set.	HwInit
23:16	***Target Component ID*** - This field identifies the Root Complex Component that is targeted by this Link Entry. Components IDs must start at 01h, as a value of 00h is Reserved	HwInit
31:24	***Target Port Number*** - This field specifies the Port Number associated with the element targeted by this Link Entry; the Target Port Number is with respect to the Root Complex Component (identified by the Target Component ID) that contains the target element.	HwInit

7.9.8.3.2 *Link Address*

The Link Address is a HwInit field located at offset 08h from the start of a Link Entry that identifies the target element for the Link Entry. For a Link of Link Type 0 in its Link Description, the Link Address specifies the memory-mapped base address of RCRB. For a Link of Link Type 1 in its Link Description, the Link Address specifies the Configuration Space address of a PCI Express Root Port or an RCiEP.

156. The memory-mapped space for accessing an RCRB is not the same as Memory Space, and must not overlap with Memory Space.

7.9.8.3.2.1 *Link Address for Link Type 0*

For a Link pointing to a memory-mapped RCRB (Link Type bit = 0), the first DWORD specifies the lower 32 bits of the RCRB base address of the target element as shown below; bits 11:0 are hardwired to 000h and Reserved for future use. The second DWORD specifies the high order 32 bits (63:32) of the RCRB base address of the target element.

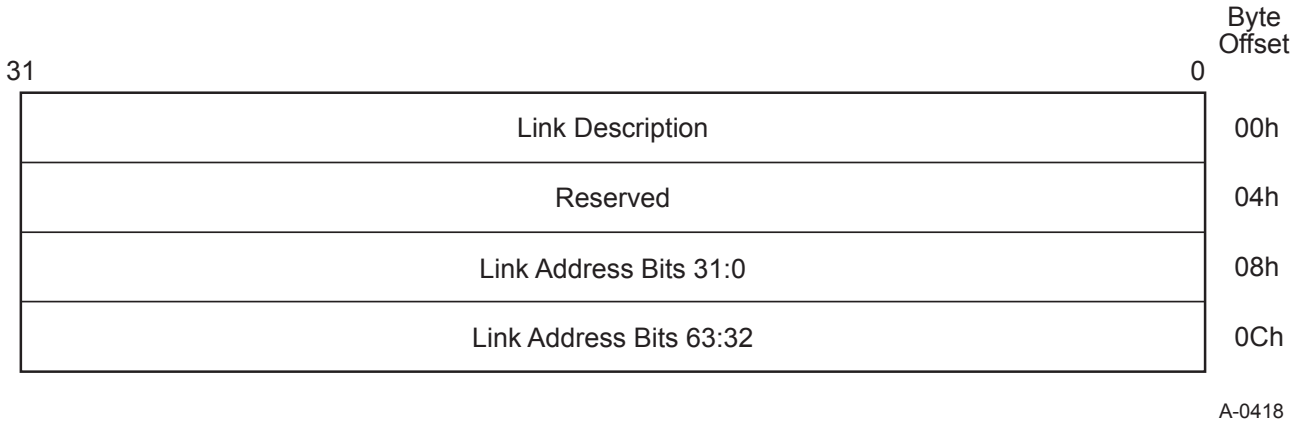

Figure 7-212 Link Address for Link Type 0

7.9.8.3.2.2 *Link Address for Link Type 1*

For a Link pointing to the Configuration Space of a Root Complex element (Link Type bit = 1), bits in the first DWORD specify the Bus, Device, and Function Number of the target element. As shown in Figure 7-213 , bits 2:0 (N) encode the number of bits n associated with the Bus Number, with N = 000b specifying $n = 8$ and all other encodings specifying n = <value of N>. Bits 11:3 are Reserved and hardwired to 0. Bits 14:12 specify the Function Number, and bits 19:15 specify the Device Number. Bits $(19 + n)$:20 specify the Bus Number, with $1 \le n \le 8$.

Bits 31:$(20 + n)$ of the first DWORD together with the second DWORD optionally identify the target element's hierarchy for systems implementing the PCI Express Enhanced Configuration Access Mechanism by specifying bits 63:$(20 + n)$ of the memory-mapped Configuration Space base address of the PCI Express hierarchy associated with the targeted element; single hierarchy systems that do not implement more than one memory mapped Configuration Space are allowed to report a value of zero to indicate default Configuration Space.

A Configuration Space base address [63:$(20 + n)$] equal to zero indicates that the Configuration Space address defined by bits $(19 + n)$:12 (Bus Number, Device Number, and Function Number) exists in the default PCI Segment Group; any non-zero value indicates a separate Configuration Space base address.

Software must not use n outside the context of evaluating the Bus Number and memory-mapped Configuration Space base address for this specific target element. In particular, n does not necessarily indicate the maximum Bus Number supported by the associated PCI Segment Group.

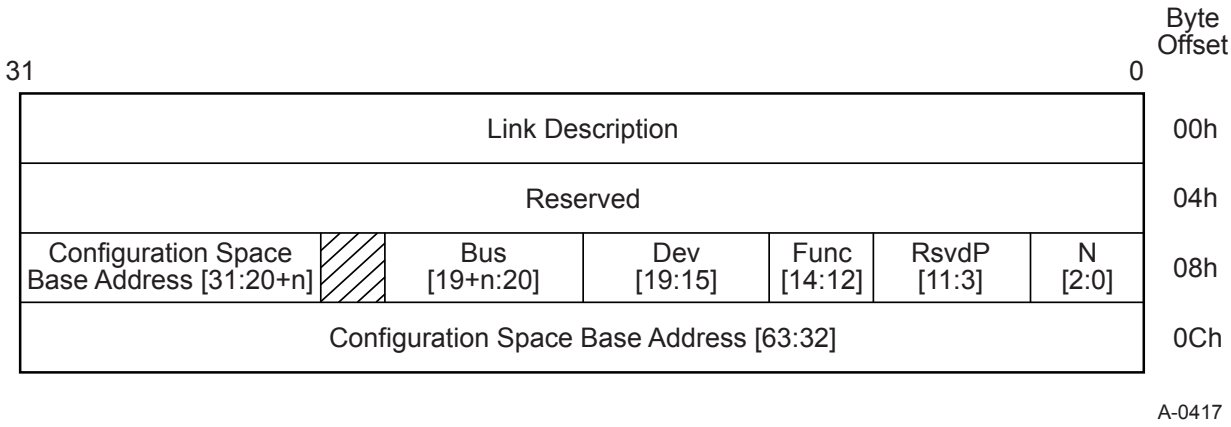

Figure 7-213 Link Address for Link Type 1

Table 7-173 Link Address for Link Type 1

Bit Location	Register Description	Attributes
2:0	***N*** - Encoded number of Bus Number bits	HwInit
14:12	***Function Number***	HwInit
19:15	***Device Number***	HwInit
(19 + *n*):20	***Bus Number***	HwInit
63:(20 + *n*)	***PCI Express Configuration Space Base Address*** (1 ≤ *n* ≤ 8) Note: A Root Complex that does not implement multiple Configuration Spaces is allowed to report this field as 0.	HwInit

7.9.9 Root Complex Internal Link Control Extended Capability

The Root Complex Internal Link Control Extended Capability is an optional Capability that controls an internal Root Complex Link between two distinct Root Complex Components. This Capability is valid for RCRBs that declare an Element Type field as Internal Root Complex Link in the Element Self-Description register of the Root Complex Link Declaration Capability structure.

The Root Complex Internal Link Control Extended Capability structure is defined as shown in Figure 7-214 .

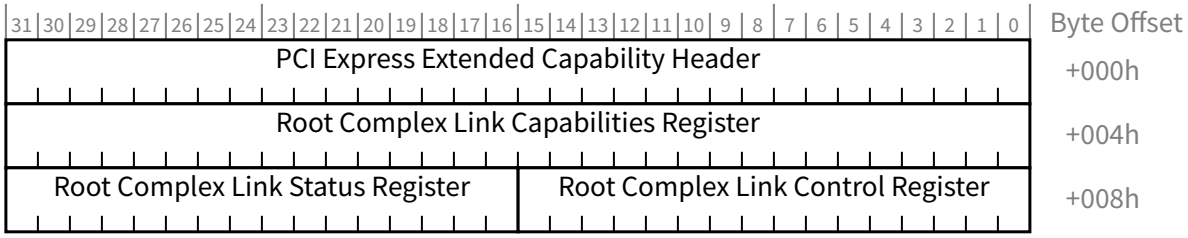

Figure 7-214 Root Complex Internal Link Control Extended Capability

7.9.9.1 Root Complex Internal Link Control Extended Capability Header (Offset 00h)

The Extended Capability ID for the Root Complex Internal Link Control Extended Capability is 0006h.

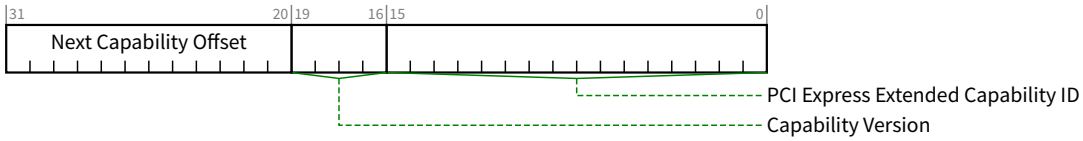

Figure 7-215 Root Complex Internal Link Control Extended Capability Header

Table 7-174 Root Complex Internal Link Control Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Root Complex Internal Link Control Extended Capability is 0006h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.	RO

7.9.9.2 Root Complex Link Capabilities Register (Offset 04h)

The Root Complex Link Capabilities Register identifies capabilities for this Link.

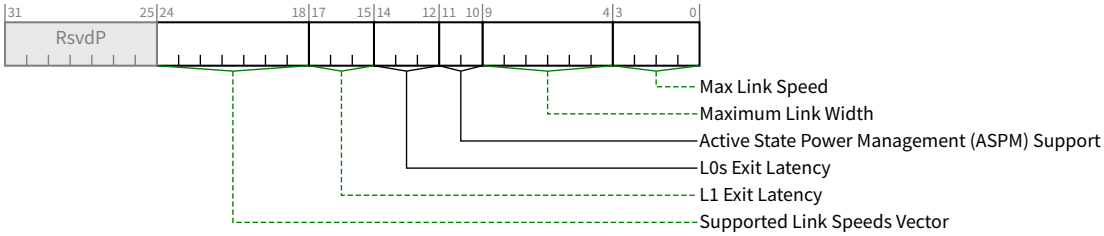

Figure 7-216 Root Complex Link Capabilities Register

Table 7-175 Root Complex Link Capabilities Register

Bit Location	Register Description	Attributes
3:0	***Max Link Speed*** - This field indicates the maximum Link speed of the associated Link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Root Complex Link Capabilities Register) that corresponds to the maximum Link speed. Defined encodings are: **0001b** Supported Link Speeds Vector field bit 0 **0010b** Supported Link Speeds Vector field bit 1 **0011b** Supported Link Speeds Vector field bit 2 **0100b** Supported Link Speeds Vector field bit 3 **0101b** Supported Link Speeds Vector field bit 4 **0110b** Supported Link Speeds Vector field bit 5 **0111b** Supported Link Speeds Vector field bit 6 **Others** All other encodings are reserved. A Root Complex that does not support this feature must report 0000b in this field.	RO
9:4	***Maximum Link Width*** - This field indicates the maximum width of the given Link. Defined encodings are: **00 0001b** x1 **00 0010b** x2 **00 0100b** x4 **00 1000b** x8 **00 1100b** x12 **01 0000b** x16 **10 0000b** x32 All other encodings are Reserved. A Root Complex that does not support this feature must report 00 0000b in this field.	RO
11:10	***Active State Power Management (ASPM) Support*** - This field indicates the level of ASPM supported on the given Link. Defined encodings are: **00b** No ASPM Support **01b** L0s Supported	RO

Bit Location	Register Description	Attributes
	10b L1 Supported **11b** L0s and L1 Supported	
14:12	***L0s Exit Latency*** - This field indicates the L0s exit latency for the given Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. If L0s is not supported, the value is undefined. Defined encodings are: **000b** Less than 64 ns **001b** 64 ns to less than 128 ns **010b** 128 ns to less than 256 ns **011b** 256 ns to less than 512 ns **100b** 512 ns to less than 1 µs **101b** 1 µs to less than 2 µs **110b** 2 µs to 4 µs **111b** More than 4 µs	RO
17:15	***L1 Exit Latency*** - This field indicates the L1 exit latency for the given Link. The value reported indicates the length of time this Port requires to complete transition from ASPM L1 to L0. If ASPM L1 is not supported, the value is undefined. Defined encodings are: **000b** Less than 1 µs **001b** 1 µs to less than 2 µs **010b** 2 µs to less than 4 µs **011b** 4 µs to less than 8 µs **100b** 8 µs to less than 16 µs **101b** 16 µs to less than 32 µs **110b** 32 µs to 64 µs **111b** More than 64 µs	RO
24:18	***Supported Link Speeds Vector*** - This field indicates the supported Link speed(s) of the associated Link. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. See Section 8.2.1 for further requirements. Bit definitions within this field are: **Bit 0** 2.5 GT/s **Bit 1** 5.0 GT/s **Bit 2** 8.0 GT/s **Bit 3** 16.0 GT/s **Bit 4** 32.0 GT/s **Bits 6:5** RsvdP	RO

IMPLEMENTATION NOTE
Supported Link Speeds With Earlier Hardware

Hardware components compliant to versions prior to the [PCIe-3.0] did not implement the Supported Link Speeds Vector field and instead returned 0000 000b in bits 24:18.

For software to determine the supported Link speeds for components where this field is contains 0000 000b, software can read bits 3:0 of the Root Complex Link Capabilities Register (now defined to be the Max Link Speed field), and interpret the value as follows:

0001b
2.5 GT/s Link speed supported

0010b
5.0 GT/s and 2.5 GT/s Link speeds supported

For such components, the same encoding is also used for the values for the Current Link Speed field (in the Root Complex Link Status Register).

IMPLEMENTATION NOTE
Software Management of Link Speeds With Future Hardware

It is strongly encouraged that software primarily utilize the Supported Link Speeds Vector instead of the Max Link Speed field, so that software can determine the exact set of supported speeds on current and future hardware. This can avoid software being confused if a future specification defines Links that do not require support for all slower speeds.

7.9.9.3 Root Complex Link Control Register (Offset 08h)

The Root Complex Link Control Register controls parameters for this internal Link.

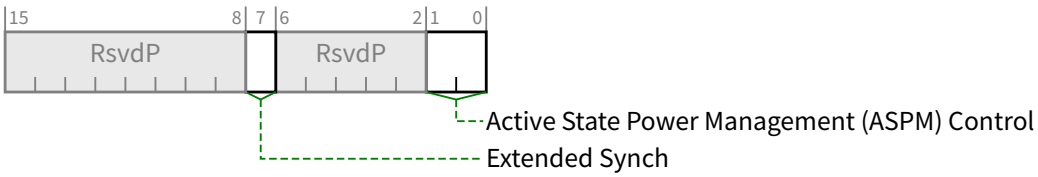

Figure 7-217 Root Complex Link Control Register

Table 7-176 Root Complex Link Control Register

Bit Location	Register Description	Attributes
1:0	***Active State Power Management (ASPM) Control*** - This field controls the level of ASPM enabled on the given Link. Defined encodings are: **00b** Disabled **01b** L0s Entry Enabled **10b** L1 Entry Enabled **11b** L0s and L1 Entry Enabled Note: "L0s Entry Enabled" enables the Transmitter to enter L0s. If L0s is supported, the Receiver must be capable of entering L0s even when the Transmitter is disabled from entering L0s (00b or 10b). Default value of this field is implementation specific. Software must not enable L0s in either direction on a given Link unless components on both sides of the Link each support L0s, as indicated by their ASPM Support field values. Otherwise, the result is undefined. ASPM L1 must be enabled by software in the Upstream component on a Link prior to enabling ASPM L1 in the Downstream component on that Link. When disabling ASPM L1, software must disable ASPM L1 in the Downstream component on a Link prior to disabling ASPM L1 in the Upstream component on that Link. ASPM L1 must only be enabled on the Downstream component if both components on a Link support ASPM L1. A Root Complex that does not support this feature for the given internal Link must hardwire this field to 00b.	RW
7	***Extended Synch*** - This bit when Set forces the transmission of additional Ordered Sets when exiting the L0s state (see Section 4.2.4.6) and when in the Recovery state (see Section 4.2.6.4.1). This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. A Root Complex that does not support this feature for the given internal Link must hardwire this bit to 0b. Default value for this bit is 0b.	RW

7.9.9.4 Root Complex Link Status Register (Offset 0Ah)

The Root Complex Link Status Register provides information about Link specific parameters.

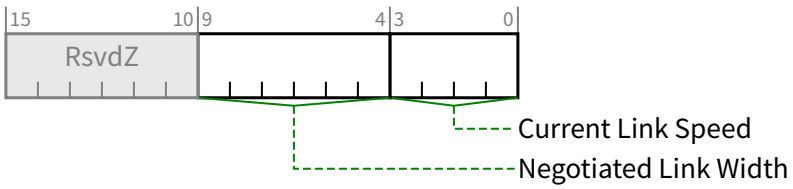

Figure 7-218 Root Complex Link Status Register

Table 7-177 Root Complex Link Status Register

Bit Location	Register Description	Attributes
3:0	***Current Link Speed*** - This field indicates the negotiated Link speed of the given Link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Root Complex Link Capabilities Register) that corresponds to the current Link speed. Defined encodings are: **0001b** Supported Link Speeds Vector field bit 0 **0010b** Supported Link Speeds Vector field bit 1 **0011b** Supported Link Speeds Vector field bit 2 **0100b** Supported Link Speeds Vector field bit 3 **0101b** Supported Link Speeds Vector field bit 4 **0110b** Supported Link Speeds Vector field bit 5 **0111b** Supported Link Speeds Vector field bit 6 All other encodings are Reserved. The value in this field is undefined when the Link is not up. A Root Complex that does not support this feature must report 0000b in this field.	RO
9:4	***Negotiated Link Width*** - This field indicates the negotiated width of the given Link. Defined encodings are: **00 0001b** x1 **00 0010b** x2 **00 0100b** x4 **00 1000b** x8 **00 1100b** x12 **01 0000b** x16 **10 0000b** x32 All other encodings are Reserved. The value in this field is undefined when the Link is not up. A Root Complex that does not support this feature must hardwire this field to 00 0000b.	RO

7.9.10 *Root Complex Event Collector Endpoint Association Extended Capability*

The Root Complex Event Collector Endpoint Association Extended Capability is implemented by Root Complex Event Collectors. It declares the RCiEPs supported by the Root Complex Event Collector. A Root Complex Event Collector must implement the Root Complex Event Collector Endpoint Association Extended Capability; no other PCI Express Device Function is permitted to implement this Capability.

The Root Complex Event Collector Endpoint Association Extended Capability, as shown in Figure 7-219 , consists of the PCI Express Extended Capability header followed by a DWORD bitmap enumerating RCiEPs on the same Bus, and optionally an additional range of Bus Numbers that may contain RCiEPs associated with the Root Complex Event Collector. Functions other than RCiEPs (e.g. Root Ports) contained in the range described by this Capability are not associated with this Root Complex Event Collector.

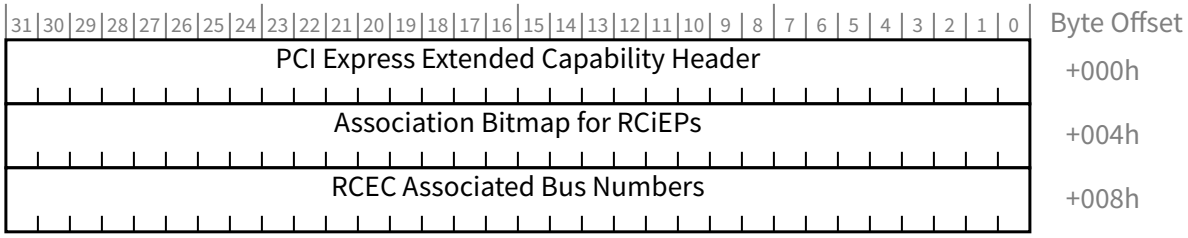

Figure 7-219 Root Complex Event Collector Endpoint Association Extended Capability

7.9.10.1 Root Complex Event Collector Endpoint Association Extended Capability Header (Offset 00h)

The Extended Capability ID for the Root Complex Event Collector Endpoint Association Extended Capability is 0007h. Figure 7-220 details allocation of fields in the Root Complex Event Collector Endpoint Association Extended Capability Header; Table 7-178 provides the respective bit definitions.

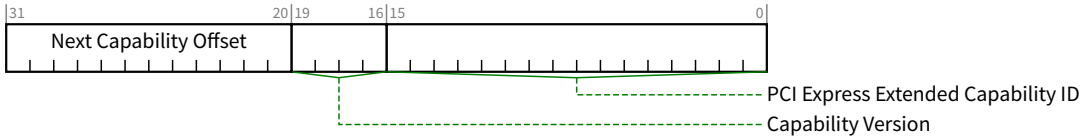

Figure 7-220 Root Complex Event Collector Endpoint Association Extended Capability Header

Table 7-178 Root Complex Event Collector Endpoint Association Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Root Complex Event Collector Endpoint Association Extended Capability is 0007h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 2h if the Extended Capability contains the RCEC Associated Bus Numbers Register (see Section 7.9.10.3). Must be 1h otherwise.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.	RO

7.9.10.2 Association Bitmap for RCiEPs (Offset 04h)

The Association Bitmap for RCiEPs is a read-only register that sets the bits corresponding to the Device Numbers of RCiEPs associated with the Root Complex Event Collector on the same Bus Number as the Event Collector itself. The bit corresponding to the Device Number of the Root Complex Event Collector must always be Set.

7.9.10.3 RCEC Associated Bus Numbers Register (Offset 08h)

The RCEC Associated Bus Numbers Register is a read-only register that indicates an additional range of Bus Numbers containing RCiEPs associated with this Root Complex Event Collector. It is permitted for Functions other than RCiEPs, including Root Ports, to appear within the Association Bus Range. Only RCiEPs in the range are associated with this Root Complex Event Collector. This register is present if the Capability Version is 2h or greater.

This register does not indicate association between an Event Collector and any Virtual Functions within the Association Bus Range (see Section 9.2.1.2). This register does not indicate association between an Event Collector and any Function on the same Bus Number as the Event Collector itself, however it is permitted for the Association Bus Range to include the Bus Number of the Root Complex Event Collector.

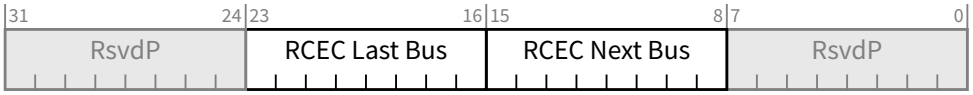

Figure 7-221 RCEC Associated Bus Numbers Register

Table 7-179 RCEC Associated Bus Numbers Register

Bit Location	Register Description	Attributes
15:8	***RCEC Next Bus*** - This field contains the lowest additional bus number containing RCiEPs associated with this Root Complex Event Collector. If all of the Devices associated with this Root Complex Event Collector are on the same bus as the Event Collector, then this field must be set to FFh.	HwInit
23:16	***RCEC Last Bus*** - This field contains the highest additional bus number containing RCiEPs associated with this Root Complex Event Collector. If all of the Devices associated with this Root Complex Event Collector are on the same bus as the Event Collector, then this field must be set to 00h.	HwInit

IMPLEMENTATION NOTE

RCEC Associated Bus Number Compatibility with Legacy Software

Legacy software may not support the use of the RCEC Associated Bus Numbers Register as a mechanism to associate Devices with a RCEC. Such software may see events in the RCEC from Devices on different bus numbers that it does not consider to be associated with the Root Complex Event Collector. System Software is strongly encouraged to report all events seen on the Root Complex Event Collector, regardless of whether or not it can determine association.

7.9.11 *Multicast Extended Capability*

Multicast is an optional normative functionality that is controlled by the Multicast Extended Capability structure. The Multicast Extended Capability is applicable to Root Ports, RCRBs, Switch Ports, Endpoint Functions, and RCiEPs. It is not applicable to PCI Express to PCI/PCI-X Bridges.

In the cases of a Switch or Root Complex or a component that contains multiple Functions, multiple copies of this Capability structure are required - one for each Endpoint Function, Switch Port, or Root Port that supports Multicast. To provide implementation efficiencies, certain fields within each of the Multicast Extended Capability structures within a component must be programmed the same and results are indeterminate if this is not the case. The fields and registers that must be configured with the same values include MC_Enable, MC_Num_Group, MC_Base_Address and MC_Index_Position. These same fields in an Endpoint's Multicast Extended Capability structure must match those configured into a Multicast Extended Capability structure of the Switch or Root Complex above the Endpoint or in which the RCiEP is integrated.

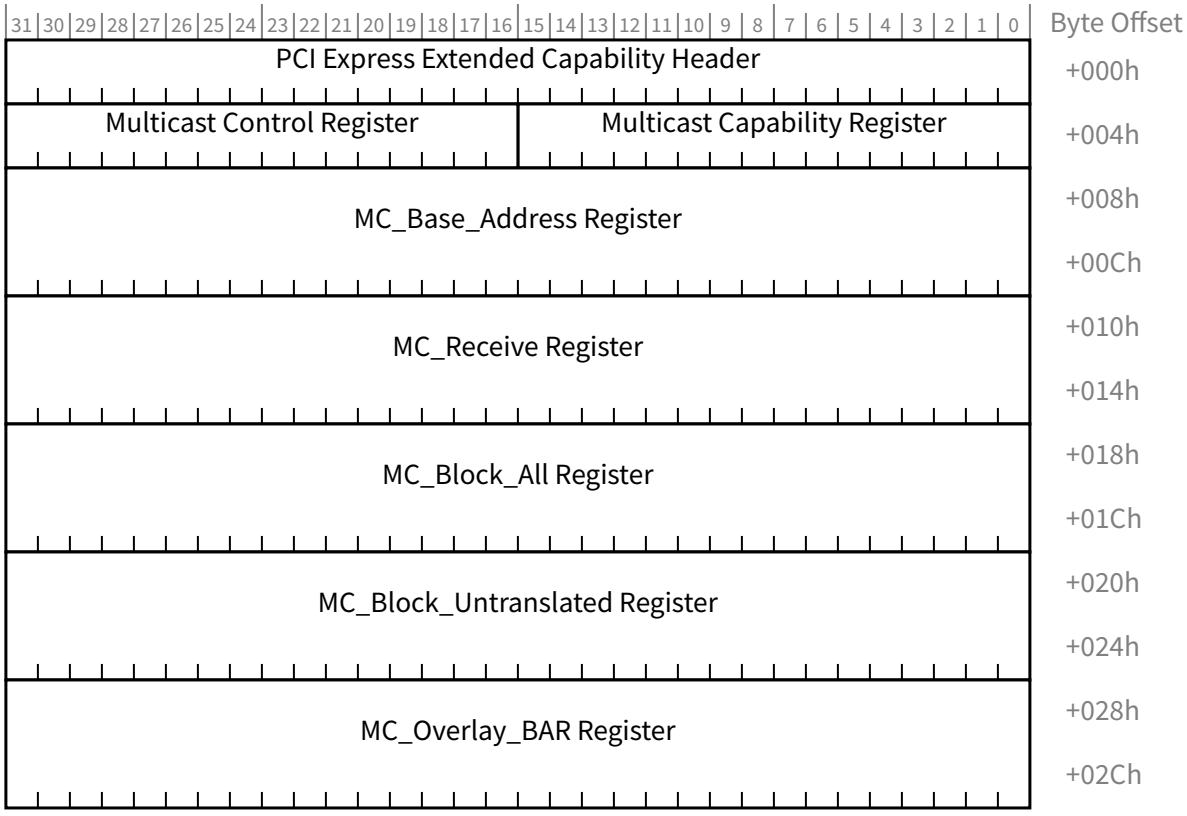

Figure 7-222 Multicast Extended Capability Structure

7.9.11.1 *Multicast Extended Capability Header (Offset 00h)*

Figure 7-223 details allocation of the fields in the Multicast Extended Capability Header and Table 7-180 provides the respective bit definitions.

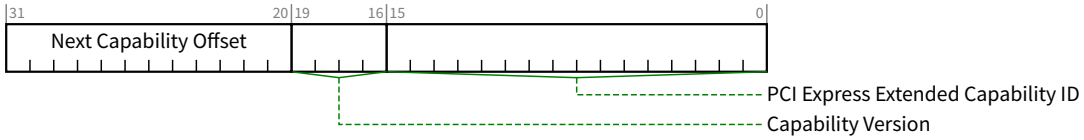

Figure 7-223 Multicast Extended Capability Header

Table 7-180 Multicast Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Multicast Extended Capability is 0012h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.9.11.2 Multicast Capability Register (Offset 04h)

Figure 7-224 details allocation of the fields in the Multicast Capability Register and Table 7-181 provides the respective bit definitions.

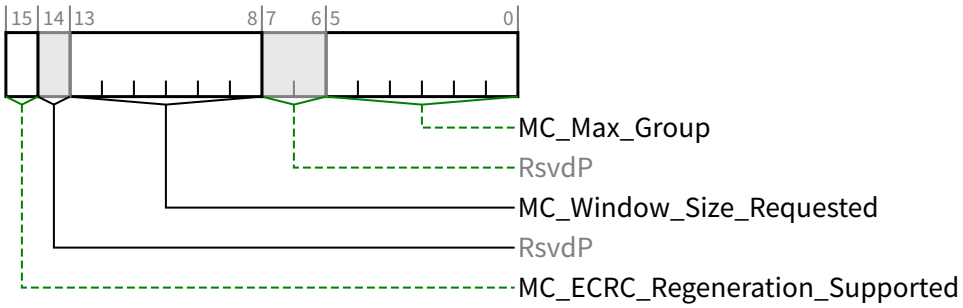

Figure 7-224 Multicast Capability Register

Table 7-181 Multicast Capability Register

Bit Location	Register Description	Attributes
5:0	***MC_Max_Group*** - Value indicates the maximum number of Multicast Groups that the component supports, encoded as M-1. A value of 00h indicates that one Multicast Group is supported.	RO

Bit Location	Register Description	Attributes
13:8	***MC_Window_Size_Requested*** - In Endpoints, the $\log_2$ of the Multicast Window size requested. RsvdP in Switch and Root Ports.	RO
15	***MC_ECRC_Regeneration_Supported*** - If Set, indicates that ECRC regeneration is supported. This bit must not be Set unless the Function supports Advanced Error Reporting, and the ECRC Check Capable bit in the Advanced Error Capabilities and Control register is also Set. However, if ECRC regeneration is supported, its operation is not contingent upon the setting of the ECRC Check Enable bit in the Advanced Error Capabilities and Control register. This bit is applicable to Switch and Root Ports and is RsvdP in all other Functions.	RO/RsvdP

7.9.11.3 Multicast Control Register (Offset 06h)

Table 7-182 details allocation of the fields in the Multicast Control Register and Table 7-182 provides the respective bit definitions.

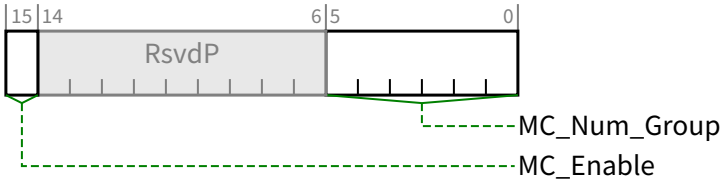

Figure 7-225 Multicast Control Register

Table 7-182 Multicast Control Register

Bit Location	Register Description	Attributes
5:0	***MC_Num_Group*** - Value indicates the number of Multicast Groups configured for use, encoded as N-1. The default value of 00 0000b indicates that one Multicast Group is configured for use. Behavior is undefined if value exceeds MC_Max_Group. This parameter indirectly defines the upper limit of the Multicast address range. This field is ignored if MC_Enable is Clear. Default value is 00 0000b.	RW
15	***MC_Enable*** - When Set, the Multicast mechanism is enabled for the component. Default value is 0b.	RW

7.9.11.4 MC_Base_Address Register (Offset 08h)

The MC_Base_Address Register contains the MC_Base_Address and the MC_Index_Position. Figure 7-226 details allocation of the fields in the MC_Base_Address Register and Table 7-183 provides the respective bit definitions.

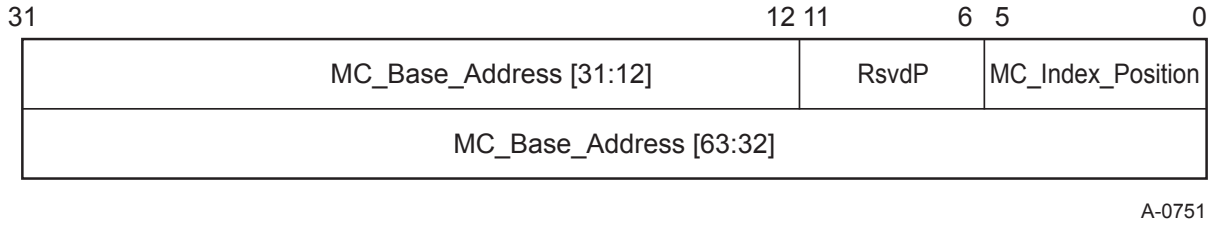

Figure 7-226 MC_Base_Address Register

Table 7-183 MC_Base_Address Register

Bit Location	Register Description	Attributes
5:0	***MC_Index_Position*** - The location of the LSB of the Multicast Group number within the address. Behavior is undefined if this value is less than 12 and MC_Enable is Set. Default is 0.	RW
63:12	***MC_Base_Address*** - The base address of the Multicast address range. The behavior is undefined if MC_Enable is Set and bits in this field corresponding to address bits that contain the Multicast Group number or address bits less than MC_Index_Position are non-zero. Default is 0.	RW

7.9.11.5 MC_Receive Register (Offset 10h)

The MC_Receive Register provides a bit vector denoting which Multicast groups the Function should accept, or in the case of Switch and Root Complex Ports, forward Multicast TLPs. This register is required in all Functions that implement the MC Capability structure.

Figure 7-227 details allocation of the fields in the MC_Receive Register and Table 7-184 provides the respective bit definitions.

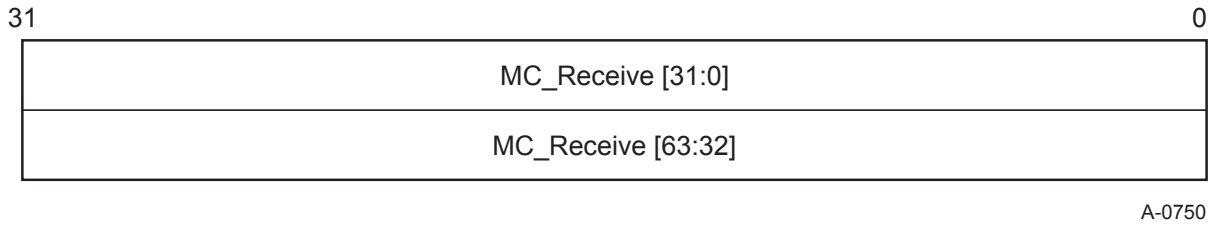

Figure 7-227 MC_Receive Register

Table 7-184 MC_Receive Register

Bit Location	Register Description	Attributes
MC_Max_Group:0	***MC_Receive*** - For each bit that's Set, this Function gets a copy of any Multicast TLPs for the associated Multicast Group. Bits above MC_Num_Group are ignored by hardware. Default value of each bit is 0b.	RW
All other bits	Reserved	RsvdP

7.9.11.6 MC_Block_All Register (Offset 18h)

The MC_Block_All Register provides a bit vector denoting which Multicast groups the Function should block. This register is required in all Functions that implement the MC Capability structure.

Figure 7-228 details allocation of the fields in the MC_Block_All Register and Table 7-185 provides the respective bit definitions.

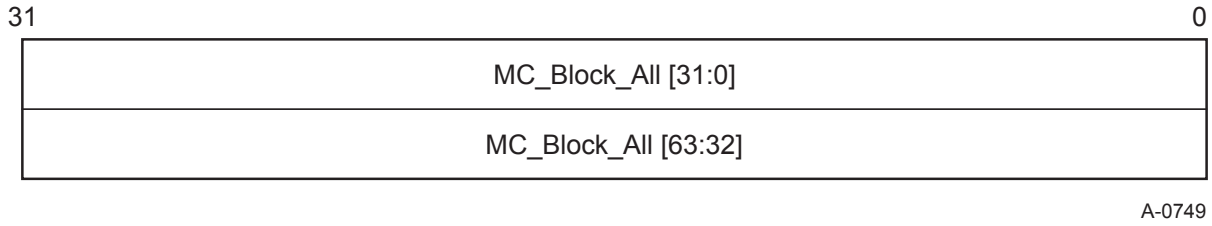

Figure 7-228 MC_Block_All Register

Table 7-185 MC_Block_All Register

Bit Location	Register Description	Attributes
MC_Max_Group:0	***MC_Block_All*** - For each bit that is Set, this Function is blocked from sending TLPs to the associated Multicast Group. Bits above MC_Num_Group are ignored by hardware. Default value of each bit is 0b.	RW
All other bits	Reserved	RsvdP

7.9.11.7 MC_Block_Untranslated Register (Offset 20h)

The MC_Block_Untranslated Register is used to determine whether or not a TLP that includes an Untranslated Address should be blocked. This register is required in all Functions that implement the MC Capability structure. However, an Endpoint Function that does not implement the ATS capability may implement this register as RsvdP.

Figure 7-229 details allocation of the fields in the MC_Block_Untranslated Register and Table 7-186 provides the respective bit definitions.

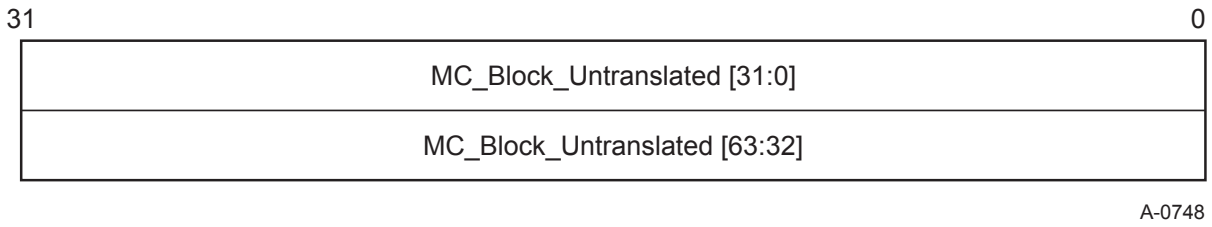

Figure 7-229 MC_Block_Untranslated Register

Table 7-186 MC_Block_Untranslated Register

Bit Location	Register Description	Attributes
MC_Max_Group:0	***MC_Block_Untranslated*** - For each bit that is Set, this Function is blocked from sending TLPs containing Untranslated Addresses to the associated MCG. Bits above MC_Num_Group are ignored by hardware. Default value of each bit is 0b.	RW
All other bits	Reserved	RsvdP

7.9.11.8 MC_Overlay_BAR Register (Offset 28h)

The MC_Overlay_BAR Register is required in Switch and Root Complex Ports that support the Multicast Extended Capability and not implemented in Endpoints. Software must interpret the Device/Port Type field in the PCI Express Capabilities Register to determine if the MC_Overlay_BAR Register is present in a Function.

The MC_Overlay_BAR specifies the base address of a window in unicast space onto which Multicast TLPs going out an Egress Port are overlaid by a process of address replacement. This allows a single BAR in an Endpoint attached to the Switch or Root Port to be used for both unicast and Multicast traffic. At a Switch Upstream Port, it allows the Multicast address range, or a portion of it, to be overlayed onto host memory.

Figure 7-230 details allocation of the fields in the MC_Overlay_BAR Register and Table 7-187 provides the respective bit definitions.

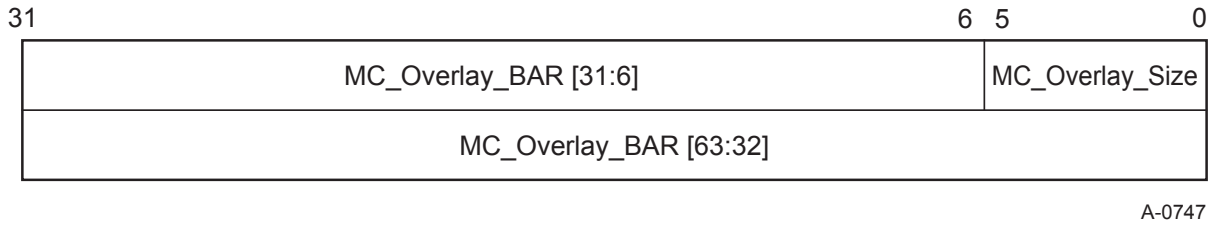

Figure 7-230 MC_Overlay_BAR Register

Table 7-187 MC_Overlay_BAR Register

Bit Location	Register Description	Attributes
5:0	***MC_Overlay_Size*** - If 6 or greater, specifies the size in bytes of the overlay aperture as a power of 2. If less than 6, disables the overlay mechanism. Default value is 00 0000b.	RW
63:6	***MC_Overlay_BAR*** - Specifies the base address of the window onto which MC TLPs passing through this Function will be overlaid. Default value is 0.	RW

7.9.12 Dynamic Power Allocation Extended Capability (DPA Capability)

The DPA Capability structure is shown in Figure 7-231 .

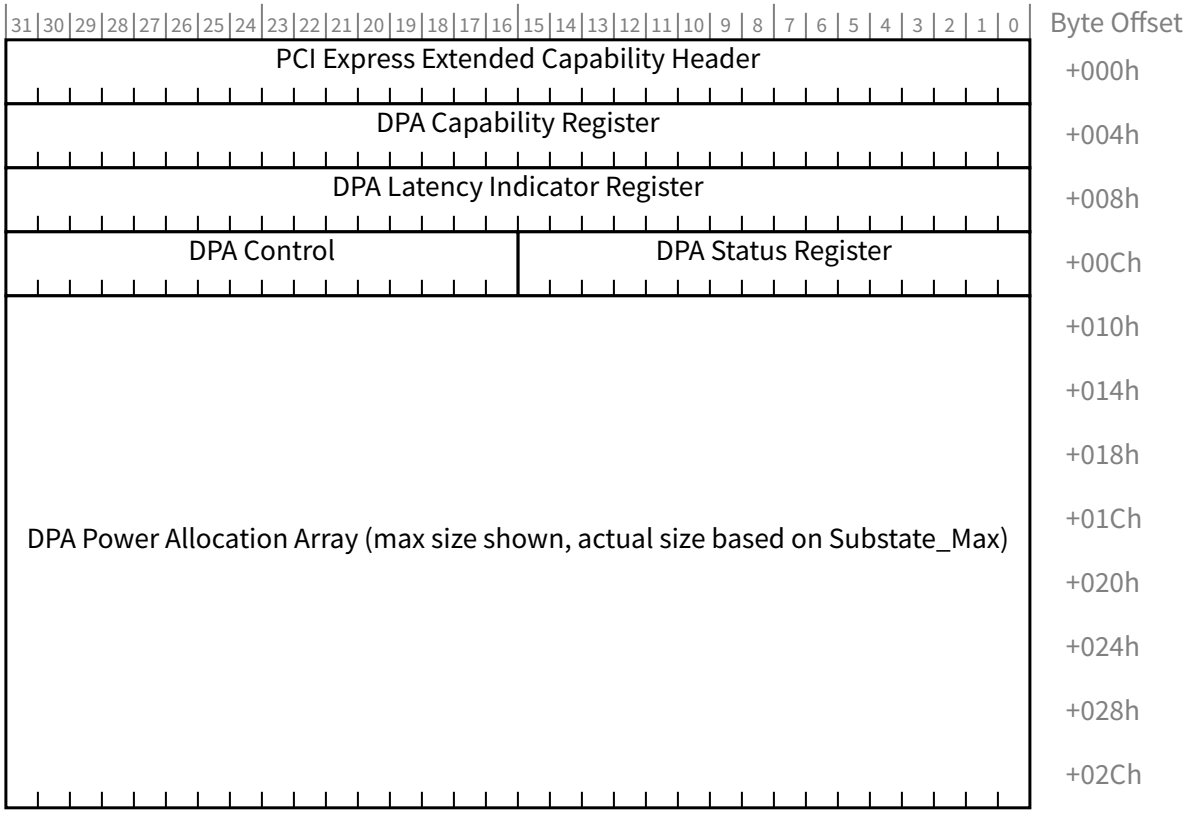

Figure 7-231 Dynamic Power Allocation Extended Capability Structure

7.9.12.1 DPA Extended Capability Header (Offset 00h)

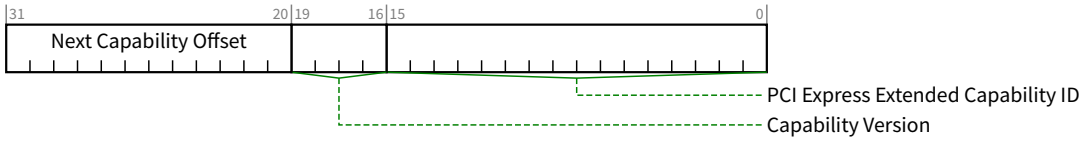

Figure 7-232 DPA Extended Capability Header

Table 7-188 DPA Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the DPA Extended Capability is 0016h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.	RO

Bit Location	Register Description	Attributes
	Must be 1h for this version of the specification.	
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.9.12.2 DPA Capability Register (Offset 04h)

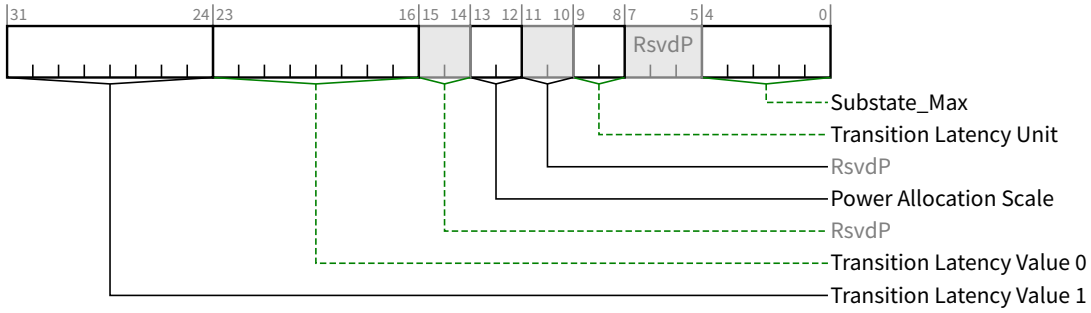

Figure 7-233 DPA Capability Register

Table 7-189 DPA Capability Register

Bit Location	Register Description	Attributes
4:0	***Substate_Max*** - Value indicates the maximum substate number, which is the total number of supported substates minus one. A value of 0 0000b indicates support for one substate.	RO
9:8	***Transition Latency Unit*** (***Tlunit***) - A substate's Transition Latency Value is multiplied by the Transition Latency Unit to determine the maximum Transition Latency for the substate. Defined encodings are **00b** 1 ms **01b** 10 ms **10b** 100 ms **11b** Reserved	RO
13:12	***Power Allocation Scale*** (***PAS***) - The encodings provide the scale to determine power allocation per substate in Watts. The value corresponding to the substate in the Substate Power Allocation field is multiplied by this field to determine the power allocation for the substate. Defined encodings are **00b** 10.0x **01b** 1.0x **10b** 0.1x **11b** 0.01x	RO
23:16	***Transition Latency Value 0*** (***Xlcy0***) - This value is multiplied by the Transition Latency Unit to determine the maximum Transition Latency for the substate	RO

Bit Location	Register Description	Attributes
31:24	***Transition Latency Value 1*** (***Xlcy1***) - This value is multiplied by the Transition Latency Unit to determine the maximum Transition Latency for the substate.	RO

7.9.12.3 DPA Latency Indicator Register (Offset 08h)

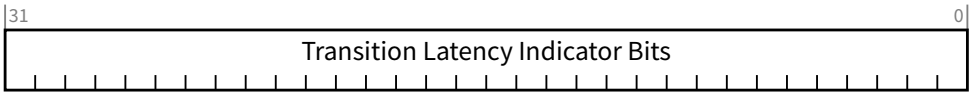

Figure 7-234 DPA Latency Indicator Register

Table 7-190 DPA Latency Indicator Register

Bit Location	Register Description	Attributes
31:0	***Transition Latency Indicator Bits*** - Each bit indicates which Transition Latency Value is associated with the corresponding substate. A value of 0b indicates Transition Latency Value 0; a value of 1b indicates Transition Latency Value 1. Only bits [Substate_Max:0] are defined. Bits above Substate_Max are RsvdP.	RO

7.9.12.4 DPA Status Register (Offset 0Ch)

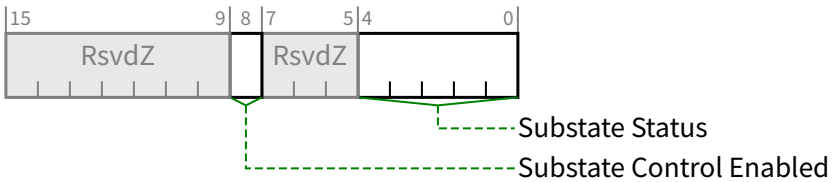

Figure 7-235 DPA Status Register

Table 7-191 DPA Status Register

Bit Location	Register Description	Attributes
4:0	***Substate Status*** - Indicates current substate for this Function. Default is 0 0000b.	RO
8	***Substate Control Enabled*** - Used by software to disable the Substate Control field in the DPA Control Register. Hardware sets this bit following a Conventional Reset or FLR. Software clears this bit by writing a 1b to it. Software is unable to set this bit directly. When this bit is Set, the Substate Control field determines the current substate. When this bit is Clear, the Substate Control field has no effect on the current substate.	RW1C

Bit Location	Register Description	Attributes
	Default value is 1b.	

7.9.12.5 DPA Control Register (Offset 0Eh)

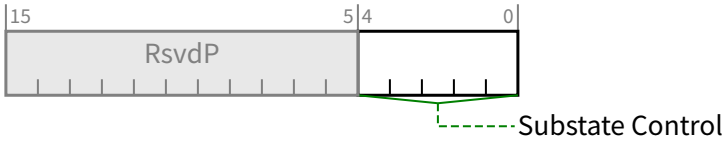

Figure 7-236 DPA Control Register

Table 7-192 DPA Control Register

Bit Location	Register Description	Attributes
4:0	***Substate Control*** - Used by software to configure the Function substate. Software writes the substate value in this field to initiate a substate transition. When the Substate Control Enabled bit in the DPA Status Register is Set, this field determines the Function substate. When the Substate Control Enabled bit in the DPA Status Register is Clear, this field has no effect on the Function substate. Default value is 0 0000b.	RW

7.9.12.6 DPA Power Allocation Array

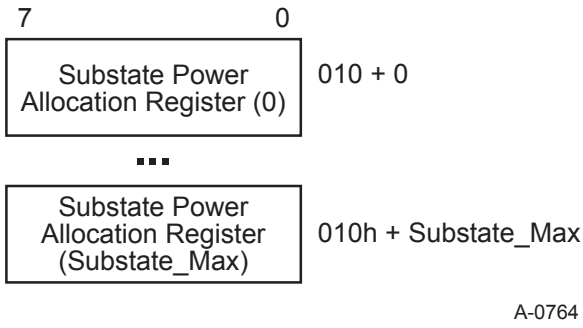

Figure 7-237 DPA Power Allocation Array

Each Substate Power Allocation register indicates the power allocation value for its associated substate. The number of Substate Power Allocation registers implemented must be equal to the number of substates supported by Function, which is Substate_Max plus one.

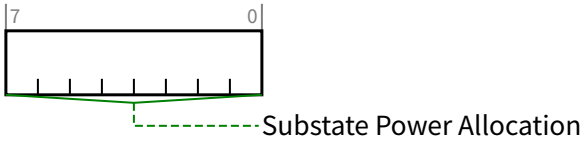

Figure 7-238 Substate Power Allocation Register (0 to Substate_Max)

Table 7-193 Substate Power Allocation Register (0 to Substate_Max)

Bit Location	Register Description	Attributes
7:0	***Substate Power Allocation*** - The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the associated substate.	RO

7.9.13 *TPH Requester Extended Capability*

The TPH Requester Extended Capability structure is required for all Functions that are capable of generating Request TLPs with TPH. For a Multi-Function Device, this capability must be present in each Function that is capable of generating Request TLPs with TPH.

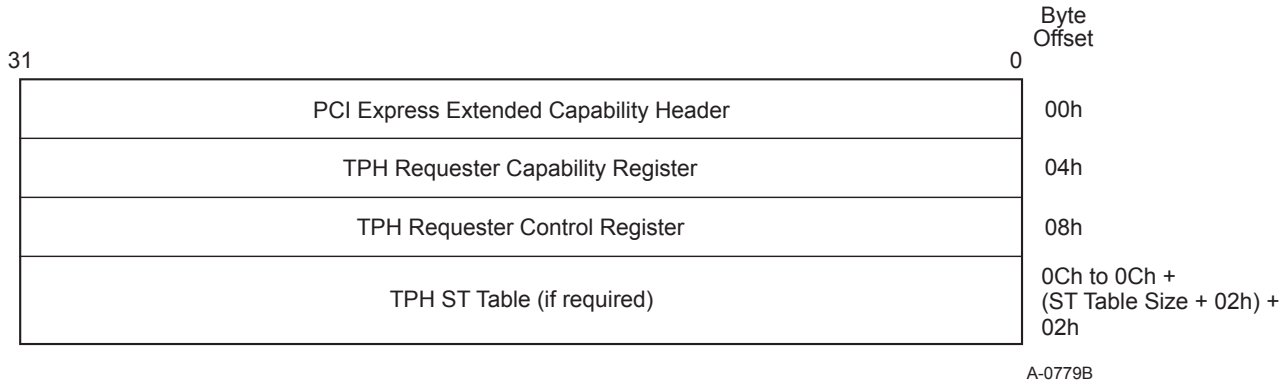

Figure 7-239 TPH Extended Capability Structure

7.9.13.1 *TPH Requester Extended Capability Header (Offset 00h)*

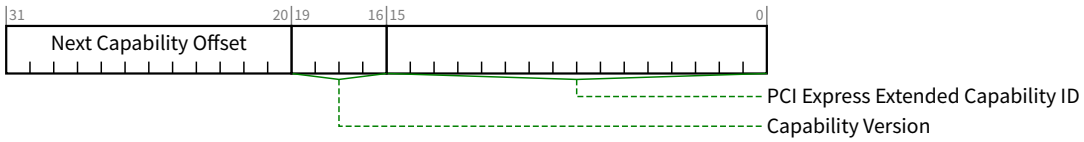

Figure 7-240 TPH Requester Extended Capability Header

Table 7-194 TPH Requester Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the TPH Requester Extended Capability is 0017h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.9.13.2 TPH Requester Capability Register (Offset 04h)

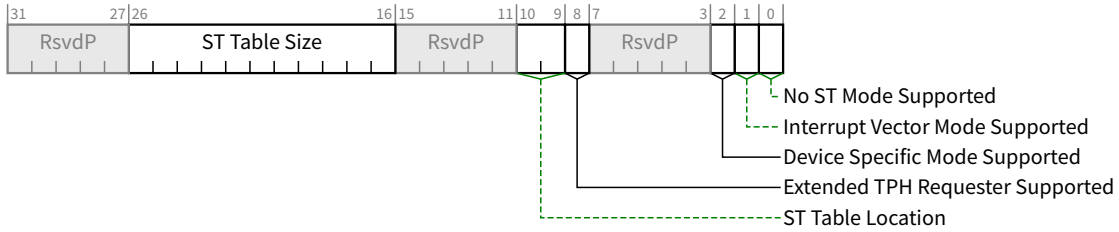

Figure 7-241 TPH Requester Capability Register

Table 7-195 TPH Requester Capability Register

Bit Location	Register Description	Attributes
0	***No ST Mode Supported*** - If set indicates that the Function supports the No ST Mode of operation. This mode is required to be supported by all Functions that implement this Capability structure. This bit must have a value of 1b.	RO
1	***Interrupt Vector Mode Supported*** - If set indicates that the Function supports the Interrupt Vector Mode of operation.	RO
2	***Device Specific Mode Supported*** - If set indicates that the Function supports the Device Specific Mode of operation.	RO
8	***Extended TPH Requester Supported*** - If Set indicates that the Function is capable of generating Requests with a TPH TLP Prefix. See Section 2.2.7.1 for additional details.	RO
10:9	***ST Table Location*** - Value indicates if and where the ST Table is located. Defined Encodings are: **00b** ST Table is not present **01b** ST Table is located in the TPH Requester Extended Capability structure **10b** ST Table is located in the MSI-X Table (see Section 7.7.2)	RO

Bit Location	Register Description	Attributes
	11b Reserved A Function that only supports the No ST Mode of operation must have a value of 00b in this field. A Function may report a value of 10b only if it implements an MSI-X Capability.	
26:16	***ST Table Size*** - Value indicates the maximum number of ST Table entries the Function may use. Software reads this field to determine the ST Table Size N, which is encoded as N-1. For example, a returned value of 000 0000 0011b indicates a table size of four entries. There is an upper limit of 64 entries when the ST Table is located in the TPH Requester Extended Capability structure. When the ST Table is located in the MSI-X Table, this value is limited by the size of the MSI-X Table. This field is only applicable for Functions that implement an ST Table as indicated by the ST Table Location field. Otherwise, the value in this field is undefined.	RO

7.9.13.3 TPH Requester Control Register (Offset 08h)

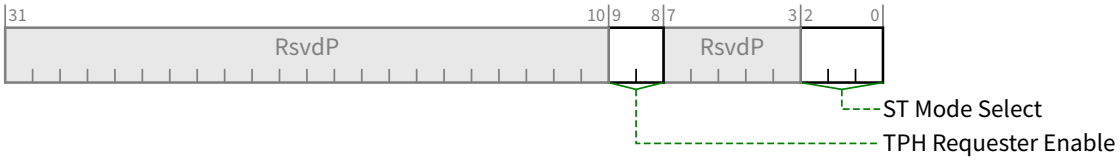

Figure 7-242 TPH Requester Control Register

Table 7-196 TPH Requester Control Register

Bit Location	Register Description	Attributes
2:0	***ST Mode Select*** - selects the ST Mode of operation. Defined encodings are: **000b** ***No ST Mode*** **001b** Interrupt Vector Mode **010b** Device Specific Mode **others** reserved for future use Functions that support only the No ST Mode of operation must hardwire this field to 000b. Function operation is undefined if software enables a mode of operation that does not correspond to a mode supported by the Function. The default value of this field is 000b. See Section 6.17.3 for details on ST modes of operation.	RW
9:8	***TPH Requester Enable*** - Controls the ability to issue Request TLPs using either TPH or Extended TPH. Defined encodings are: **00b** Function operating as a Requester is not permitted to issue Requests with TPH or Extended TPH	RW

Bit Location	Register Description	Attributes
	01b Function operating as a Requester is permitted to issue Requests with TPH and is not permitted to issue Requests with Extended TPH **10b** Reserved **11b** Function operating as a Requester is permitted to issue Requests with TPH and Extended TPH Functions that advertise that they do not support Extended TPH are permitted to hardwire bit 9 of this field to 0b. The default value of this field is 00b.	

7.9.13.4 TPH ST Table (Starting from Offset 0Ch)

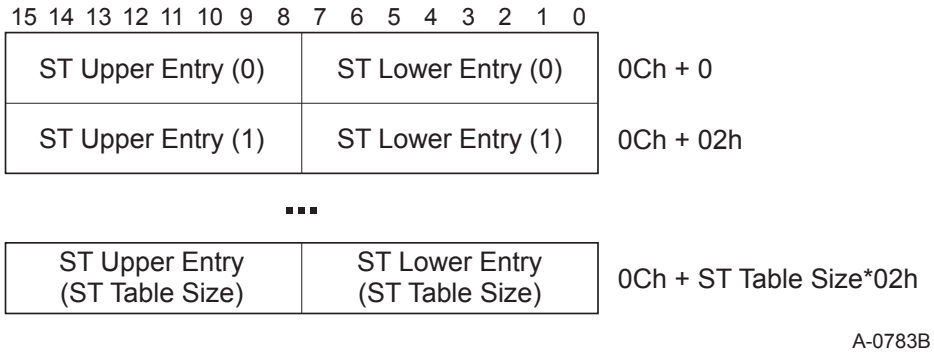

Figure 7-243 TPH ST Table

The TPH ST Table must be implemented in the TPH Requester Extended Capability structure if the value of the ST Table Location field is 01b. For all other values, the ST Entry registers must not be implemented. Each implemented ST Entry is 16 bits. The number of ST Entry registers implemented must be equal to the number of ST Table entries supported by the Function, which is the value of the ST Table Size field plus one.

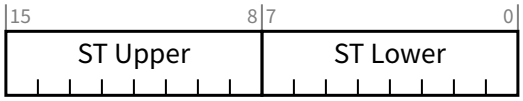

Figure 7-244 TPH ST Table Entry

Table 7-197 ***TPH ST Table Entry***

Bit Location	Register Description	Attributes
7:0	***ST Lower*** - This field contains the lower 8 bits of a Steering Tag. Default value of this field is 00h.	RW

Bit Location	Register Description	Attributes
15:8	***ST Upper*** - If the Function's Extended TPH Requester Supported bit is Set, then this field contains the upper 8 bits of a Steering Tag. Otherwise, this field is RsvdP. Default value of this field is 00h.	RW

7.9.14 *LN Requester Extended Capability (LNR Capability)*

The LN Requester Extended Capability is an optional normative capability for Endpoints. All Endpoints that support LN protocol as a Requester must implement this capability. See Section 6.21 . This capability may be implemented by any type of Endpoint, but not by any other Function type.

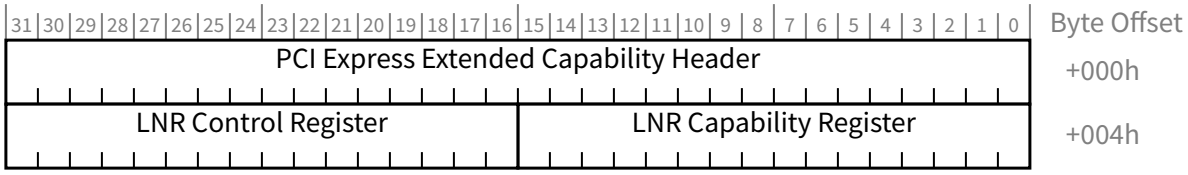

Figure 7-245 LN Requester Extended Capability

7.9.14.1 *LNR Extended Capability Header (Offset 00h)*

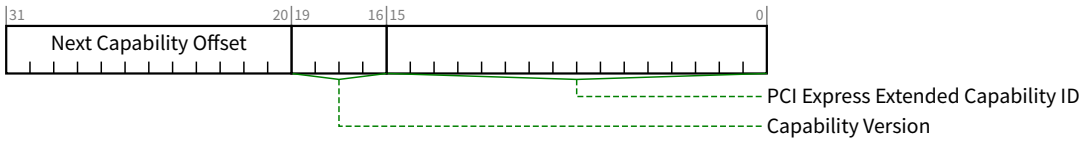

Figure 7-246 LNR Extended Capability Header

Table 7-198 LNR Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. PCI Express Extended Capability ID for the LNR Extended Capability is 001Ch.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of capabilities.	RO

7.9.14.2 LNR Capability Register (Offset 04h)

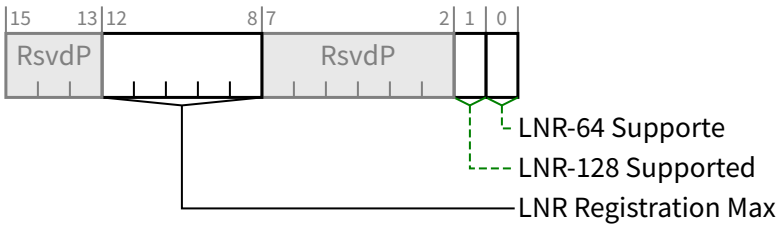

Figure 7-247 LNR Capability Register

Table 7-199 LNR Capability Register

Bit Location	Register Description	Attributes
0	***LNR-64 Supporte***d - This bit must be 1b if the Endpoint supports LN protocol for 64-byte cachelines as a Requester; otherwise, must be 0b. See Section 6.21.4 for additional details.	RO
1	***LNR-128 Supported*** - This bit must be 1b if the Endpoint supports LN protocol for 128-byte cachelines as a Requester; otherwise, must be 0b.	RO
12:8	***LNR Registration Max*** - This field, encoded as a power of 2, indicates the maximum number of cachelines that this LN Requester is capable of registering concurrently. For example, a value of 00101b indicates that the LN Requester might be capable of registering up to 32 cachelines (2^5) concurrently, and is capable of registering greater than 16.	RO

7.9.14.3 LNR Control Register (Offset 06h)

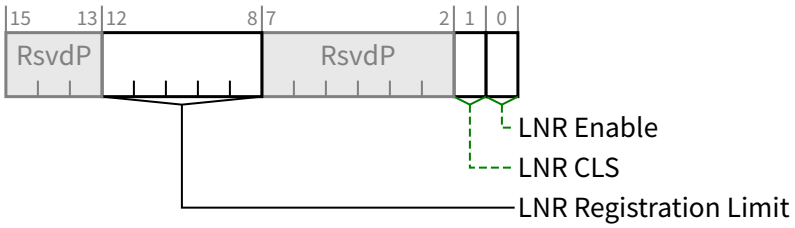

Figure 7-248 LNR Control Register

Table 7-200 LNR Control Register

Bit Location	Register Description	Attributes
0	***LNR Enable*** - When this bit is Set, the Endpoint is enabled to operate as an LN Requester. Software is permitted to Clear this bit at any time. See Section 6.21.4 for requirements regarding the LNR's internal registration state.	RW

Bit Location	Register Description	Attributes
	Default value of this bit is 0b.	
1	***LNR CLS*** - This bit controls or indicates the cache line size used with LN protocol by this Requester. See Section 6.21.4 for restrictions on setting and modifying this bit. If this bit is Clear, the cache line size is 64 bytes. If this bit is Set, the cache line size is 128 bytes. If this LN Requester supports only one cache line size, this bit is permitted to be hardwired to indicate that size. Otherwise, the default value of this bit is 0b.	RW
12:8	***LNR Registration Limit*** - This field, encoded as a power of 2, imposes a limit on the number of cachelines that this LN Requester is permitted to register concurrently. For example, a value of 00100b indicates that the LN Requester must not register more than 16 cachelines (2^4) concurrently. See Section 6.21.4 for restrictions on modifying this field. The default value of this field is 11111b.	RW

7.9.15 *DPC Extended Capability*

The Downstream Port Containment (DPC) Extended Capability is an optional normative capability that provides a mechanism for Downstream Ports to contain uncorrectable errors and enable software to recover from them. See Section 6.2.10 . This capability may be implemented by a Root Port or a Switch Downstream Port. It is not applicable to any other Device/Port type.

If a Downstream Port implements the DPC Extended Capability, that Port must also be capable of reporting the DL_Active state, and indicate so by Setting the Data Link Layer Link Active Reporting Capable bit in the Link Capabilities Register. See Section 7.5.3.6 .

If a Downstream Port implements the DPC Extended Capability, it is strongly recommended for that Port to support ERR_COR Subclass capability, and indicate so by Setting the ERR_COR Subclass Capable bit in the Device Capabilities Register. See Section 7.5.3.3 .

The various RP PIO registers must be implemented only by Root Ports that support RP Extensions for DPC, as indicated by the RP Extensions for DPC bit in the DPC Capability Register.

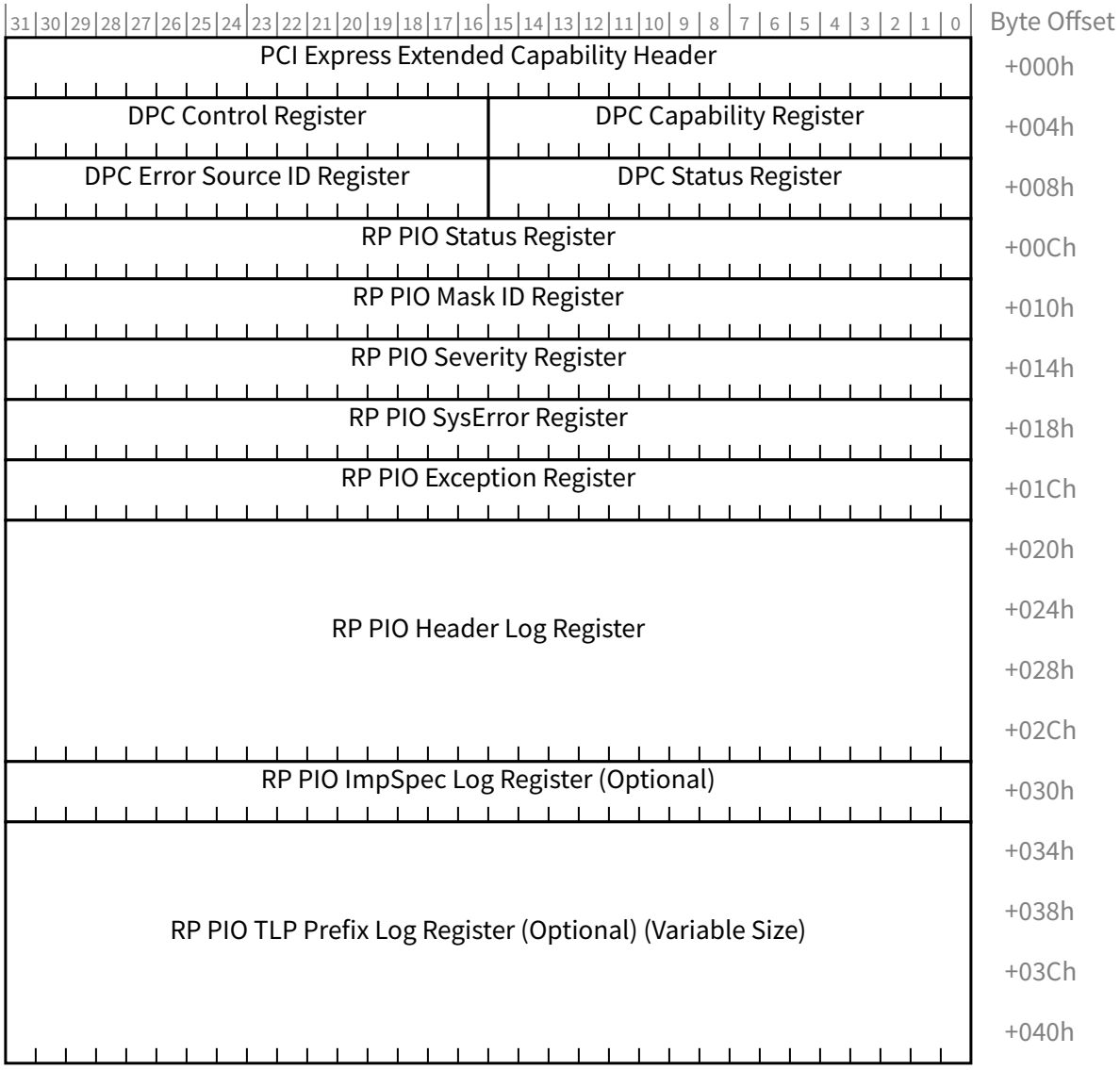

Figure 7-249 DPC Extended Capability

7.9.15.1 DPC Extended Capability Header (Offset 00h)

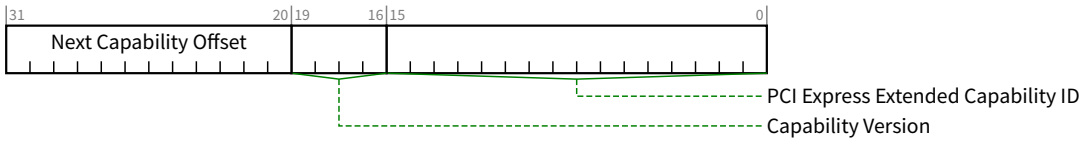

Figure 7-250 DPC Extended Capability Header

Table 7-201 DPC Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. PCI Express Extended Capability ID for the DPC Extended Capability is 001Dh.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of capabilities.	RO

7.9.15.2 DPC Capability Register (Offset 04h)

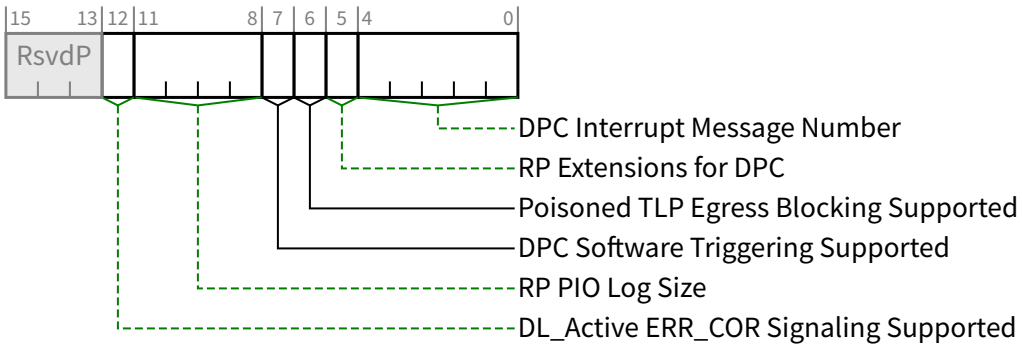

Figure 7-251 DPC Capability Register

Table 7-202 DPC Capability Register

Bit Location	Register Description	Attributes
4:0	***DPC Interrupt Message Number*** - This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with the DPC Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the Message Control Register for MSI. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined.	RO

Bit Location	Register Description	Attributes
5	***RP Extensions for DPC*** - If Set, this bit indicates that a Root Port supports a defined set of DPC Extensions that are specific to Root Ports. Switch Downstream Ports must not Set this bit.	RO
6	***Poisoned TLP Egress Blocking Supported*** - If Set, this bit indicates that the Root Port or Switch Downstream Port supports the ability to block the transmission of a poisoned TLP from its Egress Port. Root Ports that support RP Extensions for DPC must Set this bit.	RO
7	***DPC Software Triggering Supported*** - If Set, this bit indicates that a Root Port or Switch Downstream Port supports the ability for software to trigger DPC. Root Ports that support RP Extensions for DPC must Set this bit.	RO
11:8	***RP PIO Log Size*** - This field indicates how many DWORDs are allocated for the RP PIO log registers, comprised by the RP PIO Header Log, the RP PIO ImpSpec Log, and RP PIO TLP Prefix Log. If the Root Port supports RP Extensions for DPC, the value of this field must be 4 or greater; otherwise, the value of this field must be 0. See Section 7.9.15.11 , Section 7.9.15.12 , and Section 7.9.15.13 .	RO
12	***DL_Active ERR_COR Signaling Supported*** - If Set, this bit indicates that the Root Port or Switch Downstream Port supports the ability to signal with ERR_COR when the Link transitions to the DL_Active state. Root Ports that support RP Extensions for DPC must Set this bit.	RO

7.9.15.3 DPC Control Register (Offset 06h)

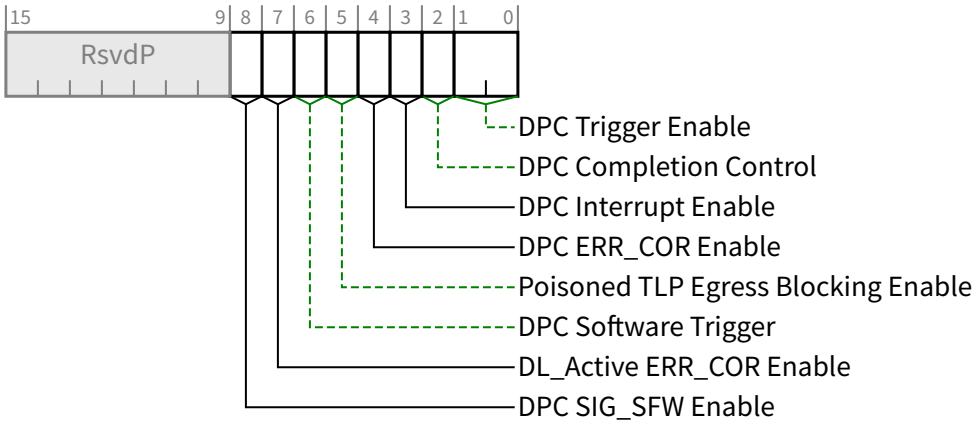

Figure 7-252 DPC Control Register

Table 7-203 DPC Control Register

Bit Location	Register Description	Attributes
1:0	***DPC Trigger Enable*** - This field enables DPC and controls the conditions that cause DPC to be triggered. Defined encodings are: **00b** DPC is disabled **01b** DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_FATAL Message	RW

Bit Location	Register Description	Attributes
	10b DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_NONFATAL or ERR_FATAL Message **11b** Reserved Default value of this field is 00b.	
2	***DPC Completion Control*** - This bit controls the Completion Status for Completions formed during DPC. See Section 2.9.3 . Defined encodings are: **0b** Completer Abort (CA) Completion Status **1b** Unsupported Request (UR) Completion Status Default value of this bit is 0b.	RW
3	***DPC Interrupt Enable*** - When Set, this bit enables the generation of an interrupt to indicate that DPC has been triggered. See Section 6.2.10.1 . Default value of this bit is 0b.	RW
4	***DPC ERR_COR Enable*** - When Set, this bit enables the sending of an ERR_COR Message to indicate that DPC has been triggered. See Section 6.2.10.2 . Default value of this bit is 0b.	RW
5	***Poisoned TLP Egress Blocking Enable*** - This bit must be RW if the Poisoned TLP Egress Blocking Supported bit is Set; otherwise, it is permitted to be hardwired to 0b. Software must not Set this bit unless the Poisoned TLP Egress Blocking Supported bit is Set. When Set, this bit enables the associated Egress Port to block the transmission of poisoned TLPs. See Section 2.7.2.2 . Default value of this bit is 0b.	RW/RO
6	***DPC Software Trigger*** - This bit must be RW if the DPC Software Triggering Supported bit is Set; otherwise, it is permitted to be hardwired to 0b. If DPC is enabled and the DPC Trigger Status bit is Clear, when software writes 1b to this bit, DPC is triggered. Otherwise, software writing a 1b to this bit has no effect. It is permitted to write 1b to this bit while simultaneously writing updated values to other fields in this register, notably the DPC Trigger Enable field. For this case, the DPC Software Trigger semantics are based on the updated value of the DPC Trigger Enable field. This bit always returns 0b when read.	RW/RO
7	***DL_Active ERR_COR Enable*** - This bit must be RW if the DL_Active ERR_COR Signaling Supported bit is Set; otherwise, it is permitted to be hardwired to 0b. Software must not Set this bit unless the DL_Active ERR_COR Signaling Supported bit is Set. When Set, this bit enables the associated Downstream Port to signal with ERR_COR when the Link transitions to the DL_Active state. See Section 6.2.10.5 . Default value of this bit is 0b.	RW/RO
8	***DPC SIG_SFW Enable*** - This bit must be implemented if the ERR_COR Subclass Capable bit in the Device Capabilities Register is Set; otherwise, it is permitted to be hardwired to 0b. If the ERR_COR Subclass Capable bit is Clear and software Sets this bit, the behavior is undefined. When Set, this bit enables sending an ERR_COR Message to indicate a DPC event that's been enabled for ERR_COR signaling. See Section 6.2.10.2 and Section 6.2.10.5 . This is an additional and alternative way to enable overall DPC ERR_COR signaling beyond the Correctable Error Reporting Enable bit in the	RW/RO

Bit Location	Register Description	Attributes
	Device Control Register. This bit does not affect a Function's ability to send ERR_COR Messages other than the ECS SIG_SFW subclass. Default value of this bit is 0b.	

7.9.15.4 DPC Status Register (Offset 08h)

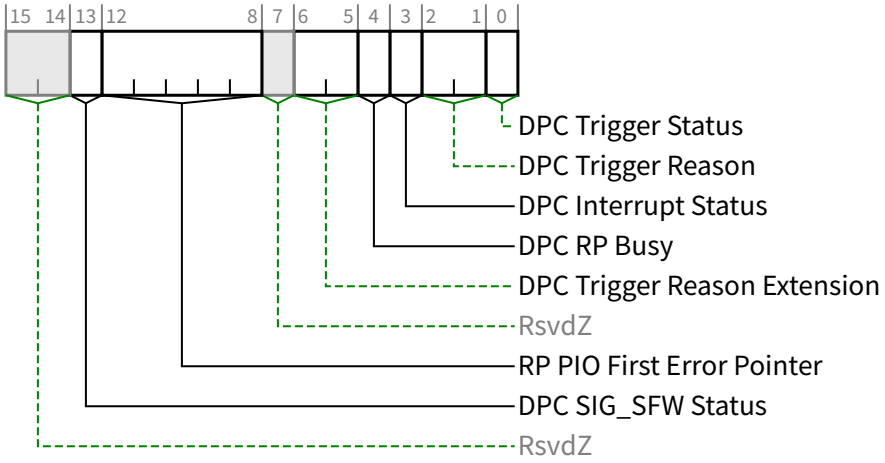

Figure 7-253 DPC Status Register

Table 7-204 DPC Status Register

Bit Location	Register Description	Attributes
0	***DPC Trigger Status*** - When Set, this bit indicates that DPC has been triggered, and by definition the Port is "in DPC". DPC is event triggered. While this bit is Set, hardware must direct the LTSSM to the Disabled State. This bit must be cleared before the LTSSM can be released from the Disabled State, after which the Port is no longer in DPC, and the LTSSM must transition to the Detect State. See Section 6.2.10 for requirements on how long software must leave the Downstream Port in DPC. Once these requirements are met, software is permitted to clear this bit regardless of the state of other status bits associated with the triggering event. After clearing this bit, software must honor timing requirements defined in Section 6.6.1 with respect to the first Configuration Read following a Conventional Reset. Default value of this bit is 0b.	RW1CS
2:1	***DPC Trigger Reason*** - This field indicates why DPC has been triggered. Defined encodings are: **00b** DPC was triggered due to an unmasked uncorrectable error **01b** DPC was triggered due to receiving an ERR_NONFATAL **10b** DPC was triggered due to receiving an ERR_FATAL **11b** DPC was triggered due to a reason that is indicated by the DPC Trigger Reason Extension field.	ROS

Bit Location	Register Description	Attributes
	This field is valid only when the DPC Trigger Status bit is Set; otherwise the value of this field is undefined.	
3	***DPC Interrupt Status*** - This bit is Set if DPC is triggered while the DPC Interrupt Enable bit is Set. This may cause the generation of an interrupt. See Section 6.2.10.1 . Default value of this bit is 0b.	RW1CS
4	***DPC RP Busy*** - When the DPC Trigger Status bit is Set and this bit is Set, the Root Port is busy with internal activity that must complete before software is permitted to Clear the DPC Trigger Status bit. If software Clears the DPC Trigger Status bit while this bit is Set, the behavior is undefined. This field is valid only when the DPC Trigger Status bit is Set; otherwise the value of this field is undefined. This bit is applicable only for Root Ports that support RP Extensions for DPC, and is Reserved for Switch Downstream Ports. Default value of this bit is undefined.	RO/RsvdZ
6:5	***DPC Trigger Reason Extension*** - This field serves as an extension to the DPC Trigger Reason field. When that field is valid and has a value of 11b, this field indicates why DPC has been triggered. Defined encodings are: **00b** DPC was triggered due to an RP PIO error **01b** DPC was triggered due to the DPC Software Trigger bit **10b** Reserved **11b** Reserved This field is valid only when the DPC Trigger Status bit is Set and the value of the DPC Trigger Reason field is 11b; otherwise the value of this field is undefined.	ROS
12:8	***RP PIO First Error Pointer*** - The value of this field identifies a bit position in the RP PIO Status Register, and this field is considered valid when that bit is Set. When this field is valid, and software writes a 1b to the indicated RP PIO Status bit (thus clearing it), this field must revert to its default value. This field is applicable only for Root Ports that support RP Extensions for DPC, and otherwise is Reserved. If this field is not Reserved, its default value is 11111b, indicating a permanently Reserved RP PIO Status bit, thus guaranteeing that this field is not considered valid.	ROS/RsvdZ
13	***DPC SIG_SFW Status*** - If the Function supports ERR_COR Subclass capability, this bit must be implemented; otherwise, it must be hardwired to 0b. If implemented, this bit is Set when a SIG_SFW ERR_COR Message is sent to signal a DPC event. See Section 6.2.10.2 and Section 6.2.10.5 . Default value of this bit is 0b	RW1CS/RsvdZ

7.9.15.5 DPC Error Source ID Register (Offset 0Ah)

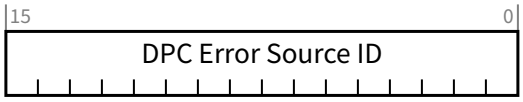

Figure 7-254 DPC Error Source ID Register

Table 7-205 DPC Error Source ID Register

Bit Location	Register Description	Attributes
15:0	***DPC Error Source ID*** - When the DPC Trigger Reason field indicates that DPC was triggered due to the reception of an ERR_NONFATAL or ERR_FATAL, this register contains the Requester ID of the received Message. Otherwise, the value of this register is undefined.	ROS

7.9.15.6 RP PIO Status Register (Offset 0Ch)

This register is present only in Root Ports that support RP Extensions for DPC. See Section 6.2.10.3 .

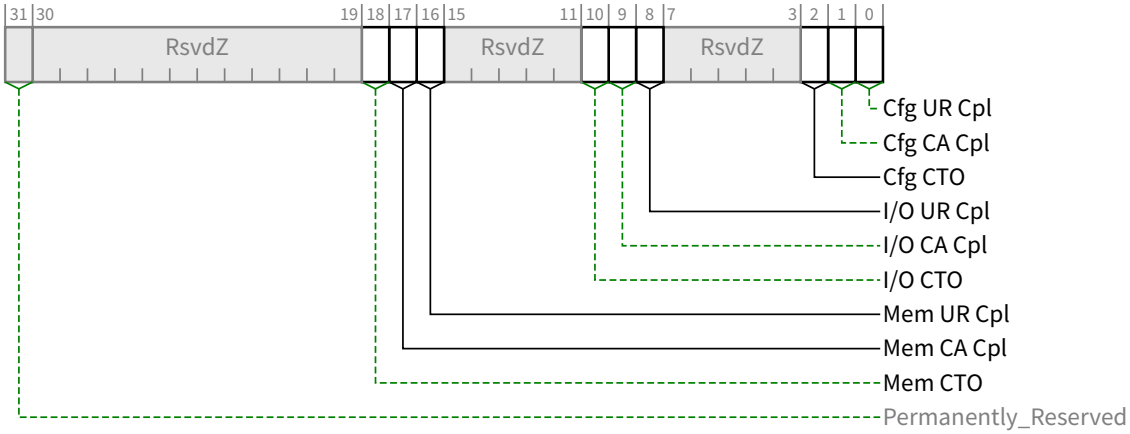

Figure 7-255 RP PIO Status Register

Table 7-206 RP PIO Status Register

Bit Location	Register Description	Attributes	Default
0	***Cfg UR Cpl*** - Configuration Request received UR Completion	RW1CS	0b
1	***Cfg CA Cpl*** - Configuration Request received CA Completion	RW1CS	0b
2	***Cfg CTO*** - Configuration Request Completion Timeout	RW1CS	0b

Bit Location	Register Description	Attributes	Default
8	***I/O UR Cpl*** - I/O Request received UR Completion	RW1CS	0b
9	***I/O CA Cpl*** - I/O Request received CA Completion	RW1CS	0b
10	***I/O CTO*** - I/O Request Completion Timeout	RW1CS	0b
16	***Mem UR Cpl*** - Memory Request received UR Completion	RW1CS	0b
17	***Mem CA Cpl*** - Memory Request received CA Completion	RW1CS	0b
18	***Mem CTO*** - Memory Request Completion Timeout	RW1CS	0b
31	**Permanently_Reserved**, since the default RP PIO First Error Pointer field value points to it.	RsvdZ	0b

7.9.15.7 RP PIO Mask Register (Offset 10h)

This register is present only in Root Ports that support RP Extensions for DPC. See Section 6.2.10.3 .

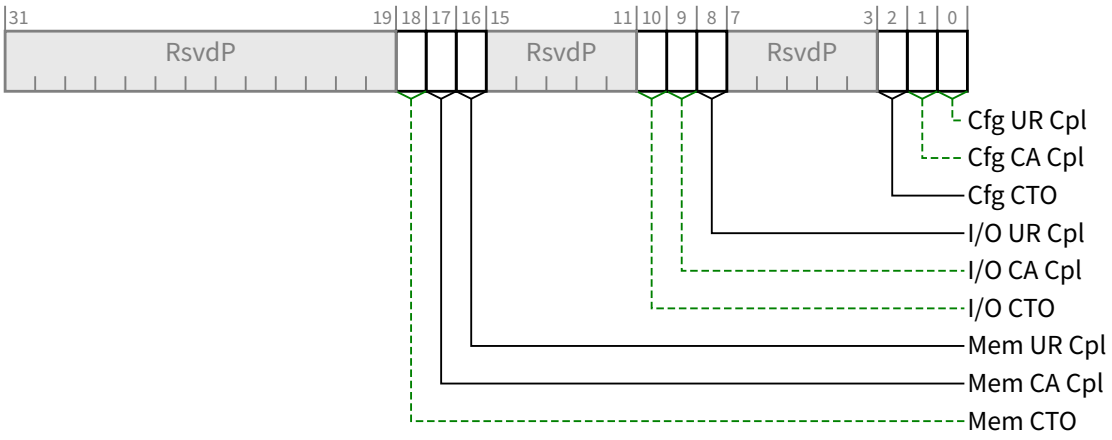

Figure 7-256 RP PIO Mask Register

Table 7-207 RP PIO Mask Register

Bit Location	Register Description	Attributes	Default
0	***Cfg UR Cpl*** - Configuration Request received UR Completion	RWS	1b
1	***Cfg CA Cpl*** - Configuration Request received CA Completion	RWS	1b
2	***Cfg CTO*** - Configuration Request Completion Timeout	RWS	1b
8	***I/O UR Cpl*** - I/O Request received UR Completion	RWS	1b
9	***I/O CA Cpl*** - I/O Request received CA Completion	RWS	1b
10	***I/O CTO*** - I/O Request Completion Timeout	RWS	1b

Bit Location	Register Description	Attributes	Default
16	***Mem UR Cpl*** - Memory Request received UR Completion	RWS	1b
17	***Mem CA Cpl*** - Memory Request received CA Completion	RWS	1b
18	***Mem CTO*** - Memory Request Completion Timeout	RWS	1b

7.9.15.8 RP PIO Severity Register (Offset 14h)

This register is present only in Root Ports that support RP Extensions for DPC. See Section 6.2.10.3 .

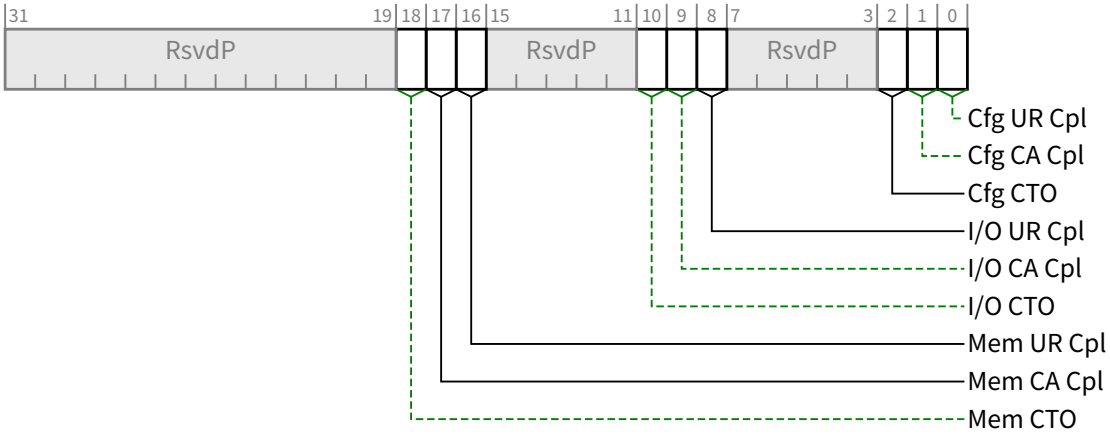

Figure 7-257 RP PIO Severity Register

Table 7-208 RP PIO Severity Register

Bit Location	Register Description	Attributes	Default
0	***Cfg UR Cpl*** - Configuration Request received UR Completion	RWS	0b
1	***Cfg CA Cpl*** - Configuration Request received CA Completion	RWS	0b
2	***Cfg CTO*** - Configuration Request Completion Timeout	RWS	0b
8	***I/O UR Cpl*** - I/O Request received UR Completion	RWS	0b
9	***I/O CA Cpl*** - I/O Request received CA Completion	RWS	0b
10	***I/O CTO*** - I/O Request Completion Timeout	RWS	0b
16	***Mem UR Cpl*** - Memory Request received UR Completion	RWS	0b
17	***Mem CA Cpl*** - Memory Request received CA Completion	RWS	0b
18	***Mem CTO*** - Memory Request Completion Timeout	RWS	0b

7.9.15.9 RP PIO SysError Register (Offset 18h)

This register is present only in Root Ports that support RP Extensions for DPC. See Section 6.2.10.3 .

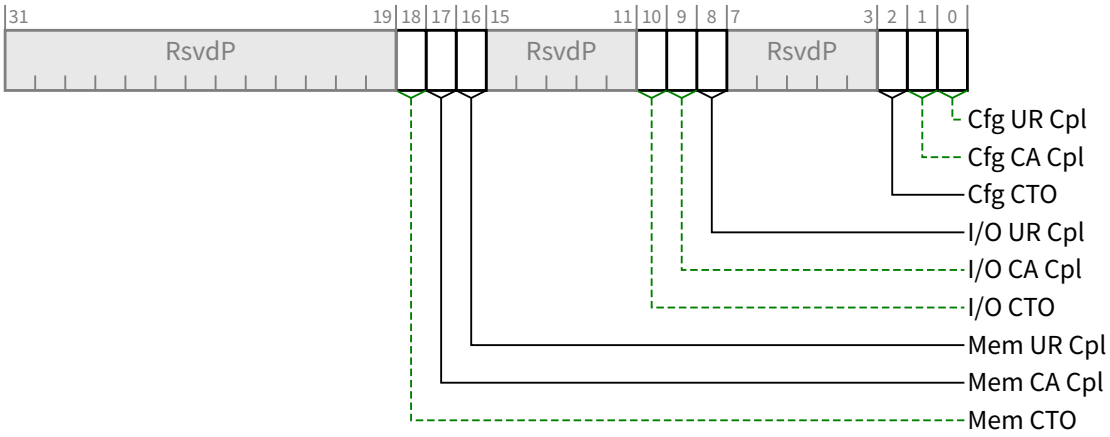

Figure 7-258 RP PIO SysError Register

Table 7-209 RP PIO SysError Register

Bit Location	Register Description	Attributes	Default
0	***Cfg UR Cpl*** - Configuration Request received UR Completion	RWS	0b
1	***Cfg CA Cpl*** - Configuration Request received CA Completion	RWS	0b
2	***Cfg CTO*** - Configuration Request Completion Timeout	RWS	0b
8	***I/O UR Cpl*** - I/O Request received UR Completion	RWS	0b
9	***I/O CA Cpl*** - I/O Request received CA Completion	RWS	0b
10	***I/O CTO*** - I/O Request Completion Timeout	RWS	0b
16	***Mem UR Cpl*** - Memory Request received UR Completion	RWS	0b
17	***Mem CA Cpl*** - Memory Request received CA Completion	RWS	0b
18	***Mem CTO*** - Memory Request Completion Timeout	RWS	0b

7.9.15.10 RP PIO Exception Register (Offset 1Ch)

This register is present only in Root Ports that support RP Extensions for DPC. See Section 6.2.10.3 .

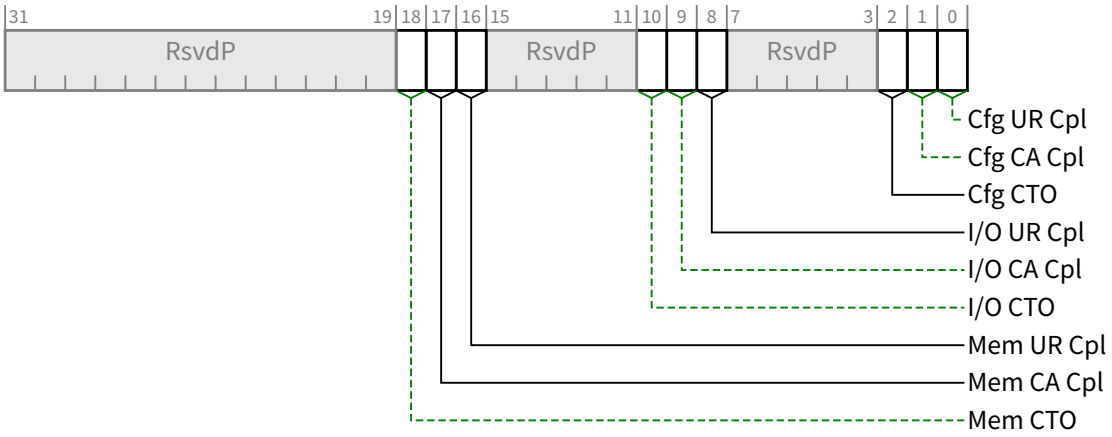

Figure 7-259 RP PIO Exception Register

Table 7-210 RP PIO Exception Register

Bit Location	Register Description	Attributes	Default
0	***Cfg UR Cpl*** - Configuration Request received UR Completion	RWS	0b
1	***Cfg CA Cpl*** - Configuration Request received CA Completion	RWS	0b
2	***Cfg CTO*** - Configuration Request Completion Timeout	RWS	0b
8	***I/O UR Cpl*** - I/O Request received UR Completion	RWS	0b
9	***I/O CA Cpl*** - I/O Request received CA Completion	RWS	0b
10	***I/O CTO*** - I/O Request Completion Timeout	RWS	0b
16	***Mem UR Cpl*** - Memory Request received UR Completion	RWS	0b
17	***Mem CA Cpl*** - Memory Request received CA Completion	RWS	0b
18	***Mem CTO*** - Memory Request Completion Timeout	RWS	0b

7.9.15.11 RP PIO Header Log Register (Offset 20h)

This register is implemented only in Root Ports that support RP Extensions for DPC. The RP PIO Header Log Register contains the header from the Request TLP associated with a recorded RP PIO error. Refer to Section 6.2.10.3 for further details. This register is 16 bytes and is formatted identically to the Header Log register in AER. See Section 7.8.4.8 .

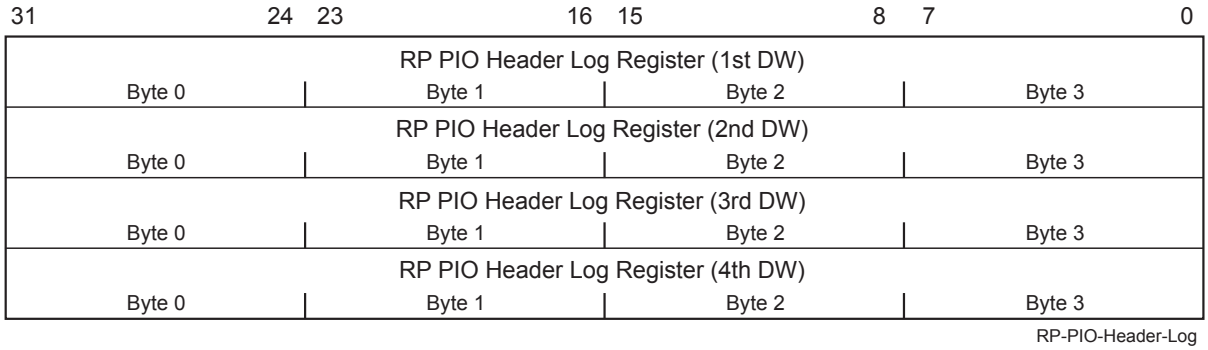

Figure 7-260 RP PIO Header Log Register

Table 7-211 RP PIO Header Log Register

Bit Location	Register Description	Attributes	Default
127:0	***TLP Header*** - of the TLP associated with the error	ROS	0

7.9.15.12 RP PIO ImpSpec Log Register (Offset 30h)

This register is permitted to be implemented only in Root Ports that support RP Extensions for DPC. The RP PIO ImpSpec Log Register, if implemented, contains implementation-specific information associated with the recorded error, e.g., indicating the source of the Request TLP. Space is allocated for this register if the value of the RP PIO Log Size field is 5 or greater. If space is allocated for the register, but the register is not implemented, the bits must be hardwired to 0b.

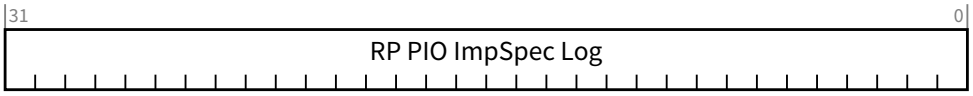

Figure 7-261 RP PIO ImpSpec Log Register

Table 7-212 RP PIO ImpSpec Log Register

Bit Location	Register Description	Attributes	Default
31:0	***RP PIO ImpSpec Log***	ROS	0

7.9.15.13 RP PIO TLP Prefix Log Register (Offset 34h)

This register is permitted to be implemented only in Root Ports that support RP Extensions for DPC. The RP PIO TLP Prefix Log Register contains any End-End TLP Prefixes from the TLP corresponding to a recorded RP PIO error. Refer to Section 6.2.10.3 for further details.

If the Root Port supports tracking Non-Posted Requests that contain End-End TLP Prefixes, this register must be implemented, and must be of sufficient size to record the maximum number of End-End TLP Prefixes for any tracked Request. See Section 2.9.3 . The allocated size in DWORDs of the RP PIO TLP Prefix Log Register is the RP PIO Log Size

minus 5 if the RP PIO Log Size is 9 or less, or 4 if the RP PIO Log Size is greater than 9. The implemented size of the TLP Prefix Log must be less than or equal to the Root Port's Max End-End TLP Prefixes field value. For the case where the Root Port never transmits Non-Posted Requests containing End-End TLP Prefixes, the allocated and implemented size of the TLP Prefix Log is permitted to be 0. Any DWORDs allocated but not implemented must be hardwired to zero.

This register is formatted identically to the TLP Prefix Log register in AER, although this register's allocated size is variable, whereas the register in AER is always 4 DWORDs. See Section 7.8.4.12 . The First TLP Prefix Log register contains the first End-End TLP Prefix from the TLP, the Second TLP Prefix Log register contains the second End-End TLP Prefix, and so forth. If the TLP contains fewer TLP Prefixes than this register accommodates, any remaining TLP Prefix Log registers must contain zero.

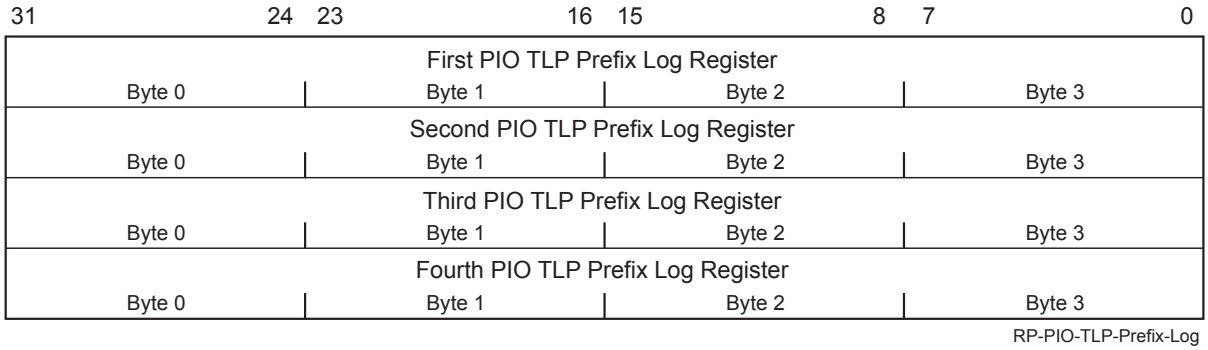

Figure 7-262 RP PIO TLP Prefix Log Register

Table 7-213 RP PIO TLP Prefix Log Register

Bit Location	Register Description	Attributes	Default
127:0	***RP PIO TLP Prefix Log***	ROS	0

7.9.16 *Precision Time Management Extended Capability (PTM Capability)*

The Precision Time Management Extended Capability is an optional Extended Capability for discovering and controlling the distribution of a PTM Hierarchy. For Root Complexes, this Capability is required in any Root Port, RCiEP, or RCRB that supports PTM. For Endpoints and Switch Upstream Ports that support PTM, this Capability is required in exactly one Function of the Upstream Port and that Capability controls the PTM behavior of all PTM capable Functions associated with that Upstream Port. For Switch Downstream Ports, PTM behavior is controlled by the same PTM Capability that controls the associated Switch Upstream Port. The PTM Capability is not permitted in Bridges, Switch Downstream Ports, and Root Complex Event Collectors.

For Switches, a single instance of this Capability controls behavior for the entire Switch. If the Upstream Port of the Switch is associated with an MFD, it is not required that the controlling Function be the Function corresponding to the Switch Upstream Port. For a given Switch, if this Capability is present, all Downstream Ports of the Switch must implement the requirements defined in Section 6.22.3.2 .

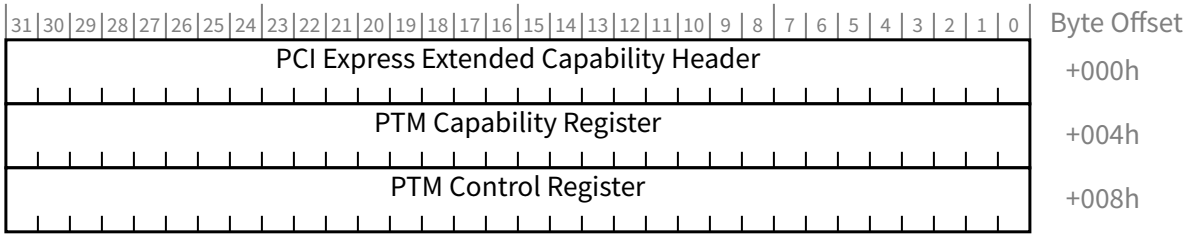

Figure 7-263 PTM Capability Structure

7.9.16.1 PTM Extended Capability Header (Offset 00h)

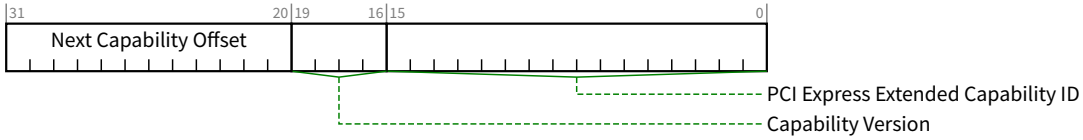

Figure 7-264 PTM Extended Capability Header

Table 7-214 PTM Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Precision Time Measurement Capability is 001Fh.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.9.16.2 PTM Capability Register (Offset 04h)

This register describes a Function's support for Precision Time Measurement. Not all fields within this register apply to all Functions capable of implementing PTM.

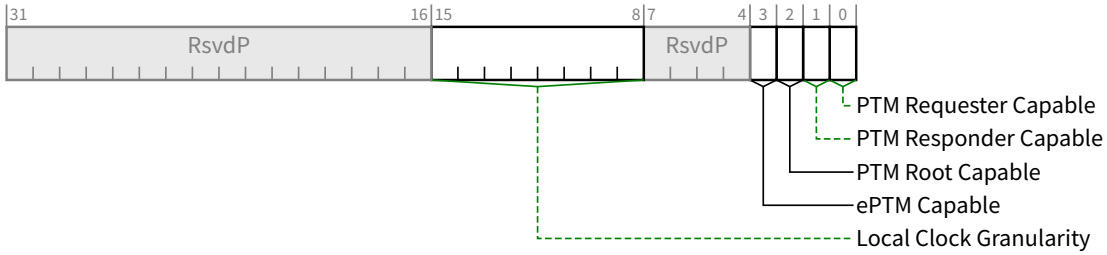

Figure 7-265 PTM Capability Register

Table 7-215 PTM Capability Register

Bit Location	Register Description	Attributes
0	***PTM Requester Capable*** - Indicates the Function implements the PTM Requester role (see Section 6.22.3.1). Endpoints and RCiEPs are permitted to Set this bit to indicate that they implement the PTM Requester role. Switch Upstream Ports must Set this bit if the Switch contains one or more of the following: • A Downstream Port that implements the PTM Responder role. • An additional Function that implements the PTM Requester role. If a Device contains multiple Upstream Port Functions, the value of this bit must be consistent across all such Functions.	HwInit
1	***PTM Responder Capable*** - Root Ports and RCRBs are permitted to, and Switches supporting PTM must, Set this bit to indicate they implement the PTM Responder role (see Section 6.22.3.2). If PTM Root Capable is Set, then this bit must be Set.	HwInit
2	***PTM Root Capable*** - Root Ports, RCRBs, and Switches are permitted to Set this bit if they are capable of being a source of PTM Master Time (see Section 6.22.1). All other Functions must hardwire this bit to 0b.	HwInit
3	***ePTM Capable*** - If Set, indicates that this device supports Enhanced Precision Time Management (ePTM). It is strongly recommended that this bit be Set in all PTM Devices.	HwInit
15:8	***Local Clock Granularity*** - Encodings are: **0000 0000b** — Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. **0000 0001b to 1111 1110b** — Indicates the period of this Time Source's local clock in ns. **1111 1111b** — Indicates the period of this Time Source's local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy. This field is RsvdP if the PTM Root Capable bit is 0b.	HwInit/RsvdP

7.9.16.3 PTM Control Register (Offset 08h)

This register controls a Function's participation in the Precision Time Measurement mechanism. Not all fields within this register apply to all Functions capable of implementing PTM.

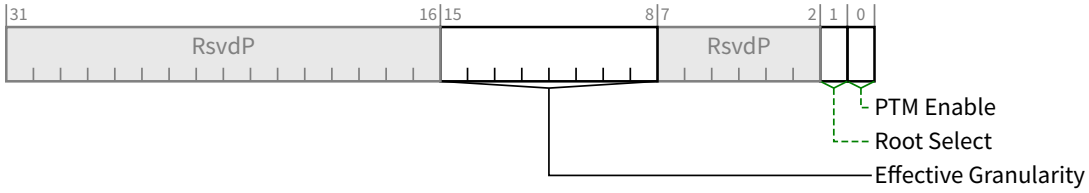

Figure 7-266 PTM Control Register

Table 7-216 PTM Control Register

Bit Location	Register Description	Attributes
0	***PTM Enable*** - When Set, this Function is permitted to participate in the PTM mechanism according to its selected role(s) (see Section 6.22.2). Default value is 0b.	RW
1	***Root Select*** - When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root. Default value is 0b.If the value of the PTM Root Capable bit is 0b, this bit is permitted to be hardwired to 0b.	RW/RO
15:8	***Effective Granularity*** - For Functions implementing the PTM Requester Role, this field provides information relating to the expected accuracy of the PTM clock, but does not otherwise affect the PTM mechanism. For Endpoints, system software must program this field to the value representing the maximum Local Clock Granularity reported by the PTM Root and all intervening PTM Time Sources. For RCiEPs, system software must set this field to the value reported in the Local Clock Granularity field by the associated PTM Time Source. Permitted values: **0000 0000b** — Unknown PTM granularity - one or more Switches between this Function and the PTM Root reported a Local Clock Granularity value of 0000 0000b. **0000 0001b to 1111 1110b** — Indicates the effective PTM granularity in ns. **1111 1111b** — Indicates the effective PTM granularity is greater than 254 ns. Default value is 00000b. If PTM Requester Capable is Clear, this field is permitted to be hardwired to 0000 0000b.	RW/RO

7.9.17 Readiness Time Reporting Extended Capability

The Readiness Time Reporting Extended Capability provides an optional mechanism for describing the time required for a Device or Function to become Configuration-Ready. In the indicated situations, software is permitted to issue Requests to the Device or Function after waiting for the time advertised in this capability and need not wait for the (longer) times required elsewhere.

Software is permitted to issue requests upon the earliest of:

- Receiving a Readiness Notifications message (see Section 6.23).
- Waiting the appropriate time as specified in this document or in applicable specifications including the [PCI] and the [PCI-PM].
- Waiting the time indicated in the associated field of this capability.
- Waiting the time defined by system software or firmware[157] .

Software is permitted to cache values from this capability and to use those cached values as long as the same device operating in the same manner has not changed.

This capability is permitted to be implemented in all Functions.

A Function must be Configuration-Ready if:

- The Immediate Readiness bit is Clear and at least Reset Time has elapsed after the completion of Conventional Reset
  - If the Immediate Readiness bit is Set, Reset Time does not apply, and is Reserved
- The Function is associated with an Upstream Port and at least DL_Up Time has elapsed after the Downstream Port above that Function reported Data Link Layer Link Active (see Section 7.5.3.8).
- The Function supports Function Level Reset and at least FLR Time has elapsed after that Function was issued a Function Level Reset.
- Immediate_Readiness_on_Return_to_D0 is Clear and at least $D3_{Hot}$ to D0 Time has elapsed after that Function was directed to the D0 state from $D3_{Hot}$.
  - If the Immediate_Readiness_on_Return_to_D0 bit is Set, $D3_{Hot}$ to D0 Time does not apply, and is Reserved

When Immediate_Readiness_on_Return_to_D0 is Clear, a Function must be Configuration-Ready when at least $D3_{Hot}$ to D0 Time has elapsed after the Function was directed to the D0 state from $D3_{Hot}$. In addition, the Function must be in either the $D0_{uninitialized}$ or $D0_{active}$ state, depending on the value of the No_Soft_Reset bit.

For VFs additional behavior is defined in Chapter 9 .

If the above conditions do not apply, Function behavior is not determined by the Readiness Time Reporting Extended Capability, and the Function must respond as defined elsewhere (including, for example, no response or a response with Configuration Retry Status).

The time values reported are determined by implementation-specific mechanisms. A Valid bit is defined in this capability to permit a device to defer reporting time values, for example to allow hardware initialization through driver-based mechanisms. If the Valid bit remains Clear and 1 minute has elapsed after device driver(s) have started, software is permitted to assume that no values will be reported.

157. For example, using ACPI tables to provide the equivalent of this capability.

Registers and fields in the Readiness Time Reporting Extended Capability are shown in Figure 7-267 . Time values are encoded in floating point as shown in Figure 7-268 . The actual time value is *Value* × *Multiplier[Scale]*. For example, the value A1Eh represents about 1 second (actually 1.006 sec) and the value 80Ah represents about 10 ms (actually 10.240 ms).

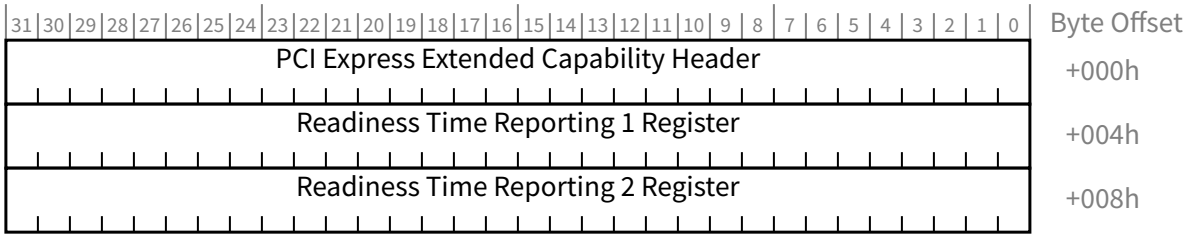

Figure 7-267 Readiness Time Reporting Extended Capability

Scale	Multiplier
0	1 ns
1	32 ns
2	1,024 ns
3	32,768 ns
4	1,048,576 ns
5	33,554,432 ns
6	Reserved
7	Reserved

$$\text{Multiplier} = 32^{\text{Scale}}$$

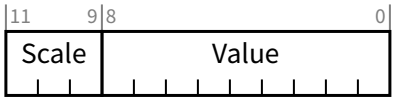

Figure 7-268 Readiness Time Encoding

7.9.17.1 Readiness Time Reporting Extended Capability Header (Offset 00h)

Figure 7-269 and Table 7-217 detail allocation of fields in the Extended Capability header.

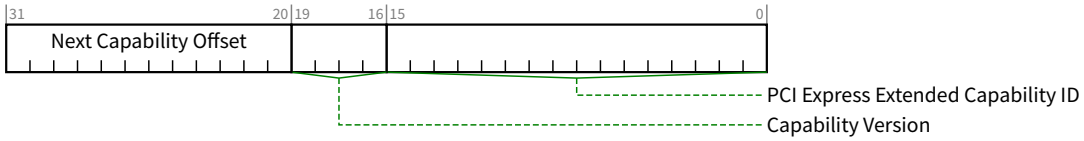

Figure 7-269 Readiness Time Reporting Extended Capability Header

Table 7-217 Readiness Time Reporting Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Readiness Time Reporting Extended Capability is 0022h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.17.2 Readiness Time Reporting 1 Register (Offset 04h)

Figure 7-270 and Table 7-218 detail allocation of fields in the Readiness Time Reporting 1 Register.

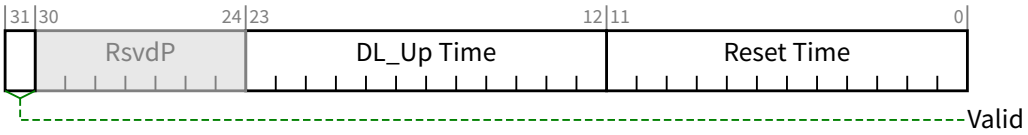

Figure 7-270 Readiness Time Reporting 1 Register

Table 7-218 Readiness Time Reporting 1 Register

Bit Location	Register Description	Attributes
11:0	***Reset Time*** - is the time the Function requires to become Configuration-Ready after the completion of Conventional Reset. This field is RsvdP if the Immediate Readiness bit is Set. This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value A1Eh.	HwInit/RsvdP
23:12	***DL_Up Time*** - is the time the Function requires to become Configuration-Ready after the Downstream Port above the Function reports Data Link Layer Link Active. This field is RsvdP in Functions that are not associated with an Upstream Port. This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value A1Eh.	HwInit/RsvdP
31	***Valid*** - If Set, indicates that all time values in this capability are valid. If Clear, indicates that the time values in this capability are not yet available.	HwInit

Bit Location	Register Description	Attributes
	Time values may depend on device configuration. Device specific mechanisms, possibly involving the device driver(s), could be involved in determining time values. If this bit remains Clear and 1 minute has elapsed after all associated device driver(s) have started, software is permitted to assume that this bit will never be set.	

7.9.17.3 Readiness Time Reporting 2 Register (Offset 08h)

Figure 7-271 and Table 7-219 detail allocation of fields in the Readiness Time Reporting 2 Register.

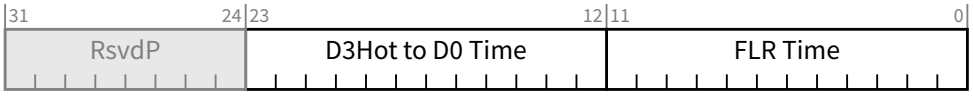

Figure 7-271 Readiness Time Reporting 2 Register

Table 7-219 Readiness Time Reporting 2 Register

Bit Location	Register Description	Attributes
11:0	***FLR Time*** - is the time that the Function requires to become Configuration-Ready after it was issued an FLR. This field is RsvdP when the Function Level Reset Capability bit is Clear (see Section 7.5.3.3). This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value A1Eh.	HwInit/RsvdP
23:12	***$D3_{Hot}$ to D0 Time*** - If Immediate_Readiness_on_Return_to_D0 is Clear, $D3_{Hot}$ to D0 Time is the time that the Function requires after it is directed from $D3_{Hot}$ to D0 before it is Configuration-Ready and has returned to either $D0_{uninitialized}$ or $D0_{active}$ state (see the *PCI Bus Power Management Interface Specification*). This field is RsvdP if the Immediate_Readiness_on_Return_to_D0 bit is Set. This field is undefined when the Valid bit is Clear. This field must be less than or equal to the encoded value 80Ah.	HwInit/RsvdP

7.9.18 Hierarchy ID Extended Capability

The Hierarchy ID Extended Capability provides an optional mechanism for passing a unique identifier to Functions within a Hierarchy. At most one instance of this capability is permitted in a Function. This capability is not applicable to Bridges, Root Complex Event Collectors, and RCRBs.

This capability takes three forms:

In Upstream Ports:

- This capability is permitted any Function associated with an Upstream Port.

- This capability is optional in Switch Upstream Ports. Support in Switch Upstream and Downstream Ports is independently optional.
- This capability is mandatory in Functions that use the Hierarchy ID Message. This includes use by the Function's driver.
- Functions, other than VFs, that have Hierarchy ID Writeable Clear, must report the Message Requester ID, Hierarchy ID, System GUID Authority ID, and System GUID fields from the most recently received Hierarchy ID Message.
- All VFs that have Hierarchy ID Writeable Clear, must report the same Hierarchy ID Valid, Message Requester ID, Hierarchy ID, System GUID Authority ID, and System GUID values as their associated PF.
- PFs must implement this capability if any of their VFs implement this capability.
- Functions that have Hierarchy ID Writeable Set must report the Hierarchy ID Valid, Message Requester ID, Hierarchy ID, System GUID Authority ID, and System GUID values programmed by software.

In Downstream Ports:

- This capability is permitted in any Downstream Port. It is recommended that it be implemented in Root Ports.
- When present in a Switch Downstream Port, this capability must be implemented in all Downstream Ports of the Switch. Support in Switch Upstream and Downstream Ports is independently optional.
- In Downstream Ports, the Hierarchy ID, System GUID Authority ID, and System GUID fields are Read / Write and contain the values to send in the Hierarchy ID Message.
- A Hierarchy ID capability is not affected by Hierarchy ID Messages forwarded through the associated Downstream Port.

In RCiEPs:

- VFs that have Hierarchy ID Writeable Clear must report the same Message Requester ID, Hierarchy ID, System GUID Authority ID, and System GUID values as their associated PF.
- PFs must implement this capability if any of their VFs implement this capability.
- Functions, other than VFs, that have Hierarchy ID Writeable Clear, must report the same Hierarchy ID Valid, Message Requester ID, Hierarchy ID, System GUID Authority ID, and System GUID values. The source of this information is outside the scope of this specification.
- Functions that have Hierarchy ID Writeable Set must report the Hierarchy ID Valid, Message Requester ID, Hierarchy ID, System GUID Authority ID, and System GUID values programmed by software.

Figure 7-272 details the layout of the Hierarchy ID Extended Capability.

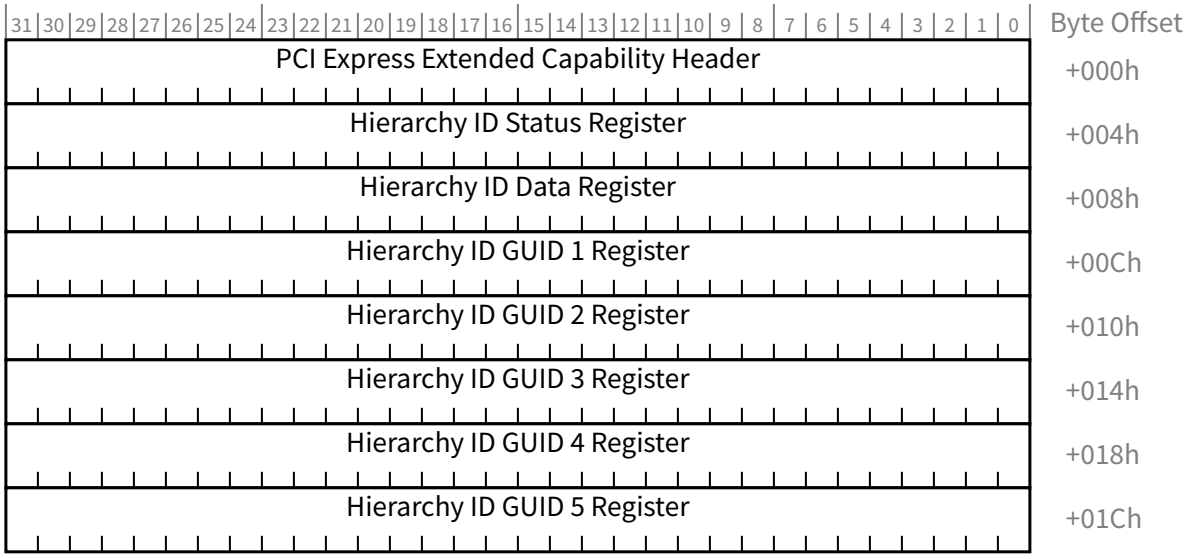

Figure 7-272 Hierarchy ID Extended Capability

7.9.18.1 Hierarchy ID Extended Capability Header (Offset 00h)

Figure 7-273 and Table 7-220 detail allocation of fields in the Hierarchy ID Extended Capability Header.

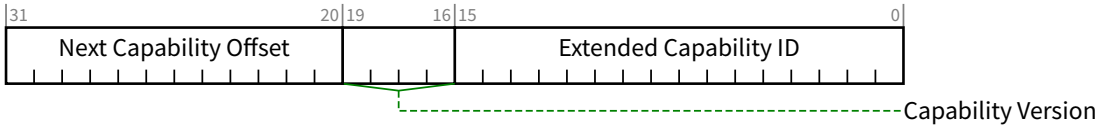

Figure 7-273 Hierarchy ID Extended Capability Header

Table 7-220 Hierarchy ID Extended Capability Header

Bit Location	Description	Attributes
15:0	***Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Hierarchy ID Extended Capability is 0028h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities in configuration space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating the list of Capabilities) or greater than 0FFh.	RO

7.9.18.2 Hierarchy ID Status Register (Offset 04h)

Figure 7-274 and Table 7-221 detail allocation of fields in the Hierarchy ID Status Register.

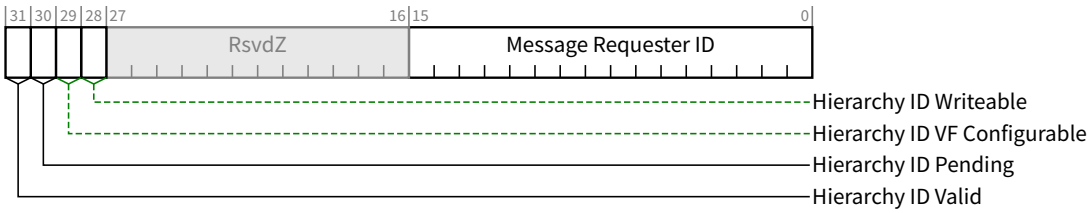

Figure 7-274 Hierarchy ID Status Register

Table 7-221 Hierarchy ID Status Register

Bit Location	Description	Attributes
15:0	***Message Requester ID*** - In an Upstream Port, this field contains the Requester ID from the most recently received Hierarchy ID Message. This field is meaningful only if Hierarchy ID Valid is 1b. This value identifies the Downstream Port (within this Hierarchy) that sent the Hierarchy ID Message. This information is not considered part of the Hierarchy ID as it can vary within the Hierarchy (e.g., different Root Ports of one Root Complex), but helps in debug situations to identify the provenance of the Hierarchy ID information. In a Downstream Port, this field is RsvdZ. For RCiEPs, this field is RsvdZ. This field defaults to 0000h.	RO/RsvdZ
28	***Hierarchy ID Writeable*** - This bit is Set to indicate that the Hierarchy ID Data and GUID registers are read/write. This bit is Clear to indicate that the Hierarchy ID and GUID registers are read only. In Downstream Ports this bit is hardwired to 1b. In Upstream Ports, Functions that are not VFs must hardwire this bit to 0b. RCiEPs that are not VFs, must hardwire this bit to either 0b or 1b. VFs in an Upstream Port and Root Complex Integrated VFs are permitted to either: • hardwire this bit to 0b or • implement this bit as read / write with a default value of 0b.	RW/RO
29	***Hierarchy ID VF Configurable*** - This bit indicates that Hierarchy ID Writeable can be configured. If Hierarchy ID Writeable is implemented as read / write, this bit is 1b. Otherwise this bit is 0b.	RO
30	***Hierarchy ID Pending*** - In Downstream Ports this requests the transmittion of a Hierarchy ID Message. Setting it requests transmission of a message based on the Hierarchy Data and GUID registers in this capability. This bit is cleared when either the transmit request is satisfied or the Link enters DL_Down. Behavior is undefined if the Hierarchy Data or GUID registers in this capability are written while this bit is Set. In Downstream Ports, this bit is Read / Write defaulting to 0b. In all other Functions, this bit is RsvdZ.	RW/RsvdZ

Bit Location	Description	Attributes
31	***Hierarchy ID Valid*** - This bit indicates that the remaining fields in this capability are meaningful. In Downstream Ports, this bit is hardwired to 1b. In all other Functions, the following rules apply: • If Hierarchy ID Writeable is Set, this bit is read/write, default 0b. • If Hierarchy ID Writeable is Clear, this bit is read only, default 0b. ◦ In VFs, this bit contains the same value as the associated PF. ◦ In Functions other than VFs that are associated with an Upstream Port, this bit is Set when a Hierarchy ID Message is received, and Cleared when the Link is DL_Down. ◦ In RCiEPs other than VFs, this bit contains a system provided value. The mechanism for determining this value is outside the scope of this specification.	RW/RO

7.9.18.3 Hierarchy ID Data Register (Offset 08h)

Figure 7-275 and Table 7-222 detail allocation of fields in the Hierarchy ID Data Register.

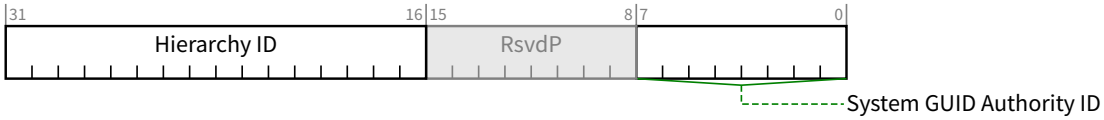

Figure 7-275 Hierarchy ID Data Register

Table 7-222 Hierarchy ID Data Register

Bit Location	Description	Attributes
7:0	***System GUID Authority ID*** - This field corresponds to the System GUID Authority ID field in the Hierarchy ID Message. See Section 6.26 for details. This field is meaningful only if Hierarchy ID Valid is 1b. If Hierarchy ID Writeable is Set, this field is read-write and contains the value programmed by software. If Hierarchy ID Writeable is Clear, this field is read only. The value is determined using the rules defined in Section 7.9.18 . This field defaults to 00h.	RO/RW
31:16	***Hierarchy ID*** - This field corresponds to the Hierarchy ID field in the Hierarchy ID Message. See Section 6.26 for details. This field is meaningful only if Hierarchy ID Valid is 1b. If Hierarchy ID Writeable is Set, this field is read-write and contains the value programmed by software. If Hierarchy ID Writeable is Clear, this field is read only. The value is determined using the rules defined in Section 7.9.18 . This field defaults to 0000h.	RO/RW

7.9.18.4 Hierarchy ID GUID 1 Register (Offset 0Ch)

Figure 7-276 and Table 7-223 detail allocation of fields in the Hierarchy ID GUID 1 Register.

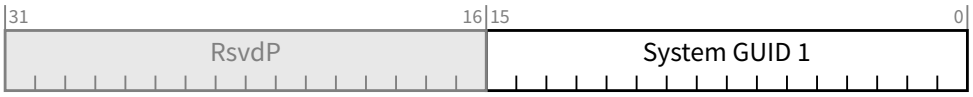

Figure 7-276 Hierarchy ID GUID 1 Register

Table 7-223 Hierarchy ID GUID 1 Register

Bit Location	Description	Attributes
15:0	***System GUID 1*** - This field corresponds to bits [143:128] of the System GUID in the Hierarchy ID Message. See Section 6.26 for details. This field is meaningful only if Hierarchy ID Valid is 1b. If Hierarchy ID Writeable is Set, this field is read-write and contains the value programmed by software. If Hierarchy ID Writeable is Clear, this field is read only. The value is determined using the rules defined in Section 7.9.18 . This field defaults to 0000h.	RO/RW

7.9.18.5 Hierarchy ID GUID 2 Register (Offset 10h)

Figure 7-277 and Table 7-224 detail allocation of fields in the Hierarchy ID GUID 2 Register.

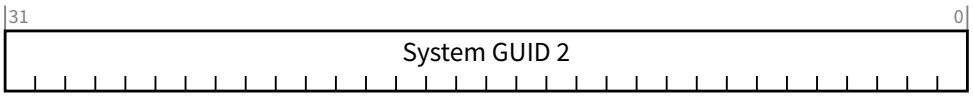

Figure 7-277 Hierarchy ID GUID 2 Register

Table 7-224 Hierarchy ID GUID 2 Register

Bit Location	Description	Attributes
31:0	***System GUID 2*** - This field corresponds to bits [127:96] of the System GUID field in the Hierarchy ID Message. See Section 6.26 for details. This field is meaningful only if Hierarchy ID Valid is 1b. If Hierarchy ID Writeable is Set, this field is read-write and contains the value programmed by software. If Hierarchy ID Writeable is Clear, this field is read only. The value is determined using the rules defined in Section 7.9.18 . This field defaults to 0000 0000h.	RO/RW

7.9.18.6 Hierarchy ID GUID 3 Register (Offset 14h)

Figure 7-278 and Table 7-225 detail allocation of fields in the Hierarchy ID GUID 3 Register.

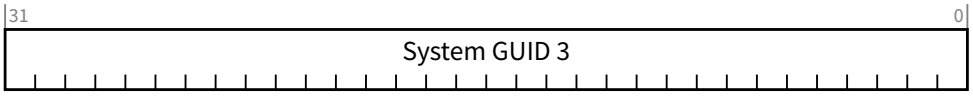

Figure 7-278 Hierarchy ID GUID 3 Register

Table 7-225 Hierarchy ID GUID 3 Register

Bit Location	Description	Attributes
31:0	***System GUID 3*** - This field corresponds to bits [95:64] of the System GUID field in the Hierarchy ID Message. See Section 6.26 for details. This field is meaningful only if Hierarchy ID Valid is 1b. If Hierarchy ID Writeable is Set, this field is read-write and contains the value programmed by software. If Hierarchy ID Writeable is Clear, this field is read only. The value is determined using the rules defined in Section 7.9.18 . This field defaults to 0000 0000h.	RO/RW

7.9.18.7 Hierarchy ID GUID 4 Register (Offset 18h)

Figure 7-279 and Table 7-226 detail allocation of fields in the Hierarchy ID GUID 4 Register.

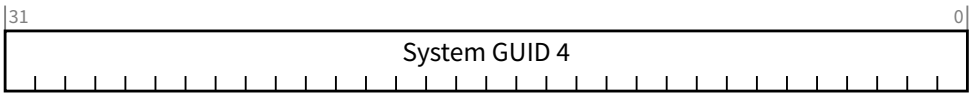

Figure 7-279 Hierarchy ID GUID 4 Register

Table 7-226 Hierarchy ID GUID 4 Register

Bit Location	Description	Attributes
31:0	***System GUID 4*** - This field corresponds to bits [63:32] of the System GUID field in the Hierarchy ID Message. See Section 6.26 for details. This field is meaningful only if Hierarchy ID Valid is 1b. If Hierarchy ID Writeable is Set, this field is read-write and contains the value programmed by software. If Hierarchy ID Writeable is Clear, this field is read only. The value is determined using the rules defined in Section 7.9.18 . This field defaults to 0000 0000h.	RO/RW

7.9.18.8 Hierarchy ID GUID 5 Register (Offset 1Ch)

Figure 7-280 and Table 7-227 detail allocation of fields in the Hierarchy ID GUID 5 Register.

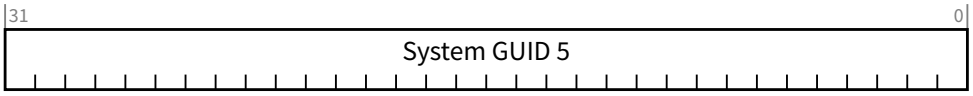

Figure 7-280 Hierarchy ID GUID 5 Register

Table 7-227 Hierarchy ID GUID 5 Register

Bit Location	Description	Attributes
31:0	***System GUID 5*** - This field corresponds to bits [31:0] of the System GUID field in the Hierarchy ID Message. See Section 6.26 for details. This field is meaningful only if Hierarchy ID Valid is 1b. If Hierarchy ID Writeable is Set, this field is read-write and contains the value programmed by software. If Hierarchy ID Writeable is Clear, this field is read only. The value is determined using the rules defined in Section 7.9.18 . This field defaults to 0000 0000h.	RO/RW

7.9.19 Vital Product Data Capability (VPD Capability)

Support of VPD is optional. All Functions are permitted to contain the capability. This includes all Functions of a Multi-Function Device associated with an Upstream Port as well as RCiEPs.

Vital Product Data (VPD) is information that uniquely identifies hardware and, potentially, software elements of a system. The VPD can provide the system with information on various Field Replaceable Units such as part number, serial number, and other detailed information. The objective from a system point of view is to make this information available to the system owner and service personnel. VPD typically resides in a storage device (for example, a serial EEPROM) associated with the Function.

Details of the VPD Data is defined in Section 6.28 .

Access to the VPD is provided using the Capabilities List in Configuration Space. The VPD Capability structure is shown in Figure 7-281 .

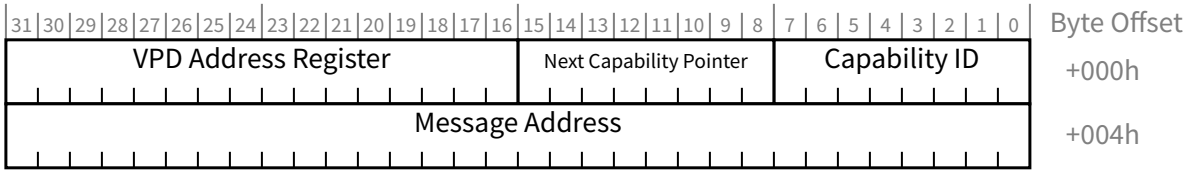

Figure 7-281 VPD Capability Structure

The following protocols are used transfer data between the VPD Data field and the VPD storage component.

- To read VPD information:
  1. Issue single write to the VPD Address Register writing the flag bit (F) to 0b and VPD Address with the address to read.
  2. The hardware device will set F to 1b when 4 bytes of data from the storage component have been transferred to VPD Data.
  3. Software can monitor F and, after it becomes 1b, read the VPD information from VPD Data.

  Behavior is undefined if either the VPD Address or VPD Data is written, prior to the flag bit becoming 1b.
- To write VPD information to the read/write portion of the VPD space:
  1. Write the data to VPD Data
  2. Then issue a single write to the VPD Address Register with F set to 1b and VPD Address set to the address where the VPD Data is to be stored.
  3. The software then monitors F and when it is set to 0b (by device hardware), the VPD Data (all 4 bytes) has been transferred from VPD Data to the storage component.

  If either the VPD Address or VPD Data is written, prior to F being becoming 0b, the results of the write operation to the storage component are unpredictable.

Behavior is undefined if a read or write of the storage component is requested and VPD Address is outside the side of the storage component.

The VPD (both the read only items and the read/write fields) is stored information and will have no direct control of any device operations.

7.9.19.1 VPD Address Register

The VPD Address Register is used to request a read or write of the VPD storage component.

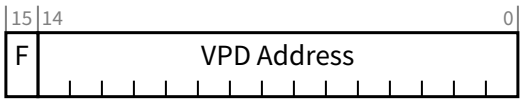

Figure 7-282 VPD Address Register

Table 7-228 VPD Address Register

Bit Location	Description	Attributes
14:0	***VPD Address*** - DWORD-aligned byte address of the VPD to be accessed. Behavior is undefined if the lowest 2 bits of this field are non-zero. The lowest two bits of the field must be either RW, or RO with a value of 00b. The remaining bits of the field must be RW. Default is implementation specific.	RW/RO (see description)
15	***F*** - The F bit is always written along with VPD Address. The value of F indicates the direction of transfer being requested (0b = read, 1b = write). When the transfer is complete, the F bit value changes to indicate completion (1b = read complete, 0b = write complete). Default is implementation specific.	RW

7.9.19.2 VPD Data Register

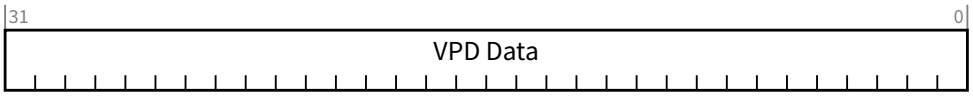

Figure 7-283 VPD Data Register

Table 7-229 VPD Data Register

Bit Location	Description	Attributes
31:0	***VPD Data*** - VPD Data can be read through this register. The least significant byte of this register (at offset 04h in this capability structure) corresponds to the byte of VPD at the address specified by VPD Address. Behavior is undefined for any read or write of this register with Byte Enables other than 1111b. Default is implementation specific.	RW

7.9.20 Native PCIe Enclosure Management Extended Capability (NPEM Extended Capability)

The Native PCIe Enclosure Management Extended (NPEM) Capability is an optional extended capability that is permitted to be implemented by Root Ports, Switch Downstream Ports, and Endpoints.

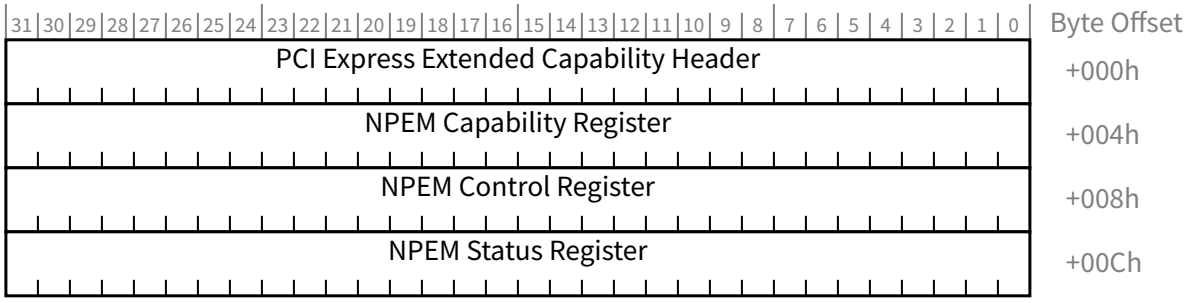

Figure 7-284 NPEM Extended Capability

7.9.20.1 NPEM Extended Capability Header (Offset 00h)

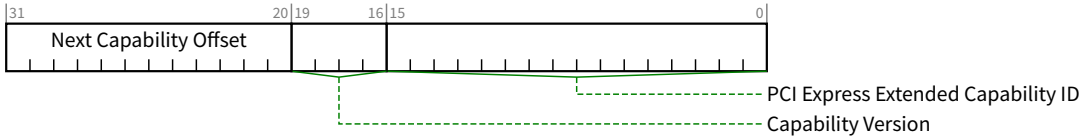

Figure 7-285 NPEM Extended Capability Header

Table 7-230 NPEM Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. PCI Express Extended Capability ID for the NPEM Extended Capability is 0029h.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of capabilities.	RO

7.9.20.2 NPEM Capability Register (Offset 04h)

The NPEM Capability Register contains an overall NPEM Capable bit and a bit map of states supported in the implementation. Implementations are required to support OK, Locate, Fail, and Rebuild states if NPEM Capable bit is Set. All other states are optional.

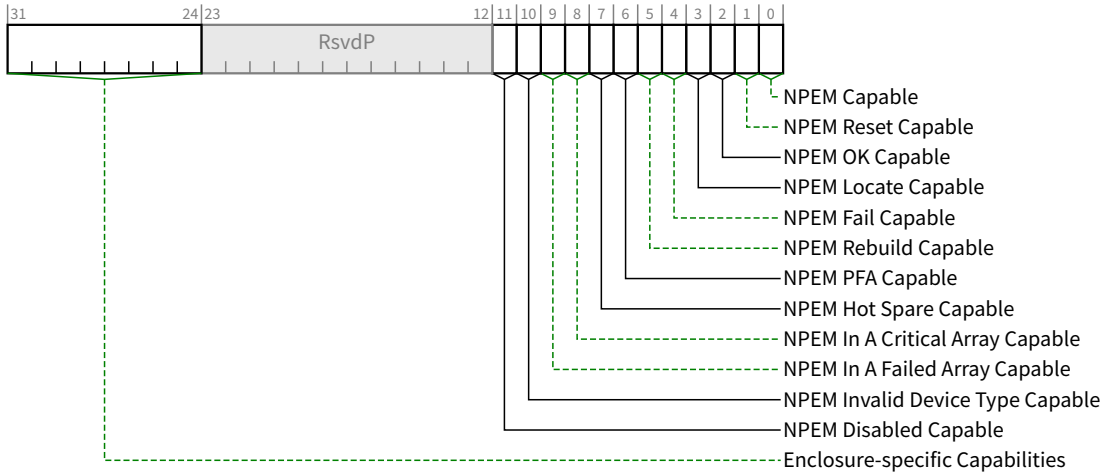

Figure 7-286 NPEM Capability Register

Table 7-231 NPEM Capability Register

Bit Location	Register Description	Attributes
0	***NPEM Capable*** - When Set, this bit indicates that the enclosure has NPEM functionality.	HwInit
1	***NPEM Reset Capable*** - A value of 1b indicates support for the optional NPEM Reset mechanism described in Section 6.29 . This capability is independently optional.	HwInit
2	***NPEM OK Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM OK state. This bit must be Set if NPEM Capable is also Set.	HwInit
3	***NPEM Locate Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM Locate state. This bit must be Set if NPEM Capable is also Set.	HwInit
4	***NPEM Fail Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM Fail state. This bit must be Set if NPEM Capable is also Set.	HwInit
5	***NPEM Rebuild Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM Rebuild state. This bit must be Set if NPEM Capable is also Set.	HwInit
6	***NPEM PFA Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM PFA state. This capability is independently optional.	HwInit
7	***NPEM Hot Spare Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM Hot Spare state. This capability is independently optional.	HwInit
8	***NPEM In A Critical Array Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM In A Critical Array state. This capability is independently optional.	HwInit
9	***NPEM In A Failed Array Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM In A Failed Array state. This capability is independently optional.	HwInit
10	***NPEM Invalid Device Type Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM_Invalid_ Device_Type state. This capability is independently optional.	HwInit

Bit Location	Register Description	Attributes
11	***NPEM Disabled Capable*** - When Set, this bit indicates that enclosure has the ability to indicate the NPEM_Disabled state. This capability is independently optional.	HwInit
31:24	***Enclosure-specific Capabilities*** - The definition of enclosure-specific bits is outside the scope of this specification.	HwInit

7.9.20.3 NPEM Control Register (Offset 08h)

The NPEM Control Register contains an overall NPEM Enable bit and a bit map of states that software controls.

Use of Enclosure-specific bits is outside the scope of this specification.

All writes to this register, including writes that do not change the register value, are NPEM commands and should eventually result in a command completion indication in the NPEM Status Register.

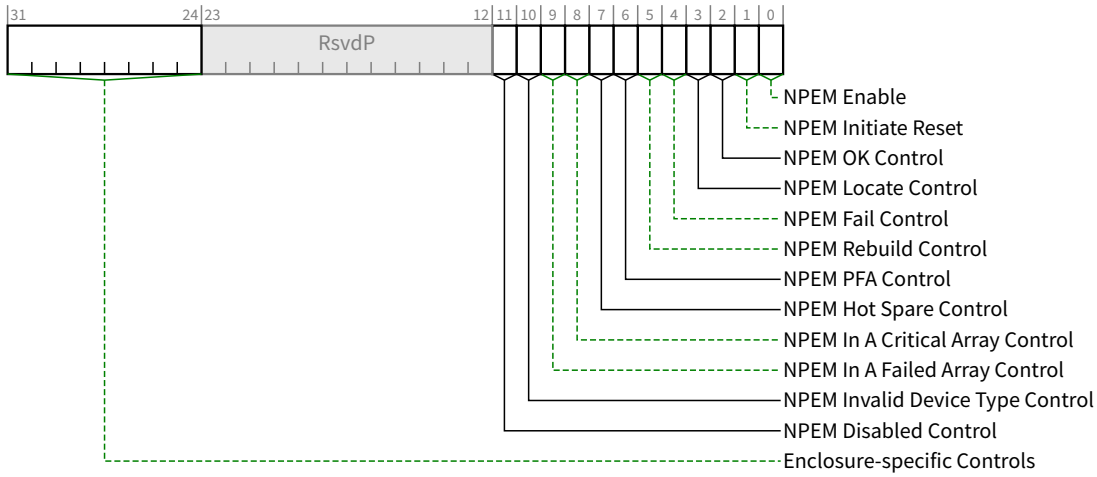

Figure 7-287 NPEM Control Register

Table 7-232 NPEM Control Register

Bit Location	Register Description	Attributes
0	***NPEM Enable*** - When Set, this bit enables the NPEM capability. When Clear, this bit disables the NPEM capability. Default value of this bit is 0b. When enabled, this capability operates as defined in this specification. When disabled, the other bits in this capability have no effect and any associated indications are outside the scope of this specification.	RW
1	***NPEM Initiate Reset*** - If NPEM Reset Capable bit is 1b, then a write of 1b to this bit initiates NPEM Reset. If NPEM Reset Capable bit is 0b, then this bit is permitted to be read-only with a value of 0b. The value read by software from this bit must always be 0b.	RW/RO
2	***NPEM OK Control*** - When Set, this bit specifies that the NPEM OK indication be turned ON. When Clear, this bit specifies that the NPEM OK indication be turned OFF.	RW/RO

Bit Location	Register Description	Attributes
	If NPEM OK Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	
3	***NPEM Locate Control*** - When Set, this bit specifies that the NPEM Locate indication be turned ON. When Clear, this bit specifies that the NPEM Locate indication be turned OFF. If NPEM Locate Capable bit in the NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
4	***NPEM Fail Control*** - When Set, this bit specifies that the NPEM Fail indication be turned ON. When Clear, this bit specifies that the NPEM Fail indication be turned OFF. If NPEM Fail Capable bit in the NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
5	***NPEM Rebuild Control*** - When Set, this bit specifies that the NPEM Rebuild indication be turned ON. When Clear, this bit specifies that the NPEM Rebuild indication be turned OFF. If NPEM Rebuild Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
6	***NPEM PFA Control*** - When Set, this bit specifies that the NPEM PFA indication be turned ON. When Clear, this bit specifies that the NPEM PFA indication be turned OFF. If NPEM PFA Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
7	***NPEM Hot Spare Control*** - When Set, this bit specifies that the NPEM Hot Spare indication be turned ON. When Clear, this bit specifies that the NPEM Hot Spare indication be turned OFF. If NPEM Hot Spare Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
8	***NPEM In A Critical Array Control*** - When Set, this bit specifies that the NPEM In A Critical Array indication be turned ON. When Clear, this bit specifies that the NPEM In A Ciritical Array indication be turned OFF. If NPEM In A Critical Array Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
9	***NPEM In A Failed Array Control*** - When Set, this bit specifies that the NPEM In A Failed Array indication be turned ON. When Clear, this bit specifies that the NPEM In A Failed Array indication be turned OFF. If NPEM In A Failed Array Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
10	***NPEM Invalid Device Type Control*** - When Set, this bit specifies that the NPEM Invaild Device Type indication be turned ON. When Clear, this bit specifies that the NPEM Invalid Device Type indication be turned OFF.	RW/RO

Bit Location	Register Description	Attributes
	If NPEM Invalid Device Type Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	
11	***NPEM Disabled Control*** - When Set, this bit specifies that the NPEM Disabled indication be turned ON. When Clear, this bit specifies that the NPEM Disabled indication be turned OFF. If NPEM Disabled Capable bit in NPEM Capability Register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b	RW/RO
31:24	***Enclosure-specific Controls*** - The definition of enclosure-specific bits is outside the scope of this specification. Enclosure-specific software is permitted to change the value of this field. Other software must preserve the existing value when writing this register. Default value of this field is 00h	RW/RO

7.9.20.4 NPEM Status Register (Offset 0Ch)

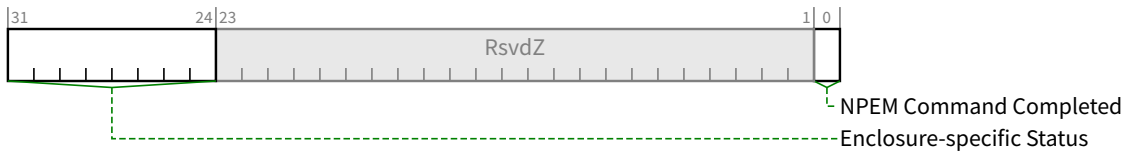

Figure 7-288 NPEM Status Register

Table 7-233 NPEM Status Register

Bit Location	Register Description	Attributes
0	***NPEM Command Completed*** - This bit is Set when an NPEM command has completed, and the NPEM controller is ready to accept a subsequent command. This bit is permitted to be hardwired to 1b if the enclosure is able to accept writes that update any portion of the NPEM Control register without any delay between successive writes. Default value of this bit is 0b. Software must wait for an NPEM command to complete before issuing the next NPEM command. However, if this bit is not set within 1 second limit on command execution, software is permitted to repeat the NPEM command or issue the next NPEM command. If software issues a write before the Port has completed processing of the previous command and before the 1 second time limit has expired, the Port is permitted to either accept or discard the write. Such a write is considered a programming error, and could result in a discrepancy between the NPEM Control Register and the enclosure element state. To recover from such a programming error and return the enclosure to a consistent state, software must issue a write to the NPEM Control Register which conforms to the NPEM command completion rules.	RW1C / RO
31:24	***Enclosure-specific Status*** - The definition of enclosure specific bits is outside the scope of this specification. Enclosure specific software is permitted to write non-zero values to this field. Other software must write 00h to this field.	RsvdZ/RO/RW1C

Bit Location	Register Description	Attributes
	The default value of this field is enclosure-specific. This field is permitted to be hardwired to 00h.	

7.9.21 Alternate Protocol Extended Capability

The Alternate Protocol Extended Capability structure is optional. It is only permitted in:

- A Function associated with a Downstream Port.
- Function 0 (and only Function 0) of a Device associated with an Upstream Port.

Figure 7-289 details allocation of register fields in the Alternate Protocol Extended Capability structure.

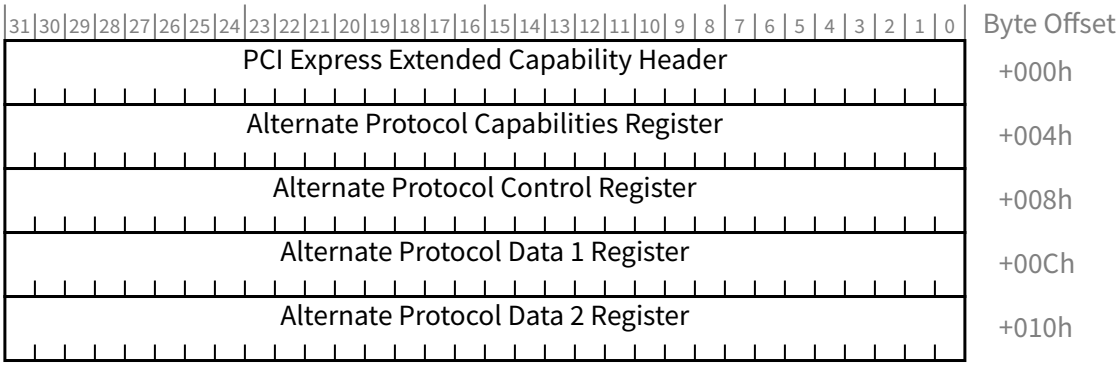

Figure 7-289 Alternate Protocol Extended Capability

7.9.21.1 Alternate Protocol Extended Capability Header (Offset 00h)

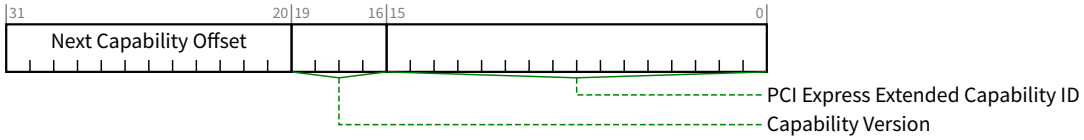

Figure 7-290 Alternate Protocol Extended Capability Header

Table 7-234 Alternate Protocol Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Alternate Protocol Capability is 002Bh.	RO

Bit Location	Register Description	Attributes
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.21.2 Alternate Protocol Capabilities Register (Offset 04h)

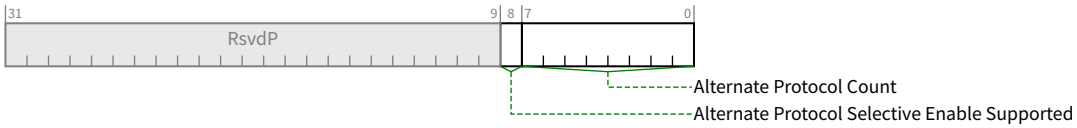

Figure 7-291 Alternate Protocol Capabilities Register

Table 7-235 Alternate Protocol Capabilities Register

Bit Location	Register Description	Attributes
7:0	***Alternate Protocol Count*** - Indicates the number of Alternate Protocols supported by one or more Lanes of this Link. Since support for PCI Express is mandatory, the value of this field must be greater than or equal to 1.	HwInit
8	***Alternate Protocol Selective Enable Supported*** - If Set, the Alternate Protocol Selective Enable Mask Register is present. If Clear, the Alternate Protocol Selective Enable Mask Register is not present and Alternate Protocol Negotiation is controlled soley by the Alternate Protocol Negotiation Global Enable bit. In Upstream Ports, this bit is hardwired to 0b. In Downstream Ports, this bit is HwInit with an implementation specific default value.	RO/HwInit

7.9.21.3 Alternate Protocol Control Register (Offset 08h)

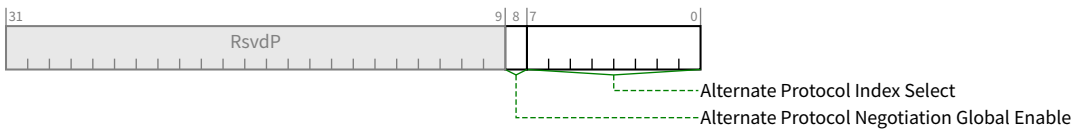

Figure 7-292 Alternate Protocol Control Register

Table 7-236 Alternate Protocol Control Register

Bit Location	Register Description	Attributes
7:0	***Alternate Protocol Index Select*** - This field determines which Lane and which Alternate Protocol of that Lane is visible in Alternate Protocol Data 1 Register and Alternate Protocol Data 2 Register. The default value of this field is 00h. Unused bits in this field are permitted to be hardwired to 0b. If Alternate Protocol Count is 01h, this field is permitted to be hardwired to 00h. Behavior is undefined if this field is greater than Alternate Protocol Count. Specific Alternate Protocol Index Select values are permitted to be disabled without renumbering other protocol index values. Disabled entries return an Alternate Protocol Vendor ID of FFFFh.	RW
8	***Alternate Protocol Negotiation Global Enable*** - When this bit is Set, Alternate Protocol Negotiation is enabled for this Link. When this bit is Clear, Alternate Protocol Negotiation is disabled for this Link. Default is 0b.	RW

7.9.21.4 Alternate Protocol Data 1 Register (Offset 0Ch)

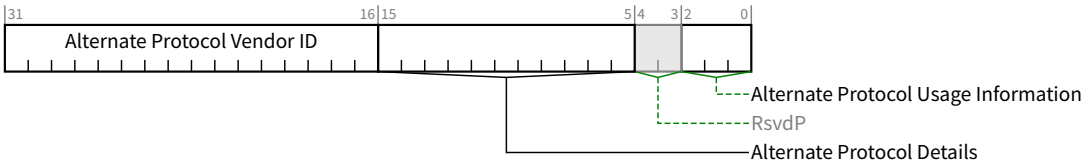

Figure 7-293 Alternate Protocol Data 1 Register

Table 7-237 Alternate Protocol Data 1 Register

Bit Location	Register Description	Attributes
2:0	***Alternate Protocol Usage Information*** - This field contains the Modified TS Usage associated alternate protocol associated with the Alternate Protocol Index Select value. If Alternate Protocol Vendor ID is FFFFh, the value of this field is undefined.	RO
15:5	***Alternate Protocol Details*** - This field contains the Alternate Protocol Details associated alternate protocol associated with the Alternate Protocol Index Select value. If Alternate Protocol Vendor ID is FFFFh, the value of this field is undefined.	RO
31:16	***Alternate Protocol Vendor ID*** - This field contains the Vendor ID associated alternate protocol associated with the Alternate Protocol Index Select value. Bits 7:0 of this field contain bits 7:0 of Vendor ID (Symbol 10). Bits 15:8 of this field contain bits 15:8 of Vendor ID (Symbol 11). If Alternate Protocol Index Select is greater than or equal to Alternate Protocol Count, this field contains FFFFh. If Alternate Protocol Index Select is associated with a disabled alternate protocol, this field contains FFFFh.	RO

7.9.21.5 Alternate Protocol Data 2 Register (Offset 10h)

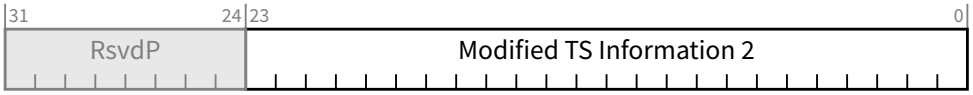

Figure 7-294 Alternate Protocol Data 2 Register

Table 7-238 Alternate Protocol Data 2 Register

Bit Location	Register Description	Attributes
23:0	***Modified TS Information 2*** - This field contains the value for symbols 12 throught 14 for the alternate protocol associated with the Alternate Protocol Index Select value. If Alternate Protocol Vendor ID is FFFFh, the value of this field is undefined. Bits 7:0 contain the value of Symbol 12. Bits 16:8 contain the value of Symbol 13. Bits 23:16 contain the value of Symbol 14.	RO

7.9.21.6 Alternate Protocol Selective Enable Mask Register (Offset 14h)

This register is present if Alternate Protocol Selective Enable Supported is Set.

This register consists of a bit mask of size Alternate Protocol Count bits. Each bit corresponds to a valid value of Alternate Protocol Index Select. This register is an integral number of DWORDs in size.

When Alternate Protocol Negotiation Global Enable is Set, a particular bit in this register is Set, and the corresponding Alternate Protocol is not disabled (see Alternate Protocol Index Select), the next Alternate Protocol negotiation is permitted to consider using that Alternate Protocol. When a particular bit in this register is Clear, the next Alternate Protocol negotiation is not permitted to consider using the corresponding Alternate Protocol.

Changes to this field will affect the next Alternate Protocol negotiation and have no effect on current operation of the Link (regardless of current protocol).

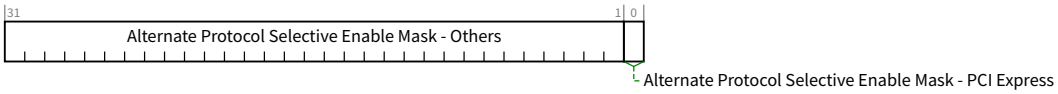

Figure 7-295 Alternate Protocol Selective Enable Mask Register

Table 7-239 Alternate Protocol Selective Enable Mask Register

Bit Location	Register Description	Attributes
0	***Alternate Protocol Selective Enable Mask - PCI Express*** - The PCI Express Protocol is always index 00h. The default value of this bit is 1b (i.e., PCI Express is always enabled by default).	RWS

Bit Location	Register Description	Attributes
	This bit is permitted to be hardwired to 1b.	
31:1	***Alternate Protocol Selective Enable Mask - Others*** - Other bits in this register represent protocols other than PCI Express. The default values of these "other" bits is implementation specific. The width of this field is shown here as 32 bits. The actual width derpends on Alternate Protocol Count. Bits in this field corresponding to disabled Alternate Protocol Index values are permitted to be hardwired to 0b. Bits in this field corresponding to Alternate Protocol Index Select values above Alternate Protocol Count are permitted to be hardwired to 0b.	RWS

7.9.22 Conventional PCI Advanced Features Capability (AF)

This capability is optional. It is permitted only in Conventional PCI Functions that are integrated into a Root Complex. A Function may contain at most one instance of this capability.

Figure 7-296 shows the layout of this capability.

Note: Due to document production limitations, this figure shows an 8 byte capability while the actual capability is only 6 bytes long. Bytes 6 and 7 in the figure are not part of the capability.

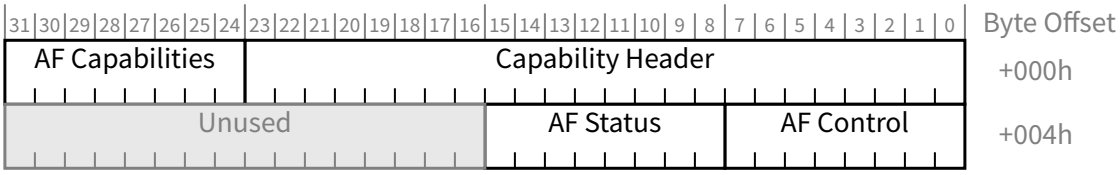

Figure 7-296 Conventional PCI Advanced Features Capability (AF)

7.9.22.1 Advanced Features Capability Header (Offset 00h)

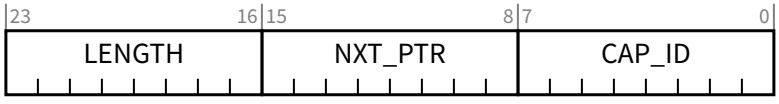

Figure 7-297 Advanced Features Capability Header

Table 7-240 Advanced Features Capability Header

Bit Location	Register Description	Attributes
7:0	***CAP_ID*** - The value of 13h in this field identifies the Function as being AF capable.	RO

Bit Location	Register Description	Attributes
15:8	***NXT_PTR*** - Pointer to the next item in the capabilities list. Must be 00h for the final item in the list.	RO
23:16	***LENGTH*** - AF Structure Length (Bytes). Shall return a value of 06h.	RO

7.9.22.2 AF Capabilities Register (Offset 03h)

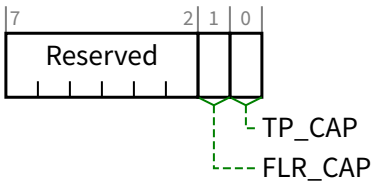

Figure 7-298 AF Capabilities Register

Table 7-241 AF Capabilities Register

Bit Location	Register Description	Attributes
0	***TP_CAP*** - Set to indicate support for the Transactions Pending (TP) bit. TP_CAP must be Set if FLR_CAP is Set.	HwInit
1	***FLR_CAP*** - Set to indicate support for Function Level Reset (INITIATE_FLR).	HwInit
7:2	Reserved - Shall be implemented as read only returning a value of 000 0000b.	RO

7.9.22.3 Conventional PCI Advanced Features Control Register (Offset 04h)

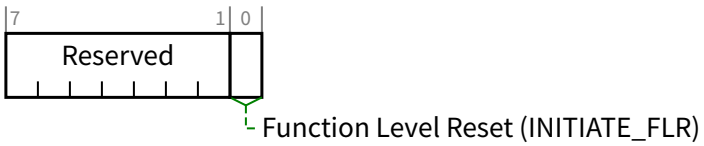

Figure 7-299 Conventional PCI Advanced Features Control Register

Table 7-242 Conventional PCI Advanced Features Control Register

Bit Location	Register Description	Attributes
0	***Function Level Reset (INITIATE_FLR)*** - A write of 1b initiates a Function Level Reset (FLR). Registers and state information that do not apply to Conventional PCI are exempt from the FLR requirements in this specification (see Section 6.6.2). The value read by software from this bit shall always be 0b.	RW

Bit Location	Register Description	Attributes
7:1	Reserved - Shall be implemented as read only returning a value of 000 0000b.	RO

7.9.22.4 AF Status Register (Offset 05h)

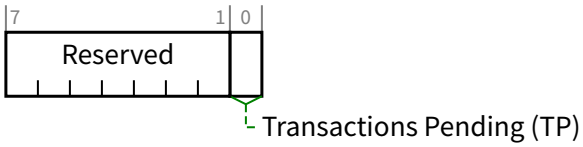

Figure 7-300 AF Status Register

Table 7-243 AF Status Register

Bit Location	Register Description	Attributes
0	***Transactions Pending (TP)*** - A value of 1b indicates that the Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. A value 0b indicates that all non-posted transactions have been completed.	RO
7:1	Reserved - Shall be implemented as read only returning a value of 000 0000b.	RO

7.9.23 SFI Extended Capability

The SFI (System Firmware Intermediary) Extended Capability is an optional capability that provides system firmware with enhanced control over primarily hot-plug mechanisms, and enables system firmware to operate as an intermediary between certain events and the operating system (see Section 6.7.4). This capability may be implemented by a Root Port or a Switch Downstream Port. It is not applicable to any other Device/Port type.

If a Downstream Port implements the SFI Extended Capability, that Port must support ERR_COR Subclass capability, and indicate so by Setting the ERR_COR Subclass Capable bit in the Device Capabilities Register. See see Section 7.5.3.3 .

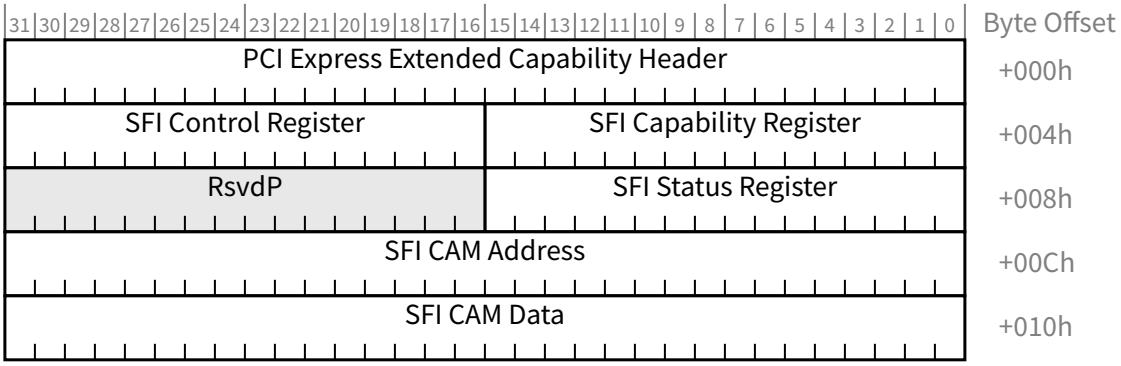

Figure 7-301 SFI Extended Capability

7.9.23.1 SFI Extended Capability Header (Offset 00h)

Figure 7-302 and Table 7-244 detail allocation of fields in the Extended Capability header.

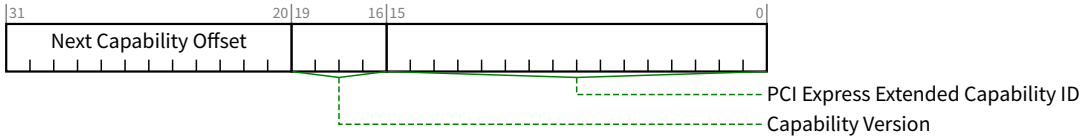

Figure 7-302 SFI Extended Capability Header

Table 7-244 SFI Extended Capability Header

Bit Location	Register Description	Attributes
15:0	***PCI Express Extended Capability ID*** - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the SFI Extended Capability is 002Ch.	RO
19:16	***Capability Version*** - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	***Next Capability Offset*** - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	RO

7.9.23.2 SFI Capability Register (Offset 04h)

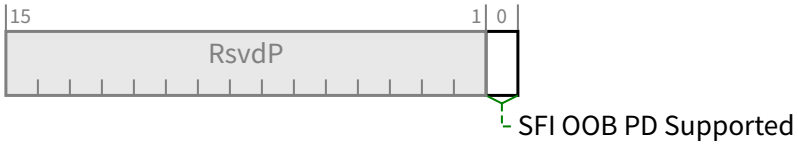

Figure 7-303 SFI Capability Register

Table 7-245 SFI Capability Register

Bit Location	Register Description	Attributes
0	***SFI OOB PD Supported*** - When Set, this bit indicates that this slot supports reporting the out-of-band presence detect state. If this Downstream Port has no implemented slot (as indicated by the Slot Implemented bit in the PCI Express Capabilities Register), then the value of this bit must be 0b.	HwInit

7.9.23.3 SFI Control Register (Offset 06h)

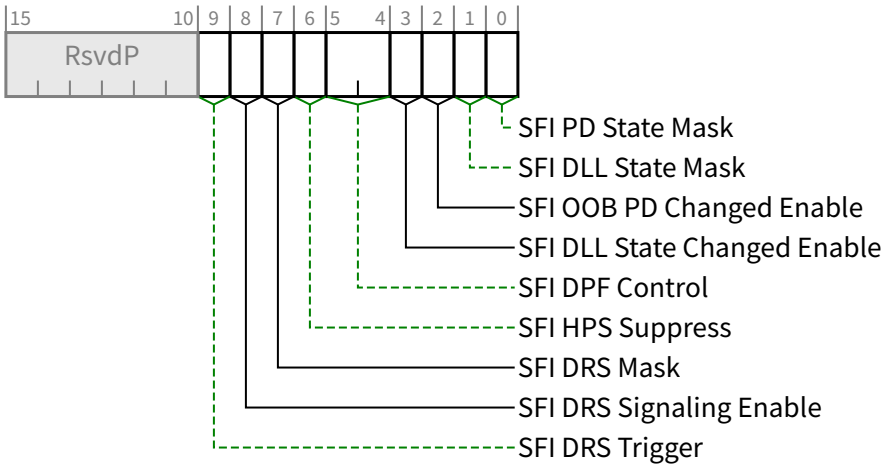

Figure 7-304 SFI Control Register

Table 7-246 SFI Control Register

Bit Location	Register Description	Attributes
0	***SFI PD State Mask*** - When Set, this bit masks the Presence Detect State bit in the Slot Status Register, making its value 0b, regardless of the actual presence detect state. Otherwise, its value indicates the actual state.	RW

Bit Location	Register Description	Attributes
	If the value of the Presence Detect State bit changes when the SFI PD State Mask bit value changes, this must cause a Presence Detect Changed event (see Section 6.7.3). Default value of this bit is 0b.	
1	***SFI DLL State Mask*** - When Set, this bit masks the Data Link Layer Link Active bit in the Link Status Register, making its value 0b, regardless of the actual Data Link Layer state. Otherwise, its value indicates the actual state. If the value of the Data Link Layer Link Active State bit changes when the SFI DLL State Mask bit value changes, this must cause a Data Link Layer State Changed event (see Section 6.7.3). Default value of this bit is 0b.	RW
2	***SFI OOB PD Changed Enable*** - When Set, this bit enables sending an ERR_COR Message for the SFI OOB PD Changed event. See Section 6.7.4.1 for other necessary conditions. This bit must be RW if the SFI OOB PD Supported bit is Set; otherwise, it is permitted to be hardwired to 0b. If the SFI OOB PD Supported bit is Clear and software Sets this bit, the behavior is undefined. Default value of this bit is 0b.	RW/RO
3	***SFI DLL State Changed Enable*** - When Set, this bit enables sending an ERR_COR Message for the SFI DLL State Changed event. See Section 6.7.4.1 for other necessary conditions. Default value of this bit is 0b.	RW
5:4	***SFI DPF Control*** - This field controls the level of Downstream Port Filtering (DPF) enabled on the Downstream Port, governing which Request TLPs targeting Downstream Components get filtered; that is, handled as if the Link is in DL_Down. See Section 6.7.4.2 . Defined encodings are: **00b** Disabled **01b** Filter all Request TLPs **10b** Filter only Configuration Request TLPs **11b** Reserved Default value of this field is 00b.	RW
6	***SFI HPS Suppress*** - When Set, this bit forces the Hot-Plug Surprise (HPS) bit in the Slot Capabilities Register to be Clear and disables associated Hot-Plug Surprise functionality. See Section 6.7.4.4 . Default value of this bit is 0b.	RW
7	***SFI DRS Mask*** - When Set, this bit masks the DRS Message Received bit in the Link Status 2 Register, making its value 0b, regardless of the actual DRS Message Received state. Otherwise, its value indicates the actual state. If the value of the DRS Message Received bit changes from Clear to Set when the SFI DRS Mask bit is Cleared, this must trigger any notification enabled by the DRS Signaling Control field in the Link Control Register (see Section 7.5.3.7). Default value of this bit is 0b.	RW
8	***SFI DRS Signaling Enable*** - When Set, this bit enables sending an ERR_COR Message for the SFI DRS Received event. See Section 6.7.4.1 for other necessary conditions. Default value of this bit is 0b.	RW
9	***SFI DRS Trigger*** - If the SFI DRS Mask bit is Clear, when software writes a 1b to this bit, the Downstream Port must behave as if a DRS Message was received. Otherwise, software writing a 1b to this bit has no effect.	RW

Bit Location	Register Description	Attributes
	It is permitted to write 1b to this bit while simultaneously writing updated values to other fields in this register, notably the SFI DRS Mask bit. For this case, the SFI DRS Trigger semantics are based on the updated value of the SFI DRS Mask bit. This bit always returns 0b when read.	

7.9.23.4 SFI Status Register (Offset 08h)

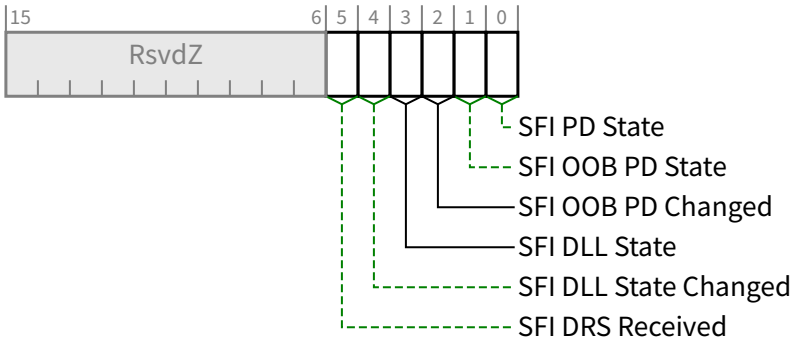

Figure 7-305 SFI Status Register

Table 7-247 SFI Status Register

Bit Location	Register Description	Attributes
0	***SFI PD State*** - This bit always indicates the actual presence detect state associated with the Presence Detect State bit in the Slot Status Register, even when the value of that bit is being masked by the SFI PD State Mask bit.	RO
1	***SFI OOB PD State*** - This bit indicates the out-of-band presence detect state, independent of the in-band presence detect state. This bit must be implemented if the SFI OOB PD Supported bit is Set; otherwise, it is permitted to be hardwired to 0b.	RO
2	***SFI OOB PD Changed*** - This bit is Set when the value reported in the SFI OOB PD State bit is changed.	RW1C
3	***SFI DLL State*** - This bit always indicates the actual link state associated with the Data Link Layer Link Active bit in the Link Status Register, even when the value of that bit is being masked by the SFI DLL State Mask bit.	RO
4	***SFI DLL State Changed*** - This bit is Set when the value reported in the SFI DLL State bit is changed.	RW1C
5	***SFI DRS Received*** - This bit always indicates the actual state associated with the DRS Message Received bit in the Link Status 2 Register, even when the value of that bit is being masked by the SFI PD State Mask bit. Clearing the SFI DRS Received bit (by writing a 1b to it) must also cause the actual state associated with the DRS Message Received bit to be Cleared.	RW1C

7.9.23.5 SFI CAM Address Register (Offset 0Ch)

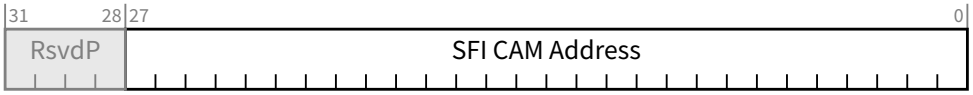

Figure 7-306 SFI CAM Address Register

Table 7-248 SFI CAM Address Register

Bit Location	Register Description	Attributes
27:0	***SFI CAM Address*** - This field specifies the target Bus, Device, and Function Numbers, along with the Extended Register Number and Register Number, in the format specified by Table 7-1 .	RW

7.9.23.6 SFI CAM Data Register (Offset 10h)

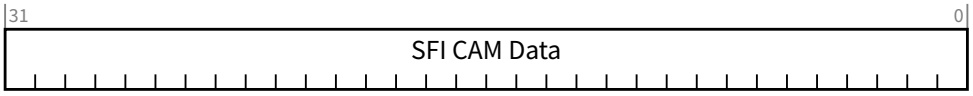

Figure 7-307 SFI CAM Data Register

Table 7-249 SFI CAM Data Register

Bit Location	Register Description	Attributes
31:0	***SFI CAM Data*** - When this field is read, the SFI CAM generates and transmits a Configuration Read Request on the Link below this Port. When this field is written, the SFI CAM generates and transmits a Configuration Write Request on the Link below this Port. In both cases, the target of the Configuration Request is determined by the value of the SFI CAM Address Register. See Section 6.7.4.3 .	RW

7.9.24 Subsystem ID and Sybsystem Vendor ID Capability

The Subsystem ID and Sybsystem Vendor ID Capability is an optional capability used to uniquely identify the add-in card or subsystem where the PCI device resides. It provieds a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI bridge on them (and, therefore, the same Vendor ID and Device ID). The format of the capability is shown in Figure 7-308 . The fields are described in Table 7-250 .

This capability is only permitted in Type 1 Configuration Space Headers.

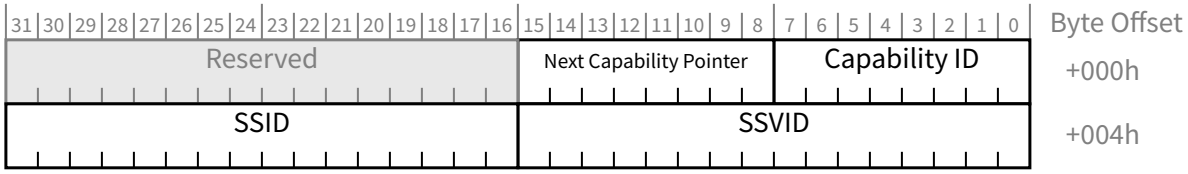

Figure 7-308 Subsystem ID and Sybsystem Vendor ID Capability

Table 7-250 Subsystem ID and Sybsystem Vendor ID Capability

Bit Location	Register Description	Attributes
DWORD 0 Bits 7:0	***Capability ID*** - Indicates the PCI Express Capability structure. This field must return a Capability ID of 0Dh indicating that this is a Subsystem ID and Sybsystem Vendor ID Capability structure.	RO
DWORD 0 Bits 15:8	***Next Capability Pointer*** - This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities.	RO
DWORD 1 Bits 15:0	***SSVID*** - The SSVID identifies the manufacturer of the add-in card or subsystem. The SSVID is assigned by PCI-SIG to insure uniqueness (the Vendor ID is used as the SSVID also). This field is read-only.	HwInit
DWORD 1 Bits 31:16	***SSID*** - The SSID identifies the particular add-in card or subsystem and is assigned by the vendor. This field is read-only.	HwInit