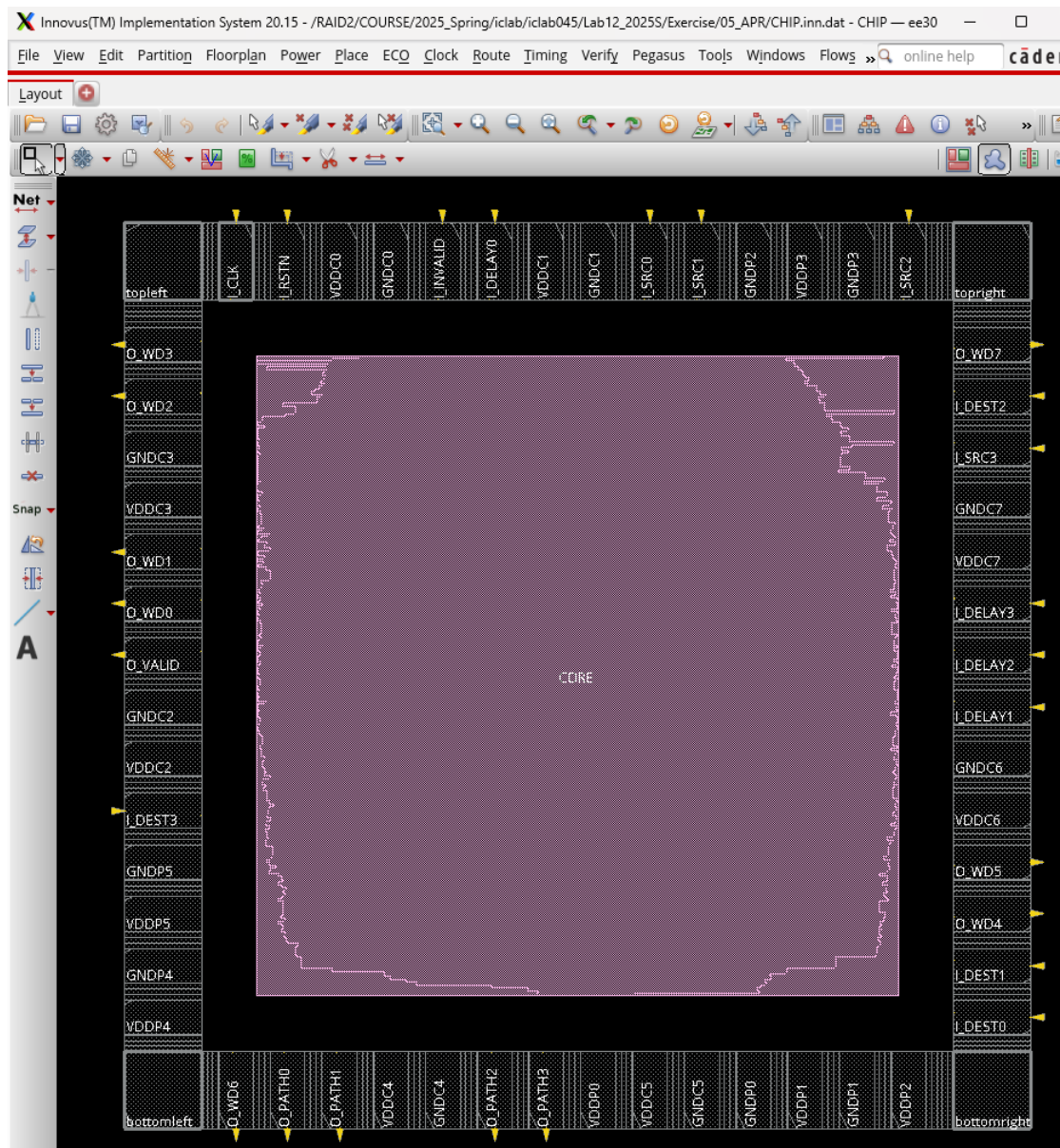
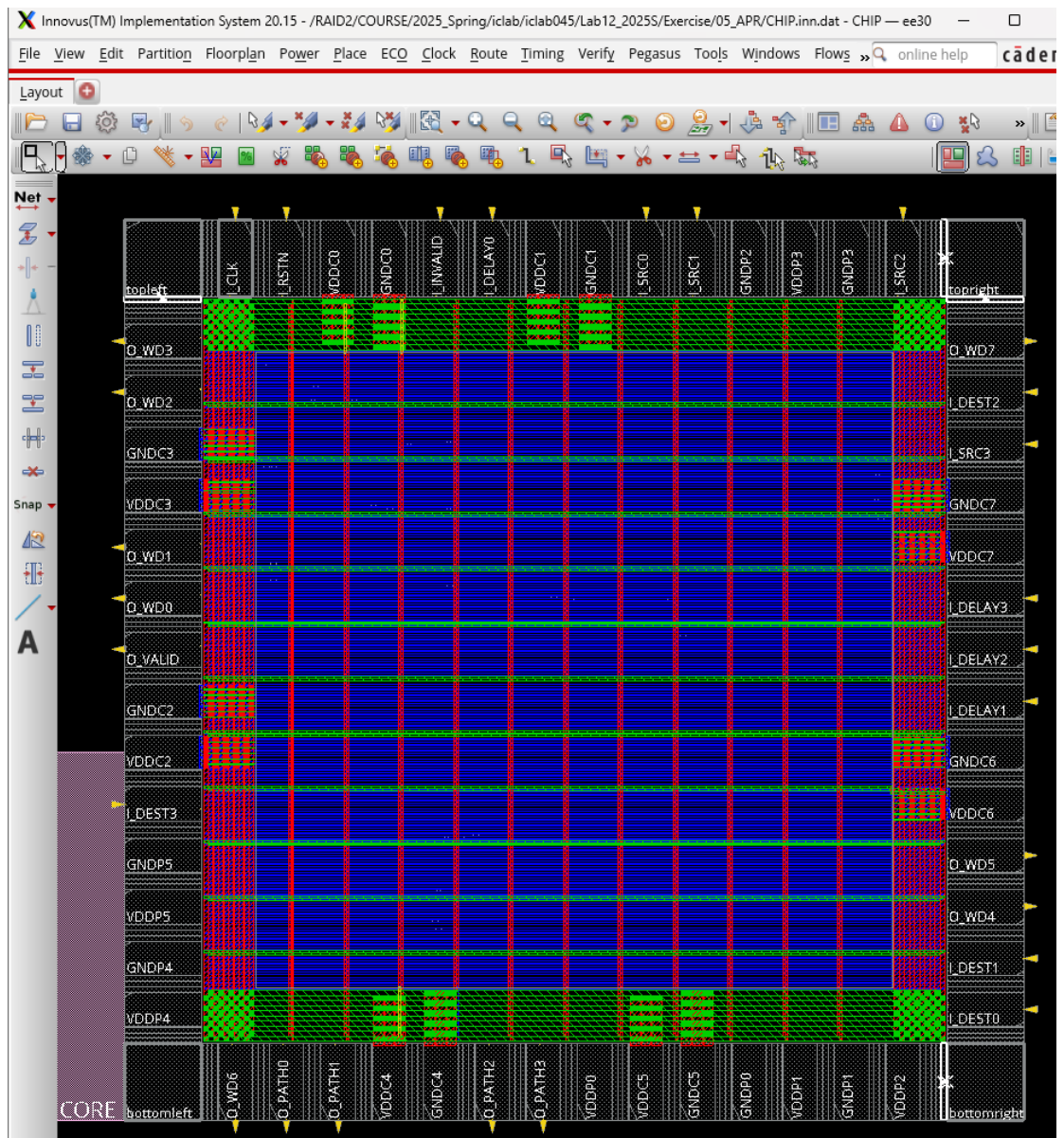
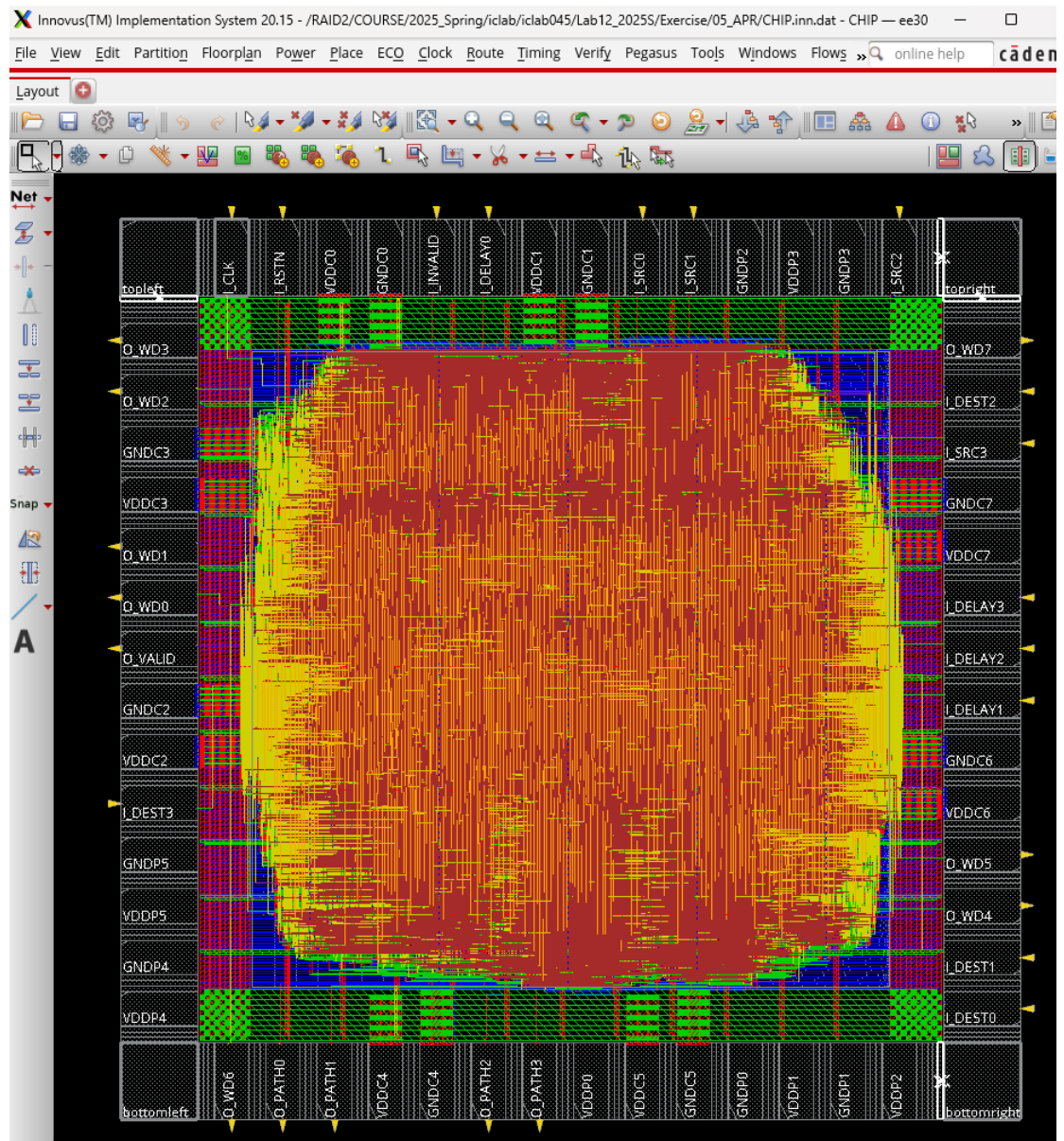


Report

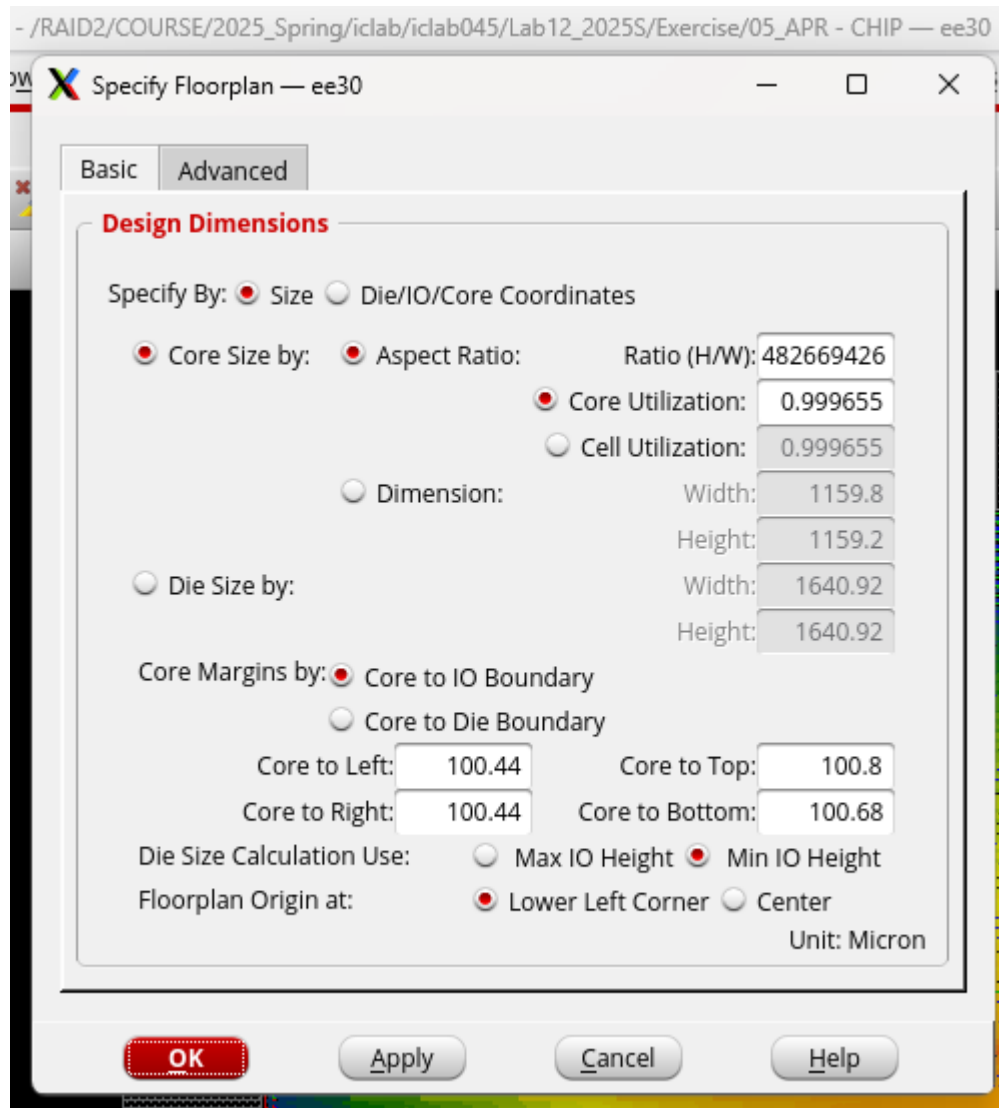
1. Chip Layout View :





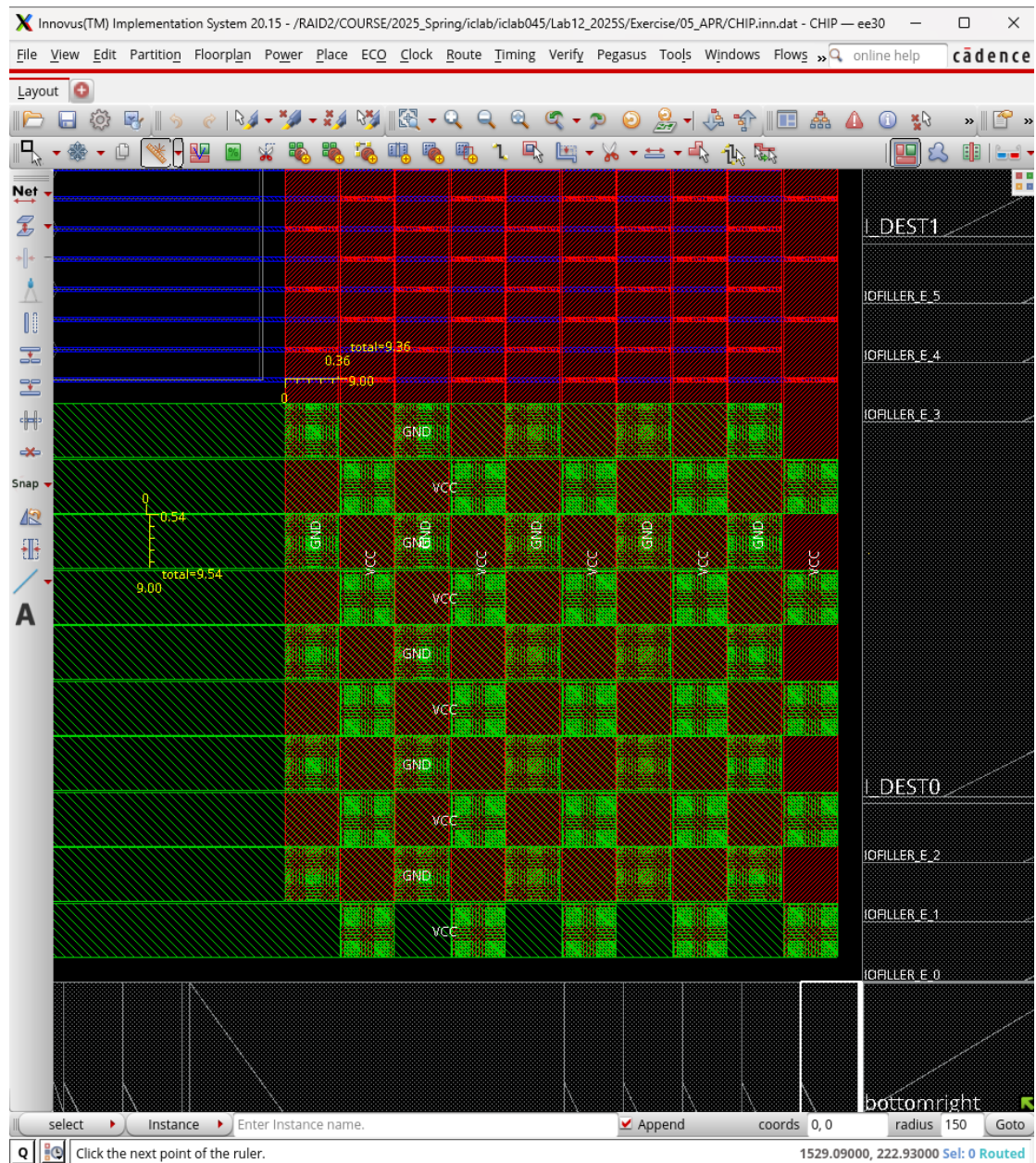


2. Core to IO boundary :



3. Core Ring :





4. Post-Route setup time analysis :

timeDesign Summary

Setup views included:
av_func_mode_max

Setup mode	all	reg2reg	default
WNS (ns):	0.117	0.192	0.117
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	1415	688	727

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 41.972%
(125.615% with Fillers)
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 3.05 sec
Total Real time: 4.0 sec

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5. Post-Route hold time analysis :

timeDesign Summary

Hold views included:
av_func_mode_min

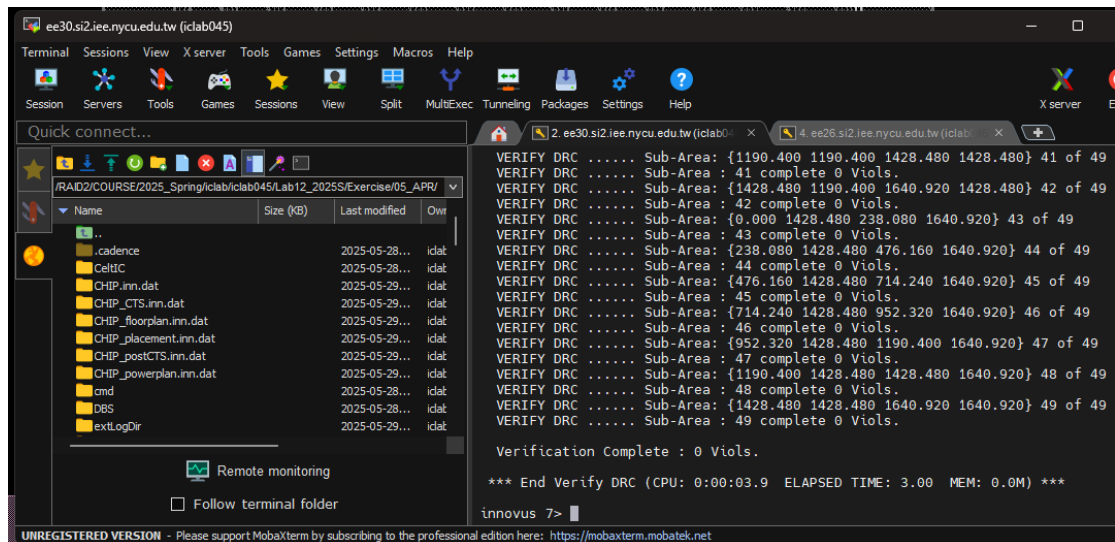
Hold mode	all	reg2reg	default
WNS (ns):	0.260	0.260	5.063
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	1415	688	727

Density: 41.972%
(125.615% with Fillers)

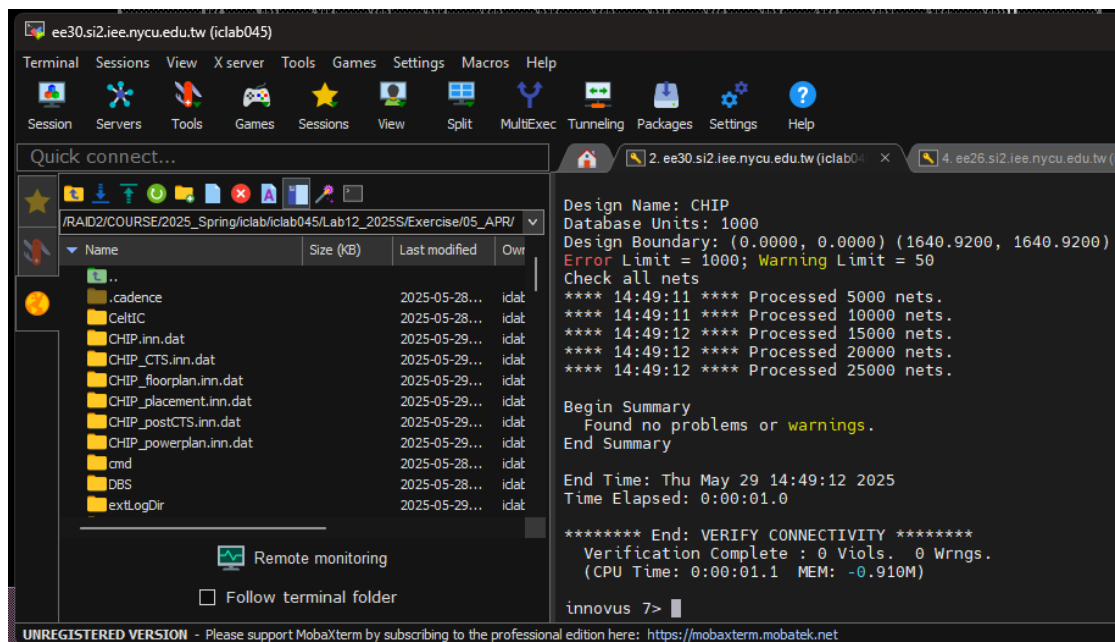
Reported timing to dir timingReports
Total CPU time: 12.72 sec
Total Real time: 14.0 sec
Total Memory Usage: 4101.0 Mbytes
Reset AAE Options
*** timeDesign #7 [finish] : cpu/real = 0:00:12.7/0:00:13.1 (1.0), tot
cpu/real = 0:20:36.6/0:39:16.7 (0.5), mem = 4101.0M
innovus 7>

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6. DRC result :



7. LVS result :



8. Post Layout simulation result :

6.si2.iee.nycu.edu.tw (iclab045)

al Sessions View X server Tools Games Settings Macros Help

Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

k connect...

RAID2/COURSE/2025_Spring/iclab/iclab045/Lab12_2025S/Exercise/05_APR/

Name	Size (KB)	Last modified	Owner
..			
.cadence		2025-05-28...	iclab045
Celtic		2025-05-28...	iclab045
cmd		2025-05-28...	iclab045
DBS		2025-05-28...	iclab045
layermap		2025-05-28...	iclab045
LEF		2025-05-28...	iclab045
LIB		2025-05-28...	iclab045
log		2025-05-28...	iclab045
power_log		2025-05-28...	iclab045
RC		2025-05-28...	iclab045
summaryReport		2025-05-28...	iclab045
timingReports		2025-05-28...	iclab045
00_combine	1	2025-05-28...	iclab045
01_setenv	1	2025-05-28...	iclab045
09_clean_up	1	2025-05-28...	iclab045
CHIP.io	1	2025-05-28...	iclab045
CHIP.sdc	8	2025-05-28...	iclab045
CHIP.cts.sdc	1	2025-05-28...	iclab045
CHIP_SHELL.v	2	2025-05-28...	iclab045
innovus.cmd	2	2025-05-28...	iclab045
innovus.log	3	2025-05-28...	iclab045
innovus.logv	6	2025-05-28...	iclab045
makefile	1	2025-05-28...	iclab045
pegasus_ui_gui.log	0	2025-05-28...	iclab045
STA_SYN.v	2 239	2025-05-28...	iclab045

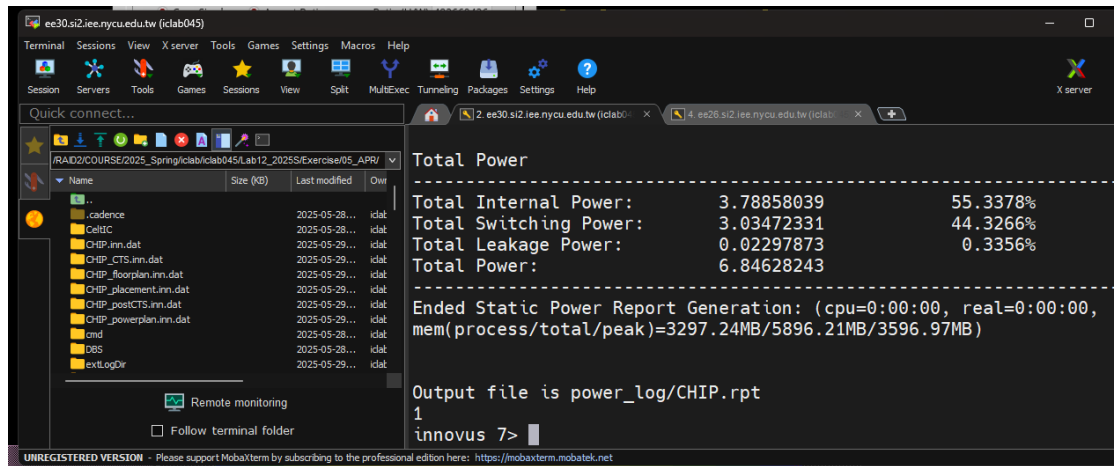
No. 991 PASS
No. 992 PASS
No. 993 PASS
No. 994 PASS
No. 995 PASS
No. 996 PASS
No. 997 PASS
No. 998 PASS
No. 999 PASS

H A S S

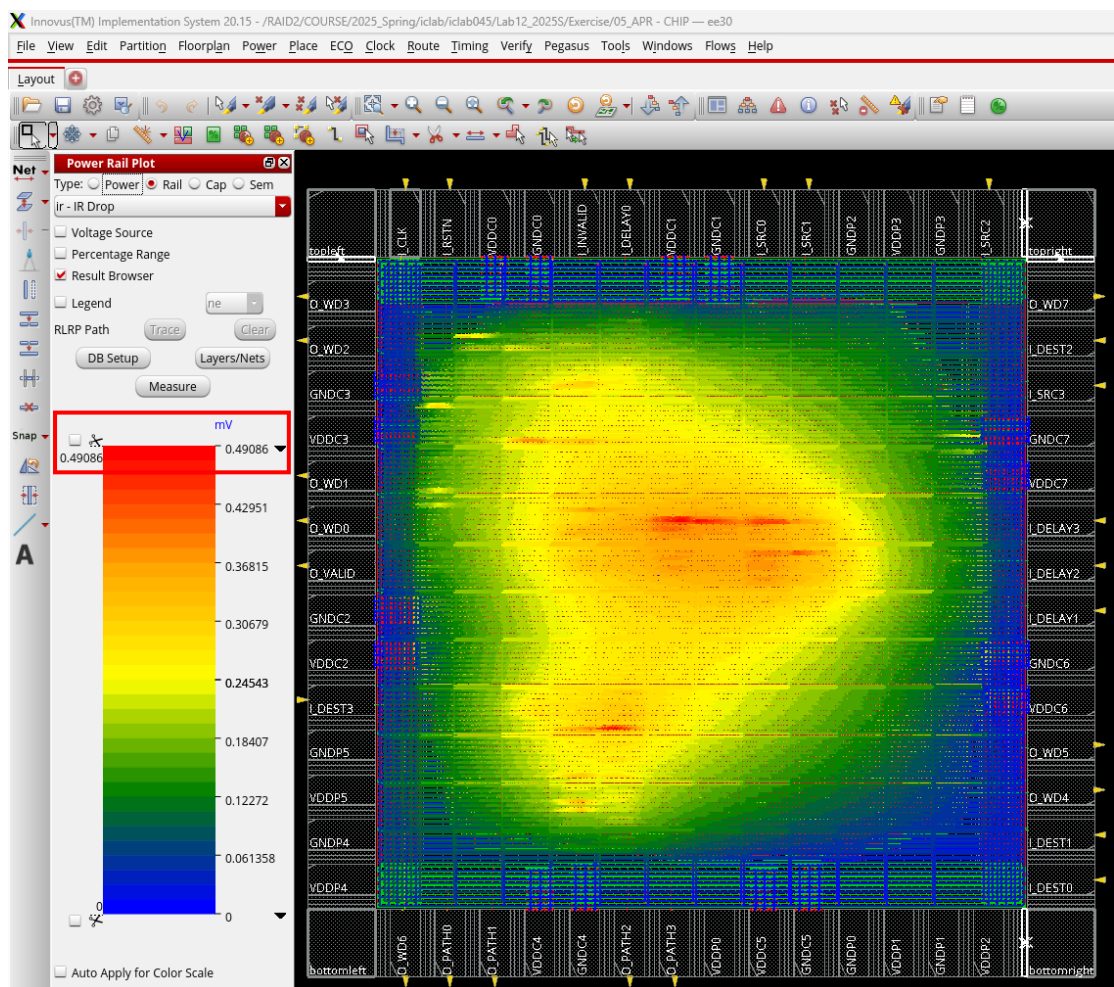
Congratulations!
execution cycles = 50000
clock period = 11.000000ns

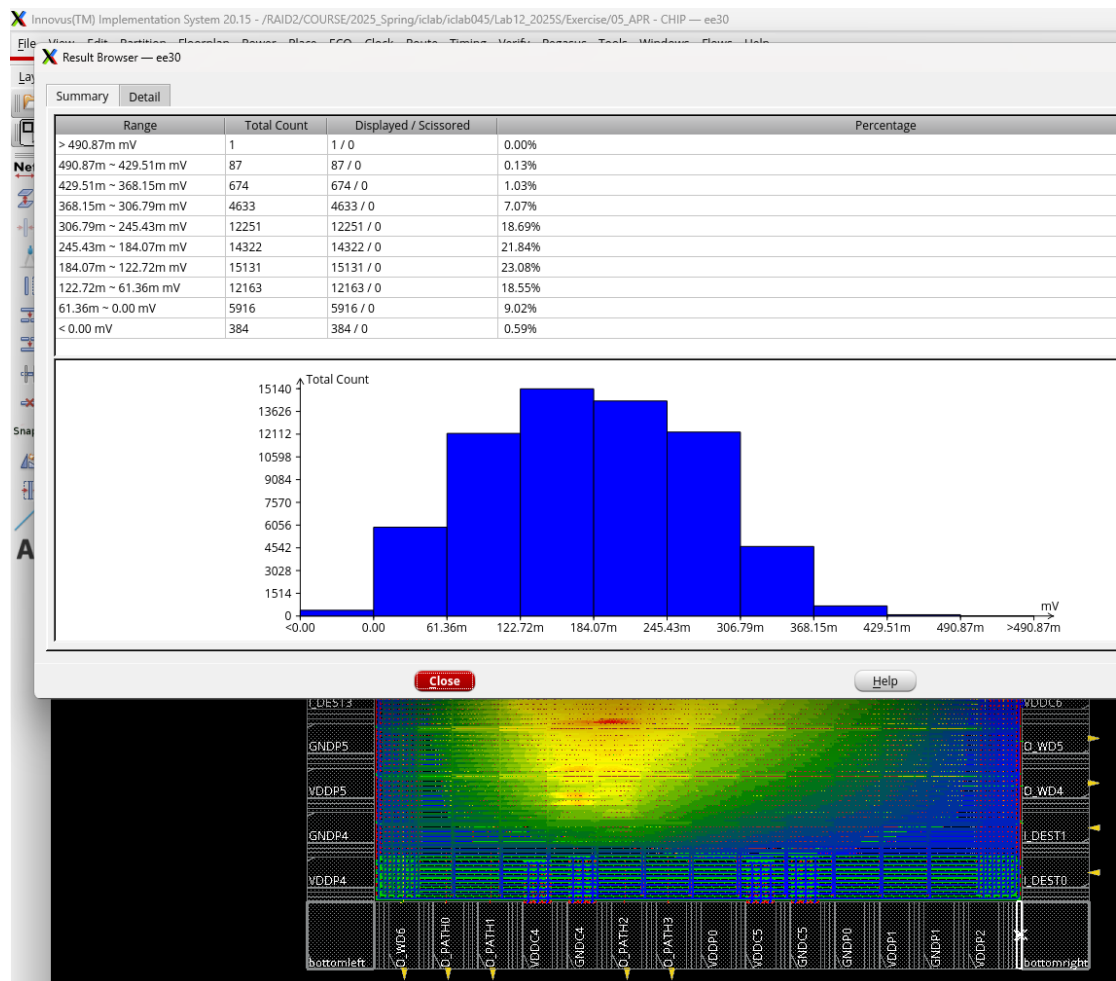
\$finish called from file "PATTERN.v", line 118.
\$finish at simulation time 1003228500
VCS Simulation Report
Time: 1003228500 ps
CPU Time: 21.390 seconds; Data structure size: 8.1M
Thu May 29 14:34:20 2025
CPU time: 4.593 seconds to compile + 1.517 seconds to elab + 1.
iclab045@ee26[~/Lab12_2025S/Exercise/06_POST]\$

9. Power result :



10. IR Drop Results :





To mitigate the IR drop issue, I used **power stripes** to stabilize voltage delivery across the standard cell rows and avoid IR drop on the cell's power lines. I also placed **8 core power pads evenly around the core perimeter** to minimize power path length and ensure balanced power distribution. Additionally, the chip was designed in a **square shape** to avoid excessively long horizontal or vertical power lines, further reducing the risk of voltage drop.