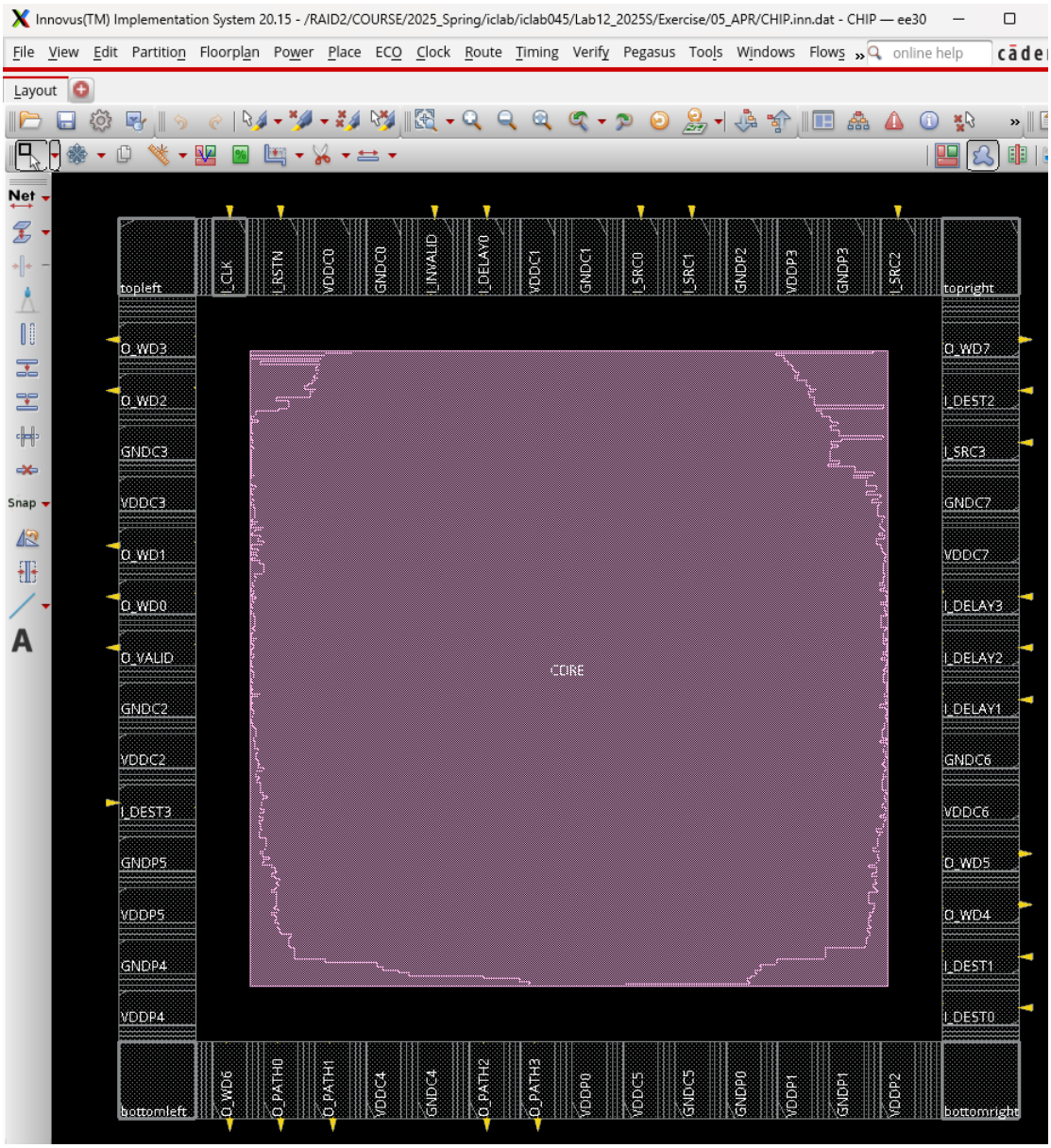
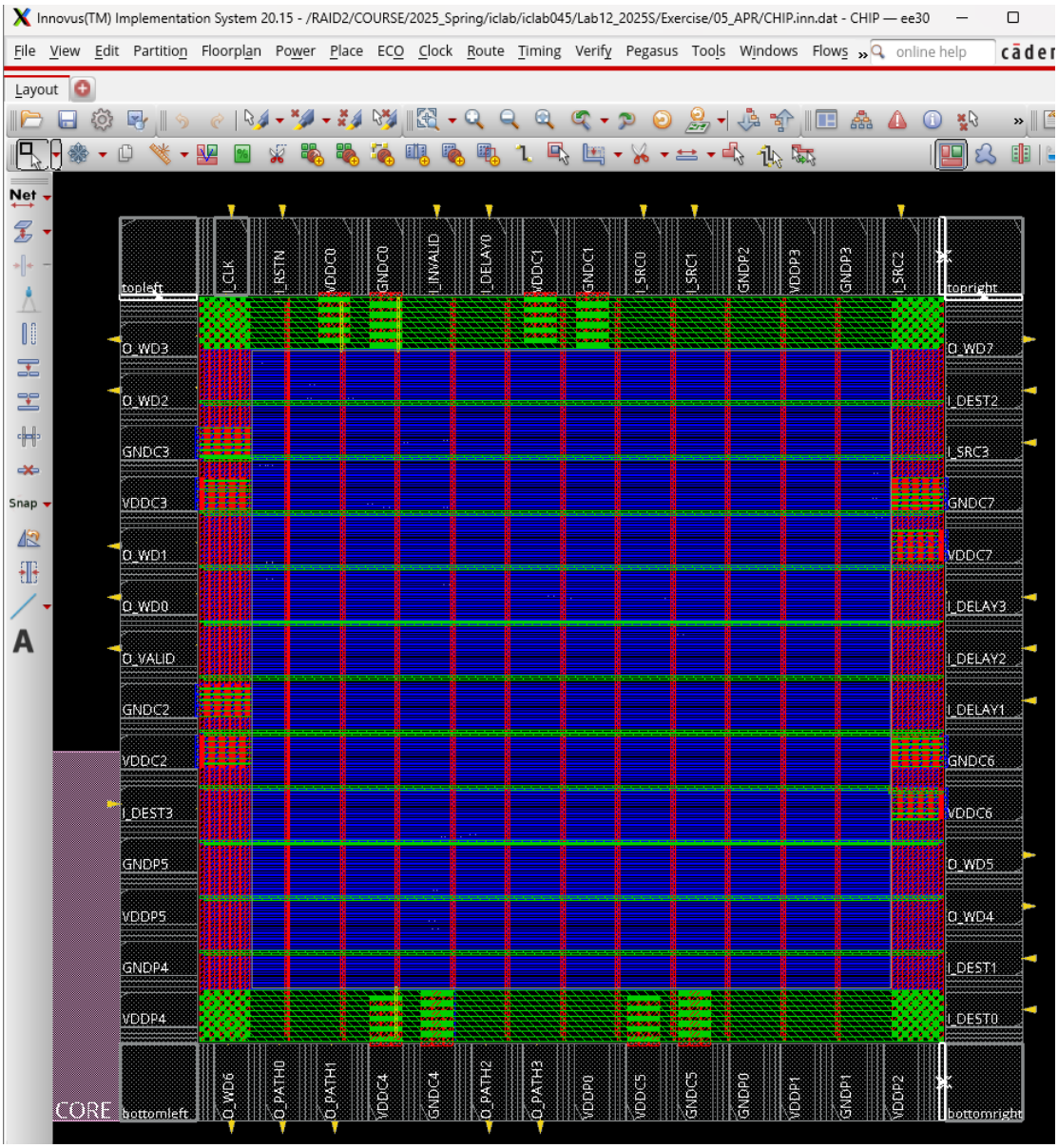
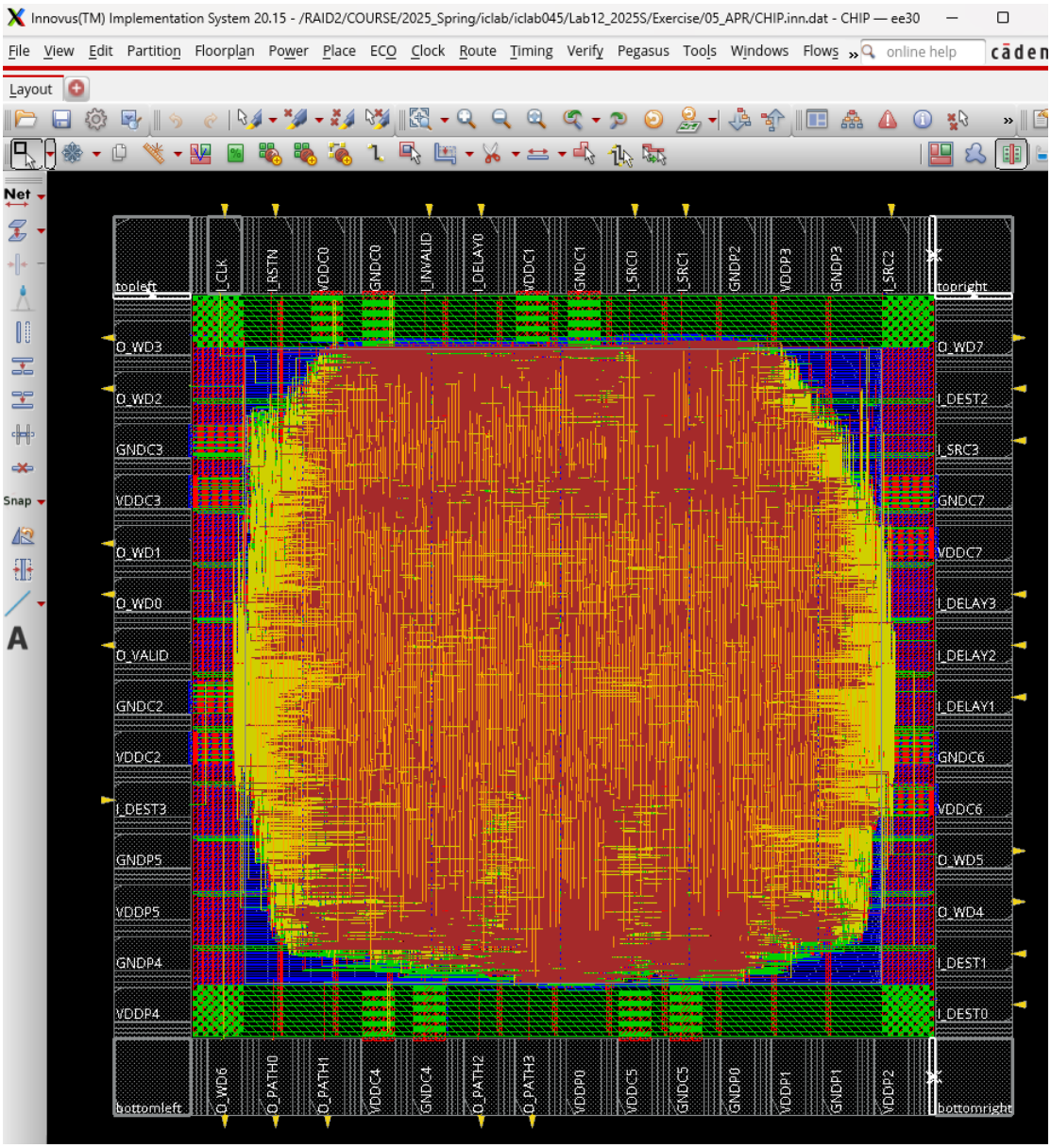
Report

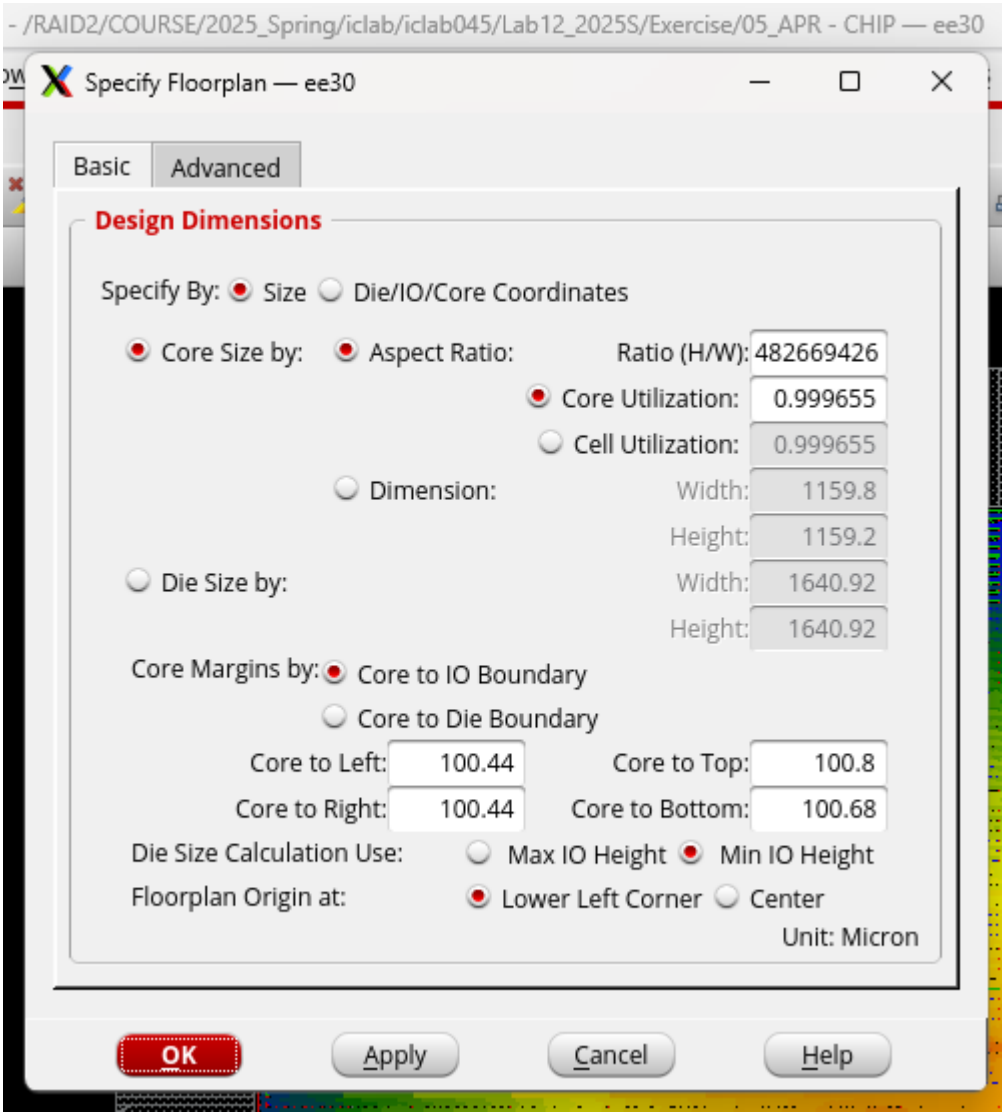
1. Chip Layout View :



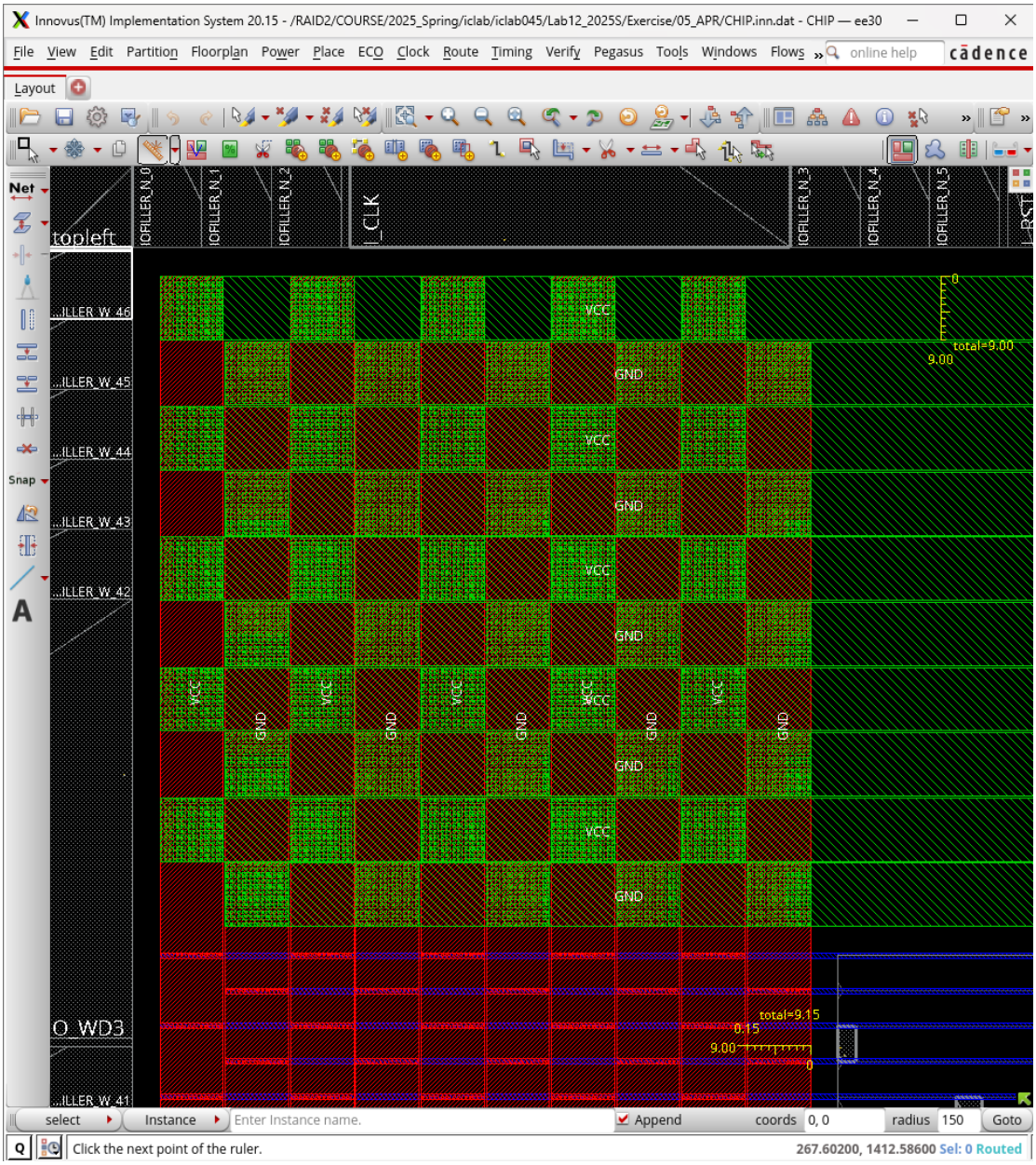

Innovus(TM) Implementation System 20.15 - /RAID2/COURSE/2025_Spring/iclab/iclab045/Lab12_2025S/Exercise/05_APR/CHIP.inn.dat - CHIP — ee30
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify Pegasus Tools Windows Flows
online help
Layout
Net
Snap
A
CORE
topleft
I_CLK
I_RSTN
VDDC0
GNDC0
I_INVALID
I_DELAY0
VDDC1
GNDC1
I_SRC0
I_SRC1
GNDP2
VDDP3
GNDP3
I_SRC2
topright
O_WD3
O_WD2
GNDC3
VDDC3
O_WD1
O_WD0
O_VALID
GNDC2
VDDC2
I_DEST3
GNDP5
VDDP5
GNDP4
VDDP4
O_WD7
I_DEST2
I_SRC3
GNDC7
VDDC7
I_DELAY3
I_DELAY2
I_DELAY1
GNDC6
VDDC6
O_WD5
O_WD4
I_DEST1
I_DEST0
bottomleft
O_WD6
O_PATH0
O_PATH1
VDDC4
GNDC4
O_PATH2
O_PATH3
VDDP0
VDDC5
GNDC5
GNDP0
VDDP1
GNDP1
VDDP2
bottomright



2. Core to IO boundary :


- /RAID2/COURSE/2025_Spring/iclab/iclab045/Lab12_2025S/Exercise/05_APR - CHIP — ee30
Specify Floorplan — ee30
Basic
Advanced
Design Dimensions
Specify By: Size Die/IO/Core Coordinates
Core Size by: Aspect Ratio: Ratio (H/W): 482669426
Core Utilization: 0.999655
Cell Utilization: 0.999655
Dimension: Width: 1159.8
Height: 1159.2
Die Size by: Width: 1640.92
Height: 1640.92
Core Margins by: Core to IO Boundary
Core to Die Boundary
Core to Left: 100.44
Core to Top: 100.8
Core to Right: 100.44
Core to Bottom: 100.68
Die Size Calculation Use: Max IO Height Min IO Height
Floorplan Origin at: Lower Left Corner Center
Unit: Micron
OK
Apply
Cancel
Help

3. Core Ring :


Innovus(TM) Implementation System 20.15 - /RAID2/COURSE/2025_Spring/iclab/iclab045/Lab12_2025S/Exercise/05_APR/CHIP.inn.dat - CHIP — ee30
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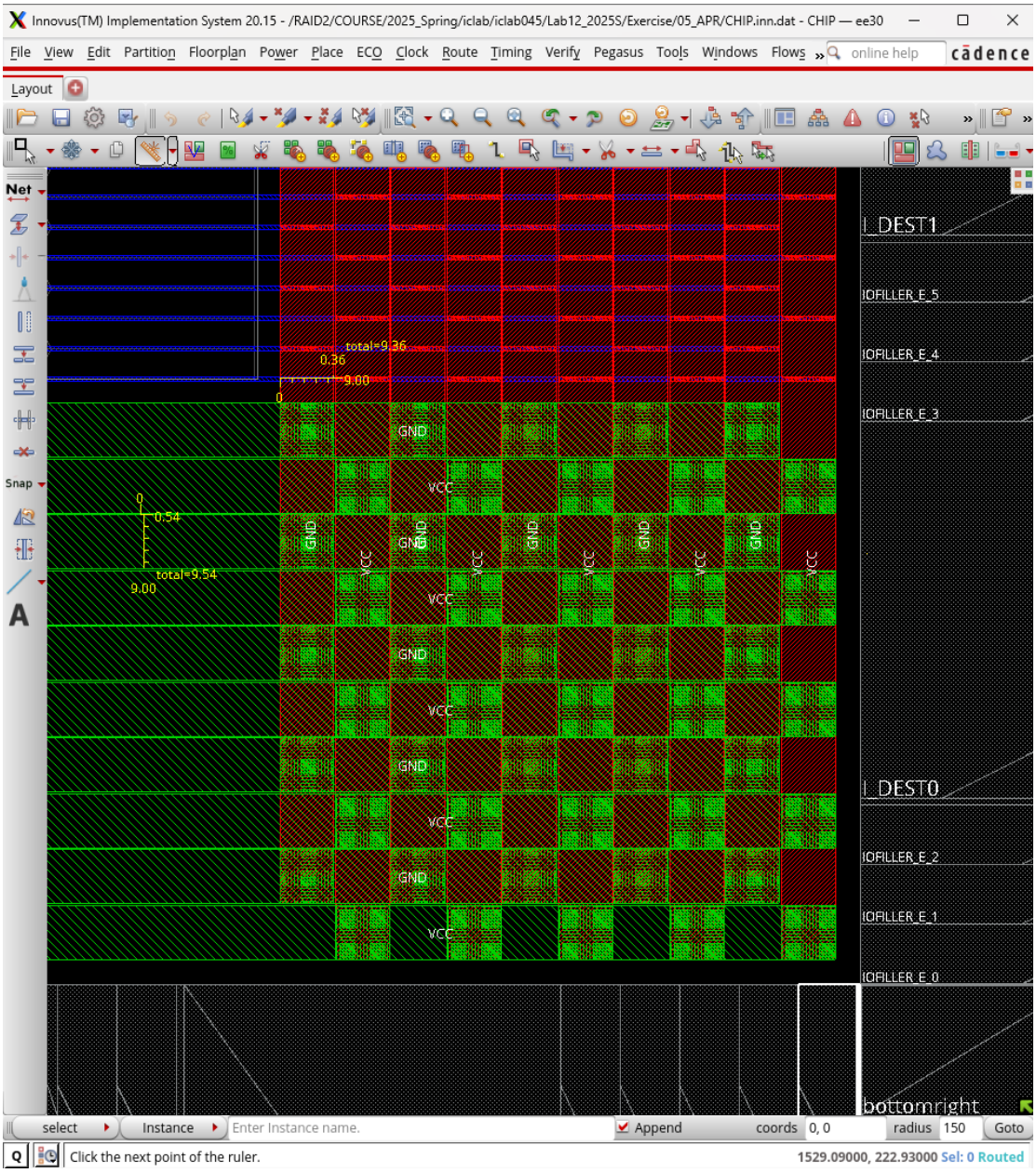
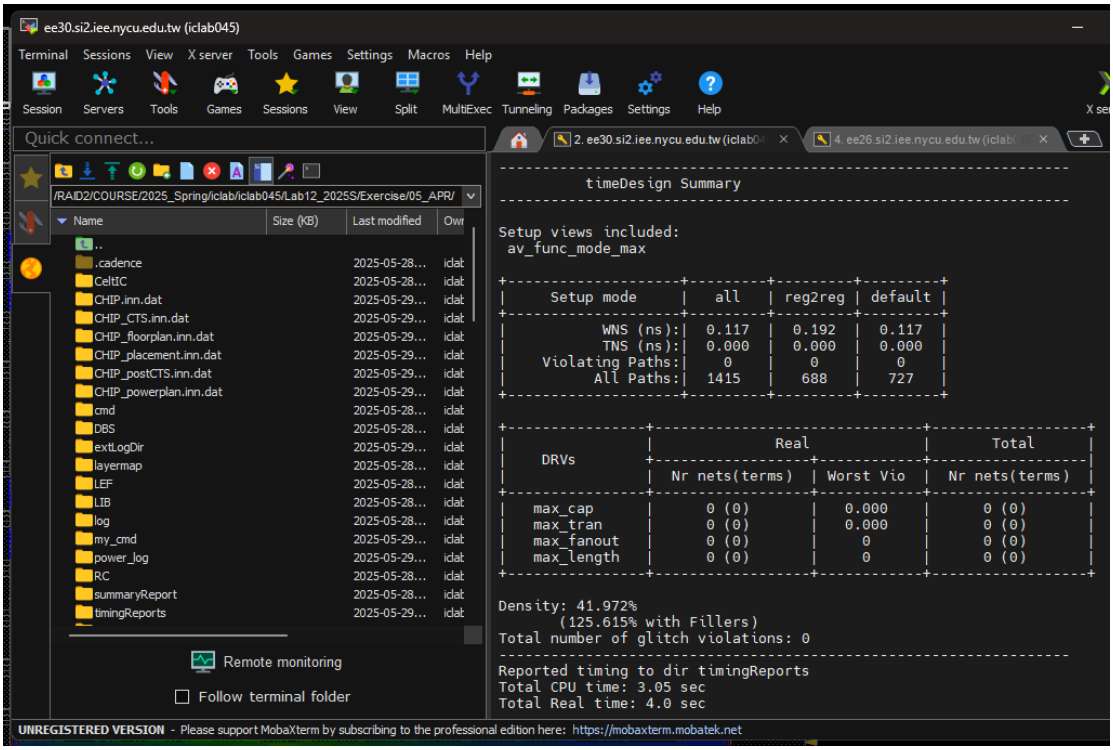
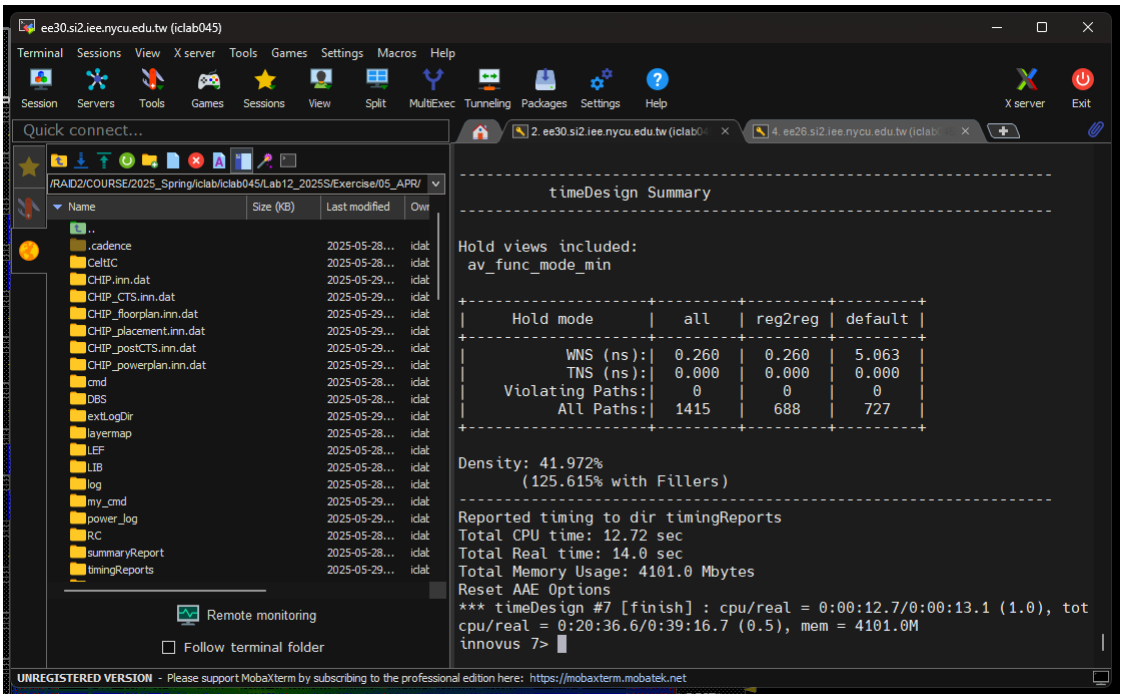
IOFILLER_N_0
IOFILLER_N_1
IOFILLER_N_2
I_CLK
IOFILLER_N_3
IOFILLER_N_4
IOFILLER_N_5
RST
...ILLER_W_46
...ILLER_W_45
...ILLER_W_44
...ILLER_W_43
...ILLER_W_42
...ILLER_W_41
O_WD3
VCC
GND
total=9.00
9.00
total=9.15
0.15
select
Instance
Enter Instance name.
Append
coords 0, 0
radius 150
Goto
Click the next point of the ruler.
267.60200, 1412.58600 Sel: 0 Routed



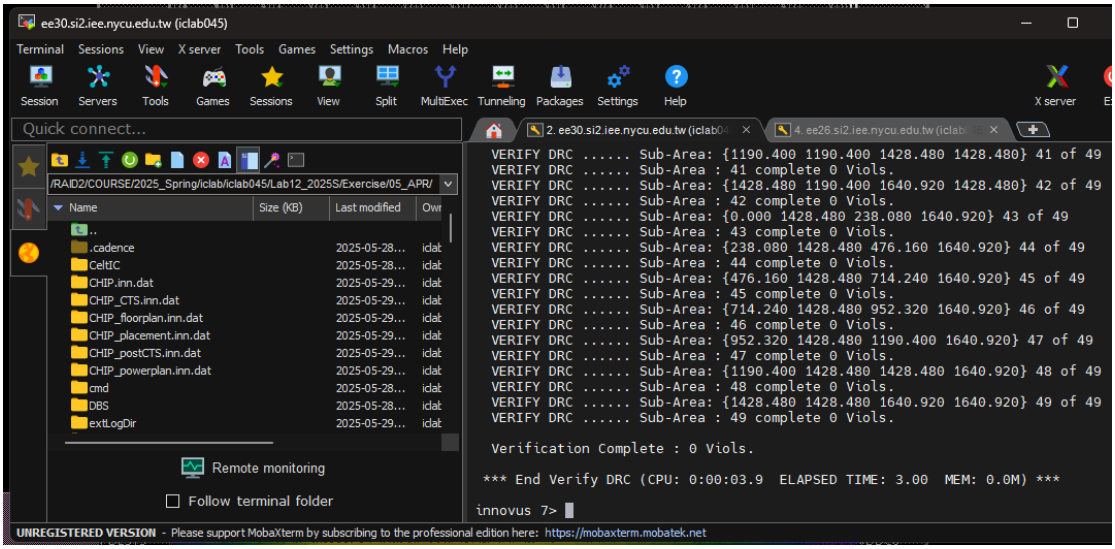
4. Post-Route setup time analysis :



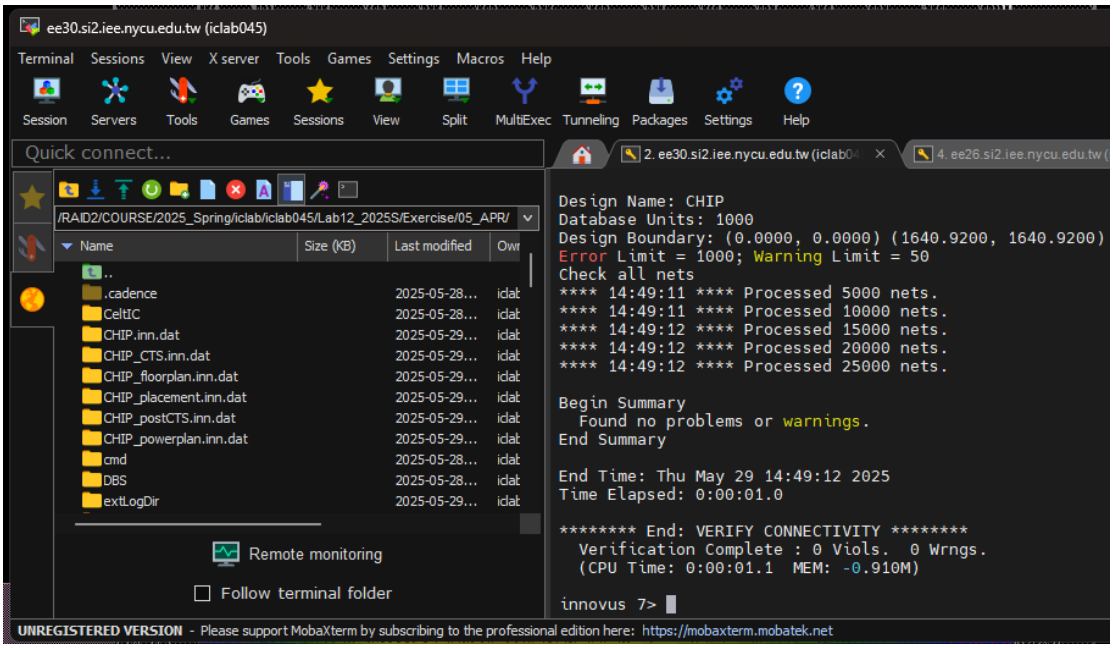
5. Post-Route hold time analysis :



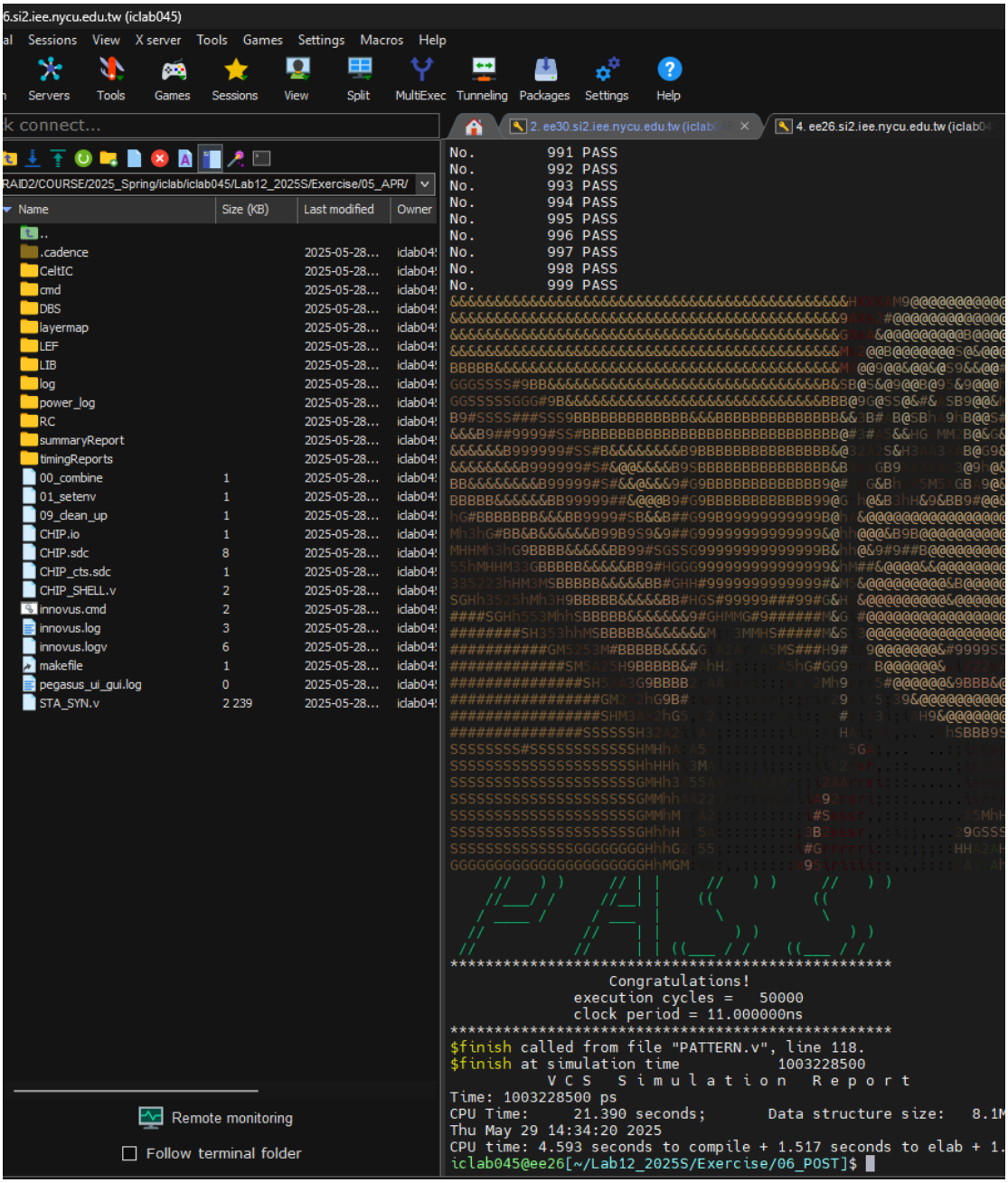
6. DRC result :



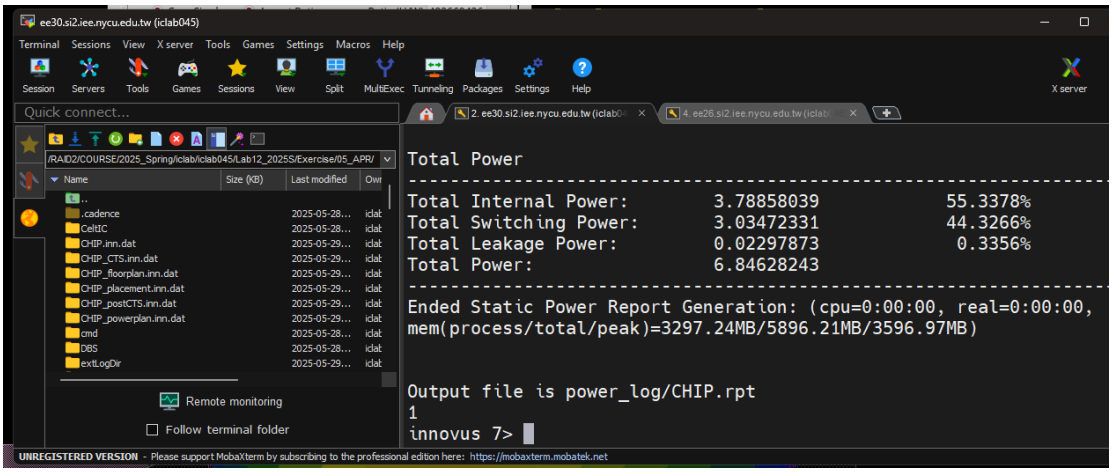
7. LVS result :



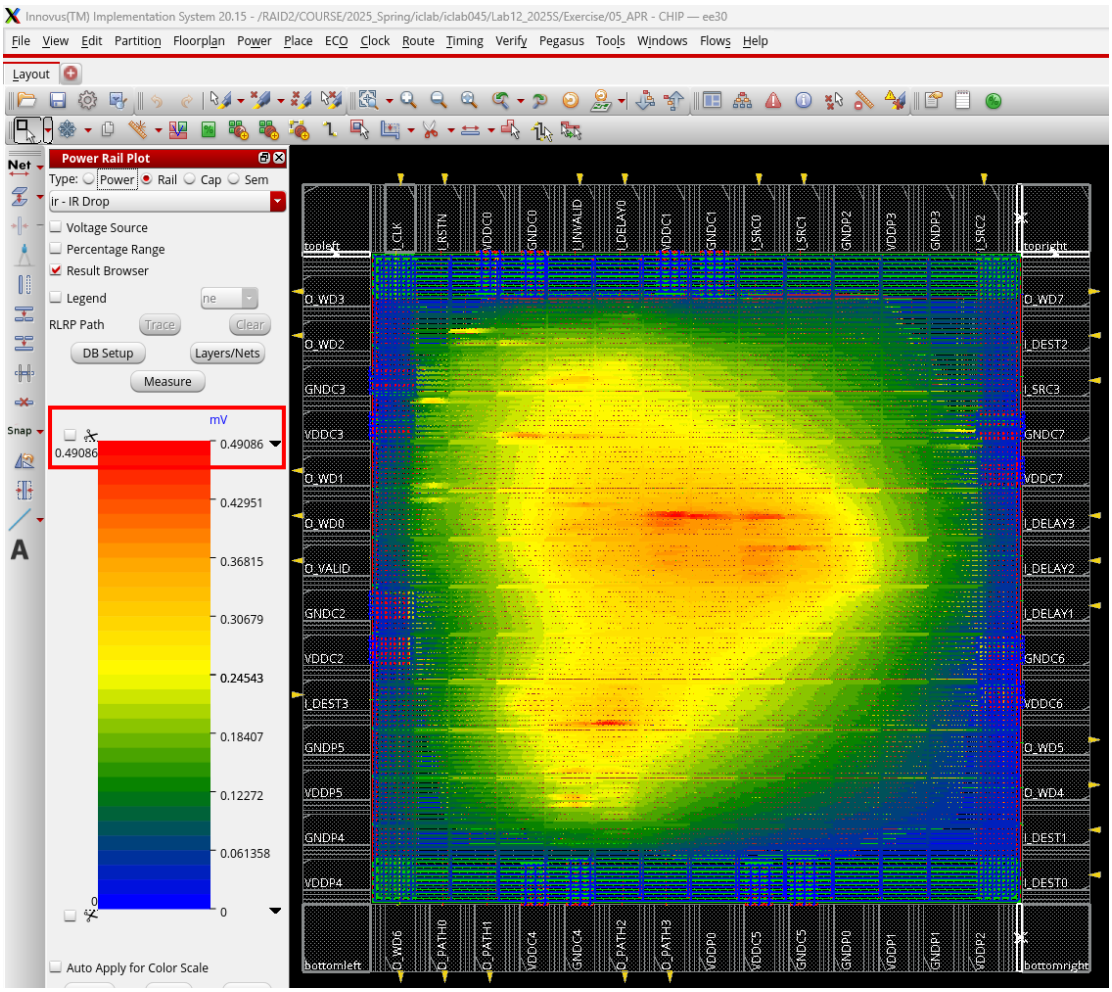
8. Post Layout simulation result :

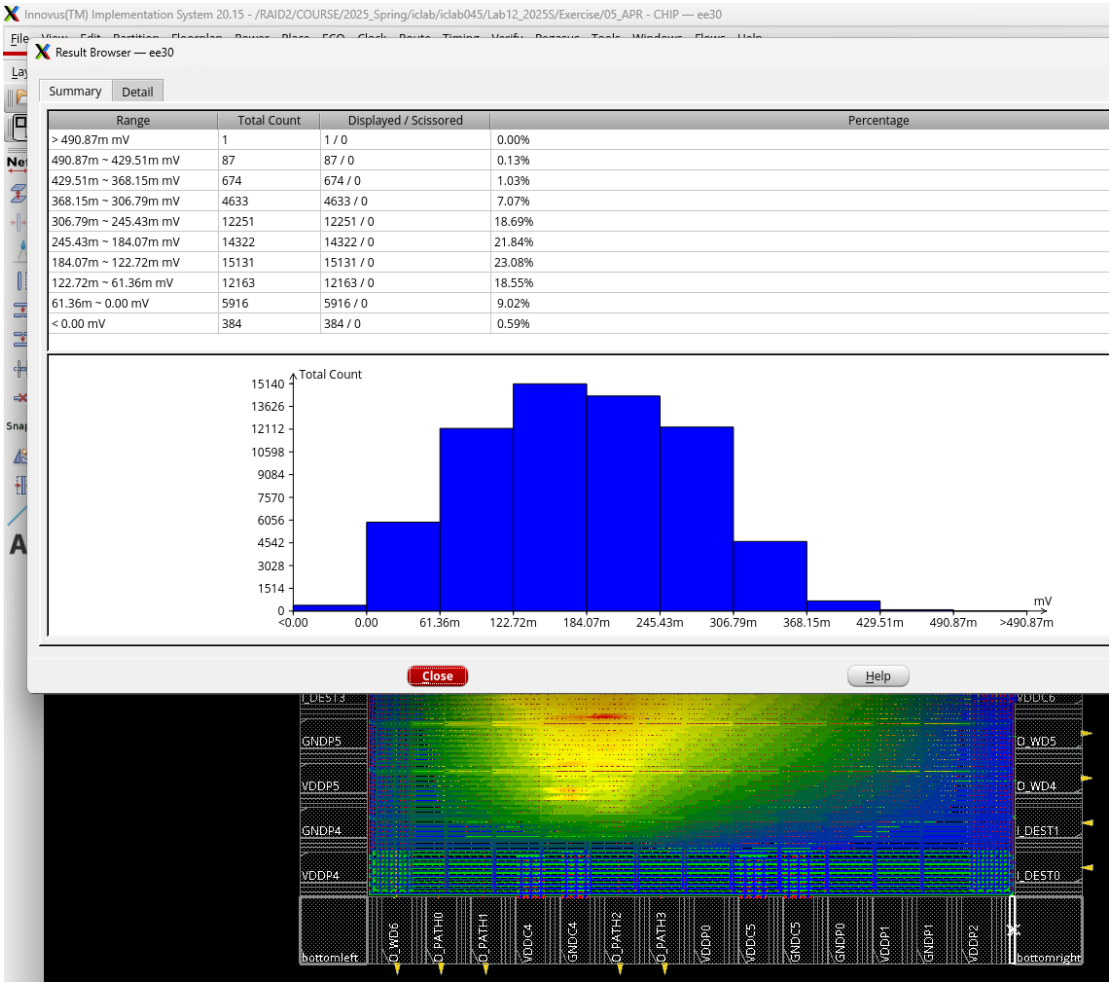


9. Power result :



10. IR Drop Results :





To mitigate the IR drop issue, I used power stripes to stabilize voltage delivery across the standard cell rows and avoid IR drop on the cell's power lines. I also placed 8 core power pads evenly around the core perimeter to minimize power path length and ensure balanced power distribution. Additionally, the chip was designed in a square shape to avoid excessively long horizontal or vertical power lines, further reducing the risk of voltage drop.