Bonus Homework

范真瑋

Gate count：

```
Number of ports:                          314
Number of nets:                           377
Number of cells:                          132
Number of combinational cells:             80
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       4

Combinational area:                706.118385
Buf/Inv area:                        0.000000
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wir

Total cell area:                   706.118385
```

(RCA)

Gate count = reported area / area of a NAND2 gate

Area of a NAND2 gate is approximately 5 um x um for 0.13um technology

此設計的面積為 706.118 um x um，因此 gate count 約為 141。

```
Number of ports:                          217
Number of nets:                           330
Number of cells:                          152
Number of combinational cells:            131
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                         16
Number of references:                      21

Combinational area:               1011.650393
Buf/Inv area:                       54.316799
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wir

Total cell area:                  1011.650393
```

(BCLA)

gate count 約為 202

```
Number of ports:                          358
Number of nets:                           437
Number of cells:                          152
Number of combinational cells:             96
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          4
Number of references:                       8

Combinational area:                828.331183
Buf/Inv area:                       13.579200
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wir

Total cell area:                   828.331183
```

(CSKA)

gate count 約為 166

```
Number of ports:                          551
Number of nets:                           691
Number of cells:                          251
Number of combinational cells:            155
Number of sequential cells:                 2
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                      11

Combinational area:               1424.118573
Buf/Inv area:                        0.000000
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wir

Total cell area:                  1424.118573
```

(CSEA)

gate count 約為 285

Critical path delay：

```
rca4/fa2/U1/Y (OR2X1)                    0.25       6.08 f
rca4/fa2/Cout (FA_2)                     0.00       6.08 f
rca4/fa3/Cin (FA_1)                      0.00       6.08 f
rca4/fa3/ha2/B (HA_2)                    0.00       6.08 f
rca4/fa3/ha2/U2/Y (AND2X1)               0.17       6.25 f
rca4/fa3/ha2/Cout (HA_2)                 0.00       6.25 f
rca4/fa3/U1/Y (OR2X1)                    0.25       6.50 f
rca4/fa3/Cout (FA_1)                     0.00       6.50 f
rca4/fa4/Cin (FA_0)                      0.00       6.50 f
rca4/fa4/ha2/B (HA_0)                    0.00       6.50 f
rca4/fa4/ha2/U2/Y (AND2X1)               0.17       6.67 f
rca4/fa4/ha2/Cout (HA_0)                 0.00       6.67 f
rca4/fa4/U1/Y (OR2X1)                    0.21       6.88 f
rca4/fa4/Cout (FA_0)                     0.00       6.88 f
rca4/Cout (RCA4_0)                       0.00       6.88 f
Cout (out)                               0.00       6.88 f
data arrival time                                   6.88
```

(RCA)

Timing Report 中，Incr 為節點造成的延遲時間，Path 為 Path 起點到此節點的總延遲時間，delay 為 6.88 ns。

```
Point                                    Incr       Path
-------------------------------------------------------------
input external delay                     0.00       0.00 f
A[1] (in)                                0.00       0.00 f
rfa2/A (RFA_14)                          0.00       0.00 f
rfa2/U5/Y (NOR2X1)                       0.11       0.11 r
rfa2/U4/Y (CLKINVX1)                     0.08       0.18 f
rfa2/P (RFA_14)                          0.00       0.18 f
bclg1/p[1] (BCLG4_4)                     0.00       0.18 f
bclg1/U4/Y (AO21X1)                      0.26       0.45 f
bclg1/U3/Y (AO21X1)                      0.24       0.69 f
bclg1/U2/Y (AO21X1)                      0.28       0.96 f
bclg1/Gout (BCLG4_4)                     0.00       0.96 f
bclg5/g[0] (BCLG4_0)                     0.00       0.96 f
bclg5/U7/Y (AO21X1)                      0.28       1.24 f
bclg5/U6/Y (AO21X1)                      0.30       1.54 f
bclg5/U5/Y (AO21X1)                      0.29       1.82 f
bclg5/Cout[3] (BCLG4_0)                  0.00       1.82 f
bclg4/Cin (BCLG4_1)                      0.00       1.82 f
bclg4/U7/Y (AO21X1)                      0.28       2.11 f
bclg4/U6/Y (AO21X1)                      0.28       2.39 f
bclg4/U5/Y (AO21X1)                      0.27       2.66 f
bclg4/Cout[3] (BCLG4_1)                  0.00       2.66 f
rfa16/Cin (RFA_0)                        0.00       2.66 f
rfa16/U1/Y (MXI2X1)                      0.14       2.80 f
rfa16/Sum (RFA_0)                        0.00       2.80 f
Sum[15] (out)                            0.00       2.80 f
data arrival time                                   2.80
```

(BCLA)

delay 為 2.80 ns。

```
rca4/fa1/U1/Y (OR2X1)                    0.25       6.13 f
rca4/fa1/Cout (FA_3)                     0.00       6.13 f
rca4/fa2/Cin (FA_2)                      0.00       6.13 f
rca4/fa2/ha2/B (HA_4)                    0.00       6.13 f
rca4/fa2/ha2/U2/Y (AND2X1)               0.17       6.30 f
rca4/fa2/ha2/Cout (HA_4)                 0.00       6.30 f
rca4/fa2/U1/Y (OR2X1)                    0.25       6.55 f
rca4/fa2/Cout (FA_2)                     0.00       6.55 f
rca4/fa3/Cin (FA_1)                      0.00       6.55 f
rca4/fa3/ha2/B (HA_2)                    0.00       6.55 f
rca4/fa3/ha2/U2/Y (AND2X1)               0.17       6.72 f
rca4/fa3/ha2/Cout (HA_2)                 0.00       6.72 f
rca4/fa3/U1/Y (OR2X1)                    0.25       6.97 f
rca4/fa3/Cout (FA_1)                     0.00       6.97 f
rca4/fa4/Cin (FA_0)                      0.00       6.97 f
rca4/fa4/ha2/B (HA_0)                    0.00       6.97 f
rca4/fa4/ha2/U2/Y (AND2X1)               0.17       7.14 f
rca4/fa4/ha2/Cout (HA_0)                 0.00       7.14 f
rca4/fa4/U1/Y (OR2X1)                    0.24       7.38 f
rca4/fa4/Cout (FA_0)                     0.00       7.38 f
rca4/Cout (RCA4_0)                       0.00       7.38 f
skip3/cout (skipLogic_0)                 0.00       7.38 f
skip3/U2/Y (CLKINVX1)                    0.04       7.42 r
skip3/U1/Y (OAI21XL)                     0.04       7.46 f
skip3/cin_next (skipLogic_0)             0.00       7.46 f
Cout (out)                               0.00       7.46 f
data arrival time                                   7.46
```

(CSKA)

delay 為 7.46 ns。

```
rca1/fa2/ha2/U2/Y (AND2X1)               0.17       0.77 f
rca1/fa2/ha2/Cout (HA_52)                0.00       0.77 f
rca1/fa2/U1/Y (OR2X1)                    0.25       1.02 f
rca1/fa2/Cout (FA_26)                    0.00       1.02 f
rca1/fa3/Cin (FA_25)                     0.00       1.02 f
rca1/fa3/ha2/B (HA_50)                   0.00       1.02 f
rca1/fa3/ha2/U2/Y (AND2X1)               0.17       1.19 f
rca1/fa3/ha2/Cout (HA_50)                0.00       1.19 f
rca1/fa3/U1/Y (OR2X1)                    0.25       1.44 f
rca1/fa3/Cout (FA_25)                    0.00       1.44 f
rca1/fa4/Cin (FA_24)                     0.00       1.44 f
rca1/fa4/ha2/B (HA_48)                   0.00       1.44 f
rca1/fa4/ha2/U2/Y (AND2X1)               0.17       1.61 f
rca1/fa4/ha2/Cout (HA_48)                0.00       1.61 f
rca1/fa4/U1/Y (OR2X1)                    0.35       1.95 f
rca1/fa4/Cout (FA_24)                    0.00       1.95 f
rca1/Cout (RCA4_6)                       0.00       1.95 f
U8/Y (AO21X1)                            0.42       2.37 f
U7/Y (AO21X1)                            0.42       2.79 f
U6/Y (AO21X1)                            0.28       3.07 f
Cout (out)                               0.00       3.07 f
data arrival time                                   3.07
```

(CSEA)

delay 為 3.07 ns。

Power consumption：

```
  Cell Internal Power  =  86.8234 uW   (83%)
  Net Switching Power  =  18.3781 uW   (17%)
                         ---------
Total Dynamic Power    = 105.2015 uW  (100%)

Cell Leakage Power     = 955.1019 nW
```

(RCA)

從 Power Report 中得知，Dynamic power 為 105.2015 uW，Static power 為 955.1019 nW。

```
  Cell Internal Power  =  87.0970 uW   (73%)
  Net Switching Power  =  32.1521 uW   (27%)
                         ---------
Total Dynamic Power    = 119.2491 uW  (100%)

Cell Leakage Power     =   1.1011 uW
```

(BCLA)

Dynamic power 為 119.2491 uW，Static power 為 1.1011 uW。

```
  Cell Internal Power  =  93.7537 uW   (81%)
  Net Switching Power  =  21.8795 uW   (19%)
                         ---------
Total Dynamic Power    = 115.6331 uW  (100%)

Cell Leakage Power     = 979.0593 nW
```

(CSKA)

Dynamic power 為 115.6331 uW，Static power 為 979.0593 nW。

```
  Cell Internal Power  = 176.4886 uW   (79%)
  Net Switching Power  =  45.9920 uW   (21%)
                         ---------
Total Dynamic Power    = 222.4806 uW  (100%)

Cell Leakage Power     =   1.9593 uW
```

(CSEA)

Dynamic power 為 222.4806 uW，Static power 為 1.9593 uW。

結果分析：

- 面積(gate count)

RCA	BCLA	CSKA	CSEA
141	202	166	285

- critical path delay

RCA	BCLA	CSKA	CSEA
6.88	2.80	7.46	3.07

- 功率消耗

RCA	BCLA	CSKA	CSEA
105.2015	119.2491	115.6331	222.4806

首先在面積方面觀察到，RCA 的面積最小，CSEA 的面積最大，因為 RCA 是最基礎的加法器，而 CSEA 在每部分都使用 2 個 RCA 來分別計算不同 carry in 的結果再做選擇，因此面積最大，而功率消耗與 gate count 呈現一定的正相關關係。

在 delay 方面，由於此處使用 critical path delay 做比較，所以 CSKA 的 delay 反而是最大的，但實際運作上，CSKA 的 delay 應該能介於 BCLA 與 CSEA 之間。再來就是 RCA 的 delay 為第二長，也驗證了最直覺的想法做出來的電路，通常效能不會太好。