# Digital Logic Gates

2016/10/3

范真瑋

## Ex1

實驗內容：

**Exercise 1**

- Find and show the sum of minterms (*F1*) of the following truth table
- Find and show the product of maxterms (*F2*) of the following truth table
- Verify *F1* = *F2* (using Dataflow modeling)

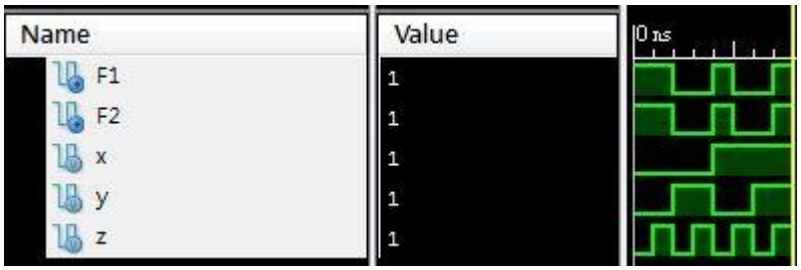
| *x* | *y* | *z* | *F* | *F'* |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

程式碼：

```
module Ex1(F1, F2, x, y, z);
output F1, F2;
input x, y, z;

wire F1, F2, x, y, z;

assign F1 = (~x&~y&~z) | (~x&~y&z) | (x&~y&~z) | (x&y&z);
assign F2 = (x|~y|z) & (x|~y|~z) & (~x|y|~z) & (~x|~y|z);


endmodule
```

```
module Ex1_tb;

   reg x;
   reg y;
   reg z;
   // Outputs
   wire F1;
   wire F2;

   // Instantiate the Unit Under Test (UUT)
   Ex1 uut (
      .x(x),
      .y(y),
      .z(z),
      .F1(F1),
      .F2(F2)
   );

   initial begin
      // Initialize Inputs
       x=0;y=0;z=0;
      #10 x=0;y=0;z=1;
      #10 x=0;y=1;z=0;
      #10 x=0;y=1;z=1;
      #10 x=1;y=0;z=0;
      #10 x=1;y=0;z=1;
      #10 x=1;y=1;z=0;
      #10 x=1;y=1;z=1;
      #10 $finish;
   end
endmodule
```

實驗結果及分析：




Sum of minterms (F1) = x'y'z' + x'y'z + xy'z' + xyz  (a sum of AND terms)
Product of maxterms (F2) = (x+y'+z)(x+y'+z')(x'+y+z')(x'y'z)  (OR terms)

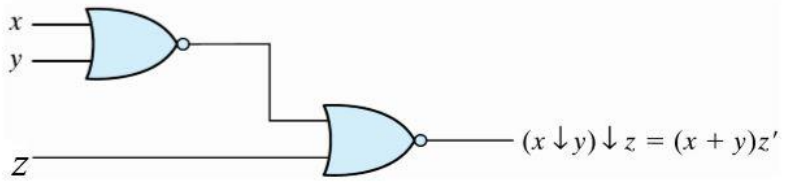
由實驗結果圖中的波形得知 F1 = F2

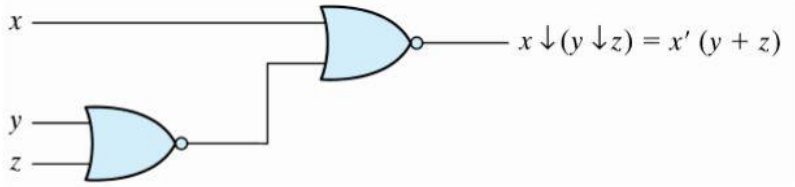
# Ex2

實驗內容：

## Exercise 2

- Derive $(x \downarrow y) \downarrow z = (x + y)z'$ and
  $x \downarrow (y \downarrow z) = x'(y + z)$ (applying DeMorgan's theorem)
- Verify $(x \downarrow y) \downarrow z = (y \downarrow x) \downarrow z$ (using Structural level modeling)
- Verify $(x \downarrow y) \downarrow z \neq x \downarrow (y \downarrow z)$ (using Structural level modeling)




程式碼：

```
module Ex2(S1, S2, S3, S4, C1, C2, C3, C4, x, y, z);
output S1, S2, S3, S4, C1, C2, C3, C4;
input x, y, z;

wire S1, S2, S3, S4, C1, C2, C3, C4, x, y, z;

nor(S1, x, y);
nor(S2, S1, z);
nor(C1, y, x);
nor(C2, C1, z);

nor(S3, x, y);
nor(S4, S3, z);
nor(C3, y, z);
nor(C4, C3, x);

endmodule
```

```
module Ex2_tb;
    reg x;
    reg y;
    reg z;
    // Outputs
    wire S1;
    wire S2;
    wire S3;
    wire S4;
    wire C1;
    wire C2;
    wire C3;
    wire C4;

    // Instantiate the Unit Under Test (UUT)
    Ex2 uut (
        .x(x),
        .y(y),
        .z(z),
        .S1(S1),
        .S2(S2),
        .S3(S3),
        .S4(S4),
        .C1(C1),
        .C2(C2),
        .C3(C3),
        .C4(C4)
    );

    initial begin
        // Initialize Inputs
        x=0;y=0;z=0;
        #10 x=0;y=0;z=1;
        #10 x=0;y=1;z=0;
        #10 x=0;y=1;z=1;
        #10 x=1;y=0;z=0;
        #10 x=1;y=0;z=1;
        #10 x=1;y=1;z=0;
        #10 x=1;y=1;z=1;
        #10 $finish;
    end
endmodule
```

實驗結果及分析：


$(x \downarrow y) \downarrow z = [(x + y)' + z]' = (x + y)z'$

$x \downarrow (y \downarrow z) = [x + (y + z)']' = x'(y + z)$

由實驗結果圖中的波形得知 S2 = C2 ，所以$(x \downarrow y) \downarrow z = (y \downarrow x) \downarrow z$

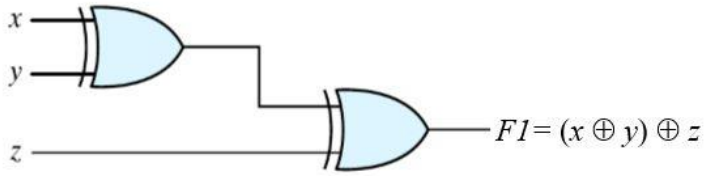
S4≠C4 ，所以$(x \downarrow y) \downarrow z \neq x \downarrow (y \downarrow z)$

# Ex3

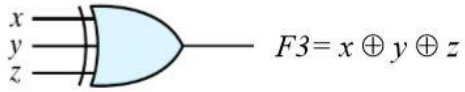
實驗內容：

## Exercise 3

- $F1 = (x \oplus y) \oplus z$, $F2 = x \oplus (y \oplus z)$, $F3 = x \oplus y \oplus z$
- Verify $F1 = F2 = F3$ (using Schematic)




(a) Using 2-input gates

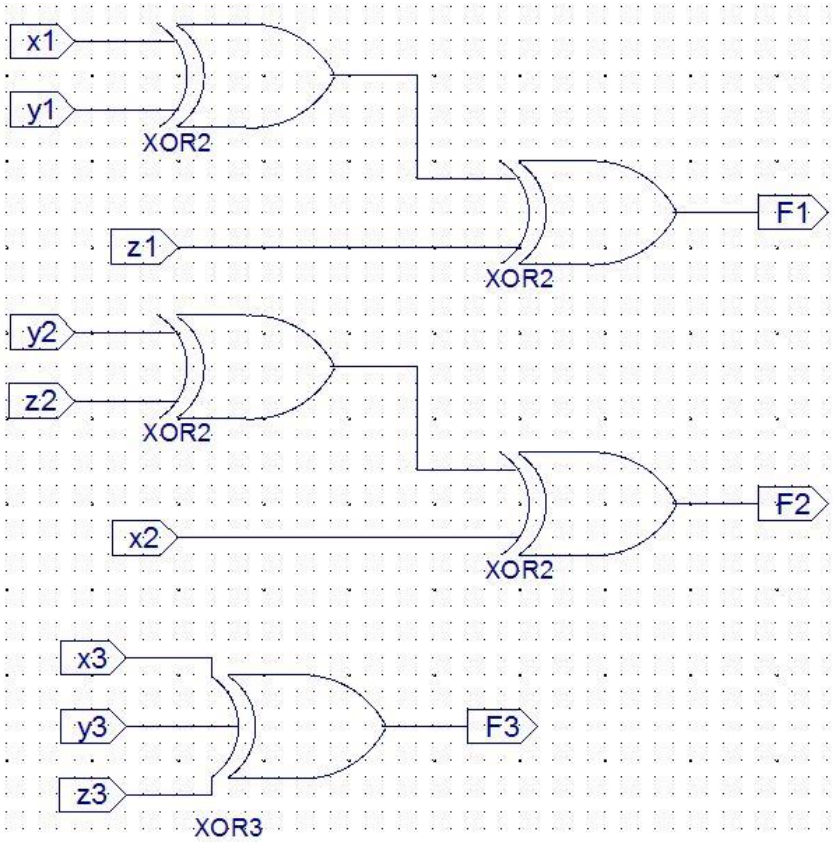



(b) 3-input gate

| x | y | z | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

(c) Truth table

電路圖：

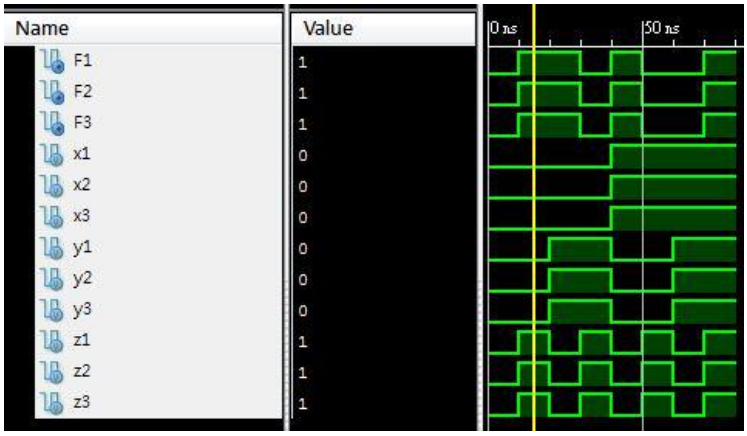


程式碼：

```
module Ex3_Ex3_sch_tb();

// Inputs
reg x1;
reg x2;
reg x3;
reg y1;
reg y2;
reg y3;
reg z1;
reg z2;
reg z3;

// Output
wire F1;
wire F2;
wire F3;

// Bidirs

// Instantiate the UUT
   Ex3 UUT (
       .x1(x1),
       .x2(x2),
       .x3(x3),
       .y1(y1),
       .y2(y2),
       .y3(y3),
       .z1(z1),
       .z2(z2),
       .z3(z3),
       .F1(F1),
       .F2(F2),
       .F3(F3)
   );
```

```
// Initialize Inputs
   initial begin
      x1=0;y1=0;z1=0;
      x2=0;y2=0;z2=0;
      x3=0;y3=0;z3=0;
      #10
      x1=0;y1=0;z1=1;
      x2=0;y2=0;z2=1;
      x3=0;y3=0;z3=1;
      #10
      x1=0;y1=1;z1=0;
      x2=0;y2=1;z2=0;
      x3=0;y3=1;z3=0;
      #10
      x1=0;y1=1;z1=1;
      x2=0;y2=1;z2=1;
      x3=0;y3=1;z3=1;
      #10
      x1=1;y1=0;z1=0;
      x2=1;y2=0;z2=0;
      x3=1;y3=0;z3=0;
      #10
      x1=1;y1=0;z1=1;
      x2=1;y2=0;z2=1;
      x3=1;y3=0;z3=1;
      #10
      x1=1;y1=1;z1=0;
      x2=1;y2=1;z2=0;
      x3=1;y3=1;z3=0;
      #10
      x1=1;y1=1;z1=1;
      x2=1;y2=1;z2=1;
      x3=1;y3=1;z3=1;
      #10 $finish;
   end
endmodule
```

實驗結果及分析：




由實驗結果圖中的波形得知 F1 = F2 = F3