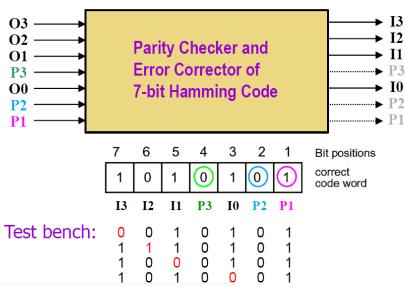
FPGA Board 2016/11/14

范真瑋

實驗內容:

Exercise: Parity Checker and Error Corrector

Design and verify the Parity Checker and Error Corrector of 7-bit Hamming Code using FPGA board



程式碼:

```
21 module corrector(I3, I2, I1, I0, O3, O2, O1, O0, P3, P2, P1);
22  output I3,I2,I1,I0;
23  wire [0:7]D;
24 wire A,B,C;
25 input 03,02,01,00,P3,P2,P1;
26
    _generate x1(C,B,A,O3,O2,O1,O0,P3,P2,P1);
    assign D[0] = (~C) && (~B) && (~A),
27
            D[1] = (\sim C) \&\& (\sim B) \&\& (A),
28
            D[2] = (~C) && (B) && (~A),
29
            D[3] = (\sim C) \&\& (B) \&\& (A),
30
            D[4] = (C) && (\sim B) && (\sim A),
31
            D[5] = (C) && (~B) && (A),
            D[6] = (C) && (B) && (~A),
33
34
            D[7] = (C) && (B) && (A);
35 assign IO = 00 ^ D[3],
            I1 = O1 ^ D[5],
36
            I2 = O2 ^ D[6],
37
            I3 = O3 ^ D[7];
38
    endmodule
39
40
    module _generate(C3,C2,C1,O3,O2,O1,O0,P3,P2,P1);
output C3,C2,C1;
41
42
43 input 03,02,01,00,P3,P2,P1;
44
    assign C1 = 03^02^01^P3,
45
            C2 = O3^02^00^P2.
46
            C3 = O3^01^00^P1;
47
48 endmodule
```

```
25 module hamming_tb;
26
       // Inputs
27
      reg 03;
28
      reg 02;
29
      reg 01;
30
      reg 00;
31
      reg P3;
32
33
      reg P2;
34
      reg P1;
35
      // Outputs
36
37
      wire I3;
      wire I2;
38
      wire I1;
39
      wire IO;
40
41
      // Instantiate the Unit Under Test (UUT)
42
43
      corrector uut (
44
          .I3(I3),
          .I2(I2),
45
          .I1(I1),
46
          .IO(IO),
47
48
          .03(03),
          .02(02),
49
         .01(01),
50
51
         .00(00),
52
          .P3(P3),
53
          .P2(P2),
          .P1(P1)
54
      );
55
56
      initial begin
57
58
         // Initialize Inputs
         03 = 0;
59
         02 = 0;
60
         01 = 1;
61
         P3 = 0;
62
63
          00 = 1;
          P2 = 0;
64
          P1 = 1;
65
       end
66
67
68 endmodule
```

實驗分析:

利用 parity checker 加上 decoder 可以找出 Hamming Code 錯誤的位置並修正