

# Synopsys Design Vision EDA tool

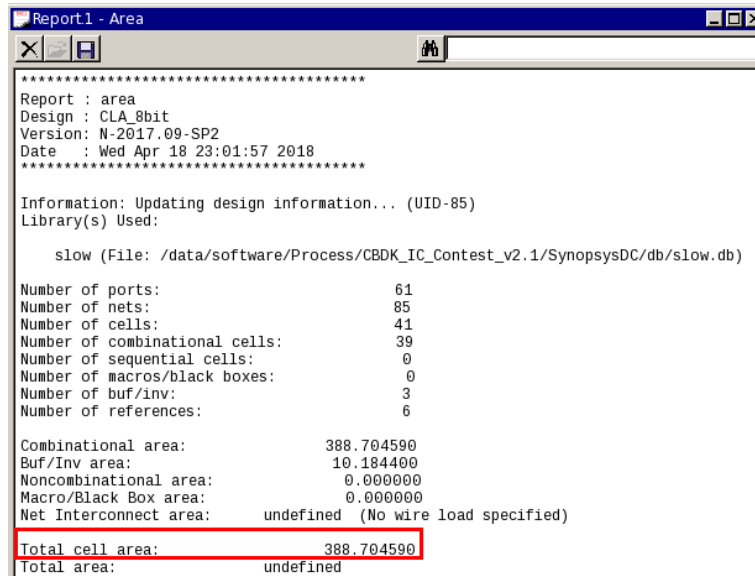
范真瑋

合成步驟：

1. 設置.synopsys\_dc.setup
2. 使用指令 dv 調用 design compiler
3. 檢查 Library 是否正確載入
4. 讀取檔案
5. 選擇 TOP module   current\_design CLA\_8bit
6. 加入 Buffer   set\_fix\_multiple\_port\_nets -all -buffer\_constants
7. 移除空接腳位   remove\_unconnected\_ports -blast\_buses [get\_cells \* -hier]
8. Design→Compile Design
9. 查看 Area、Timing、Power Report、Critical Path
10. 儲存電路(CLA\_syn.v)與.sdf 檔案  
      write\_sdf -version 1.0 -context verilog CLA.sdf
11. 修改 testbench
12. 在 CLA\_syn.v 中加入與 testbench 相同的`timescale
13. 輸入指令進行模擬   ncverilog CLA\_tb.v +access+r
14. 使用 SimVision 觀察波型

Gate count :

(RTL)



```
Report1 - Area
*****
Report : area
Design : CLA_8bit
Version: N-2017.09-SP2
Date   : Wed Apr 18 23:01:57 2018
*****
Information: Updating design information... (UID-85)
Library(s) Used:
    slow (File: /data/software/Process/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:          61
Number of nets:           85
Number of cells:          41
Number of combinational cells: 39
Number of sequential cells:  0
Number of macros/black boxes: 0
Number of buf/inv:        3
Number of references:      6

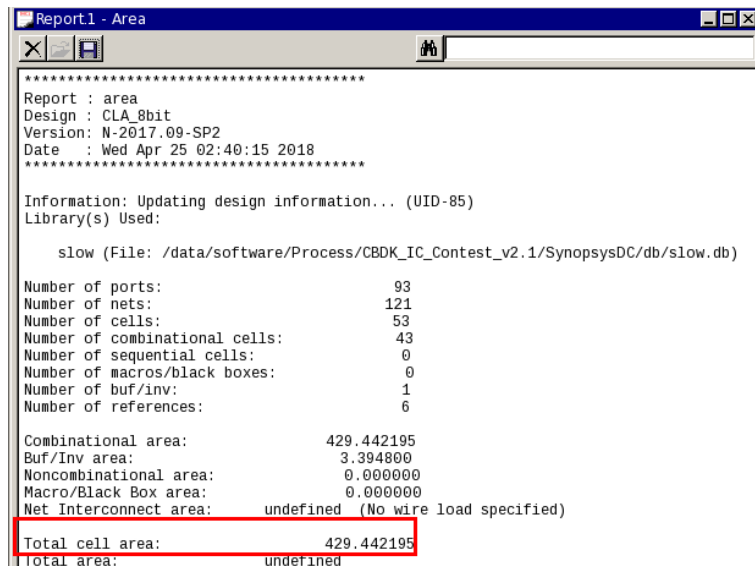
Combinational area:      388.704590
Buf/Inv area:            10.184400
Noncombinational area:   0.000000
Macro/Black Box area:    0.000000
Net Interconnect area:   undefined (No wire load specified)
Total cell area:         388.704590
Total area:              undefined
```

Gate count = reported area / area of a NAND2 gate

Area of a NAND2 gate is approximately 5 um x um for 0.13um technology

此設計的面積為 388.705 um x um ，因此 gate count 約為 78 。

(gate level)



```
Report1 - Area
*****
Report : area
Design : CLA_8bit
Version: N-2017.09-SP2
Date   : Wed Apr 25 02:40:15 2018
*****
Information: Updating design information... (UID-85)
Library(s) Used:
    slow (File: /data/software/Process/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:          93
Number of nets:           121
Number of cells:          53
Number of combinational cells: 43
Number of sequential cells:  0
Number of macros/black boxes: 0
Number of buf/inv:        1
Number of references:      6

Combinational area:      429.442195
Buf/Inv area:            3.394800
Noncombinational area:   0.000000
Macro/Black Box area:    0.000000
Net Interconnect area:   undefined (No wire load specified)
Total cell area:         429.442195
Total area:              undefined
```

此設計的面積為 429.442 um x um ，因此 gate count 約為 86 。

## Critical path delay :

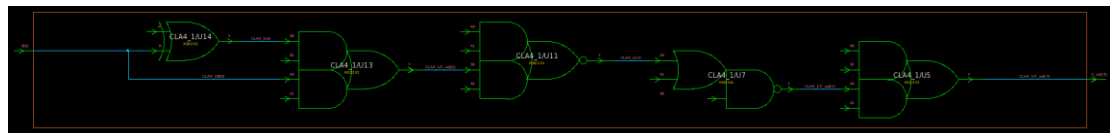
### (RTL)

Operating Conditions: slow Library: slow  
Wire Load Model Mode: top

Startpoint: B[0] (input port)  
Endpoint: C\_out (output port)  
Path Group: (none)  
Path Type: max

Point	Incr	Path
input external delay	0.00	0.00 r
B[0] (in)	0.00	0.00 r
U20/Y (XNOR2X1)	0.14	0.14 r
CLA4_1/B[0] (CLA_4bit_1)	0.00	0.14 r
CLA4_1/U14/Y (XOR2X1)	0.20	0.34 f
CLA4_1/U13/Y (AO22X1)	0.36	0.70 f
CLA4_1/U11/Y (AOI22X1)	0.22	0.92 r
CLA4_1/U7/Y (AOI21XL)	0.14	1.05 f
CLA4_1/U5/Y (AO22X1)	0.29	1.34 f
CLA4_1/C_out[3] (CLA_4bit_1)	0.00	1.34 f
CLA4_2/C_in (CLA_4bit_0)	0.00	1.34 f
CLA4_2/U13/Y (AO22X1)	0.37	1.72 f
CLA4_2/U11/Y (AOI22X1)	0.22	1.94 r
CLA4_2/U7/Y (AOI21XL)	0.17	2.10 f
CLA4_2/U5/Y (AO22X1)	0.30	2.40 f
CLA4_2/C_out[3] (CLA_4bit_0)	0.00	2.40 f
U21/Y (OR2X1)	0.20	2.60 f
C_out (out)	0.00	2.60 f
data arrival time		2.60

(Path is unconstrained)



Timing Report 中，Incr 為節點造成的延遲時間，Path 為 Path 起點到此節點的總延遲時間，可以知道 critical path 為 B[0]到 C\_out (如同 Schematic 圖)，且 delay 為 2.60 ns。

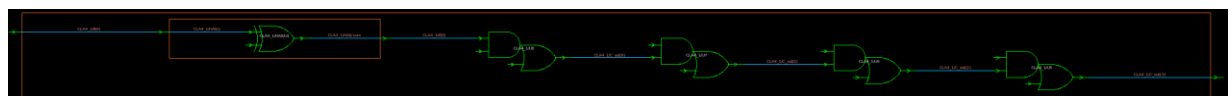
### (gate level)

Operating Conditions: slow Library: slow  
Wire Load Model Mode: top

Startpoint: B[0] (input port)  
Endpoint: C\_out (output port)  
Path Group: (none)  
Path Type: max

Point	Incr	Path
input external delay	0.00	0.00 r
B[0] (in)	0.00	0.00 r
U20/Y (XNOR2X1)	0.14	0.14 r
CLA4_1/B[0] (CLA_4bit_1)	0.00	0.14 r
CLA4_1/HA0/y (half_adder_7)	0.00	0.14 r
CLA4_1/HA0/U1/Y (XOR2X1)	0.20	0.34 f
CLA4_1/HA0/sum (half_adder_7)	0.00	0.34 f
CLA4_1/U8/Y (AO21X1)	0.28	0.62 f
CLA4_1/U7/Y (AO21X1)	0.29	0.91 f
CLA4_1/U6/Y (AO21X1)	0.29	1.20 f
CLA4_1/U5/Y (AO21X1)	0.29	1.50 f
CLA4_1/C_out[3] (CLA_4bit_1)	0.00	1.50 f
CLA4_2/C_in (CLA_4bit_0)	0.00	1.50 f
CLA4_2/U8/Y (AO21X1)	0.29	1.79 f
CLA4_2/U7/Y (AO21X1)	0.29	2.08 f
CLA4_2/U6/Y (AO21X1)	0.31	2.40 f
CLA4_2/U5/Y (AO21X1)	0.30	2.70 f
CLA4_2/C_out[3] (CLA_4bit_0)	0.00	2.70 f
U21/Y (OR2X1)	0.20	2.90 f
C_out (out)	0.00	2.90 f
data arrival time		2.90

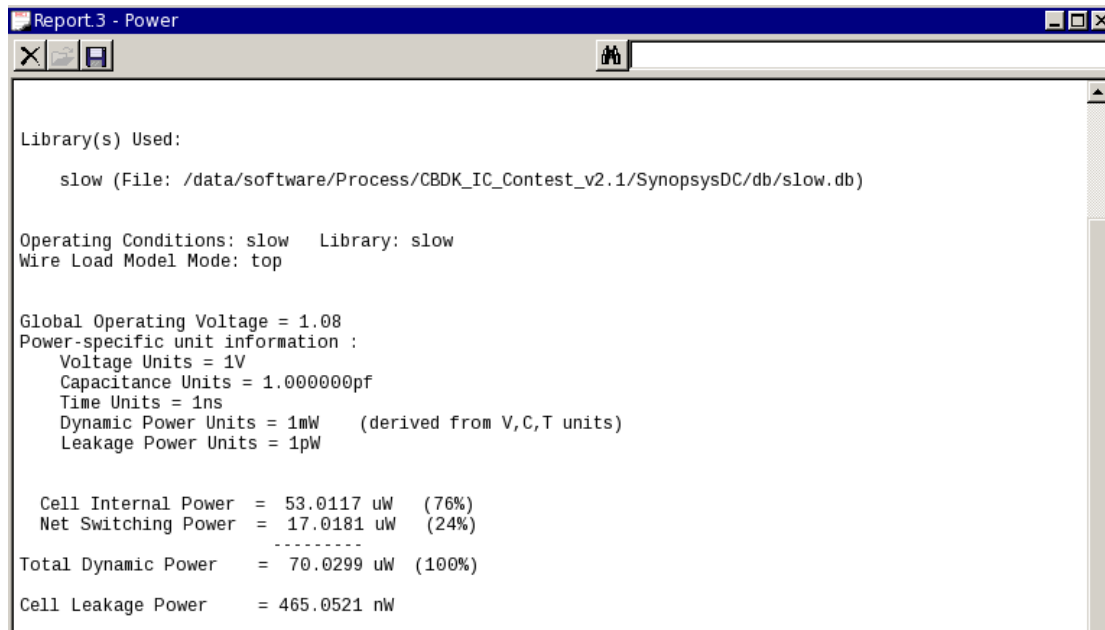
(Path is unconstrained)



可知 critical path 為 B[0]到 C\_out (如同 Schematic 圖)，且 delay 為 2.90 ns。

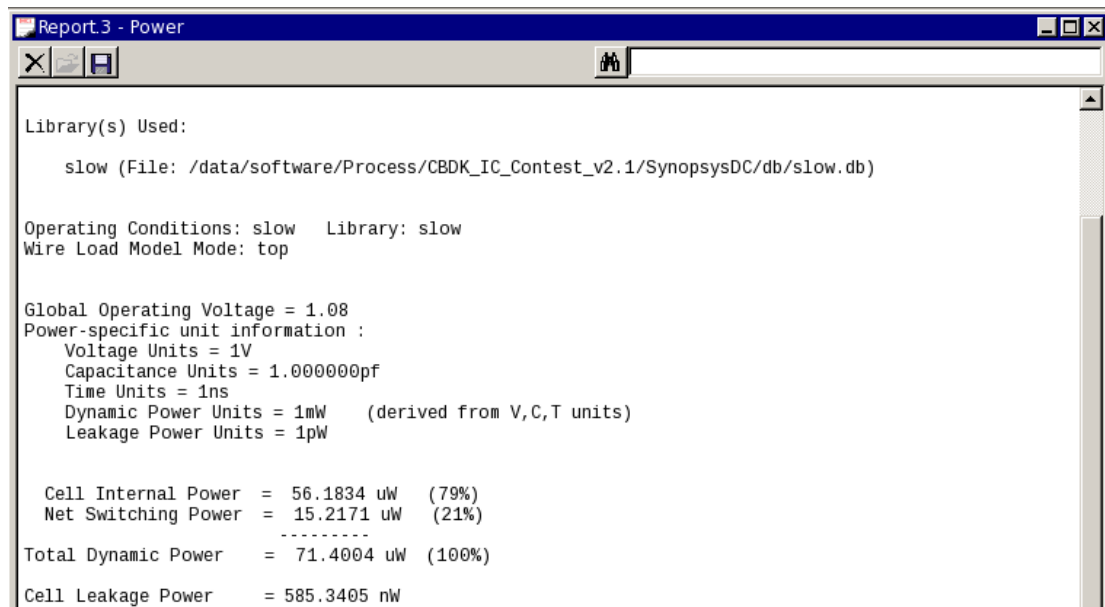
## Power consumption :

(RTL)



從 Power Report 中得知，Dynamic power 為 70.0299 uW，Static power 為 465.0521 nW。

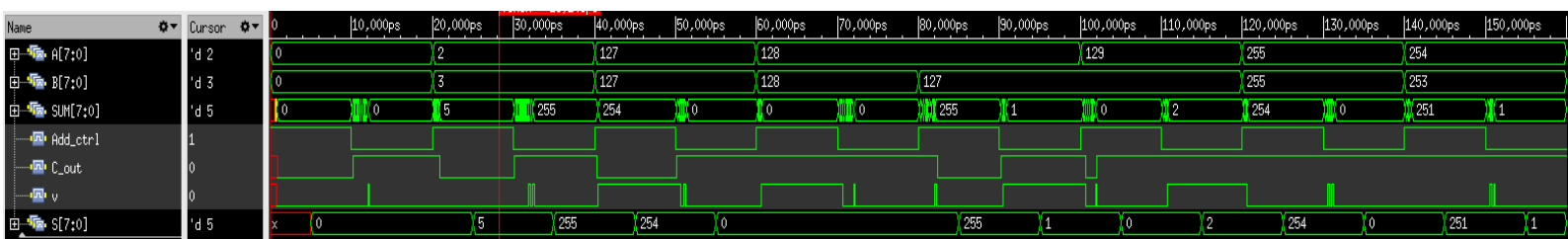
(gate level)



得知 Dynamic power 為 71.4004 uW，Static power 為 585.3405 nW。

## 結果分析：

(RTL 合成後的模擬結果)



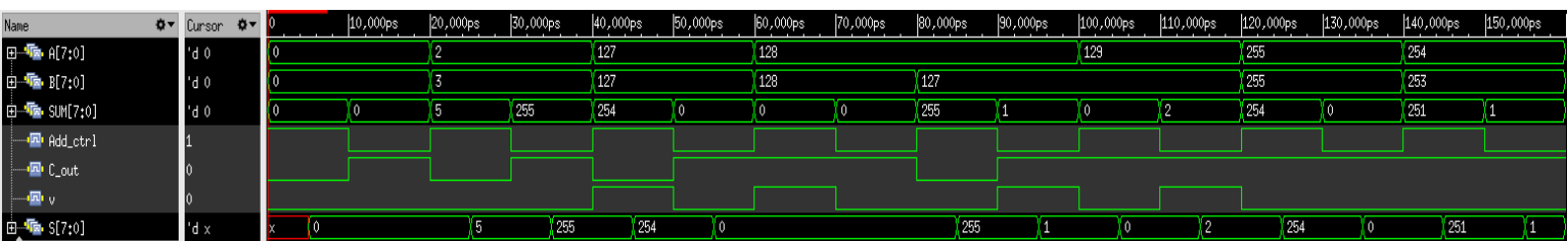
波形圖中左側的 A 與 B 均為 8-bit binary 輸入，SUM 為 8-bit 輸出，Add\_ctrl 為 1-bit 輸入選擇做加法或減法，C\_out 為 1-bit carry out 輸出，v 為 1-bit overflow 輸出，S 為 testbench 中用來檢查運算結果是否正確的變數。Add\_ctrl=1 做加法運算，Add\_ctrl=0 做減法運算。測試的資料有邊界值、正常數值，各挑選正數與負數做加法與減法，因為資料以 8-bit 表示，數值範圍是-128~127，因此做加減法後，數值過大或過小都會造成 overflow，使 v 變為 1。

```
ncsim> run
      5ns      0      +      0      =      0      (correct)
     15ns      0      -      0      =      0      (correct)
     25ns      2      +      3      =      5      (correct)
     35ns      2      -      3      =     -1      (correct)
     45ns    127      +    127      =     -2      (correct) (overflow)
     55ns    127      -    127      =      0      (correct)
     65ns   -128      +   -128      =      0      (correct) (overflow)
     75ns   -128      -   -128      =      0      (correct)
     85ns   -128      +    127      =     -1      (correct)
     95ns   -128      -    127      =      1      (correct) (overflow)
    105ns   -127      +    127      =      0      (correct)
    115ns   -127      -    127      =      2      (correct) (overflow)
    125ns     -1      +     -1      =     -2      (correct)
    135ns     -1      -     -1      =      0      (correct)
    145ns     -2      +     -3      =     -5      (correct)
    155ns     -2      -     -3      =      1      (correct)

Simulation complete via $finish(1) at time 160 NS + 0
./CLA_tb.v:158      #5 $finish;
ncsim> exit
```

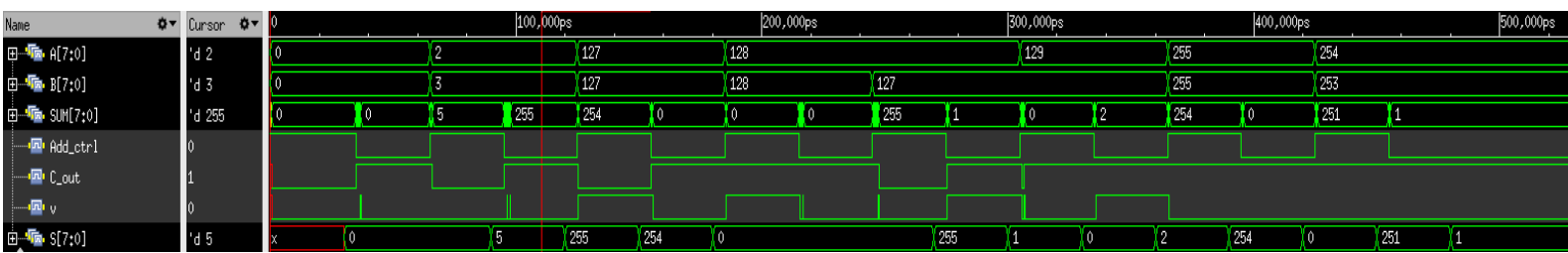
經模擬與親自驗證結果皆正確。

(RTL 合成前的模擬結果)

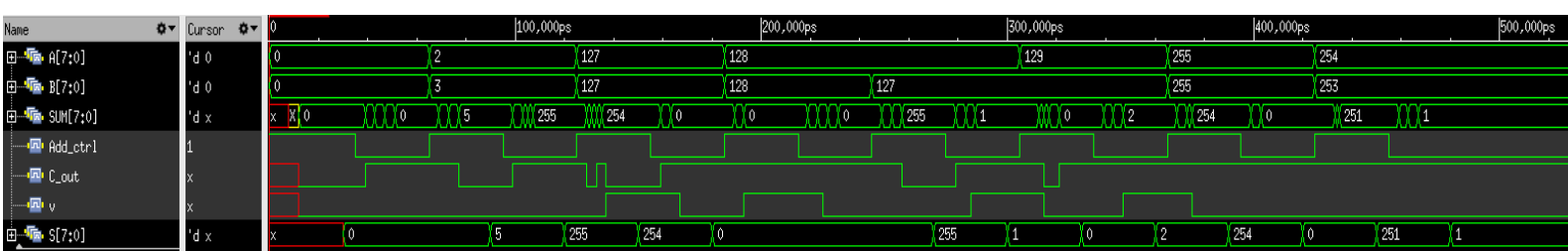


與合成前的結果相比，可發現合成後多了 delay，因為原本沒有設定 gate delay，而合成時使用了 tsmc13 製程，來模擬實際情況，因此可看到輸出結果時會有 delay。

(gate level 合成後的模擬結果)



(gate level 作業一的模擬結果)



然而因為作業一的 gate level 就有使用 gate delay，因此合成前後的波形圖差不多，不過作業一的 gate delay 是自己訂的，而這次作業的 delay 為 tsmc13 製程的 delay。相比之下，作業一的 gate delay 較久，較晚得到運算結果。