

习题课

第五次 第六次作业

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P255 3.14

DADDIU R4, R1, #800

foo: L.D F2, 0(R1) 2 stalls

MUL.D F4, F2, F0 6 stalls

L.D F6, 0(R2) 2 stalls

ADD.D F6, F4, F6 4 stalls

S.D F6, 0(R2)

DADDIU R1, R1, #8 2 stalls

DADDIU R2, R2, #8

DSLTU R3, R1, R4 2 stalls

BNEZ R3, foo 1 stall



Clock cycle	Unscheduled code		Scheduled code	
1	DADDIU	R4,R1,#800	DADDIU	R4,R1,#800
2	L.D	F2,0(R1)	L.D	F2,0(R1)
3	stall		L.D	F6,0(R2)
4	MUL.D	F4,F2,F0	MUL.D	F4,F2,F0
5	L.D	F6,0(R2)	DADDIU	R1,R1,#8
6	stall		DADDIU	R2,R2,#8
	stall		DSLTU	R3,R1,R4
	stall		stall	
	stall		stall	
7	ADD.D	F6,F4,F6	ADD.D	F6,F4,F6
8	stall		stall	
9	stall		stall	
10	stall		BNEZ	R3,foo
11	S.D	F6,0(R2)	S.D	F6,-8(R2)
12	DADDIU	R1,R1,#8		
13	DADDIU	R2,R2,#8		
14	DSLTU	R3,R1,R4		
15	stall			
16	BNEZ	R3,foo		
17	stall			

2 stalls

6 stalls

>2 stalls

4 stalls

2 stalls

2 stalls

1 stall

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Iteration	Instruction	Issues at	Executes/ Memory	Write CDB at	Comment
1	L.D F2,0(R1)	1	2	3	First issue
1	MUL.D F4,F2,F0	2	4	19	Wait for F2 Mult rs [3–4] Mult use [5–18]
1	L.D F6,0(R2)	3	4	5	Ldbuf [4]
1	ADD.D F6,F4,F6	4	20	30	Wait for F4 Add rs [5–20] Add use [21–29]
1	S.D F6,0(R2)	5	31		Wait for F6 Stbuf1 [6–31]
1	DADDIU R1,R1,#8	6	7	8	
1	DADDIU R2,R2,#8	7	8	9	
1	DSLTU R3,R1,R4	8	9	10	
1	BNEZ R3,foo	9	11		Wait for R3
2	L.D F2,0(R1)	10	12	13	Wait for BNEZ Ldbuf [11–12]
2	MUL.D F4,F2,F0	11	44 19	34	Wait for F2 Mult busy Mult rs [12–19] Mult use [20–33]
2	L.D F6,0(R2)	12	13	14	Ldbuf [13]
2	ADD.D F6,F4,F6	13	35	45	Wait for F4 Add rs [14–35] Add use [36–44]
2	S.D F6,0(R2)	14	46		Wait for F6 Stbuf [15–46]
2	DADDIU R1,R1,#8	15	16	17	
2	DADDIU R2,R2,#8	16	17	18	
2	DSLTU R3,R1,R4	17	18	20	
2	BNEZ R3,foo	18	20		Wait for R3
3	L.D F2,0(R1)	19	21	22	Wait for BNEZ Ldbuf [20–21]
3	MUL.D F4,F2,F0	20	23 34	49	Wait for F2 Mult busy

					Mult rs [21–34] Mult use [35–48]
3	L.D F6,0(R2)	21	22	23	Ldbuf [22]
3	ADD.D F6,F4,F6	22	50	60	Wait for F4 Add rs [23–49] Add use [51–59]

3	S.D F6,0(R2)	23	55		Wait for F6 Stbuf [24–55]
3	DADDIU R1,R1,#8	24	25	26	
3	DADDIU R2,R2,#8	25	26	27	
3	DSL TU R3,R1,R4	26	27	28	
3	BNEZ R3,foo	27	29		Wait for R3



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a. 对于非条件分支指令，其下一条指令直接存储在BTB中，因此省去了通过地址取指令的过程，因此节省了1 cycle

b. 考虑如下指令

```
    jmp L1
```

```
    ...
```

```
L: mov r1, r0
```

在对应5% unconditional branch, 90% hit rate, 2 cycles penalty for a buffer miss中，其性能提升为：



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$$5\% * (90\% * (-1) + 10\% * 2) = -0.035$$

为了使得BTB帮助机器获得性能提升，即：buffer中存储的指令所带来的收益要比因buffer miss所带来的penalty要大，设hit rate = x ,那么：

$$x * (-1) + (1-x) * 2 < 0$$

$$\text{解得： } x > 2/3 = 66.7\%$$

