

# State Diagram

Lab 4 Report  
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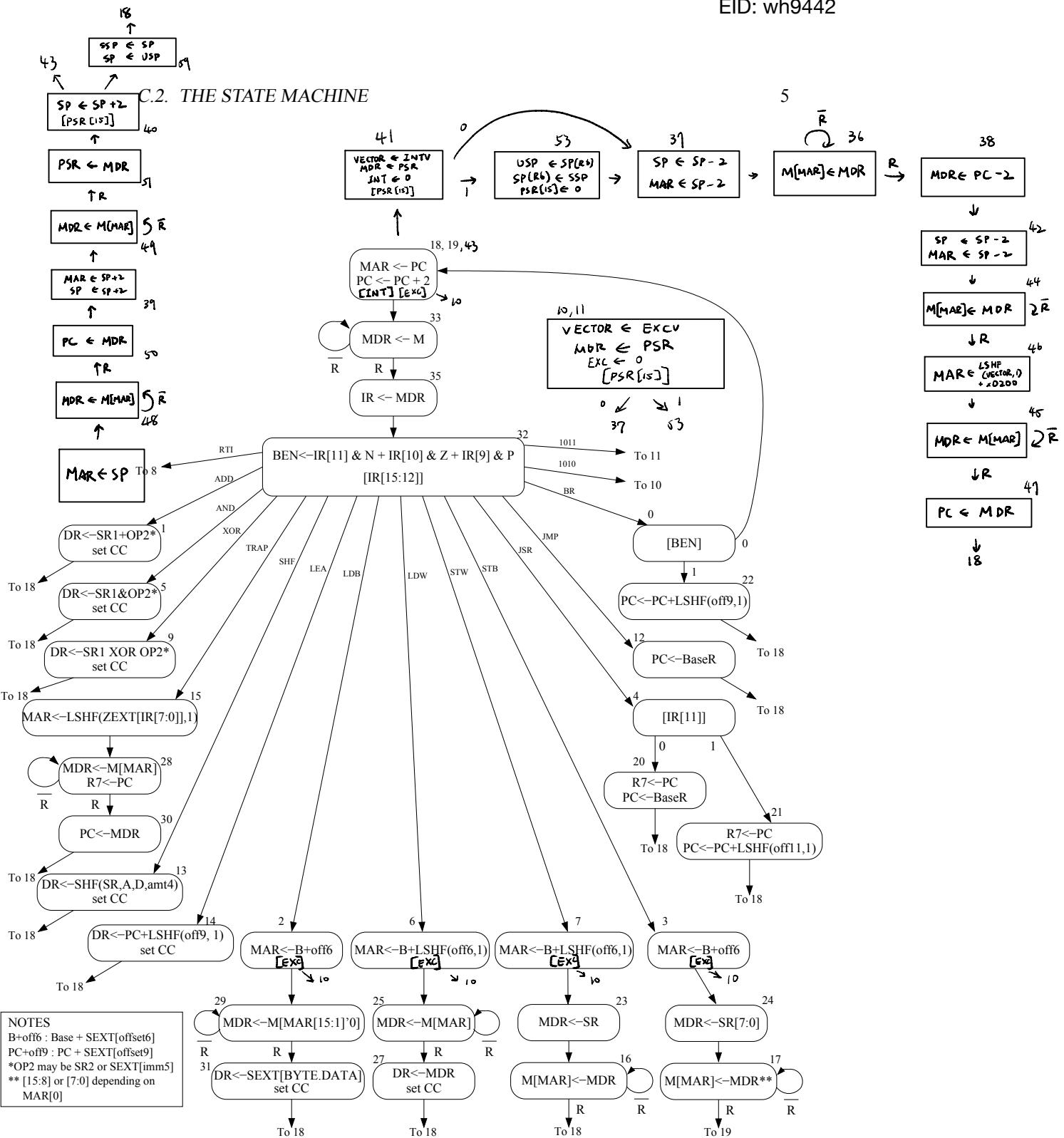


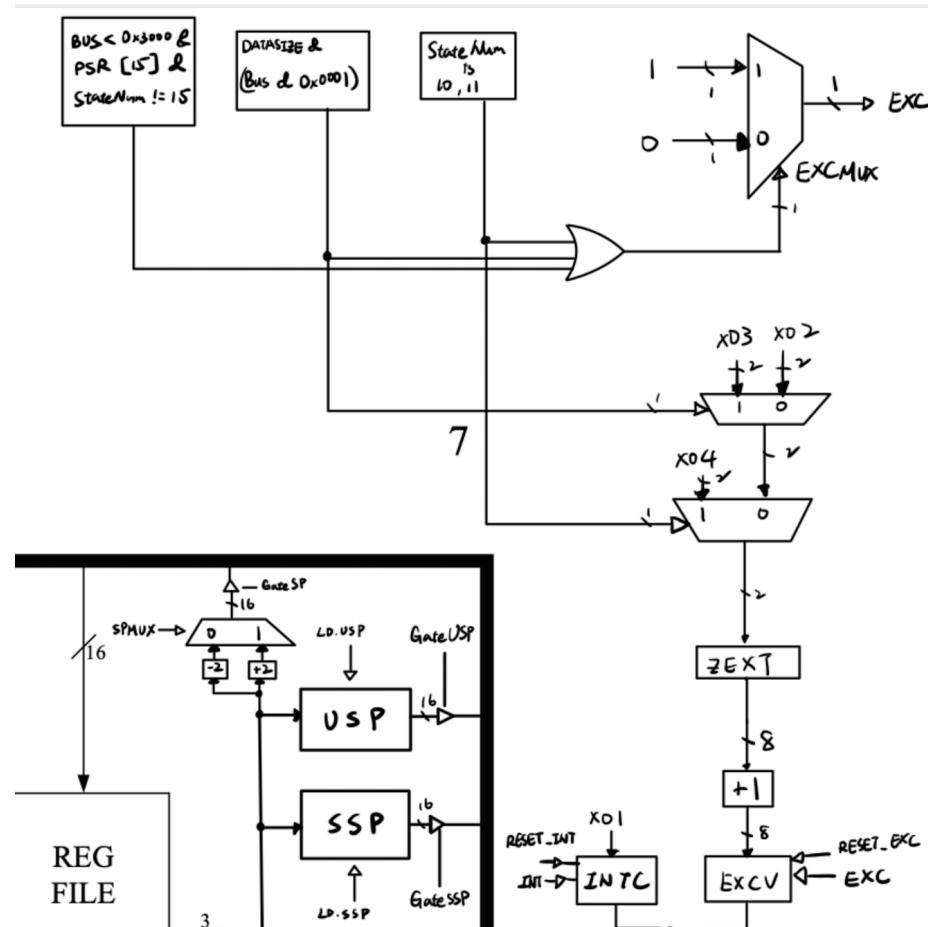
Figure C.2: A state machine for the LC-3b

## Interrupt/Exception State Description

In state 18/19/43, the interrupt signal is checked. If INT is 1, the state diagram will go to state 41. Also, the exception signal is checked. If EXC is 1, the state diagram will go to state 10.

Next, the VECTOR register will be loaded as the value in INTV. Since we only have 1 interrupt handler here, the INTV will always be x01. Also, in state 41, MDR will store the current PSR and reset the INT to 0 to accept nested interrupts. Here, PSR[15] will decide the next state. If PSR[15] is set to high, we need to set the machine into privilege mode. Hence, the next state would be state 53 and do context switching to switch the stack pointer to supervisor stack pointer. In contrast, if PSR[15] is set to zero, which means that we are already in the supervisor mode, we don't need to switch to supervisor again. The next state would be 37.

The logic is quite similar to exception handling block - state 10/11. The VECTOR register will be loaded as the value in EXCV. The value of EXCV will be determined by the logic below. And do the same logic in state 41 to store PSR to MDR and reset EXC.



In state 37, we will get the stack pointer and load into MAR for storing PC and PSR. In state 36, 38, 42, 44 are all the states to load PC and PSR into supervisor stack pointer. Next, in state 46, we load the address of the exception/interrupt entry handler by left-shifting the VECTOR 1 and plus x2000 to MAR. Next state, 45, 47, we read the stored exception/interrupt handler address to the PC to start executing the exception/interrupt handler.

## **RTI**

The RTI instruction is to switch back to the last state before executing an exception or interrupt. In the states 8, 48, 50, 38, 48, 51, 40, we get the PC, PSR, SP value back. Later, in state 40, we will check the restored PSR[15] to determine whether we are still in the nested interrupt/exception. If PSR[15] is set to 0, we will go to state 43, which is state 18 to keep executing the nested interrupt/exception. If PSR[15] is set to 1, we need to do context switching back by switching the stack pointer.

## **Datapath Change**

### **SSP/USP/SPMUX**

Add two 16-bit register SSP/USP to store value for user stack pointer value and supervisor stack pointer. Each register has a LD and a Gate signal to load value from SR1 and release the value to the BUS. For the SPMUX, the SPMUX signal will generate the result of SR1+2/SR1-2 with a Gate signal.

### **DRMUX/SR1MUX**

To allow the calculation of stack pointer (R6), we increase DRMUX/SR1MUX control signal from 1-bit to 2-bits.

### **GateOldPC**

I add a Gate signal to release PC-2 to the BUS for the state 38.

### **PSR**

Add PSR[15], PSR[14:3] to support PSR in the data path. Use LD.PSR to load BUS data into the PSR. Use LD.USP to control the value of PSR[15] of supervisor mode/user mode. Also, since we reuse the CC-bits, we need to add a MUX to determine the input data is from original logic or BUS data.

### **EXCV/INTV/VECTOR**

We add three blocks to check three exceptions and use a logic gate to generate the EXC signal and load to the EXCV register. I use EXC signal to determine the VECTOR data source. Use GateVector to release the VECTOR data to BUS. Also, add a signal of RESET\_INT and RESET/EXC to support nested interrupt/exception.

## **Microsequencer Change**

EXC & INT & PSR[15] is loaded to the microsequencer to determine the next state.

In this microsequencer, I add a new MUX to use less state number. If the EXC is set, we will get the next state number to 10. If we need to determine the state by PSR[15], we use bit 4. If we need to determine the state by INT, we use bit 4. Also add the COND from 2 bits to 3 bits to support this.

# Data Path

## C.4. THE CONTROL STRUCTURE

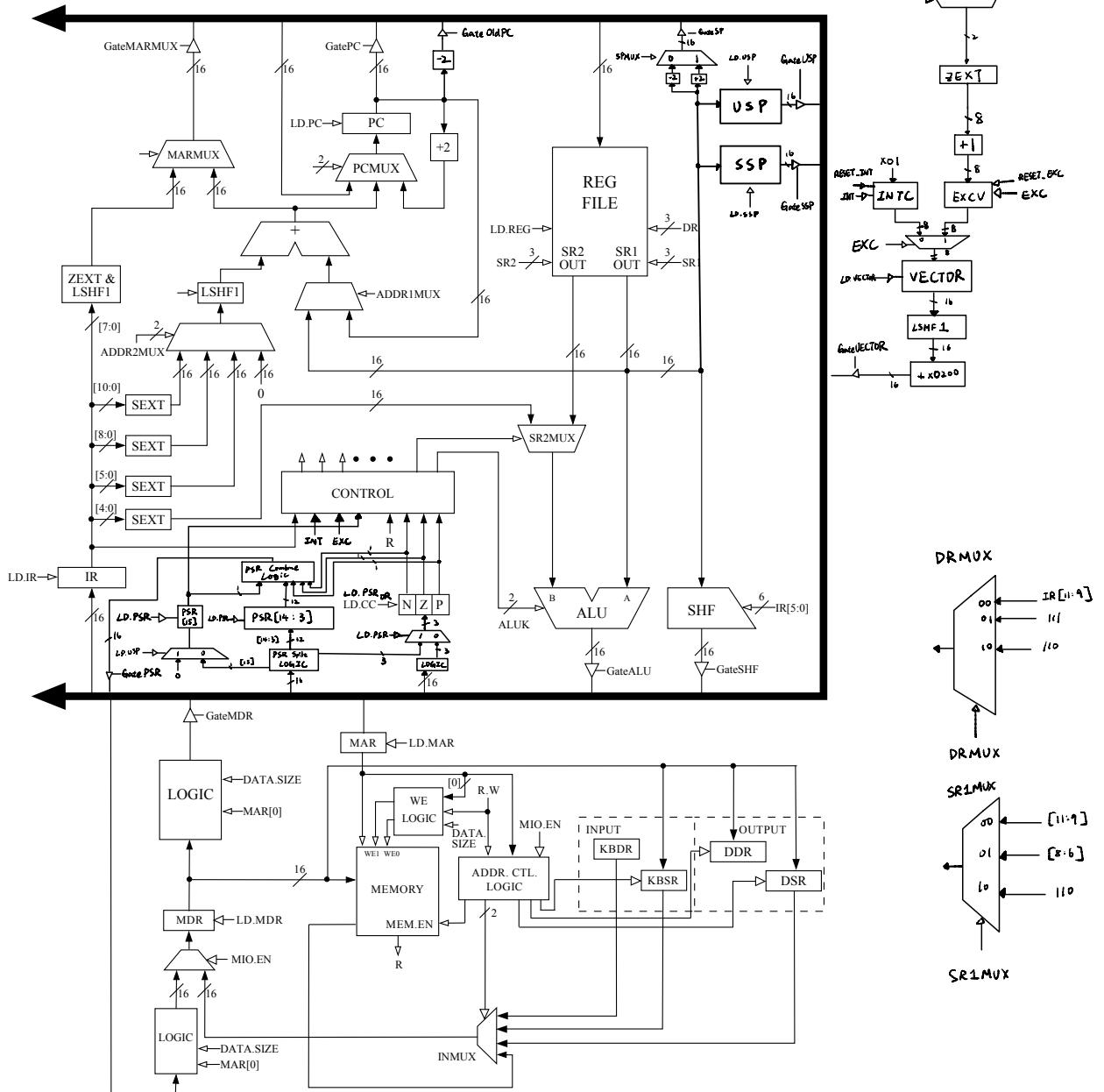


Figure C.3: The LC-3b data path

provide you with the additional flexibility of more states, so we have selected a control store consisting of  $2^6$  locations.

# Modified Control Signal

## COND/2

- [011] - IR [11]
- [001] - R
- [010] - BEN
- [101] - INT
- [110] - PSR [15]

## DRMUX/2

- [00] - IR [11:9]
- [01] - 111
- [10] - 110

## SR1MUX/2

- [00] - IR [11:9]
- [01] - IR [8:6]
- [10] - 110

<b>LD.PSR/1</b>	NO, LOAD
<b>LD.USP/1</b>	NO, LOAD
<b>LD.SSP/1</b>	NO, LOAD
<b>LD.VECTOR/1</b>	NO, LOAD

<b>GatePSR/1</b>	NO, YES
<b>GateUSP/1</b>	NO, YES
<b>GateSSP/1</b>	NO, YES
<b>GateSP/1</b>	NO, YES
<b>GateVector</b>	NO, YES

## SPMUX/1

- [0] - SR1-2
- [1] - SR1+2

## RESET\_INT/1

- [0] - Reset INT Register

## RESET\_EXC/1

- [0] - Reset INT Register

# Microsequencer

## 10 APPENDIX C. THE MICROARCHITECTURE OF THE LC-3B, BASIC MACHINE

