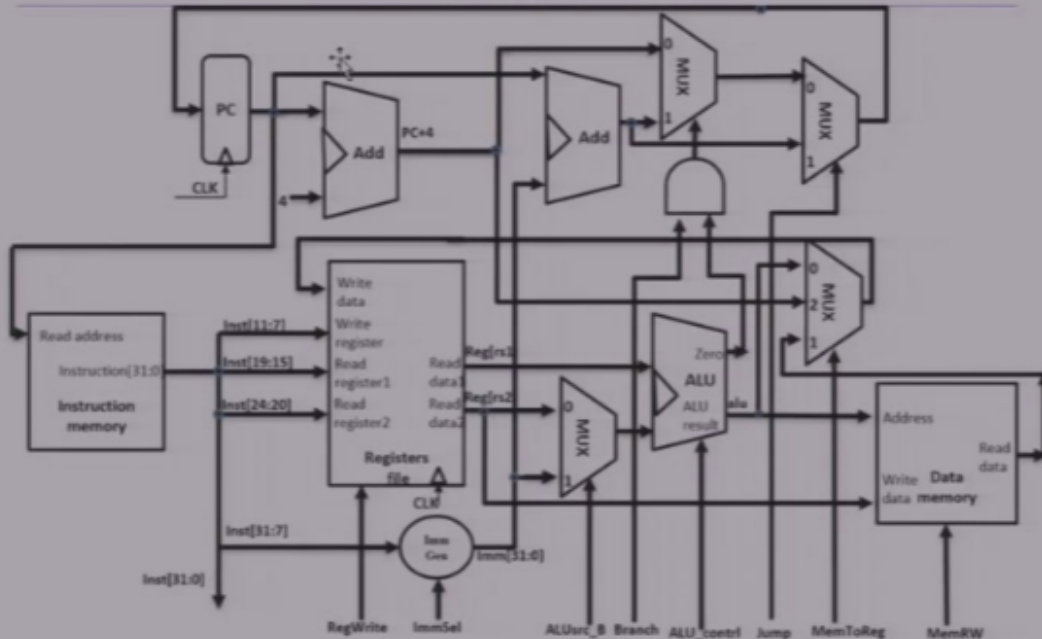


5. (20%) Examine the difficulty of adding a proposed `ss rs2, rs1, imm` (Store Sum) instruction to RISC-V.
 Interpretation: `Mem[Reg[rs2]] = Reg[rs1] + immediate`

Picture 1



1) (3%) Which new functional blocks (if any) do we need for this instruction?

some additional muxes

2) (2%) Which existing functional blocks (if any) require modification?

No functional blocks need to be modified

4.2 (20%) Implement the following C code in RISC-V assembly. Hint: Remember that the stack pointer must remain aligned on a multiple of 16:

```
int fun(int i){
    if (i==0)
        return 0;
    else if (i == 1)
        return 1;
    else
        return fun(i-1) + fun(i-2);
}
```

4.1 (10%) Assume the following register contents:

`t0 = 0x1234567812345678` `t6 = 0x0000000AAAAAAAAA`

For the register values shown above, what is the value of `s2` for the following sequence of instructions?

`Slli s1, t6, 0x4`

`Srai s2, t0, 0x8`

`xor s1, s1, t0`

`or s2, s2, s1`

`s1 = 0x123456D2B89EFCDE`

`s2 = 0x123676D6F89EFCDE`

3. (15%) To convert the pseudoinstruction(left) into the shortest sequence of RISCV instructions.

<u>Pseudoinstruction</u>	<u>Function</u>	<u>RISCV instructions</u>
<u>Bnez rs, Lable</u>	if (<u>rs</u> !=0) goto <u>Lable</u>	<u>bne rs,x0,L</u>
<u>J Lable</u>	goto <u>Lable</u>	<u>jal x0,Lable;</u> <u>/beq x0,x0,lable</u>
<u>Mv rd, rs</u>	<u>rd = rs</u> copy the register	<u>addi rd,rs,0;</u> <u>/or rd,rs,x0</u> <u>/add rd rs x0</u>
<u>Not rd,rs</u>	<u>rd = ~rs</u>	<u>xori rd,rs,-1;</u>
<u>Snez rd,rs</u>	<u>Rd = (rs!=0)?1:0</u>	<u>Sltu rd,x0.rs</u>

2. (15%) Assemble: To convert the RISCV instructions into machine code.

<u>Address (Hex)</u>	<u>RISCV Assembly Instruction</u>	<u>Machine Code (Hex)</u>
200000	Loop: <u>jal x0, L1</u>	<u>0x0700006F</u>

200004	<u>add s2, s3, s4</u>	<u>0x01498933</u>
200008	<u>beq t3, t4, Loop</u>	<u>0xFFDE0CE3</u>
.....		--
200070	<u>L1:</u>	--

1.2(8%) A and B are the floating-point number with IEEE754 single precision. Write down the Binary representation of c.

A=C20E6666

B=25.1 C=A+B

A = C20E6666 = (-1)¹ * (1+0.1125) * 2⁽¹³²⁻¹²⁷⁾ = -35.6

31	30	23	22	0
1	0000100		0	0011 1001 1001 1001 10		

B = 25.1

C = -10.5 = C1280000 = (-1)¹ * (1+0.3125) * 2⁽¹³⁰⁻¹²⁷⁾

31	30	23	22	0
1	0000010		0	1010 0000 0000 0000 00		

1.1(12%) The data have no inherent meaning. Given the pattern:

(04 C0 00 6F)₁₆

What does it represent, assuming that it is:

1) a two's complement integer	04C0006F
2) signed and magnitude integer	04C0
3) A IEEE754 single precision floating-point number	$2^{-118} \times (1.100\ 0000\ 0000\ 0000\ 0110\ 1111)_2 =$
4) A RISC-V instruction	Jal x0,76 or jal x0,0x4c

1.2(8%) A and B are the floating-point number with IEEE754 single precision. Write down the Binary representation of c.

A=C20E6666

B=25.1 C=A+B

A = C20E6666 = $(-1)^1 * (1+0.1125) * 2^{(132-127)} = -35.6$

31	30	23	22	0
1	0000100	0	0011 1001 1001 1001 10	

B = 25.1

C = -10.5 = C1280000 = $(-1)^1 * (1+0.3125) * 2^{(130-127)}$

31	30	23	22	0
1	0000010	0	1010 0000 0000 0000 00	