选择题

I.   Please choose the best answer and fill it into following table.

1	2	3	4	5	6	7	8	9	10
B	A	B	C	A	A	A	B	D	C

11
A

Chapter 4

1. Pipeline CPU Design .....

答案：(1). 0, 0, 0, 1, 0

答案：(2).

sub x5, x7, x11
 nop
 nop
 ld   x13, 8(x5)
 ld   x7, 4(x2)
 nop
 add   x13, x5, x13
 nop
 nop
 sd   x13, 0(x5)

答案：(3).

 sub x5, x7, x11
 ld   x13, 8(x5)
 ld   x7, 4(x2)
 add   x13, x5, x13
 sd   x13, 0(x5)

答案：(4).

cycle	ForwardA	ForwardB	
1	X (don't care)	X (don't care)	No instruction in EX

			stage yet
2	X	X	
3	0	0	
4	2	0	
5	0	0	
6	0	1	
7	0	2	

Chapter 5

1．书后5.1 In this exercise we look at memory locality properties of。。。

【答案】：1）2
2）ABC
3）E

2．书后5.2 Caches are important to providing a high-performance。。

【答案】．
1）

Word Address	Binary Address	Tag	Index	Hit/Miss
0x03	0000 0011	0	3	M
0xb4	1011 0100	b	4	M
0x2b	0010 1011	2	b	M
0x02	0000 0010	0	2	M
0xbf	1011 1111	b	f	M
0x58	0101 1000	5	8	M
0xbe	1011 1110	b	e	M
0x0e	0000 1110	0	e	M
0xb5	1011 0101	b	5	M
0x2c	0010 1100	2	c	M
0xba	1011 1010	b	a	M
0xfd	1111 1101	f	d	M

2)

Word Address	Binary Address	Tag	Index	Offset	Hit/Miss
0x03	0000 0011	0	1	1	M
0xb4	1011 0100	b	2	0	M
0x2b	0010 1011	2	5	1	M
0x02	0000 0010	0	1	0	H
0xbf	1011 1111	b	7	1	M
0x58	0101 1000	5	4	0	M
0xbe	1011 1110	b	6	0	H
0x0e	0000 1110	0	7	0	M
0xb5	1011 0101	b	2	1	H
0x2c	0010 1100	2	6	0	M
0xba	1011 1010	b	5	0	M
0xfd	1111 1101	f	6	1	M

3．书后5.5 For a direct-mapped cache design with a 64-bit address。。。。

【答案】：1）4（错），改成8，即使在RV64I(即寄存器64位的指令集)中，每个word也是4个字节
2）32
3）1.21

4．Cache system 。。。。
答案：
(1)

Address	00	16	48	08	56	16	08	56	32	00	60
Read/write	r	r	r	r	r	r	r	w	w	r	r
Line#	0	2	2	1	3	2	1	3	0	0	3
Tag	0	0	1	0	1	0	0	1	1	0	1
Hit/miss	m	m	m	m	m	m	h	h	m	h	h

答案：(2).

Address	064	032	064	000	112	064	128	048	240	000
Read/write	r	r	r	r	w	w	r	r	r	w
Set #	0	2	0	0	3	0	0	3	3	0
Tag	1	0	1	0	1	1	2	0	3	0
Hit/miss	m	m	h	m	m	h	m	m	m	m
Dirty-set					1	1				1

Please write down the dirty block number <u>7, 4, 0</u> .（2分）

5. **Consider a virtual memory system with the following properties:**

答案：

（1） $2^{26}*(4+22)$ 占用：$2^{26}*32$

（2） TLB can hold 64*16KB =1M <8M

Increase the page size to 128KB