Weidong Ye

weidongye.com | (480) 678-0155 | wye5@illinois.edu
United States Citizen

OBJECTIVE

I am a MS ECE graduate with extensive industry and research experience looking for a great start to my career!

EDUCATION

MS in Electrical & Computer Engineering May 2017
University of Illinois at Urbana-Champaign

- Major GPA: 4.0; Cumulative GPA: 3.8
- Thesis: *Determining Application-specific Peak Power and Energy Requirements for Ultra-low-power Processors*

BSE in Electrical Engineering May 2015
Arizona State University

- Major GPA: 4.0; Cumulative GPA: 4.0

PUBLICATION

- H. Cherupalli*, H. Duwe*, **W. Ye***, R. Kumar and J. Sartori, "Software-based Gate-level Information Flow Security for IoT Systems", In the *50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO),* Boston, Massachusetts, USA, October 2017
- H. Cherupalli*, H. Duwe*(presenter), **W. Ye***, R. Kumar and J. Sartori, "Bespoke Processors for Applications with Ultra-low Area and Power Constraints", In the *44th ACM/IEEE International Symposium on Computer Architecture (ISCA),* Toronto, Ontario, Canada, June 2017
- H. Cherupalli*, H. Duwe*, **W. Ye*(presenter)**, R. Kumar and J. Sartori, "Determining Application-specific Peak Power and Energy Requirements for Ultra-low-power Processors", In the *22nd International Conference on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), Xi'An, ShaanXi, China, April 2017 [**Best Paper Award**]
- H. Cherupalli*(presenter), H. Duwe*, **W. Ye***, R. Kumar and J. Sartori, "Enabling Effective Module-oblivious Power Gating for Embedded Processors", In the *23rd Symposium on High Performance Computer Architecture* (HPCA), Austin, Texas, USA, February 2017
- H. E. Chung, **W. Ye**, S. G. Vora, S. Rednour and D. R. Allee, "A Passive Very Low-Frequency (VLF) Electric Field Imager", in *IEEE Sensors Journal*, vol. 16, no. 9, pp. 3181-3187, May 1, 2016.

* indicates equal contribution

EXPERIENCE

Graduate Research Assistant August 2015 - May 2017
PASSAT Research Group — Advisor: Professor Rakesh Kumar — Urbana, IL

- Performed research and co-authored papers published at all four of the top-tier computer architecture conferences in 2017, including a best paper award at ASPLOS

Architecture Research Intern May 2016 - August 2016
NVIDIA Research — Manager: Dr. Steve Keckler — Westford, MA

- Built a memory access pattern profiler using NVIDIA's SASSI (binary instrumentation) framework
- Architected new memory instructions to improve DRAM row buffer hit rate, performance, and energy efficiency

Embedded Systems Engineer Intern January 2014 - July 2015
Intel Corporation — IOTG PED Performance Measurement and Analysis Team — Chandler, AZ

- Developed OpenCL microbenchmarks to demosntrate GPU pipeline latency, thread dispatch rate, and branching penalty of SIMD operations on Intel GPU EUs
- Built Yocto Linux image to boot Intel's pre-production SoC platform
- Automated software tools to run Heterogenous Compute Index(Intel's internal benchmark) for quick data collection on Intel's processors
- Identified system IO bottlenecks using 10 and 40 Gb/s optical fiber NICs with Intel DPDK (Data Plane Development Kit: A set of libraries and drivers for fast packet processing on Intel x86)
- Delivered performance reports for 5+ iterations of pre-production firmware for Intel's 40 Gb/s NICs
- Brought up Intel's Skylake systems for EFI boot and early silicon performance testing
- Designed methods and developed scripts to automate video transcoding performance and quality metrics on Intel Media SDK and Intel Iris Pro Graphics
- Communicated and collaborated with software development team in Beijing, China in Mandarin Chinese to expedite the integration and troubleshoot of software tools

US Army Research Lab Contract Researcher August 2014 - May 2015
ASU Flexible Display Center — Army Research Lab Electric Field Imaging Research Contract — Chandler, AZ

- Designed and manufactured 2D electric field imaging arrays on flexible and hard PCB substrate
- Automated data acquisition to speed up experiments 10X
- Published findings in *IEEE Sensors Journal*

EXPERIENCE CONTINUED

DRAM Product Engineering Intern May 2013 - August 2013

Micron Technology — Silicon Alignment Group — Boise, ID

- Delivered results for full chip and base-standard supply sweeps across multiple designs using Hspice
- Reported early silicon bugs measured in die level and packaged products using μmate3 and Advantest t5501
- Developed scripts to automatically pull and plot volume production characterization data

Summer Undergraduate Research Fellowship May 2012 - August 2012

National Institute of Standards and Technology (NIST) — Electromagnetics Division — Boulder, CO

- Developed test methods to establish a standardized system to analyze RF personal alert safety systems for firefighters using anechoic and reverberation chambers
- Designed and implemented a MATLAB program suite to automate a spectrum analyzer, vector network analyzer, and reverberation chamber motor to optimize RF measurement & data acquisition process

ACADEMIC PROJECT

Senior Design Project & Honors Thesis December 2014

Electric Field Monitoring of Power Lines on UAVs — Faculty Mentor: Professor David Allee

- Designed and built D-dot sensor and 60Hz lock-in amplifier to sense electric field of power lines
- Custom built UAV capable of lifting payload and GPS auto-pilot
- Won Senior Design prize for having best project in class

HONORS AND AWARDS

President Barack Obama Scholarship (2011-2014) - Offered to students with families financially underprivileged. Obama Scholars received one-on-one guidance by a faculty in their field of study

Ira A. Fulton College of Engineering Alumni Association Scholarship (2012-2013) - Scholarship presented to two Engineering students by the Ira A. Fulton College of Engineering Alumni Association

Gary & Diane Tooker Engineering Scholarship (2012-2013) - Gary Tooker (former CEO of Motorola) and his wife's generously awarded this scholarship to the top five Electrical Engineering students at ASU

Joseph and Sandy Palais Senior Design Prize (2014) - This award is presented by a panel of judges to the best electrical engineering senior design team project of 17 senior design teams

IEEE Region 6 Poster Competition (2015) - Won 3rd place for presenting at San Diego State University

NSF Graduate Research Fellowship Honorable Mention (2016) - The NSF accords Honorable Mention to meritorious applicants who do not receive Fellowship awards. This is considered a significant national academic achievement

ASPLOS Best Paper Award (2017) Among the 56 accepted papers, with 17% acceptance rate, our paper was selected as one of the two best papers at ASPLOS 2017

LEADERSHIP EXPERIENCE

ECE Student Advancement Committee 2016-2017

Graduate Committee Member — Urbana-Champaign, IL

- Work with ECE Illinois's faculty & staff to improve student life
- Improve grad student recruitment process to encourage higher matriculation rate diverse and all students

IEEE-Eta Kappa Nu (HKN) 2012-2015

VP & Treasurer — Epsilon Beta Chapter — Tempe, AZ

- Honors society for IEEE-allied fields
- Organized events where members can network and find employment opportunities with corporate sponsors

VOLUNTEER & OUTREACH EXPERIENCE

Intel Involved (2014) - Promoted STEM education at a local Boys & Girls Club. Taught 6th graders how to program in Arduino using an Intel Galileo development platform

E2 Camp Mentor (2014) - Served as cabin leader for incoming freshmen at ASU Engineering School's E2 Camp. Taught incoming students soft skills required to succeed

Night of the Open Door (2015) - Demoed engineering projects and technologies to adults and kids from the general public to generate interest in STEM

ECEE Deparment Student Mentor (2015) - Talked on panels and mentored high school and undergraduate students to encourage undergraduate research