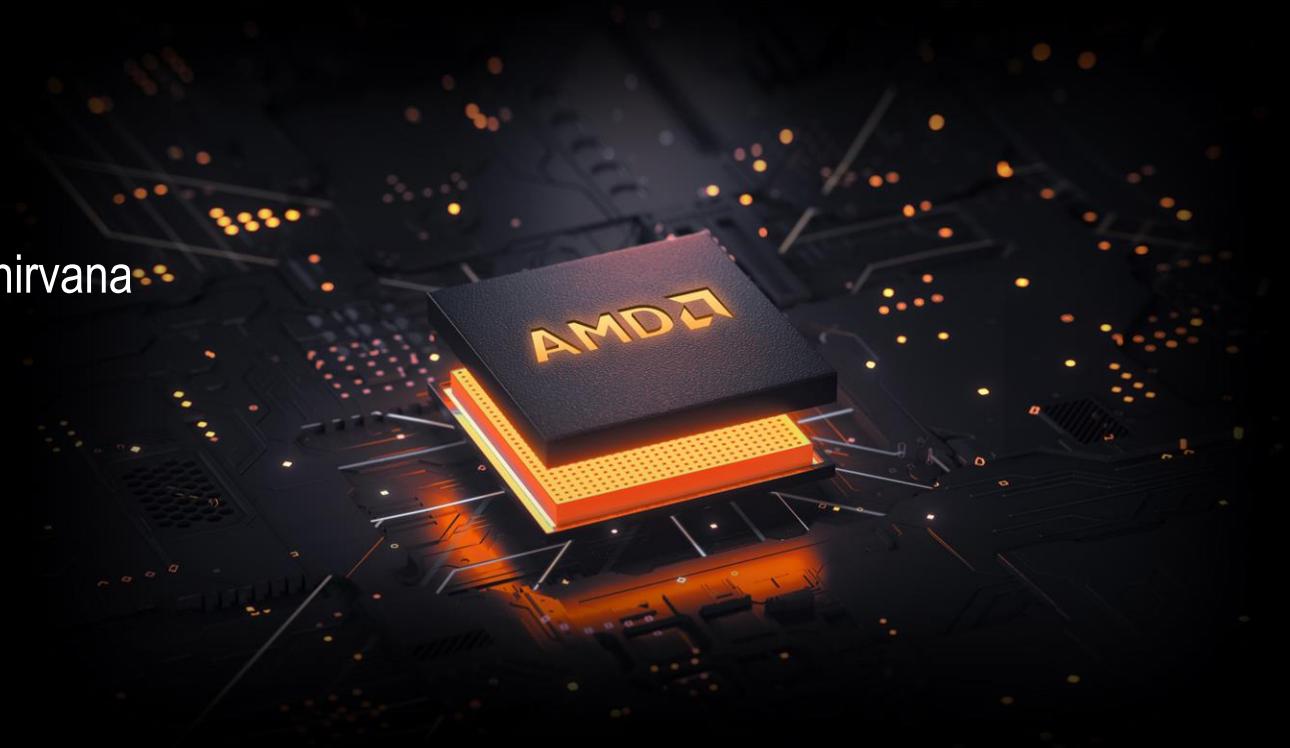
Chiplet Ecosystem

Challenges and obstacles to overcome to reach chiplet nirvana



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Advanced Micro Devices

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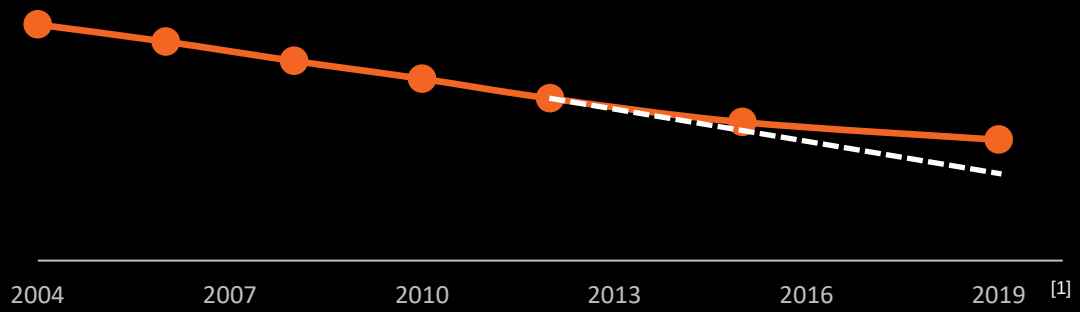
AMD

Outline

- Why chiplets?
- Chiplet ecosystem
  - Principles
  - Challenges
  - Enablement
- UCIe - Chiplet application
- Summary

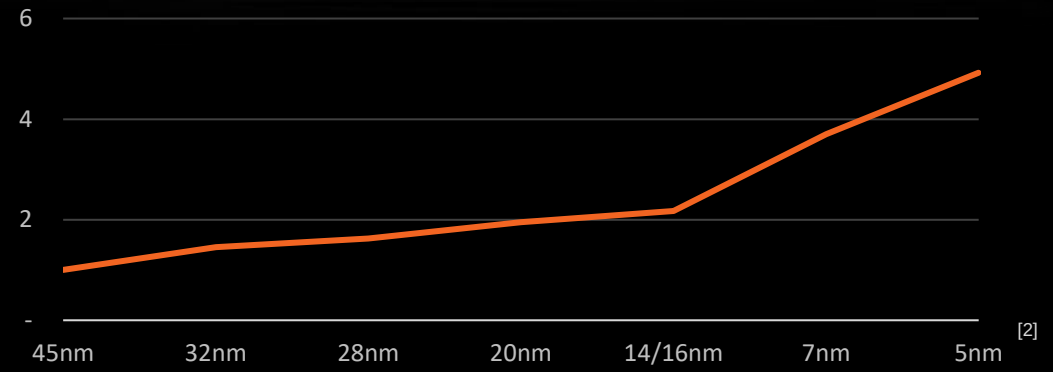
Why Chiplets?

Slowing of Moore's Law



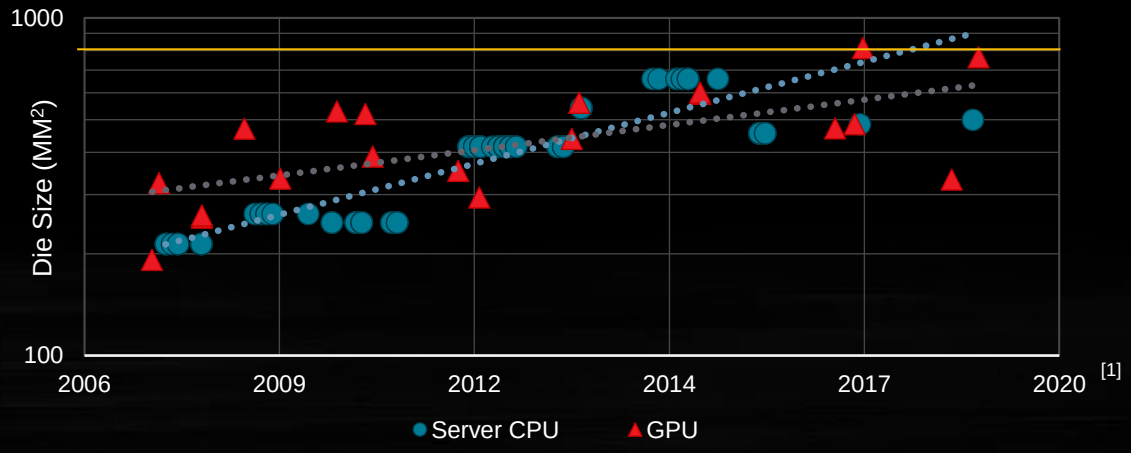
[1]

Increasing Cost



[2]

Reticle Limit



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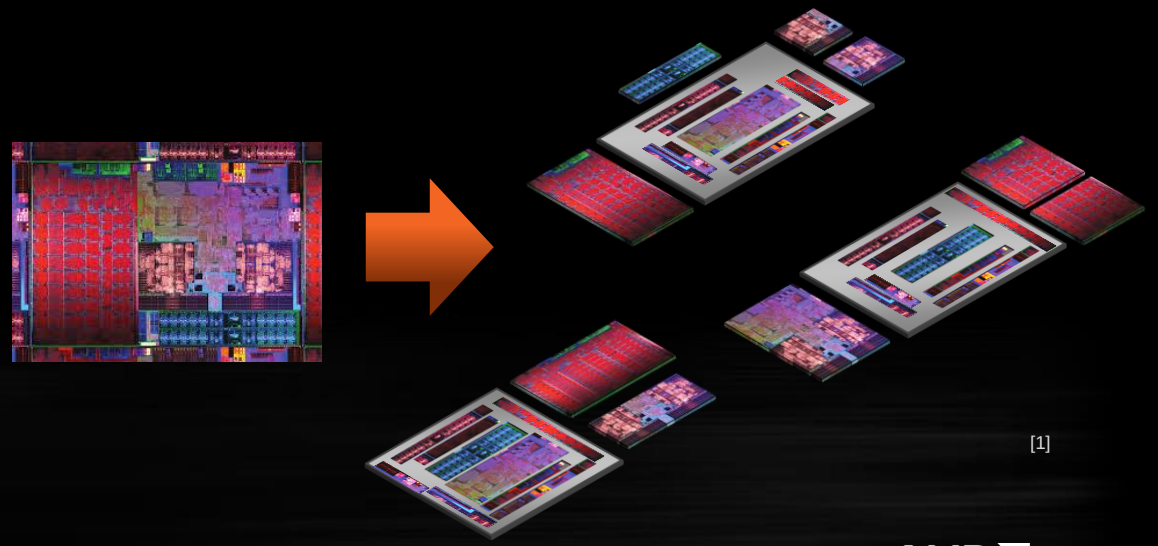
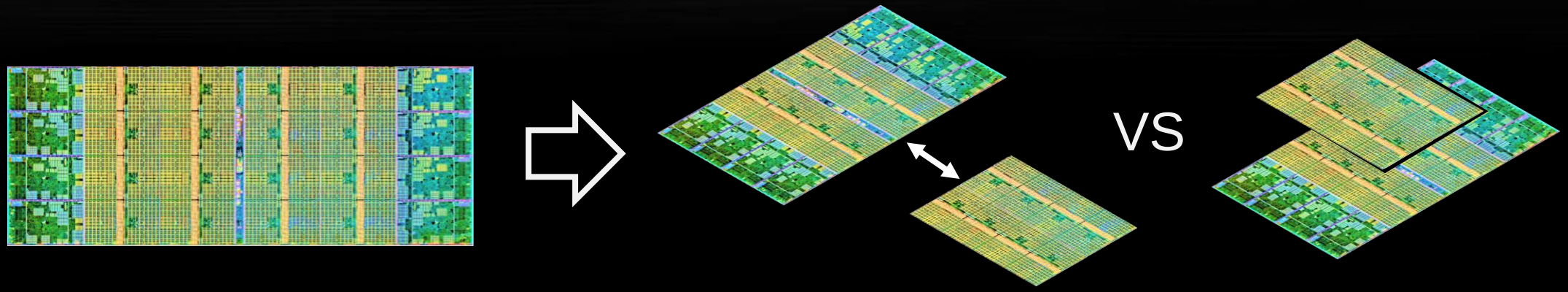


[1]

[1] Naffziger, VLSI Short Course, 2020, [2] Cost per yielded mm² for a 250mm² die

Choices Beyond Monolithic



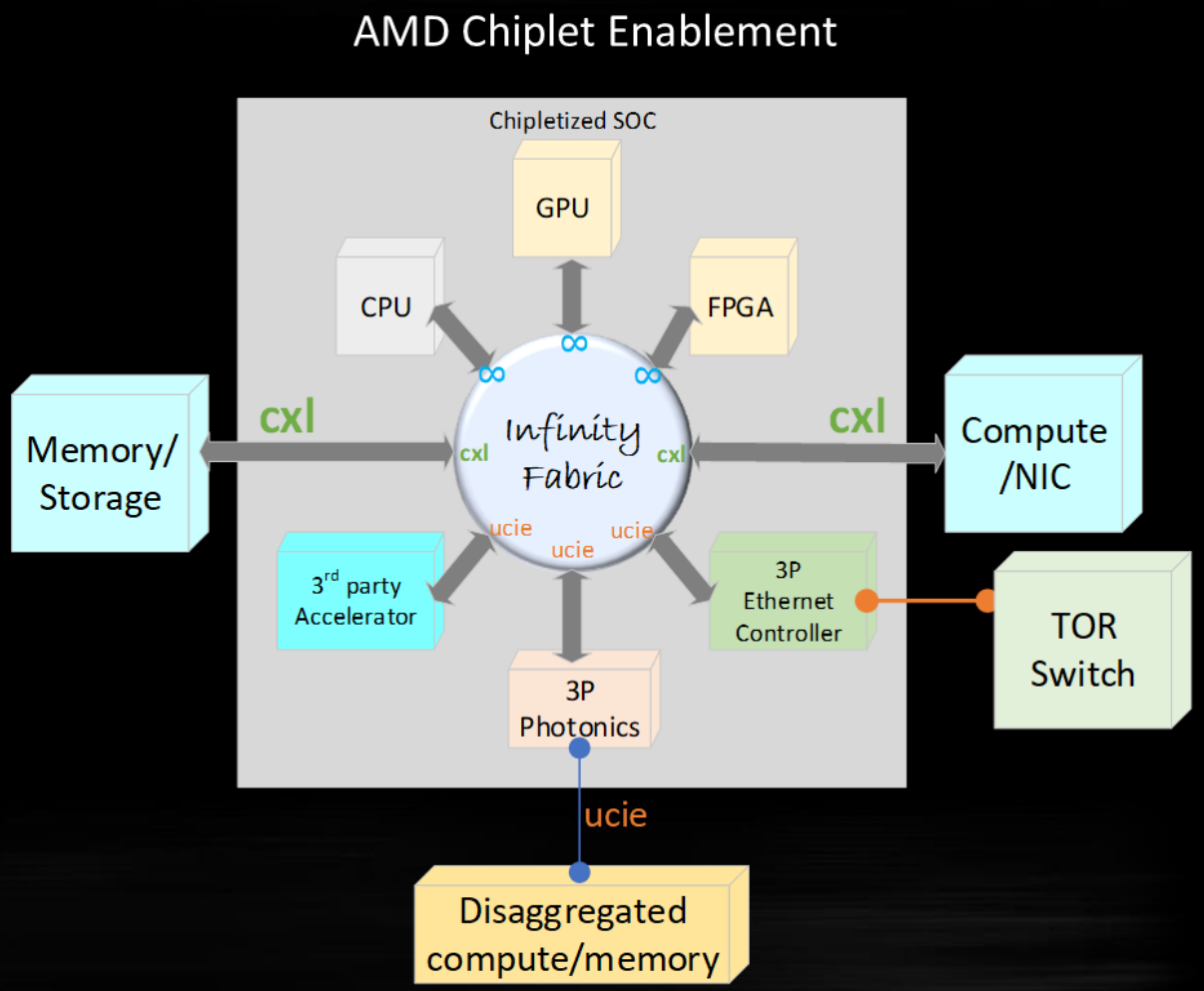
	2.5D	3D
Small Die Yield; Avoid Reticle Size Limit	✓	✓
Heterogeneous Integration	✓	✓
Product Flexibility	✓	✓
Latency		✓
Bandwidth		✓
Power		✓
Footprint		✓

Wuu, IEDM Short Course, 2022

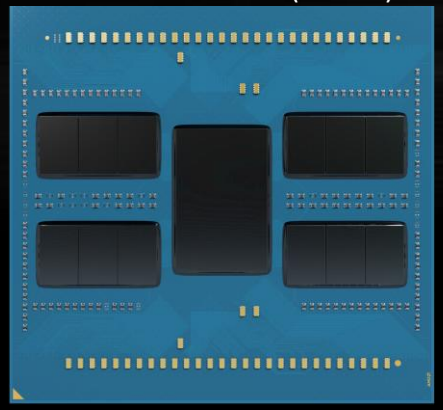
Chiplets Outlook

DOMAIN SPECIFIC ACCELERATION TO MEET COMPUTE DEMAND

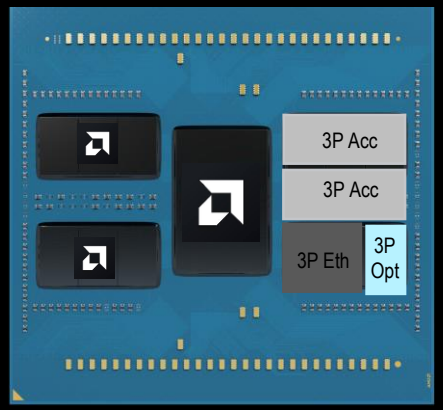
- Need many kinds of compute
- Mix and match chiplets from many vendors
- Expect systems on packages with many forms of compute, memory and I/O integrated
- Reduces developmental cost and time to market



AMD 4th Gen EPYC (Genoa)



Chiplets are good



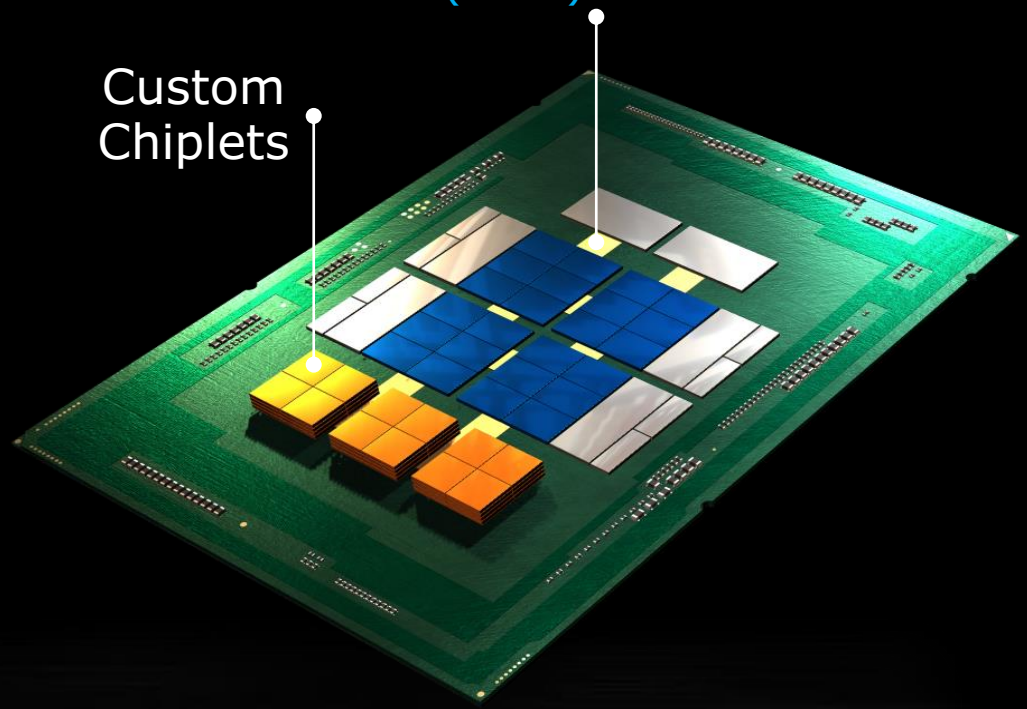
Chiplet ecosystem even better!

How do we get there?

Chiplet Ecosystem Enablement Pillars

- Widely adopted standard
- Vendor agnostic integration model

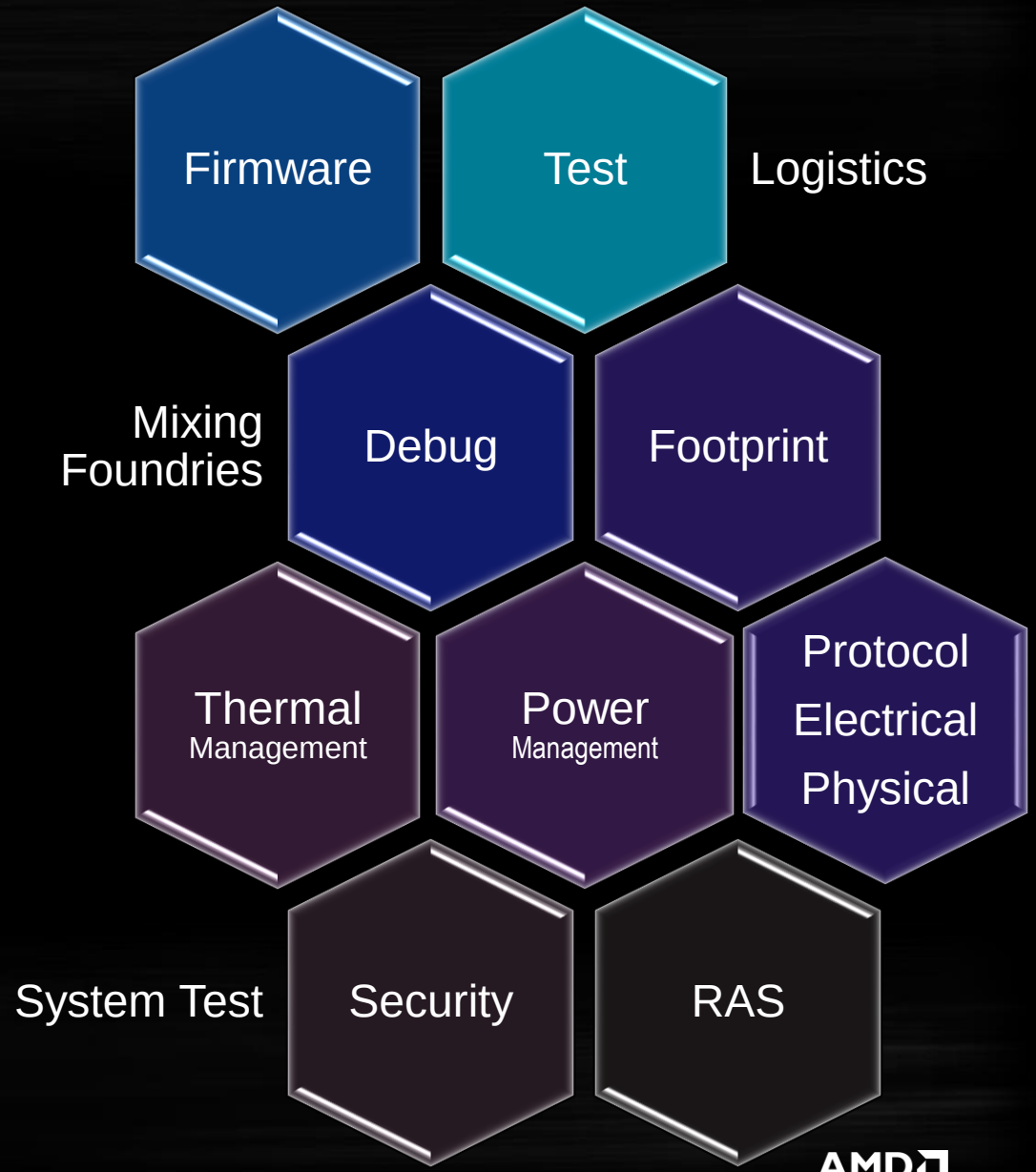
- Emerging standard
  - Universal Chiplet Interconnect Express (UCIe)
  - Supported by multiple foundries, OSAT, hyperscalars, processor and device vendors
  - 110 companies and growing



Src: UCIe Consortium

Chiplet Ecosystem Challenges

- Standard integration model for all functions
  - Protocol/Electrical/Physical
  - Software/firmware
  - Security & Manageability
  - Debug and Test
  - Power/Thermal/RAS
- Additional challenges
  - Logistics
  - Mixing Foundries
  - System Test



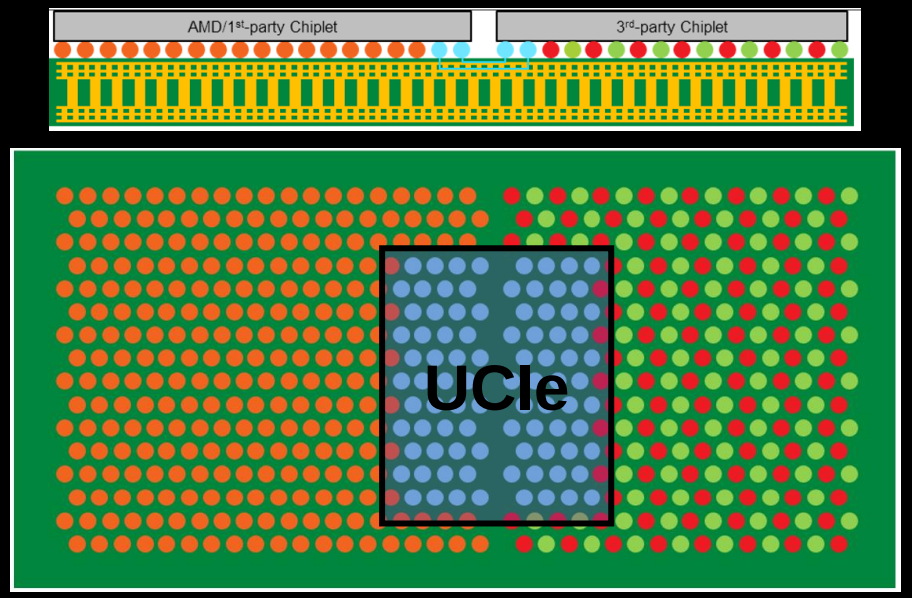
Protocol

- Pcie/CXL device integration model well understood
  - Software/driver
  - Address translation
  - Error isolation and recovery

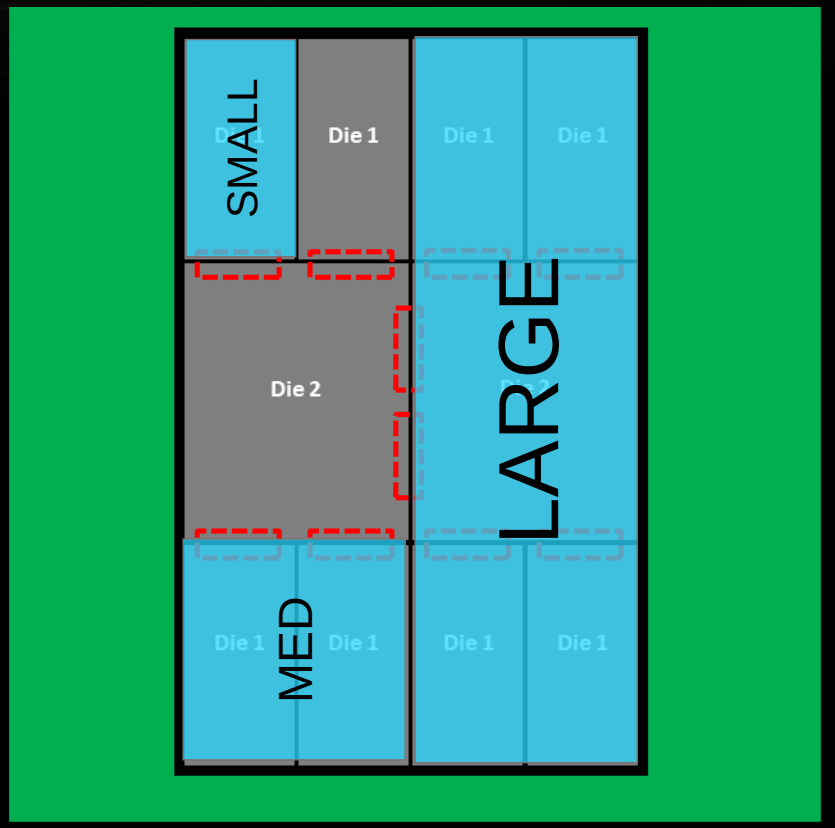
- Memory attach
  - Needs to be defined
  - Simple interface needed
  - Likely on a path to support this

- ISA-agnostic compute attach (co-processor model)
  - HMM or other memory management instead of device ATS/ATC
  - Standard coherency architecture like CXL (simplified) or CHI
  - Needs work and alignment in consortium

Floor Planning & Chiplet Footprint



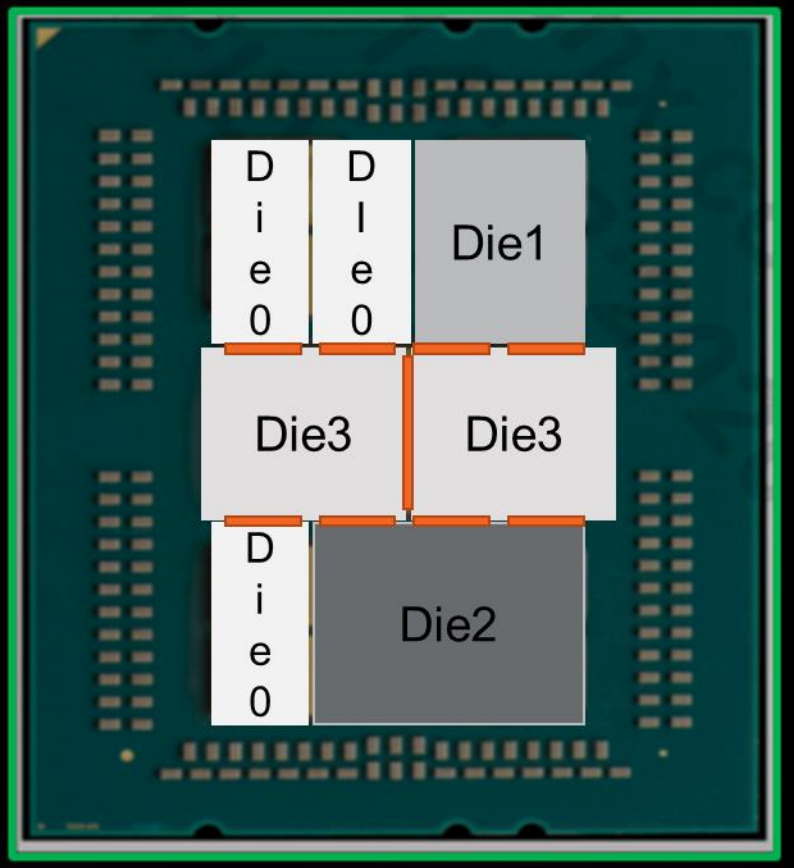
UCIe addresses only the interconnect component
Power Delivery and DFX connectivity equally important



Modular Footprints must be planned upfront

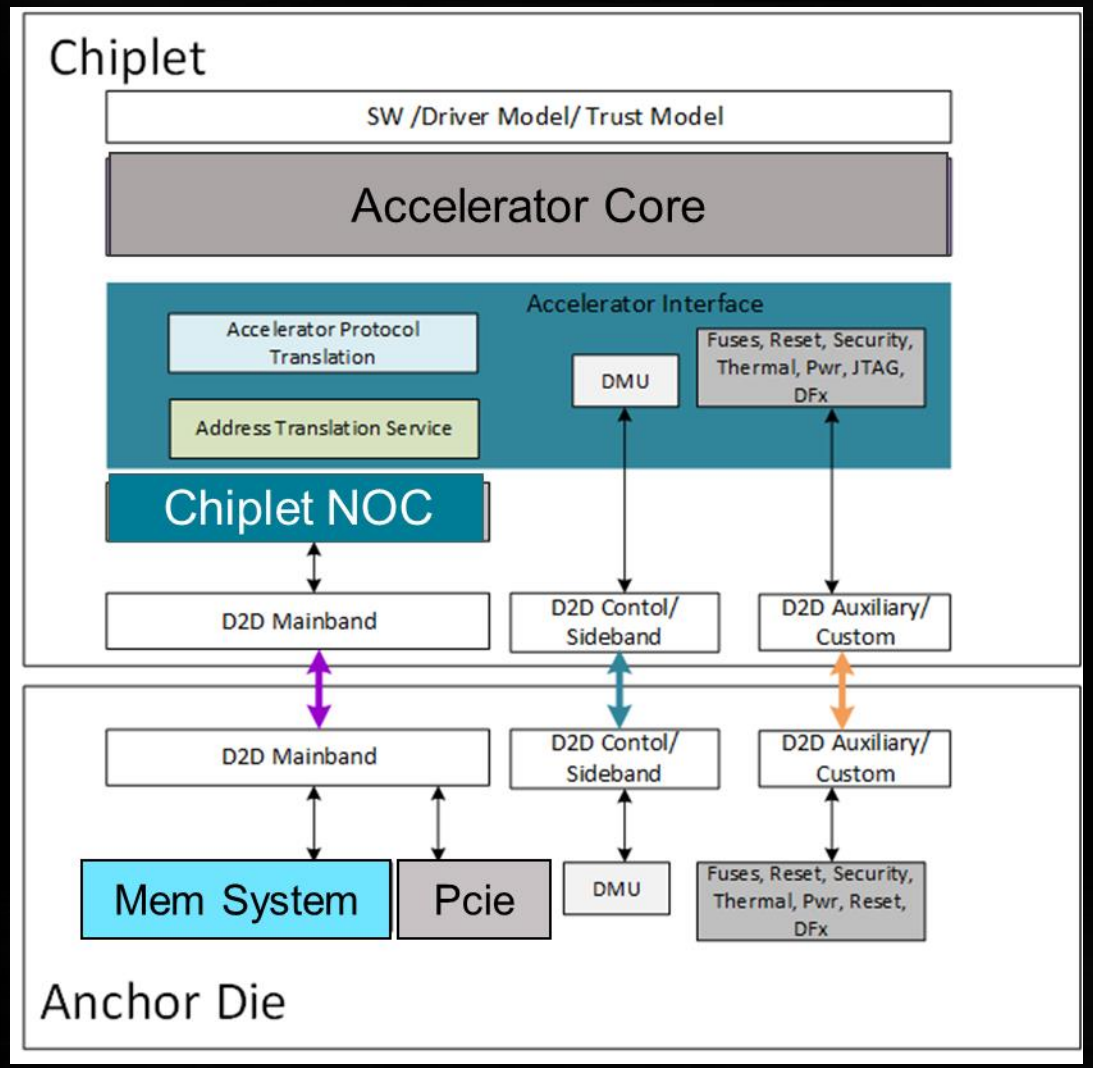
Package Resources & Impact

- Typically, many package resources allocated for external IO and logic power delivery
- Chiplet interconnects are
  - Buried deep in the interior of the dies
  - Designed to be small (and coexist with SoC Logic)
  - Ideal chiplet interconnects will leverage available Digital supplies
  - Operating on noisy supplies, pushes solutions to wide and slow
- Some (costlier!) solutions available for the higher end
- Need very good measurement and debug capabilities



Chiplet Ecosystem Solution Stack

PCIE/CXL DEVICE INTEGRATION MODEL



Scalable Design Verification/Platform Emulation

Production Testing

SW Stack (Command Processor, Accelerator driver)

Manageability (SPDM/MCTP)

Runtime RAS, Security

Runtime FW operation (Power, Thermal, Management/Telemetry)

Chiplet FW authentication

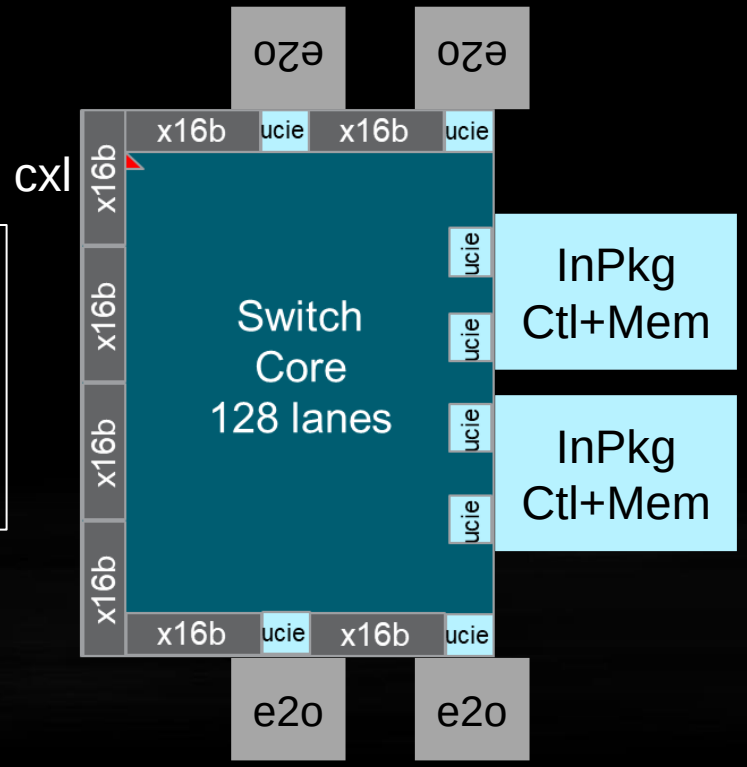
Accelerator Interface	Secure Boot/ Reset / Repair
D2D protocol	DMU (Die Management Unit)
D2D Adapter	D2D Control/ Sidebands

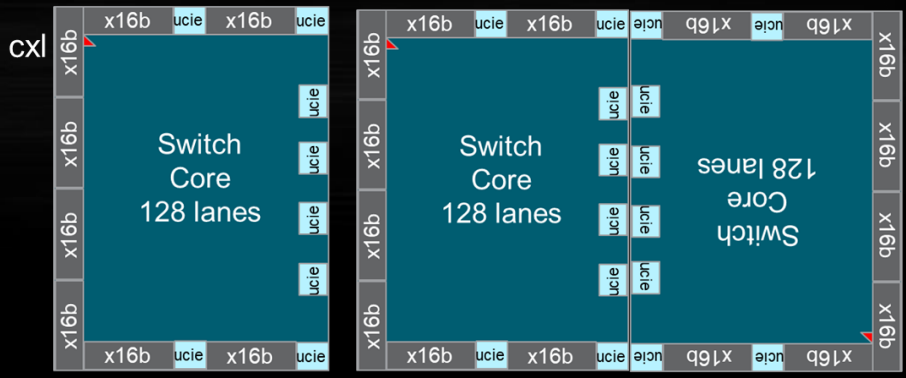
D2D Physical transport

Chiplet Applications

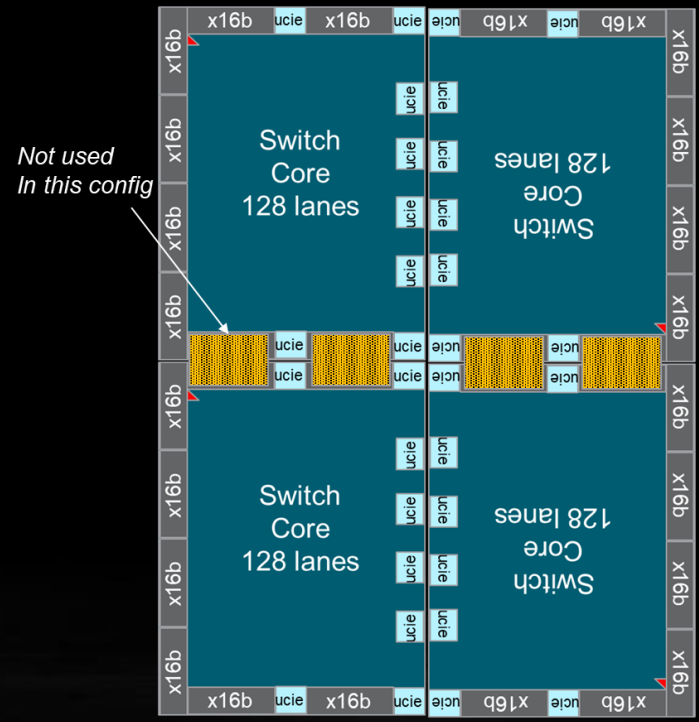
- Scalable CXL switch for illustration
  - Cost benefits due to standardized bridge chips
  - Flexibility to add
    - co-packaged optics
    - in-package memory
  - Many product options with a single die

128 lanes electrical
128 lanes equivalent optical
In-package memory





Small (128 lanes) Medium (256 lanes)



Large (384 lanes)

Summary

- Wide adoption of standard is critical
  - UCIe clears the bar with over 110 companies within 6 months of incorporation
  - UCIe on a path to enable multiple protocols – CXL, AXI, etc.
- Pcie/CXL device integration model is well established
- Critical for partners to collaborate closely
- May need custom solutions to kick start ecosystem
- Very promising but may take a few years for an ecosystem

Acknowledgements

- Alex Branover, Senior Fellow, AMD (alex.branover@amd.com)
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