CLASS 3

T04

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VER 01

DESCRIPTION:
Sub-system of Load Sharing for ADC - PWM Modulator

Sub-system of Load Sharing for ADC - PWM Modulator

Version History

VERSION:	VERSION:	CHANGE:
00	WEWEI	Edit on Sub-system of Load Sharing for ADC - PWM Modulator by WEWEI
01	WEWEI	Modified section 6.2 and added section 7.2.3 by WEWEI
01	RBMAR	1. Added section 3.1.6 2. Modified section 3.2.1.2 with the latest code for common mode voltage injection 3. Added section 8 (Appendices)

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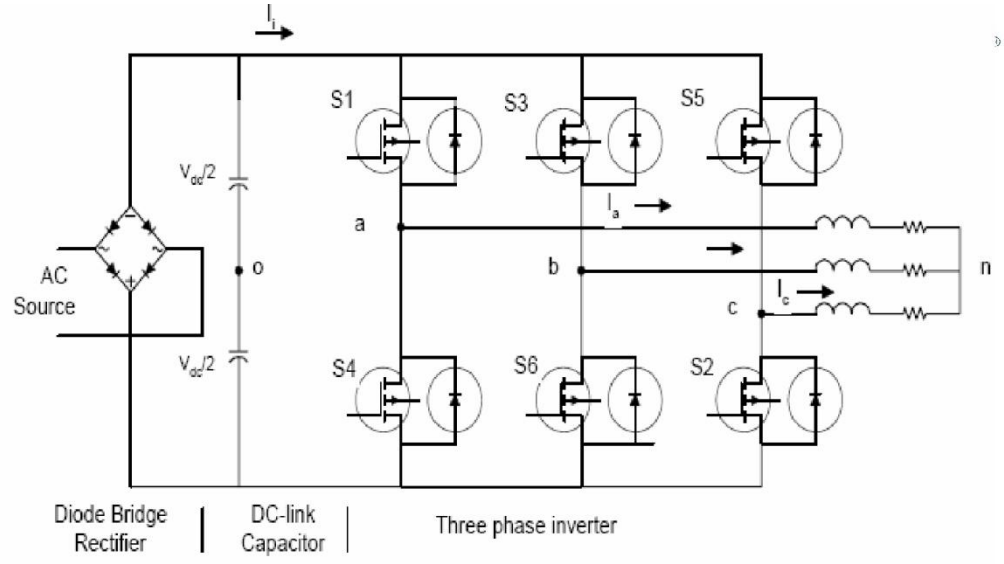


Figure 1. Three-phase voltage source inverter

The topology of a typical three-phase PWM-VSI (pulse width modulation – voltage source inverter) is shown in Figure 1. Assign the middle point of the DC link capacitor voltage as 0V, the virtual grounding, as shown in the circuit diagram. The zero sequence signal, v0, is the instantaneous voltage of the center point of the PWM output voltages, i.e. $v_o = \frac{v_a + v_b + v_c}{3}$ (1-1)

From the circuit diagram it's clear that the phase voltage of the PWM outputs are $v_a - v_0, v_b - v_0, \text{and } v_c - v_0$. The change of the zero sequence signals will not affect the phase or line voltage of the PWM output.

S1 to S6 are the six power switches that shape the output, which are controlled by the switching variables a, a', b, b', c and c'. The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg. ie. if a is on then a' is off and vice versa. In such, six non-zero output voltages (known as non-zero switching states) and two zero output voltages (known as zero switching states) are possible. These eight topologies are shown in Figure 2.

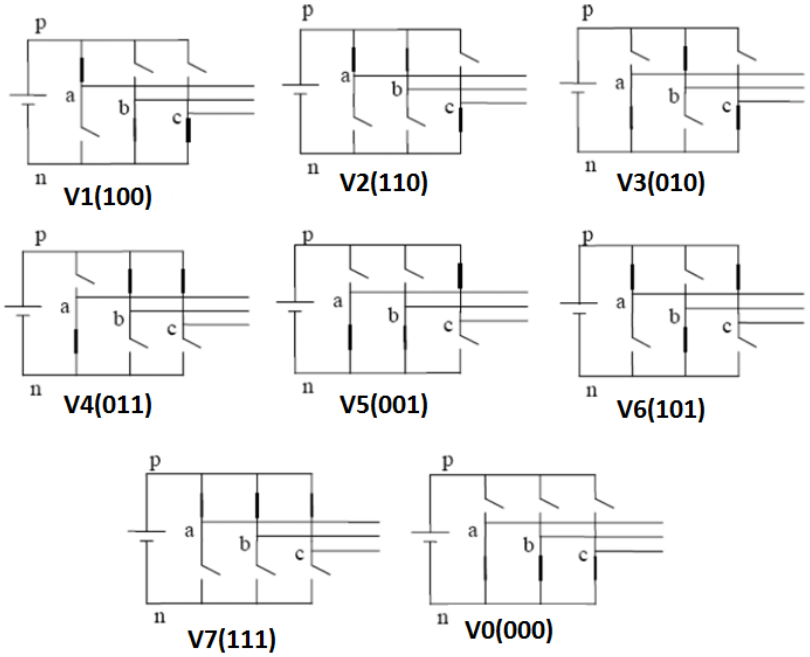


Figure 2. Eight switching states topologies

SVPWM is based on the representation of the three phase quantities as vectors in a two-dimensional (α-β) plane. In this modulation technique, the three phase quantities can be transformed to their equivalent two-phase quantity. Let the three-phase sinusoidal voltage component be

$$U_a = |\vec{U}| \cos\alpha$$
$$U_b = |\vec{U}| \cos(\alpha - 120°)$$
$$U_c = |\vec{U}| \cos(\alpha + 120°)$$

(1-2)

Then, the two-phase quantity for SVPWM analysis is:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

(1-3)

This transformation is equivalent to an orthogonal projection of Va,Vb,Vc onto the two-dimensional α-β plane. The same transformation can be applied to the desired output voltage to get the desired reference voltage vector, V* in the α-β plane. The objective of SVPWM technique is to approximate the reference voltage vector V* using the eight switching patterns. To code the above eight switching states in binary, it is required to have three bits, Let '1' denote the switch is ON and '0' denote the switch in OFF. Table 1 gives the details of different phase and line voltages for the eight states.

Table 1. Switching patterns and output vectors

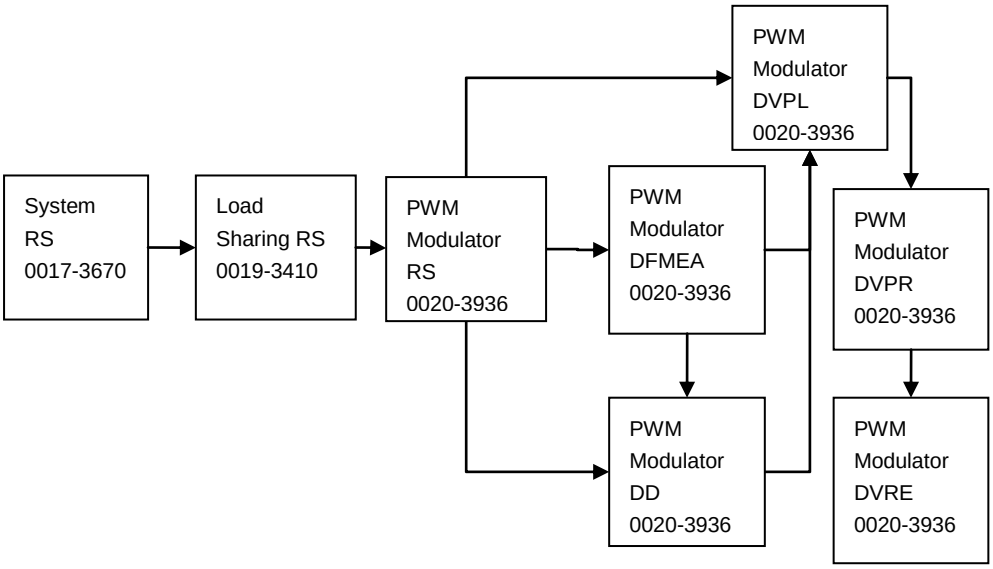
Voltage vectors	Switching vectors			Line to neutral voltage			Line to line voltage			U_α	U_β
	A	B	C	Uan	Ubn	Ucn	Uab	Ubc	Uca		
V0	0	0	0	0	0	0	0	0	0	0	0
V1	1	0	0	2/3	-1/3	-1/3	1	0	-1	2/3	0
V2	1	1	0	1/3	1/3	-2/3	0	1	-1	1/3	$1/\sqrt{3}$
V3	0	1	0	-1/3	2/3	-1/3	-1	1	0	-1/3	$1/\sqrt{3}$
V4	0	1	1	-2/3	1/3	1/3	-1	0	1	-2/3	0
V5	0	0	1	-1/3	1/3	2/3	0	-1	1	-1/3	$-1/\sqrt{3}$
V6	1	0	1	1/3	-2/3	1/3	1	-1	0	1/3	$-1/\sqrt{3}$
V7	1	1	1	0	0	0	0	0	0	0	0

1.1 Document Scope

Since PWM modulator with common mode injection capability is the sub-level of load sharing, the Requirement Specification, Design Description, Design Failure Mode and Effect Analysis, Design Verification Plan and Design Verification Procedure are combined together in this document. The purpose of this document is to modify the PWM so that it has the common mode voltage injection capability to control common mode circulation current. The study of different PWM scheme can facilitate our modification.

1.2 Document Structure

The heritage of this document is shown below:



1.3 Abbreviation

Abbreviation	Description
CMV	Common Mode Voltage
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
DPWM	Digital Pulse Width Modulation

1.4 References

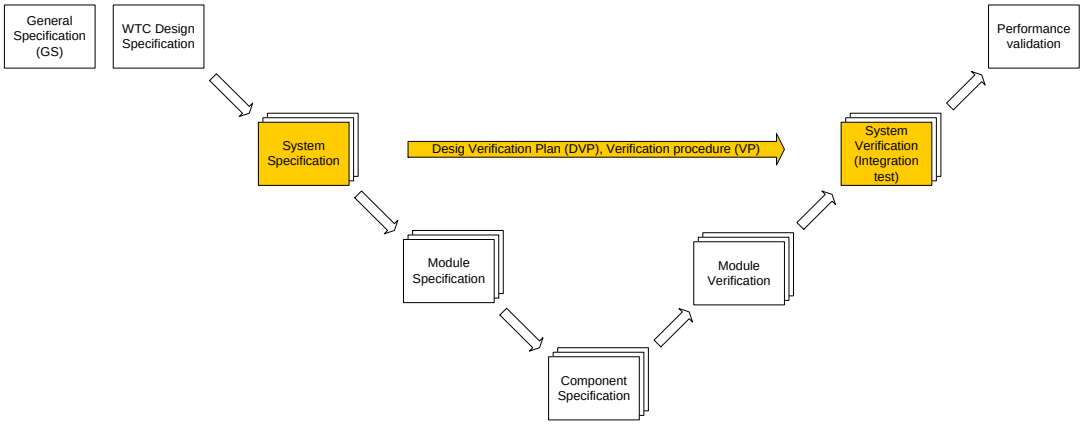
Reference Number	Description
1	Simulation and Comparison of SPWM Control for Three Phase Inverter
2	Control of Voltage Source Inverters using PWM/SVPWM for Adjusting Speed Drive Applications
3	Review of Carrier Based PWM Methods and Development of Analytical PWM Tools
4	PWM Simulink model
5	Generation of Zero Sequence Voltage U0
6	System RS (DMS # 0017-3670)
7	Load sharing RS (DMS # 0019-3410)
8	Carrier Based PWM-VSI Drives in the Overmodulation Region

SIMULATION AND COMPARISON OF SP\ Control of Voltage Source Inverters usin Review of Carrier Based PWM Methods a PWM Simulink model.doc Generation of Zero Sequence Voltage U0 **Error! Not a valid link.**

2. Requirement Specification for PWM Modulator

2.1 Introduction

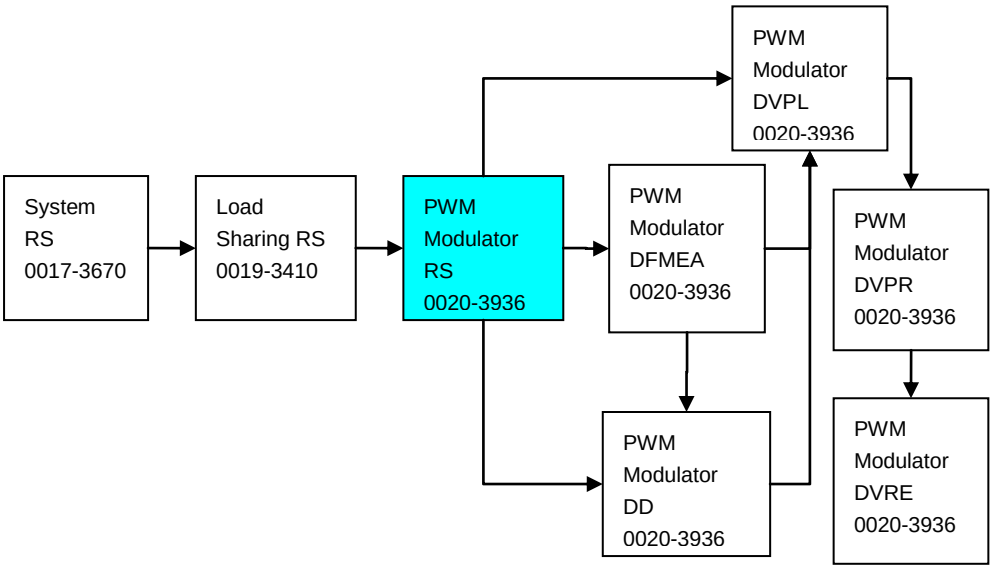
This section provides the RS for the Advance Digital Control (ADC) project workpackage WPA.1 PWM Modulator.



The present project is one of research in nature and will only follow the above model where appropriate.

2.2 Document Structure

The heritage of this section is shown below:



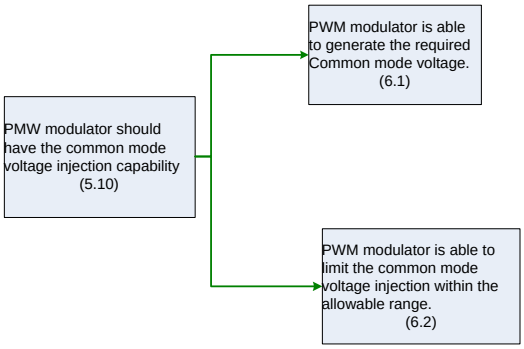
2.3 Requirement Specification Heritage

In the load sharing RS (DMS 0019-3410), the requirement for PWM Modulator includes the following items:

RS 5.11 - PMW modulator should have the common mode voltage injection capability

2.4 Function Tree

The following function tree is to describe the function blocks required to achieve PWM Modulator for WPA.1 Distributed Control.



2.5 Functional Requirement Specification

2.5.1 6.1 Requirement

PWM modulator is able to generate the required common mode voltage.

Motivation: In order to generate the required gate signal at IGBT.
Source: System RS, Load sharing RS
Verification method: Modified Vestas Power Controller (CT360).
Conflicts: Not applicable.

2.5.2 6.2 Requirement

PWM modulator is able to limit the common mode voltage injection within the allowable range.

Motivation: Ensure the voltage injection is within the capability of the power converters.
Source: System RS, Load sharing RS
Verification method: Modified Vestas Power Controller (CT360).
Conflicts: Not applicable.

3. Design Description for PWM Modulator

3.1 Design Description

This section is subdivided into 5 main parts:

- **Voltage Space Vector:** This section demonstrates the definition and usage of voltage space vectors.
- **Sector Identification:** This includes the procedure to identify the sectors. Both the 6-sector identification and 12-sector identification are discussed.
- **Calculation of Duty Cycles**: This section explains the procedure to determine the duty cycles for a 6-sector voltage space vectors.
- **Calculation of CMV U_0 and Its Two Limits:** This section derives the general formula for CMV in terms of duty cycles. The maximum and minimum values are also derived and summarized.
- **Transistor Switching Time With and Without CMV Injection U_0:** By using the relation among CMV injection, duty cycles and transistor switching times, the transistor switching time with and without CMV injection is formulated.

3.1.1 Voltage Space Vector

From Table 1, when drawing the six non -zero voltages vectors (V1-V6) in α-β plane, they shape the axes of a hexagonal as depicted in Figure 3. The two zero vectors (V0 and V7) are at the origin and apply zero voltage to the load. We define the area enclosed by two adjacent vectors, within the hexagon, as a sector, as shown in Figure 3.

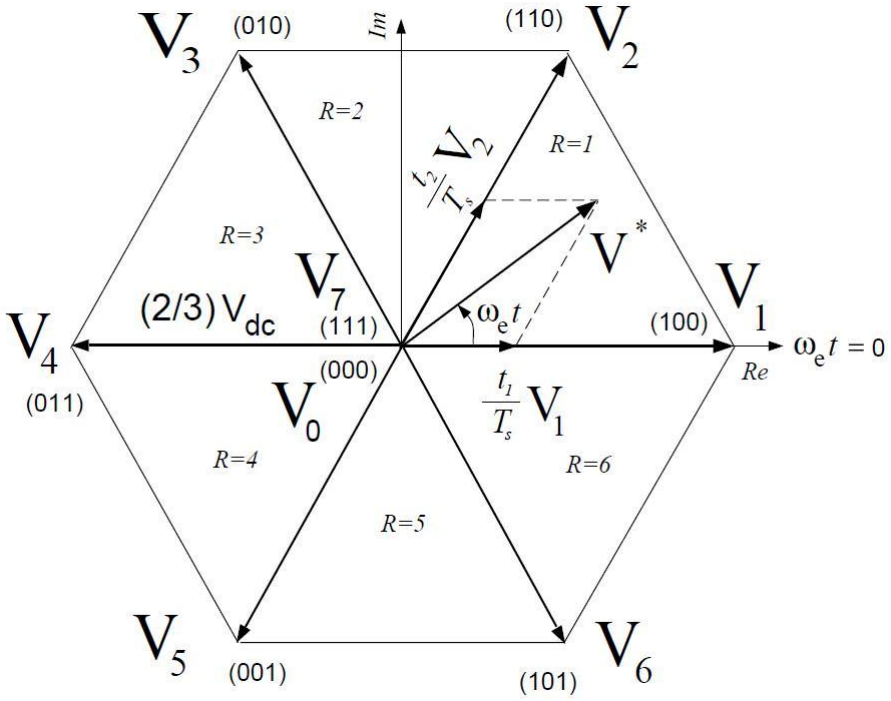


Figure 3. Six-Sector Definition

The desired three phase voltages at the output of the inverter could be represented by an equivalent vector V* rotating in the counter clock wise direction as shown in Figure 3. The magnitude of this vector is related to the magnitude of the output voltage and the time this vector takes to complete one revolution is the same as the fundamental time period of the output voltage. The sectors are defined as 1 ~ 6 when the voltage vector rotates a cycle. The reference vector V* is then synthesized using a combination of the two adjacent active switching vectors and one or both of the zero vectors.

Although theoretically an infinite number of zero sequence signals and therefore modulation methods could be developed, the performance and implementation constraints of practical PWM-VSI drives reduce the possibility to a small number. Over the last three decades of PWM technology evolution, about ten high performance carrier based PWM methods were developed and of these only several have gained wide acceptance. The modulators illustrated in Figure 1 can be separated into two groups. In the Continuous PWM (CPWM) methods, the modulation waves are always within the triangle peak boundaries. Within every carrier cycle, the triangular carrier wave and the modulation wave intersect and therefore on and off switching occur. In the Discontinuous PWM (DPWM) methods, the modulation wave of a phase has at least one segment which is clamped to the positive and/or negative DC rail for at most a total of 120 degrees (over a fundamental cycle). Therefore, the corresponding inverter leg discontinues modulation within such intervals. Since no modulation implies no switching losses, the switching loss characteristics of CPWM and DPWM methods are different. Detailed studies indicated the waveform quality and linearity characteristics are also significantly different. Therefore, this classification aids in distinguishing the important differences between CPWM and DPWM methods [03].

Of the modern CPWM methods, the triangle intersection implementation of the Space Vector PWM (SVPWM) method is one of the most popular CPWM methods. SVPWM [03]: The zero sequence signal of SVPWM is generated by employing the minimum magnitude test which compares the magnitudes of the three reference signals and selects the signal with minimum magnitude [03]. Scaling this signal with 0.5, the zero sequence signal of SVPWM is found. Since the direct digital implementation utilized the space vector

theory, the method was named SVPWM. In addition to its implementation simplicity, the SVPWM method has superior performance characteristics (compared to other CPWM methods) and is possibly the most popular high performance PWM method. However, its high modulation range performance is inferior to DPWM methods, which also employ similar magnitude rules to generate their modulation waves.

In the DPWM methods, a zero sequence signal which brings one of the three modulation signals to the same level with the positive or negative peak of the triangular carrier wave is selected. Since the switching in the corresponding inverter leg ceases, the switching losses are eliminated so long as this condition persists. Therefore, the inverter switching losses can be controlled with the zero sequence signals [08].

In the following, the modern DPWM methods – DPWM0 and DPWM1 and their magnitude rules are summarized.

DPWM0 [03]: All three reference modulation signals va, vb, and vc are phase shifted by 30 degree (leading), and of the three new signals vax, vbx, and vcx, the one with the maximum magnitude determines the zero sequence signal. Adding this zero sequence signal to the three original modulation waves va, vb, and vc , the DPWM0 waves va*, vb*, and vc* are generated. This method has minimum switching losses at 30 degree leading power factor operating condition, and its waveform quality at high modulation is superior to SVPWM [03].

DPWM1 [03]: The reference signal with the maximum magnitude defines the zero sequence signals. This method has minimum switching losses at unity power factor operating condition, and its waveform quality at high modulation is superior to SVPWM [03, 08].

In SVPWM and DPWM0, we use the 6-sector identification as shown in Figure 3. Because the reference signal with the maximum magnitude defines the 0-sequence signals, and also the discontinuous property of DPWM1, the 12-sector indemnification is need for DPWM1.

3.1.2 Sector Identification

3.1.2.1 6-Sector Identification

The SVPWM or DPWM0 can be derived with V0 = V7 if U_α and U_β are given.

The model is using a mapping to simplify the calculation needed. The following three steps are used to determine in which sector the voltage is located.

Firstly, we map U* to $U_{1x} - U_{1\perp x}(U_\alpha - U_\beta)$ plane as shown in Figure 4:

$$U_{1x} = U^* \cdot \cos\alpha = U_\alpha \tag{3-1}$$

$$U_{1\perp x} = U^* \cdot \sin\alpha = U_\beta \tag{3-2}$$

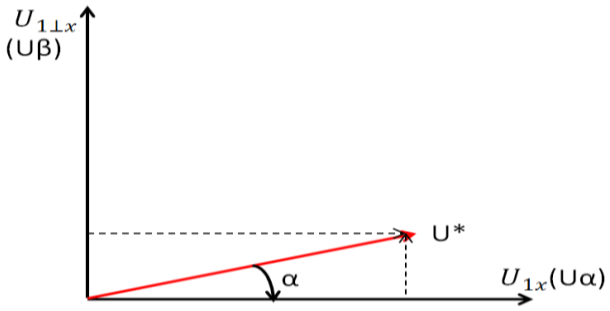


Figure 4. Reference vector in $U_{1x} - U_{1\perp x}(U_\alpha - U_\beta)$ plane

Secondly, we map U* to $U_{2y} - U_{2\perp y}$ plane as shown in Figure 5:

$$U_{2y} = U^* \cdot \sin\left(\frac{\pi}{6} - \alpha\right) = -\frac{1}{2}U_\alpha + \frac{\sqrt{3}}{2}U_\beta \tag{3-3}$$

$$U_{2\perp y} = -U^* \cdot \cos\left(\frac{\pi}{6} - \alpha\right) = -\frac{\sqrt{3}}{2}U_\alpha - \frac{1}{2}U_\beta \quad (3\text{-}4)$$

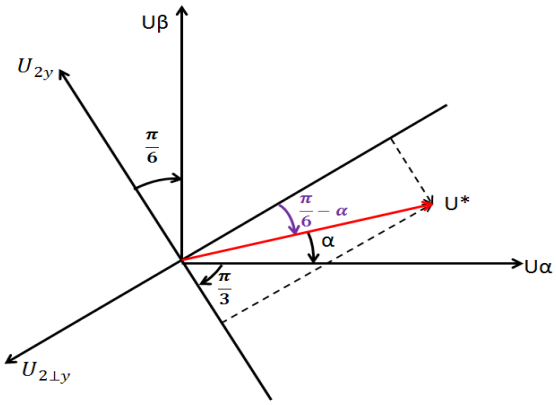


Figure 5. Reference vector in $U_{2y} - U_{2\perp y}$ plane

Thirdly, we map U* to $U_{3z} - U_{3\perp z}$ plane as shown in Figure 6:

$$U_{3z} = -U^* \cdot \cos\left(\frac{\pi}{3} - \alpha\right) = -\frac{1}{2}U_\alpha - \frac{\sqrt{3}}{2}U_\beta \quad (3\text{-}5)$$

$$U_{3\perp z} = U^* \cdot \sin\left(\frac{\pi}{3} - \alpha\right) = \frac{\sqrt{3}}{2}U_\alpha - \frac{1}{2}U_\beta \quad (3\text{-}6)$$

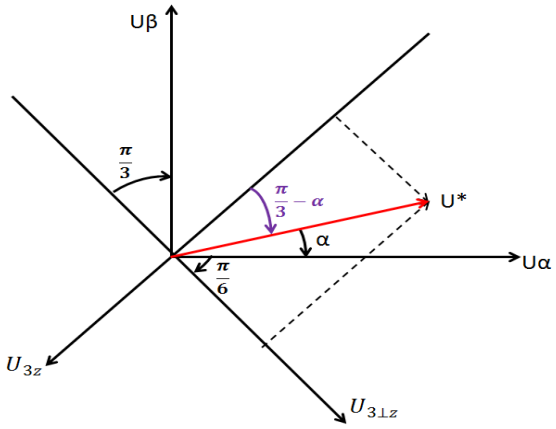


Figure 6. Reference vector in $U_{3z} - U_{3\perp z}$ plane

With the above mapping method, we are now able to determine in which sector the voltage is located. Take U* in Figure 4 as an example. From Figure 4, we notice that it is located at the +ve $U_{1\perp x}$ half plane. Thus, only sectors 1, 2 and 3 are possible. Then from Figure 6, we know that it is located at the +ve $U_{3\perp z}$ half plane, thus only sectors 1, 5 and 6 are possible. Combine the two, we conclude that U* is in sector 1.

Similar conclusion can be drawn for other sectors. In summary:

Sector 1: +ve $U_{1\perp x}$ half plane, +ve $U_{3\perp z}$ half plane

Sector 2: +ve $U_{1\perp x}$ half plane, -ve $U_{2\perp y}$ half plane, -ve $U_{3\perp z}$ half plane

Sector 3: +ve $U_{1\perp x}$ half plane, +ve $U_{2\perp y}$ half plane,-ve $U_{3\perp z}$ half plane

Sector 4: -ve $U_{1\perp x}$ half plane, -ve $U_{3\perp z}$ half plane

Sector 5: -ve $U_{1\perp x}$ half plane, +ve $U_{2\perp y}$ half plane, +ve $U_{3\perp z}$ half plane

Sector 6: -ve $U_{1\perp x}$ half plane, -ve $U_{2\perp y}$ half plane, +ve $U_{3\perp z}$ half plane

For the coding, we using the following notations:
Uar = Ualpha * sqrt(3);
Ubr = Ubeta * sqrt(3);

$$t_a = -U_\beta = -U_{1\perp x}$$

$$t_b = -\frac{\sqrt{3}}{2}U_\alpha - \frac{1}{2}U_\beta = U_{2\perp y}$$

$$t_c = \frac{\sqrt{3}}{2}U_\alpha - \frac{1}{2}U_\beta = U_{3\perp z}$$

Here are the codes used to generate 6-sector numbers:

```
function [Sector] = modulatorN6S(ta,tb,tc)
if ta < 0
   if tc > 0
      Sector = 0;                    // Sector 1: +ve U1⊥x half plane, +ve U3⊥z half plane
   else
      if tb > 0
         Sector = 2;      // Sector 3: +ve U1⊥x half plane, +ve U2⊥y half plane, -ve U3⊥z half plane
      else
         Sector = 1;      // Sector 2: +ve U1⊥x half plane, -ve U2⊥y half plane, -ve U3⊥z half plane
      end
   end
else
   if tc < 0
      Sector = 3;                    // Sector 4: -ve U1⊥x half plane, -ve U3⊥z half plane
   else
      if tb < 0
         Sector = 5;      // Sector 6: -ve U1⊥x half plane, -ve U2⊥y half plane, +ve U3⊥z half plane
      else
         Sector = 4;      // Sector 5: -ve U1⊥x half plane, +ve U2⊥y half plane, +ve U3⊥z half plane
      end
   end
end
```

The actual waveform is shown in Figure 7.
The 1st waveform is the reference voltage in α-β frame (blue curve is Ualpha and green curve is Ubeta).

The 2nd waveform is 3-phase voltage (blue curve is Uar, green curve is Ubr and red curve is Ucr).

The 3rd waveform is the signal generated from above code (blue curve is ta, green curve is tb and red curve is tc).

The 4th waveform is the sector number (sector 0 to 5).

From the waveform it can be verified that the sector numbers are following the definition shown in Figure 3.

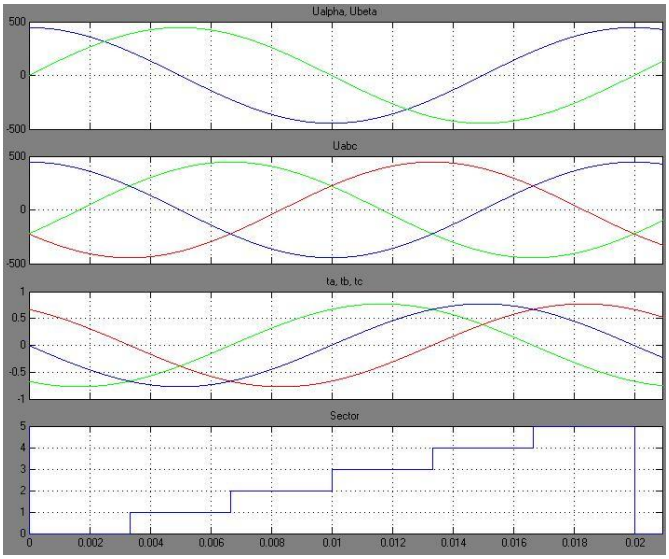


Figure 7. Waveform of 6-Sector Determination

3.1.2.2 12-Sector Identification

For DPWM1, we use 12-sector identification.
First we divide the circle into 6 sectors, same as what we did for SVPWM. Then, within each sector, we divide them into two – one is T000=0 and the other one is T111=0. Hence, 12 sectors are determined.

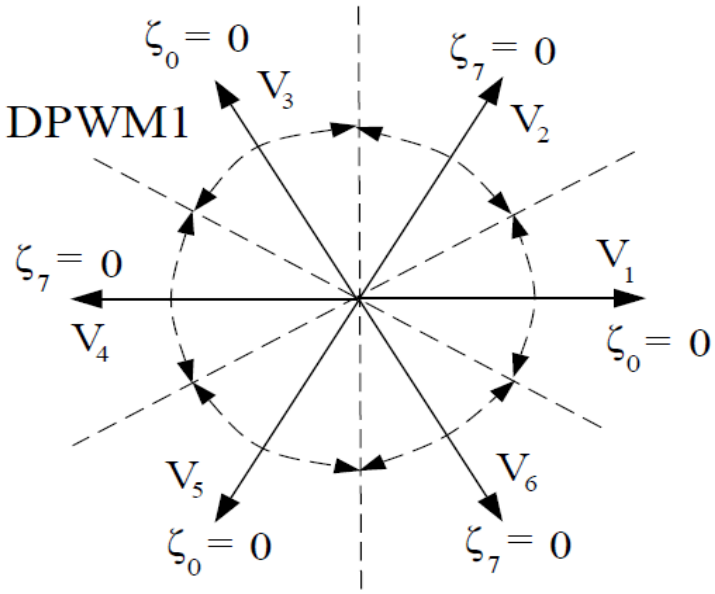


Figure 8. DPWM1 Sector Definition

3.1.2.2.1 Sector 0 and 1

Following the definition shown in Figure 8, within the original sector 1 of SVPWM, we need to differentiate sector 0 and 1 for DPWM1.

For sector 0, we have

$$0 < \alpha < 30^\circ \Rightarrow \tan(\alpha) < \tan 30^\circ$$

$$\Rightarrow \frac{U_\beta}{U_\alpha} < \frac{\sqrt{3}}{3} \Rightarrow U_\alpha - \sqrt{3} \cdot U_\beta > 0$$

$$\Rightarrow \underbrace{\frac{\sqrt{3}}{2} U_\alpha - \frac{1}{2} U_\beta}_{t_c} \underbrace{- U_\beta}_{t_a} > 0$$

$$\Rightarrow t_a + t_c > 0$$

Thus, the code for determine sector 0 and 1 is:

```
if ta < 0                                                    // from 6-sector identification
   if tc > 0        // from 6-sector identification, identify the original sector 1 of SVPWM
      if (ta + tc) > 0                                       // Condition to identify sector 0
         Sector = 0;
      else
         Sector = 1;                          // if not sector 0, then it should be sector 1
      end
```

3.1.2.2.2 Sector 4 and 5

Similarly, to identify sector 4 from the original sector 3 of SVPWM, we have

$$\Rightarrow \frac{U_\beta}{-U_\alpha} > \tan 30^\circ = \frac{\sqrt{3}}{3} \Rightarrow U_\alpha + \sqrt{3} \cdot U_\beta > 0$$

$$\Rightarrow \underbrace{\frac{\sqrt{3}}{2} U_\alpha + \frac{1}{2} U_\beta}_{-t_b} \underbrace{+ U_\beta}_{-t_a} > 0$$

$$\Rightarrow t_a + t_b < 0$$

Thus the code for determine sector 4 and 5 is:

```
if ta < 0                                                    // from 6-sector identification
   if tc > 0
      ⋮
   else
      if tb > 0      // from 6-sector identification, identify the original sector 3 of SVPWM
         if (ta + tb) < 0                                    // Condition to identify sector 4
            Sector = 4;
         else
            Sector = 5;                          // if not sector 4, then it should be sector 5
         end
```

3.1.2.2.3 Sector 2 and 3

To differentiate DPWM1 sector 2 and 3 (both belongs to the original sector 2 of SVPWM), within the original sector 2 of SVPWM:

$$if \quad U_\alpha > 0 \quad i.e. \quad t_c > t_b \Rightarrow \text{sec}tor2$$

$$otherwise \Rightarrow \text{sec}tor3$$

Thus the code for determine sector 2 and 3 is:

```
if ta < 0                                                    // from 6-sector identification
   if tc > 0
      ⋮
   else
      if tb > 0
         ⋮
      else          // from 6-sector identification, identify the original sector 2 of SVPWM
         if tc > tb
            Sector = 2;                                      // Condition to identify sector 2
         else
            Sector = 3;                          // if not sector 2, then it should be sector 3
```

end

3.1.2.2.4 Sector 6 and 7

To identify DPWM1 sector 6 & 7 from the original sector 4 of SVPWM, for sector 6, we have:

$$\frac{-U_\beta}{-U_\alpha} < \tan 30^\circ = \frac{\sqrt{3}}{3} \Rightarrow U_\alpha - \sqrt{3}\cdot U_\beta < 0$$

$$\Rightarrow \underbrace{\frac{\sqrt{3}}{2}U_\alpha - \frac{1}{2}U_\beta}_{t_c} \underbrace{-U_\beta}_{t_a} < 0$$

$$\Rightarrow t_a + t_c < 0$$

Thus the code for determine sector 6 and 7 is:

```
if ta < 0                                                    // from 6-sector identification
    ⋮
else
    if tc < 0       // from 6-sector identification, identify the original sector 4 of SVPWM
      if (ta + tc) < 0
         Sector = 6;                                         // Condition to identify sector 6
      else
         Sector = 7;                          // if not sector 6, then it should be sector 7
      end
```

3.1.2.2.5 Sector 10 and 11

To identify DPWM1 sector 10 & 11 from the original sector 6 of SVPWM, for sector 10, we have:

$$\Rightarrow \frac{-U_\beta}{U_\alpha} > \tan 30^\circ = \frac{\sqrt{3}}{3} \Rightarrow U_\alpha + \sqrt{3}\cdot U_\beta < 0$$

$$\Rightarrow \underbrace{\frac{\sqrt{3}}{2}U_\alpha + \frac{1}{2}U_\beta}_{-t_b} \underbrace{+U_\beta}_{-t_a} < 0$$

$$\Rightarrow t_a + t_b > 0$$

Thus the code for determine sector 10 and 11 is:

```
if ta < 0                                                    // from 6-sector identification
    ⋮
else
    if tc < 0
        ⋮
    else
       if tb < 0    // from 6-sector identification, identify the original sector 6 of SVPWM
         if (ta + tb) > 0
            Sector = 10;                                     // Condition to identify sector 10
         else
            Sector = 11;                         // if not sector 10, then it should be sector 11
         end
```

3.1.2.2.6 Sector 8 and 9

To differentiate DPWM1 sector 8 and 9 (both belongs to the original sector 5 of SVPWM), within the original sector 5 of SVPWM:

$$if \quad U_\alpha < 0 \quad i.e. \quad t_b > t_c \Rightarrow \mathrm{sec}tor8$$

$$otherwise \Rightarrow \mathrm{sec}tor9$$

Thus the code for determine sector 8 and 9 is:

```
if ta < 0                                                    // from 6-sector identification
    ⋮
else
    if tc < 0
        ⋮
```

```
else
   if tb < 0
      ⋮
   else        // from 6-sector identification, identify the original sector 5 of SVPWM
     if tb > tc
        Sector = 8;                                  // Condition to identify sector 8
     else
        Sector = 9;                          // if not sector 8, then it should be sector 9
     end
```

3.1.3 Calculation of Duty Cycles

3.1.3.1 Some Notations

Let's denote,

$$t_a = -V_\beta \tag{3-7}$$

$$t_b = -\frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta \tag{3-8}$$

$$t_c = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta \tag{3-9}$$

T1: The time when S1 turns ON (or off time of S1);
T2: The time when S3 turns ON (or off time of S3);
T3: The time when S5 turns ON (or off time of S5);
D1: Duration where one and only one out of three power switches (S1, S3 & S5) is ON in the switching cycle;
D2: Duration where two out of three power switches (S1, S3 & S5) are ON in the switching cycle;

From
Figure 9, we have:
Ti=min(T1,T2,T3)
Tk=max(T1,T2,T3)
Tj=sum(T1,T2,T3)-min(T1,T2,T3)-max(T1,T2,T3)

Then
Tj=Ti+D1;
Tk=Tj+D2.

Please note that all the time values discussed below are nomilized to Ts/2.

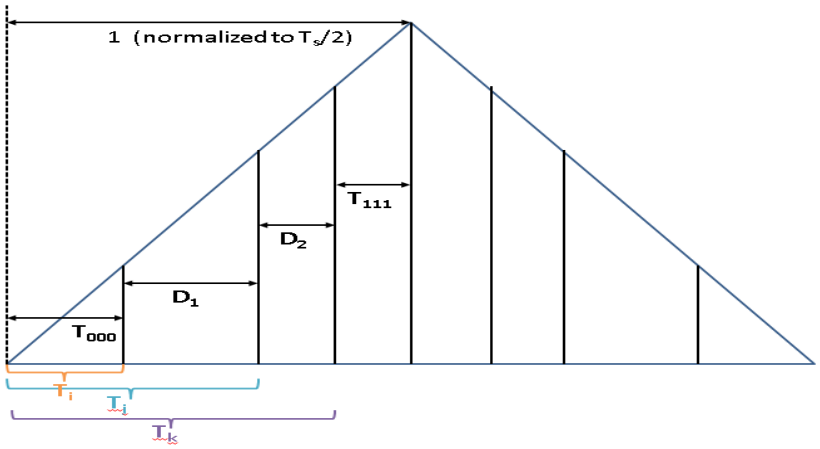


Figure 9. Illustration of different switching times of each transistor in one PWM cycle (off time).

3.1.3.2 Case 0 (Sector 1)

The voltages when normalized to $\frac{\sqrt{3}}{2}V_{dc}$ are:

$$V_1 = D_1 \cdot \frac{2}{\sqrt{3}} \tag{3-10}$$

$$V_2 = D_2 \cdot \frac{2}{\sqrt{3}} \tag{3-11}$$

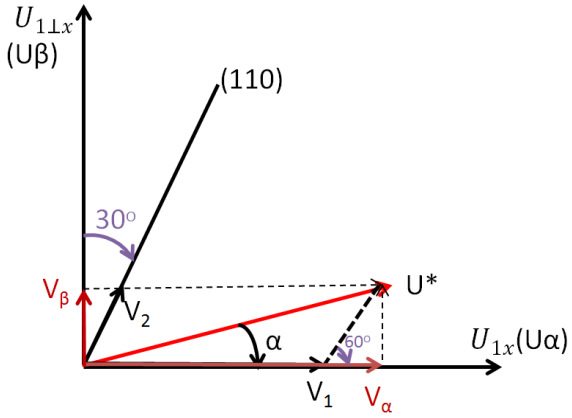


Figure 10. Calculation of duty cycle from Vα, Vβ

From Figure 10, we have:

$$V_\alpha = V_2 \cdot \sin 30° + V_1 = D_2 \cdot \frac{1}{\sqrt{3}} + D_1 \cdot \frac{2}{\sqrt{3}}$$

$$V_\beta = V_2 \cdot \cos 30° = D_2$$

$$\therefore D_1 = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_c \tag{3-12}$$

$$D_2 = V_\beta = -t_a \tag{3-13}$$

3.1.3.3 Case 1 (Sector 2)

$$V_3 = D_1 \cdot \frac{2}{\sqrt{3}} \tag{3-14}$$

$$V_2 = D_2 \cdot \frac{2}{\sqrt{3}} \tag{3-15}$$

$$\therefore V_\alpha = V_2 \cdot \sin 30° - V_3 \cdot \sin 30° = D_2 \cdot \frac{1}{\sqrt{3}} - D_1 \cdot \frac{1}{\sqrt{3}}$$

$$V_\beta = V_2 \cdot \cos 30° + V_3 \cdot \cos 30° = D_2 + D_1$$

$$\therefore D_1 = -\frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_c \tag{3-16}$$

$$D_2 = \frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_b$$

(3-17)

3.1.3.4 Case 2 (Sector 3)

$$V_3 = D_1 \cdot \frac{2}{\sqrt{3}}$$

(3-18)

$$V_4 = D_2 \cdot \frac{2}{\sqrt{3}}$$

(3-19)

$$\therefore V_\alpha = -V_3 \cdot \sin 30° - V_4 = -D_1 \cdot \frac{1}{\sqrt{3}} - D_2 \cdot \frac{2}{\sqrt{3}}$$

$$V_\beta = V_3 \cdot \cos 30° = D_1$$

$$D_2 = -\frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_b \quad \therefore D_1 = V_\beta = -t_a$$

(3-20)

(3-21)

3.1.3.5 Case 3 (Sector 4)

$$V_5 = D_1 \cdot \frac{2}{\sqrt{3}}$$

(3-22)

$$V_4 = D_2 \cdot \frac{2}{\sqrt{3}}$$

(3-23)

$$\therefore V_\alpha = -V_5 \cdot \sin 30° - V_4 = -D_1 \cdot \frac{1}{\sqrt{3}} - D_2 \cdot \frac{2}{\sqrt{3}}$$

$$V_\beta = -V_5 \cdot \cos 30° = -D_1$$

$$D_2 = -\frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_c \quad \therefore D_1 = -V_\beta = t_a$$

(3-24)

(3-25)

3.1.3.6 Case 4 (Sector 5)

$$V_5 = D_1 \cdot \frac{2}{\sqrt{3}}$$

(3-26)

$$V_6 = D_2 \cdot \frac{2}{\sqrt{3}}$$

(3-27)

$$\therefore V_\alpha = V_6 \cdot \sin 30° - V_5 \cdot \sin 30° = -D_1 \cdot \frac{1}{\sqrt{3}} + D_2 \cdot \frac{1}{\sqrt{3}}$$

$$V_\beta = -V_5 \cdot \cos 30° - V_6 \cdot \cos 30° = -D_1 - D_2$$

$$D_2 = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_c$$

$$\therefore D_1 = -\frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_b$$

(3-28)

(3-29)

3.1.3.7 Case 5 (Sector 6)

$$V_1 = D_1 \cdot \frac{2}{\sqrt{3}}$$

(3-30)

$$V_6 = D_2 \cdot \frac{2}{\sqrt{3}}$$

(3-31)

$$D_2 = -V_\beta = t_a \quad \therefore V_\alpha = V_1 + V_6 \cdot \sin 30° = D_1 \cdot \frac{2}{\sqrt{3}} + D_2 \cdot \frac{1}{\sqrt{3}}$$

$$V_\beta = -V_6 \cdot \cos 30° = -D_2$$

$$\therefore D_1 = \frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_b$$

(3-32)

(3-33)

3.1.4 Calculation of CMV U_0 and Its Two Limits

3.1.4.1 CMV U_0 calculation

From the circuit diagram it's obvious that the instantaneous voltage of the PWM output voltage $v_a, v_b,$ and v_c can be either $V_{dc}/2$ or $-V_{dc}/2$.

A typical PWM switching waveform for top gate of IGBT is shown in Figure 11.

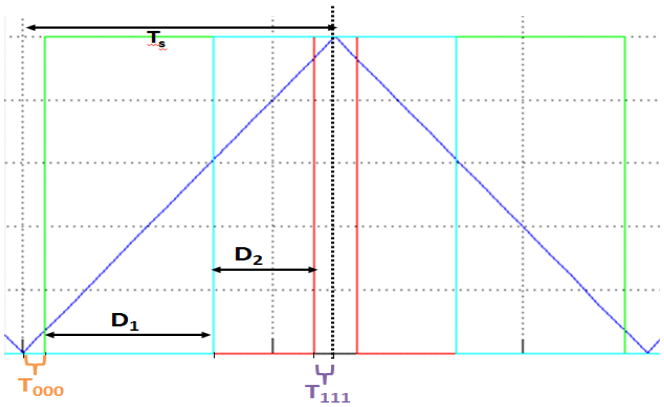


Figure 11. Example: PWM Top Gate Signal

The blue colour line is the counter signal for PWM switching signals. The red, green and cyan colour lines are the switching signals for the top gates of the three legs of the IGBT, low level means the top gate is off and the bottom gate is on.

As marked on the graph, during "T000" period all the bottom gates of the 3 IGBT legs are turned on so the output voltage of $v_a, v_b, \text{and } v_c$ are all $-\mathrm{V_{dc}}/2$. During period "D1" one top gate is on and another two are off, i.e. one of $v_a, v_b, \text{and } v_c$ is $\mathrm{V_{dc}}/2$ and the other two are $-\mathrm{V_{dc}}/2$. Same for "D2" and "T111" periods.

To summarize, with equation (1-1), the instantaneous value of the zero sequence signal is,

$$v_0 = \begin{cases} -V_{dc}/2, \mathrm{t} \in \mathrm{T}_{000} \\ -V_{dc}/6, \mathrm{t} \in D_1 \\ V_{dc}/6, \mathrm{t} \in D_2 \\ V_{dc}/2, \mathrm{t} \in \mathrm{T}_{111} \end{cases}$$

Assume the time for half of the PWM switching cycle is Ts. So the common mode voltage during the 1st half of PWM switching cycle is, $U_0 = \left[-\frac{U_{dc}}{2} \cdot \mathrm{T}_{000} - \frac{U_{dc}}{6} \cdot D_1 + \frac{U_{dc}}{6} \cdot D_2 + \frac{U_{dc}}{2} \cdot \mathrm{T}_{111} \right] / T_s$

(3-34)

3.1.4.2 Two Limits of CMV U_0

As discussed above, if the voltages are normalized to $\frac{U_{dc}}{T_s}$, then equation (3-34) becomes,:

$$U_0 = -\frac{1}{2} T_{000} - \frac{1}{6} D_1 + \frac{1}{6} D_2 + \frac{1}{2} \cdot T_{111}$$

(3-35)

Take note that from here onwards, D1 is duty ratio with respect to Ts, i.e. it is already divided by Ts. Two extreme conditions of U_0 are shown in Figure 12 and are discussed in the following sub-sections.

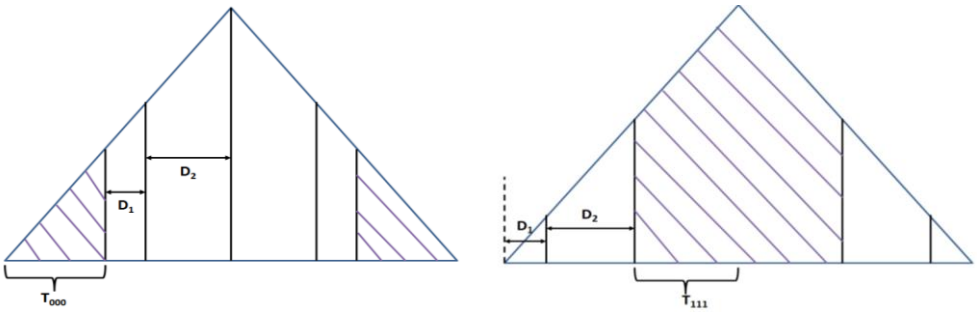
3.1.4.2.1 Minimum value of common mode voltage $U_{0\min}$

Let $T_{000} = 1 - D_1 - D_2$ and $T_{111} = 0$, so the minimum possible value of U_0 is,

$$U_{0\min} = -\frac{1}{2}(1 - D_1 - D_2) - \frac{1}{6} D_1 + \frac{1}{6} D_2 + \frac{1}{2} \cdot 0 = -\frac{1}{2} + \frac{1}{3} D_1 + \frac{2}{3} D_2$$

(3-36)

Substitute the values of D1 and D2 in each sector (refer to section 4.2-4.7) into equation (3-36), we are able to get the minimum value of U_0 for each sector.



(a) (b)

Figure 12. (a) the minimum value and (b) the maximum value of common mode voltage

3.1.4.2.2 Maximum value of common mode voltage $U_{0\max}$

Let $T_{000}=0$ and $T_{111}=1-D_1-D_2$, so the maximum possible value of U_0 is,

$$U_{0\max}=-\frac{1}{2}\cdot 0-\frac{1}{6}D_1+\frac{1}{6}D_2+\frac{1}{2}(1-D_1-D_2)=\frac{1}{2}-\frac{2}{3}D_1-\frac{1}{3}D_2 \quad (3\text{-}37)$$

Substitute the values of D1 and D2 in each sector (refer to section 2.3.2-2.3.7) into equation (3-37), we are able to get the maximum value of U_0 for each sector.

3.1.4.2.3 Summarization

As discussed above, the allowable range of voltage injection is：

$$U_0\in\left[-\frac{1}{2}+\frac{1}{3}D_1+\frac{2}{3}D_2,\quad \frac{1}{2}-\frac{2}{3}D_1-\frac{1}{3}D_2\right] \quad (3\text{-}38)$$

If Vα and Vβ are given, D1 and D2 are fixed for each sector. Thus the zero-sequence voltage injection should be carefully chosen such that it follows the condition in equation (3-38).

3.1.5 Transistor Switching Time With and Without CMV Injection U_0U_0

3.1.5.1 Transistor Switching Time with CMV Injection U_0U_0

Refer to section 2.4 for the calculation of common mode voltage U0 (here, U0 is normalized to Udc and Ti is normalized to Ts), we have:

$$U_0=-\frac{1}{2}T_i-\frac{1}{6}D_1+\frac{1}{6}D_2+\frac{1}{2}\cdot(1-T_i-D_1-D_2)=\frac{1}{2}-T_i-\frac{2}{3}D_1-\frac{1}{3}D_2 \quad (3\text{-}39)$$

$$\Rightarrow T_i=\frac{1}{2}-U_0-\frac{2}{3}D_1-\frac{1}{3}D_2 \quad (3\text{-}40)$$

$$T_j=T_i+D_1=\frac{1}{2}-U_0+\frac{1}{3}D_1-\frac{1}{3}D_2 \quad (3\text{-}41)$$

$$T_k=T_j+D_2=\frac{1}{2}-U_0+\frac{1}{3}D_1+\frac{2}{3}D_2 \quad (3\text{-}42)$$

Equ. (3-40) to (3-42) are the off time of each gate, convert them into on time of each gate, we have:

$$\therefore T_k^{'}=1-T_k=\frac{1}{2}+U_0-\frac{1}{3}D_1-\frac{2}{3}D_2 \quad (3\text{-}43)$$

$$T_j^{'}=1-T_j=\frac{1}{2}+U_0-\frac{1}{3}D_1+\frac{1}{3}D_2=T_k^{'}+D_2 \quad (3\text{-}44)$$

$$T_i^{'}=1-T_i=\frac{1}{2}+U_0+\frac{2}{3}D_1+\frac{1}{3}D_2=T_j^{'}+D_1 \quad (3\text{-}45)$$

3.1.5.2 Transistor Switching Time without CMV Injection U_0U_0

3.1.5.2.1 SVPWM

With the same notation defined in section 2.3.1, we have

$$T_i = \frac{1 - D_1 - D_2}{2} \tag{3-46}$$

$$T_j = T_i + D_1 = \frac{1 + D_1 - D_2}{2} \tag{3-47}$$

$$T_k = T_j + D_2 = \frac{1 + D_1 + D_2}{2} \tag{3-48}$$

Equations (3-46) to (3-48) are the off time of each gate, convert them into on time of each gate, we have:

$$T_k^{'} = 1 - T_k = \frac{1 - D_1 - D_2}{2} \tag{3-49}$$

$$T_j^{'} = 1 - T_j = \frac{1 - D_1 + D_2}{2} = T_k^{'} + D_2 \tag{3-50}$$

$$T_i^{'} = 1 - T_i = \frac{1 + D_1 + D_2}{2} = T_j^{'} + D_1 \tag{3-51}$$

Switching time of each transistor (S1 to S6) is shown in Figure 13.

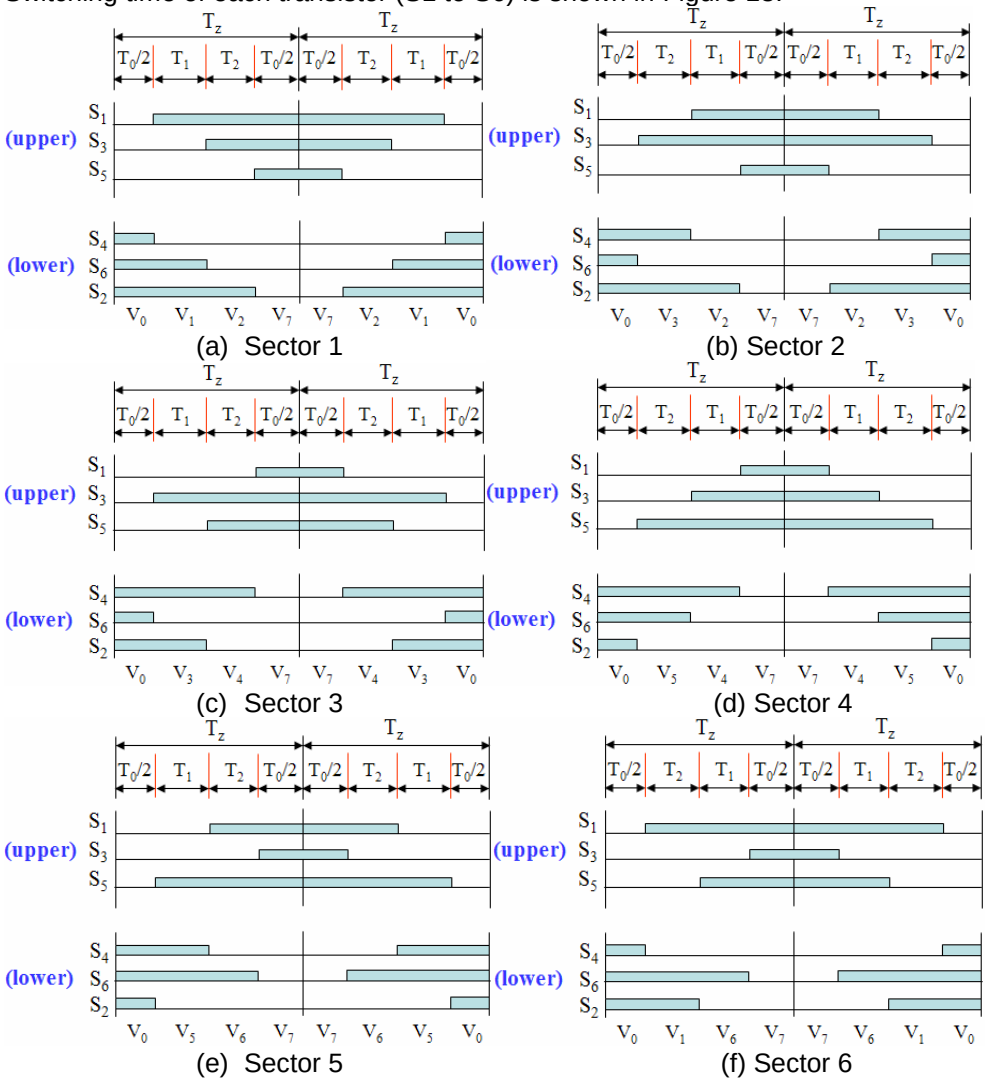


Figure 13. Switching pulse pattern for the three phases in the 6 different sectors

To summarize, for the SVPWM case, we have:

$$T_k = \begin{cases} \dfrac{1-D_1-D_2}{2} & \text{if no voltage injection} \\ \dfrac{1}{2}+U_0-\dfrac{1}{3}D_1-\dfrac{2}{3}D_2 & \text{if there is a voltage injection} \end{cases} \quad (3\text{-}52)$$

$$T_j = T_k + D_2 \quad (3\text{-}53)$$

$$T_i = T_j + D_1 \quad (3\text{-}54)$$

where T_i, T_j and T_k in equations (3-52) to (3-54) are the on time of each gate.

3.1.5.2.1.1 Case 0 (Sector 1)

Substitute the D1 and D2 values obtained in section 2.3 and with equations (3-52) to (3-54), we have:

$$T_3 = \begin{cases} \dfrac{1-D_1-D_2}{2} = \dfrac{1+t_a-t_c}{2} & \text{if no voltage injection} \\ \dfrac{1}{2}+U_0-\dfrac{1}{3}D_1-\dfrac{2}{3}D_2 = \dfrac{1}{2}+U_0+\dfrac{2}{3}t_a-\dfrac{1}{3}t_c & \text{if there is a voltage injection} \end{cases}$$

$$T_2 = T_3 + D_2 = T_3 - t_a$$

$$T_1 = T_2 + D_1 = T_2 + t_c$$

3.1.5.2.1.2 Case 1 (Sector 2)

Substitute the D1 and D2 values obtained in section 2.3 and with equations (3-52) to (3-54), we have:

$$T_3 = \begin{cases} \dfrac{1-D_1-D_2}{2} = \dfrac{1+t_b+t_c}{2} & \text{if no voltage injection} \\ \dfrac{1}{2}+U_0-\dfrac{1}{3}D_1-\dfrac{2}{3}D_2 = \dfrac{1}{2}+U_0+\dfrac{2}{3}t_b+\dfrac{1}{3}t_c & \text{if there is a voltage injection} \end{cases}$$

$$T_1 = T_3 + D_2 = T_3 - t_b$$

$$T_2 = T_1 + D_1 = T_1 - t_c$$

3.1.5.2.1.3 Case 2 (Sector 3)

Substitute the D1 and D2 values obtained in section 2.3 and with equations (3-52) to (3-54), we have:

$$T_1 = \begin{cases} \dfrac{1-D_1-D_2}{2} = \dfrac{1+t_a-t_b}{2} & \text{if no voltage injection} \\ \dfrac{1}{2}+U_0-\dfrac{1}{3}D_1-\dfrac{2}{3}D_2 = \dfrac{1}{2}+U_0+\dfrac{1}{3}t_a-\dfrac{2}{3}t_b & \text{if there is a voltage injection} \end{cases}$$

$$T_3 = T_1 + D_2 = T_1 + t_b$$

$$T_2 = T_3 + D_1 = T_3 - t_a$$

3.1.5.2.1.4 Case 3 (Sector 4)

Substitute the D1 and D2 values obtained in section 2.3 and with equations (3-52) to (3-54), we have:

$$T_1 = \begin{cases} \dfrac{1-D_1-D_2}{2} = \dfrac{1-t_a+t_c}{2} & \text{if no voltage injection} \\ \dfrac{1}{2}+U_0-\dfrac{1}{3}D_1-\dfrac{2}{3}D_2 = \dfrac{1}{2}+U_0-\dfrac{1}{3}t_a+\dfrac{2}{3}t_c & \text{if there is a voltage injection} \end{cases}$$

$$T_2 = T_1 + D_2 = T_1 - t_c$$

$$T_3 = T_2 + D_1 = T_2 + t_a$$

3.1.5.2.1.5 Case 4 (Sector 5)

Substitute the D1 and D2 values obtained in section 2.3 and with equations (3-52) to (3-54), we have:

$$T_2 = \begin{cases} \dfrac{1-D_1-D_2}{2} = \dfrac{1-t_b-t_c}{2} & if\ no\ voltage\ injection \\ \dfrac{1}{2}+U_0-\dfrac{1}{3}D_1-\dfrac{2}{3}D_2 = \dfrac{1}{2}+U_0-\dfrac{1}{3}t_b-\dfrac{2}{3}t_c & if\ there\ is\ a\ voltage\ injection \end{cases}$$

$$T_1 = T_2 + D_2 = T_2 + t_c$$
$$T_3 = T_1 + D_1 = T_1 + t_b$$

3.1.5.2.1.6 Case 5 (Sector 6)

Substitute the D1 and D2 values obtained in section 2.3 and with equations (3-52) to (3-54), we have:

$$T_2 = \begin{cases} \dfrac{1-D_1-D_2}{2} = \dfrac{1-t_a+t_b}{2} & if\ no\ voltage\ injection \\ \dfrac{1}{2}+U_0-\dfrac{1}{3}D_1-\dfrac{2}{3}D_2 = \dfrac{1}{2}+U_0-\dfrac{2}{3}t_a+\dfrac{1}{3}t_b & if\ there\ is\ a\ voltage\ injection \end{cases}$$

$$T_3 = T_2 + D_2 = T_2 + t_a$$
$$T_1 = T_3 + D_1 = T_3 - t_b$$

3.1.5.2.2 DPWM1

From Figure 8, we have:

$$if \quad \zeta_0 = 0 \Rightarrow T_{000} = 0$$
$$\Rightarrow T_i = 0$$
$$T_j = T_i + D_1 = D_1$$
$$T_k = T_j + D_2 = D_1 + D_2$$

Above are the off time of each gate, convert them into on time of each gate, we have:

$$\Rightarrow T_i^{'} = 1 - T_i = 1$$
$$T_j^{'} = 1 - T_j = 1 - D_1$$
$$T_k^{'} = 1 - T_k = 1 - D_1 - D_2$$

(3-55)

$$if \quad \zeta_7 = 0 \Rightarrow T_{111} = 0$$
$$\Rightarrow T_k = 1$$
$$T_j = T_k - D_2 = 1 - D_2$$
$$T_i = T_j - D_1 = 1 - D_1 - D_2$$

Above are the off time of each gate, convert them into on time of each gate, we have:

$$\Rightarrow T_k^{'} = 1 - T_k = 0$$
$$T_j^{'} = 1 - T_j = D_2$$
$$T_i^{'} = 1 - T_i = D_1 + D_2$$

(3-56)

To summarize, we have:

$$if \quad \zeta_0 = 0 \quad \Rightarrow \quad \begin{matrix} T_i = 1 \\ T_j = 1 - D_1 \\ T_k = 1 - D_1 - D_2 \end{matrix} \quad , \quad if \quad \zeta_7 = 0 \quad \Rightarrow \quad \begin{matrix} T_k = 0 \\ T_j = D_2 \\ T_i = D_1 + D_2 \end{matrix}$$

(3-57)

3.1.5.2.2.1 Sector 0

$\because \zeta_0 = 0$

From section 2.3, we have $D_1 = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_c$ and $D_2 = V_\beta = -t_a$, from Figure 13 and using equation (3-57):

$$\Rightarrow \quad \begin{matrix} T_1 = 1 \\ T_2 = 1 - D_1 = 1 - t_c \\ T_3 = 1 - D_1 - D_2 = 1 + t_a - t_c \end{matrix}$$

(3-58)

3.1.5.2.2.2 Sector 1

$\because \zeta_7 = 0$

From section 2.3, we have $D_1 = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_c$ and $D_2 = V_\beta = -t_a$, from Figure 13 and using equation (3-57):

$$\Rightarrow \quad \begin{matrix} T_3 = 0 \\ T_2 = D_2 = -t_a \\ T_1 = D_1 + D_2 = t_c - t_a \end{matrix}$$

(3-59)

3.1.5.2.2.3 Sector 2

$\because \zeta_7 = 0$

From section 2.3, we have $D_1 = -\frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_c$ and $D_2 = \frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_b$, from Figure 13 and using equation (3-57):

$$\Rightarrow \quad \begin{matrix} T_3 = 0 \\ T_1 = D_2 = -t_b \\ T_2 = D_1 + D_2 = -t_b - t_c \end{matrix}$$

(3-60)

3.1.5.2.2.4 Sector 3

$\because \zeta_0 = 0$

From section 2.3, we have $D_1 = -\frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_c$ and $D_2 = \frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_b$, from Figure 13 and using equation (3-57):

$$\Rightarrow \quad \begin{matrix} T_2 = 1 \\ T_1 = 1 - D_1 = 1 + t_c \\ T_3 = 1 - D_1 - D_2 = 1 + t_b + t_c \end{matrix}$$

(3-61)

3.1.5.2.2.5 Sector 4

$\because \zeta_0 = 0$

From section 2.3, we have $D_1 = V_\beta = -t_a$ and,

$D_2 = -\frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_b$

, from Figure 13 and using equation (3-57):

$$\begin{aligned} & T_2 = 1 \\ \Rightarrow \quad & T_3 = 1 - D_1 = 1 + t_a \\ & T_1 = 1 - D_1 - D_2 = 1 + t_a - t_b \end{aligned}$$

(3-62)

3.1.5.2.2.6 Sector 5

$\because \zeta_7 = 0$

From section 2.3, we have $D_1 = V_\beta = -t_a$ and,

$D_2 = -\frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_b$, from Figure 13 and using equation (3-57):

$$\begin{aligned} & T_1 = 0 \\ \Rightarrow \quad & T_3 = D_2 = t_b \\ & T_2 = D_1 + D_2 = -t_a + t_b \end{aligned}$$

(3-63)

3.1.5.2.2.7 Sector 6

$D_2 = -\frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_c$ $\because \zeta_7 = 0$

From section 2.3, we have $D_1 = -V_\beta = t_a$ and

, from Figure 13 and using equation (3-57):

$$\begin{aligned} & T_1 = 0 \\ \Rightarrow \quad & T_2 = D_2 = -t_c \\ & T_3 = D_1 + D_2 = t_a - t_c \end{aligned}$$

(3-64)

3.1.5.2.2.8 Sector 7

$\because \zeta_0 = 0$

From section 2.3, we have $D_1 = -V_\beta = t_a$ and

$D_2 = -\frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_c$, from Figure 13 and using equation (3-57):

$$\begin{aligned} & T_3 = 1 \\ \Rightarrow \quad & T_2 = 1 - D_1 = 1 - t_a \\ & T_1 = 1 - D_1 - D_2 = 1 - t_a + t_c \end{aligned}$$

(3-65)

3.1.5.2.2.9 Sector 8

$D_2 = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_c$ $\because \zeta_0 = 0$

From section 2.3, we have $D_1 = -\frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_b$ and

, from Figure 13 and using equation (3-57):

$$T_3 = 1$$
$$\Rightarrow \quad T_1 = 1 - D_1 = 1 - t_b$$
$$T_2 = 1 - D_1 - D_2 = 1 - t_b - t_c$$

(3-66)

3.1.5.2.2.10 Sector 9

$D_2 = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_c \quad \because \zeta_7 = 0$

From section 2.3, we have $D_1 = -\frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta = t_b$ and

, from Figure 13 and using equation (3-57):

$$T_2 = 0$$
$$\Rightarrow \quad T_1 = D_2 = t_c$$
$$T_3 = D_1 + D_2 = t_b + t_c$$

(3-67)

3.1.5.2.2.11 Sector 10

$D_2 = -V_\beta = t_a \quad \because \zeta_7 = 0$

From section 2.3, we have $D_1 = \frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_b$ and

, from Figure 13 and using equation (3-57):

$$T_2 = 0$$
$$\Rightarrow \quad T_3 = D_2 = t_a$$
$$T_1 = D_1 + D_2 = t_a - t_b$$

(3-68)

3.1.5.2.2.12 Sector 11

$D_2 = -V_\beta = t_a \quad \because \zeta_0 = 0$

From section 2.3, we have $D_1 = \frac{\sqrt{3}}{2}V_\alpha + \frac{1}{2}V_\beta = -t_b$ and

, from Figure 13 and using equation (3-57):

$$T_1 = 1$$
$$\Rightarrow \quad T_3 = 1 - D_1 = 1 + t_b$$
$$T_2 = 1 - D_1 - D_2 = 1 - t_a + t_b$$

(3-69)

3.1.5.2.3 DPWM0

The discussion of general case of DPWM0 is same as for DPWM1, thus equation (3-57) is also valid for DPWM0.
According to
Figure 14, DPWM0 has the same sector definition as for SVPWM, thus it has the same duty cycle values for each sector as in SVPWM case.

Combining equation (3-57) and substitute DI, D2 values obtained from section 3.1.3 for each of the 6 sectors for DPWM0, we are able to determine the switching time of the transistors.

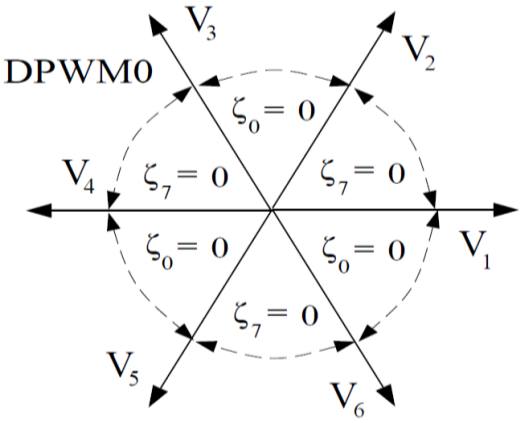


Figure 14. Sector definition for DPWM0

The results are:
case 0,
T1 = - ta + tc;
T2 = - ta;
T3 = 0;
case 1,
T1 = 1 + tc;
T2 = 1;
T3 = 1 + tb + tc;
case 2,
T1 = 0;
T2 = - ta + tb;
T3 = tb;
case 3,
T1 = 1 - ta + tc;
T2 = 1 - ta;
T3 = 1;
case 4,
T1 = tc;
T2 = 0;
T3 = tb + tc;
case 5,
T1 = 1;
T2 = 1 - ta + tb;
T3 = 1 + tb;

3.1.5.2.4 DPWMMIN

For DPWMMIN, the reference signal with the minimum value defines the zero sequence. In each sector, the phase with minimum current shall be tied to low without switching. Thus T111 is always 0, which means $\zeta_7 = 0$ is true for all the six sectors. The discussion of general case of DPWMMIN is same as for DPWM1, thus equation (3-57) is also valid for DPWMMIN.

According to Figure 15, DPWMMIN is same as DPWM0 for sector 1, 3 and 5, but different for sector 2, 4 and 6. Hence, the code for case 0, 2 and 4 is the same as for DPWM0 and we only need to analyse cases 1, 3 and 5.

Same as DPWM0, DPWMMIN also have the same sector definition as for SVPWM, thus it has the same duty cycle values for each sector as in SVPWM case. Combining equation (3-57) and substitute DI, D2 values obtained from section 3.1.3 for sectors 2, 4 and 6 for DPWMMIN, we are able to determine the switching time of the transistors.

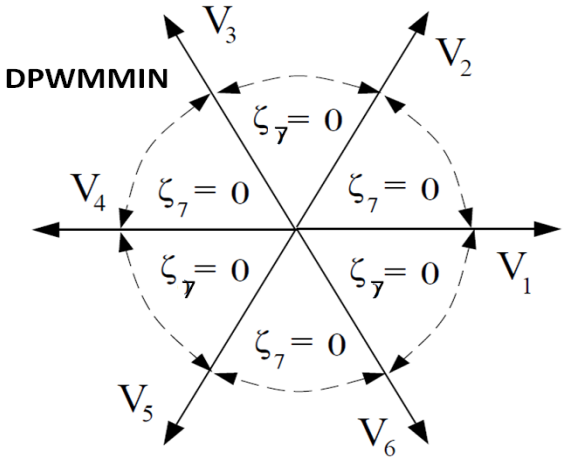


Figure 15. Sector definition for DPWMMIN

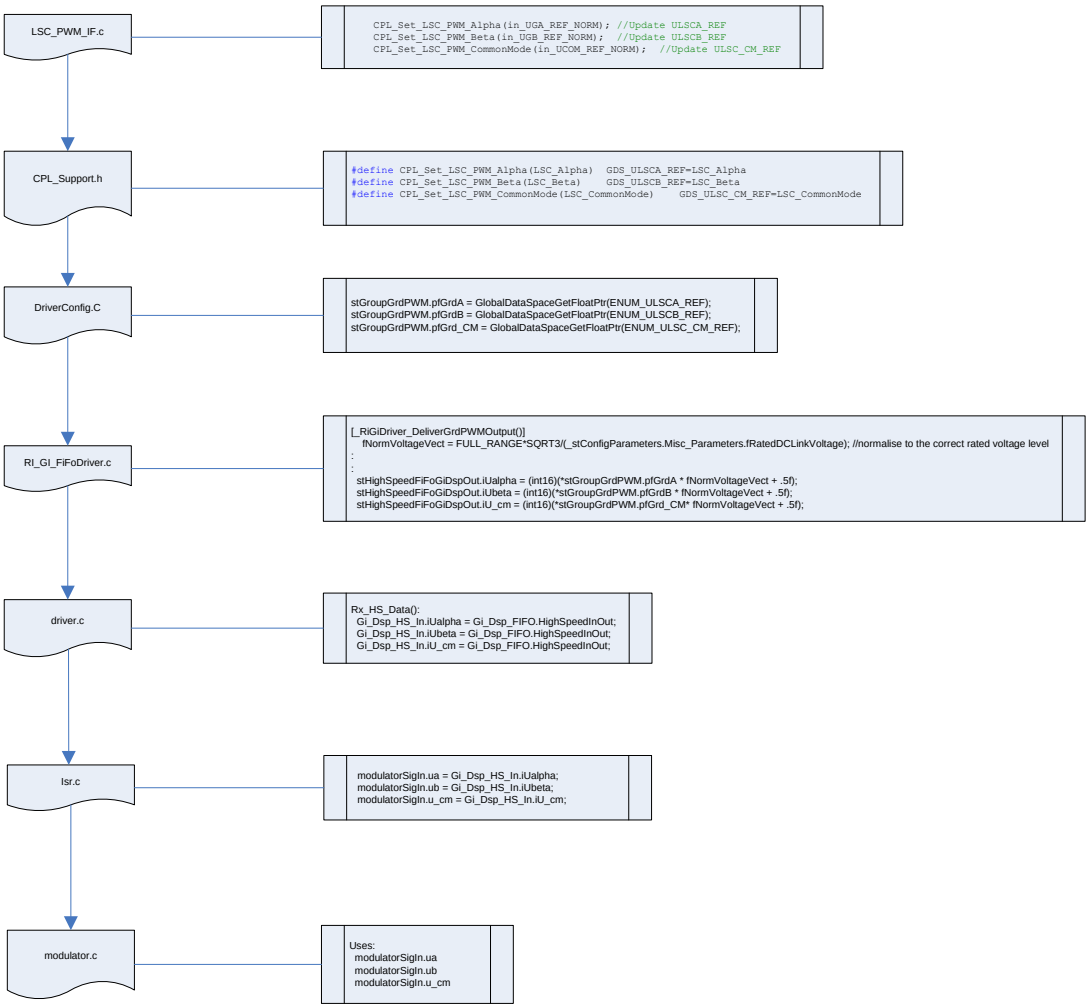
The results are:

```
case 0,
    T1 = - ta + tc;
    T2 = - ta;
    T3 = 0;
case 1,
    T1 = - tb;
    T2 = - tb - tc;
    T3 = 0;
case 2,
    T1 = 0;
    T2 = - ta + tb;
    T3 = tb;
case 3,
    T1 = 0;
    T2 = - tc;
    T3 = ta - tc;
case 4,
    T1 = tc;
    T2 = 0;
    T3 = tb + tc;
case 5,
    T1 = ta - tb;
    T2 = 0;
    T3 = ta;
```

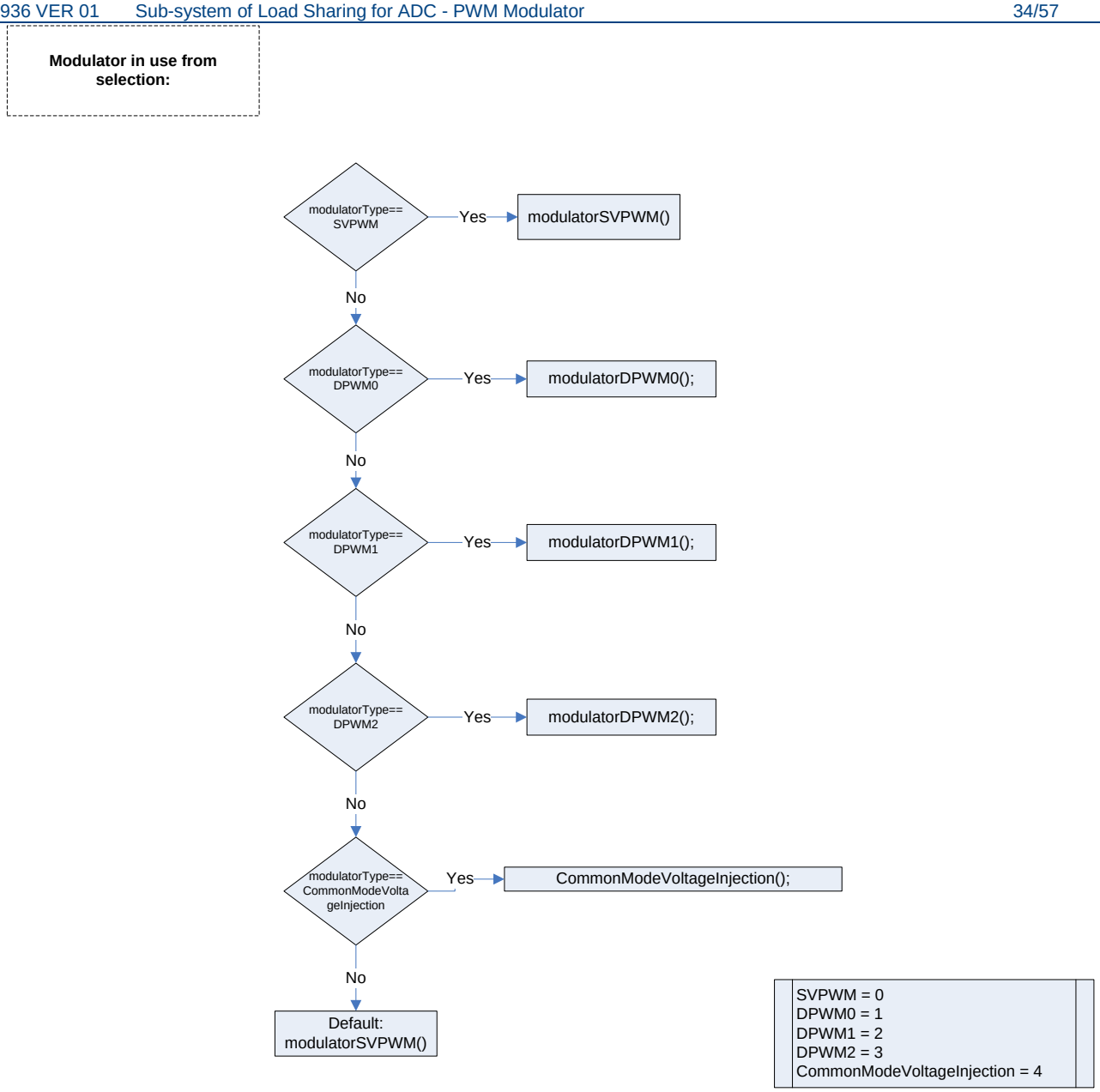
3.1.6 Software flow chart for PWM

The reference is passed down from Application layer all the way down to fifo then to GI-DSP. This flow is shown in the figure 16. For information on how these reference is being derived, please refer reference 1. For software aspect of it, refer to reference 2.

Data Flow from Application Layer LSC_PWM_IF all the way to modulator



16 Flowchart of passing the PWM reference, Alpha, Beta and Common-mode Voltage



17: flowchart on which modulator used

For the code implementation of common mode voltage injection, please refer to section 3.2.1.2.

3.2 Design Verification

3.2.1 CMV injection

3.2.1.1 Simulation Results

We developed the PWM Block to test the correctness of the above formulas. The block diagram is shown in Figure 18.

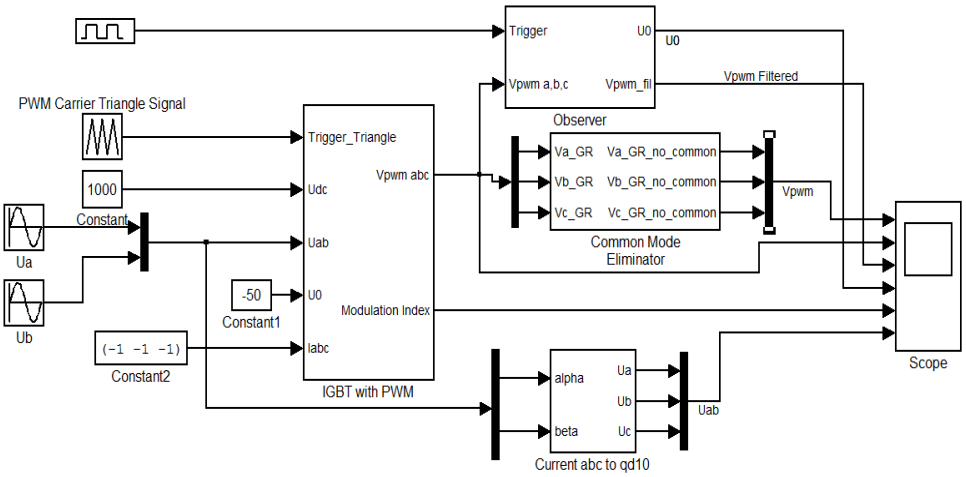


Figure 18. The PWM Block Diagram

The top U0 signal is the signal we get from equation (1-1), it is the average voltage of the center point of the PWM output voltages. The Vpwm filtered is the 3-phase output voltage. The actual waveform is shown in Figure 19.

The 1st waveform is the actual 3-phase PWM output voltage. The 2nd waveform is the average voltage of v_0. The 3rd waveform is the modulation index and the 4th waveform is the reference 3-phase voltage.

From the waveform we could see that the actual PWM output voltage is the same as the reference voltage. The average voltage U0 is also the same as the reference level which is -50. Thus, the above discussion and calculation of duty cycles are verified.

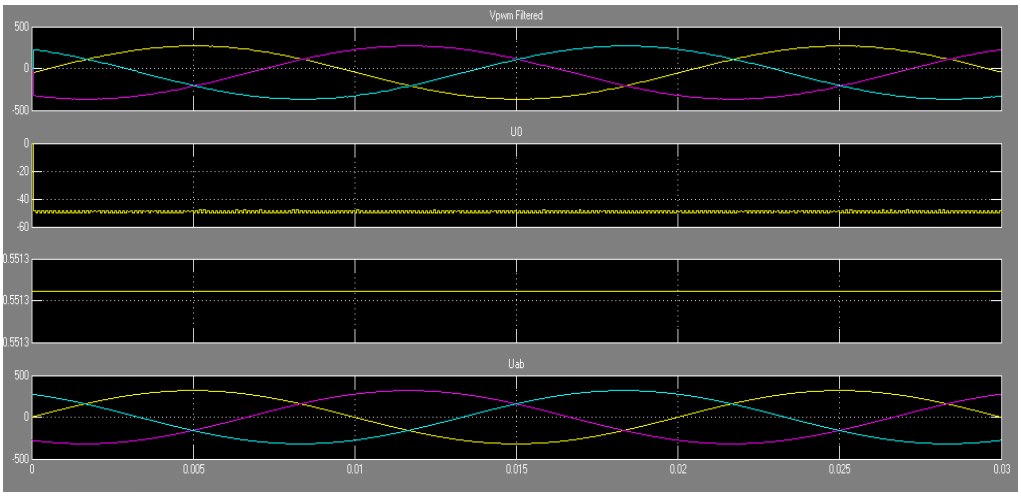


Figure 19. Waveform of V0 and Va, Vb, Vc.

3.2.1.2 Implementation in C Code

Below is the code for common mode voltage injection in C code:

```
static void CommonModeVoltageInjection (void)
{
  int32_t temp;
  int32_t duty1;
  int32_t duty2;
  int32_t duty1_2Third;
  int32_t duty2_2Third;
  int32_t duty1_4Third;
  int32_t duty2_4Third;
  int32_t U0min, U0max, U0_limited;

  //->Transformation
  modulatorSig.ta = -modulatorSig.ub;    //ta = - ub
  temp            =  modulatorSig.ua;
  temp            =  56756 * temp;
  temp            =  temp >> 15;
```

```
//tb = -0.5 * ub - sqrt(3)/2 * ua
  modulatorSig.tb =  (int16_t) (( ((int32_t) modulatorSig.ta) - temp ) >> 1);
//tb = -0.5 * ub + sqrt(3)/2 * ua
  modulatorSig.tc =  (int16_t) (( ((int32_t) modulatorSig.ta) + temp ) >> 1);
//divide uCom by sqrt3
  modulatorSig.u_cm = (int16_t) (((int32_t)modulatorSig.u_cm * 18918 )>>15);
  //<-Transformation

  //->Find sector
  modulatorN6S();
  //<-Find sector

  //->Calculate compare values
  switch(modulatorSig.n)
  {
    case 0: //000 - 100 - 110 - 111 - 110 - 100 - 000 //bingl: mc:T3, mb:T2 and ma: T1
    {
              duty1=modulatorSig.tc; //D1=tc
      duty2=-modulatorSig.ta; //D2=-ta
    }
    break;
    case 1: //000 - 010 - 110 - 111 - 110 - 010 - 000
    {
              duty1=-modulatorSig.tc; //D1=-tc
      duty2=-modulatorSig.tb; //D2=-tb
    }
    break;
    case 2: //000 - 010 - 011 - 111 - 011 - 010 - 000
    {
      duty1=- modulatorSig.ta; //D1=-ta
      duty2=modulatorSig.tb; //D2=tb
    }
    break;
    case 3: //000 - 001 - 011 - 111 - 011 - 001 - 000
    {
      duty1=modulatorSig.ta; //D1=ta
      duty2=-modulatorSig.tc; //D2=-tc
    }
    break;
    case 4: //000 - 001 - 101 - 111 - 101 - 001 - 000
    {
              duty1=modulatorSig.tb; //D1=tb
      duty2=modulatorSig.tc; //D2=tc
    }
    break;
    case 5: //000 - 100 - 101 - 111 - 101 - 100 - 000
    {
              duty1=-modulatorSig.tb; //D1=-tb
      duty2=modulatorSig.ta; //D2=ta
    }
    break;
    default:
      duty1=0;
              duty2=0;
    break;
  }
//  temp = duty1*2*10923;
  duty1_2Third = ((duty1*21845) >> 15);

//  temp = duty1*4*10923;
  duty1_4Third = ((duty1*21845) >> 14);

//  temp = duty2*2*10923;
  duty2_2Third = ((duty2*21845) >> 15);

//  temp = duty2 * 4*10923;
  duty2_4Third = (duty2*21845 >> 14);




  //<-Calculate max and min common mode voltage values
//  U0min=(-16384 + duty1*2/3 + duty2*4/3)>> 1; //U0mim=-0.5+D1*1/3+D2*2/3
//  U0max=(16384 - duty1*4/3 - duty2*2/3)>> 1; //U0mim=0.5-D1*2/3-D2*1/3

  U0min=(-16384 + duty1_2Third + duty2_4Third)>> 1; //U0mim=-0.5+D1*1/3+D2*2/3
  U0max=(16384 - duty1_4Third - duty2_2Third)>> 1; //U0mim=0.5-D1*2/3-D2*1/3

  //<-Limit the U0 value to within the allowable range
  if (modulatorSig.u_cm>U0max)
              U0_limited=U0max;
```

```
  else if (modulatorSig.u_cm<U0min)
              U0_limited=U0min;
  else U0_limited=modulatorSig.u_cm;

  //->Calculate compare values

  switch(modulatorSig.n)
  {
    case 0: //000 - 100 - 110 - 111 - 110 - 100 - 000
    {
      modulatorSig.mc = (int16_t)((16384 + 2*U0_limited - duty1_2Third - duty2_4Third) >> 1);
//equals 0.5+U0-D1*1/3-D2*2/3
      modulatorSig.mb = -modulatorSig.ta + modulatorSig.mc; //equals mc+D2
      modulatorSig.ma =  modulatorSig.tc + modulatorSig.mb; //equals mb+D1
    }
    break;
    case 1: //000 - 010 - 110 - 111 - 110 - 010 - 000
    {
      modulatorSig.mc = (int16_t)((16384 + 2*U0_limited - duty1_2Third - duty2_4Third) >> 1);
//equals 0.5+U0-D1*1/3-D2*2/3
      modulatorSig.ma = -modulatorSig.tb + modulatorSig.mc; //equals mc+D2
      modulatorSig.mb = -modulatorSig.tc + modulatorSig.ma; //equals ma+D1
    }
    break;
    case 2: //000 - 010 - 011 - 111 - 011 - 010 - 000
    {
      modulatorSig.ma = (int16_t)((16384 + 2*U0_limited - duty1_2Third - duty2_4Third) >> 1);
//equals 0.5+U0-D1*1/3-D2*2/3
      modulatorSig.mc =  modulatorSig.tb + modulatorSig.ma; //equals ma+D2
      modulatorSig.mb = -modulatorSig.ta + modulatorSig.mc; //equals mc+D1
    }
    break;
    case 3: //000 - 001 - 011 - 111 - 011 - 001 - 000
    {
      modulatorSig.ma = (int16_t)((16384 + 2*U0_limited - duty1_2Third - duty2_4Third) >> 1);
//equals 0.5+U0-D1*1/3-D2*2/3
      modulatorSig.mb = -modulatorSig.tc + modulatorSig.ma; //equals ma+D2
      modulatorSig.mc =  modulatorSig.ta + modulatorSig.mb; //equals mb+D1
    }
    break;
    case 4: //000 - 001 - 101 - 111 - 101 - 001 - 000
    {
      modulatorSig.mb = (int16_t)((16384 + 2*U0_limited - duty1_2Third - duty2_4Third) >> 1);
//equals 0.5+U0-D1*1/3-D2*2/3
      modulatorSig.ma = modulatorSig.tc + modulatorSig.mb; //equals mb+D2
      modulatorSig.mc = modulatorSig.tb + modulatorSig.ma; //equals ma+D1
    }
    break;
    case 5: //000 - 100 - 101 - 111 - 101 - 100 - 000
    {
      modulatorSig.mb = (int16_t)((16384 + 2*U0_limited - duty1_2Third - duty2_4Third) >> 1);
//equals 0.5+U0-D1*1/3-D2*2/3
      modulatorSig.mc =  modulatorSig.ta + modulatorSig.mb; //equals mb+D2
      modulatorSig.ma = -modulatorSig.tb + modulatorSig.mc; //equals mc+D1
    }
    break;
    default:
    break;
  }
  if(modulatorSig.ma<0)
    modulatorSig.ma = 0;
  if(modulatorSig.mb<0)
    modulatorSig.mb = 0;
  if(modulatorSig.mc<0)
    modulatorSig.mc = 0;

 }
```

3.2.1.3 Debugging

We define uua, uub, uuc and uu0 for debugging purpose.
Let's take sector 1 as an example:
When at (100), we have:

$$u_a = \frac{2}{3} D_1$$

When at (110), we have:

$$u_a = \frac{1}{3} D_2$$

Thus, $u_a = \frac{2}{3} D_1 + \frac{1}{3} D_2 = \frac{1}{3}(2 \cdot D_1 + D_2) = \frac{1}{3}[D_1 + (D_1 + D_2)]$

$$but \quad \sin ce \quad D_1 = \frac{m_a - m_b}{tcount} \text{ and } D_1 + D_2 = \frac{m_a - m_c}{tcount},$$

We have:

$$u_a = \frac{1}{3} \cdot \frac{(m_a - m_b) + (m_a - m_c)}{tcount} = \frac{2 \cdot m_a - m_b - m_c}{3 \cdot tcount} = \frac{3 \cdot m_a - (m_a + m_b + m_c)}{3 \cdot tcount}$$

$$= \frac{3 \cdot m_a - temp}{3 \cdot tcount}$$

Similarly, we can get $u_b = \frac{3 \cdot m_b - temp}{3 \cdot tcount}$ and $u_c = \frac{3 \cdot m_c - temp}{3 \cdot tcount}$

From equation (3-39)

$$U_0 = -\frac{1}{2} T_1 - \frac{1}{6} D_1 + \frac{1}{6} D_2 + \frac{1}{2} \cdot (1 - T_1 - D_1 - D_2) = \frac{1}{2} - T_1 - \frac{2}{3} D_1 - \frac{1}{3} D_2$$

$$\Rightarrow T_1 = \frac{1}{2} - U_0 - \frac{2}{3} D_1 - \frac{1}{3} D_2$$

Convert it into ON time of each transistor, we have:

$$T_1' = 1 - T_1 = \frac{1}{2} + U_0 + \frac{2}{3} D_1 + \frac{1}{3} D_2$$

$$\Rightarrow U_0 = T_1' - \frac{1}{2} - \frac{2}{3} D_1 - \frac{1}{3} D_2 = \frac{6 \cdot m_a - 3 \cdot tcount - 4 \cdot (m_a - m_b) - 2 \cdot (m_b - m_c)}{6 \cdot tcount}$$

$$= \frac{2m_a + 2m_b + 2m_c - 3 \cdot tcount}{6 \cdot tcount} = \frac{2 \cdot temp - 3 \cdot tcount}{6 \cdot tcount}$$

Below is the debugging code. Please note that the coefficient 28379=sqrt(3)*16384 is used to scale to timer value.

```
//->Calculate u0, ua, ub & uc reference from timer compare values for debug
  temp  = (int32_t) modulatorSig.maScaled;
  temp += (int32_t) modulatorSig.mbScaled;
  temp += (int32_t) modulatorSig.mcScaled;

modulatorSig.uua = (int16_t) ((28379*(3*((int32_t) modulatorSig.maScaled) - temp))/(3*((int32_t)
modulatorPar.tcount)));
modulatorSig.uub = (int16_t) ((28379*(3*((int32_t) modulatorSig.mbScaled) - temp))/(3*((int32_t)
modulatorPar.tcount)));
modulatorSig.uuc = (int16_t) ((28379*(3*((int32_t) modulatorSig.mcScaled) - temp))/(3*((int32_t)
modulatorPar.tcount)));

modulatorSig.uu0 = (int16_t) ((28379*(2*temp - 3*((int32_t) modulatorPar.tcount)))/(6*((int32_t)
modulatorPar.tcount)));
//<-Calculate u0, ua, ub & uc reference from timer compare values for debug
```

3.2.2 DPWMMIN

3.2.2.1 Simulation Results

The set up in Figure 18 is also used for simulation for DPWMMIN.

The Vpwm filtered is the 3-phase output voltage. The actual waveform is shown in Figure 20.

The 1st waveform is the input signal to the PWM, the 2nd waveform is the actual 3-phase PWM output voltage. The 3rd waveform is the average voltage of v_0 . The 4th waveform is the modulation index and the 5th waveform is the reference 3-phase voltage.

From the waveform we could see that the actual PWM output voltage is generally lower than the reference voltage by 200V. Also when the reference voltage goes closer to its maximum value, the actual PWM output voltage indeed drops. This verified that the common mode voltage in existing mode is same as DPWMMIN defined in literature as shown in Figure 21.

Below is the simulation result.

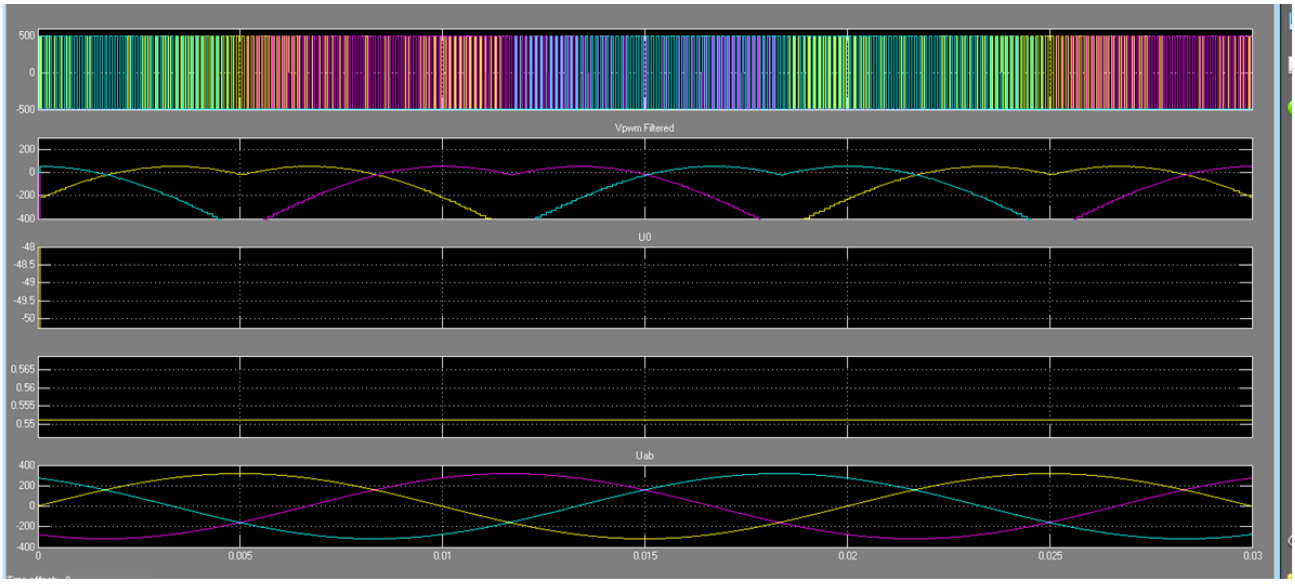


Figure 20. Waveform of output of DPWMMIN

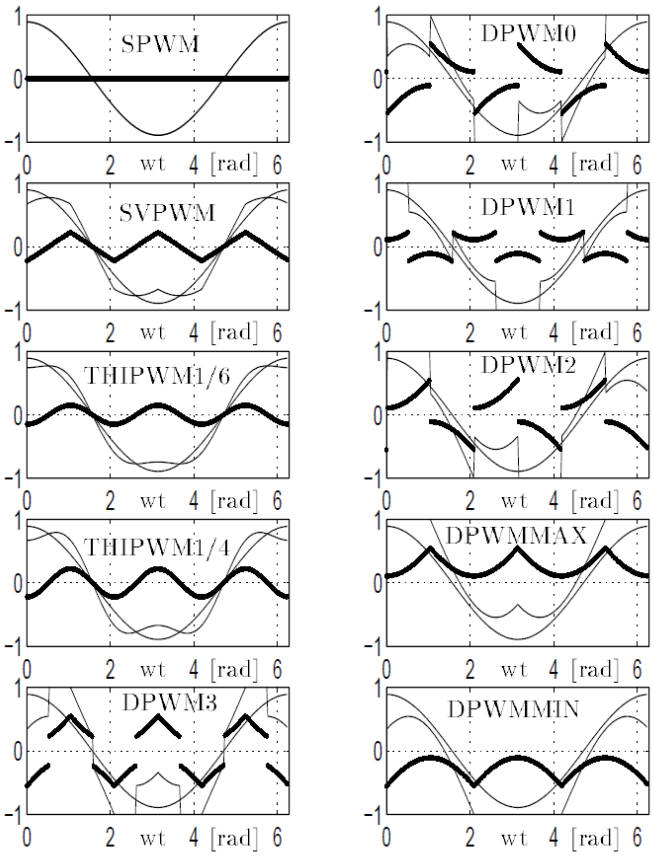


Figure 21. Modulation waveform s of the modern PWM methods (Mi=0.7)

In the above figure, the dark line is the common mode voltage in each PWM scheme. DPWMMIN has non-uniform thermal stress on switching device; the lower leg has higher loss.

3.2.2.2 Implementation in C Code

```
static void modulatorDPWMMIN( void )
{
  int32_t temp;
  //->Transformation
  //ta = -      ub
  //tb = -0.5 * ub - sqrt(3)/2 * ua
  //tb = -0.5 * ub + sqrt(3)/2 * ua
  modulatorSig.ta = -modulatorSig.ub;
  temp            =  modulatorSig.ua;
  temp            =  56756 * temp;
  temp            =  temp >> 15;
  modulatorSig.tb =  (int16_t) (( ((int32_t) modulatorSig.ta) - temp ) >> 1);
  modulatorSig.tc =  (int16_t) (( ((int32_t) modulatorSig.ta) + temp ) >> 1);
  //<-Transformation
  //->Find sector
  modulatorN6S();
  //<-Find sector
  //->Calculate compare values
  switch(modulatorSig.n)
  {
    case 0: //000 - 100 - 110 - 100 - 000
    {
      modulatorSig.ma = -modulatorSig.ta + modulatorSig.tc;
      modulatorSig.mb = -modulatorSig.ta;
      modulatorSig.mc = 0;
    }
    break;
    case 1: //010 - 110 - 000 - 110 - 010
    {
      modulatorSig.ma = - modulatorSig.tb;
      modulatorSig.mb = - modulatorSig.tb - modulatorSig.tc;
      modulatorSig.mc = 0;
    }
    break;
    case 2: //000 - 010 - 011 - 010 - 000
    {
      modulatorSig.ma = 0;
      modulatorSig.mb = modulatorSig.tb - modulatorSig.ta;
      modulatorSig.mc = modulatorSig.tb;
    }
    break;
    case 3: //001 - 011 - 000 - 011 - 001
    {
      modulatorSig.ma = 0;
      modulatorSig.mb = - modulatorSig.tc;
      modulatorSig.mc = modulatorSig.ta - modulatorSig.tc;
    }
    break;
    case 4: //000 - 001 - 101 - 001 - 000
    {
      modulatorSig.ma = modulatorSig.tc;
      modulatorSig.mb = 0;
      modulatorSig.mc =  modulatorSig.tb + modulatorSig.tc;
    }
    break;
    case 5: //100 - 101 - 000 - 101 - 100
    {
      modulatorSig.ma = modulatorSig.ta - modulatorSig.tb;
```

```
            modulatorSig.mb = 0;
            modulatorSig.mc = modulatorSig.ta;
          }
          break;
          default:
          break;
        }
        //<-Calculate compare values
}
```

4. DFMEA for PWM Modulator

The PWM modulator is purely algorithm. It is either working or not working. Thus, the failure mode of PWM modulator is only limited to software failure. Please refer to the attached file:

DFMEA_Sub-system of Load Sharing for A

5. DVPL for PWM Modulator

Please refer to the attached file:

DVPL_Sub-system of Load Sharing for ADC

6. DVPR for PWM Modulator

6.1 Background

6.1.1 Purpose

The purpose of this section is to demonstrated full fulfilment to the Requirement specification stated in section 2 in this document.

6.2 Test Specification

6.2.1 Test setup

Oscilloscope with 4 probes	1pcs
Modified Vestas Power Controller (CT360)	1pcs
55kw test bench	1pcs

6.2.2 Measurement system

Persistence measurement which do not exceed 1 us, for a duration of 10s.

6.2.2.1 Sensor list

Not applicable.

6.2.2.2 Test procedure and success criteria

Attention: Please do note for all the tests below, we could only use one string. And we only tested at VPC level, it is not tested in test bench.

6.2.2.2.1 Test cases # 01-10 for CMV Injection, when Ucom_ref is within maximum Ucom and minimum Ucom Limits

Software team to hardcode those parameters at VPC line side:

a. Udc=700V,
b. $U_\alpha = A \cdot \cos(\omega t)$,
   $U_\beta = A \cdot \sin(\omega t)$
   where
   $\omega = 2\pi f, \quad f = 50Hz, \quad and\ A \quad should \quad be \quad small, \quad let\ A = 210V$
c. Comon Mode modulator is enabled.
d. Setup the VPC and using the Oscilloscope to detect the bottom leg phase A, B, and C voltages (Ua, Ub and Uc) as shown in Figure 22.
e. The exact values of U_α and $U\beta$ for each test case are shown in Table 2.
f. The expected duty cycle of each phase are shown in Table 2.
g. Using the oscilloscope math function to calculate and display Ucom based on 3 phase PWM signal. The expected Ucom should be same as Ucom_ref.
h. The test cases are success if the measured da, db and dc are same as the expected values shown in Table 2, and the measured Ucom is same as the Ucom_ref.

Table 2. Test cases for CMV Injection, when Ucom_ref is within maximum Ucom and minimum Ucom Limits

Tc #	Reference	Ucom_ ref	Angle (°C)	Uα	Uβ	U0min	U0max	Expected da(phase A duty cycle) or T1	Expected db(phase B duty cycle) or T2	Expected dc(phase C duty cycle) or T3
01	DVPL-01 PWM modulator is able to generate the required common mode voltage	50	0	210	0	-0.35	0.2	0.871428571	0.421428571	0.421428571
02		50	45	148.492426	148.49242	-0.210222253	0.28786 7963	0.783560609	0.649074281	0.281650825
03		50	80	36.46612224	206.80963	-0.218092211	0.27018 6672	0.623523032	0.8012419	0.289520783
04		50	100	-36.46611115	206.80963	-0.270186661	0.21809 2217	0.519334127	0.853336355	0.341615233
05		50	180	-210	1.125 E-05	-0.2	0.34999 9986	0.271428571	0.721428585	0.721428558
06		20	0	210	0	0	0.2	0.828571429	0.378571429	0.378571429
07		20	20	197.3354508	71.824229	20	0.21809 2213	0.810479215	0.476476974	0.298758097
08		20	40	160.8693347	134.9854	40	0.27018 6665	0.758384764	0.580665878	0.246663644

09		20	110	-71.82422364	197.33545	110	0.207657676	0.425965395	0.824013753	0.335735138
10		20	140	-160.8693274	134.9854	140	0.218092209	0.298758104	0.810479219	0.476476963

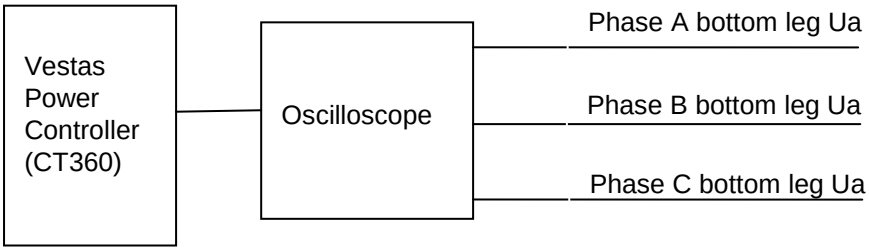


Figure 22. VPC test setup for PWM Modulator

6.2.2.2.2 Test cases 11-18 for CMV Injection, when Ucom_ref is beyond maximum Ucom and minimum Ucom Limits

Note: these test cases are used to test limits of Ucom, testing the values beyond the maximum and minimum values of Ucom.

Software team to hardcode those parameters at VPC line side:

a. Udc=700V,

b. $U_\alpha = A \cdot \cos(\omega t) = 0.3 \cdot U_{dc} \cdot \cos\left(\frac{\theta \cdot \pi}{180}\right)$,

$U_\beta = A \cdot \sin(\omega t) = 0.3 \cdot U_{dc} \cdot \sin\left(\frac{\theta \cdot \pi}{180}\right)$

where

$\omega = 2\pi f, \quad f = 50Hz, \quad and\ A \quad should \quad be \quad small, \quad let\ A = 210V$

c. CM modulator is enabled.

d. Setup the VPC and using the Oscilloscope to detect the bottom leg phase A, B, and C voltages (Ua, Ub and Uc) as shown in Figure 22.

e. The exact values of U_α and $U\beta$ for each test case are shown in Table 3.

f. The expected duty cycle of each phase are shown in Table 3.

g. Using the oscilloscope math function to calculate and display Ucom based on 3 phase PWM signal. The expected Ucom should be different from Ucom_ref because it is beyond [U0min, U0max]. The expected Ucom should be either U0min or U0max.

h. The test cases are success if the measured da, db and dc are same as the expected values shown in Table 3, and the measured Ucom is same as the expected value shown in Table 3.

Table 3. Test cases 11-18 for CMV Injection, when Ucom_ref is beyond maximum Ucom and minimum Ucom Limits

TC #	Reference	U0min (V)	U0max (V)	Ucom_ref	Angle (°C)	Uα	Uβ	Expected Ucom	Expected da(phase A duty cycle) or T1	Expected db(phase B duty cycle) or T2	Expected dc(phase C duty cycle) or T3
11	DVPL-02 PWM modulator is able to limit	-201.5075819	147.1555743	170	135	-148.4924181	148.49243	147.1555743	0.498090223	1	0.632576524
12				150	135	-	148	147.15557	0.4980902	1	0.6325765

	the common mode voltage					148.4924181	.49243	43	23		24
13	injection within the allowable range			-210	135	-148.4924181	148.49243	-201.5075819	0	0.501909777	0.134486301
14				-230	135	-148.4924181	148.49243	-201.5075819	0	0.501909777	0.134486301
15		-168.1346624	168.134668	190	90	5.62693E-06	210	168.134668	0.740192391	1	0.480384758
16				180	90	5.62693E-06	210	168.134668	0.740192391	1	0.480384758
17				-180	90	5.62693E-06	210	-168.1346624	0.259807633	0.519615242	0
18				-190	90	5.62693E-06	210	-168.1346624	0.259807633	0.519615242	0

6.3 Execution and reporting

6.3.1 Risk Assessment

Not applicable.

6.3.2 Resources needed

6.3.3 Responsible

	Description	Action	Responsible
Data	Data storage	DVRE	WEWEI,BINGL
	Data type	What format should the data be in	WEWEI,BINGL
	Post processing	Not applicable	Not applicable
		Not applicable	Not applicable
Report (DVRE)	Test setup	Description of the device under test and test setup	WEWEI
	Measurement system	Description of the measurement system	WEWEI
	Test reporting	Reporting of the test (logbook etc) and results	WEWEI
	Verification reporting	Analyse and conclusions	WEWEI

7. DVRE for PWM Modulator

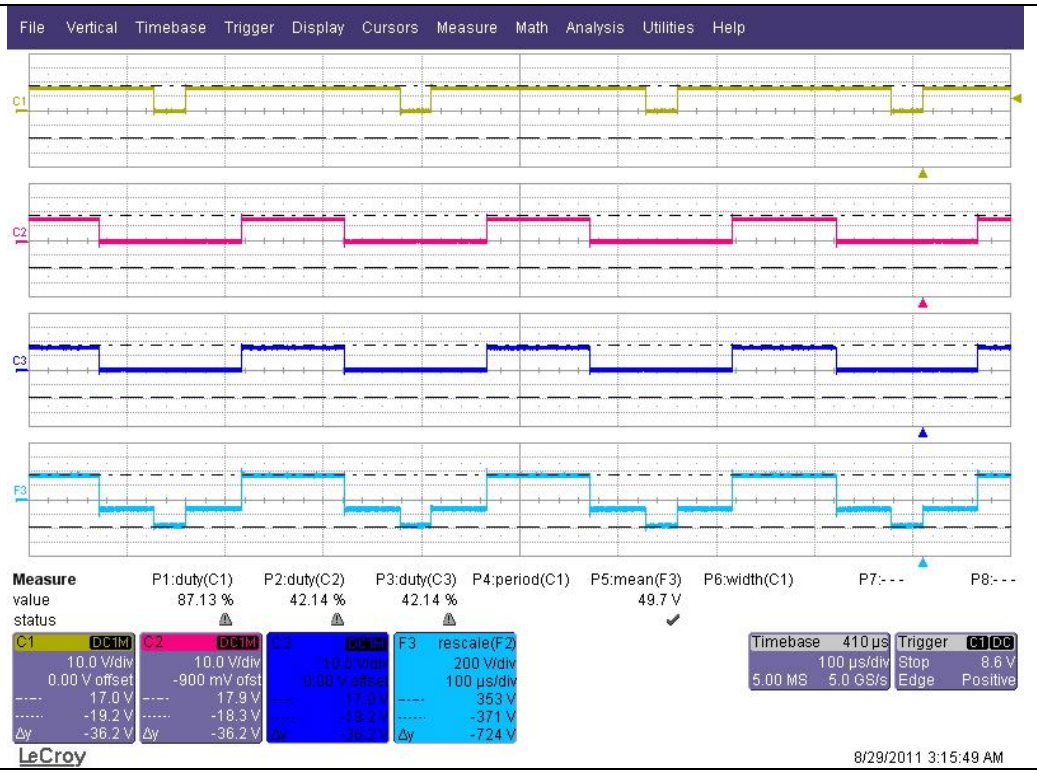
7.1 Test Results

The below test results are based on ADC code release 3.0 with some modification related to the SPR: drive00020734.

TC 001

Observations:

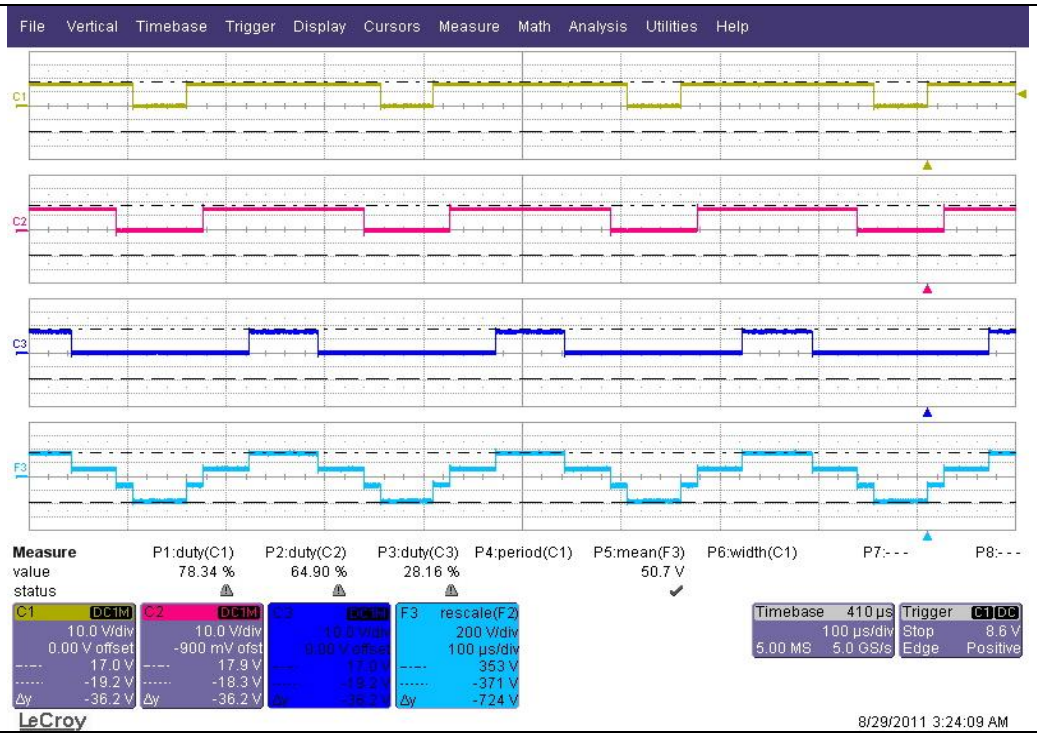
1. 0.01% error on phase a duty cycle
2. 0.08% error on CMV



TC 002

Observations:

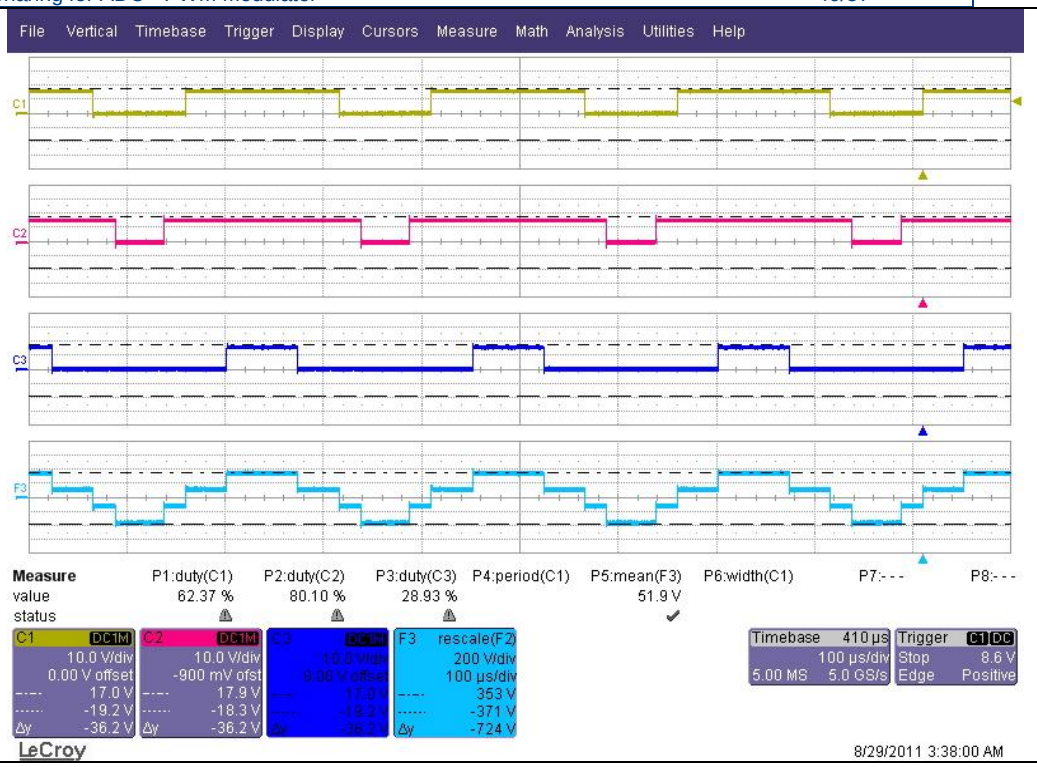
1. 0.01% error on phase a duty cycle
2. 0.133% error on CMV



TC 003

Observations:

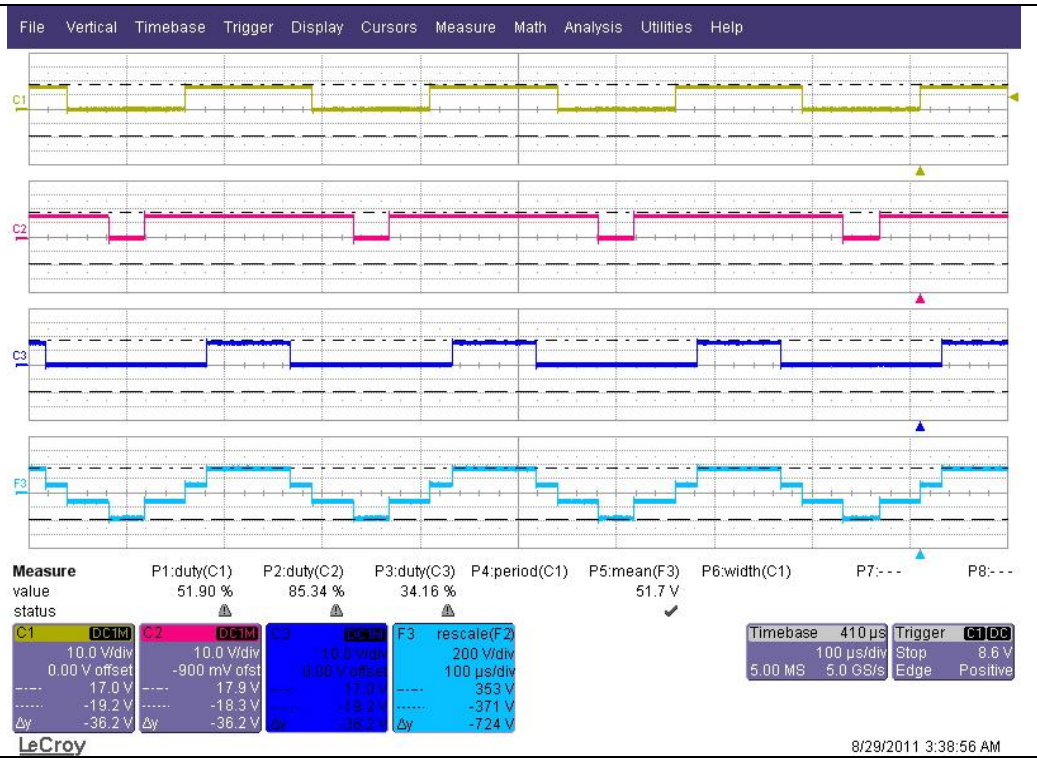
1. 0.02% error on phase a duty cycle
2. 0.02% error on phase b duty cycle
3. 0.02% error on phase c duty cycle
4. 0.133% error on CMV



TC 004

Observations:

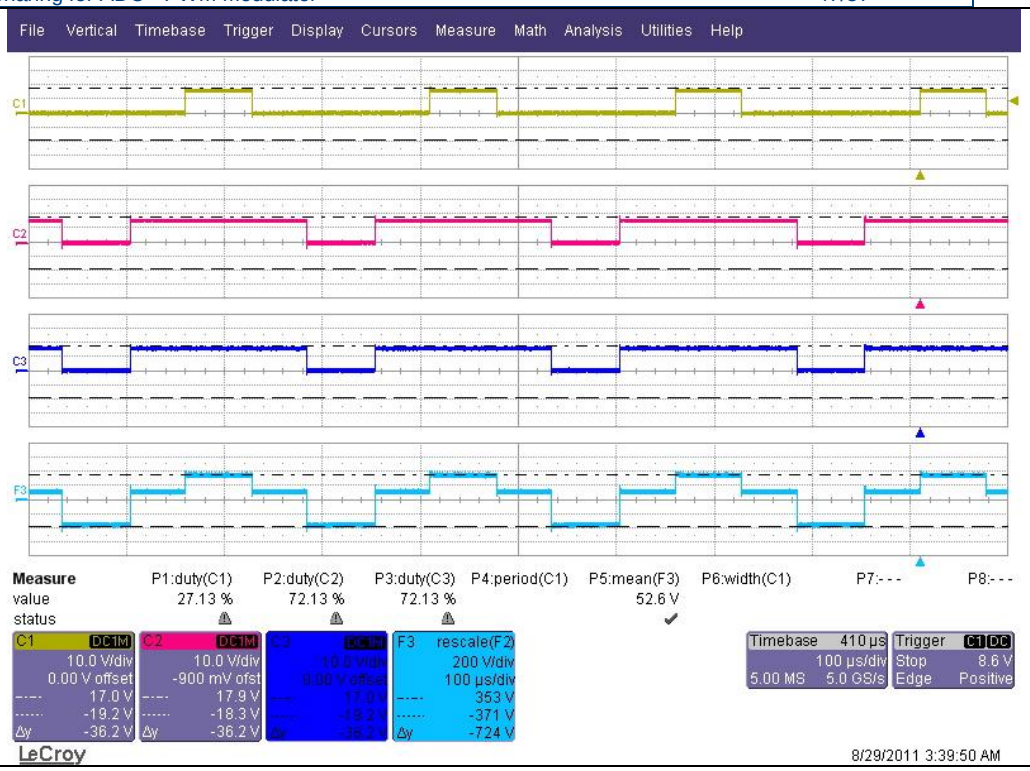
1. 0.03% error on phase a duty cycle
2. 0.01% error on phase b duty cycle
3. 0.133% error on CMV



TC 005

Observations:

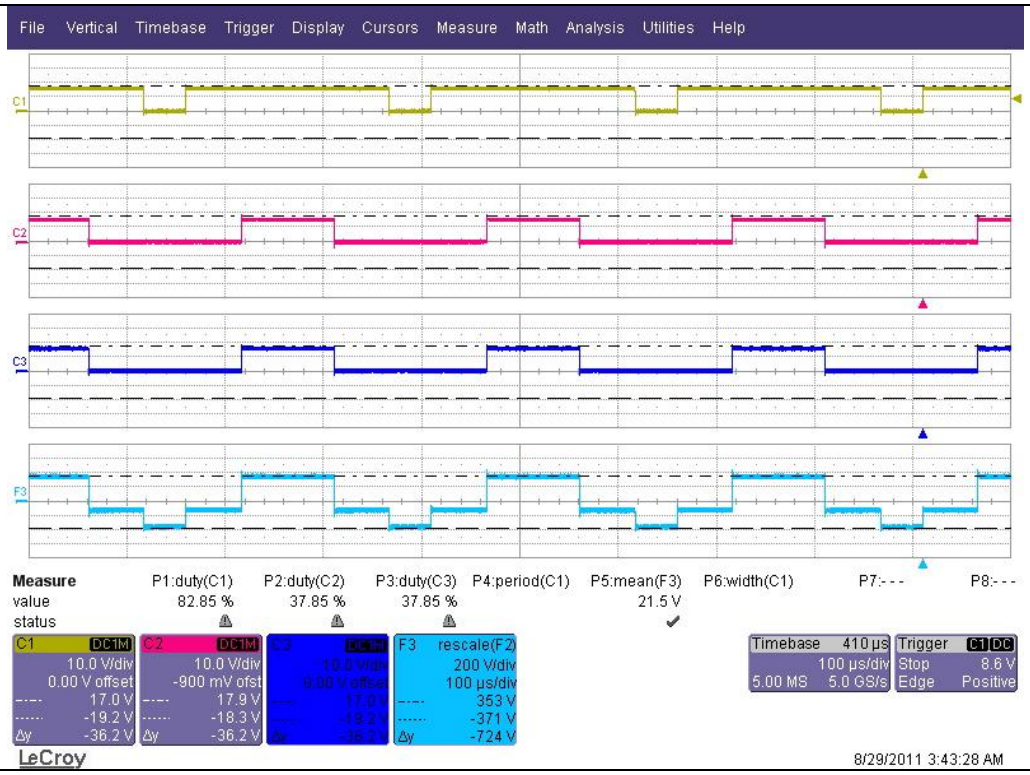
1. 0.01% error on phase a duty cycle
2. 0.01% error on phase b duty cycle
3. 0.01% error on phase c duty cycle
4. 0.18% error on CMV



TC 006

Observations:

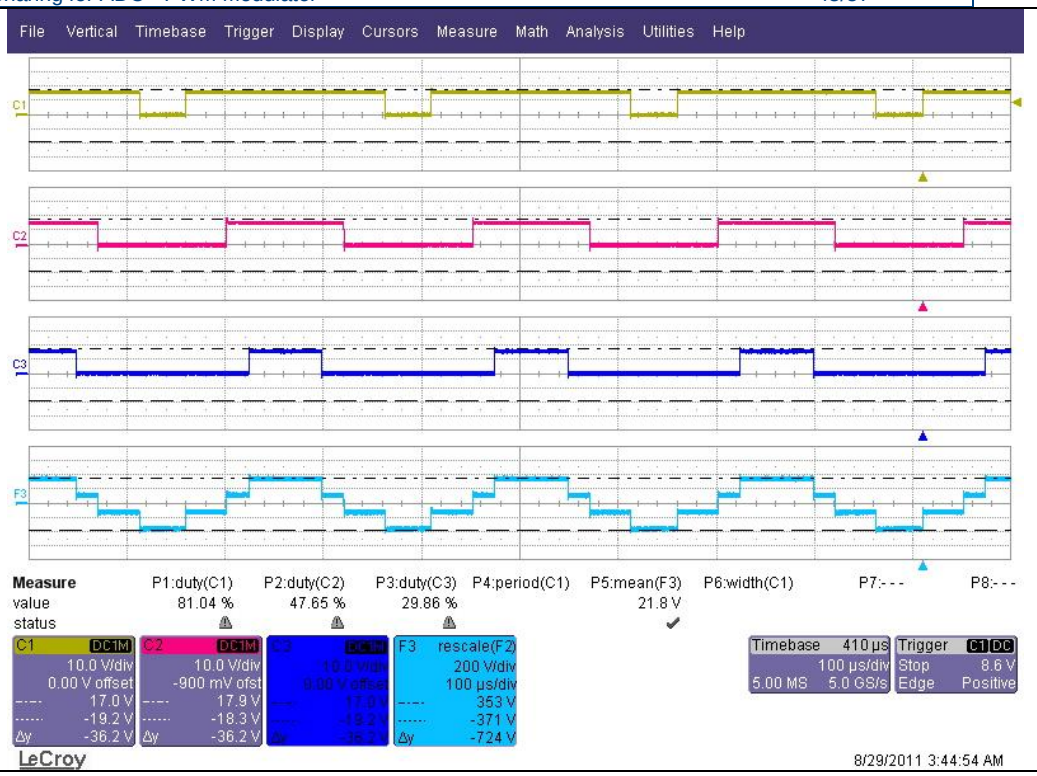
1. 0.01% error on phase a duty cycle
2. 0.01% error on phase b duty cycle
3. 0.01% error on phase c duty cycle
4. 0.25% error on CMV



TC 007

Observations:

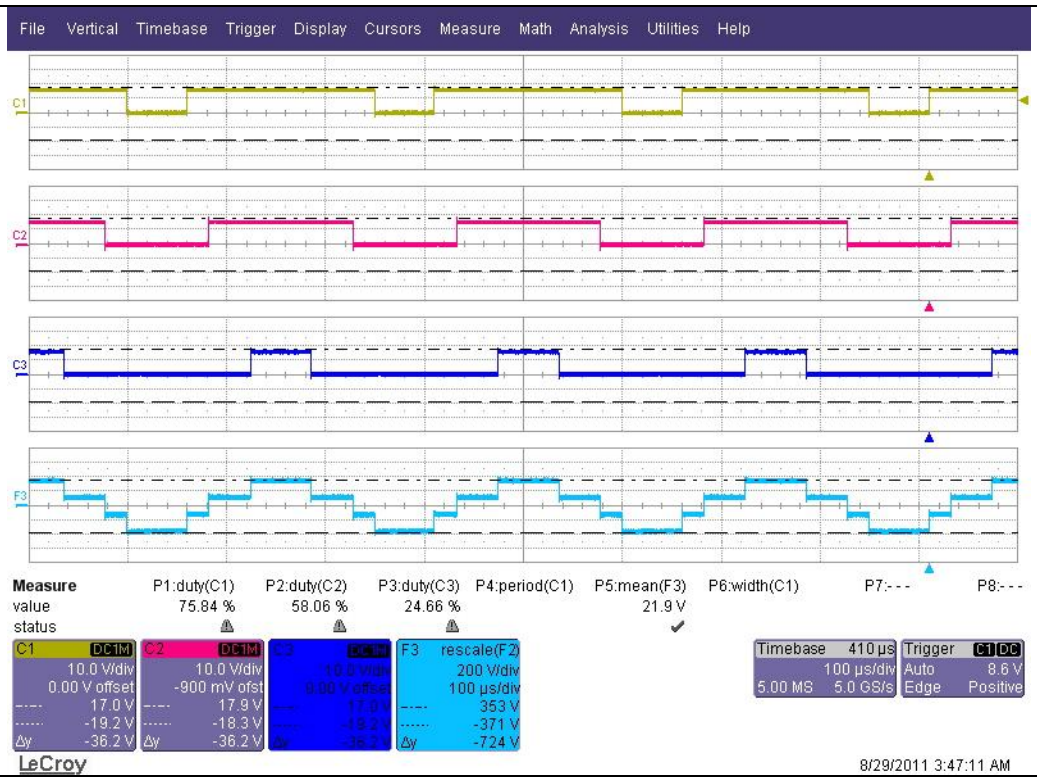
1. 0.01% error on phase a duty cycle
2. 0.01% error on phase c duty cycle
3. 0.25% error on CMV



TC 008

Observations:

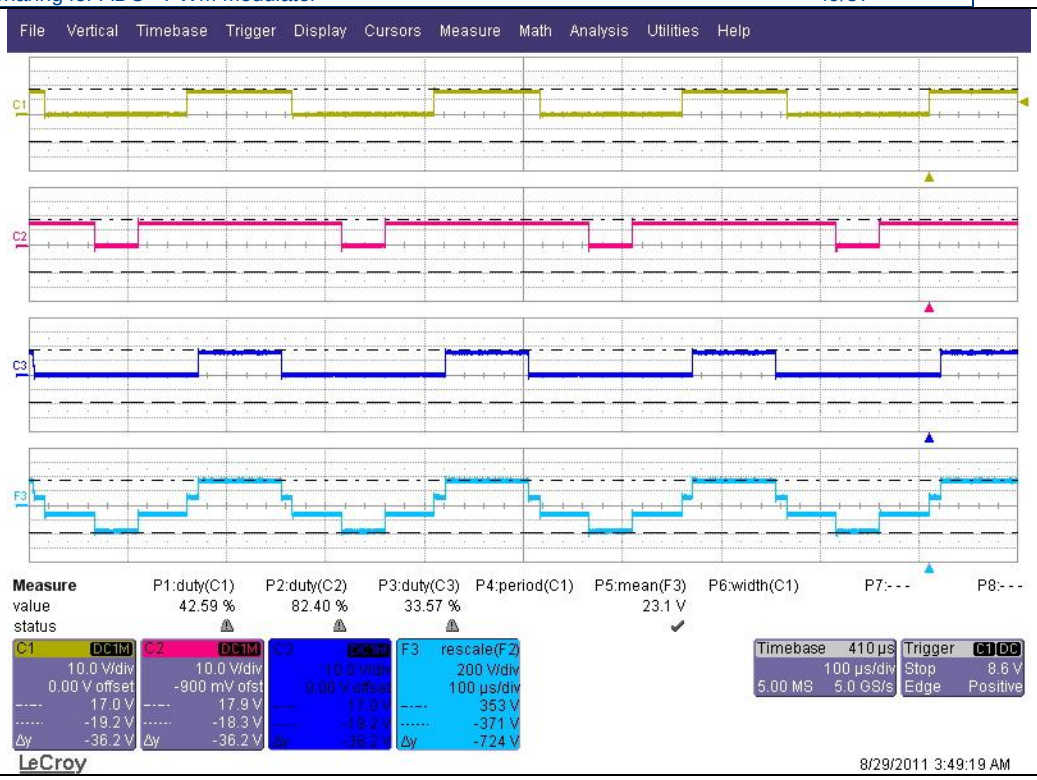
1. 0.01% error on phase b duty cycle
2. 0.133% error on CMV



TC 009

Observations:

1. 0.01% error on phase a duty cycle
2. 0.063% error on CMV

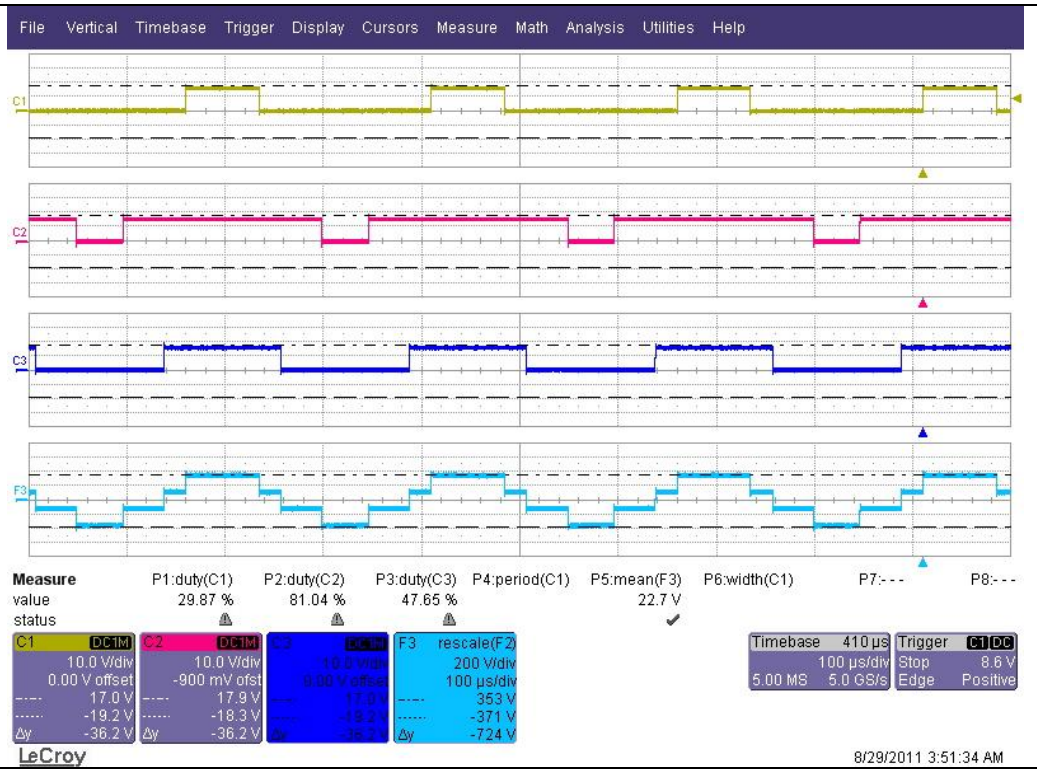


TC 010

Observations:

.

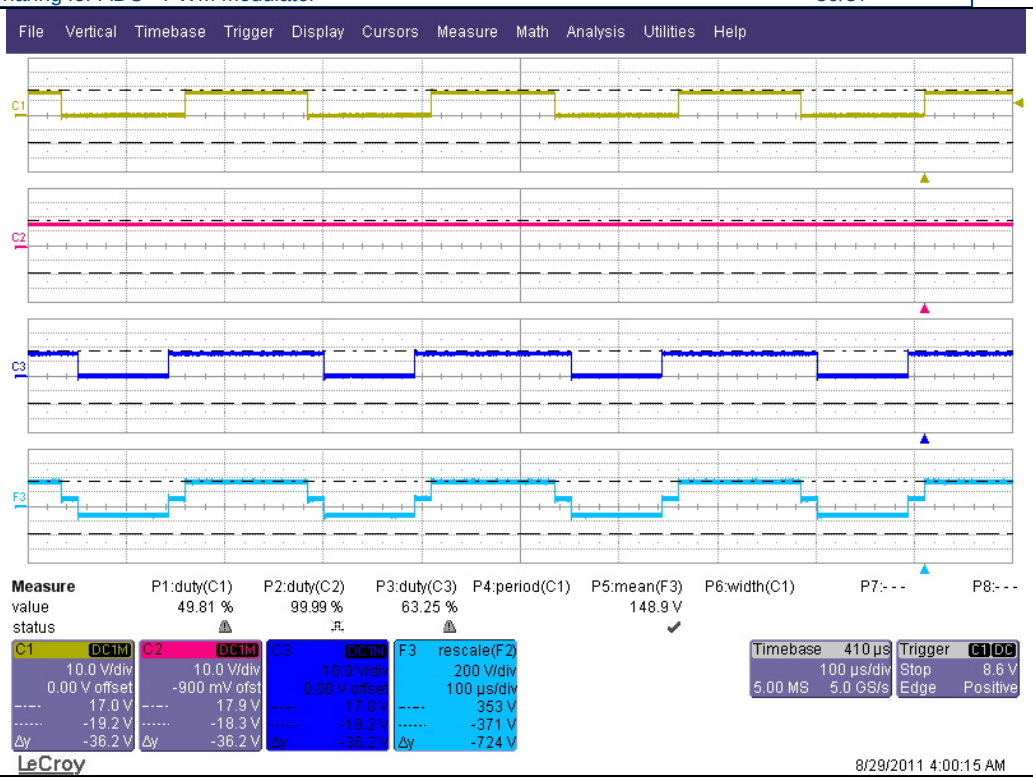
1. 0.01% error on phase a duty cycle
2. 0.01% error on phase b duty cycle
3. 0.133% error on CMV



TC 011

Observations:

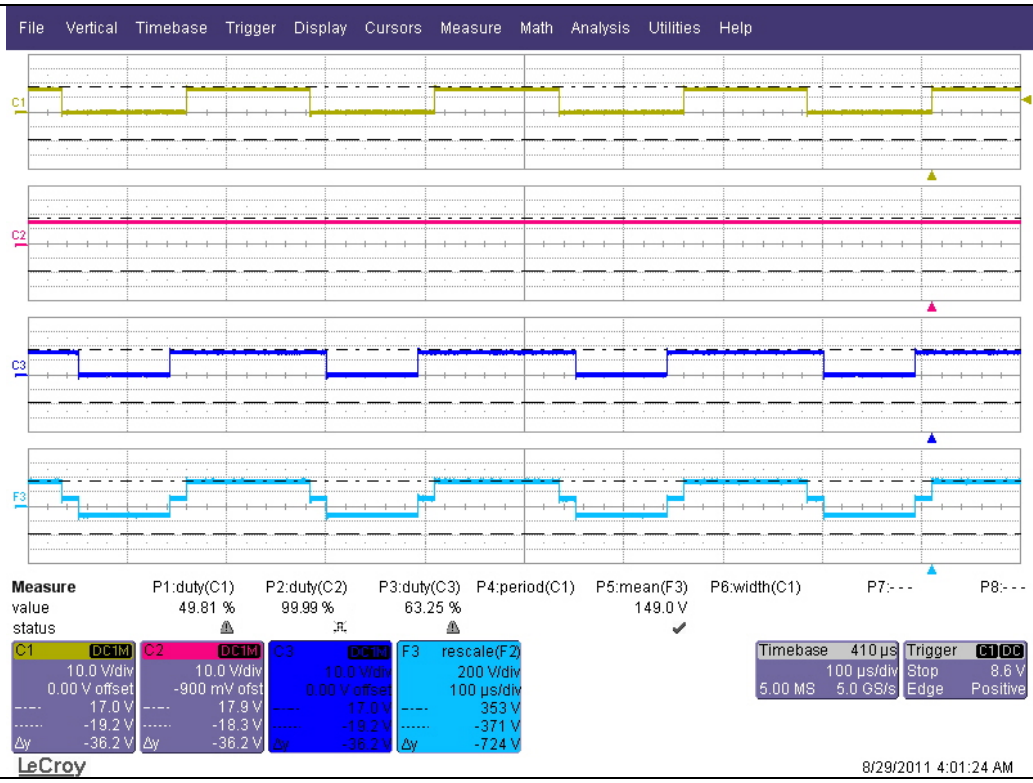
1. 0.01% error on phase b duty cycle
2. 0.01% error on phase c duty cycle
3. 0.026% error on CMV



TC 012

Observations:

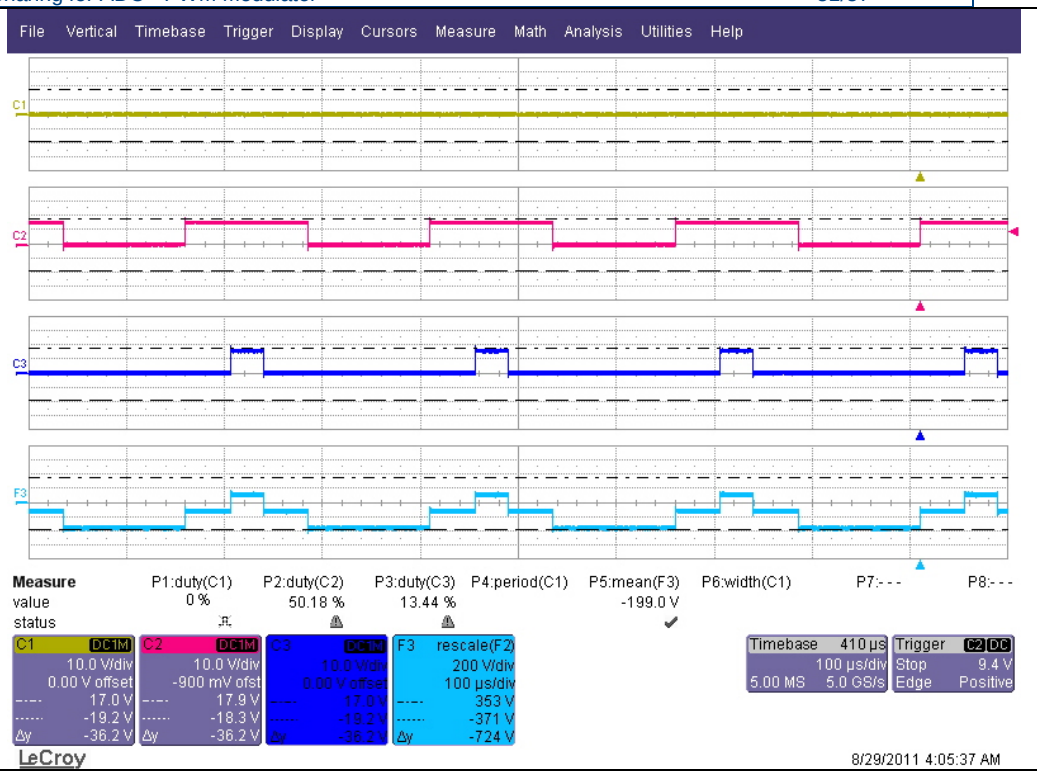
1. 0.01% error on phase b duty cycle
2. 0.01% error on phase c duty cycle
3. 0.026% error on CMV



TC 013

Observations:

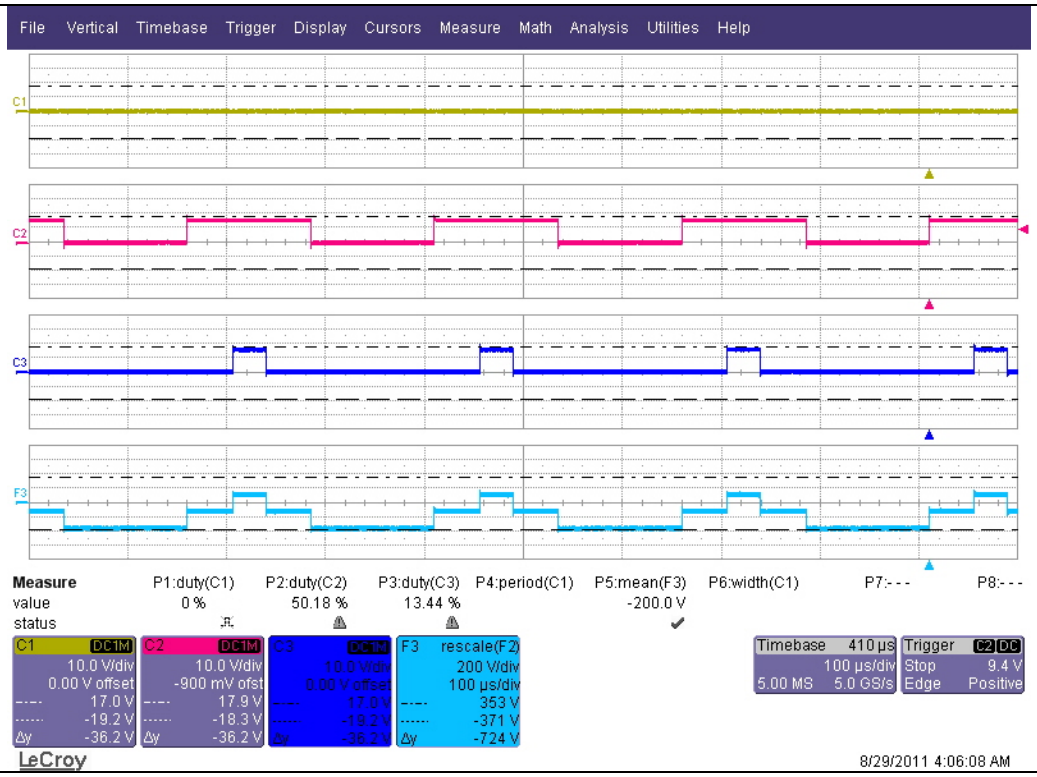
1. 0.01% error on phase b duty cycle
2. 0.01% error on phase c duty cycle
3. 0.022% error on CMV



TC 014

Observations:

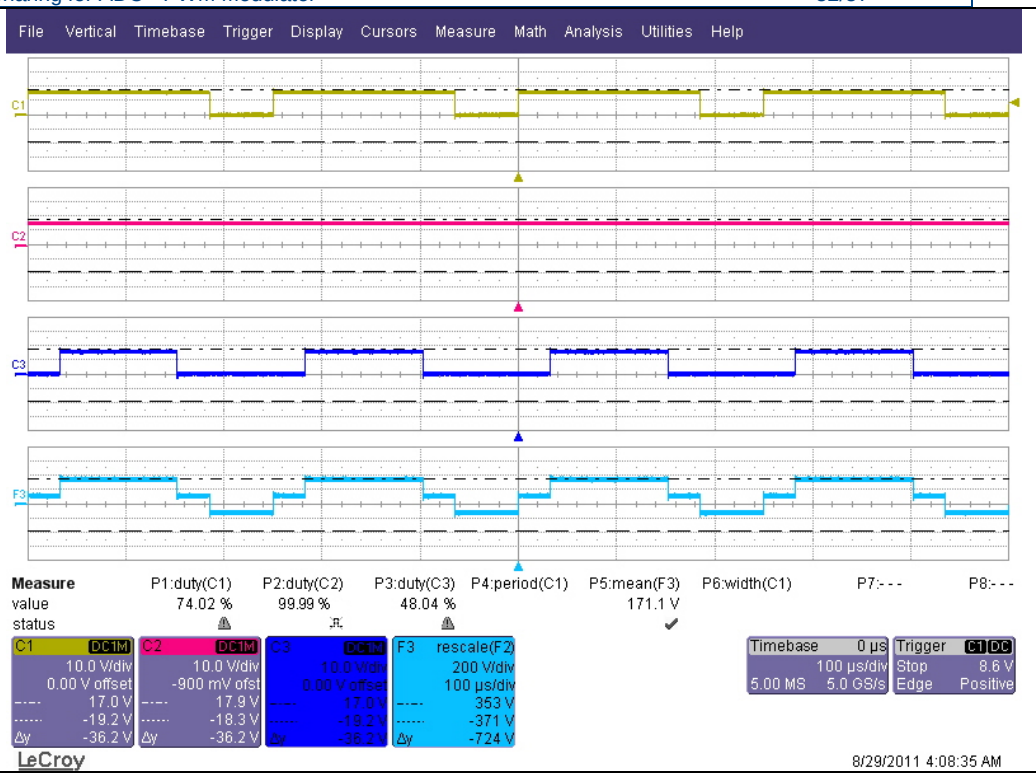
1. 0.01% error on phase b duty cycle
2. 0.01% error on phase c duty cycle
3. 0.022% error on CMV



TC 015

Observations:

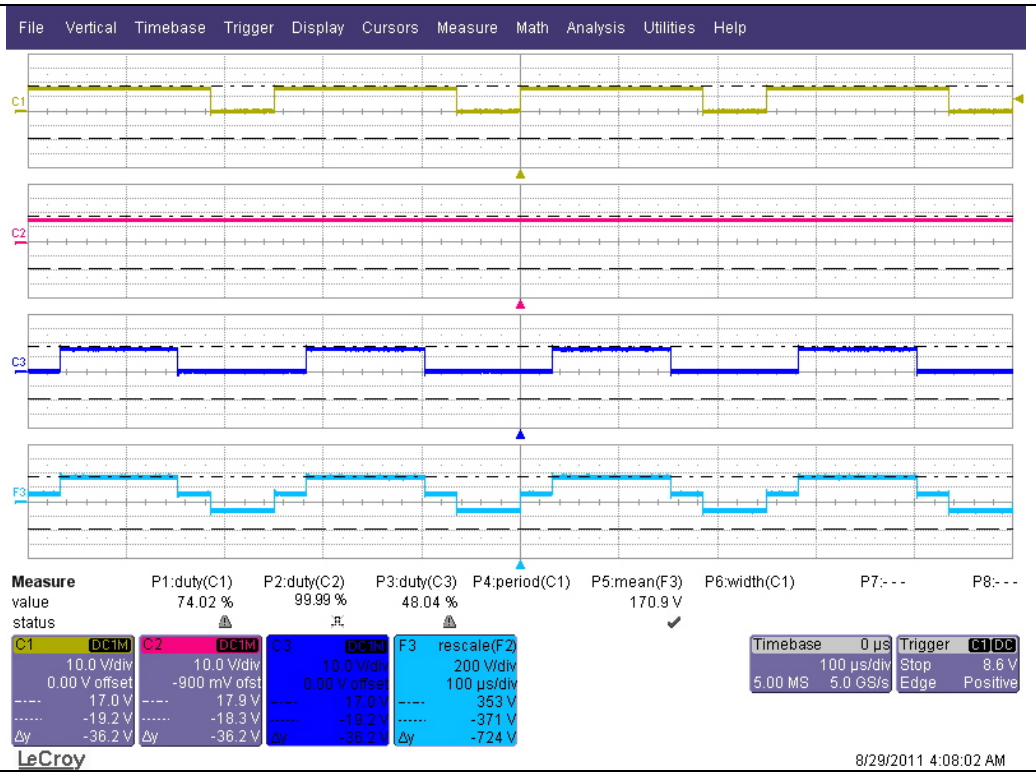
1. 0.01% error on phase b duty cycle
2. 0.011% error on CMV



TC 016

Observations:

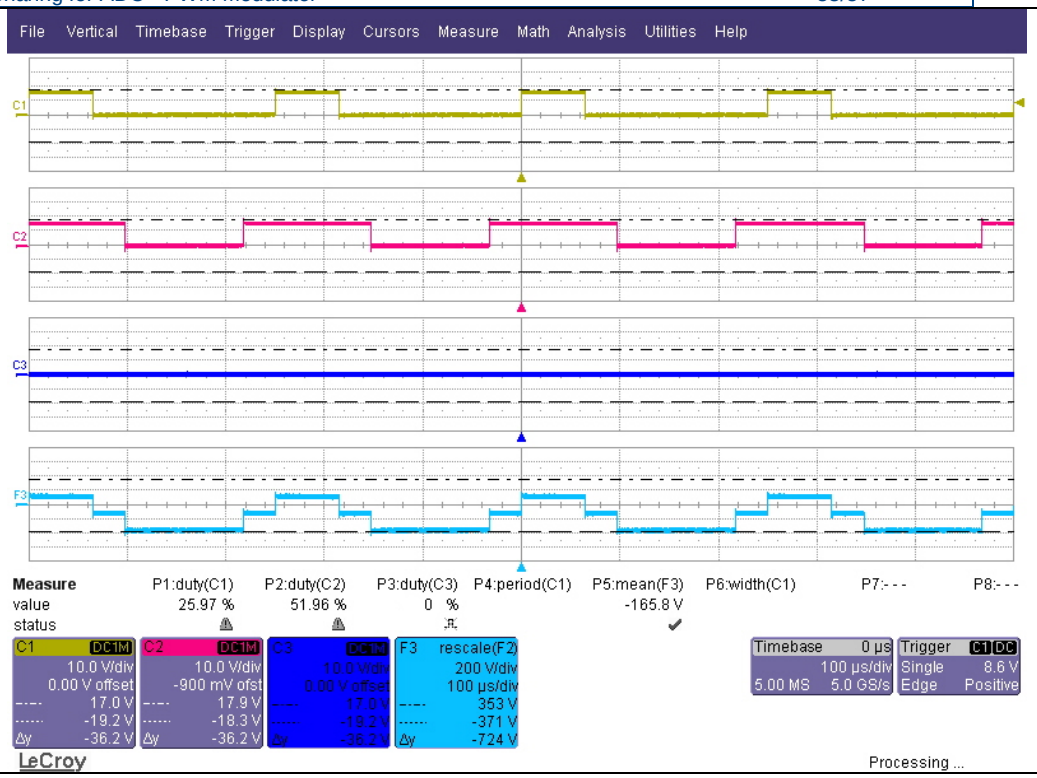
1. 0.01% error on phase b duty cycle
2. 0.011% error on CMV



TC 017

Observations:

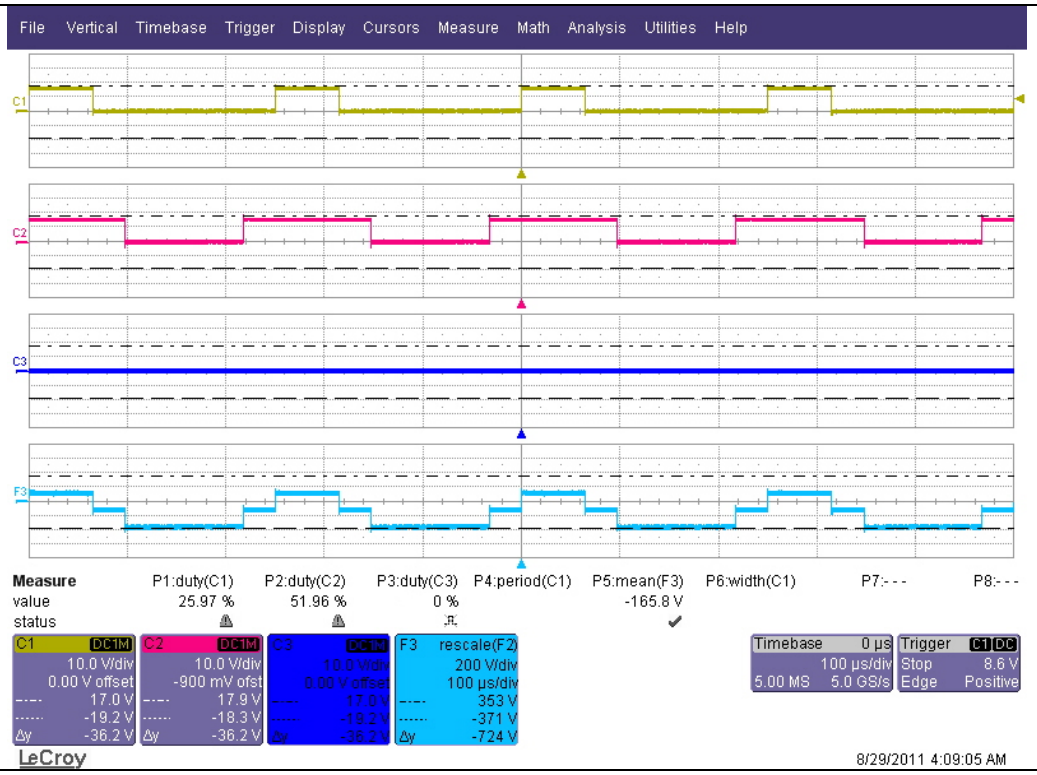
1. 0.01% error on phase a duty cycle
2. 0.017% error on CMV



TC 018

Observations:

1. 0.01% error on phase a duty cycle
2. 0.017% error on CMV



7.2 Overall summery

For all the results shown in section 7.1, the first waveform is the phase a duty cycle (da), the second waveform is the phase b duty cycle (db), the third waveform is the phase c duty cycle (dc) and the last waveform is the common mode voltage calculated based on the above three waveforms. The formula for generating the fourth waveform is:

$$V_a = \tfrac{1}{2} \cdot V_{dc} \cdot da - \tfrac{1}{2} \cdot V_{dc}(1 - da)$$

$$V_b = \tfrac{1}{2} \cdot V_{dc} \cdot db - \tfrac{1}{2} \cdot V_{dc}(1 - db)$$

$$Vc = \tfrac{1}{2} \cdot V_{dc} \cdot dc - \tfrac{1}{2} \cdot V_{dc}(1 - dc)$$

$$v_o = \frac{v_a + v_b + v_c}{3}$$

From the above four formulas, the common mode voltage is :

$$V_o = V_{dc} \cdot \left(\frac{da + db + dc}{3} - 0.5 \right)$$

The percentage error for phase a, b and c duty cycles and the error of measured common mode voltage are shown in the tables in section 7.1.
We can see from the observations in section 7.1, for all the test cases, the duty cycles have at most 0.03% discrepancy from the theoretical value calculated using equation (3-34). For the common mode voltage, the largest error is 0.25% which occurs at TC 006 and TC 007. With this small error, we can conclude that the performance of the common mode voltage injection is very good.

7.2.1 Test cases # 01-10

Take test case # 01 as an example.

Normalize all the values to Vdc/sqrt(3):

$$U_{com\_ref}(nomalized) = U_{com\_ref} / V_{dc} = 50/700 = 0.0714$$

.

$$U_{\alpha}(nomalized) = U_{\alpha} * \sqrt{3}/V_{dc} = 210 * \sqrt{3}/700 = 0.5196$$

$$U_{\beta}(nomalized) = U_{\beta} * \sqrt{3}/V_{dc} = 0 * \sqrt{3}/700 = 0$$

Then, ta, tb and tc can be determined based on section 3.1.1:

$$t_a = -U_{\beta} = 0$$

$$t_b = -\frac{\sqrt{3}}{2} U_{\alpha} - \frac{1}{2} U_{\beta} = -0.45$$

$$t_c = \frac{\sqrt{3}}{2} U_{\alpha} - \frac{1}{2} U_{\beta} = 0.45$$

Refering to section 3.1.1, the polarity of ta, tb and tc determines that the voltage vector is in sector 6 of the voltage space vector. Using equation (3-32) and (3-33), we get:

$$\therefore D_1 = \frac{\sqrt{3}}{2} V_{\alpha} + \frac{1}{2} V_{\beta} = -t_b = 0.45$$

$$\therefore D_2 = -V_{\beta} = t_a = 0$$

Then the minimum and maximum common mode voltages are:

$$U_{0\min} = -\frac{1}{2} + \frac{1}{3} D_1 + \frac{2}{3} D_2 = -0.35$$

$$U_{0\max} = \frac{1}{2} - \frac{2}{3} D_1 - \frac{1}{3} D_2 = 0.2$$

Since Ucom_ref (0.0714) is in between U0min (-0.35) and U0max (0.2), then the Ucom_ref that we injected into the VPC is the actual common mode voltage.

Hence, using equations (3-43) – (3-45), we have:

$$T_2 = \frac{1}{2} + U_0 - \frac{1}{3}D_1 - \frac{2}{3}D_2 = 0.421$$
$$T_3 = T_2 + D_2 = 0.421$$
$$T_1 = T_2 + D_1 = 0.871$$

T1, T2 and T3 are the phase a, b and c duty cycle calculated theoretically (same as da, db and dc we decribed above). From VPC, we are getting the same results as shown in section 7.1, which verifies that our algorithm is correct.

To further verify that the common mode voltage is correct, we use the measured phase a, b and c duty cycles to calculate the common mode voltage as follows:

$$V_o = V_{dc} \cdot \left(\frac{da + db + dc}{3} - 0.5 \right) = 700 \cdot \left(\frac{0.8713 + 0.4214 + 0.4214}{3} - 0.5 \right) = 49.96$$

This result is almost same as the the Ucom_ref we injected, with only 0.08%=(49.96-50)/50 error. Hence, we conclude that our algorithm is correct.

7.2.2 Test cases # 11-18

Take test case # 11 as an example.

Normalize all the values to Vdc/sqrt(3):

$$U_{com\_ref}(nomalized) = {U_{com\_ref}}/{V_{dc}} = {170}/{700} = 0.2429$$
.
$$U_{\alpha}(nomalized) = U_{\alpha} * {\sqrt{3}}/{V_{dc}} = -148.49 * {\sqrt{3}}/{700} = 0.3674$$
$$U_{\beta}(nomalized) = U_{\beta} * {\sqrt{3}}/{V_{dc}} = 148.49 * {\sqrt{3}}/{700} = 0.3674$$

Then, ta, tb and tc can be determined based on section 3.1.1:

$$t_a = -U_{\beta} = -0.3674$$
$$t_b = -\frac{\sqrt{3}}{2}U_{\alpha} - \frac{1}{2}U_{\beta} = 0.1345$$
$$t_c = \frac{\sqrt{3}}{2}U_{\alpha} - \frac{1}{2}U_{\beta} = -0.5019$$

Refering to section 3.1.1, the polarity of ta, tb and tc determines that the voltage vector is in sector 3 of the voltage space vector. Using equation (3-20) and (3-21), we get:

$$\therefore D_1 = -t_a = 0.3674$$
$$\therefore D_2 = t_b = 0.1345$$

Then the minimum and maximum common mode voltages are:

$$U_{0\min} = -\frac{1}{2} + \frac{1}{3}D_1 + \frac{2}{3}D_2 = -0.2879$$
$$U_{0\max} = \frac{1}{2} - \frac{2}{3}D_1 - \frac{1}{3}D_2 = 0.2102$$

Since Ucom_ref (0.2429) is not within U0min (-0.2879) and U0max (0.2102), then the Ucom_ref that we injected into the VPC is not the final common mode voltage. The common mode voltage should be limited to U0max, with the value of 0.2102.

Hence, using equations (3-43) – (3-45), we have:

$$T_1 = \frac{1}{2} + U_0 - \frac{1}{3}D_1 - \frac{2}{3}D_2 = 0.4981$$
$$T_3 = T_1 + D_2 = 0.6326$$
$$T_2 = T_3 + D_1 = 1$$

T1, T2 and T3 are the phase a, b and c duty cycle calculated theoretically (same as da, db and dc we decribed above). From VPC, we are getting almost same results as shown in section 7.1, with only 0.01% error, which verifies that our algorithm is correct.

To further verify that the common mode voltage is correct, we use the measured phase a, b and c duty cycles to calculate the common mode voltage as follows:

$$V_o = V_{dc} \cdot \left(\frac{da + db + dc}{3} - 0.5 \right) = 700 \cdot \left(\frac{0.4981 + 0.9999 + 0.6325}{3} - 0.5 \right) = 147.14V = 0.2102\,p.u.$$

This result is not the same as the the Ucom_ref we injected, but same as the U0max. Thus, we could conclude that the algorithm is capable of limiting the injected Ucom_ref with its allowable range. Hence, we conclude that our algorithm is correct.

7.2.3 Comparison with the old wrong code (Release 3.0)

In release 3.0, when we define common mode voltage, we first normalized it w.r.t sqrt(3)*Vdc in RI_GI_FiFoDrive.c.

However, when we calculate the transistor switching time using equations (3-43) – (3-45) in modulator.c, the U0 in the equations are normalized to Vdc. Thus, it is expected that a factor of sqrt(3) in the final output Ucom.
However, the multiplication of sqrt(3) in RI_GI_FiFoDrive.c did not affect the calculation of Umin and Umax because the value of Ucom_ref has no influence on these two values. They are solely depending on duty1 and duty2 as indicated in equations (3-36) – (3-37).

With this, for test cases 01-10, a factor of sqrt(3) is expected and for test cases 11-18, the result in release 3.0 with some modification related to SPR: drive00020734 is expected to be the same as in release 3.0.

Thirteen test cases are selected among the 18 test cases and comparison is shown in Table 4, which proves the above conclusion.

Table 4. Comparison of release 3.0 and release 4.0 results

	Release 4.0				Release 3.0				Factor= (Ucom2)/(Ucom 1)
TC #	da	db	dc	Ucom 1	da	db	dc	Ucom2	1.73
01	0.871428571	0.421428571	0.421428571	49.96	0.9236	0.4737	0.4737	86.56666667	1.73
02	0.783560609	0.649074281	0.281650825	50.07	0.8358	0.7013	0.334	86.59	1.73
03	0.623523032	0.8012419	0.289520783	50.07	0.6757	0.8535	0.3417	86.54333333	1.73

04	0.519334127	0.853336355	0.341615233	50.07	0.4115	0.9135	0.546	86.56666667	1.73
05	0.271428571	0.721428585	0.721428558	50.09	0.3236	0.7736	0.7736	86.52	1.73
06	0.828571429	0.378571429	0.378571429	20.05	0.8494	0.3995	0.3995	34.62666667	1.73
07	0.810479215	0.476476974	0.298758097	20.05	0.8313	0.4974	0.3197	34.62666667	1.73
09	0.425965395	0.824013753	0.335735138	20.01	0.4468	0.8448	0.3566	34.58	1.73
10	0.298758104	0.810479219	0.476476963	20.03	0.3197	0.8312	0.4973	34.58	1.73
11	0.498090223	1	0.632576524	147.04	0.4981	0.9999	0.6325	147.1166667	1
13	0	0.501909777	0.134486301	-200.96	0	0.5019	0.1344	-201.53	1
15	0.740192391	1	0.480384758	168.02	0.7401	0.9999	0.4803	168.07	1
17	0.259807633	0.519615242	0	-167.97	0.2597	0.5196	0	-168.1633333	1

8. APPENDICES

8.1 References

Reference Number	Description
Ref1	DD for Load Sharing & Circulation Current Control for ADC Distrbuted Converter
Ref2	ADC Control Software Design for DigiPower

8.2 Word/Abbreviation List

Word/ Abbreviation:	Explanation:
DD	Design Description
ADC	Advanced Digital Control
PWM	Pulse width Modulation
CMV	Common Mode Voltage