# Simple PWM Approach for Three Phase Voltage Source Inverter with Reduced Complexity

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**Abstract:** PWM techniques are becoming popular in the present day applications due to the control of amplitude and frequency in the output voltage from VSI. There are two popular approaches for the implementation of PWM Algorithms. Carrier based and Space Vector Approach. Both the approaches give the same performance, but due to simplicity, mostly carrier based approach has been preferred. A large variety of PWM algorithms have been developed based on the scalar approach. Based on the modulating waveforms, the PWM algorithms mainly classified as continuous PWM (CPWM) and discontinuous PWM (DPWM) and active zero state PWM (AZSPWM) and near state PWM (NSPWM) algorithms. In the CPWM algorithms, the sinusoidal PWM (SPWM) and space vector PWM (SVPWM) algorithms are popular. A simple scalar pulse width modulation (PWM) approach that unites the conventional PWM methods and most recently developed reduced common mode voltage PWM method under one umbrella will be developed. It becomes an easy task to program the pulse patterns of various high performance PWM methods and benefit from their performance in modern three phase voltage source inverters for applications such as motor drives, PWM rectifiers and active filters. To validate the proposed algorithms, numerical simulation studies have to be developed by using Matlab-simulink.

**Keywords:** PWM, VSI, SPWM, CPWM.

## I. INTRODUCTION

Three-Phase, three-wire voltage-source inverters (VSI) are widely utilized in ac motor drive and utility interface applications requiring high performance and high efficiency. In Fig. 1, the standard three-phase two-level VSI circuit diagram is illustrated. The classical VSI generates ac output voltage from dc input voltage with required magnitude and frequency by programming high-frequency rectangular voltage pulses. The carrier-based pulse width modulation (PWM) technique is the preferred approach in most applications due to the low-harmonic distortion waveform characteristics with well-defined harmonic spectrum, fixed switching frequency, and implementation simplicity. Carrier-based PWM methods employ the "per-carrier cycle volt-second balance" principle to program a desirable inverter

output voltage waveform [1]. In every PWMcycle, the reference voltage, which is fixed over the PWM cycle, corresponds to a fixed volt-second value. According to the volt-second balance principle, the inverter output voltages made of rectangular voltage pulses must result in the same volt-seconds as this reference volt-second value.
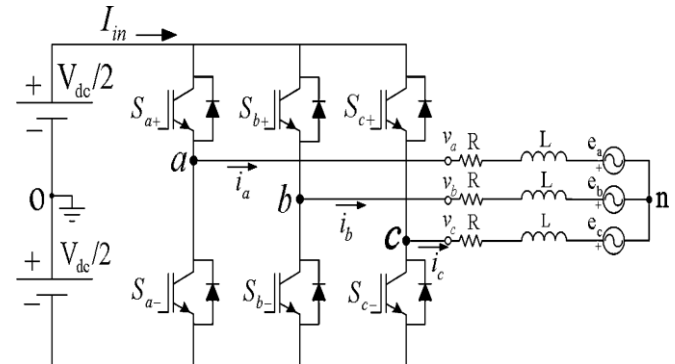


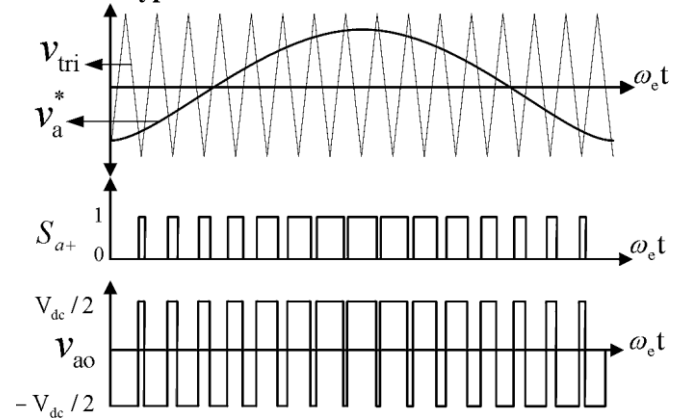**Fig.1. Circuit diagram of a PWM-VSI drive connected to an R-L-E type load.**



**Fig.2. Triangle intersection PWM phase "a" modulation wave v∗a , switching signal and vao voltage.**

There are two main implementation techniques for carrier based PWM methods: 1) scalar implementation and 2) space vector implementation. In the scalar approach, as shown in Fig2, for each inverter phase, a modulation wave is compared with a triangular carrier wave [using analog circuits or digital hardware units (PWM units) as conventionally found in motor control microcontroller or

DSP chips] and the intersections define the switching instants for the associated inverter leg switches. In the space vector approach, as illustrated in the space vector diagram in Fig. 3, the time lengths of the inverter states are precalculated for each carrier cycle by employing space vector theory and the voltage pulses are directly programmed [2], [3]. The mathematics involved in the scalar method modulation waves and the space vector calculations is related. With proper modulationwaves, the scalar and space vector PWM pulse patterns can be made identical [1]. Thus, both techniques may have equivalent performance results.
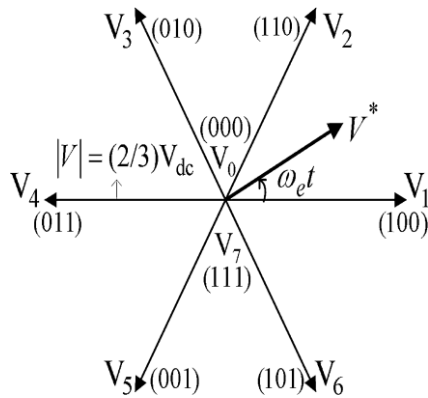


**Fig.3. Voltage space vectors of three-phase two-level inverter. The upper switch states are shown in the brackets (Sa+, Sb+, Sc+). "1" is ON and "0" is OFF state.**

But the scalar approach is simpler than the space vector approach from the implementation perspective as the involved computations are generally fewer and less complex [1]–[9]. Based on the scalar or vector approach, there are various PWM methods proposed in the literature which differ in terms of their voltage linearity range, ripple voltage/current, switching losses, and high-frequency common mode voltage/current properties. The conventional sinusoidal PWM (SPWM) [10], space vector PWM (SVPWM) [3], discontinuous PWM1 (DPWM1) [11], and the recently developed active zero state PWM (AZSPWM) methods [12], [13], near state PWM (NSPWM) [14], and remote state PWM(RSPWM) [15] methods, are a few (and themost important ones) to name. In particular, the last few have been recently developed with the quest for reducing the VSI common mode voltage (CMV) magnitude [16]. However, the implementation of these methods is not easy and not reported in the literature to sufficient depth. Furthermore, the relation between the conventional and recently developed reduced CMV (RCMV) PWM methods is not well understood both in terms of implementation characteristics and performance characteristics.

Therefore, difficulties arise in implementing and understanding the performance attributes of these PWM methods. This paper first reviews the PWM principles and establishes a general scalar approach that treats the conventional andRCMV–PWM methods, and unites most methods under one umbrella. The paper then reviews the pulse patterns and performance of the popular PWM methods, and provides guidance for simple practical implementation which is favorable over the conventional methods (space vector or scalar [1]–[9]). The experimental results verify the feasibility of the proposed approach.

## II. REVIEW OF THE CARRIER-BASED PWM PRINCIPLES

The PWM approach is based on the "per-carrier cycle voltsecond balance" principle, which is generally applicable principle to all power electronic converters. According to this principle, in a PWM period(TS), the average value of the output voltage is equal to the reference value. Thus, an output voltage with a desirable value is obtained by creating a reference voltage and matching this reference voltage with the pulse width modulated inverter output voltages for each PWM period. Therefore, the fundamental constraint in programming the PWMpulses for each phase involves the volt-seconds balance. In scalar PWM, the reference (modulation) wave of each phase ($v^*_a$, $v^*_b$, $v^*_c$) is compared with a carrier wave (vtri) and the intersections define the switching instants for switches of the associated inverter phase leg (see Fig. 2). The period of the carrier wave is equal to one PWM period(TS). In a PWMperiod, if the modulation wave is larger (smaller) than carrier wave, the upper switch is ON (OFF). The upper and lower switches of each leg operate in complementary manner (Sa+ = 1 → Sa− = 0). The per-carrier cycle average value of the voltage of one VSI leg output ($v_{ao}$) (phase to dc bus midpoint voltage) is equal to the reference value of that leg ($v^*_a$) due to the volt-second balance principle. The fundamental output voltage (may be obtained by removing the PWMripple from the output voltage) has the same waveform as the modulation wave. If a sinusoidal fundamental output voltage is wanted, then a modulation wave consisting of sinusoidal form with proper fundamental frequency and magnitude is compared with the high-frequency carrier wave.

In a three-phase VSI, under balanced operating conditions, the reference voltages of each leg have the same shape but they are 120◦ phase shifted from each other. To obtain sinusoidal output voltages, in the scalar implementation three symmetric and 120◦ phase shifted sinusoidal modulation waves are compared with the carrier wave and this method is called as the conventional SPWM method, which has been used in motor drives for many decades [10]. However, in three-phase, three-wire VSIs, constraining the reference modulation waves to pure sinusoidal form is not favorable in most cases, as will be discussed in the following. In three-phase, three-wire inverters where the neutral point of the load is isolated, no neutral current path exists (except for very high frequencies where circuit parasitic capacitances establish a current flow path) and only the inverter line-to-line voltages determine the load current subcarrier frequency content. Thus, the n-o potential in Fig. 1, which will be symbolized with vno, can be freely varied. In such applications, any common bias voltage (zero-sequence signal (v0 ) can be added (injected) to the SPWM

reference voltages (modulation waves). The injection of a zerosequence signal simultaneously shifts each reference wave in the vertical direction (with respect to the carrier wave). Therefore, the inverter line-to-line voltage per-carrier cycle average value is not affected. However, v0 changes the position of the output line-to-line voltage pulses (see Fig. 8).

Therefore, it significantly influences the harmonic distortion, voltage linearity, and switching frequency characteristics [1], [2], [17], [18]. With a proper zero-sequence signal injection (theoretically, infinite choices exists! [1]), the overall inverter performance increases substantially over SPWM. Ever since this advantage has been understood, the zero-sequence signal injection technique has been in wide utilization in practice. Obtained with zero-sequence signal injection, SVPWM [1], [3], [18] and DPWM1 [11], [19] are two highly popular examples. While the former method provides low harmonic distortion, the latter yields low switching losses. Furthermore, compared to SPWM, both methods extend the voltage linearity range of the VSI by 15% [20], [21]. In three-phase, three-wire VSIs, not only the modulation waves, but also the carrier waves are per phase and can be arbitrarily selected. The carrier waves may be triangular or sawtooth, for each phase. The carrier of a phase may be phase shifted with respect to the carriers of other phases. It may even be at a different frequency. In all these cases, the volt-seconds balance is not affected and the per-carrier cycle average value of the VSI leg output voltage is retained. In three-phase VSIs, conventionally one common triangular carrier wave is utilized for all phases due to its symmetric switching sequence which results in low harmonic distortion, low switching loss, and "one switching at a time" characteristics. While this constraint allows easy implementation of conventional PWM methods, it also constrains the variety of PWM methods with the scalar implementation, as will be discussed in the next section.

The a for ementioned discussions indicate that in the scalar implementation both the zero-sequence signal and the carrier signals allow degrees of freedom to obtain variousPWMpulse patterns with substantial differences in performance. While some of these possibilities have been explored in the past, some others are undiscovered. The next section will formally treat the subject and explore the possibilities. However, the space vector approach, as a different approach to form the PWM pulse pattern from the scalar approach requires a brief review at this stage. This is because some PWMmethods with favorable pulse patterns have been first invented based on the space vector approach [12], [13] and their scalar equivalents will be found during the aforementioned discussed exploration state. While the space vector implementation of such pulse patterns is laborious, to be obtained with aid of the generalized scalar PWM approach, the scalar method-based equivalents are easy to implement. Thus, it is important to show the pulse pattern equivalency and implementation advantage. In the space vector approach, employing the complex variable

transformation, the time domain phase reference voltages are translated to the complex reference voltage vector (V*) with the magnitude (V*$_{1m}$) that rotates in the complex coordinates with the $\omega_e t$ angular speed (see Fig. 3) in the following equation:

$$V^* = \frac{2}{3}\left(v_a^* + a v_b^* + a^2 v_c^*\right) = V_{1m}^* e^{j\omega_e t}, \text{ where } a = e^{j(2\pi/3)} \tag{1}$$

Since there are eight possible inverter states available, the vector transformation yields eight voltage vectors as shown in Fig. 3. Of these voltage vectors, six of them (V1 , V2 , V3 , V4 , V5 , V6 ) are active voltage vectors, and two of them (V0 and V7) are zero-voltage vectors (which provide degree of controllability similar to the zero-sequence signal of the scalar implementation) which generate zero output voltage. In the space vector analysis, the duty cycles of the voltage vectors are calculated according to the vector volt-second balance rule defined in the following equations, and these voltage vectors are applied with the calculated duty cycles:
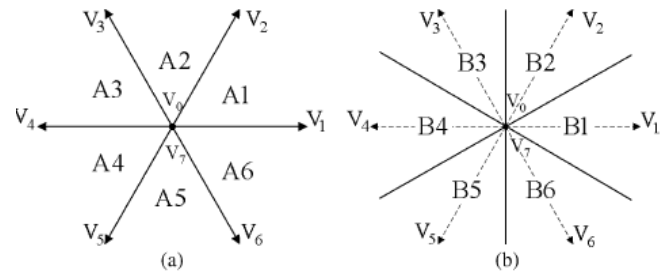


Fig. 4. Voltage space vectors and 60° sector definitions. (a) A-type region. (b) B-type region.

$$\sum_{k=0}^{7} V_k t_k = V^* T_S \tag{2}$$

$$\sum_{k=0}^{7} t_k = T_S. \tag{3}$$

Each PWM method utilizes different voltage vectors, vector time lengths, and sequences. Therefore, the vector space is divided into segments. There are six A-type and six B-type segments available (see Fig. 4). Investigations reveal that all space vector PWM methods utilize either A-type or B-type segments, and the utilized voltage vectors of these PWMmethods alternate at the boundaries of the corresponding segments [16]. For example, the space vector implemented SVPWM and AZSPWM1 utilize A-type and NSPWM utilizes B-type segments [14], [16]. In the space vector approach, the implementation is straightforward, but quite laborious [2]–[9]. The space vectors segments must be found and vector duty cycles must be calculated. Then, given a vector sequence, the phase switch duty cycles are calculated and loaded to the PWM counter of the PWM generator of a control board of the VSI. Should the reference voltage tip point fall out of the inverter voltage hexagon (overmodulation condition [20], [21]), then corrections to the vector duty calculations or recalculations with the modified reference vector become necessary. Thus, the direct space vector implementation is always a difficult task for a PWM

generator. Section III provides the generalized scalar PWM implementation approach which overcomes the involved procedure and computations.

## III. GENERALIZED SCALAR PWM APPROACH

The generalized scalar PWM approach provides degrees of freedom in the choice of both the zero-sequence signal and the carrier waves [22]. First, the zero-sequence signals can be arbitrarily generated, but generating them based on the phase reference voltages (original modulation signals) provides significant advantages. Until present, most useful PWM pulse patterns could be obtained by this approach [1], [18]. Therefore, in most cases, the zero-sequence signals are obtained by evaluating the reference voltages. Second, the carrier waves of different phases can be selected arbitrarily. However, recent studies have illustrated that employing triangular carrier waves at the same frequency, and selecting the phase relation between the
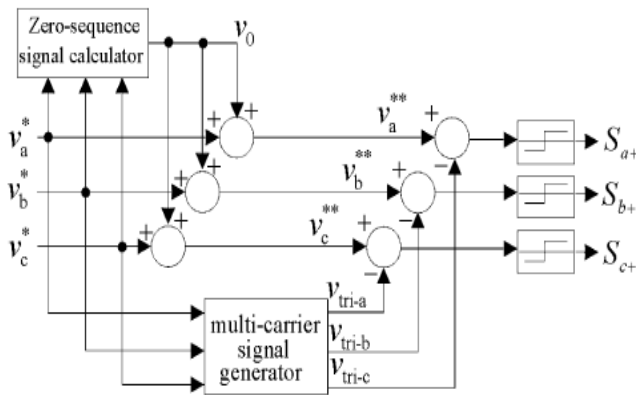


**Fig.5. Block diagram of the generalized carrier-based scalar PWM employing the zero-sequence signal injection principle and multicarrier signals.**
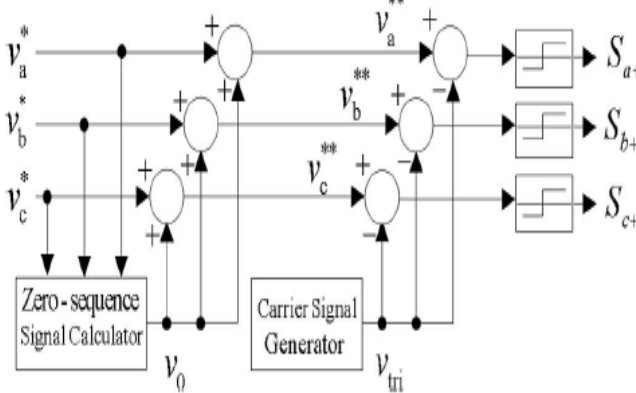


**Fig.6. Block diagram of the conventional scalar PWM method employing zero-sequence signal injection and a common triangular carrier wave.**

carrier waves of different phases based on the voltage references yields favorable results [14], [23], [24]. As a result, the generalized scalar PWM approach will favor such constraints for the purpose of keeping the scope of the paper within practical boundaries. Further relaxing the constraints and investigating alternative pulse patternswith favorable

characteristics is a subject matter of future research. Given the described set of constraints, the generalized block diagram of scalar PWM approach with zero-sequence signal injection principle is illustrated in Fig. 5. In the generalized scalar approach; according to the original three-phase sinusoidal reference signals (voltage references with single star superscripts) and zero-sequence signals, the final reference (modulation) signals (voltage references with double star superscripts) are generated. Then, the individual modulation and carrier waves are compared to determine the associated inverter leg switch states and output voltages. In the conventional approach (see Fig. 6), which is the special case of generalized approach, only one triangular carrier wave is utilized for all phases.

In the scalar representation, the modulation waves are defined as follows:

$$v_a^{**} = v_a^* + v_0 = V_{1m}^* \cos(\omega_e t) + v_0 \tag{4}$$

$$v_b^{**} = v_b^* + v_0 = V_{1m}^* \cos\left(\omega_e t - \frac{2\pi}{3}\right) + v_0 \tag{5}$$

$$v_c^{**} = v_c^* + v_0 = V_{1m}^* \cos\left(\omega_e t + \frac{2\pi}{3}\right) + v_0 \tag{6}$$

where $v_a^*$ , $v_b^*$ , and $v_c^*$ are the original sinusoidal reference signals and $v_0$ is the zero-sequence signal. Using the zero-sequence
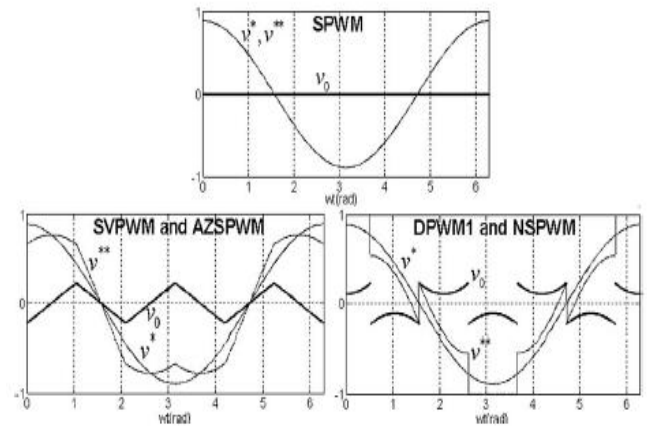


**Fig. 7. Modulation waveforms and zero-sequence signals of the popular PWM methods (Mi = 0.7).**

signal injected modulation waves, the duty cycle of each switch can be easily calculated in the following for both single and multicarrier methods:

$$d_{x+} = \frac{1}{2}\left(1 + \frac{v_x^{**}}{V_{dc}/2}\right) , \quad \text{for } x \in \{a, b, c\} \tag{7}$$

$$d_{x-} = 1 - d_{x+}, \quad \text{for } x \in \{a, b, c\} \tag{8}$$

It is helpful to define a modulation index (Mi , voltage utilization level) term at this stage. For a given dc-link voltage (Vdc), the ratio of the fundamental component magnitude of the line to neutral inverter output voltage (V1m) to the fundamental component magnitude of the six-

step mode voltage ($V_{1m\text{-}6\text{-step}} = 2V_{dc}/\pi$) is termed the modulation index Mi [1]

$$M_i = \frac{V_{1m}}{V_{1m\text{-}6\text{-step}}}$$

(9)

There are two commonly used zero-sequence signals in practical applications (see Fig. 7). For both cases, simple magnitude rules described in [1] are utilized to generate these signals. The zero-sequence signal of the widely utilized continuous PWM (CPWM) methods is generated by employing the minimum magnitude test which compares the magnitudes of the threephase original reference signals and selects the signal which has minimum magnitude [1]. Scaling this signal by 0.5, the zerosequence signal of these CPWM methods is found. Assume $|v_a^*| < |v_b^*|, |v_c^*|$. This modulation wave is recognized as SVPWM modulation wave in [1]. Inside the voltage linearity region, in the CPWM methods, the modulation waves are always within the carrier triangle peak boundaries; within every carrier cycle, the triangle and modulation waves intersect, and ON and OFF switchings always occur. In discontinuous PWM (DPWM) methods, the zero-sequence signal is injected such that reference signal of one phase is always clamped to the positive or negative dc bus. The clamped phase is alternated throughout the fundamental cycle. In the most common DPWM modulation wave (in the literature recognized as the DPWM1 modulation wave), the phase signal which is the largest in magnitude is clamped to the dc bus with the same polarity [1]. Assume $|v_a^*| \geq |v_b^*|, |v_c^*|$, then $v_0 = (\text{sign}(v_a^*)) \cdot (V_{dc}/2) - v_a^*$. The inverter leg whose modulation wave is clamped to the dc bus is not switched, therefore, switching losses are reduced in DPWM methods. The two popular zero-sequence signal

TABLE I. AZSPWM1, AZSPWM3, AND NSPWM SPACE VECTOR REGION DEPENDENT POLARITY ALTERNATING CARRIER SIGNALS

| AZSPWM1 | | | | | | |
|---|---|---|---|---|---|---|
| Carrier | A1 | A2 | A3 | A4 | A5 | A6 |
| $v_{tri\text{-}a}$ | $-v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ |
| $v_{tri\text{-}b}$ | $v_{tri}$ | $v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $v_{tri}$ |
| $v_{tri\text{-}c}$ | $-v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ |
| **AZSPWM3** | | | | | | |
| | A1 | A2 | A3 | A4 | A5 | A6 |
| $v_{tri\text{-}a}$ | $v_{tri}$ | $v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $v_{tri}$ |
| $v_{tri\text{-}b}$ | $-v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ |
| $v_{tri\text{-}c}$ | $-v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ |
| **NSPWM** | | | | | | |
| | B1 | B2 | B3 | B4 | B5 | B6 |
| $v_{tri\text{-}a}$ | $v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ |
| $v_{tri\text{-}b}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $-v_{tri}$ | $-v_{tri}$ | $v_{tri}$ |
| $v_{tri\text{-}c}$ | $-v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $v_{tri}$ | $-v_{tri}$ |

injection CPWM and DPWM method waveforms are shown in Fig. 7 along with the zero-sequence signal. SPWM is the naive form, where no zero-sequence signal is injected. Us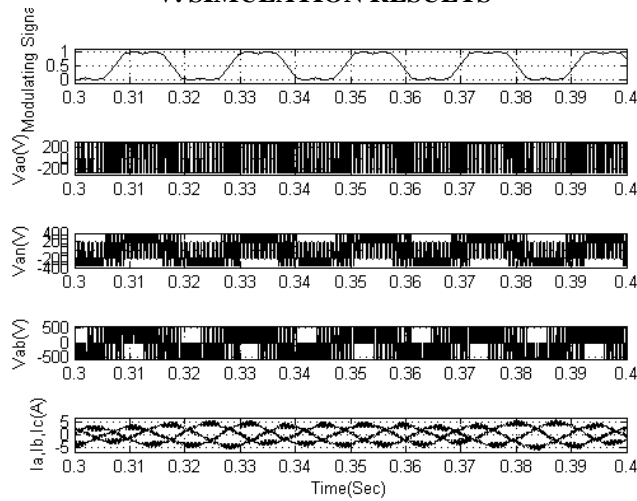ing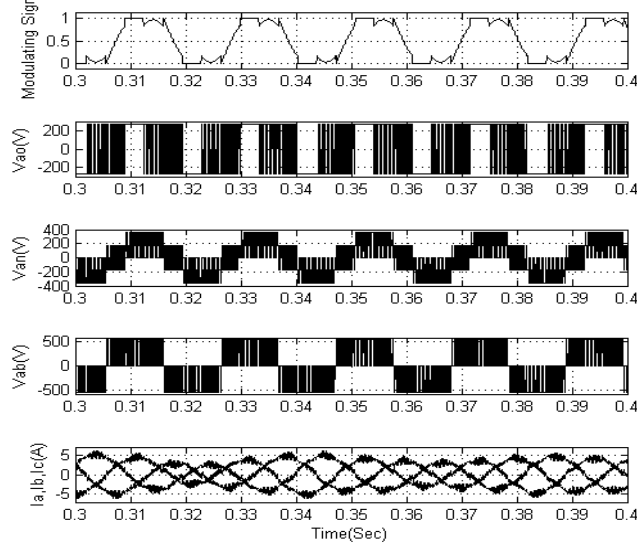 the discussed CPWM modulation wave along with a common triangular carrierwave for all phases, SVPWM method yields. Likewise, using the discussed DPWM modulation wave along with a common triangular carrier wave for all phases, DPWM1 yields.

## IV. PULSE PATTERNS AND PERFORMANCE CHARACTERISTICS OF POPULAR PWM METHODS

Since a large number of PWM methods exist and each method with unique pulse pattern yields unique performance characteristics, full investigation of all PWM methods in regard to their pulse pattern and performance is a laborious task. However, the theoretically infinite choice of methods, in practice reduces to a relatively small count when a systematic evaluation and performance comparison (among the many methods) is made. References [1], [2], and [16] involve such thorough investigation of large count of PWM methods and in conclusion it appears that only the popular methods discussed in this paper deserve significant attention. This section aims to review the popular PWM methods with the focus on their pulse patterns such that in the following section the practical implementation can be discussed to sufficient depth. Observing the pulse patterns, the performance characteristics can be studied, and thus major advantages of these methods can be recognized. Therefore, while reviewing the pulse patterns of the popular methods, it will also be possible to demonstrate why these methods are so well accepted. The pulse pattern of SVPWM is illustrated in Fig. 8 for the region A1 [see Fig. 4(a)].With equally partitioned two zero states [(0 0 0) and (1 1 1)], SVPWM provides very low PWM ripple and provides voltage linearity for the modulation index range of 0<Mi <0.907.

As it has symmetric zero stages, from thePWM ripple reduction perspective SVPWM is the best method. But as Mi increases the ripple also increases and it looses its advantage around Mi ≈ 0.6 where discontinuous PWM methods can be used [1]. For example increasing the switching frequency by 50% and employing the DPWM1 method (of which the pulse pattern is illustrated in Fig. 9(a) for region A1∩B2 of Fig. 4), the switching count and, therefore, the switching losses remain the same (as one of the phases ceases switching during the PWM period) while the ripple of DPWM1 becomes less compared to SVPWM. Due to reduction of the total zero state duty cycles at high Mi and 50% increase of the carrier frequency (decrease of the carrier cycle), the effect of the zero states on ripple decreases and they can be lumped as one [1]. Thus, low ripple or low loss results. Consequently, SVPWM at lowMi , and DPWM1 at high Mi have been widely used. It has been illustrated that transition between methods is seamless (the load current is not disturbed) and a combination of the two methods has been successfully used in commercial drives. However, for both SVPWM and DPWM1, as shown at the bottom of the pulse pattern diagrams, the inverter CMV is high. In motor drive applications, higher CMV is associated with increased common mode current (motor leakage current), higher risk of nuisance trips, and reduced bearing life [24]–[26].

### V. SIMULATION RESULTS



**Fig.8. AZSPWM**
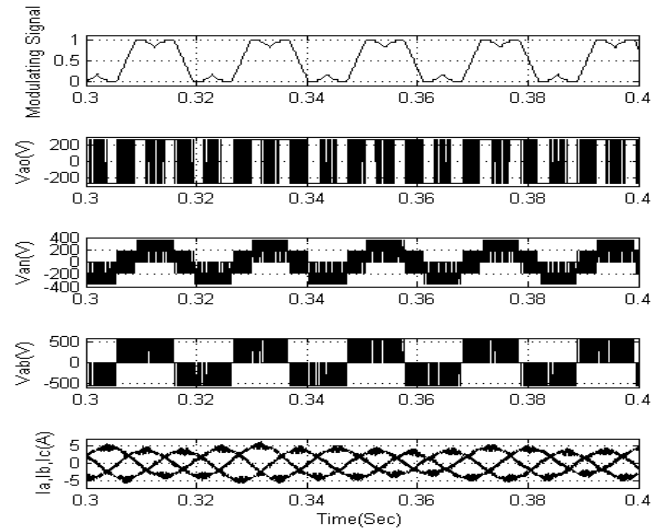


**Fig.9. DPWM0.**



**Fig.10. DPWM1.**



**Fig.11. DPWM3.**



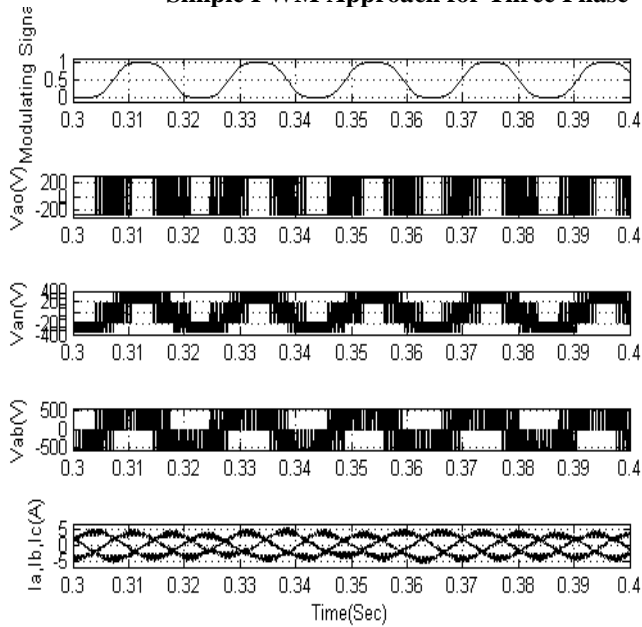**Fig.12. DPWMMAX.**



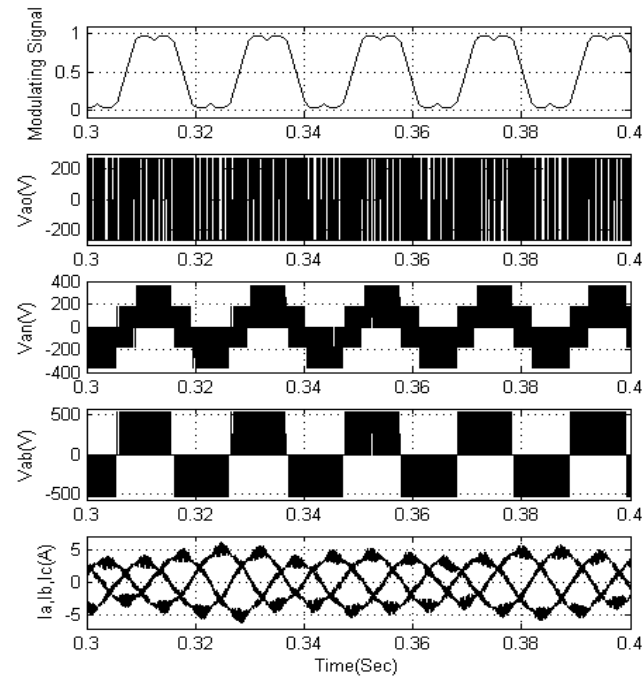**Fig.13. DPWMMIN.**

**Fig.14. NSPWM.**
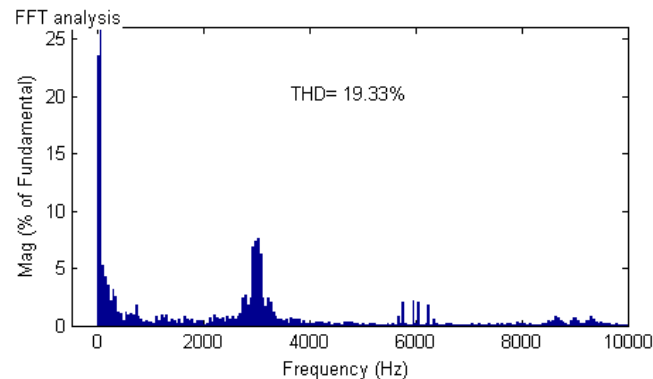


**Fig.15. SVPWM_48.**
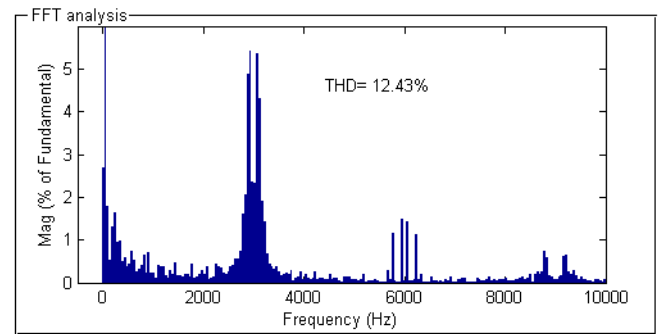


**Fig.16. FFTAnalysisToolResult_AZSVPWM.**



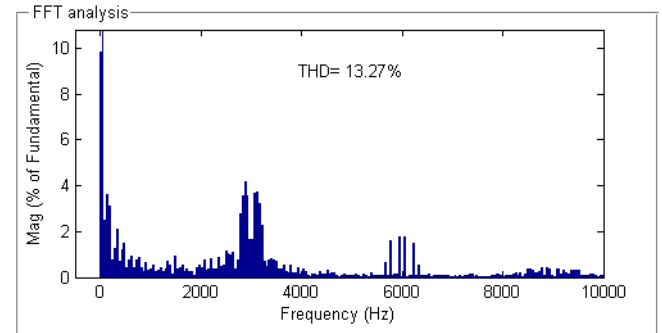**Fig.17. FFTAnalysisToolResult_DPWM1.**



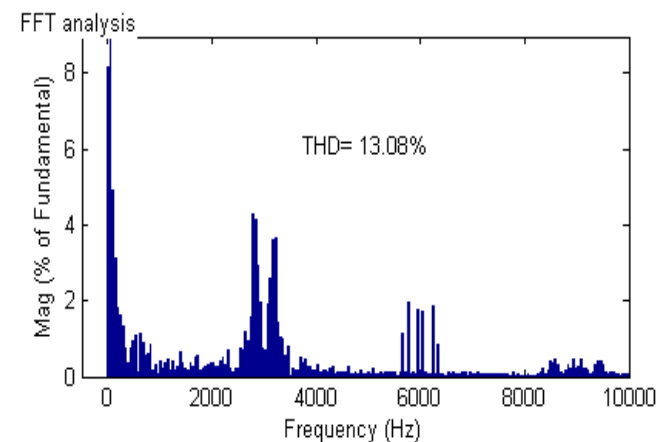**Fig.18. FFTAnalysisToolResult_DPWM2.**



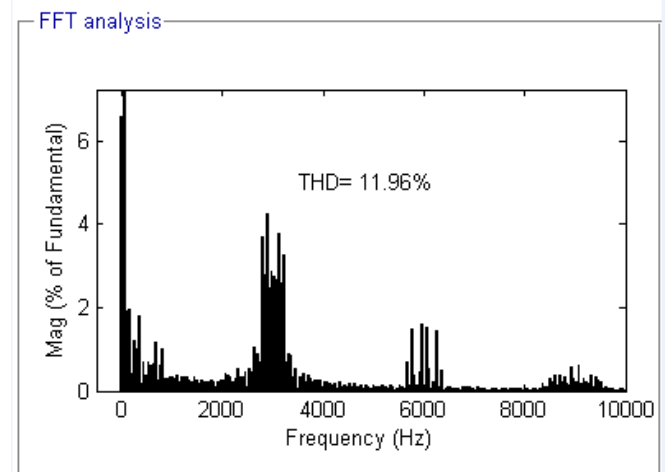**Fig.19. FFTAnalysisToolResult_DPWM3.**



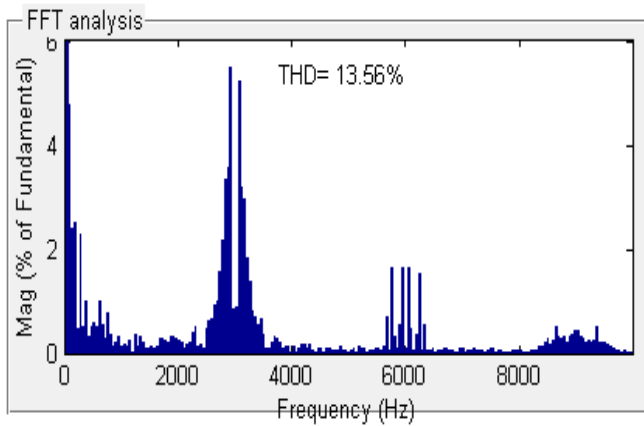**Fig.20. FFTAnalysisToolResult_DPWMIN.**

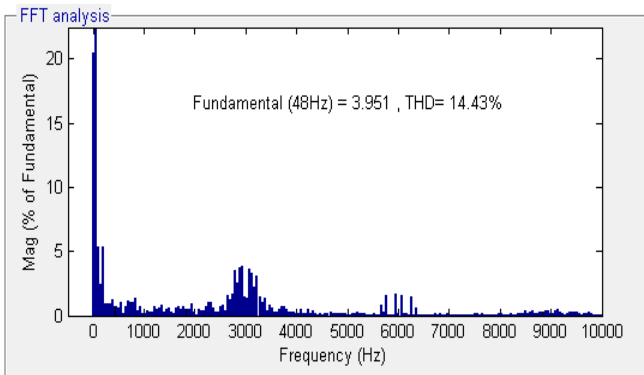**Fig.21. FFTAnalysisToolResult_DPWMMAX.**



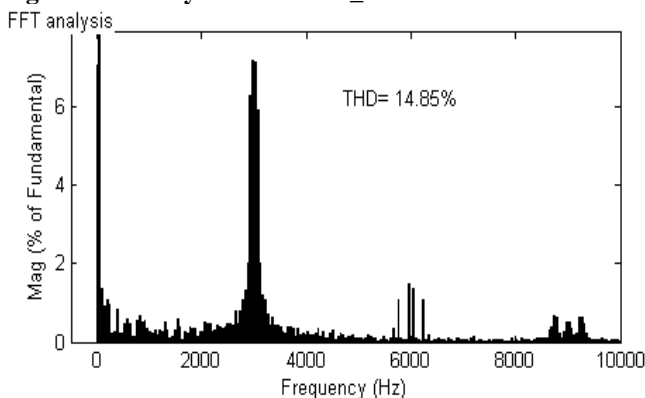**Fig22. FFTAnalysisToolResult_DPWMO.**
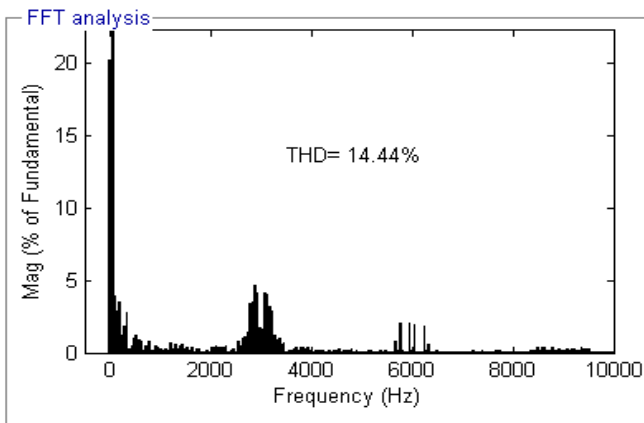


**Fig23. FFTAnalysisToolResult_NSPWM.**



**Fig.24. FFTAnalysisToolResult_SVPWM.**

## VI. CONCLUSION

PWM principles are reviewed for three-phase, three-wire inverter drives. The characteristics, pulse patterns, and implementation of the popular PWM methods are discussed. The generalized scalar PWM approach is established and it is shown that it unites the conventional PWM methods and most recently developed reduced common mode voltage PWM methods under one umbrella. Through a detailed example, the method to generate the pulse patterns of these PWM methods via the generalized scalar PWM approach is illustrated. It is shown that the generalized scalar approach yields a simple and powerful implementation with modern control chips which have digital PWM units. With this approach, it becomes an easy task to program the pulse patterns of various high performance PWM methods and benefit from their performance in modern VSIs for applications such as motor drives, PWM rectifiers, and active filters. The theory is verified by laboratory experiments. It is demonstrated that with the proposed approach both the conventional PWM pulse patterns (such as those of SVPWM and DPWM1) and the recently developed improved high-frequency common mode voltage/current performance method pulse patterns (NSPWM, AZSPWM1, and AZSPWM3) can be easily generated. Applying such pulse patterns to motor drives, it has been demonstrated that NSPWM, AZSPWM1, and AZSPWM3 methods provide good performance. Thus, the inverter design engineers are encouraged to include such pulse patterns in their designs.

## VII. REFERENCES

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