

A High-Performance Generalized Discontinuous PWM Algorithm

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Abstract—In this paper, a generalized discontinuous pulsewidth modulation (GDPWM) method with superior high modulation operating range performance characteristics is developed. An algorithm which employs the conventional space-vector PWM method in the low modulation range, and the GDPWM method in the high modulation range, is established. As a result, the current waveform quality, switching losses, voltage linearity range, and the overmodulation region performance of a PWM voltage-source inverter (PWM-VSI) drive are on-line optimized, as opposed to conventional modulators with fixed characteristics. Due to its compactness, simplicity, and superior performance, the algorithm is suitable for most high-performance PWM-VSI drive applications. This paper provides detailed performance analysis of the method and compares it to the other methods. The experimental results verify the superiority of this algorithm to the conventional PWM methods.

Index Terms—Discontinuous modulation, harmonics, inverter, pulsewidth modulation, switching losses.

I. INTRODUCTION

VOLTAGE-SOURCE inverters (VSI's) are widely utilized in ac motor drive, utility interface, and uninterrupted power supply (UPS) applications as means for dc \leftrightarrow ac electric energy conversion. As shown in Fig. 1, the classical VSI has a relatively simple structure and generates a low-frequency output voltage with controllable magnitude and frequency by programming high-frequency voltage pulses. Carrier-based PWM methods employ the "per-carrier-cycle volt-second balance" principle to program a desirable inverter output voltage waveform. Two main implementation techniques exist. In the direct digital technique, the space-vector concept is utilized to calculate the duty cycle of the inverter switching devices, and digital counters utilize the duty cycle information to program the switch gate signals [1]. In the triangle intersection technique, the reference voltage (modulation) waveforms are compared with the triangular carrier wave and the intersections define the switching instants [2]. Although the early triangle

Paper IPCSD 98-32, presented at the 1997 Applied Power Electronics Conference and Exposition, Atlanta, GA, February 23-27, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Drives Committee of the IEEE Industry Applications Society. Manuscript released for publication April 23, 1998.

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Publisher Item Identifier S 0093-9994(98)06783-8.

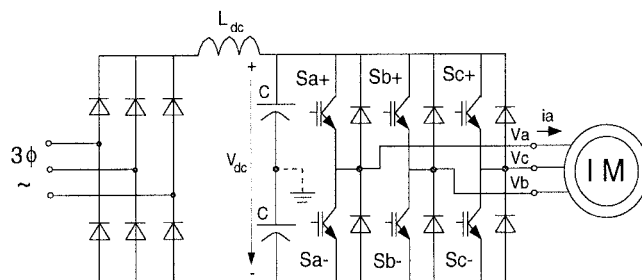


Fig. 1. Circuit diagram of a diode rectifier front-end type PWM-VSI drive.

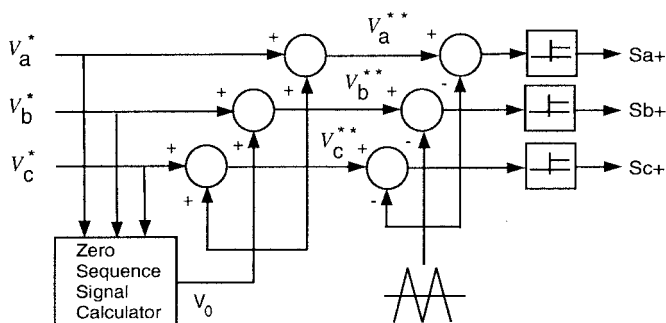


Fig. 2. Triangle-intersection-technique-based PWM employing the zero-sequence injection principle.

intersection implementations employed analog circuits, low-cost digital microelectronics have proven the viability of digital hardware/software implementations.

The absence of the neutral current path in three wire loads provides a degree of freedom in determining the duty cycle of the inverter switches. In the direct digital implementation, the degree of freedom appears as the partitioning of two zero states [3]. In a triangle intersection implementation, this degree of freedom appears in choosing the modulation wave. Any zero-sequence signal can be injected to the reference modulation waves [4], [5]. In Fig. 1, the potential difference between the three-wire load neutral point and the center point of the dc-link capacitor, v_0 , is the zero-sequence voltage, and it can be arbitrarily selected. The zero-sequence signal injection technique block diagram is illustrated in Fig. 2. In both direct digital and triangle intersection methods, the voltage linearity, waveform quality (current ripple), and switching losses are all influenced by the choice of the zero-sequence signal (zero-state partitioning). Recognizing this property, many researchers have been investigating high-performance PWM methods.

With performance and implementation simplicity being the main criteria, only a few of the many PWM methods have gained acceptance [6].

Due to its simplicity, the sinusoidal PWM (SPWM) method has found a wide range of applications since the early development of PWM-VSI technology [2]. However, the SPWM method is linear between 0% and 78.5% of six-step voltage value. Therefore, there is poor voltage utilization. Employing the zero-sequence signal injection technique, King developed an analog hardware-based PWM method [4] and illustrated the method is linear between 0% and 90.7% of six-step voltage value. Thus, King's method, also termed the space-vector PWM (SVPWM) method, significantly improves inverter voltage utilization. The following years witnessed the development of several similar modulation methods, such as the third harmonic injection PWM (THIPWM) method [5], [7], [8]. Utilizing a discontinuous type of zero-sequence signal, Depenbrock developed a modulation method with discontinuous modulation waves (later named as the discontinuous PWM (DPWM) method and hereinafter referred to as DPWM1) that also provides a wider linearity range than SPWM [9]. Since during each carrier cycle one phase ceases modulation, the associated phase is clamped to the positive or negative dc rail and the switching losses of the associated inverter leg are eliminated. Depenbrock thoroughly investigated DPWM1 and illustrated its superior voltage linearity range, reduced switching loss, and the superior high modulation range current waveform quality [9]. However, the poor low modulation range performance (narrow pulse problems and poor current waveform quality [10]) and implementation complexity have limited the application of this modulator. Prior to DPWM1, a modulation method which has similar modulation waveforms and characteristics to DPWM1 was developed by Schörner [11]. Schörner's modulator and DPWM1 are identical at the maximum voltage linearity operating point. However, at all other operating points, Schörner's method yields continuous modulation and, therefore, has higher switching losses than DPWM1.

Employing the space-vector theory, Pfaff *et al.* established the carrier-based PWM direct digital implementation technique [12]. Since modern high-performance ac drives employ vector control, programming the switch duty cycles also in the vector coordinates would be an intuitive and direct approach. Therefore, this implementation immediately gained acceptance. Skudelny *et al.* later thoroughly investigated the technique and termed the method that equally splits the two inverter zero states as the SVPWM method and illustrated its superior performance characteristics [1]. Recent studies illustrated this method is equivalent to King's method [10]. The recent digital software-based triangle intersection implementation of SVPWM also has employed King's approach to generate the modulation signal [13].

Ogasawara *et al.* developed a direct digital PWM method with superior high modulation range waveform quality and reduced switching loss characteristics suitable for induction motor drives operating near 30° lagging power factor angle [3] (minimum switching losses for 30° lagging power factor). Later, it was recognized that this space-vector-theory-based

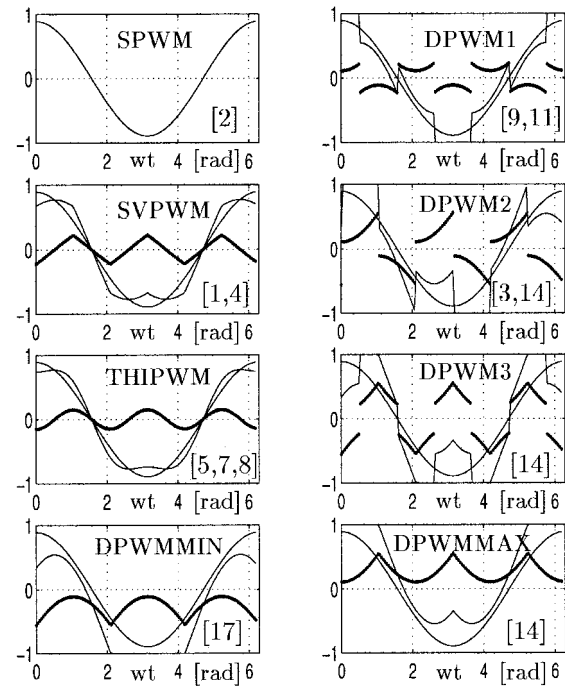


Fig. 3. Modulation waveforms of the modern PWM methods ($M_i = 0.7$).

method has a triangle-intersection-implementation-based DPWM equivalent (DPWM2) [14]. This modulator was later reinvented and termed the “minimum switching loss PWM” method (this is only true for 30° lagging power factor) [15]. The modulation waveforms of these modulators and several other popular PWM methods [14], [16], [17] are shown in Fig. 3, along with their zero-sequence signals. In the figure, unity triangular carrier wave gain is assumed and the signals are normalized to $V_{dc}/2$. Therefore, $\pm V_{dc}/2$ saturation limits correspond to ± 1 . Since the performance of a modulator is voltage-utilization (modulation-index) dependent, at this stage a modulation index definition is required.

Modulation Index: For a given dc-link voltage V_{dc} , the ratio of the fundamental component magnitude of the line-to-neutral inverter output voltage V_{1m} to the fundamental component magnitude of the six-step mode voltage $2V_{dc}/\pi$ is termed the modulation index M_i [6]:

$$M_i = \frac{V_{1m}}{\frac{2}{\pi}V_{dc}}. \quad (1)$$

As discussed in detail in [6], [10], [16], and [18], the performance of the popular PWM methods is modulation-index dependent, and no single modulator provides a satisfactory performance over a very wide modulation range. Therefore, a high-performance drive with a wide operating range must combine at least two PWM methods and on-line select a proper modulator as a function of the modulation index. In the lower modulation range, the modulation methods with continuous modulation wave (CPWM methods) are superior to DPWM methods, while in the higher modulation range, the opposite is true. Therefore, in the low modulation range, SVPWM is superior to all other modulators due to its superior performance and implementation simplicity [13]. In the high modulation

region, DPWM methods are superior to SVPWM and the other CPWM methods. However, the DPWM method of choice depends on the performance criteria, and no modulator has an overall superior performance. The switching losses, waveform quality, and voltage linearity characteristics are different in each DPWM method. Therefore, selecting only two PWM methods (SVPWM and a DPWM method) results in a less than optimal performance, while employing more than two PWM methods substantially increases the algorithm complexity. A simple DPWM method with on-line controllable characteristics would be a superior and practically realizable approach.

This paper develops a high performance generalized DPWM (GDPWM) method and an algorithm combining GDPWM with SVPWM to maximize the drive performance in the whole modulation range. First, the GDPWM method is described, then the modulator characteristics are studied and compared to the other popular methods to illustrate its performance superiority. Finally, laboratory test results are illustrated to verify the capabilities of the method. This paper will focus on the triangle intersection implementation (digital hardware/software based), however, the algorithm can be employed in a direct digital implementation, also. The recent Ph.D. dissertation by Reinold [18] and this paper have important similarities. However, this paper provides more detailed analysis, more global approach, simpler implementations, and a thorough modulator design method.

II. THE GDPWM METHOD

A careful examination of the DPWM1 and DPWM2 modulation waveforms of Fig. 3 indicates that there exists a 30° phase-angle distance between their dc-rail clamped 60° segments. While in DPWM1 the center of each dc-rail clamped segment is aligned with the cosine modulation wave peak, in DPWM2 a 30° phase difference exists. The modulation signals of the two methods are similar to each other and, furthermore, the magnitude rules involved in generating them are similar [10]. The minimum switching loss characteristic of DPWM1 under unity power factor operating condition and of DPWM2 under 30° lagging power factor is intuitive. In each case, the dc-rail clamped switch conducts the largest current, and minimum switching losses are obtained. In fact, this characteristic has been the reason for the development and widespread use of these modulators. However, under different power factor operating conditions than those described, the performance of these modulators degrades. Following the recognition of the similarities between these modulators, an attempt toward unifying them in this research has lead to the development of a high-performance GDPWM method [10].

GDPWM is a DPWM method which covers a range of modulators, including the DPWM1 and DPWM2 methods. Fig. 4 illustrates the zero-sequence signal generation method of GDPWM. For illustration purposes, the triangular carrier wave peak-to-peak voltage is scaled to the VSI dc-link voltage V_{dc} . Therefore, the modulator saturates at a signal value larger than $\pm V_{dc}/2$. To aid the description of GDPWM, it is useful to define the modulator phase angle ψ increasing from the intersection point of the two reference modulation waves at

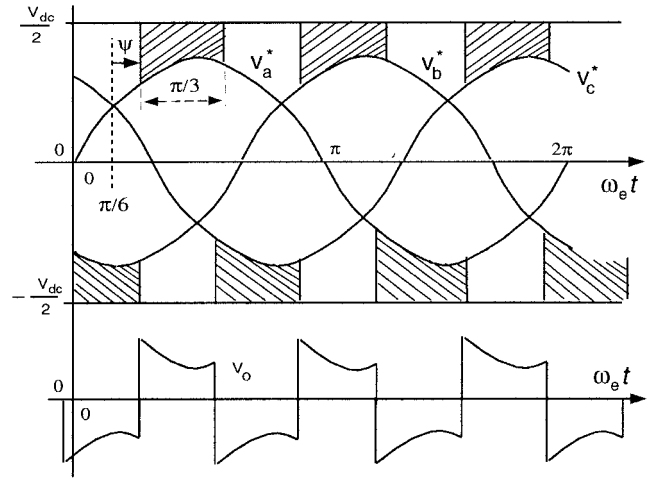


Fig. 4. Generalized DPWM zero-sequence signal generation method; ψ is the only control parameter.

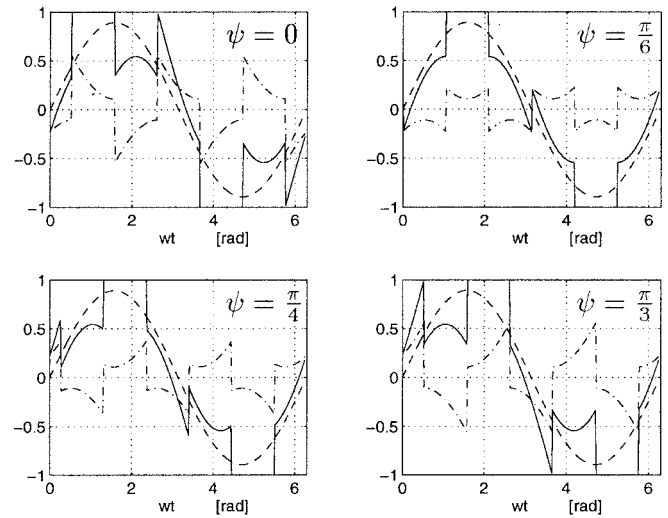


Fig. 5. GDPWM method modulation waves ("—"), their zero-sequence signal ("--") and the fundamental component ("· · ·") for $M_i = 0.7$ and four different modulator phase-angle values.

$\omega_e t = \pi/6$, as shown in Fig. 4. From ψ to $\psi + \pi/3$, the zero-sequence signal is the shaded signal which is equal to the difference between the saturation line ($V_{dc}/2$) and the reference modulation signal which passes the *maximum magnitude test*. In the *maximum magnitude test*, all three reference modulation signals v_a^* , v_b^* , and v_c^* are phase shifted by $\psi - \pi/6$, and of the three new signals v_{ax}^* , v_{bx}^* , and v_{cx}^* , the one with the maximum magnitude determines the zero-sequence signal. Assume $|v_{ax}^*| \geq |v_{bx}^*|, |v_{cx}^*|$, then, $v_0 = (\text{sgn}(v_{ax}^*)) \frac{V_{dc}}{2} - v_{ax}^*$. Adding this zero-sequence signal to the three original modulation waves v_a^* , v_b^* , and v_c^* , the GDPWM waves v_a^{**} , v_b^{**} , and v_c^{**} are generated.

Since the GDPWM zero-sequence signal must not be too large to force a modulation wave outside the triangular carrier wave boundaries, the control range of ψ is confined to the interval $[0, \pi/3]$. Within this ψ range, the modulator is linear between $0.0 \leq M_i \leq \pi/2\sqrt{3} \approx 0.907$. Fig. 5 illustrates the modulation and zero-sequence waveforms for four different ψ

values and $M_i = 0.7$. Notice that DPWM1 corresponds to $\psi = \pi/6$ and DPWM2 to $\psi = \pi/3$. For $\psi = 0$, the DPWM0 method, which was reported in [14] and [19], results.

Since it only requires a phase shift operation (rotation) and several comparisons, the GDPWM method is simple and can be easily implemented on a digital signal processor (DSP) or microprocessor. Although the ψ variable is helpful in the analysis and graphic illustration of this method, in the practical implementation, a modified control variable $\psi_m = \psi - \frac{\pi}{6}$ results in reduced computations. With this variable, DPWM0 corresponds to $\psi_m = -\frac{\pi}{6}$, DPWM1 to $\psi_m = 0$, and DPWM2 to $\psi_m = \frac{\pi}{6}$ values. Employing d - q transformations and expanding the terms in a manner to minimize the computational requirements, the rotation calculation can be accomplished in the following equations:

$$v_{ax}^* = v_a^* \cos(\psi_m) - \frac{(v_c^* - v_b^*)}{\sqrt{3}} \sin(\psi_m) \quad (2)$$

$$v_{bx}^* = v_b^* \cos(\psi_m) + \left(\frac{1}{2} \frac{(v_c^* - v_b^*)}{\sqrt{3}} - \frac{\sqrt{3}v_a^*}{2} \right) \sin(\psi_m) \quad (3)$$

$$v_{cx}^* = -v_{ax}^* - v_{bx}^* \quad (4)$$

Applying the maximum magnitude test to the above signals, the switch to be clamped to the positive or negative rail is defined, and the zero-sequence signal is calculated and added. Duty cycles of the inverter switches are then computed and passed to the PWM counters.

Fig. 6 summarizes the direct digital PWM technique that employs space vectors, and it illustrates the direct digital PWM equivalent of the GDPWM method. As the figure indicates, in the direct digital implementation, the inverter zero states t_0 (000) and t_7 (111) are alternately set to zero for 60° segments. The diagram indicates that the direct digital implementation is straightforward. However, it is computationally more involved than the triangle intersection implementation [3], [20]. Therefore, the direct digital implementation is less practical. However, the space-vector coordinate illustration of the method aids visualization of these modulator characteristics, such as the voltage linearity and waveform quality which will be investigated in the following sections in detail.

The $\psi \rightarrow \pi/6$ region of GDPWM is suitable for PWM voltage-source converter (VSC) utility interface applications and ac permanent magnet (PM) motor applications where the load power factor is near unity. The DPWM2 region provides desirable performance characteristics for near 30° lagging power factor loads, such as induction motor drives. The $\psi \rightarrow 0$ region is suitable for near 30° leading power factor applications, such as induction generators. In all these cases, the phase that conducts the largest current is not switched. Therefore, the inverter switching losses are significantly reduced. It is apparent that ψ , the control parameter of GDPWM, strongly affects the inverter switching losses and waveform quality. The following sections investigate these characteristics.

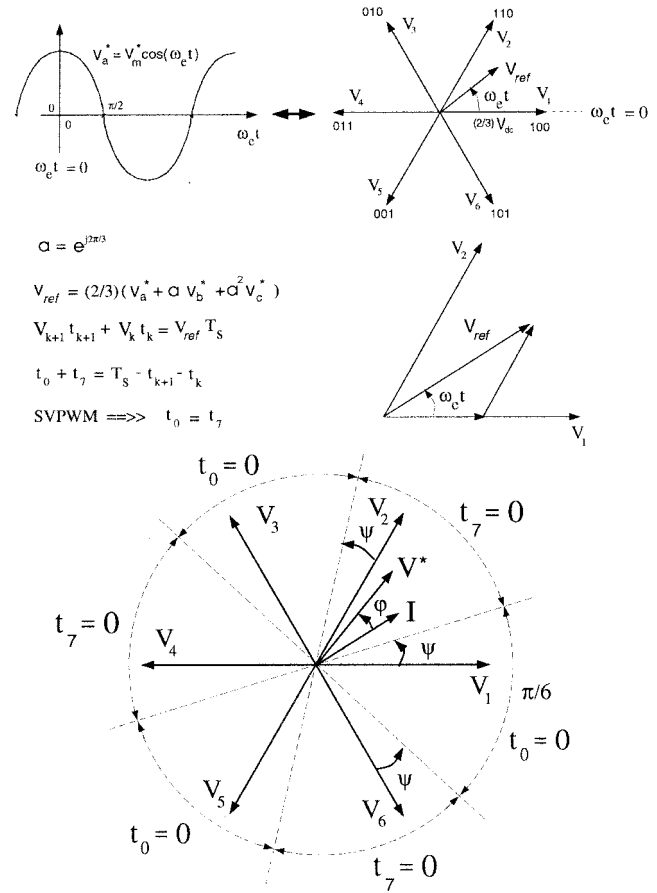


Fig. 6. Graphic summary of the direct digital PWM technique and the GDPWM method space-vector illustration.

III. WAVEFORM QUALITY

Linear modulation range inverter output current harmonics (switching-frequency harmonics) of the carrier-based PWM methods are concentrated at the carrier frequency, its sidebands, its multiples, and the sidebands of its multiples. An inverter's waveform quality is determined by the rms value (per fundamental cycle) of these harmonics. Since each zero-sequence signal (zero-state partitioning) and each modulation index value result in a unique inverter output voltage waveform, the harmonic current waveform and its rms value is unique for each modulator and modulation index value.

Since the discussed zero-sequence signal injection PWM methods have periodic zero-sequence signals, the switching signals and the harmonic currents are periodic, also. With the assumption that the carrier frequency is higher than the fundamental frequency by at least an order of magnitude and the load high frequency model can be approximated with an inductance, the harmonic current rms value of these periodic waveform modulators can be closed-form calculated as a function of the modulation index [10], [16]. To obtain a load inductance and carrier frequency independent formula, the rms harmonic current can be normalized to a base value. The resulting harmonic distortion factor (HDF) function is a polynomial which only depends on the modulation index. The

HDF of SVPWM, DPWM1, and DPWM2 are as follows [10]:

$$\text{HDF}_{\text{SVPWM}} = \frac{3}{2} \left(\frac{\pi}{4} M_i \right)^2 - \frac{4\sqrt{3}}{\pi} \left(\frac{\pi}{4} M_i \right)^3 + \left(\frac{27}{16} - \frac{81\sqrt{3}}{64\pi} \right) \left(\frac{\pi}{4} M_i \right)^4 \quad (5)$$

$$\text{HDF}_{\text{DPWM1}} = 6 \left(\frac{\pi}{4} M_i \right)^2 - \left(\frac{8\sqrt{3} + 45}{2\pi} \right) \left(\frac{\pi}{4} M_i \right)^3 + \left(\frac{27}{8} + \frac{27\sqrt{3}}{32\pi} \right) \left(\frac{\pi}{4} M_i \right)^4 \quad (6)$$

$$\text{HDF}_{\text{DPWM2}} = 6 \left(\frac{\pi}{4} M_i \right)^2 - \frac{35\sqrt{3}}{2\pi} \left(\frac{\pi}{4} M_i \right)^3 + \left(\frac{27}{8} + \frac{81\sqrt{3}}{64\pi} \right) \left(\frac{\pi}{4} M_i \right)^4 \quad (7)$$

The exact relation between the HDF function and the phase “ a ” (arbitrarily selected) harmonic current RMS value I_{ah} is as follows:

$$I_{ah}^2 = \left(\frac{V_{dc}}{24L_{\sigma}f_c} \right)^2 \times \text{HDF}(M_i). \quad (8)$$

The HDF function of the GDPWM method for any ψ value can be roughly approximated by linearly interpolating the HDF of DPWM1 (HD1) and DPWM2 (HD2), which are its two end points [10]. Since it is symmetric about $\psi = \frac{\pi}{6}$, the HDF of GDPWM (HDF_{GD}) can be written in two pieces, as follows:

$$\text{HDF}_{\text{GD}}(\psi) = \begin{cases} \left(\frac{6\psi}{\pi} \right) \text{HD1} + \left(1 - \frac{6\psi}{\pi} \right) \text{HD2}, & 0 \leq \psi \leq \frac{\pi}{6} \\ \left(2 - \frac{6\psi}{\pi} \right) \text{HD1} + \left(\frac{6\psi}{\pi} - 1 \right) \text{HD2}, & \frac{\pi}{6} \leq \psi \leq \frac{\pi}{3}. \end{cases} \quad (9)$$

Fig. 7 shows the HDF curves of all the discussed PWM methods under equal inverter average switching frequency (the HDF of the DPWM methods is multiplied by $(\frac{2}{3})^2$). The GDPWM method HDF function varies between the DPWM1 and DPWM2 HDF curves. Since the difference between the HDF of DPWM1 and DPWM2 is only noticeable in the high modulation index range and it is at most 10%–15%, the HDF of GDPWM is not a strong function of ψ . The HDF curves indicate that the CPWM methods have better HDF in the low modulation range, while the DPWM methods (including GDPWM) are superior in the high modulation range. Therefore, a high-performance PWM-VSI drive should employ at least two modulators and select a different modulator in each region. Utilizing the HDF formula, the transition point can be calculated according to the design criteria.

In the very low modulation index range, all CPWM methods have practically equal HDF. However, as M_i increases, the SPWM performance rapidly degrades, while the remaining CPWM methods maintain low HDF over a fairly wide range. The THIPWM method with the theoretically minimum HDF (THIPWM1/4 with $v_{0\text{opt}} = \frac{V_{dm}}{4} \sin 3\theta$) [8] has only slightly smaller HDF than SVPWM and the conventional THIPWM

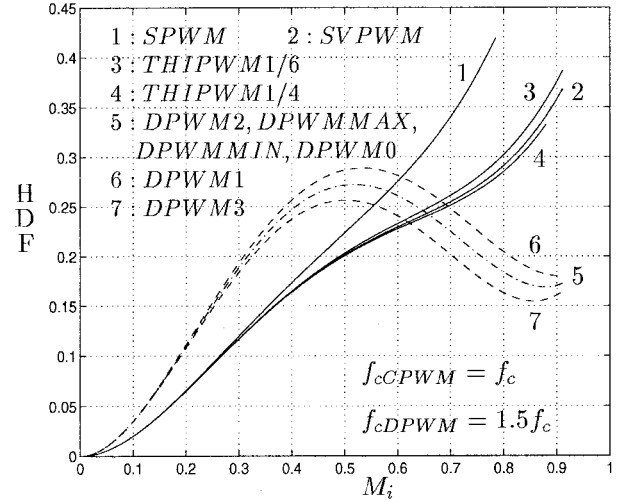


Fig. 7. HDF = $f(M_i)$ curves in the linear modulation range under equal inverter average switching frequency.

(THIPWM1/6 with $v_0 = \frac{V_{dm}}{6} \sin 3\theta$). Since SVPWM is easier to implement and has a wider voltage linearity range, it is superior to all CPWM methods [10]. Therefore, a high-performance drive should employ SVPWM in the low modulation index range.

In the high modulation index range, as Fig. 7 indicates, DPWM methods are superior to SVPWM. Therefore, in the high modulation index region, DPWM methods should be selected. The intersection point of the DPWM method of choice and the SVPWM HDF curves define the optimal transition point. Although in the high modulation range the DPWM3 method has less HDF than the other DPWM methods, the difference is negligible. Therefore, the DPWM method selection criteria can be based on the switching loss characteristics or voltage linearity characteristics which are stronger functions of the DPWM methods. Since it sweeps a wide range of modulation waveforms, the GDPWM method has the potential of optimizing these performance characteristics. Therefore, a clear understanding of the switching loss mechanism and the voltage linearity characteristics of DPWM methods is required.

IV. SWITCHING LOSSES

The switching losses of a PWM-VSI drive are load-current dependent and increase with the current magnitude. Switching device manufacturers' databooks (for example, insulated gate bipolar transistor (IGBT) device databooks [21]) indicate this relation is approximately linear, i.e., the switching losses are proportional to the current magnitude.

With CPWM methods, all three phase currents are commutated within each carrier cycle of a full fundamental cycle. Therefore, for all CPWM methods, the switching losses are the same and independent of the power factor. With DPWM methods, however, the switching losses are significantly influenced by the modulation method and load power factor angle. DPWM methods cease to switch each switch for a total of 120° per fundamental cycle and the location of each dc-rail clamped segment with respect to the modulation wave fundamental component phase is modulator type dependent.

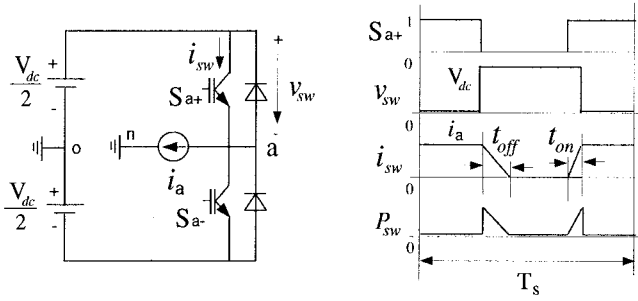


Fig. 8. PWM-VSI single-phase model for commutation analysis and per-carrier-cycle switching loss diagram under linear commutation.

Therefore, the load power factor and the modulation method together determine the time interval that the load current is not commutated. Since the switching losses are strongly dependent on, and linearly increase with, the magnitude of the commuting phase current, selecting a DPWM method with reduced switching losses can significantly contribute to the performance of a drive. Therefore, it is necessary to characterize and compare the switching losses of DPWM methods.

Assuming the inverter switching devices have linear current turn-on and turnoff characteristics with respect to time and accounting only for the fundamental component of the load current, the switching losses of a PWM-VSI drive can be analytically modeled [14]. As shown in Fig. 8, the single-phase inverter model and the switching voltage/current diagram aid in calculating the switching losses. The average value of the local (per carrier cycle) switching loss over the fundamental cycle $P_{s\text{ wave}}$ can be calculated as follows:

$$P_{s\text{ wave}} = \frac{1}{2\pi} \frac{V_{dc}(t_{on} + t_{off})}{2T_s} \int_0^{2\pi} f_i(\theta) d\theta. \quad (10)$$

In the above formula, t_{on} and t_{off} variables represent the turn-on and turnoff times of the switching devices, and $f_i(\theta)$ is the switching current function. The switching current function $f_i(\theta)$ equals zero in the intervals where modulation ceases and the absolute value of the corresponding phase current value elsewhere. For example, for phase "a," this function is as follows:

$$f_{ia}(\theta) = \begin{cases} 0, & |v_a^{**}| \geq \frac{V_{dc}}{2} \\ |i_a|, & |v_a^{**}| < \frac{V_{dc}}{2}. \end{cases} \quad (11)$$

The calculation assumes steady-state operating conditions, where the currents are practically sinusoidal functions. Therefore, (10) is a function of the load power factor angle and the current magnitude. As a result, the power factor angle φ enters the formula as the integral boundary term. Normalizing $P_{s\text{ wave}}$ to P_o , the switching loss value under CPWM condition (which is φ independent), the switching loss function (SLF) of a DPWM method can be found:

$$P_o = \frac{V_{dc} I_{\max}}{\pi T_s} \times (t_{on} + t_{off}) \quad (12)$$

$$\text{SLF} = \frac{P_{s\text{ wave}}}{P_o}. \quad (13)$$

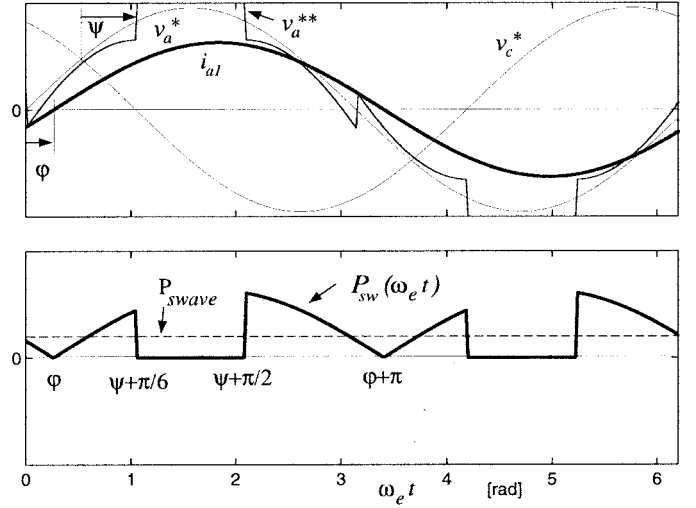


Fig. 9. The average switching losses of GDPWM, $P_{s\text{ wave}} = f(\psi, \varphi)$.

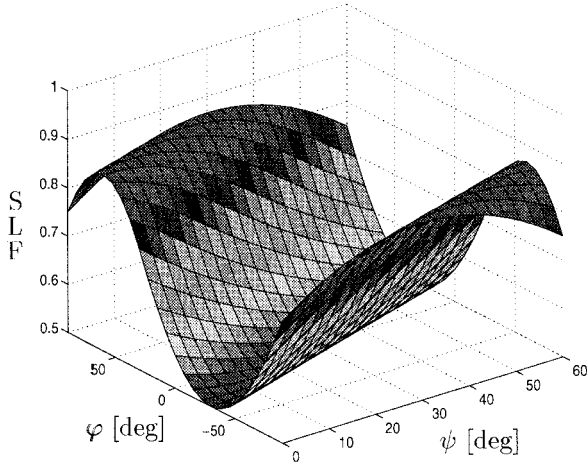
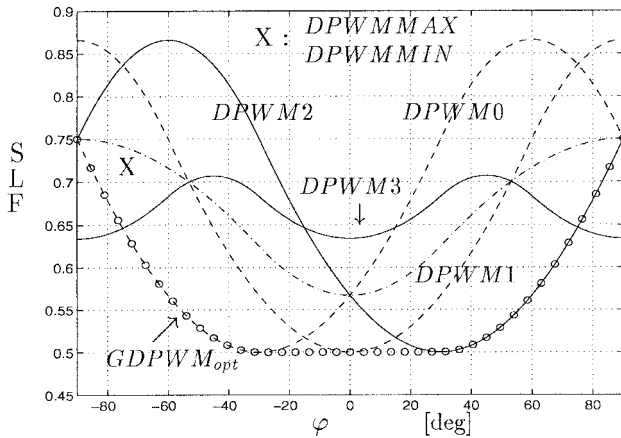
In (12), the variable I_{\max} represents the load current fundamental component maximum value. By the definition of (10), the SLF of CPWM methods is unity. The SLF of DPWM methods can be easily calculated with the above procedure. Fig. 9 shows the ψ - and φ -dependent switching current and switching loss function waveforms of GDPWM. Applying the procedure to GDPWM yields the following SLF:

$$\text{SLF}_{\text{GDPWM}} = \begin{cases} \frac{\sqrt{3}}{2} \cos\left(\frac{4\pi}{3} + \psi - \varphi\right), & -\frac{\pi}{2} \leq \varphi \leq -\frac{\pi}{2} + \psi \\ 1 - \frac{1}{2} \sin\left(\frac{\pi}{3} + \psi - \varphi\right), & -\frac{\pi}{2} + \psi \leq \varphi \leq \frac{\pi}{6} + \psi \\ \frac{\sqrt{3}}{2} \cos\left(\frac{\pi}{3} + \psi - \varphi\right), & \frac{\pi}{6} + \psi \leq \varphi \leq \frac{\pi}{2}. \end{cases} \quad (14)$$

The SLF of DPWM0, DPWM1, and DPWM2 can be easily evaluated from (14) by substituting $\psi = 0$, $\psi = \pi/6$, and $\psi = \pi/3$. The SLF of the remaining DPWM methods are reported in [10].

As shown in Fig. 10, the SLF surface of GDPWM indicates that its switching losses are a strong function of φ , and they can be minimized by controlling ψ as a function of φ . It is apparent from the figure that the SLF surface touches the SLF = 0.5 plane along a straight line. In the $-\pi/6 \leq \varphi \leq \pi/6$ region, selecting $\psi = \varphi + \pi/6$ results in minimum switching loss value ($\text{SLF}_{\min} = 0.5$), which is equal to 50% of the CPWM methods ($\text{SLF}_{\text{CPWM}} = 1.0$). Outside this range, the modulator phase angle must be held at the boundary value of $\psi = \pi/3$ (DPWM2) for positive φ and at the value of $\psi = 0$ (DPWM0) for negative φ , so that the GDPWM voltage linearity is retained. As a result, in these operating regions, the switching losses become more than 50% and less than 75% of the switching losses of CPWM methods, and the exact amount can be found from the three-dimensional (3-D) SLF surface of Fig. 10.

Fig. 11 shows the SLF characteristics of the modern DPWM methods, along with the optimum SLF solution of the GDPWM method. Note that, outside the $-75^\circ \leq \varphi \leq 75^\circ$

Fig. 10. $SLF = f(\psi, \varphi)$ function of the GDPWM method.Fig. 11. $SLF = f(\varphi)$ characteristics of the modern DPWM methods under fixed carrier frequency constraint ($SLF_{CPWM} = 1$).

range, DPWM3 yields minimum switching losses. The graphic suggests that combining GDPWM and DPWM3 would result in optimum SLF. A control algorithm should select GDPWM within $-75^\circ \leq \varphi \leq 75^\circ$ and optimize it with the above-described ψ choice. Outside this φ range, DPWM3 should be selected. With this algorithm, the switching losses become less than 65% of the CPWM methods.

The switching loss analysis with the aid of SLF has shown that the modulator choice strongly influences the inverter efficiency and thermal design. Since the switching losses are load-power-factor-angle dependent, the modulator choice should involve the power factor. Drives mostly operating within the $-75^\circ \leq \varphi \leq 75^\circ$ range could employ an on-line SLF optimized GDPWM algorithm. Most ac motor drives, such as induction motors and PM motors belong to this category. Utility interface and UPS applications also operate near unity power factor conditions and could utilize such an algorithm. In reactive power compensation applications (PWM-VSI var compensators), the DPWM3 method could be included in the algorithm and selected outside the $-75^\circ \leq \varphi \leq 75^\circ$ range, such that both the switching losses and the HDF are minimized simultaneously.

When the performance criteria is only switching loss minimization, the above-discussed algorithms can utilize the load power factor information and select a modulation signal which minimizes the SLF. However, as the linear modulation range expires at high modulation index levels, the nonlinear modulation range performance characteristics increasingly dominate drive performance. The waveform quality, voltage gain, and dynamic performance characteristics of the drive substantially degrade and, in addition to SLF and HDF, the inverter overmodulation performance characteristics must be considered. The following section discusses the voltage linearity of GDPWM and other modern PWM methods.

V. OVERMODULATION AND VOLTAGE GAIN

In the triangle intersection PWM technique, when the modulation wave magnitude becomes larger than the triangular carrier wave peak value ($\pm V_{dc}/2$), the inverter ceases to match the reference per-carrier-cycle volt-seconds. As a result, the reference output-voltage relations become nonlinear within certain carrier cycles. SPWM's linear modulation range ends at $V_{1m}^* = V_{dc}/2$, i.e., a modulation index of $M_{LSPWM} = \pi/4 \approx 0.785$. Injecting a zero-sequence signal to the SPWM signal can flatten and contain the modulation wave within the triangle boundaries, such that the linearity range is extended to, at most, $M_{Lmax} = \pi/2\sqrt{3} \approx 0.907$. This is the theoretical inverter fundamental component voltage linearity limit [4], [5]. With the exception of THIPWM1/4, which loses linearity at $M_{LTHIPWM1/4} = \frac{3\sqrt{3}}{7\sqrt{7}}\pi \approx 0.881$, all the modern zero-sequence signal injection PWM methods are linear until M_{Lmax} .

Practically, the theoretical voltage linearity limits are further reduced due to the inverter blanking time and minimum pulsewidth (MPW) constraints. In applications that require large inverter blanking time (high-power drives) or MPW control (narrow pulses may cause significant transient overvoltages and commutation failure and increase harmonic distortion in most drives [10], [22]), the voltage linearity range is significantly reduced. With an MPW limit of t_{MPW} , a carrier cycle of T_s , and a theoretical modulator voltage linearity limit of M_{Lmax}^t , the practical modulator voltage linearity limit M_{Lmax}^p can be calculated in the following [10]:

$$M_{Lmax}^p = M_{Lmax}^t \times \left(1 - k_m \frac{t_{MPW}}{T_s}\right). \quad (15)$$

If no MPW constraint is employed, then the linearity is limited by the blanking time t_d and, in (15), replacing t_{MPW} with $2t_d$, the linearity limit can be calculated. In both cases, the k_m coefficient is 1 for DPWM methods and 2 for CPWM methods. Therefore, DPWM methods have superior voltage linearity characteristics. This is due to the fact that DPWM methods utilize only one zero state (with a long duration) in a carrier cycle, while CPWM methods have two zero states (with smaller time lengths). Since the smallest zero-state time length determines the minimum allowable pulsewidth, the DPWM methods (including GDPWM) can allow smaller minimum on time values. Hence, a higher linear modulation limit.

In the DPWM methods, the near-zero modulation index operating region also exhibits nonlinear reference output-voltage relations. Since the zero-sequence signal of DPWM methods near zero modulation index is large, injecting this signal to the sinusoidal references results in nearly saturated modulation signals. Therefore, the DPWM methods have a lower limit on the voltage linearity. The following minimum voltage linearity limit equation holds for all the discussed DPWM methods [10]:

$$M_{L\min}^P = \frac{\pi}{\sqrt{3}} \frac{t_{MPW}}{T_s}. \quad (16)$$

The nonlinear modulation region from zero modulation index until $M_{L\min}^P$ is termed the “undermodulation region.” DPWM methods experience significant performance difficulties in the undermodulation region, and operating in this region is normally avoided.

The region starting from the end of the linear modulation region of a modulator, $M_{L\max}^P$, until the six-step operating point ($M_i = 1$) is termed the overmodulation region. All modulators experience performance degradation in the overmodulation region [10]. The output voltage waveform quality degrades and results in substantial harmonic current. The output volt-seconds become substantially less than the reference; the fundamental component voltage gain decreases, and the phase of the output voltage vector deviates from the reference value. Therefore, the steady-state and dynamic performance of a drive substantially degrades in the overmodulation region.

In open-loop drives (voltage-feedforward-controlled drives with constant volts per hertz ratio), the dynamic performance requirements are not stringent. Waveform quality, switching losses, and the fundamental component voltage gain characteristics determine the overmodulation region performance [23]. A modulator with low waveform distortion, low switching losses, and high gain is desirable to operate an open-loop drive in the overmodulation region. The advantageous waveform quality and switching loss characteristics of the DPWM methods in the higher end of the linear modulation region are partially retained in the overmodulation region. The intervals without modulation wave saturation retain these characteristics, while the saturation intervals imply increasing harmonic distortion and reduced switching losses. As the six-step operation mode is approached, the waveform distortion becomes very large (large amount of subcarrier frequency harmonics are generated), while the switching losses become negligible. A detailed study indicated that GDPWM waveform quality characteristics are superior to SVPWM and other modulators in the lower portion of the overmodulation region ($M_i < 0.95$), while a switching loss comparison indicated no notable difference [10], [23]. The last performance criteria for open-loop drives is the fundamental component voltage gain characteristic. Therefore, the voltage gain characteristics of the modern PWM methods need to be investigated.

For each modulator, a unique nonlinear fundamental component voltage gain relation exists, and this relation can be closed-form calculated by means of Fourier analysis of the saturated modulation wave [10], [23]. For example, the gain

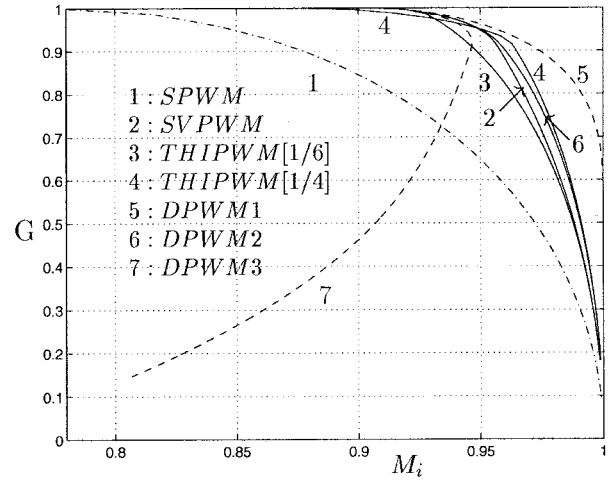


Fig. 12. $G = f(M_i)$ voltage gain characteristics of the modern modulators.

function for DPWM1 is given as follows:

$$G_{DPWM1} = \frac{M_i}{M_i^*} = \frac{\sqrt{3}}{\pi} - \frac{1}{2} - \frac{1}{M_i^*} + \left(\frac{\pi}{4\sqrt{3}} \right) \frac{1}{M_i^{*2}} + \left(\frac{3}{\pi} \right) \arcsin \left(\frac{\pi}{2\sqrt{3}M_i^*} \right) + \left(\frac{\sqrt{3}}{2M_i^*} \right) \times \sqrt{1 - \left(\frac{\pi}{2\sqrt{3}M_i^*} \right)^2}. \quad (17)$$

Fig. 12 shows the voltage gain characteristics of various PWM methods [10], [23]. As the figure indicates, except for DPWM1, all the modulators experience a substantial gain reduction in the overmodulation range (furthermore, in DPWM3, the output voltage decreases). In order to operate in the overmodulation range, such modulators require a wide modulation signal range (increased word length in digital systems and a wide voltage range in analog systems). However, this either increases the processor cost or reduces modulation waveform resolution, which degrades performance. Therefore, the DPWM1 voltage gain characteristic is superior to all other modern PWM methods [23].

As DPWM1 and DPWM2 voltage gain characteristics indicate, the GDPWM method voltage gain is a function of ψ , and $\psi = \pi/6$ provides maximum gain (DPWM1). In particular, in the high end of the overmodulation range, a small deviation from $\psi = \pi/6$ value results in a large gain reduction. Therefore, the $\psi = \pi/6$ is the optimal gain point and should be selected to fully utilize the resolution range of the digital/analog PWM circuit. This final argument suggests the GDPWM method has superior overall performance in the overmodulation region and, with its optimal voltage gain characteristic, the $\psi = \pi/6$ operating point should be selected.

In the late 1980's, Stanke and Nyland recognized the performance deficiency of SPWM in the high modulation region and developed an algorithm for high-power drives which selects a programmed-pulse PWM (often termed “optimal PWM”) method in the high modulation (including the overmodulation) region [24]. At high modulation levels, the optimized pulse pattern is similar to the pulse pattern of DPWM1, however, the

approach has limited dynamic performance. Transitions from SPWM to the programmed-pulse pattern with low transients is only possible at specific angles, and the algorithm is involved. Therefore, the GDPWM approach that extends the modulator linearity as much as possible without degrading the drive dynamic performance is superior in most applications, including the high-power drives with near megawatt ratings.

In closed-loop drives (current/flux/torque-regulated drives widely employing vector control principles), the dynamic performance requirements are stringent. In addition to the waveform quality and switching losses, the modulator voltage phase and magnitude relations determine the overmodulation region performance [25]. The GDPWM phase angle ψ can be controlled in a manner to reduce the phase or magnitude error of the inverter output voltage vector, hence, improving the dynamic performance. The closed-loop drive overmodulation issues are involved [10], [25] and will not be further discussed in this paper.

VI. A HIGH-PERFORMANCE PWM ALGORITHM

The performance analysis conducted thus far clearly shows that selecting SVPWM in the lower end of the linear modulation range and GDPWM in the remainder results in a superior overall performance when compared to the conventional PWM methods. To maximize the drive performance, the transition point from SVPWM to GDPWM and the ψ value of GDPWM must be properly selected. As the previous sections indicate, the transition point from SVPWM to GDPWM is determined by the waveform quality characteristics, while the GDPWM modulator phase angle ψ is determined from the switching loss and voltage gain characteristics. Fig. 13 shows the on-line modulator selector flow diagram of the proposed algorithm. Simple in structure and computational procedure, the algorithm requires only two transition modulation indices and φ as optimization parameters. With φ on-line estimated, the algorithm on-line calculates the optimal ψ to maximize the drive performance.

The transition value $M_{i\ tr2}$ is determined by the GDPWM linearity limit from (15) for $k_m = 1$. However, the optimal value of $M_{i\ tr1}$ depends on the carrier frequency value, as well as the SLF and HDF characteristics. To assist in selecting this transition value, the HDF curves of SVPWM and GDPWM for various carrier frequency values are compared in Fig. 14 for $\psi = \pi/4$ (approximate average value over $0 \leq \psi \leq \pi/3$). As the figure indicates, depending on the carrier frequency value, three practical cases can be distinguished.

- 1) Constant carrier frequency ($f_c = \text{const.}$)—As Fig. 14 indicates, the theoretical HDF curves of SVPWM and GDPWM do not intersect and SVPWM is superior to GDPWM until $M_{i\ tr1}$ (calculated from (15) for $k_m = 2$). As a result, transition from SVPWM to GDPWM at a point before $M_{i\ tr1}$ implies an increase in the current waveform distortion. However, according to Fig. 10, with early entrance to GDPWM, the switching losses can be reduced by as much as 50%. If the waveform quality requirements are not stringent, the $M_{i\ tr1}$ value should be selected as small as possible. Given an HDF

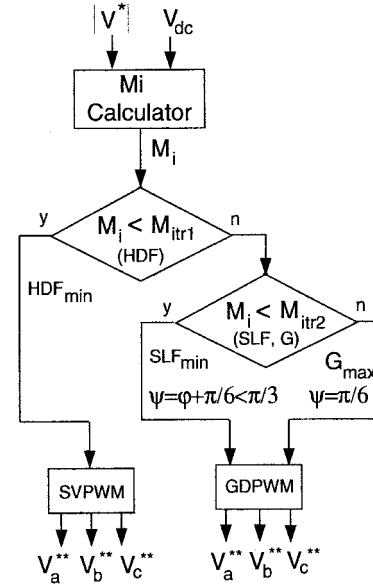


Fig. 13. The combined high-performance PWM algorithm flow diagram.

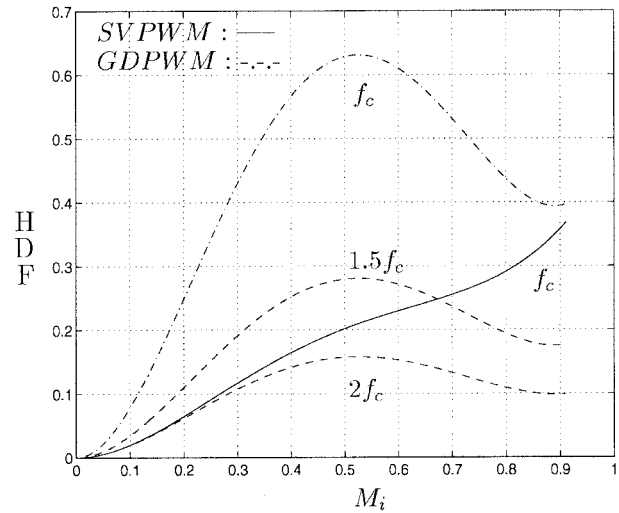


Fig. 14. HDF = $f(M_i)$ curves of SVPWM and GDPWM for various carrier frequency values illustrate the optimal transition points/regions.

limit, the $M_{i\ tr1}$ transition point can be easily determined from Fig. 14. More precise calculations to determine its value could involve (8) and (15) [10].

- 2) Constant inverter average switching frequency ($f_{s\ wave} = \text{const.}$)—In this case, the carrier frequency for the SVPWM case is selected as f_c and for GDPWM as $1.5f_c$, such that the inverter average switching frequency $f_{s\ wave}$ remains constant. The HDF curves of Fig. 14 indicate the intersection point of SVPWM and GDPWM is at $M_{i\ tr1} \approx 0.65$. Therefore, this $M_{i\ tr1}$ value minimizes the HDF of the drive and, under this condition, the switching losses in the GDPWM mode are reduced by, at most, 25% when compared to SVPWM.
- 3) Constant switching losses ($P_{s\ wave} = \text{const.}$)—In this case, the carrier frequency for the SVPWM case is

selected as f_c and for GDPWM as $2f_c$, such that the inverter switching losses $P_{s\text{wave}}$ remain constant (this is true for $-30^\circ \leq \varphi \leq 30^\circ$ where the optimal SLF of GDPWM is 0.5). Fig. 14 indicates that the SVPWM and GDPWM method curves are close together until near a modulation index of 0.3, then GDPWM method becomes superior. With this approach, smallest possible $M_{i\text{tr1}}$ becomes equal to the undermodulation limit of GDPWM defined in (16). Fig. 14 indicates, in applications with small current ripple requirement, $M_{i\text{tr1}} \approx 0.3$ would yield superior performance.

The full PWM algorithm can be easily and efficiently programmed in a microprocessor or a DSP, leading to a low-cost high-performance drive. Since the transition from SVPWM to GDPWM only involves a zero-sequence signal, oscillatory transitions do not affect the load current fundamental component and motion control. Only the switching frequency harmonic content changes. The computational requirements of the algorithm (including the modulation signal generation) are only slightly higher than the conventional modulation methods. Thus, the algorithm is suitable over a wide range of applications where low cost, high performance, and high energy efficiency are in demand. Perhaps, the most suitable applications of the combined algorithm are the future generation multipurpose intelligent drives. With the controller tuning the modulator on-line for the application, or by allowing the user to configure the modulator of his/her choice, an increased level of performance and satisfaction to the customer would result. Therefore, it is believed that this algorithm will be an indispensable feature of future-generation drives.

Note that a PWM algorithm which is solely based on bus clamping the inverter leg corresponding to the phase with the largest current [26] does not guarantee voltage linearity (including the low modulation index range) except for the power factor angle range of $-30^\circ < \varphi < 30^\circ$. If the power factor angle is outside this range, and the phase with the largest current is selected to be clamped to the positive/negative dc rail, the zero-sequence signal generated becomes too large in magnitude. Regardless of the modulation index value, at least one of the two remaining modulation signals saturates, and nonlinear modulation results. Therefore, the approach proposed in this paper, which utilizes the power factor information and selects a ψ with the highest possible overall performance, is superior and more reliable.

VII. EXPERIMENTAL RESULTS

The high-performance PWM algorithm, which combines the SVPWM and GDPWM method superior performance characteristics, was tested in the laboratory on a constant volts-per-hertz-controlled 5-hp induction motor drive. The three-phase 460-V 21-A 10-hp PWM-VSI utilized a diode rectifier front end with a dc-bus voltage of 620 V. The PWM-VSI drive control board was fully digital and employed a 40-MHz 24-b fixed-point DSP. The digital PWM algorithm employed the triangle intersection technique, and a simple software code generated the modulation signals. The carrier frequency was fixed at 5 kHz, and modulation waves were fed

to the digital PWM counters to generate the VSI gate switch signals. The drive had a 4- μ s blanking time and, through symmetric blanking time compensation, the voltage pulses were precisely generated. A minimum pulsewidth control algorithm was employed and, through a pulse elimination method (PEM), voltage pulses less than 12 μ s were eliminated.

The DSP computed the SVPWM zero-sequence signal by comparing the three reference signals and multiplying the signal with the smallest magnitude by 0.5. The GDPWM modulation waveforms were computed by the algorithm described in Section II. The GDPWM method employed the minimum SLF control algorithm ($\psi = \varphi + \frac{\pi}{6} \leq \frac{\pi}{3}$ for motoring) until the end of the linear region. The phase difference between a modulation wave and the corresponding phase current was measured to estimate φ . In the overmodulation region, an inverse gain compensation method was employed. A dc-bus voltage disturbance decoupling algorithm was also employed to reduce the sensitivity of the drive to dc-bus voltage variations [10].

Since the carrier frequency was fixed at 5 kHz, the transition point from SVPWM to GDPWM was determined by the linearity limit of SVPWM (with 12- μ s PEM control), which was calculated from (15) as $M_{i\text{tr1}} = 0.798$. However, the experimental observation suggested that the current waveform quality with SVPWM did not immediately degrade and was slightly better than with GDPWM until approximately 0.81. Therefore, the transition value was selected as $M_{i\text{tr1}} = 0.81$. Figs. 15–17 illustrate the modulator reference voltage and motor phase current waveforms immediately before, during, and after transition ($M_i = 0.79, 0.81, 0.82$) under 50% of the rated motor torque (T_{eR}). As shown in the same oscillograms, the modulation waves were output from the DSP through an A/D converter and the carrier signal voltage gain is 10 V/620 V. The current waveform quality of all three figures, in particular the peak current ripple, is practically the same. Since the speed reference signal of the drive is fed to the DSP through an A/D converter, at the transition modulation index operating point ($M_i = M_{i\text{tr1}}$) a small reference signal noise results in an oscillation between SVPWM and GDPWM. However, this zero-sequence signal oscillation only affects the carrier frequency harmonic content of the motor current and, as Fig. 16 shows, it does not disturb the motor current fundamental component and motion quality. Therefore, it is not necessary to prohibit modulator oscillations with any control algorithms. Since the carrier frequency is constant, changing from SVPWM to GDPWM results in significant reduction in switching losses. With φ at this operating point being larger than 30° (Fig. 17 indicates $\varphi \approx 40^\circ$), the SLF curve in Fig. 11 indicates the losses are reduced by at least 45% when compared to SVPWM.

The GDPWM linear modulation limit with 12- μ s PEM control is $M_{L\text{max}} = 0.85$ [calculated from (15)]. Beyond this point, the voltage gain criteria becomes more important than the SLF optimization criteria, and a transition to DPWM1 ($\psi = 30^\circ$) is required. However, the experimental study indicated transition at a modulation index value as high as 0.86 did not cause noticeable waveform quality degradation. Therefore, $M_{i\text{tr2}} = 0.86$ was selected. As a result, within

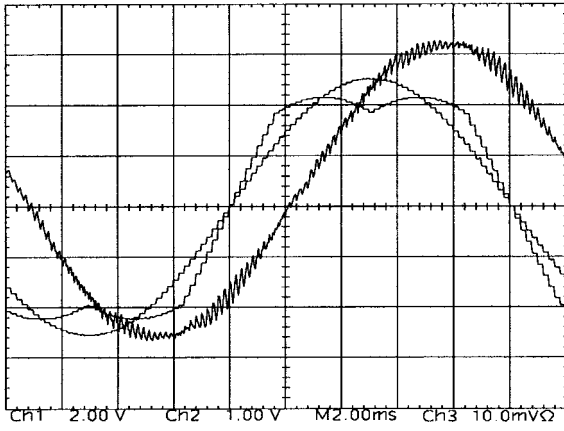


Fig. 15. Experimental SVPWM modulation wave, its fundamental component, and the motor current waveforms ($M_i = 0.79$, 49 Hz, 50% T_{eR}). Scaling: 2 A/div, 2 V/div, and 2 ms/div.

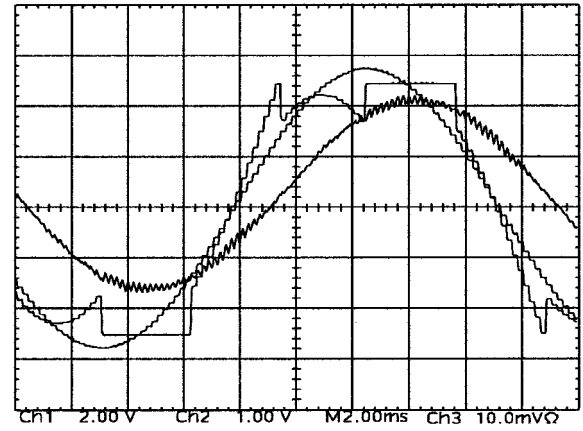


Fig. 18. Experimental GDPWM modulation wave, its fundamental component, and the motor current waveforms ($M_i = 0.854$, 53 Hz, 100% T_{eR}) with $\psi = \varphi + 30^\circ \leq 60^\circ$. Scaling: 5 A/div, 2 V/div, and 2 ms/div.

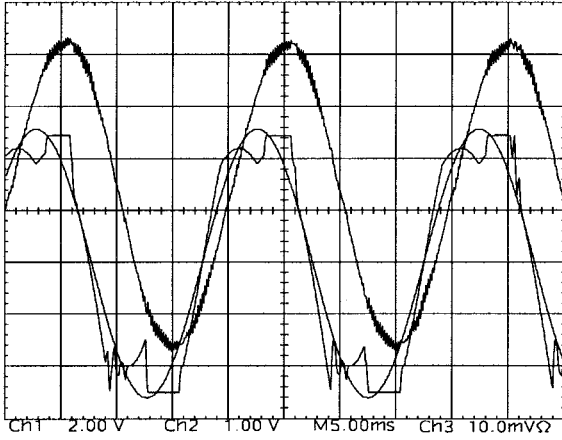


Fig. 16. Transition from SVPWM to GDPWM ($M_i = 0.81$, 50 Hz, 50% T_{eR}) with $\psi = \varphi + 30^\circ \leq 60^\circ$. Scaling: 2 A/div, 2 V/div, and 5 ms/div.

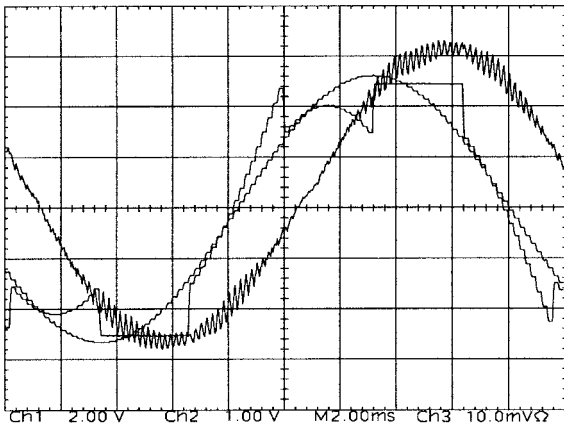


Fig. 17. Experimental GDPWM modulation wave, its fundamental component, and the motor current waveforms ($M_i = 0.82$, 51 Hz, 50% T_{eR}) with $\psi = \varphi + 30^\circ \leq 60^\circ$. Scaling: 2 A/div, 2 V/div, and 2 ms/div.

$0.81 < M_i < 0.86$, the GDPWM method reduces the switching losses significantly and maintains high waveform quality.

As shown in Fig. 18, at $M_i = 0.854$ and 100% T_{eR} , the algorithm on-line optimizes ψ to minimize the switch-

TABLE I
SVPWM AND OPTIMAL GDPWM THERMAL PERFORMANCE DATA

Method	M_i	T_L %	I_{max} (A)	T ($^\circ\text{C}$)
SVPWM	0.79	50	6	31.2
GDPWM _{opt}	0.81	50	6	30.6
GDPWM _{opt}	0.854	100	10	30.8

ing losses. Since the power factor angle for this operating condition is less than 30° , the transistor which conducts the largest current is held on, and this reduces the switching losses by approximately 50% when compared to SVPWM. Confirming the improvement in the switching losses, the laboratory measurements showed a notable decrease in the heat sink temperature. The experimental heat sink temperature data for these and the above-discussed operating conditions is illustrated in Table I in detail. The laboratory dynamometer power rating limited the experiment to a 5-hp motor and the inverter could not be fully loaded (the inverter rating is 10 hp). Therefore, the heat sink temperatures were relatively low. The table indicates the GDPWM full motor load heat sink temperature and switching losses are less than SVPWM under 50% motor load. Hence, there are improved energy efficiency and reduced thermal stress.

Above $M_{i\text{tr}2}$, the GDPWM algorithm on-line selects $\psi = \frac{\pi}{6}$ for maximum voltage gain, and the inverse-gain-compensated modulator operates in the overmodulation range. Figs. 19 and 20 show the modulator and motor phase current waveforms during and after transition to the nonlinear modulation range ($M_i = 0.86, 0.903$). As the figures indicate, oscillation of ψ during transition does not distort the fundamental component current, and motion quality is not affected. As the HDF curves of Fig. 7 suggest, in the upper linear modulation range, the phase current ripple of GDPWM decreases as the modulation index increases. In the overmodulation range, the switching losses are reduced by at least 40% when compared to SVPWM. As the modulation index is further increased, a large amount of subcarrier frequency voltage/current harmonics are generated, and the waveform quality degrades. However, as Figs. 21 and 22 indicate, the modulated segments of the current waveform

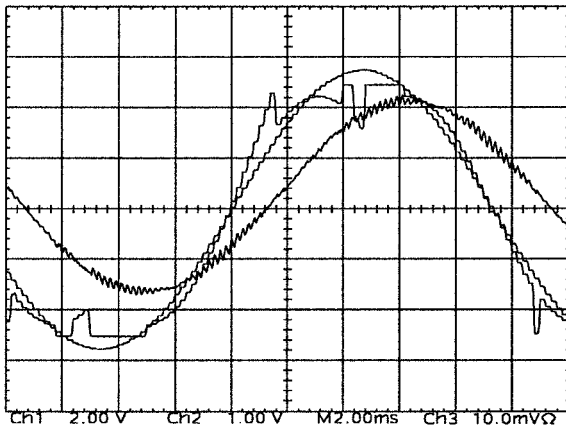


Fig. 19. Transition of GDPWM from $\psi = \varphi + 30^\circ$ to $\psi = 30^\circ$ ($M_i = 0.86$, 54 Hz, 100% T_{eR}). Scaling: 5 A/div, 2 V/div, and 2 ms/div.

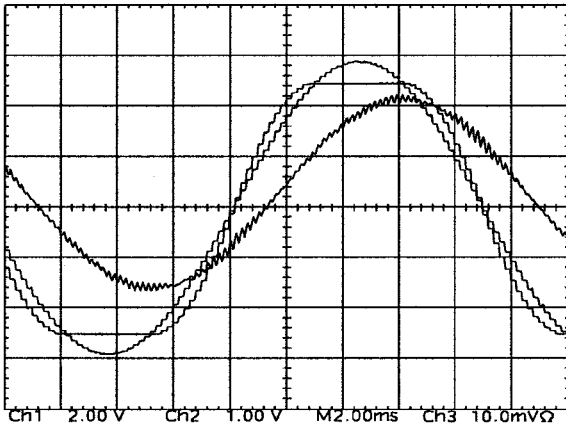


Fig. 20. Experimental GDPWM modulation wave, its fundamental component, and the motor current waveforms ($M_i = 0.903$, 56 Hz, 100% T_{eR}) with $\psi = 30^\circ$. Scaling: 5 A/div, 2 V/div, and 2 ms/div.

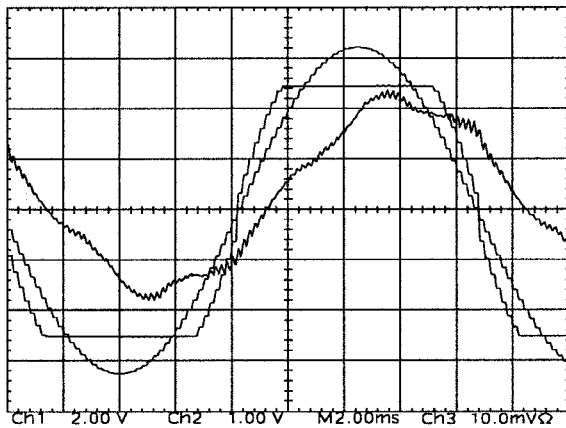


Fig. 21. GDPWM modulation wave, its fundamental component, and the motor current waveforms in the overmodulation range ($M_i = 0.96$, 59 Hz, 100% T_{eR}) with $\psi = 30^\circ$. Scaling: 5 A/div, 2 V/div, and 2 ms/div.

still retain the harmonic low distortion characteristic of the GDPWM method.

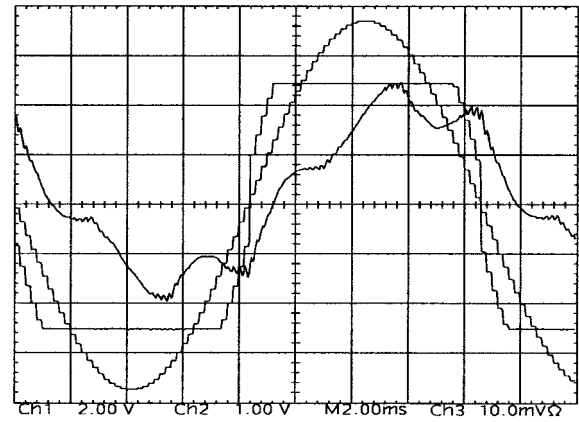


Fig. 22. GDPWM modulation wave and motor current waveforms in the overmodulation range ($M_i = 0.986$, 60 Hz, 100% T_{eR}) with $\psi = 30^\circ$. Scaling: 5 A/div, 2 V/div, and 2 ms/div.

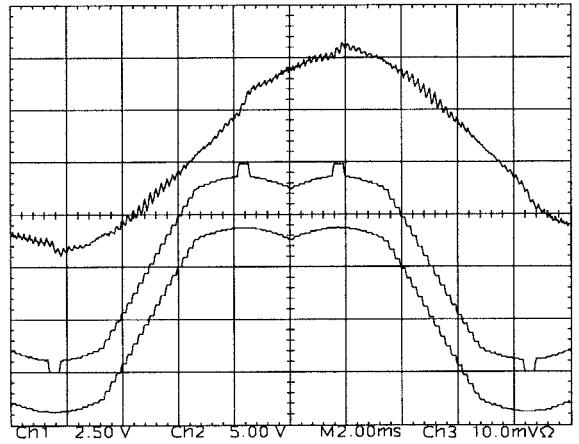


Fig. 23. SVPWM modulation wave, PEM-controlled modulation wave, and the motor current waveforms for $M_i = 0.815$, 49 Hz. Scaling: 5 A/div, 2 V/div, and 2 ms/div.

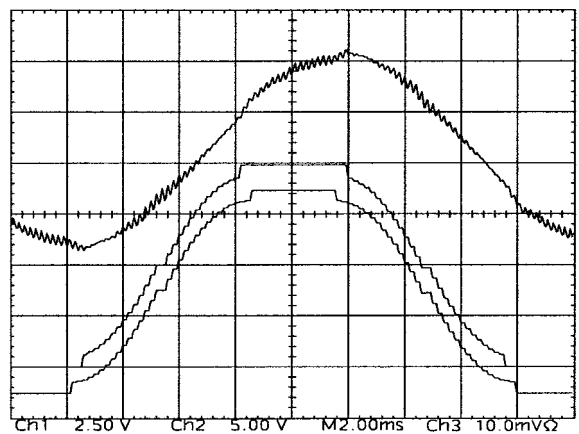


Fig. 24. GDPWM modulation wave, PEM-controlled modulation wave, and the motor current waveforms for $M_i = 0.867$, 53 Hz with $\psi = 30^\circ$. Scaling: 5 A/div, 2 V/div, and 2 ms/div.

Figs. 23 and 24 illustrate and compare the effect of the PEM algorithm on the SVPWM and GDPWM method performance. As the experimental waveforms indicate, eliminating voltage pulses narrower than 12 μ s, the SVPWM method loses linear-

ity at a lower modulation index than the GDPWM method, and the phase current waveform distorts significantly. As all the experimental waveforms indicate, the SVPWM method in the lower modulation range combined with the GDPWM method in the remainder of the range is a superior approach.

VIII. CONCLUSION

A GDPWM method with on-line performance optimization capability has been developed, and its characteristics have been analytically and experimentally investigated. An algorithm that combines the superior high modulation range performance characteristics of GDPWM and the superior low modulation range performance characteristics of SVPWM has been developed and implemented. The self-optimization procedure of the algorithm, which minimizes the harmonic distortion, reduces the switching losses, and provides superior overmodulation range performance has been described. The algorithm has a simple structure, and it is suitable for DSP- or microprocessor-based digital implementation. The phase angle ψ of the modulator is on-line controlled, in order to optimize the drive performance. The operating characteristics of GDPWM and the high-performance PWM algorithm have been verified with laboratory experiments. The switching losses, harmonic distortion, and voltage linearity characteristics have been both experimentally and theoretically investigated and reported. A detailed modulator design method is established, and the modulation index level at which the transition from SVPWM to GDPWM occurs is analytically determined.

ACKNOWLEDGMENT

The authors thank D. W. Schlegel of Rockwell Automation for his technical assistance during this research.

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