Chapter 3

Review of Carrier Based PWM Methods and Development of Analytical PWM Tools

3.1 VSI Operation and The Volt-Seconds Principle

Shown in Fig. 3.1, the basic circuit structure of the VSI is relatively simple. Each inverter leg consists of two self commutated switching devices (gate turn-on and turn-off devices such as MOSFET, IGBT, GTO, and MCT) with reverse parallel diodes which are often termed as the feedback diodes. In three phase sinusoidal power applications, except during the drive stand-by mode, power-off mode, and blanking periods (also termed as dead time), the upper and lower devices are always gated with complementary logic signals. During commutation both devices are disabled for a short blanking time to avoid short circuit condition across the DC voltage source. Considering the blanking time and the

commutation time are significantly shorter than the normal operating duty cycle of the switches, the switching devices can be assumed ideal in most PWM-VSI performance analysis studies. Since in each inverter leg the switches operate in a complementary manner, under normal operating conditions, at any time three switches are simultaneously in "on state," and three switches are in "off-state." In each inverter leg, depending on the polarity of the associated phase current, either the "on-state" switching device or its reverse parallel diode conducts the current. Combining the possible switch "on" or "off" states, eight unique inverter states are distinguished. These inverter states are generally described with the upper switch Boolean logic signals (Sa+, Sb+, Sc+), and "1" corresponds to on-state condition while "0" corresponds to off-state condition. Of the eight possibilities, (000) and (111) short circuit the output terminals of the three phase load and yield a zero output voltage. Hence they are termed the zero states. The remaining six states are termed active states and numbered with the decimal equivalent of their boolean states.

With its simple structure and switching constraints described above, the VSI generates a low frequency output voltage with controllable magnitude and frequency by programming high frequency voltage pulses. Of the various pulse programming methods, the carrier based PWM methods are the preferred approach in most applications due to the low harmonic distortion waveform characteristics with well defined harmonic spectrum, the fixed switching frequency, and implementation simplicity.

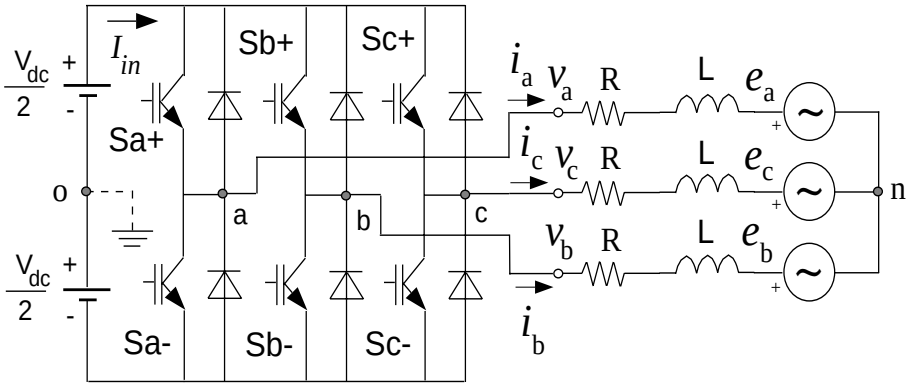

Figure 3.1: Circuit diagram of a PWM-VSI connected to an R-L-E type load.

Carrier based PWM methods employ the "per carrier cycle volt-second balance" principle to program a desirable inverter output voltage waveform. According to this principle, a sequence of inverter states is generated over a carrier cycle in a manner that for each phase the average value of the rectangular pulse output voltage approaches its reference voltage value. This principle has been utilized in DC/DC converters for a long time and is commonly termed as duty cycle control, or PWM control. However, its application to three phase VSI's is not as intuitive as the DC/DC converters. PWM-VSI modulator design and implementation is also substantially more complex than the DC/DC converter duty cycle controllers. This is so, because in a three phase PWM-VSI, the duty cycle of each switch is time variant both under steady state and dynamic operating conditions. In addition, the inverter output line-to-line voltages can not be independently controlled by any switch, i.e. the VSI is a coupled system. Therefore, a detailed modulator study requires a knowledge of both microscopic

(per carrier cycle) and macroscopic (over a fundamental cycle) behavior. Following the description of two carrier based PWM implementation techniques, the microscopic and macroscopic views will be provided.

Two main carrier based PWM implementation techniques exist: the triangle intersection technique and the direct digital technique. In the triangle intersection technique, for example in the Sinusoidal PWM (SPWM) method [177], as shown in Fig. 3.2, the reference modulation wave is compared with a triangular carrier wave and the intersections define the switching instants. Within every carrier cycle, the average value of the output voltage becomes equal to the reference value. In particular, in the digital implementation which employs the regular sampling technique, this result becomes obvious as the reference volt-seconds precisely equals the output volt-seconds. This principle is illustrated in Fig. 3.3 in detail. In the regular sampling technique, the modulation signals are sampled/output at the positive (and/or negative) peak of the triangular carrier cycle and held constant for the remainder of the carrier cycle. Although the early triangle intersection implementations mostly involved analog hardware circuits, the advent of low cost digital electronics rendered the analog solutions obsolete. Most present triangle intersection implementations involve high resolution digital PWM counters and comparators. Therefore, in this work the term triangle intersection is generally not associated with the analog implementations, and typically digital implementation is implied.

The direct digital implementation involves the space vector theory [108].

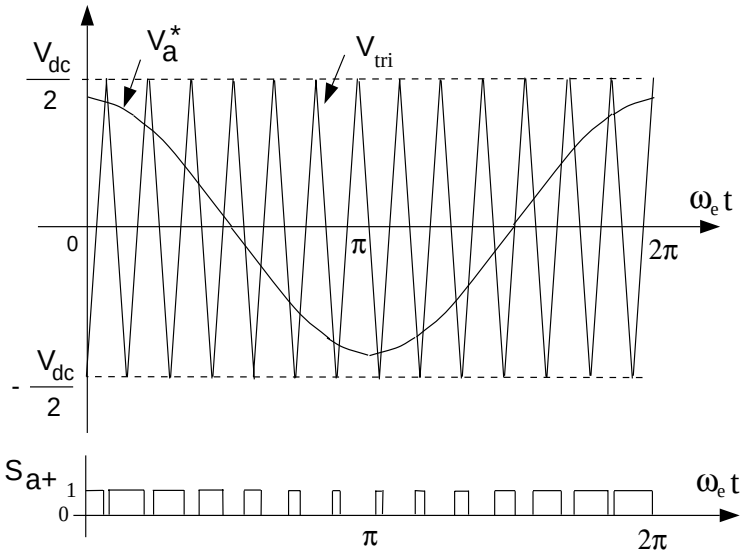

Figure 3.2: Triangle intersection PWM phase "a" modulation and switching signals.

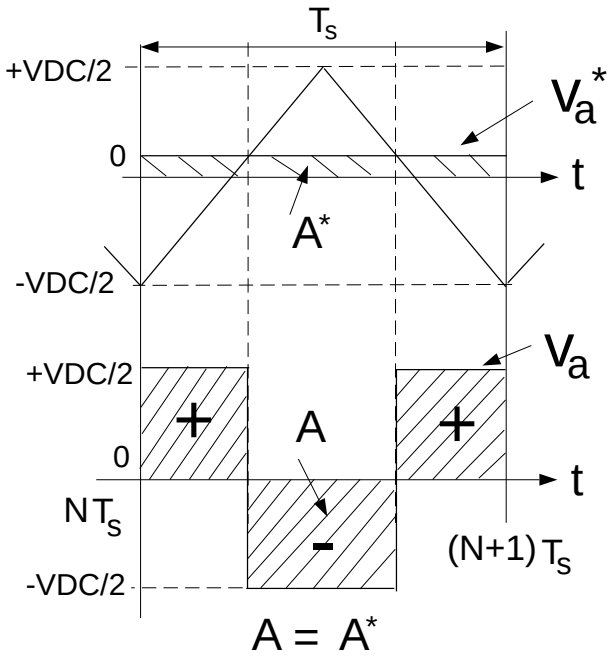

Figure 3.3: An illustration of the per carrier cycle volt-second balance principle.

The space vector theory employs the following complex number transformation which transforms the three phase time domain variables x_a, x_b, x_c, to a time parametric complex number variable, i.e. a space vector X.

$$X = \frac{2}{3}(x_a + ax_b + a^2x_c) \tag{3.1}$$

In the transformation equation "a" represents the conventional 120° rotation operator, $e^{j\frac{2\pi}{3}}$, and "j" represents the imaginary axis unit. Applying this transformation to the seven discrete inverter states, the inverter voltage vectors, and the hexagon which the tip points of these vectors form are obtained. The inverter voltage vectors and the hexagon are illustrated in Fig. 3.4 in detail. This diagram is commonly termed as the space vector diagram. Applying the transformation to the three phase voltage references generated by the controller of a PWM-VSI drive, a reference voltage vector is also obtained. In the direct digital approach, the time integral of the reference voltage vector and the time integral of a selected sequence of inverter voltage vectors over a carrier cycle are equated. Of the available inverter voltage vectors, the two zero states and the two vectors adjacent to the reference voltage vector are selected to match the reference volt-seconds. The volt-second balance calculation gives the total time length of each adjacent inverter state and the total zero state time length [29, 158]. Figure 3.4 graphically illustrates the complex number volt-second balance in detail. Once the inverter state time lengths are determined, the number and sequence of commutations are selected by the user. Finally, the

switch duty cycles are calculated from the data and loaded to the digital PWM counters to generate the selected output voltages. Since the approach does not involve a modulation signal, it is often termed as the direct digital approach, and this term will be adopted in the remainder of this thesis. Note in this method the duty cycles are precalculated for each carrier cycle, and therefore the regular sampling technique is implied. In both direct digital and triangle intersection methods, with the volt-second balance principle being quite simple, a variety of PWM methods have appeared in the technical literature; each method results from a unique placement of the voltage pulses in isolated neutral type loads. Following a modulation index definition, which will be immediately utilized, the freedom in placing voltage pulses in isolated neutral type loads will be discussed in detail.

Modulation Index: Since the performance characteristics of a modulator are primarily dependent on the voltage utilization level, i.e. modulation index, it is helpful to define a modulation index term at this stage. For a given DC link voltage V_{dc}, the ratio of the fundamental component magnitude of the line to neutral inverter output voltage, V_{1m}, to the fundamental component magnitude of the six-step mode voltage, $V_{1m6step}$, is termed the modulation index M_i [68]:

$$M_i = \frac{V_{1m}}{V_{1m6step}} \tag{3.2}$$

$$V_{1m6step} = \frac{2V_{dc}}{\pi} \tag{3.3}$$

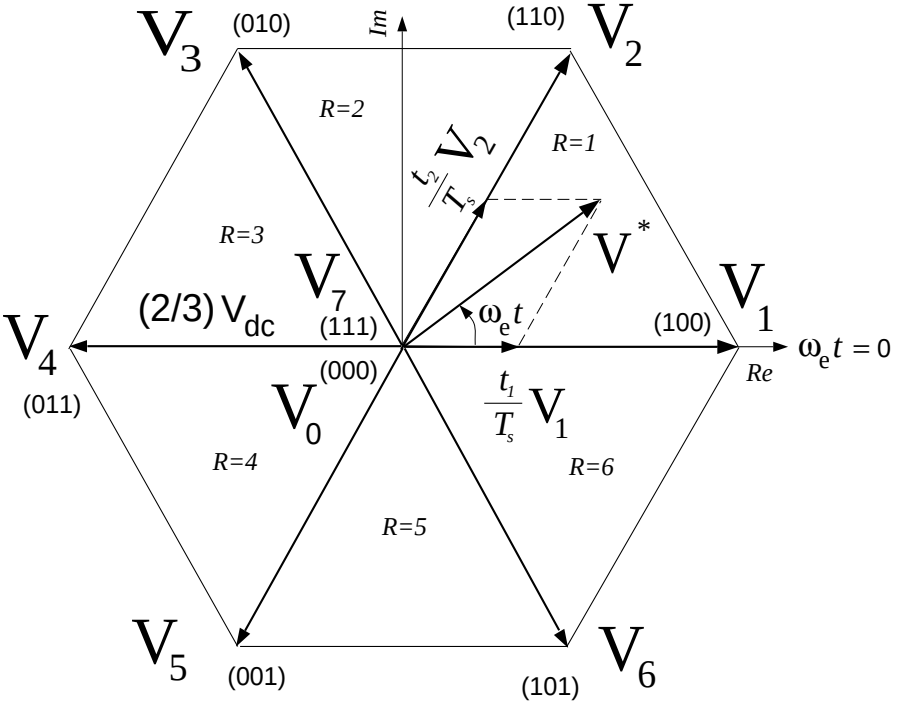

Figure 3.4: The space vector diagram illustrates the direct digital PWM technique implementation principle.

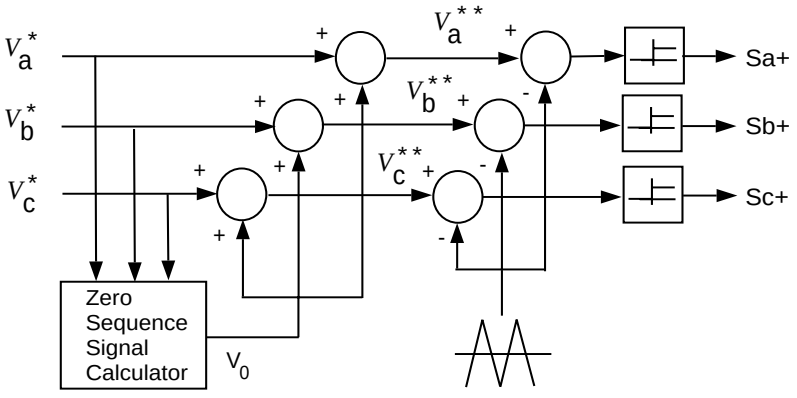

Figure 3.5: The generalized signal block diagram of the triangle intersection technique based PWM employing the zero sequence injection principle.

3.2 The Zero Sequence Signal Injection Principle

In most three phase AC motor drive and utility interface applications the neutral point is isolated and no neutral current path exists. In such applications the neutral voltage can be different from zero. Therefore, in the triangle intersection implementations any zero sequence signal can be injected to the reference modulation waves. Possibly K. G. King was the first researcher to utilize this concept in a voltage source inverter [101]. In the zero sequence signal injection technique, the n-o potential in Fig. 3.1 which will be symbolized with v_0 can be freely varied. This degree of freedom is illustrated in Fig.3.5 with the generalized modulator signal diagram. A properly selected zero sequence signal can extend the volt-second linearity range of SPWM. Furthermore, it can improve the waveform quality and reduce the switching losses significantly. Recognizing these properties, many researchers have been investigating the zero sequence signal dependency of the modulator performance and a large number of PWM methods with unique characteristics have been reported [68]. Detailed research showed the freedom in selecting the partitioning of the two zero states "0" (000) and "7" (111) in the direct digital PWM technique is equivalent to the freedom in selecting the zero sequence signal in the triangle intersection PWM technique [29, 146].

Although it does not affect the inverter line-to-line voltage per carrier cycle

average value, the zero sequence signal of a modulator significantly influences the switching frequency characteristics. Therefore, the per carrier cycle (microscopic) characteristics of different modulators are important and must be accurately modeled and carefully analyzed.

As shown in Fig. 3.6 in the triangle intersection method, the modulation signals are compared with the triangular carrier wave and the intersection points define the switching instants. The duty cycle of each switch can be easily calculated in the following.

$$d_{Sx+} = \frac{1}{2}(1 + \frac{v_x^{**}}{\frac{V_{dc}}{2}}) \qquad for \qquad x \in \{a, b, c\} \tag{3.4}$$

$$d_{Sx-} = 1 - d_{Sx+} \qquad for \qquad x \in \{a, b, c\} \tag{3.5}$$

With the modulation waveforms defined with the following cosine functions, the $w_e t$ time axis of the modulation waves and complex plane reference voltage vector angle $w_e t$ coincide.

$$v_a^{**} = v_a^* + v_0 = V_{1m}^* \cos(w_e t) + v_0 \tag{3.6}$$

$$v_b^{**} = v_b^* + v_0 = V_{1m}^* \cos(w_e t - \frac{2\pi}{3}) + v_0 \tag{3.7}$$

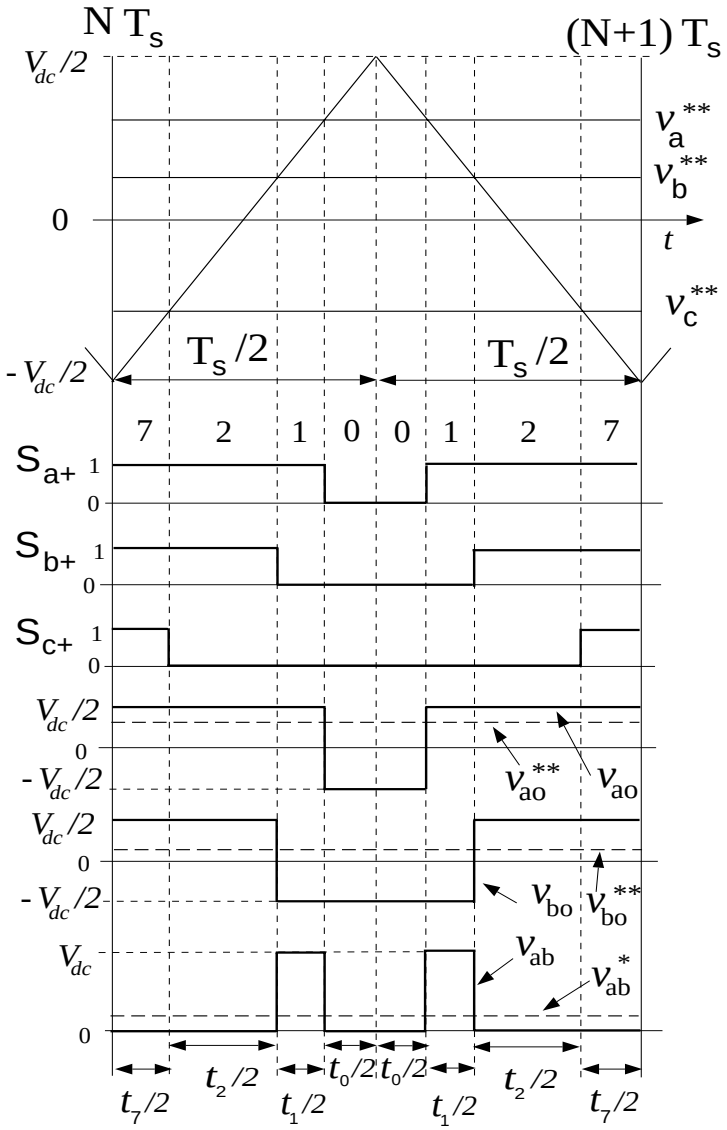

Figure 3.6: The per carrier cycle view of switch logic signals, inverter states, and VSI output voltages for $0 \leq w_e t \leq \frac{\pi}{3}$ $(R = 1)$.

$$v_c^{**} = v_c^* + v_0 = V_{1m}^* \cos\left(w_e t + \frac{2\pi}{3}\right) + v_0 \tag{3.8}$$

For the above defined modulation functions and $0 \leq w_e t \leq \frac{\pi}{3}$, the inverter states of the triangle intersection PWM methods are 7-2-1-0-0-1-2-7 as shown in Fig. 3.6. This symmetric switching sequence is superior to other sequences due to its low harmonic distortion characteristic. Therefore, this sequence is adopted in the direct digital methods also [29]. As will be later discussed in detail, either the two "7" states at both ends of the carrier cycle, or the "0" states in the middle are often omitted to further reduce the commutation count and therefore to reduce the average switching frequency. The zero state to be eliminated is the state which reduces the switching losses more than the other zero state [146]. Notice that in Fig. 3.6, a zero sequence signal simultaneously shifts the three reference signals in the vertical direction and while it changes the position of the output line-to-line voltage pulses, it does not affect their width. The time length of the active and zero states of the triangle intersection methods are not explicitly calculated in the algorithm. However, for analysis purposes they can be directly calculated from the duty cycle information; Figure 3.6 illustrates these relations. However, in the direct digital technique, the inverter state time lengths are directly calculated employing space vector theory and Zero State Partitioning (ZSP) is selected by the programmer.

In the space vector approach, employing the complex variable transformation, the time domain modulation signals are translated to the complex reference

voltage vector which rotates in the complex coordinates at the $w_e t$ angular speed in the following.

$$V^* = \frac{2}{3}(v_a^* + a v_b^* + a^2 v_c^*) = V_{1m}^* e^{j w_e t} \quad where \quad a = e^{j\frac{2\pi}{3}} \tag{3.9}$$

The complex number volt-second balance equation in the R'th sector of the hexagon in Fig. 3.4 determines the time length of the two adjacent state active inverter states R and $R+1$ $(R = 6 \rightarrow R+1 = 1)$ and the total zero state time length in the following.

$$V_R t_R + V_{R+1} t_{R+1} = V^* T_s \tag{3.10}$$

$$t_R = \frac{2\sqrt{3}}{\pi} M_i \sin(R\frac{\pi}{3} - w_e t) T_s \tag{3.11}$$

$$t_{R+1} = \frac{2\sqrt{3}}{\pi} M_i \sin(w_e t - (R-1)\frac{\pi}{3}) T_s \tag{3.12}$$

$$t_0 + t_7 = T_s - t_R - t_{R+1} \tag{3.13}$$

Defined by the following, ZSP of the two inverter zero states, ζ_0 and ζ_7, provides the degree of freedom in the direct digital technique [146].

$$\zeta_0 = \frac{t_0}{t_0 + t_7} \tag{3.14}$$

$$\zeta_7 = 1 - \zeta_0 \tag{3.15}$$

In order to simplify the analytical investigations, the inverter state time lengths can be expressed in terms of per carrier cycle or per half carrier cycle duty cycle in the following.

$$d_R = \frac{t_R}{T_s} = \frac{t_R/2}{T_s/2} \qquad for \qquad R \in \{0, 1, ..., 7\} \tag{3.16}$$

With the degree of freedom in the triangle intersection PWM being the v_0 signal, and in the direct digital technique the ζ_0 partitioning, the modern PWM methods are discussed next.

3.3 Modern PWM Methods and The Magnitude Rules

Although theoretically an infinite number of zero sequence signals and therefore modulation methods could be developed, the performance and implementation constraints of practical PWM-VSI drives reduce the possibility to a small number. Over the last three decades of PWM technology evolution, about ten high

performance carrier based PWM methods were developed and of these only several have gained wide acceptance. Figure 3.7 illustrates the modulation and zero sequence signal waveforms of these modern triangle intersection PWM methods. In the figure, unity triangular carrier wave gain is assumed and the signals are normalized to $\frac{V_{dc}}{2}$. Therefore, $\pm\frac{V_{dc}}{2}$ voltage saturation limits correspond to ± 1. In the figure only phase "a" modulation wave is shown, and the modulation signals of phase "b" and "c" are identical waveforms with 120° phase lag and lead with respect to phase "a."

The modulators illustrated in Fig. 3.7, can be separated into two groups. In the Continuous PWM (CPWM) methods, the modulation waves are always within the triangle peak boundaries. Within every carrier cycle, the triangular carrier wave and the modulation wave intersect and therefore on and off switchings occur. In the Discontinuous PWM (DPWM) methods, the modulation wave of a phase has at least one segment which is clamped to the positive and/or negative DC rail for at most a total of 120° (over a fundamental cycle). Therefore, within such intervals the corresponding inverter leg discontinues modulation. Since no modulation implies no switching losses, the switching loss characteristics of CPWM and DPWM methods are different. Detailed studies indicated the waveform quality and linearity characteristics are also significantly different. Therefore, this classification aids in distinguishing the important differences between CPWM and DPWM methods.

Of the four modern CPWM methods shown in Fig. 3.7, the SPWM method

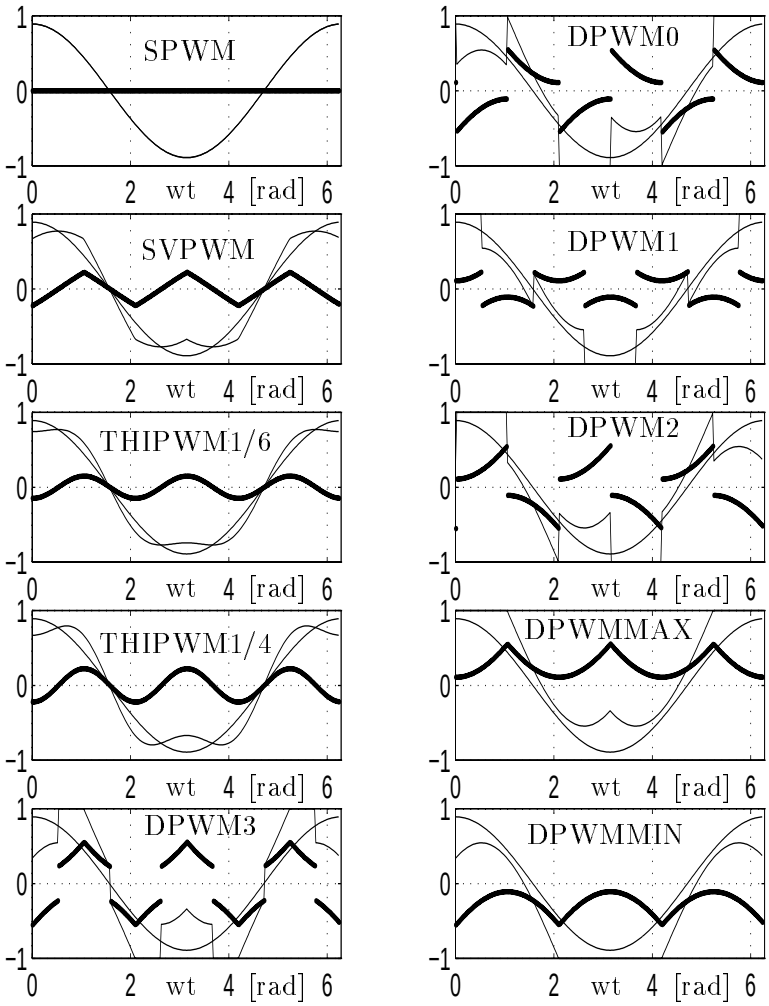

Figure 3.7: Modulation waveforms of the modern PWM methods ($M_i = 0.7$).

[177] is the simplest modulator with limited voltage linearity range and poor waveform quality in the high modulation range. The triangle intersection implementation of the Space Vector PWM (SVPWM) method and the two Third Harmonic Injection PWM (THIPWM) methods are the remaining three popular CPWM methods. These modulators are discussed in the following.

THIPWM: Due to the simplicity of algebraically defining their zero sequence signals, these modulators have been frequently discussed in the literature. With v_a^* defined as in (3.6), the zero sequence signal of THIPWM1/6 is $v_0 = -\frac{V_{1m}}{6}\cos 3w_e t$ [32] and for THIPWM1/4, $v_0 = -\frac{V_{1m}}{4}\cos 3w_e t$ [24] is selected. Both methods suffer from implementation complexity, because generating the $\cos 3w_e t$ signal is difficult both with hardware and software. Trigonometric identities can be utilized to compute $\cos 3w_e t$ from the $\cos w_e t$ signal, however the computational intensity (several multiplications are required) results in loss of significance by several bits and poor resolution is obtained in signal processors with limited wordlength. Often, a large look-up table is employed to store the base function of such modulators and the modulation signals are on-line accessed from this table to compute the modulation signals. Although the THIPWM1/4 has theoretically minimum harmonic distortion, it is only slightly better than SVPWM and has a narrower voltage linearity range [68, 105]. With their performance being very similar to SVPWM and implementation complexity significantly higher, both THIPWM methods have academic and historical value, but little practical importance. Also note when higher order triplen harmonics are added to the THIPWM1/6 signal (such as $\frac{V_{1m}}{9}\cos 9w_e t$), the zero sequence signal

approaches a triangle and the resulting modulation signal approaches SVPWM.

SVPWM [101, 29]: The zero sequence signal of SVPWM is generated by employing the minimum magnitude test which compares the magnitudes of the three reference signals and selects the signal with minimum magnitude [50]. Scaling this signal with 0.5, the zero sequence signal of SVPWM is found. Assume $|v_a^*| \leq |v_b^*|, |v_c^*|$, then $v_0 = 0.5 \times v_a^*$. The analog implementation of SVPWM which employs a diode rectifier circuit to collect the minimum magnitude signal from the three reference signals (was shown in Fig. 2.4) is possibly the earliest zero sequence signal injection PWM method reported [101]. About a decade later, this modulator re-appeared in the literature with direct digital implementation [29]. Since the direct digital implementation utilized the space vector theory, the method was named SVPWM. In addition to its implementation simplicity, the SVPWM method has superior performance characteristics (compared to all other CPWM methods) and is possibly the most popular high performance PWM method. However, its high modulation range performance is inferior to DPWM methods, which also employ similar magnitude rules to generate their modulation waves. In the following the modern DPWM methods and their magnitude rules are summarized.

DPWM1 [42, 178]: The reference signal with the maximum magnitude defines the zero sequence signal. Assume $|v_b^*|, |v_c^*| \leq |v_a^*|$, then $v_0 = sign(v_a^*)\frac{V_{dc}}{2} - v_a^*$. This method has minimum switching losses at unity power factor operating condition, and its waveform quality at high modulation is superior to

SVPWM [42].

DPWM2 [107, 146]: All three reference modulation signals v_a^*, v_b^*, and v_c^* are phase shifted by 30° (lagging), and of the three new signals v_{ax}^*, v_{bx}^*, and v_{cx}^*, the one with the maximum magnitude determines the zero sequence signal. Assume $|v_{ax}^*| \geq |v_{bx}^*|, |v_{cx}^*|$, then, $v_0 = (sign(v_a^*))\frac{V_{dc}}{2} - v_a^*$. Adding this zero sequence signal to the three original modulation waves v_a^*, v_b^*, and v_c^*, the DPWM2 waves v_a^{**}, v_b^{**}, and v_c^{**} are generated. This method has minimum switching losses at 30° lagging power factor operating condition, and its waveform quality at high modulation is superior to SVPWM [146].

DPWM0 [90, 107]: All three reference modulation signals v_a^*, v_b^*, and v_c^* are phase shifted by 30° (leading), and of the three new signals v_{ax}^*, v_{bx}^*, and v_{cx}^*, the one with the maximum magnitude determines the zero sequence signal. Assume $|v_{ax}^*| \geq |v_{bx}^*|, |v_{cx}^*|$, then, $v_0 = (sign(v_a^*))\frac{V_{dc}}{2} - v_a^*$. Adding this zero sequence signal to the three original modulation waves v_a^*, v_b^*, and v_c^*, the DPWM0 waves v_a^{**}, v_b^{**}, and v_c^{**} are generated. This method has minimum switching losses at 30° leading power factor operating condition, and its waveform quality at high modulation is superior to SVPWM [90, 107].

DPWM3 [105]: The reference signal with the intermediate magnitude defines the zero sequence signal. Assume $|v_b^*| \leq |v_a^*| \leq |v_c^*|$, then $v_0 = sign(v_a^*)\frac{V_{dc}}{2} - v_a^*$. This method has low harmonic distortion characteristics [105].

DPWMMAX [191]: The reference signal with the maximum value defines the zero sequence. Assume $v_b^* \leq v_a^* \leq v_c^*$, then $v_0 = \frac{V_{dc}}{2} - v_c^*$ yields and phase

"c" is unmodulated [191].

DPWMMIN [105]: The reference signal with the minimum value defines the zero sequence. Notice the DPWMMAX and DPWMMIN methods have nonuniform thermal stress on the switching devices and in DPWMMAX the upper devices have higher conduction losses than the lower, while in DPWMMIN the opposite is true.

All the magnitude tests require a small number of computations and therefore can be easily implemented in a microcontroller or DSP. Due to the simplicity of the algorithms, it is easy to program two or more methods and on-line select a modulator in each operating region in order to obtain the highest performance [62, 69]. Similar to SVPWM analog implementation of King [101] and DPWM1 analog implementation of Depenbrock [42], analog or digital hardware implementations of the remainder of the discussed modulators can be easily developed by following the magnitude test computational procedures.

With the exception of THIPWM and SPWM methods, all the above discussed triangle intersection PWM methods can be easily implemented in the direct digital method. Mapping the zero state partitioning of the time domain modulation waves of Fig. 3.7 onto the vector space domain, the direct digital implementation equivalents can be easily obtained. This mapping is illustrated in Fig. 3.8 in detail. Assuming the fundamental component modulation signals of the three phases are cosine functions in time, the origin in the time domain is mapped to the real axis of the complex plane. Therefore, with the aid of

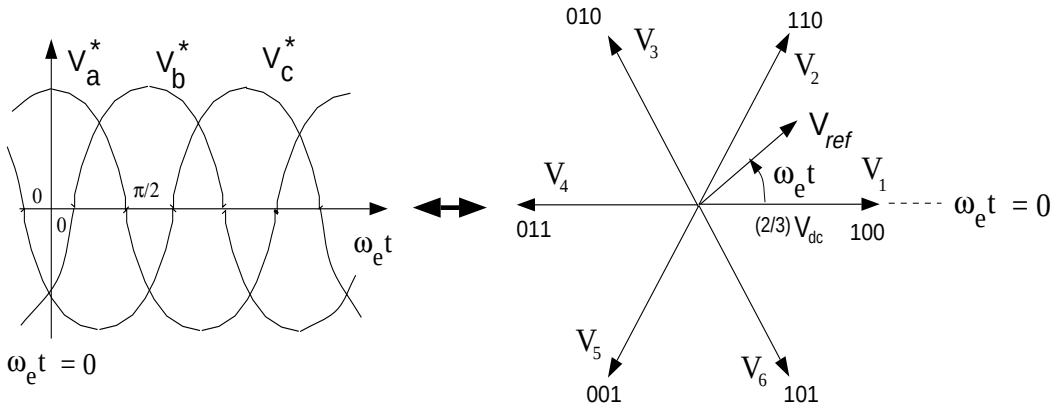

Figure 3.8: Time to complex coordinate mapping aids illustrating the equivalency between the direct digital and triangle intersection PWM methods.

this mapping, the ZSP of each triangle intersection PWM method can be identified. Figure 3.9 illustrates this equivalency and the ZSP of each method. A clear illustration of this equivalency is an important step towards simplifying the learning process.

Due to its simplicity, the magnitude test is a very effective tool for simulation, analysis, and graphic illustration of various modulation methods. For example, the simulation or DSP implementation of the SVPWM method with a direct digital technique is involved: the sector to which the voltage vector belongs has to be identified first, then the time length of each active vector must be calculated, and finally gate pulses must be generated in a correct sequence [29]. Although it is possible to reduce the direct digital PWM algorithms, the effort does not yield as simple and intuitive a solution as the magnitude test [98, 175]. Therefore, employing the magnitude test the triangle intersection PWM

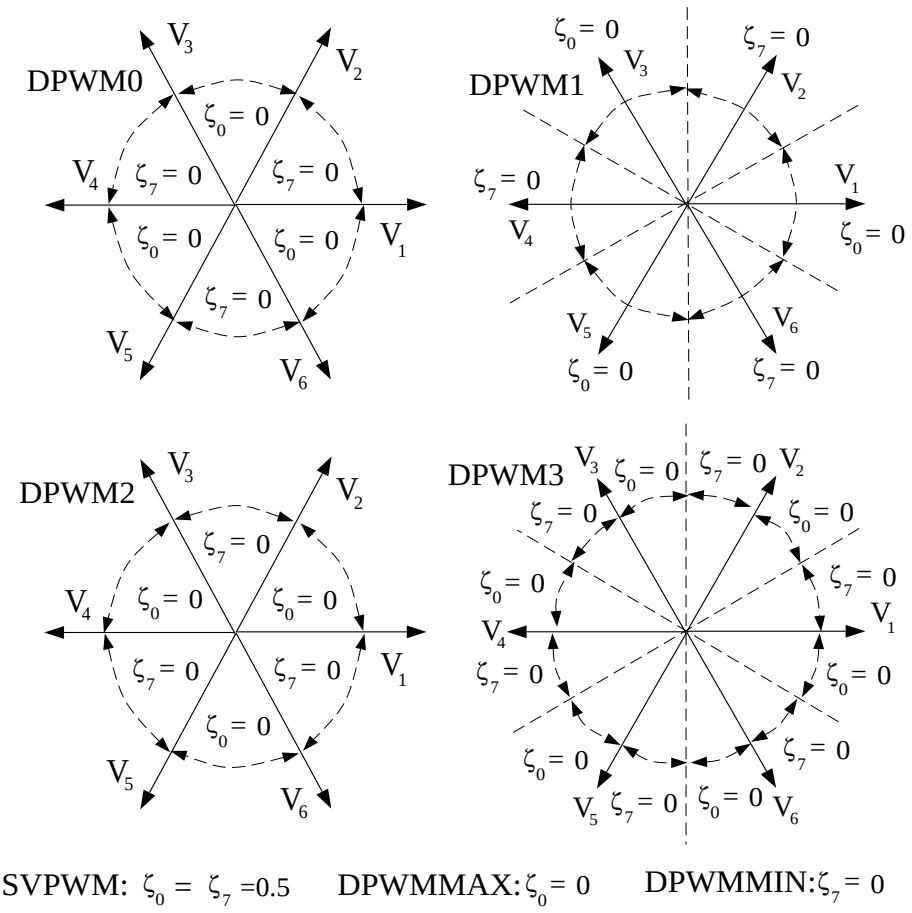

Figure 3.9: Zero state partitioning of the modern PWM methods. DPWMMIN, DPWMMAX, and SVPWM have space invariant partitioning.

method is superior to the direct digital method from a simulation as well as implementation perspective.

In voltage feedforward controlled drives ($\frac{V}{f}$ etc.), often the base modulation signals ($\sin\theta$ etc.) are stored in a table and the data is read on-line and scaled with the modulation index to generate the modulation signals. Since in such an implementation the on-line trigonometric function computations are eliminated, the processor performance requirements can be less stringent. The table of SPWM is a simple sinusoidal function. The SVPWM table can be easily generated by employing the minimum magnitude rule. Although their tables can be generated as easily as the SVPWM method, their poorer performance renders the remaining CPWM methods obsolete. Although CPWM methods can be implemented with this approach easily, the DPWM methods do not have a base function and they can not be easily implemented with table look-up approach. Therefore, applications utilizing DPWM methods require microcontroller or DSPs with computationally superior characteristics and the magnitude rules can be employed for generating the modulation signals.

Since in current controlled drives typically vector control is employed, the sine and cosine functions of the reference voltage vector are normally available for modulation signal generation. Therefore, the modulation signals can be real-time calculated and the magnitude rules can be employed. Therefore, generating the modulation signals with the magnitude rules is the preferred approach in high performance closed loop vector controlled drives.

3.4 A High Performance GDPWM Method

A careful examination of the DPWM0 and DPWM1 modulation waveforms of Fig. 3.7 indicates there exists a 30° phase angle distance between their bus clamped 60° segments. While in DPWM1 the center of each bus clamped segment is aligned with the cosine modulation wave peak, in DPWM0 a 30° phase difference exists. The same relation is true between DPWM1 and DPWM2. The modulation signals of the three methods are similar to each other and furthermore the magnitude rules involved in generating them have the same procedure. The minimum switching loss characteristic of DPWM0 under $-30°$ power factor angle operating condition, of DPWM1 under 0°, and of DPWM2 under 30° is intuitive. In each case, the bus clamped switch conducts the largest current and minimum switching losses are obtained. In fact, this characteristic has been the reason for developing these modulators. However, under different power factor operating conditions from the specified, the performance of these modulators degrades. Following the recognition of the similarities between these modulators, an attempt towards unifying them in this thesis has lead to the development of a high performance Generalized DPWM (GDPWM) method [62].

GDPWM is a DPWM method which covers a range of modulators including the DPWM0, DPWM1, and DPWM2 methods. Figure 3.10 illustrates the zero sequence signal generation method of GDPWM. To aid the description of GDPWM, it is useful to define the modulator phase angle ψ increasing from the intersection point of the two reference modulation waves at $w_e t = \frac{\pi}{6}$ as shown in

Fig. 3.10. From ψ to $\psi + \frac{\pi}{3}$, the zero sequence signal is the shaded signal which is equal to the difference between the saturation line ($\frac{V_{dc}}{2}$) and the reference modulation signal which passes the maximum magnitude test. In the maximum magnitude test, all three reference modulation signals v_a^*, v_b^*, and v_c^* are phase shifted by $\psi - \frac{\pi}{6}$, and of the three new signals v_{ax}^*, v_{bx}^*, and v_{cx}^*, the one with the maximum magnitude determines the zero sequence signal. Assume $|v_{ax}^*| \geq |v_{bx}^*|, |v_{cx}^*|$, then, $v_0 = (sign(v_a^*))\frac{V_{dc}}{2} - v_a^*$. Adding this zero sequence signal to the three original modulation waves v_a^*, v_b^*, and v_c^*, the GDPWM waves v_a^{**}, v_b^{**}, and v_c^{**} are generated. For $\psi = 0$ DPWM0, for $\psi = \frac{\pi}{6}$ DPWM1, for $\psi = \frac{\pi}{3}$ DPWM2 correspond to only three operating points on the full ψ range of the modulator ($0 \leq \psi \leq \frac{\pi}{3}$). Due to their superior performance characteristics, these three operating points of GDPWM have found a wide range of applications.

Since the GDPWM zero sequence signal must not be too large to force a modulation wave outside the triangular carrier wave boundaries, the control range of ψ is confined to the interval $[0, \frac{\pi}{3}]$. Within this ψ range, the modulator is linear between $0.0 \leq M_i \leq \frac{\pi}{2\sqrt{3}} \approx 0.907$. Figure 3.11 illustrates the modulation and zero sequence waveforms for four different ψ values and $M_i = 0.7$. Notice that DPWM1 corresponds to $\psi = \frac{\pi}{6}$ and DPWM2 to $\psi = \frac{\pi}{3}$. Note that the DPWM1 region is quite attractive in PWM-VSC utility interface applications and AC Permanent Magnet (PM) motor applications where the load power factor is near unity, while the DPWM2 end provides desirable performance characteristics for lagging loads near 30° such as induction motor drives.

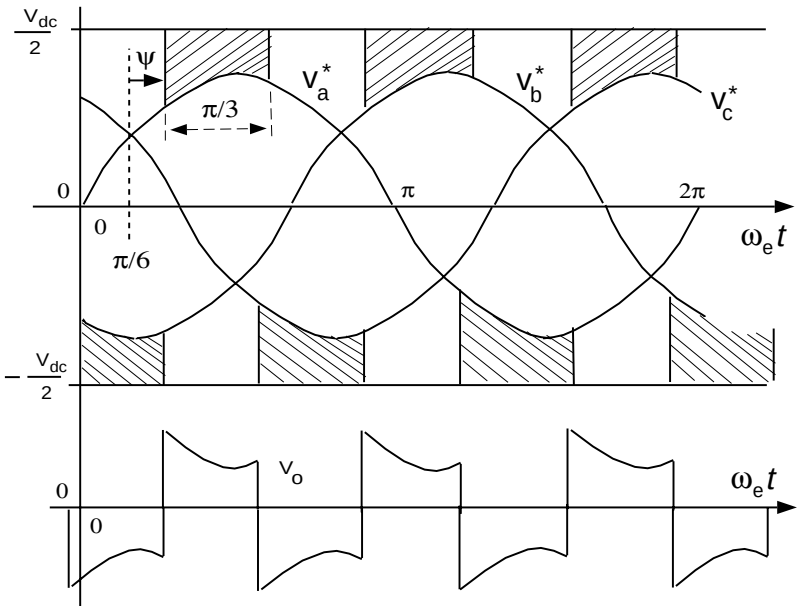

Figure 3.10: Generalized DPWM zero sequence signal generation method: ψ is the only control parameter.

The $\psi = 0$ region is suitable for operating an induction machine as a generator. In all these cases, the phase that conducts the largest current is not switched. Therefore, the inverter switching losses are significantly reduced. As will be shown later in this and the following chapters in detail, the only control parameter of GDPWM, ψ, substantially influences the waveform quality and overmodulation region characteristics also.

A careful observation of Fig. 3.10 indicates a more general approach to forming a DPWM signal is possible. Theoretically, a positive zero sequence signal of $v_{0p} = \frac{V_{dc}}{2} - v^*_{abcmax}$ always clamps the largest positive signal to the positive rail while the other signals are contained within the carrier signal boundaries ($v^*_{abcmax} = max(v^*_a, v^*_b, v^*_c)$). Also, a negative zero sequence signal

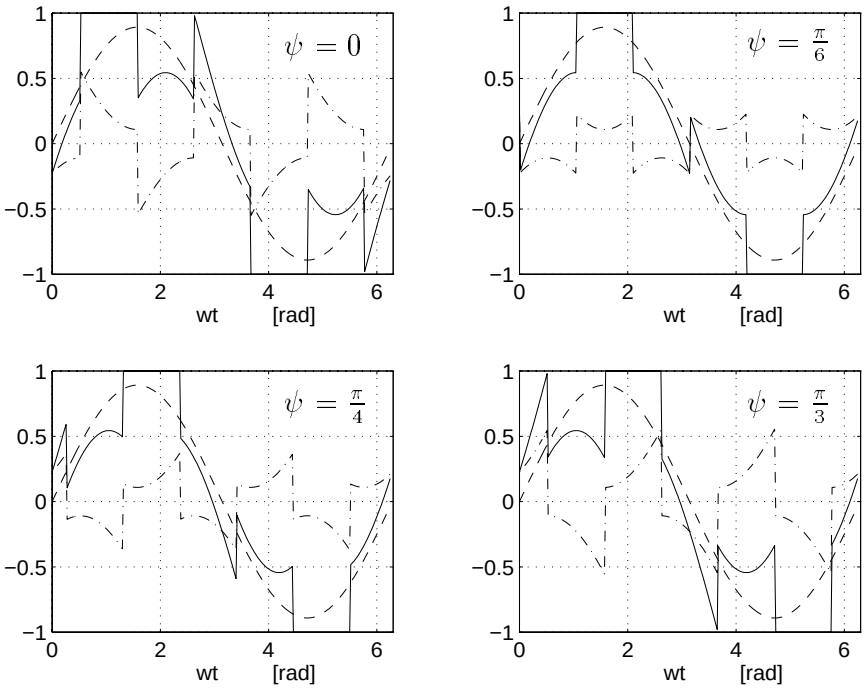

Figure 3.11: GDPWM method modulation waves("–"), their zero sequence signal ("-.") and the fundamental component ("- -") for $M_i = 0.7$ and four different modulator phase angle values.

of $v_{0n} = -\frac{V_{dc}}{2} - v^*_{abcmin}$ clamps the largest negative signal to the negative rail and the other two modulation signals are contained within the triangle wave boundaries. All the DPWM methods are formed by selecting pieces from these two zero sequence signals. Therefore, it is possible, to define more detailed zero sequence signal generation rules than the rules of GDPWM and form a modulator which covers GDPWM, DPWM3 and the other DPWM modulators also. However, such an approach would increase the modulator complexity and become practically infeasible. Furthermore, as will be later illustrated in detail, GDPWM covers the most practical modulators and yields satisfactory results for most applications.

Since it only requires a phase shift operation (rotation) and several comparisons, the GDPWM method is simple and can be easily implemented on a DSP or microprocessor. Although the ψ variable is helpful in the analysis and graphic illustration of this method, in the practical implementation a modified control variable $\psi_m = \psi - \frac{\pi}{6}$ results in reduced computations and is preferable. With this variable, DPWM0 corresponds to $\psi_m = -\frac{\pi}{6}$, DPWM1 to $\psi_m = 0$ and DPWM2 to $\psi_m = \frac{\pi}{6}$ values. Employing d-q transformations and expanding the terms in a manner to minimize the computational requirements, the rotation calculation can be accomplished in the following equations.

$$v^*_{ax} = v^*_a \cos(\psi_m) - \frac{(v^*_c - v^*_b)}{\sqrt{3}} \sin(\psi_m) \tag{3.17}$$

$$v_{bx}^* = v_b^* \cos(\psi_m) + (\frac{1}{2}\frac{(v_c^* - v_b^*)}{\sqrt{3}} - \frac{\sqrt{3}v_a^*}{2}) \sin(\psi_m) \tag{3.18}$$

$$v_{cx}^* = -v_{ax}^* - v_{bx}^* \tag{3.19}$$

Applying the maximum magnitude test to the above signals, the switch to be clamped to the positive or negative rail is defined and the zero sequence calculation is followed by the zero sequence signal injection. With the modulation signal computation stage completed, the duty cycles of the inverter switches are computed from (3.4) and (3.5) and the last stage involves loading the PWM counters with these duty cycle values.

Figure 3.12 shows the space vector coordinate illustration of the GDPWM method. As the figure indicates, in the direct digital implementation the inverter zero states, t_0 (000) and t_7 (111) are interchangeably set to zero for 60° segments. The diagram indicates the direct digital implementation is straightforward. However, it is computationally more involved than the triangle intersection implementation [38, 114, 146]. Therefore, the direct digital implementation is less practical. However, the space vector co-ordinate illustration of the method aids visualization of this modulator characteristics such as the voltage linearity and waveform quality which will be investigated in the following sections in detail.

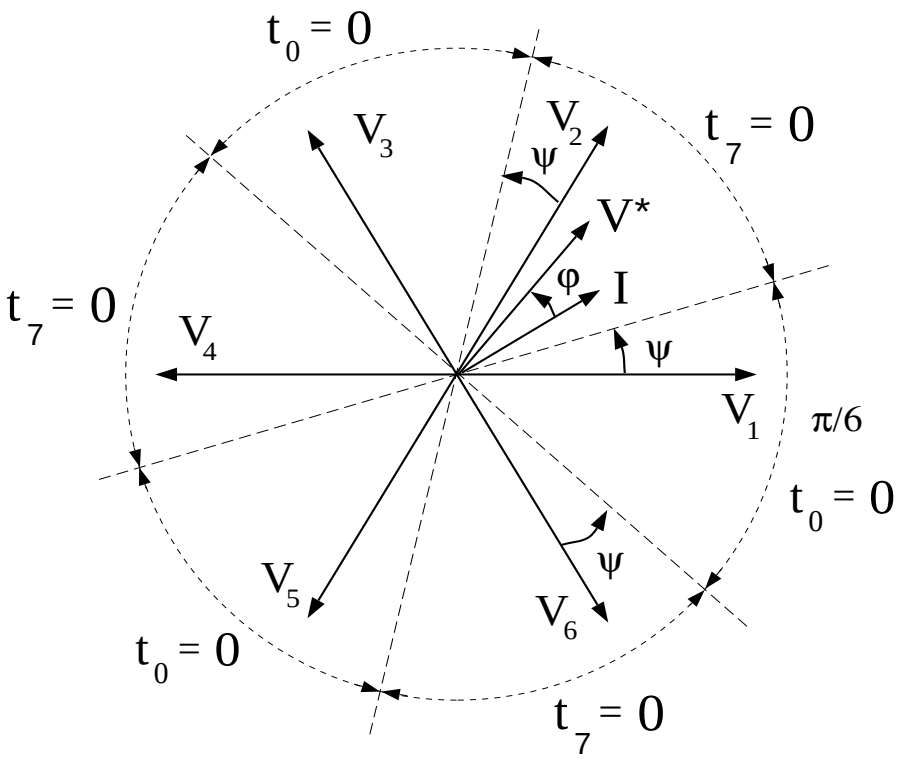

Figure 3.12: The GDPWM method space vector illustration aids the direct digital implementation.

3.5 Waveform Quality

The linear modulation range output voltage of a carrier based PWM-VSI drive contains harmonics at the carrier frequency, at its integer multiples, and at the side bands of all these frequencies which will all be termed as "the switching frequency harmonics." With sufficiently high carrier frequency, f_s, to fundamental frequency, f_e, ratios ($\frac{f_s}{f_e} > 20$) the low frequency reference volt-seconds are programmed accurately and the subcarrier frequency harmonic content is negligible [30]. Since modern power electronics switching devices such as IGBTs and MOSFETs typically meet this requirement, the voltage and current waveform quality of the PWM-VSI drives is determined by the switching frequency harmonics. In high power drive applications where the switching frequency is low, synchronization of the carrier signal with the fundamental component yields very low subcarrier frequency harmonic content. Therefore, the subcarrier frequency harmonic content can be neglected in most applications. Since they determine the switching frequency harmonic copper losses and the torque ripple of a motor load and the line current Total Harmonic Distortion (THD) of a PWM-VSC, the switching frequency harmonic characteristics of a PWM-VSI drive are important in determining its performance. While the THD and the copper losses are measured over a fundamental cycle and therefore require a per fundamental cycle (macroscopic) RMS ripple current value calculation, the peak and local harmonic stresses are properly investigated on a per carrier cycle (microscopic) base. Therefore, first a microscopic and then a macroscopic

investigation is required.

Perhaps, the most intuitive and straightforward approach for analytical investigation of the switching frequency harmonic characteristics of a PWM-VSI is the vector space approach [4, 31, 103, 105]. As illustrated in the vector diagram of Fig. 3.13, in the first sector of the inverter hexagon, selecting the adjacent and zero states to balance the reference volt-seconds results in generating the harmonic voltage vectors V_{1h}, V_{2h}, and V_{0h} within each carrier cycle. As the figure indicates, the magnitude and phase of each harmonic voltage vector is modulation index and space dependent. Along with the harmonic voltage vectors, the duty cycle of the active inverter states and partitioning of the two zero states determine the harmonic current trajectories. Instead of the harmonic current trajectories, the conceptual harmonic flux (time integral of the harmonic voltage vector) λ_h trajectories can be investigated and with the assumption the load switching frequency model is an inductance, the harmonic current and harmonic flux trajectories are only different in scale ($\lambda = Li$). Since the inductance component of the load transient impedance model (an R-L series circuit) dominates the resistance component, this assumption is valid in most applications with $\frac{f_s}{f_e} > 20$). The harmonic flux in the N'th carrier cycle is calculated in the following.

$$\lambda_h(M_i, \theta, V_0) = \int_{NT_s}^{(N+1)T_s} (V_k - V^*)dt \tag{3.20}$$

In the above formula, V_k is the inverter output voltage vector of the k'th

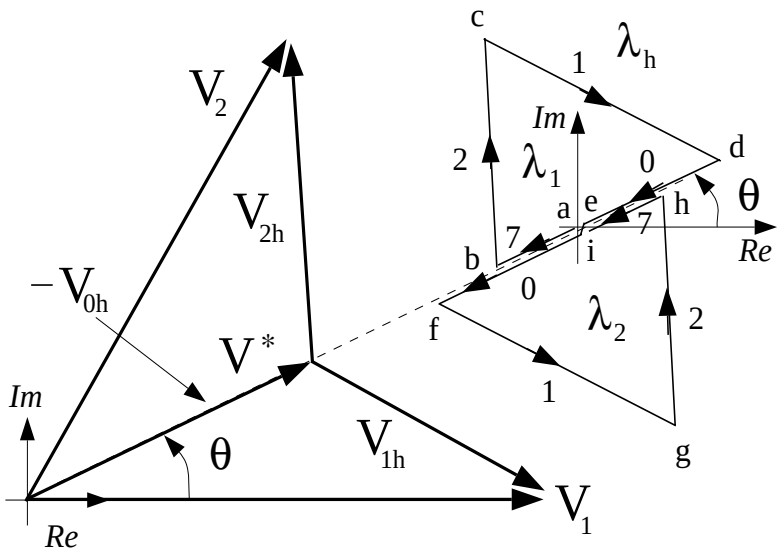

Figure 3.13: Harmonic flux trajectories in the first segment of the hexagon.

state and within the carrier cycle it changes according to the selected switching sequence. For example, in the first segment of the inverter hexagon ($R = 1$), all the modern PWM methods generate the sequence 7-2-1-0-0-1-2-7 and in the DPWM methods the "7" or the "0" states are absent. Note the above harmonic flux calculation requires no load information, and completely characterizes the switching frequency behavior of a modulator. Since for high $\frac{f_s}{f_e}$ values the V^* term can be assumed constant within a carrier cycle, and the V_k terms are constant complex numbers, the above integral can be closed form calculated and the flux trajectories are linear over each state. Assuming its value at the beginning of the carrier cycle is zero, the harmonic flux vector becomes zero at the half cycle point and at the end of the carrier cycle again. Therefore, (3.20) always assumes zero initial value. Since in the triangular intersection and direct digital PWM methods only symmetric switching sequences are generated, the

integral need only be calculated in the first half of the carrier cycle and the second half of the trajectory is exactly symmetrical to the first. As illustrated in Fig. 3.13 for the first segment of the inverter hexagon, the harmonic flux trajectories form two triangles which may slide along the reference vector line in opposite directions with respect to the origin. It is apparent from the diagram ZSP determines the slip of the triangles and affects the harmonic characteristics. Therefore, the harmonic flux trajectories of each PWM method are unique.

Calculating the harmonic flux vector for a half carrier cycle for the first region of the vector space for an arbitrary set of M_i, θ, and ZSP (or v_0) and normalizing to λ_b for further simplification, the following normalized analytical harmonic flux formula $\lambda_1(d, M_i, \theta)$ yields.

$$\lambda_b = \frac{2V_{dc}}{\pi}\frac{T_s}{2} \tag{3.21}$$

$$\lambda_1 = \frac{\lambda_{h1}}{\lambda_b} \tag{3.22}$$

$$\lambda_1 = \begin{cases} -M_i e^{j\theta} d & 0 \le d \le d_7 \\ -\frac{\pi}{3} e^{j\frac{\pi}{3}} d_7 + (\frac{\pi}{3} e^{j\frac{\pi}{3}} - M_i e^{j\theta}) d & d_7 \le d \le d_7 + d_2 \\ -M_i e^{j\theta}(d_7 + d_2) + \frac{\pi}{3} e^{j\frac{\pi}{3}} d_2 + & \\ (\frac{\pi}{3} - M_i e^{j\theta})(d - d_7 - d_2) & d_7 + d_2 \le d \le 1 - d_0 \\ \frac{\pi}{3}(d_1 + d_2 e^{j\frac{\pi}{3}}) - M_i e^{j\theta} d & 1 - d_0 \le d \le 1 \end{cases} \tag{3.23}$$

In the above equation, the "d" variable is inverter state duty cycle over a half carrier cycle ($\frac{t}{\frac{T_s}{2}}$). As the equation indicates, it starts at 0 at the beginning of the half carrier cycle and it becomes 1 at the end of the half carrier cycle. In the second half of the carrier cycle, the harmonic flux can be calculated from the symmetry condition: $\lambda_2(d) = -\lambda_1(1-d)$. However, in this half the inverter state duty cycles must be evaluated in the reverse sequence to the first half of the carrier cycle. The above equation can be easily programmed for any PWM method and the space and modulation index dependency of the harmonic flux/current can be graphically illustrated. Since the inverter hexagon has a six-fold symmetry, only the first segment need be investigated. The duty cycle of the active states d_1 and d_2 in this segment are calculated from (3.11) and (3.12). In the direct digital method the zero states are directly defined, while in the triangle intersection method the modulation waves are utilized to calculate the phase duty cycles from (3.4) and (3.5). For example, for R=1 Fig. 3.6 suggests $d_0 = d_{a-} = 1 - d_{a+}$ and $d_7 = d_{c+}$.

Figure 3.14 illustrates the normalized harmonic flux trajectories which are calculated from (3.23) for various modulators and operating conditions. To allow better visualization and clearer harmonic flux trajectory comparison, only the trajectories in the first half of a carrier cycle are illustrated in the figure and the second half is always the exact symmetric of the first. Figure 3.14 (a) illustrates the space dependency of the SPWM method harmonic flux. As the figure indicates, the "0" and "7" state duty cycles are not always equally split and the varying triangle shapes indicate the space dependency of the harmonic

flux is strong. Figure 3.14 (b) compares SVPWM and THIPWM1/4 for two different angular positions. At $w_e t = 30°$ the triangles are identical, however at $w_e t = 15°$ the triangles have slipped. While SVPWM splits the zero states equally, the THIPWM1/4 method does slide the triangle in the direction that the center of gravity becomes closer to the origin. Since the distance to the origin is equal to the magnitude of the harmonic flux, the trajectories which are closer to the origin result in smaller harmonic flux and the per carrier cycle RMS flux value decreases[106]. Figure 3.14 (c) and (d) compare SVPWM and DPWM1 and illustrate that the DPWM method always skips one of the two zero states. Therefore the DPWM1 flux triangle is quite distant from the origin. However, increasing the carrier frequency shrinks the triangle size and brings the weight center of the triangle closer to the origin and reduces the harmonic flux. When comparing the CPWM and DPWM modulator performances, to account for the reduction in the number of per fundamental cycle switchings of the DPWM methods, a carrier frequency coefficient k_f is introduced in the following.

$$k_f = \frac{f_{sCPWM}}{f_{sDPWM}} \tag{3.24}$$

Employing (3.23), the per carrier cycle RMS value of the harmonic flux λ_{1RMS} can be closed form calculated. Since the first and the second halves of the trajectory have the same RMS value due to symmetry, calculating only the first is sufficient. Involved calculations yield the following M_i and duty cycle

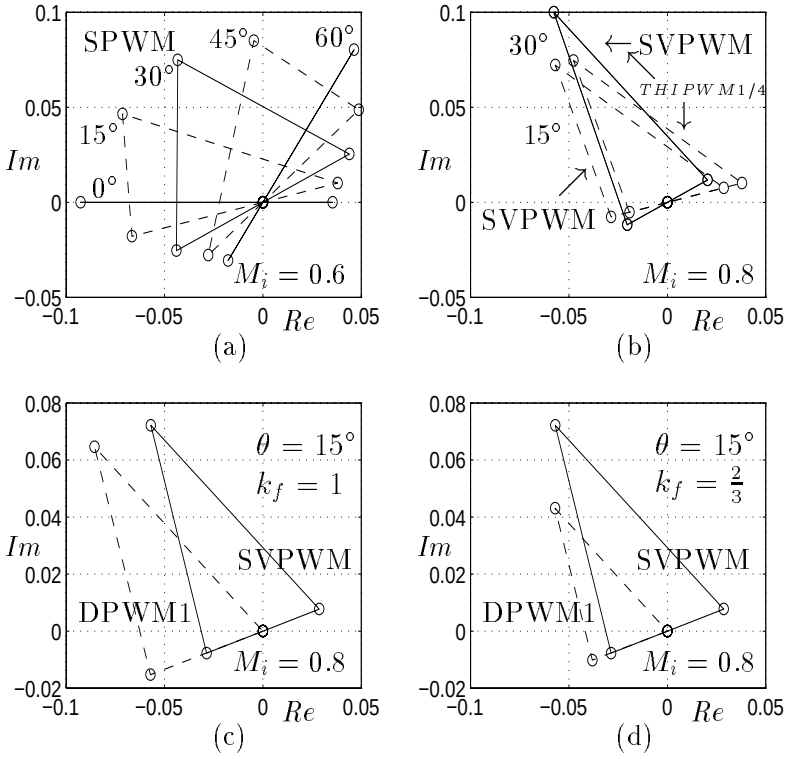

Figure 3.14: The switching frequency harmonic flux trajectories of various PWM methods. (a): SPWM, (b): SVPWM and THIPWM1/4 compared for $w_e t = 15°$ and $w_e t = 30°$ values, (c): SVPWM and DPWM1 compared ($k_f = 1$), (d): SVPWM and DPWM1 compared for $k_f = \frac{2}{3}$.

dependent formula.

$$\lambda_{1RMS}^2 = \int_0^1 \lambda_1^2 dd = \lambda_{11}^2 + \lambda_{12}^2 + \lambda_{13}^2 \tag{3.25}$$

$$\lambda_{11}^2 = \frac{\pi^2}{18} M_i^2 (\frac{1}{3} + d_0^2 + d_1^2 - d_0 - d_1 + 2d_0 d_1) \tag{3.26}$$

$$\lambda_{12}^2 = \frac{\pi^4}{72} [\frac{1}{3}(2d_1^3 - 4d_2^3 - 4d_1^4 + 2d_2^4 + 7d_1 d_2^3 - 2d_2 d_1^3) + d_1^2 d_2^2] \tag{3.27}$$

$$\lambda_{13}^2 = \frac{\pi^4}{72} [-d_1 d_2^2 + d_0(d_1 d_2^2 - 2d_1^3 + 2d_2^3 - d_1^2 d_2)] \tag{3.28}$$

Employing the above formula, the θ and M_i dependency of λ_{1RMS}^2 of various PWM methods can be easily computed and graphically illustrated. Figure 3.15 and Fig. 3.16 compare the RMS harmonic flux characteristics of the modern PWM methods for two modulation index values. The figures indicate the CPWM methods have lower harmonic distortion than the DPWM methods and the difference is more pronounced at low M_i. The THIPWM1/4 method, which is the minimum harmonic distortion method (the optimality condition can be verified by searching the minimum of (3.25) with respect to d_0 [105]), has only slightly less distortion than SVPWM and only near the 15° and 45° range. Since the DPWM methods have a discrete ZSP (0 or 1), within certain segments the ZSP of various DPWM methods is the same (see Fig.3.9). Therefore, calculating

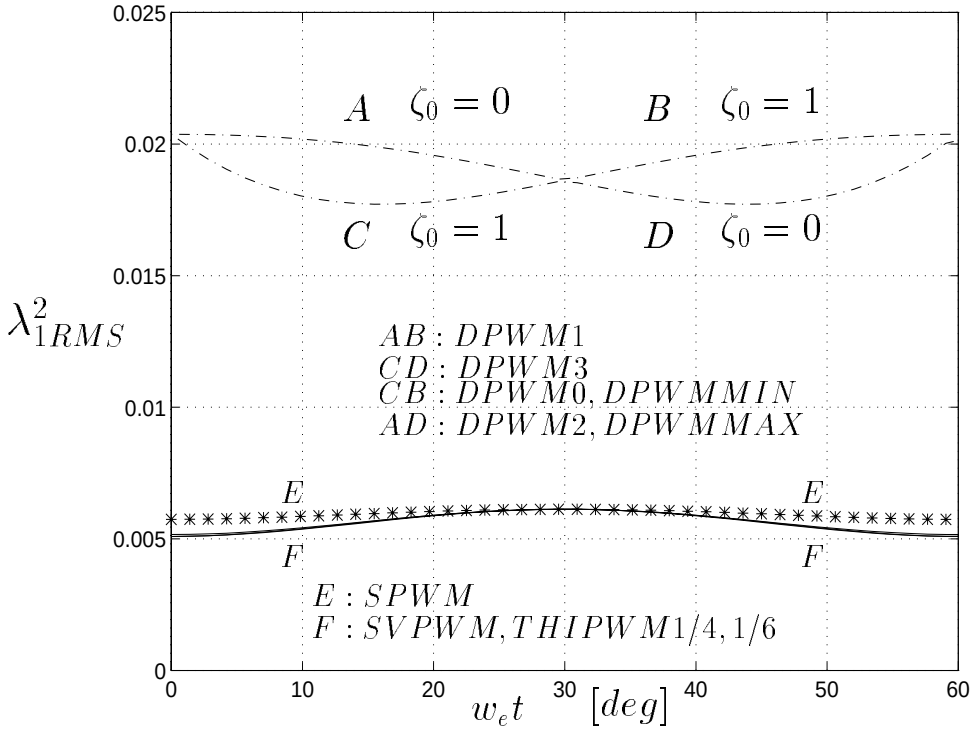

Figure 3.15: The space dependency of the per carrier cycle normalized RMS harmonic flux of the modern PWM methods for $M_i = 0.4$.

the RMS harmonic flux of DPWM methods is a relatively simple task. According to Fig. 3.15, $\zeta_0 = 0$ for segment A and $\zeta_0 = 1$ for segment C are the only two functions required to determine the RMS flux curves of all DPWM methods. The overall comparison indicates that SVPWM provides superior performance in the low modulation range. However, as M_i increases the performance of DPWM methods significantly improves and becomes comparable to SVPWM.

As Fig. 3.15 and Fig. 3.16 clearly illustrate the strong space dependency of the per carrier cycle RMS harmonic distortion characteristics of all the modern

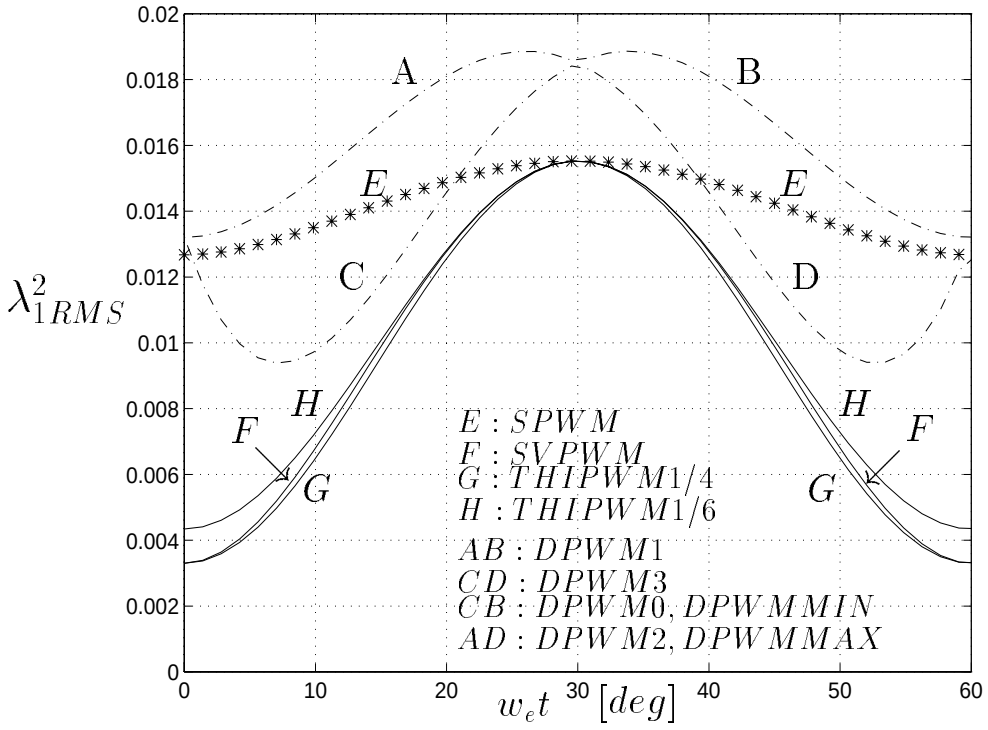

Figure 3.16: The space dependency of the per carrier cycle normalized RMS harmonic flux of the modern PWM methods for $M_i = 0.78$.

PWM methods, it becomes apparent that performance can be gained by modulating the carrier frequency. If the carrier frequency is methodically increased at the high RMS harmonic flux intervals and reduced at the low harmonic RMS flux intervals, then the overall harmonic distortion characteristics can be reduced [72]. Provided the inverter average switching frequency is maintained constant, the switching loss characteristics are not affected by the frequency modulation and performance gain without efficiency reduction becomes possible. Since the frequency modulation techniques are most beneficial to modulators with strongly space dependent RMS harmonic flux characteristics, CPWM methods are more suitable candidates than DPWM methods for this approach. In addition to reducing the RMS harmonic distortion and the peak ripple current, the frequency modulation techniques also flatten the inverter output voltage/current harmonic spectrum. Therefore, they are suitable for high power quality applications that require a flat harmonic spectrum with no dominant harmonic content.

Since it determines the waveform quality and harmonic losses, the per fundamental cycle RMS value λ_{1FRMS} of the harmonic flux is the most important performance characteristic of a modulator. Since the λ^2_{1RMS} characteristics of the modern PWM methods have sixfold space symmetry, the per fundamental cycle (per 60° in space) RMS harmonic flux value can be calculated in the following.

$$\lambda_{1FRMS}^2 = \frac{3}{\pi}\int_0^{\frac{\pi}{3}} \lambda_{1RMS}^2 d\theta \tag{3.29}$$

For each modulator, the above integral yields a polynomial function of M_i with unique coefficients and it can be written in the following M_i dependent Harmonic Distortion Function (HDF) formula.

$$\lambda_{1FRMS}^2 = \frac{\pi^2}{288} HDF = \frac{\pi^2}{288}(a_m {M_i}^2 + b_m {M_i}^3 + c_m {M_i}^4) \tag{3.30}$$

$$HDF = a_m {M_i}^2 + b_m {M_i}^3 + c_m {M_i}^4 \tag{3.31}$$

Calculating a_m, b_m, and c_m of each modulator involves significant algebraic manipulations. The resulting HDF functions of the discussed modulators are summarized in the following.

$$HDF_{SPWM} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{9}{8})(\frac{4}{\pi}M_i)^4 \tag{3.32}$$

$$HDF_{THIPWM6} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{4}{\pi}M_i)^4 \tag{3.33}$$

$$HDF_{THIPWM4} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{63}{64})(\frac{4}{\pi}M_i)^4 \tag{3.34}$$

$$HDF_{SVPWM} = \frac{3}{2}(\frac{4}{\pi}M_i)^2 - \frac{4\sqrt{3}}{\pi}(\frac{4}{\pi}M_i)^3 + (\frac{27}{16} - \frac{81\sqrt{3}}{64\pi})(\frac{4}{\pi}M_i)^4 \qquad (3.35)$$

Notice in all the CPWM methods the first two terms are the same and the third term involves the dominant coefficient of the ZSP of each method. As was shown in Fig. 3.15 and Fig. 3.16, the harmonic flux of DPWM methods consists of a combination of the A, B, C, and D segments. A and B yield equivalent distortion, likewise do C and D. Therefore, calculating the HDF of A and B segments (HDF_{DMAX}), and C and D segments (HDF_{DMIN}) is sufficient in determining the performance of all the DPWM methods discussed. The results are as follows.

$$HDF_{DMAX} = 6(\frac{4}{\pi}M_i)^2 - (\frac{8\sqrt{3}+45}{2\pi})(\frac{4}{\pi}M_i)^3 + (\frac{27}{8} + \frac{27\sqrt{3}}{32\pi})(\frac{4}{\pi}M_i)^4 \quad (3.36)$$

$$HDF_{DMIN} = 6(\frac{4}{\pi}M_i)^2 + (\frac{45-62\sqrt{3}}{2\pi})(\frac{4}{\pi}M_i)^3 + (\frac{27}{8} + \frac{27\sqrt{3}}{16\pi})(\frac{4}{\pi}M_i)^4 \quad (3.37)$$

For the same carrier frequency the DPWM methods have less switchings per fundamental cycle than the CPWM methods. Therefore, to account for the carrier frequency effect, the PWM frequency coefficient k_f is included in the HDF formulas of the DPWM methods.

$$HDF_{DPWM1} = {k_f}^2 \times HDF_{DMAX} \qquad (3.38)$$

$$HDF_{DPWM3} = {k_f}^2 \times HDF_{DMIN} \tag{3.39}$$

$$HDF_{DPWM0} = {k_f}^2 \times 0.5 \times (HDF_{DMIN} + HDF_{DMAX}) \tag{3.40}$$

$$HDF_{DPWM2} = HDF_{DPWMMIN} = HDF_{DPWMMAX} = HDF_{DPWM0} \tag{3.41}$$

The relation between HDF and the per phase harmonic current RMS value I_h for a load with a transient inductance L_σ, which can be utilized in calculating the harmonic copper losses, is as follows.

$$I_{xh}^2 = \left(\frac{V_{dc}}{24 L_\sigma f_s}\right)^2 \times HDF(M_i) \qquad for \qquad x \in \{a, b, c\} \tag{3.42}$$

Figure 3.17 shows the HDF curves of all the discussed PWM methods. In the very low modulation index range all CPWM methods have practically equal HDF which is superior to all DPWM methods. As the modulation index increases the SPWM performance rapidly degrades while the remaining CPWM methods maintain low HDF over a wide modulation range. The figure indicates the THIPWM1/4 performance is only slightly better than SVPWM, and the difference is less noticeable from the local differences shown in Fig. 3.14 and Fig. 3.16. In the high modulation range the DPWM methods are superior to SVPWM (Fig. 3.17) and the intersection point of the DPWM method of

choice and SVPWM defines the optimal transition point. Although in the high modulation range the DPWM3 method has less HDF than the other DPWM methods, the improvement is marginal and the modulator selection criteria can be based on the switching loss and voltage linearity characteristics which are stronger functions of the DPWM methods. The HDF function of the GDPWM method is ψ dependent, and varies between curves 5 and 6 of Fig. 3.17. Its HDF can be approximated with the average value of (3.38) and (3.40).

$$HDF_{GDPWM} \approx {k_f}^2 \times 0.25 \times (HDF_{DMIN} + 3 \times HDF_{DMAX}) \qquad (3.43)$$

Since the HDF of each PWM method is unique, harmonic spectrum of each method is also unique. Since the DPWM methods have two less switchings per carrier cycle than CPWM methods, for the same carrier frequency, the switching frequency side band harmonics of the DPWM methods are wider and larger in magnitude. Calculating the individual harmonics and the peak ripple current is involved and will be omitted herein. Having illustrated the superior high modulation range waveform quality characteristics of the DPWM methods over SVPWM, in the next section the switching losses of DPWM methods will be characterized to aid an intelligent modulator choice. Following a brief section on the inverter input current harmonics, the switching losses of the DPWM methods will be analytically modeled and their performance evaluated.

Notice all the PWM switching frequency harmonic calculations performed

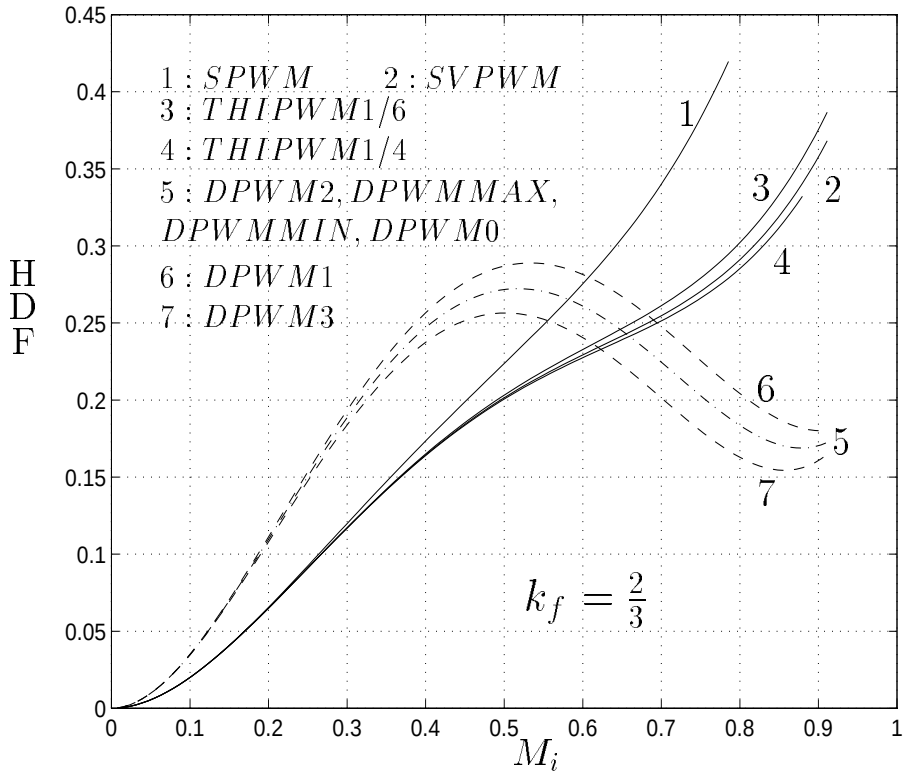

Figure 3.17: $HDF = f(M_i)$ curves in the linear modulation range under constant inverter average switching frequency condition.

until this stage are valid within the voltage linearity range of the corresponding modulators. Therefore, they are valid for SPWM until a modulation index of 0.785, for THIPWM1/4 until 0.881, and until 0.907 for the remainder of the modulators. Outside the voltage linearity range the low frequency harmonic content significantly increases and the performance substantially degrades. These characteristics will be investigated in the next chapter.

3.6 Inverter Input Current Harmonics

The DC link input current of a PWM inverter I_{in} consists of the DC average value I_{dc} which corresponds to the average power transfer to the load, and switching frequency component I_{inh}, which is due to PWM switching. Since during the zero states the DC link is decoupled from the AC load, the RMS value of the ripple current I_{inhRMS}, which is required in DC link capacitor design and loss calculations, is independent of the zero sequence signal and therefore of the modulator type. Since the duty cycles of the inverter active states are independent of the carrier frequency, I_{inhRMS} is also independent of the carrier frequency. Similar to the inverter output harmonic current RMS value calculation, I_{inhRMS} can also be easily calculated by establishing a per carrier cycle RMS value formula and evaluating it over 60° in vector space [103]. The calculation yields the following M_i, load power factor ($\cos\varphi$) and load current fundamental component RMS value (I_{1RMS}) dependent DC link current ripple factor K_{Iin} formula.

$$K_{Iin} = \frac{I^2_{inhRMS}}{I^2_{1RMS}} = \frac{2\sqrt{3}}{\pi^2} M_i + (\frac{8\sqrt{3}}{\pi^2} - \frac{18}{\pi^2} M_i) M_i \cos^2 \varphi \qquad (3.44)$$

Figure 3.18 illustrates the M_i and $\cos\varphi$ dependency of the K_{Iin} factor. The maximum ripple occurs at $\cos\varphi = 1$ and at $M_i = \frac{5\sqrt{3}}{18} \approx 0.48$ (a reasonable design point for capacitor sizing) and the ripple is independent of $\cos\varphi$ at $M_i = \frac{8\sqrt{3}}{18} \approx 0.77$. The closed form approach is intuitive and can aid capacitor design, while the previously reported computer simulation data evaluation based graphic illustration is laborious and not user-friendly [210].

Notice although the RMS value of the ripple is independent of the modulation method, the harmonic spectrum is strongly influenced by the modulation method choice. A recent publication investigates the harmonic spectrum characteristics of various PWM methods for AC/DC/AC PWM-VSI drives [170].

The DC average value of the DC link input current, I_{dc}, can also be closed form calculated as a function of the modulation index, RMS load current, and the load power factor. Assuming steady state operating conditions and sinusoidal load currents with zero harmonics, the average value of the input current can be calculated from the inverter average input power equation in the following.

$$I_{dc} = \frac{3\sqrt{2}}{\pi} M_i I_{1RMS} \cos\varphi \qquad (3.45)$$

Although the above formula may not be useful in design, it helps understand

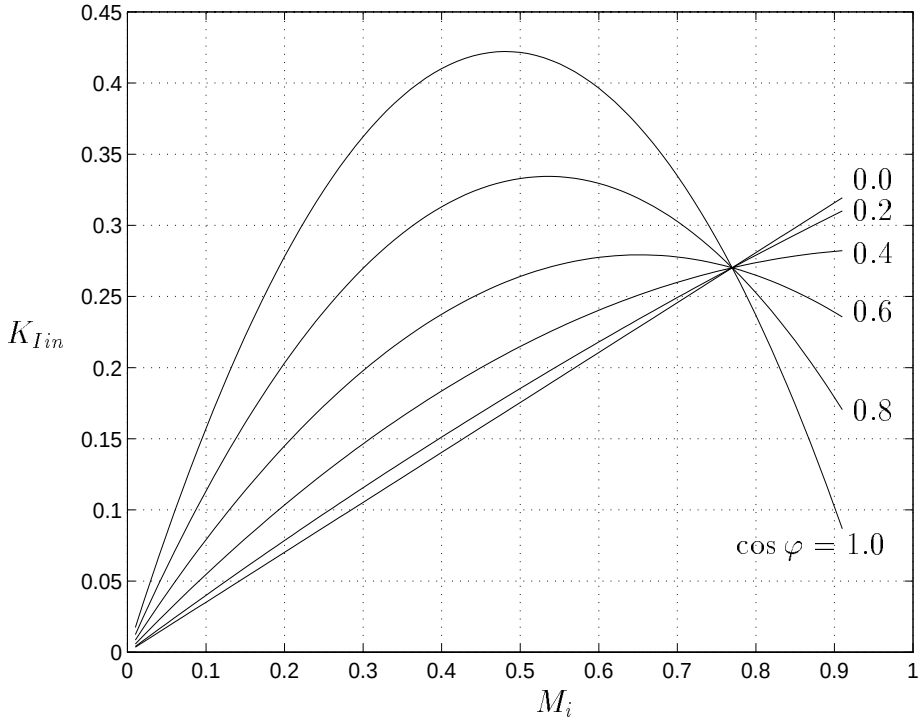

Figure 3.18: Normalized inverter input harmonic current RMS value characteristics $K_{Iin} = f(M_i)$ of PWM-VSI for $\cos\varphi$ as parameter.

the inverter steady state behavior. It indicates DC bus loading linearly increases with the modulation index and the load current active component ($I_{1RMS}\cos\varphi$).

3.7 Switching Losses

The switching losses of a PWM-VSI drive are load current dependent and increase with the current magnitude. Switching device manufacturer's data books (for example, IGBT data books [81]) indicate this relation is approximately linear, i.e. the switching losses are proportional to the current magnitude.

With CPWM methods, all the three phase currents are commutated within each carrier cycle of a full fundamental cycle. Therefore, for all CPWM methods the switching losses are the same and independent of the load current phase angle (power factor angle). With DPWM methods, however, the switching losses are significantly influenced by the modulation method and load power factor angle. Because DPWM methods cease to switch each switch for a total of 120° per fundamental cycle and the location of the unmodulated segments with respect to the modulation wave fundamental component phase is modulator type dependent. Therefore, the load power factor and the modulation method together determine the time interval that the load current is not commutated. Since the switching losses are strongly dependent on and linearly increase with the magnitude of the commutating phase current, selecting a DPWM method with reduced switching losses can significantly contribute to the performance of

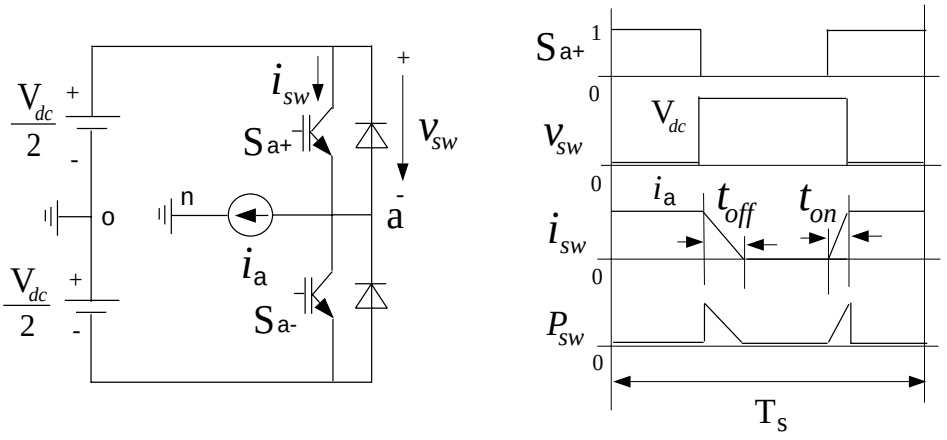

Figure 3.19: The inverter per phase model and per carrier cycle switching loss diagram under linear commutation.

a drive. Therefore, it is necessary to characterize and compare the switching losses of DPWM methods.

Assuming the inverter switching devices have linear current turn-on and turn-off characteristics with respect to time and accounting only for the fundamental component of the load current, the switching losses of a PWM-VSI drive can be analytically modeled [107]. Shown in Fig. 3.19, the single phase inverter model and the switching voltage/current diagram aid calculating the switching losses. Deriving the local (per carrier cycle) switching loss formula and calculating its average value over the fundamental cycle, the per fundamental cycle inverter per device switching loss P_{swave} can be calculated as follows.

$$P_{swave} = \frac{1}{2\pi} \frac{V_{dc}(t_{on} + t_{off})}{2T_s} \int_0^{2\pi} f_i(\theta) d\theta \tag{3.46}$$

In the above formula, t_{on} and t_{off} variables represent the turn-on and turn-off times of the switching devices, and $f_i(\theta)$ is the switching current function. The switching current function $f_i(\theta)$ equals zero in the intervals where modulation ceases and the absolute value of the corresponding phase current value elsewhere. For example, for phase "a," this function is as follows.

$$f_{ia}(\theta) = \begin{cases} 0 & |v_a^{**}| \geq \frac{V_{dc}}{2} \\ |i_a| & |v_a^{**}| < \frac{V_{dc}}{2} \end{cases} \tag{3.47}$$

The calculation assumes steady state operating conditions where the currents are practically sinusoidal functions. Therefore, $|i_a|$ is a function of the load power factor angle and the current magnitude. As a result, the phase current power factor angle φ enters the formula as the integral boundary term and φ dependent switching loss formula yields. Normalizing P_{swave} to P_o, the switching loss value under CPWM condition (which is φ independent), the Switching Loss Function (SLF) of a modulator can be found.

$$P_o = \frac{V_{dc} I_{max}}{\pi T_s} \times (t_{on} + t_{off}) \tag{3.48}$$

$$SLF = \frac{P_{swave}}{P_o} \tag{3.49}$$

In (3.48) the variable I_{max} represents the load current fundamental component maximum value. By the definition of (3.46), the SLF of CPWM methods is

unity. The SLF of DPWM methods can be easily calculated from their current switching function. Figure 3.20 shows the ψ and φ dependent switching current and switching loss function waveforms of GDPWM. Applying the procedure to GDPWM yields the following SLF.

$$SLF_{GDPWM} = \begin{cases} \frac{\sqrt{3}}{2}\cos\left(\frac{4\pi}{3}+\psi-\varphi\right) & -\frac{\pi}{2} \le \varphi \le -\frac{\pi}{2}+\psi \\ 1-\frac{1}{2}\sin\left(\frac{\pi}{3}+\psi-\varphi\right) & -\frac{\pi}{2}+\psi \le \varphi \le \frac{\pi}{6}+\psi \\ \frac{\sqrt{3}}{2}\cos\left(\frac{\pi}{3}+\psi-\varphi\right) & \frac{\pi}{6}+\psi \le \varphi \le \frac{\pi}{2} \end{cases} \tag{3.50}$$

The SLF function of the DPWM0, DPWM1, and DPWM2 can be easily evaluated from (3.50) by substituting $\psi = 0$, $\psi = \frac{\pi}{6}$, and $\psi = \frac{\pi}{3}$. The SLF of the remaining DPWM methods are as follows.

$$SLF_{DPWMMIN} = \begin{cases} \frac{1}{2}-\frac{1}{4}\sin\varphi & -\frac{\pi}{2} \le \varphi \le -\frac{\pi}{6} \\ 1-\frac{\sqrt{3}}{4}\cos\varphi & -\frac{\pi}{6} \le \varphi \le \frac{\pi}{6} \\ \frac{1}{2}+\frac{1}{4}\sin\varphi & \frac{\pi}{6} \le \varphi \le \frac{\pi}{2} \end{cases} \tag{3.51}$$

$$SLF_{DPWMMAX} = SLF_{DPWMMIN} \tag{3.52}$$

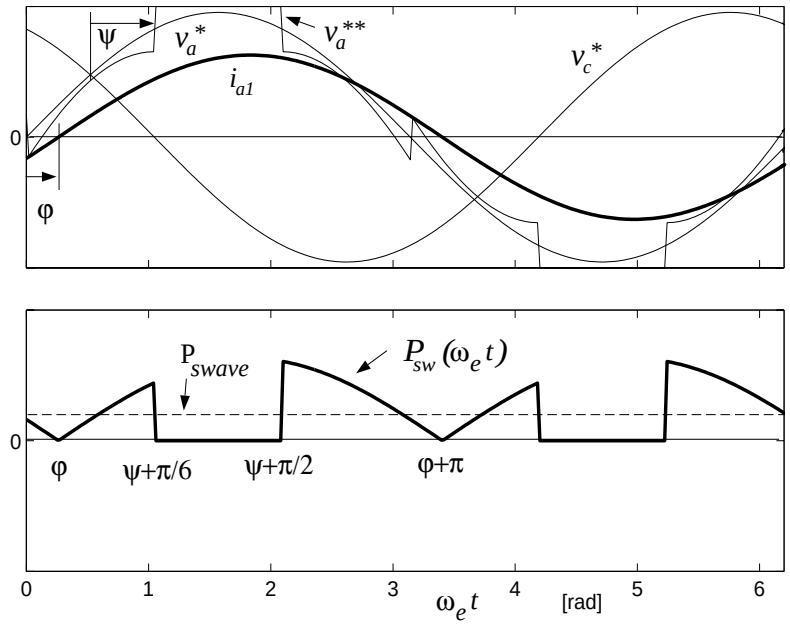

Figure 3.20: The average switching losses of GDPWM, $P_{swave} = f(\psi, \varphi)$.

$$SLF_{DPWM3} = \begin{cases} 1 + 0.5(\sqrt{3} - 1)\sin\varphi & -\frac{\pi}{2} \leq \varphi \leq -\frac{\pi}{3} \\ 0.5(\cos\varphi - \sin\varphi) & -\frac{\pi}{3} \leq \varphi \leq -\frac{\pi}{6} \\ 1 - 0.5(\sqrt{3} - 1)\cos\varphi & -\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{6} \\ 0.5(\cos\varphi + \sin\varphi) & \frac{\pi}{6} \leq \varphi \leq \frac{\pi}{3} \\ 1 - 0.5(\sqrt{3} - 1)\sin\varphi & \frac{\pi}{3} \leq \varphi \leq \frac{\pi}{2} \end{cases} \tag{3.53}$$

Shown in Fig. 3.21, SLF surface of GDPWM indicates that its switching losses are a strong function of the load power factor angle. As the three dimensional graphic indicates, the switching losses can be minimized by controlling the modulator phase angle as a function of the load power factor angle. It is apparent from the figure the SLF surface touches the $SLF = 0.5$ plane along a straight line. In the $-\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{6}$ region, selecting $\psi = \varphi + \frac{\pi}{6}$ results in

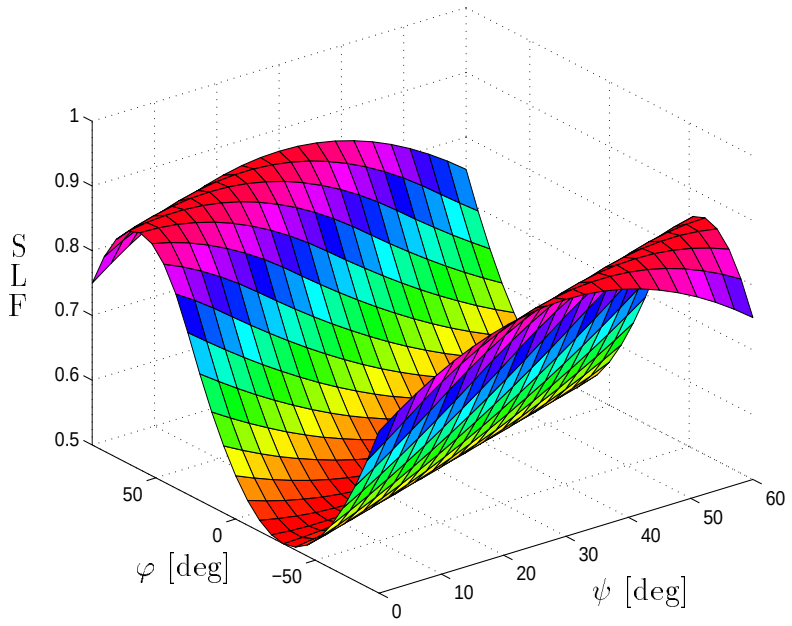

Figure 3.21: $SLF = f(\psi, \varphi)$ function of the GDPWM method.

minimum switching loss value ($SLF_{min} = 0.5$) which is equal to 50 % of the CPWM methods ($SLF_{CPWM} = 1.0$). Outside this range, the modulator phase angle must be held at the boundary value of $\psi = \frac{\pi}{3}$ (DPWM2) for positive φ and at the value of $\psi = 0$ (DPWM0) for negative φ so that the GDPWM voltage linearity is retained. As a result, in these operating regions the switching losses become more than 50 % and less than 75 % of the switching losses of CPWM methods and the exact amount can be found from the 3-D SLF surface of Fig. 3.21.

Figure 3.22 shows the SLF characteristics of the modern DPWM methods along with the optimum SLF solution of the GDPWM method. Note that outside the $-\frac{5\pi}{12} \leq \varphi \leq \frac{5\pi}{12}$ range DPWM3 yields minimum switching losses. As

Fig. 3.22 indicates, the switching losses of DPWM methods strongly depend on φ and can be reduced to 50% of the CPWM methods. The graphic suggests combining GDPWM and DPWM3 would result in optimum SLF. A control algorithm should select GDPWM within $-\frac{5\pi}{12} \leq \varphi \leq \frac{5\pi}{12}$ and optimize it with the above described ψ choice. Outside this φ range DPWM3 should be selected. With such a choice, the optimal SLF curve of Fig. 3.23 results. Note with this algorithm the switching losses become less than 65% of the CPWM methods.

The switching loss analysis with the aid of SLF has shown the modulator choice strongly influences the drive efficiency and thermal design. Since the switching losses are load power factor angle dependent, the modulator choice should involve the power factor value. Drives mostly operating near unity power factor could utilize GDPWM and optimize its phase angle for minimum losses. For example, most induction motor drives and permanent magnet motor drives operate within $-30° \leq \varphi \leq 30°$ range and therefore on-line optimized GDPWM is sufficient in such applications. In reactive power compensation applications (PWM-VSI VAr compensators) the DPWM3 method provides minimum switching losses in addition to low harmonic distortion. Applications with widely varying power factor conditions could utilize the combined algorithm and benefit from both DPWM3 and the optimal GDPWM method. Induction motor drives with frequent no-load operating conditions can utilize this algorithm to maximize the drive performance. Perhaps, the most suitable applications of the combined algorithm are the future generation intelligent drives such as universal drives. With the controller tuning the modulator on-line for the application, or

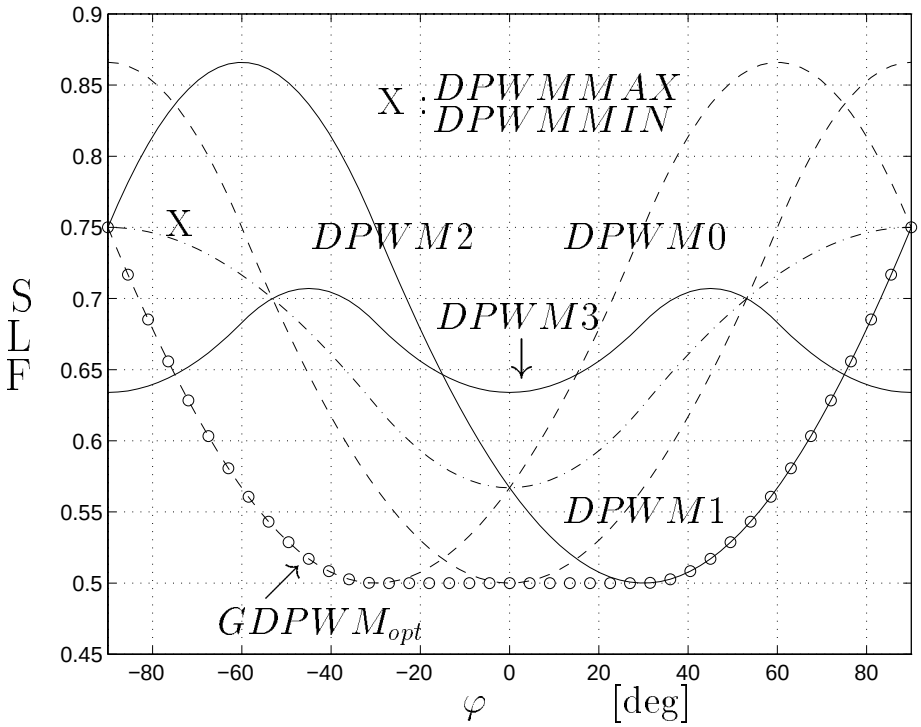

Figure 3.22: $SLF = f(\varphi)$ characteristics of the popular DPWM methods under fixed carrier frequency constraint ($SLF_{CPWM} = 1$).

by allowing the user to configure the modulator of his/her choice, an increased level of performance and satisfaction to the costumer would result. Therefore, this algorithm will be an indispensable feature of future generation drives.

Although the absolute switching loss values obtained from (3.46) may have limited accuracy due to unmodeled switching device characteristics, the relative switching losses which are represented with the SLF function are always predicted with higher accuracy. Since the SLF derivation assumes the same device characteristics both in P_{swave} and P_o, the error direction is the same in both terms and therefore the relative error is less than the absolute error. The SLF functions are effective analytical tools for evaluating and comparing

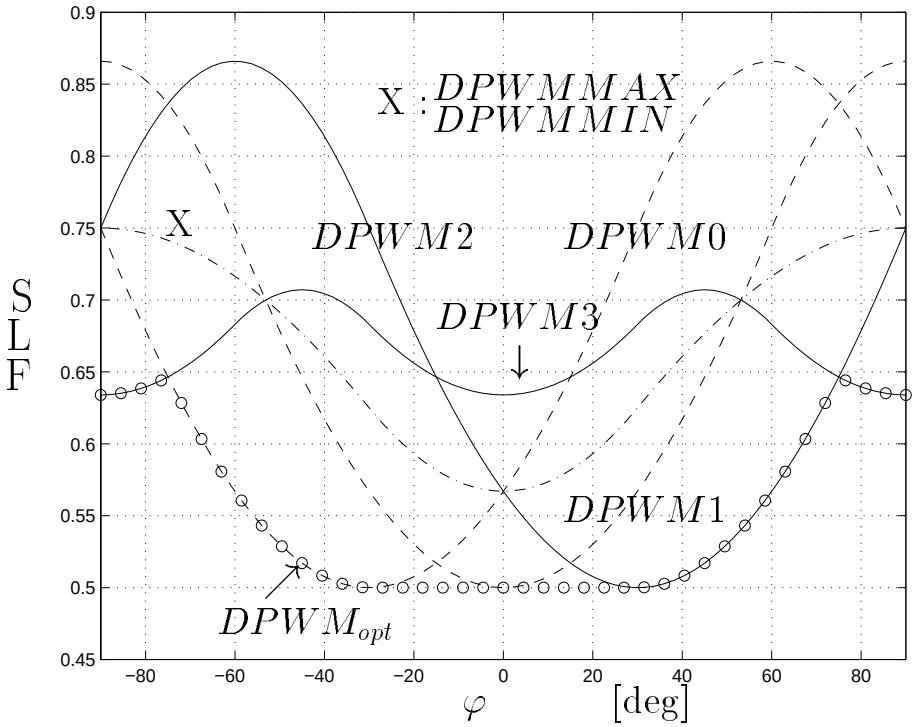

Figure 3.23: Graphic illustrates combining the SLF of GDPWM and DPWM3 minimum switching losses are attained.

the switching losses of various DPWM methods. In particular, the switching loss comparison of different PWM methods with SLF is highly accurate and meaningful. The detailed thermal modeling approach is very laborious [125] and depending on the thermal model accuracy, the calculation accuracy can be poorer than the SLF approach. Device characteristic modeling in a computer simulation is more involved than the first two methods and its accuracy is again limited to the accuracy of the device simulation model.

Unlike the switching losses, the switching device conduction losses are only slightly dependent on the modulator type. The modulator type and load power factor dependency of the conduction losses was investigated thoroughly by Kolar et al. and it was illustrated the zero sequence signal has a negligible influence on the conduction losses [107]. Therefore, switching device loss comparison of various modulators need only involve the SLF function.

When the performance criteria is only switching loss minimization, the above discussed algorithms can utilize the load power factor information and select a modulation signal which minimizes the SLF function. However, as the linear modulation range expires at high modulation index levels, the nonlinear modulation range performance characteristics increasingly dominate the drive performance. The waveform quality, voltage gain, and dynamic performance characteristics of the drive substantially degrade and in addition to SLF and

HDF, the inverter overmodulation performance characteristics must be considered. The following brief section discusses the linearity boundaries of the modern modulators. Then laboratory experiments illustrate the linear modulation region performance characteristics of the conventional and the newly developed high performance modulator/control algorithms.

3.8 Voltage Linearity

In the triangle intersection PWM technique, when the modulation wave magnitude becomes larger than the triangular carrier wave peak value, $\pm\frac{V_{dc}}{2}$, the inverter ceases to match the reference per carrier cycle volt-seconds, and a nonlinear reference-output voltage relation results within certain intervals. The linearity limit of a modulation method can be calculated by equating the peak of the modulation wave to the triangular carrier wave signal magnitude. With each modulation method, the peak of the modulation signal occurs at a different angle. SPWM's linear modulation range ends at $V_{1m}^{*} = \frac{V_{dc}}{2}$ i.e. a modulation index of $M_{LSPWM} = \frac{\pi}{4} \approx 0.785$. As previously discussed, injecting a zero sequence signal to the SPWM signal can flatten and contain the modulation wave within $\pm\frac{V_{dc}}{2}$ such that the linearity range is extended to at most $M_{Lmax} = \frac{\pi}{2\sqrt{3}} \approx 0.907$ which is the theoretical inverter linearity limit [32, 101]. With the exception of THIPWM1/4 which looses linearity at $M_{LTHIPWM1/4} = \frac{3\sqrt{3}}{7\sqrt{7}}\pi \approx 0.881$, all the discussed zero sequence injection PWM methods are linear until M_{Lmax}. Since SVPWM and all the discussed DPWM methods utilize the full inverter

hexagon, it is obvious they all have the same voltage linearity limit of M_{Lmax}. In the direct digital technique, when the reference voltage vector falls outside the modulator linearity region, (3.13) yields $t_0 + t_7 \leq 0$, indicating the reference volt-seconds can not be matched by the inverter and a volt-second error is inevitable. It is obvious that the smallest modulation index where the nonlinear (overmodulation) relation between the reference and output volt-seconds begins is defined by the largest circle inside the inverter hexagon.

Practically the theoretical voltage linearity limits are further reduced due to the inverter blanking time and Minimum Pulse Width (MPW) constraints. With a minimum allowable pulse width of t_{MPW}, a carrier cycle of T_s, and a theoretical modulator voltage linearity limit of M^t_{Lmax}, the practical modulator voltage linearity limit, M^p_{Lmax}, can be calculated by employing (3.4) in the following.

$$M^p_{Lmax} = M^t_{Lmax} \times (1 - k_m \frac{t_{MPW}}{T_s}) \tag{3.54}$$

The k_m coefficient is 1 for DPWM methods and 2 for CPWM methods. Therefore, DPWM methods have superior voltage linearity characteristics. This is due to the fact that DPWM methods utilize only one zero state in a carrier cycle while CPWM methods have two zero states. Therefore, the zero state time length of DPWM methods is always larger than the CPWM methods. Since the smallest zero state time length determines the minimum allowable pulse width, the DPWM methods can accomodate smaller minimum-on-time values. Hence,

a higher linear modulation limit.

In the DPWM methods, the low modulation index operating region also exhibits nonlinear reference-output voltage relations. Since in these methods the zero sequence signal at near zero modulation index is substantially large, the injection of this signal to the sinusoidal reference signals results in nearly saturated modulation signals. Figure 3.24 illustrates the modulation signal and the zero sequence signal at low modulation for DPWM1. Therefore, the DPWM methods have a lower limit on the voltage linearity. This limit can be calculated in a similar manner to the maximum voltage linearity limit. It can be seen in Fig. 3.24, the DPWM1 narrow pulse occurs at the $\theta = 0$ point and repeats every sixty-degrees. Again, the duty cycle calculation can be performed to determine the minimum voltage linearity limit. The calculation yields the following practical minimum voltage linearity limit equation which holds for all the discussed DPWM methods.

$$M_{Lmin}^{p} = \frac{\pi}{\sqrt{3}} \frac{t_{MPW}}{T_s} \tag{3.55}$$

The region starting from the end of the linear modulation region of a modulator until the six-step operating point ($M_i = 1$) is called the overmodulation region. All the PWM-VSI drives experience performance degradation in the overmodulation region [64, 75, 88, 169]. In the DPWM methods, as discussed in the above paragraph, from zero modulation index until M_{Lmin}^{p} an additional

nonlinear region exists. Perhaps, this nonlinear region can be termed as "undermodulation" region. In this region, similar performance problems as in the overmodulation region exist. In the overmodulation and undermodulation regions, the HDF and SLF functions are not accurate and they are not a suitable measure for performance evaluation. The following two chapters will investigate the overmodulation region behavior of different drive types and modulators. The influence of the blanking time and minimum pulse width on the modulator linearity will also be discussed in more detail. However, at this stage the linear modulation region drive performance laboratory investigations will be reported.

3.9 Experimental Results

The high performance PWM algorithm, which combines the SVPWM and GDPWM method superior performance characteristics, was tested in the laboratory on a $\frac{V}{f}$ controlled 5 HP induction motor drive. The VSI utilized a diode rectifier front end with a DC bus voltage of 620 V. The PWM-VSI drive control board was fully digital and employed a 40 MHz, 24-bit fixed point DSP. The digital PWM algorithm employed the triangular intersection technique and a simple software code generated the modulation signals. The carrier frequency was fixed at 5 kHz and modulation waves were fed to the digital PWM counters to generate the VSI gate switch signals. The drive had a $4\mu s$ blanking time, and through symmetric blanking time compensation the voltage pulses were precisely generated [117].

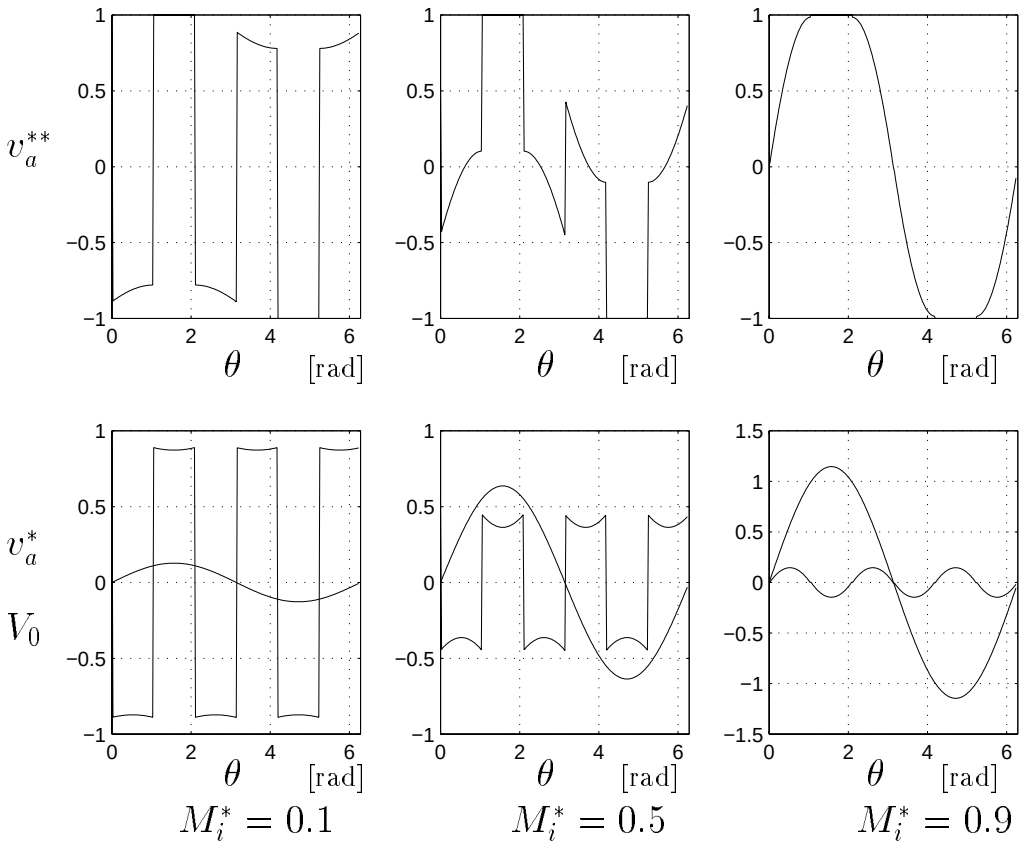

Figure 3.24: The modulation and zero sequence signals of DPWM1 for three M_i values.

The DSP generated the SVPWM and GDPWM modulation signals by employing the magnitude rules described in this chapter. Since the carrier frequency was fixed at 5 kHz, the theoretical HDF curve of SVPWM would be superior to GDPWM's curve within the linear modulation region. A transition from SVPWM to GDPWM in the linear modulation region would, therefore, imply waveform quality degradation. However, as discussed in the voltage linearity section of this chapter, the voltage linearity region of SVPWM expires before the GDPWM in the presence of minimum pulse width constraints. In the laboratory tests, a minimum pulse width control algorithm was employed and voltage pulses less than $12\mu s$ were eliminated (this approach is termed as Pulse Elimination Method (PEM)). With the given minimum pulse width constraint, the SVPWM linearity limit was calculated from (3.54) as $M_{iSVPWMmax} = 0.798$. This modulation index value could be selected as the transition modulation index from SVPWM to GDPWM. However, the experimental observation suggested that the current waveform quality with SVPWM did not immediately degrade and was slightly better than with GDPWM until approximately 0.81. Therefore, the transition modulation index value was selected as $M_{itr1} = 0.81$. Above this value, GDPWM was employed. The GDPWM method employed minimum SLF control algorithm ($\psi = \varphi + \frac{\pi}{6} \leq \frac{\pi}{3}$ for motoring) until the end of the linear region. The phase difference between a modulation wave and the corresponding phase current was measured to estimate the power factor angle.

Figure 3.25, Figure 3.26, and Figure 3.27 illustrate the modulation signal and motor phase current waveforms immediately before, during, and after transition

($M_i = 0.79, 0.81, 0.82$) at 50% of the rated motor torque (T_{eR}). Shown in the same oscillograms, the modulation waves were output from the DSP through and A/D converter and the triangular carrier signal gain is 10V/620V. The current waveform quality of all three figures, in particular the peak current ripple, is practically the same. Since the speed reference signal of the drive was fed to the DSP through an A/D converter, at the transition modulation index operating point ($M_i = M_{itr1}$) a small reference signal noise resulted in an oscillation between SVPWM and GDPWM. However, this zero sequence signal oscillation only affected the carrier frequency harmonic content of the motor current and as Fig. 3.26 shows, it would not disturb the motor current fundamental component and motion quality. This result is in correlation with the theory, which indicates the harmonic flux is zero at the beginning and the end of the carrier cycle. Due to the load equivalent resistance, the harmonic currents become slightly different from zero at the beginning and the end of the cycle. However, the residue current exponentially decays to zero with the load equivalent circuit R-L time constant. Therefore, rapid transition from SVPWM to GDPWM and back does not result in performance degradation. Therefore, it is not necessary to prohibit oscillations with any involved control algorithms.

Since the carrier frequency was constant, changing from SVPWM to GDPWM results in significant reduction in switching losses. With the power factor angle at the 50 % load operating point being larger than 30°, the SLF curve in Figure 3.22 indicates the losses are reduced by at least 45% when compared to SVPWM. As shown in Fig. 3.28 at $M_i = 0.854$ and 100% T_{eR}, the algorithm

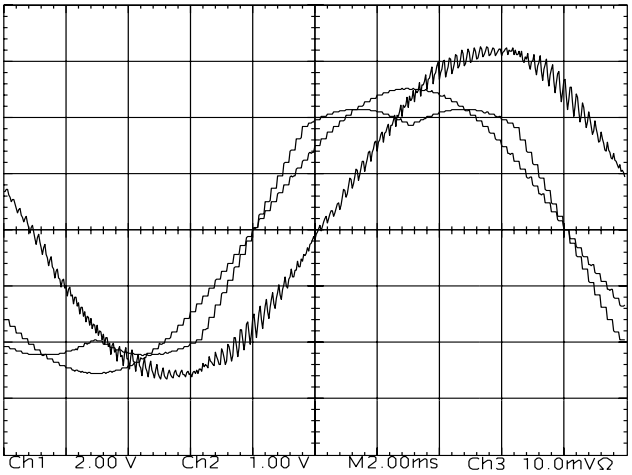

Figure 3.25: Experimental SVPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.79$, 49 Hz, $50\%T_{eR}$). Scales: 2 A /div, 2 V /div, 2ms/div.

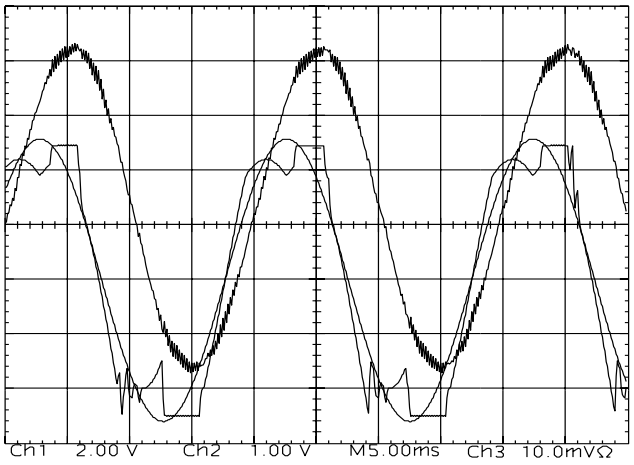

Figure 3.26: Transition from SVPWM to GDPWM ($M_i = 0.81$, 50 Hz, $50\%T_{eR}$). Scales: 2 A /div, 2 V /div, 5ms/div.

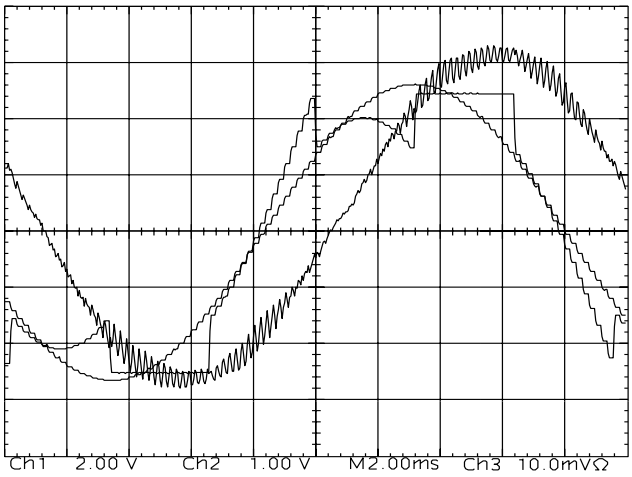

Figure 3.27: Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.82$, 51 Hz, $50\%T_{eR}$). Scales: 2 A /div, 2 V /div, 2ms/div.

on-line optimizes ψ to minimize the switching losses. Since the power factor angle for this operating condition is less than 30°, the transistor which conducts the largest current is held on and this reduces the switching losses by approximately 50% when compared to SVPWM. Confirming the improvement in the switching losses, the laboratory measurements showed notable decrease in the heat sink temperature. The experimental data for these operating conditions is illustrated in Table 3.1 in detail. The table indicates the GDPWM full load switching losses are less than the SVPWM switching losses under 50 % load operating condition.

A PWM algorithm which is solely based on not modulating the phase current with the largest magnitude [162] does not guarantee voltage linearity (at any M_i) except for the power factor angle range of $-30° < \varphi < 30°$. If the power factor angle is outside this range, and the phase with the largest current is clamped

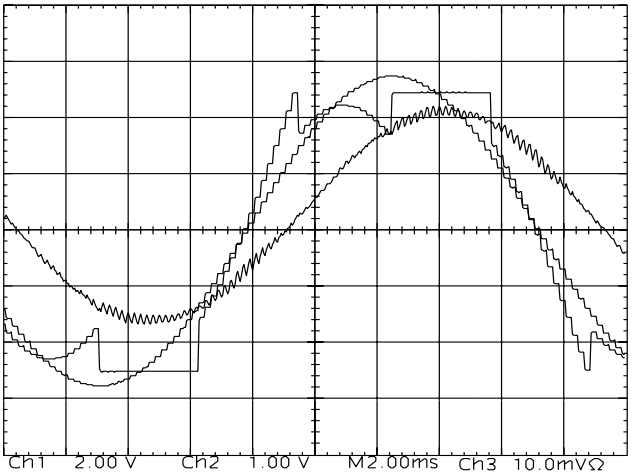

Figure 3.28: Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.854$, 53 Hz, $100\%T_{eR}$). Scaling: 5 A /div, 2 V /div, 2ms/div.

Table 3.1: SVPWM and GDPWM thermal performance data comparison

Method	M_i	T_L %	I_{max} (A)	T ($^\circ C$)
SVPWM	0.79	50	6	31.2
$GDPWM_{opt}$	0.81	50	6	30.6
$GDPWM_{opt}$	0.854	100	10	30.8

to the positive/negative DC rail, the zero sequence signal becomes too large in magnitude. Regardless the modulation index value, the modulation signal of at least one of the two remaining phases saturate and nonlinear modulation results. Therefore, the GDPWM approach is superior.

Since the experimental system employs a PEM algorithm, the voltage linearity of GDPWM method practically ends at 0.854 modulation index (calculated from (3.54)). The modulator and drive behavior outside this region (in the overmodulation region), will be discussed in the next chapter in detail and experimental results will be provided.

3.10 Summary

In this chapter, modern carrier based PWM methods were thoroughly reviewed. Reviewing the principles and building correlation between various methods, it has become possible to group the methods, find equivalency between several methods, and furthermore establish a unified approach to study, evaluate, and program all the PWM methods. The well known waveform quality and switching loss function characteristics of the modern PWM methods have been reviewed and the algebraic functions simplified and gathered to form a user-friendly "PWM toolbox." These tools were utilized to illustrate and compare the performance characteristics of various PWM methods. The switching loss and waveform quality comparisons indicate SVPWM at low modulation and

DPWM methods at the high modulation range have superior performance. The tools and graphics aid the modulator selection and PWM inverter design process. The magnitude test is an elegant method for generating the modulation waveforms fast and accurately by digital hardware/software or analog hardware. The analytical methods are also helpful in generating graphics of the microscopic current ripple characteristics and illustrating the performance characteristics and the difference between various modulators. Therefore, they aid visual learning. As a result, the linear modulation region performance analysis provided in this chapter helps the PWM learning and design experience become simple and intuitive. Furthermore, it lays the foundations for the investigation of the overmodulation region modulator behavior.

In this chapter, also the GDPWM method with on-line performance optimization capability has been developed and its characteristics have been analytically and experimentally studied. An algorithm that combines the superior high modulation range performance characteristics of GDPWM and the superior low modulation range performance characteristics of SVPWM method has been developed and implemented. The self-optimization procedure of the algorithm which minimizes the harmonic distortion and reduces the switching losses has been described. The algorithm has a simple structure and it is suitable for DSP or microprocessor based digital implementation. The phase angle ψ of the modulator is on-line controlled in order to optimize the drive performance and reduce the switching losses. The operating characteristics of the GDPWM method and the high performance PWM algorithm have been verified in the

laboratory tests. The losses, harmonic distortion and other characteristics have been both experimentally and theoretically investigated and reported. The transition modulation index value from SVPWM to GDPWM was investigated and an approach to estimate this value has been proposed.

With the linear modulation region performance of all the modulators well defined and illustrated in this chapter, the overmodulation region performance of these modulators remain unknown. Should the PWM method with the highest overmodulation region performance be known, the only remaining task would be to integrate its modulation algorithm to the high performance PWM algorithms discussed in this chapter. However, with the HDF and SLF functions not being valid in the overmodulation region, the overmodulation region performance of the modern PWM methods is difficult to predict. The following chapters investigate the overmodulation region performance of voltage feedforward controlled drives and closed loop current controlled drives.

Throughout this study it has been found the performance of voltage feedforward controlled and closed loop current controlled drives involve different modulator overmodulation performance characteristics. Therefore, in this work voltage feedforward drives and closed loop current controlled drives have been separately investigated and reported. With the voltage feedforward drive performance issues being simpler than the closed loop current controlled drives, the voltage feedforward controlled drive overmodulation issues are investigated first.