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Modified SVPWM Algorithm for Three Level VSI With Synchronized and Symmetrical Waveforms

Abdul Rahiman Beig, *Member, IEEE*, G. Narayanan, *Member, IEEE*, and V. T. Ranganathan, *Senior Member, IEEE*

***Abstract*—The objective of the present work is to improve the output waveform of three level inverters used in high-power applications, where the switching frequency is very low. This is achieved by maintaining the synchronization, half-wave symmetry, quarter-wave symmetry, and three-phase symmetry in the pulsewidth modulation (PWM) waveforms. The principles of achieving synchronization and symmetries in terms of space vectors for three level inverters are presented. A novel synchronized space vector pulsewidth modulation (SVPWM) algorithms is proposed and verified experimentally. The experimental waveforms of the inverter output voltage and motor no load current for different operating conditions of the drive are presented. The performance measure in terms of the weighted total harmonic distortion (*THD*) of the line voltage is computed for the linear modulation region of the drive for the proposed algorithm and compared with that of synchronized SVPWM and synchronized sine-triangle pulsewidth modulation (SPWM) technique. The comparative results show that consideration of synchronization and symmetry results in improved *THD*. Another significant feature of the proposed algorithm is that the symmetry and synchronization leads to self-balancing of the direct current (dc) bus capacitor voltages over every one third cycle of the fundamental.**

***Index Terms*—Harmonic distortion, induction motor drives, pulsewidth modulated inverters, pulsewidth modulation.**

I. Introduction

THREE level inverters have certain advantages over conventional two level inverters [1].

- Three level inverters can synthesize double the voltage levels using the devices of similar voltage rating. Hence, the power handling capacity can be doubled.
- For a given switching frequency, three level voltage can have double the bandwidth.
- Three level inverters have improved total harmonic distortion (*THD*) compared to two level inverters.

Because of these features, three level inverters are finding application especially in medium voltage high-power drives.

In order to reduce the switching losses, the switching frequency (f_{sw}) of the high-power inverters is limited to low values (350 Hz to 1 KHz). Hence, the pulse number (P), defined as the ratio of f_{sw} to the fundamental frequency F_s is low. Under such circumstances, the output voltage of the inverter will be rich in harmonics [2]–[6]. The output voltage must be synchronized with its fundamental component in order to eliminate subharmonics. Like two level sine-triangle pulsewidth modulation (SPWM), in three level SPWM, with P equal to the odd integer multiple of three, the inverter output waveforms will be synchronized with half-wave symmetry (HWS), quarter-wave symmetry (QWS), three phase symmetry (TPS) [3], [4]. The three level space vector pulsewidth modulation (SVPWM) algorithms for high-power applications use this feature to achieve synchronization and waveform symmetry [5]. In this conventional three level SVPWM scheme, P can take only values $3, 9, 15\ldots$ The major drawback of this scheme is that f_{sw} varies over a wide range with F_s in variable speed drives.

In the case of conventional two level inverters, it is shown that the flexibility in selecting the space vectors results in design of SVPWM sequences which generate synchronized output waveforms with HWS, QWS, and TPS for any odd integer values of P [6]. The objective of this paper is to exploit similar features of three level space vectors and design SVPWM sequences for three level inverter resulting in synchronized PWM outputs waveforms with HWS, QWS, and TPS. No such attempt is made in the literature in this direction and for the first time a novel synchronized three level SVPWM algorithm with waveform symmetries is proposed for low-switching frequency applications. Even though three level SVPWM is an active area of research, most of the work is focussed on specific issues related to conventional symmetrical SVPWM algorithm like simplifying the algorithm [7], implementation issues [8]–[11], reducing the switching losses [12], neutral point voltage balancing [13]–[18], or reducing common mode voltage [19].

The computational complexity of three level SVPWM can be reduced to that of two level SVPWM, as shown in [7] and is applied to conventional SVPWM algorithm. In the present work, the simplified method given in [7] is further modified so that computation of synchronized SVPWM sequences and implementation on digital controller using assembly program is simple and modular. In Section II, this modified simple approach to SVPWM is explained.

The design of the three level SVPWM sequences require different approach compared to two level SVPWM techniques as there are additional redundancies in space vectors, zero vector is no longer the common vector for all the regions of space vector space and direct current (dc) bus balancing has to be maintained. The basic principle of the space vector approach to synchronization and symmetry and design of sequences is detailed in Section III. The present work shows that by proper design of SVPWM sequences it is possible to get synchronization and various waveform symmetries for any integer

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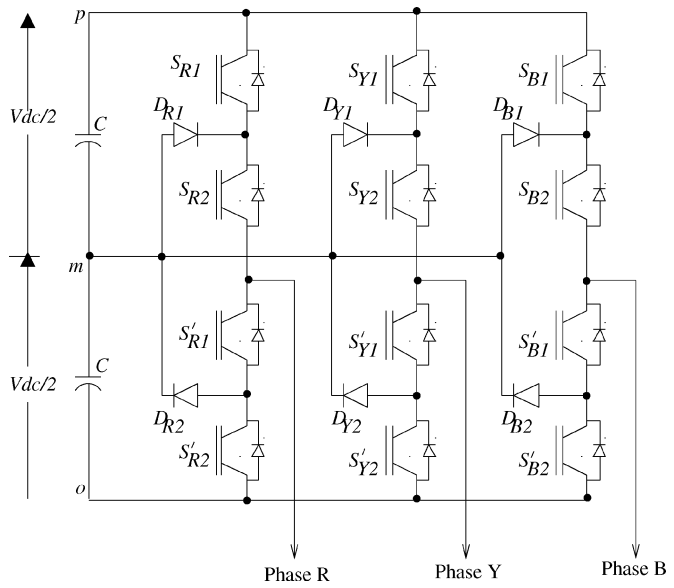

Fig. 1. Three level diode clamp inverter.

values of P. The proposed PWM technique is implemented on TMS320F240 fixed point DSP controller. The proposed PWM technique is verified experimentally on three level diode clamp voltage source inverter fed v/f induction motor drive. The implementation details and typical experimental results are presented in Section IV.

The performance of the proposed technique is studied over the entire linear modulation region of the drive. A comparison in terms of the weighted *THD* of the output line voltage (V_{LWTHD}) for the proposed synchronized SVPWM technique with waveform symmetries and conventional synchronized SVPWM technique shows that consideration of symmetry results in improved *THD*. Similarly, a comparison of V_{LWTHD} of proposed synchronized SVPWM with waveform symmetries and synchronized SPWM technique with waveform symmetries proves the superiority of the present method over synchronized SPWM technique. Also the variation of V_{LWTHD} as a function of P is studied and this result can be used for the optimal design of PWM technique in order to achieve minimum *THD*.

A major requirement of three level PWM sequences is that the dc bus capacitor voltages must be balanced. It is shown that the proposed technique ensures the dc link capacitor voltage balancing over (1/3)*rd* cycle of the fundamental. This is an important result because the proposed method is simple, do not require any additional computation or feed back signal compared to other methods presented in the literature [13]–[18]. The proposed method also results in minimum common mode voltage.

Compared to the other three level SVPWM algortihms, the present work has a unique feature that it addresses all the major issues related to the three level PWM techniques such as computational complexity, synchronization, *THD*, dc bus voltage balancing, and common mode voltage. Hence, the proposed SVPWM method will be suitable for high-power applications as it eliminates subharmonics by maintaining synchronization, improves *THD* through various waveform symmetries, results in balanced dc bus voltage, and low common mode voltage.

TABLE I
DIODE CLAMP INVERTER: SWITCH STATUS AND DEFINITION OF STATE FOR POLE R

Switch status	State	Pole voltage
$S_{R1}=ON, S_{R2}=ON,$ $S'_{R1}=OFF, S'_{R2}=OFF,$ $D_{R1}=OFF, D_{R2}=OFF$	$+1$	$V_{Rm}=\frac{V_{dc}}{2}$
$S_{R1}=OFF, S_{R2}=ON,$ $S'_{R1}=ON, S'_{R2}=OFF,$ D_{R1} or D_{R2} will conduct depending on the polarity of the load current	0	$V_{Rm}=0V$
$S_{R1}=OFF, S_{R2}=OFF,$ $S'_{R1}=ON, S'_{R2}=ON,$ $D_{R1}=OFF, D_{R2}=OFF$	-1	$V_{Rm}=-\frac{V_{dc}}{2}$

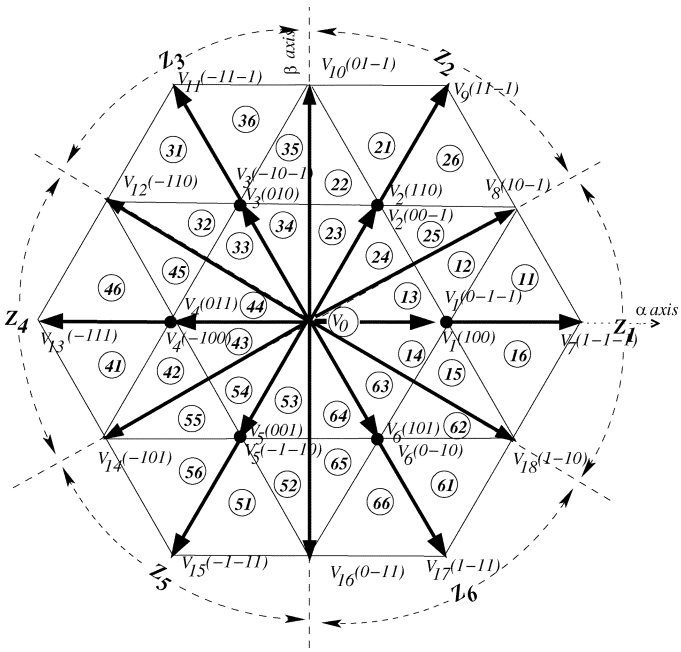

Fig. 2. Space vectors of three level inverter with sector and subsector definition.

II. SIMPLIFIED APPROACH TO SVPWM

Fig. 1 shows the circuit diagram of a three level diode clamp inverter. The states are defined in Table I. The space vectors associated with the three level inverters on $\alpha-\beta$ plane are shown in Fig. 2. In the space vector approach to PWM, the reference vector is sampled at regular interval T_s. The sampled reference vector $\overline{V}_r$ is approximated by time averaging the nearest three vectors, $\overline{V}_x$, $\overline{V}_y$, and $\overline{V}_z$ according to (1) and (2)

$$\overline{V}_r T_s = \overline{V}_x T_x + \overline{V}_y T_y + \overline{V}_z T_z \tag{1}$$

$$T_s = T_x + T_y + T_z \tag{2}$$

where T_x, T_y, and T_z are the dwell times of $\overline{V}_x$, $\overline{V}_y$, and $\overline{V}_z$, respectively.

Unlike two level inverters, the zero vector is no longer common for all the regions. So solution to (1) and (2) involves solving three simultaneous equations. In order to simplify

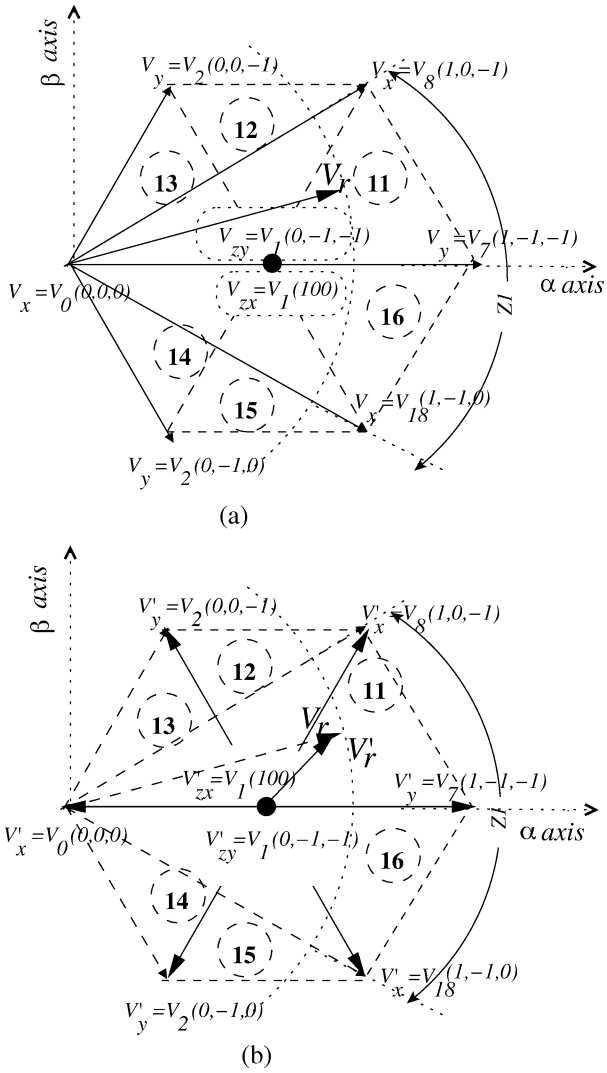

Fig. 3. (a) Vectors of sector 1. (b) Mapping of vectors of sector 1 to fictitious vectors.

the above equations, a simple approach based on the method given in [7] is adopted, in which the symmetry of the space vectors is exploited. The space vector plane is divided in to six sectors, each of 60°, as shown in Fig. 2. Each sector Z, where $Z = 1, 2, 3, \ldots, 6$, is associated with one pivot vector $\overline{V}_z$ and six other vectors. The pivot vector $\overline{V}_1$ and other six vectors of sector 1 are redrawn in Fig. 3(a). The vectors of the other sectors are phase displaced by $\pi/3$ radians. All the six sectors exhibit symmetry. All the vectors associated with the given sector Z, can be mapped to a set of seven fictitious vectors with $\overline{V}_1$ as the center as defined by (3). This is illustrated in Fig. 3(b)

$$\begin{aligned}
\overline{V}'_r &= \overline{V}_r e^{j(Z-1)\pi/3} - \overline{V}_1 \\
\overline{V}'_x &= \overline{V}_x e^{j(Z-1)\pi/3} - \overline{V}_1 \\
\overline{V}'_y &= \overline{V}_y e^{j(Z-1)\pi/3} - \overline{V}_1 \\
\overline{V}'_z &= \overline{V}_z e^{j(Z-1)\pi/3} - \overline{V}_1
\end{aligned} \tag{3}$$

The fictitious vectors are similar to those of two level inverters.

TABLE II
PIVOT VECTORS AND INVERTER STATES

Sector Z	Pivot Vector $\overline{V}_z$	$\overline{V}_{zx}$	$\overline{V}_{zy}$
1	$\overline{V}_1$	100	0-1-1
2	$\overline{V}_2$	00-1	110
3	$\overline{V}_3$	010	-10-1
4	$\overline{V}_4$	-100	011
5	$\overline{V}_5$	001	-1-10
6	$\overline{V}_6$	0-10	101

The vector $\overline{V}'_z$ forms the origin and its magnitude is always zero and for a given sector this vector is similar to the zero vector of two level inverters. The three nearest vectors can be identified as $\overline{V}'_z$, $\overline{V}'_x$, and $\overline{V}'_y$ as shown in Fig. 3. Now the solution to (1) is similar to that of two level inverters, as in (4)

$$V'_{r\alpha} T_s = V'_{x\alpha} T_x + V'_{y\alpha} T_y \tag{4a}$$
$$V'_{r\beta} T_s = V'_{x\beta} T_x + V'_{y\beta} T_y \tag{4b}$$
$$T_z = T_s - T_x - T_y. \tag{4c}$$

Thus, the computational complexity of three level inverters is reduced to that of two level inverters. Implementation of above method is simple as it requires only the computation of $\overline{V}'_r$ and is explained in Section IV. With the sector definition given above, all the sectors are symmetric and a modular approach can be used in implementation.

Conventional SVPWM sequences will have switching sequences $\overline{V}_{zx} \Longleftrightarrow \overline{V}_x \Longleftrightarrow \overline{V}_y \Longleftrightarrow \overline{V}_{zy}$. The T_z interval is equally derived between pivot vectors $\overline{V}_{zx}$ and $\overline{V}_{zy}$. The pivot vectors $\overline{V}_{zx}$ and $\overline{V}_{zy}$ are defined in Table II. State V_{zx} is defined as the state of V_z obtained by switching only one phase of the inverter from state V_x. Similarly state V_{zy} is defined as the state of V_z obtained by switching only one phase of the inverter from state V_y. These sequences ensure that in each sampling interval, each of the phases is switched at least once. Also these sequences satisfy following two conditions for minimum switching frequency.

- Condition 1: Only one switch is switched during state transition. That is transition from state 1 to state -1 and vice versa is not allowed.
- Condition 2: The final state of present sample will be the initial state of next sample.

In the next section, these SVPWM sequences are modified to achieve synchronized output waveforms with HWS and TPS.

In the present method, the sector decides the angle through which the reference vector $\overline{V}_r$ is to be rotated to get the fictitious reference vector $\overline{V}'_r$ whereas in the simplified method given in [7], the offset values to be subtracted from $\overline{V}_r$ to obtain $\overline{V}'_r$ has to be stored in the form of lookup table or programmed accordingly. This slight modification helps in developing subroutines to generate switching sequence and helps in implementing in DSP assembly program which is clear from the implementation details given in Section IV.

III. Space Vector Approach to Synchronization and Symmetry

In this section, the principles of obtaining synchronization and various symmetry in terms of space vectors is derived.

A. Need for Synchronization and Symmetry

- Synchronization: At low switching frequencies, it is necessary to maintain perfect synchronization of inverter output voltage with respect to its own fundamental to avoid subharmonics. This is possible if and only if the PWM output pole voltage waveform satisfies the condition given below

$$v_{Rm}(\theta \pm 2\pi) = v_{Rm}(\theta)$$
$$v_{Ym}(\theta \pm 2\pi) = v_{Ym}(\theta)$$
$$v_{Bm}(\theta \pm 2\pi) = v_{Bm}(\theta)$$

  where θ is any arbitrary angle measured from the reference axis. This can be achieved if the same inverter state is switched at θ and $(\theta \pm 2\pi)$ and the dwell time of these states must be equal. This demands the $\overline{V}_r$ to be sampled at θ and $(\theta \pm 2\pi)$, which is possible only if there are integral number of samples per cycle of the fundamental.
- TPS: At low switching frequency, lower order harmonics are dominant. The PWM sequences should be designed to eliminate some of these harmonics. The three-phase symmetry will ensure that all the harmonics and the fundamental of all the three phases will be perfectly balanced. So the triplen harmonics will be cancelled from the line voltage. For a phase sequence of *R-Y-B*, the TPS can be achieved if the inverter output voltages of three phases satisfy the following condition:

$$v_{Bm}\left(\theta - \frac{2\pi}{3}\right) = v_{Ym}\left(\theta + \frac{2\pi}{3}\right) = v_{Rm}(\theta).$$

  The above condition can be met if the switch position of pole R at θ, the switch position of pole Y at $(\theta + 2\pi/3)$, and the switch position of pole B at $(\theta - 2\pi/3)$ are same. For example, if the inverter state at θ is (101), then at $(\theta + 2\pi/3)$ the state (110) must be used and at $(\theta - 2\pi/3)$ state (011) must be used to achieve TPS and dwell time of these states must be equal.
- HWS: The half wave symmetry will ensure elimination of even harmonics from the output voltage. In order to achieve HWS, the pole voltage at θ and $(\pi + \theta)$ should have opposite polarity that is

$$v_{Rm}(\theta \pm \pi) = -v_{Rm}(\theta)$$
$$v_{Ym}(\theta \pm \pi) = -v_{Ym}(\theta)$$
$$v_{Bm}(\theta \pm \pi) = -v_{Bm}(\theta).$$

  In order to achieve this, the switch position of a given phase at θ and $(\theta \pm \pi)$ must be opposite. If at θ the switch position of a given phase is "1," then at $(\theta \pm \pi)$ it must be "-1" and vice versa. But if the switch position of a given phase is "0" at θ, then the switch position of the same phase must be "0" at $(\theta \pm \pi)$.

The conditions of waveform symmetry for a given sample k are summarized in Table III. The necessary and sufficient conditions in terms of the inverter states to achieve synchronization and symmetry at the line and pole voltages are given in Table IV. In Tables III and IV, the states with a prime ($'$) indicate the complementary states. Complementary state of 1 is state -1 and vice versa and complementary state of 0 is state 0 itself. The conditions of HWS and TPS given in column 2 and 3 of Table IV, relate the inverter states over an interval of 60°. So the inverter states of each sector are related by (5)

TABLE III
Conditions of Synchronization, HWS, and TPS in Terms of Pole Voltages

	Synchronization	HWS	TPS	TPS
Pole voltage at θ	Pole voltage at $\theta \pm 2\pi$	Pole voltage at $\theta \pm \pi$	Pole voltage at $\theta + 2\pi/3$	Pole voltage at $\theta - 2\pi/3$
v_{Rm}	v_{Rm}	$-v_{Rm}$	v_{Bm}	v_{Ym}
v_{Ym}	v_{Ym}	$-v_{Ym}$	v_{Rm}	v_{Bm}
v_{Bm}	v_{Bm}	$-v_{Bm}$	v_{Ym}	v_{Rm}

TABLE IV
Conditions of Synchronization, HWS, and TPS in Terms of Inverter States

	Synchronization	HWS	TPS	TPS
Inverter state at θ	Inverter state at $\theta \pm 2\pi$	Inverter state at $\theta \pm \pi$	Inverter state at $\theta + 2\pi/3$	Inverter state at $\theta - 2\pi/3$
S_R	S_R	S_R'	S_B	S_Y
S_Y	S_Y	S_Y'	S_R	S_B
S_B	S_B	S_B'	S_Y	S_R

$$S_R\left(\theta + \frac{\pi}{3}\right) = S_Y'(\theta)$$
$$S_Y\left(\theta + \frac{\pi}{3}\right) = S_B'(\theta)$$
$$S_B\left(\theta + \frac{\pi}{3}\right) = S_R'(\theta). \quad (5)$$

So one of the requirements of synchronization and symmetry is that, there should be integral number of samples (N) per sector and these samples should be placed at identical positions in each sector. Under these conditions, the sampled reference voltages satisfy the conditions given in Table IV. Hence, for a given sample n, where $n = 1, 2, 3 \ldots N$, the dwell times T_x, T_y and T_z of nearest three vectors will be equal in all the sectors.

B. Number of Samples per Sector, Pulse Number and Switching Sequence

1) Odd Values of N: For odd values of N, there will be $(N-1)$ samples within the sector placed at an equal distance of $(\pi/3N)$ and one sample on the sector boundary. Depending on how the change of $\overline{V}_z$ is accomplished, there are two possibilities.

- TYPE 1: All the samples except the sample on sector boundary will have sequences $\overline{V}_{zx} \iff \overline{V}_x \iff \overline{V}_y \iff \overline{V}_{zy}$.
  The sample $n = N$ which falls on the sector boundary will have the sequence,
  $\overline{V}_{zx} \longrightarrow \overline{V}_x \longrightarrow \overline{V}_y$. The last state $\overline{V}_y$, of the Nth sample of the present sector will be the starting state $\overline{V}_{zx}$, in the first sample of the next sector. So the sample $n = 1$

will have the sequence, $\overline{V}_{zx} \longrightarrow \overline{V}_x \longrightarrow \overline{V}_y \longrightarrow \overline{V}_{zy}$. There will not be any switching from one sample to another sample during sector change over. The pulse number is given by $P = (3/2)(N-1)$.

- TYPE 2: All the samples will have sequences $\overline{V}_{zx} \Longleftrightarrow \overline{V}_x \Longleftrightarrow \overline{V}_y \Longleftrightarrow \overline{V}_{zy}$.
  The sequence of the last sample in a sector will always end with state $\overline{V}_{zy}$ and the first sample in a sector will start with state $\overline{V}_{zx}$. This type of sequences will cause an additional switching during sector change over. The pulse number is given by $P = (3/2)(N+1)$.

2) Even Values of N: For even values of N, all the samples will be within the sector placed at an equal distance of $(\pi/3N)$. All the samples except $n = 1$ and $n = N$ will have sequences $\overline{V}_{zx} \Longleftrightarrow \overline{V}_x \Longleftrightarrow \overline{V}_y \Longleftrightarrow \overline{V}_{zy}$.

The sample $n = 1$ and $n = N$ will have the sequences $\overline{V}_{zx} \longrightarrow \overline{V}_x \longrightarrow \overline{V}_y \longrightarrow \overline{V}_x$ and $\overline{V}_x \longrightarrow \overline{V}_y \longrightarrow \overline{V}_x \longrightarrow \overline{V}_{zx}$.

In these samples, one of the phases will be switched twice and another phase will be clamped. The pulse number will be $P = 3N/2$. Combining all the three cases, it can be seen that synchronization, HWS and TPS can be achieved for any integral value of P.

It can be seen that these sequences also exhibit the conditions of QWS given in (6) in addition to the conditions of synchronization, HWS and TPS, even though the sequences are designed without considering conditions of QWS

$$\begin{aligned} S_R(\theta_R + \theta) &= S_R(\theta_R - \theta) \\ S_Y(\theta_Y + \theta) &= S_Y(\theta_Y - \theta) \\ S_B(\theta_B + \theta) &= S_B(\theta_B - \theta) \end{aligned} \tag{6}$$

where θ_R, θ_Y, and θ_B are the instants at which the R, Y and B phase fundamental waveforms have their positive or negative peaks. So the output voltages will also have QWS.

IV. Experimental Implementation and Results

The conventional space vector modulation algorithm explained in Section II can be modified to incorporate the conditions of synchronization and symmetry. So the modified algorithm is as follows:

1) Identification of sector Z: From the normalized values of $V_{r\alpha}$ and $V_{r\beta}$, the sector Z is identified as follows.

If $V_{r\alpha} \geq 0$ and $V_{r\beta} \geq 0$, then, if $V_{r\beta} > V_{r\alpha} tan(\pi/6)$, then $Z = 2$, else, $Z = 1$.

If $V_{r\alpha} \geq 0$ and $V_{r\beta} < 0$, then, if $V_{r\beta} > V_{r\alpha} tan(\pi/6)$, then $Z = 6$, else, $Z = 1$.

If $V_{r\alpha} < 0$ and $V_{r\beta} \geq 0$, then, if $V_{r\beta} > |V_{r\alpha}| tan(\pi/6)$, then $Z = 3$, else, $Z = 4$.

If $V_{r\alpha} < 0$ and $V_{r\beta} < 0$, then, if $|V_{r\beta}| > |V_{r\alpha}| tan(\pi/6)$, then $Z = 5$, else, $Z = 4$.

2) Identification of subsectors: Map V_r to fictitious vector V_r' using the expression $\overline{V}_r' = \overline{V}_r e^{j(Z-1)\pi/3} - \overline{V}_1$. From the α and β components of V_r', determine the sub-sector. Determination of subsector is similar to identifying sectors as explained in step 1 above except that $V_{r\alpha}$ and $V_{r\beta}$ are replace by $V_{r\alpha}'$ and $V_{r\beta}'$, respectively.

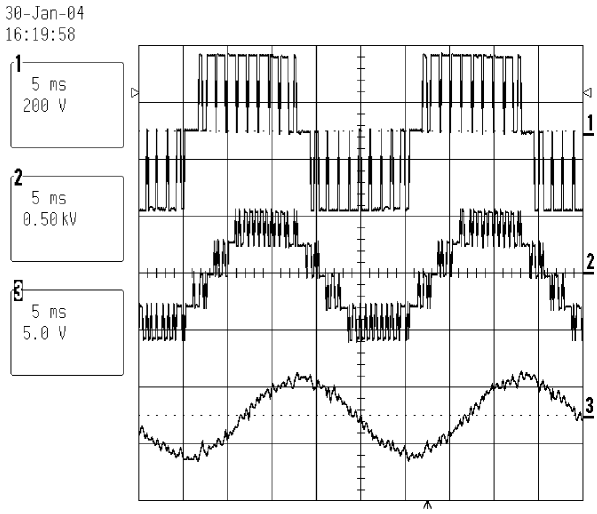

Fig. 4. Experimental waveforms: ch1: v_{Rm} (Scale:200 V/div) ch2: v_{RY} (Scale:500 V/div) ch3: i_R (Scale:11.1 A/div) for $F_s = 40$ Hz, $N = 7$, $P = 10$.

3) Computation of switching intervals T_z, T_x, and T_y: From sector , subsector, $V_{r\alpha}'$, and $V_{r\beta}'$, the T_z, T_x and T_y can be computed using (4).

4) Identification of switching sequence: The F_s and f_{sw} will decide the value of N. A sector and subsector combination and N will uniquely define the switching sequence and this can be programmed in the form of subroutines.

This can be implemented in another way also. The switching sequences of all the six subsectors of sector 1 are stored in the form of a look up table. Using this the switching sequence of other sectors are computed using (5).

The above algorithm is implemented in TMS320F240 based controller. The event manager is programmed in compare mode. Depending on the value of sector and subsector, the corresponding subroutine is executed and the counters are loaded with proper values. Thus, the switching pulses are generated. The exact sampling time interval is maintained using end of period interrupt of event manager module. The event manager module can generate six independent signals. The complementary signals and the dead time between these signals are generated in the external circuit. This SVPWM algorithm is applied to open loop v/f induction motor drive. The experimental drive consists of a 400 V, 10 HP, three phase, 50 Hz, induction motor powered from a 30 KVA, insulated gate bipolar transistor (IGBT) based three phase three level diode clamp inverter. The dc bus voltage is set at 510 V. The typical experiential results for $F_s = 40$ Hz is shown in Fig. 4. The harmonic spectra of V_{Rm}, V_{RY} and i_R, computed from the experimental data is given in Fig. 5.

It can be seen from harmonic spectra of experimental waveforms (Fig. 5) that, the output voltage has no sub harmonics and even harmonics. Hence, the modified SVPWM guaranties synchronization and half-wave symmetry. The harmonic spectra shows that the triplen harmonics which are present in phase

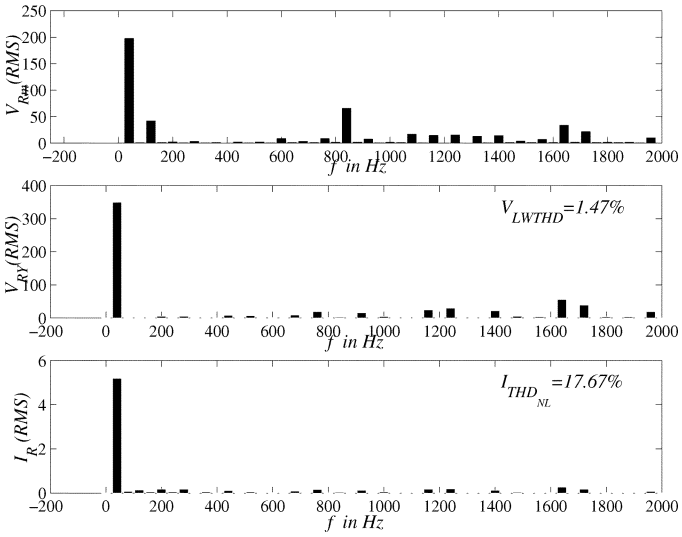

Fig. 5. Harmonic spectrum of v_{Rm}, v_{RY}, and i_R at $F_s = 40$ Hz, $N = 7$, $P = 10$.

voltage are absent from line voltage and motor current. This proves that the SVPWM preserves three phase symmetry.

V. Performance Analysis

The performance of the proposed synchronized SVPWM sequences is studied in terms of the *THD* of output waveforms, effect of PWM on dc bus midpoint voltage variation and common mode voltage. Some of these results are presented in this section.

A. THD

In high-power drives, the *THD* of the motor no load current, $I_{THD_{NL}}$, which is a function of voltage spectra and motor parameters is a suitable performance index at low switching frequencies [2]. $I_{\mathrm{THD_{NL}}}$ is defined in (7)

$$I_{THD_{NL}} = \frac{\sqrt{\sum I_n^2}}{I_{1_{NL}}}, n \neq 1 \tag{7}$$

where $I_{1_{NL}}$ is the RMS value of the fundamental component of the motor no load current.

Measuring $I_{THD_{NL}}$ experimentally is a difficult process. So another quantity which is proportional to $I_{THD_{NL}}$ and easy to compute, is the weighted *THD* of the line voltage (V_{LWTHD}) [6]. V_{LWTHD} is defined in (8)

$$V_{\mathrm{LWTHD}} = \frac{\sqrt{\sum \left(\frac{V_n}{n}\right)^2}}{V_1}, n \neq 1, \tag{8}$$

The V_{LWTHD} gives the measure of $I_{\mathrm{THD_{NL}}}$ as these are related as follows:

$$V_{\mathrm{LWTHD}} = \frac{L_l}{L_o} I_{THD_{NL}} \tag{9}$$

where L_o is the magnetizing inductance and L_l is the total leakage inductance. Therefore, V_{LWTHD} can be used as the measure of $I_{THD_{NL}}$.

The drive is run at no load at different values of F_s in the linear modulation range (i.e., $M_i < 0.886$, where modulation index, M_i is defined as the ratio between the magnitude of reference vector to the dc bus voltage V_{dc}). In each case, the motor current waveform is stored using high bandwidth digital storage scope (LeCroy make, 200 MHz, 40 000 points per channel). From this data, exactly one cycle data of the no load current is taken. The frequency components are computed using MATLAB-FFT function. From the harmonic components, the $I_{THD_{NL}}$ of motor no load current is computed using (7) and its variation is shown in Fig. 6.

Fig. 7 give the plot of V_{LWTHD} of line voltage with respect to M_i for different switching frequencies. This result can be used for the optimal selection of switching frequency to minimize *THD*. The graph with * mark shows the variation of V_{LWTHD} for a given switching frequency. In this case, the f_{sw} is varied from 380 to 420 Hz.

Fig. 8 shows the comparison of V_{LWTHD} of the proposed synchronized SVPWM with HWS and TPS and conventional synchronized SVPWM without HWS and TPS. In both the cases, synchronization is maintained. The proposed synchronized SVPWM with symmetry will result in better *THD*.

Fig. 9 shows the comparison of V_{LWTHD} of proposed synchronized SVPWM and synchronized SPWM. In both the cases, P is selected such that synchronization , HWS and TPS is maintained. In the case of SPWM, in order to maintain synchronization, HWS and TPS, P should be odd integral multiple of three. These results show that the proposed synchronized SVPWM sequences result in improved *THD*. Since the proposed SVPWM guaranties synchronization and symmetry for all integer values of P, the overall variation of switching frequency throughout the linear range of modulation is low compared to that of synchronized SPWM.

B. Self Balancing of DC Bus Capacitor Voltage

In symmetrical SVPWM, in every sample the voltage imbalance during the interval t_{zx} is cancelled by the voltage imbalance in interval t_{zy}. In addition to this, because of the synchronization and symmetry considerations, the timing intervals of a given sample n will be equal in all the sectors. Hence, it can be shown that for a given sample n, the variation of dc bus midpoint voltage ΔV_m in a sector is equal but opposite to ΔV_m in next sector.

As an example for a balanced three phase load such as three phase induction motor load, with phase sequence R-Y-B, power factor of ϕ and dc bus capacitor C, the dc bus mid point voltage imbalance at interval 1 of sample 1 in sector 1, is given by

$$\begin{aligned}\Delta V_{m1} &= \frac{1}{C}\int_{\pi/3}^{(\pi/3)+\theta_{11}} i_{a11}\, d\theta \\ &= \frac{I}{C}\left[2.\cos\left(\frac{\theta_{11}}{2}\right).\cos\left(\frac{\pi}{3} \pm \phi + \frac{\theta_{11}}{2}\right)\right]\end{aligned}$$

where I is the peak value of the load current, θ_{11} is the dwell time of the interval 1 of sample 1 and i_{a11} is the dc bus midpoint current at interval 1 of sample 1 of sector 1.

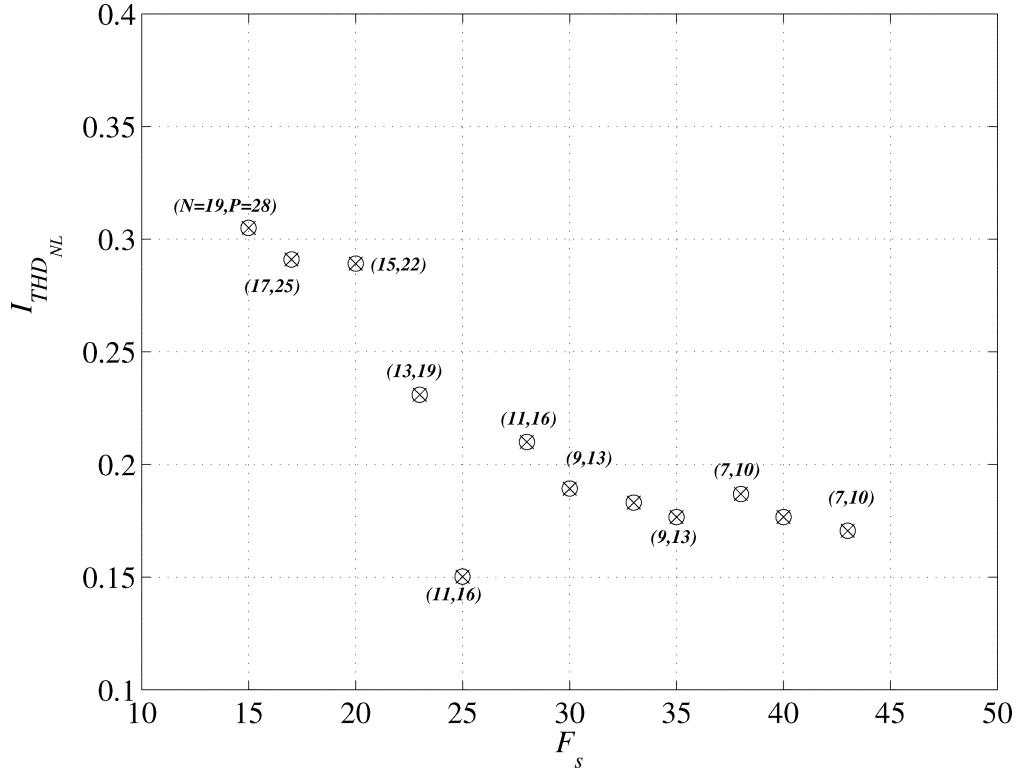

Fig. 6. Experimental results: $I_{THD_{NL}}$ v/s F_s.

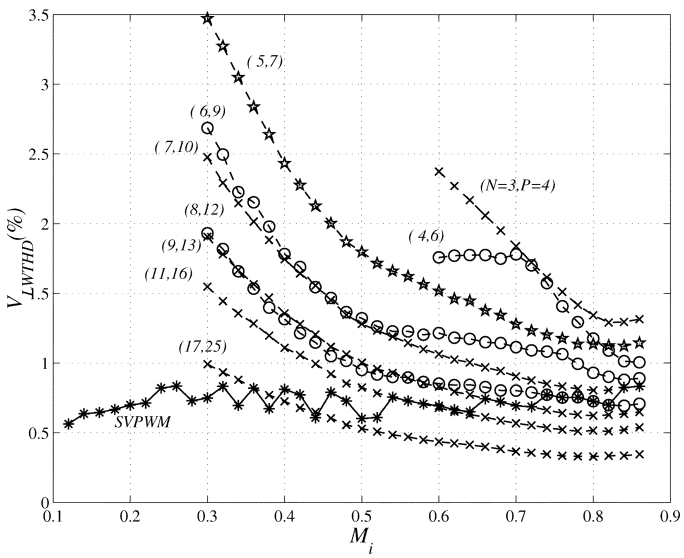

Fig. 7. $V_{\mathrm{LWTHD}}(\%)$ v/s M_i plot.

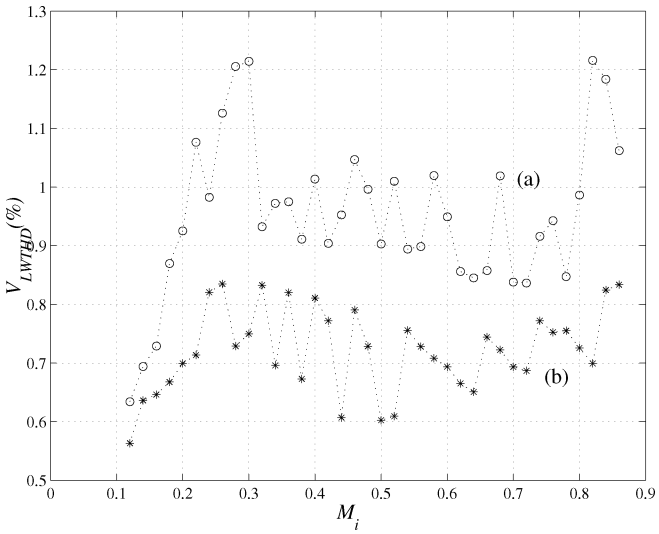

Fig. 8. $V_{\mathrm{LWTHD}}(\%)$ v/s M_i plot. (a) SVPWM (synchronized but no symmetry). (b) SVPWM (synchronized with HWS and TPS).

Similarly dc mid point voltage imbalance at interval 1 of sample 1 in sector 2, is given by

$$\Delta V_{m2} = \frac{1}{C}\int_{2\pi/3}^{(2\pi/3)+\theta_{11}} i_{c_{21}}\, d\theta = \frac{I}{C}\left[-2.\cos\left(\frac{\theta_{11}}{2}\right).\cos\left(\frac{\pi}{3}\pm\phi+\frac{\theta_{11}}{2}\right)\right]$$

where i_{c21} is the dc bus midpoint current at interval 1 of sample 1 of sector 2 From above

$$\Delta V_{m1} = -\Delta V_{m2}.$$

This is true for all values of n.

The dc bus capacitor voltage imbalance in one sector will be equal and opposite to that in next sector. Hence, because of symmetry and synchronized approach, the dc bus capacitor voltages are balanced over every $2\pi/3$ radians. This is illustrated by the

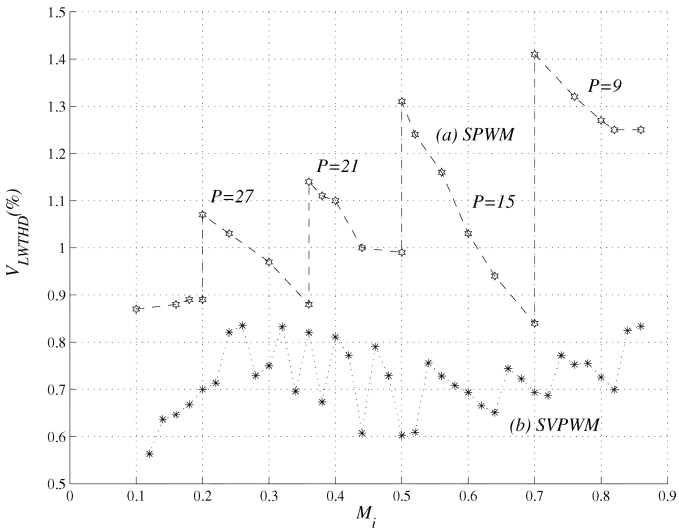

Fig. 9. $V_{\mathrm{LWTHD}}(\%)$ v/s M_i plot. (a) SPWM. (b) SVPWM.

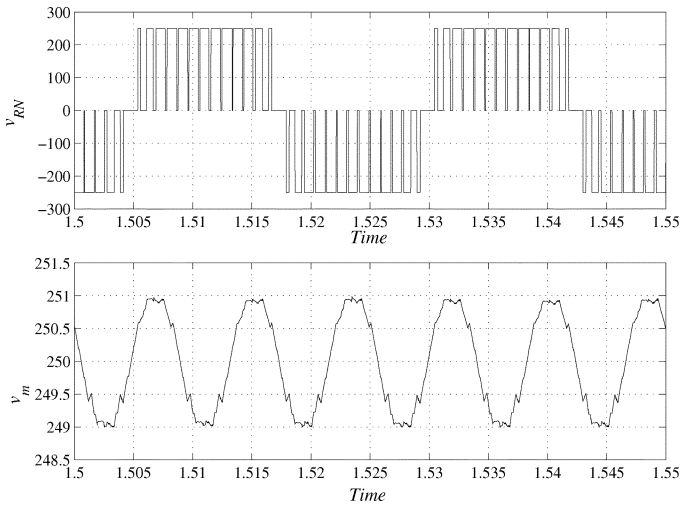

Fig. 10. Simulation results: v_{Rm} and dc bus midpoint voltage v_m at no load, $F_s = 40$ Hz, $N = 7$, $P = 10$, $V_{dc} = 500$ V.

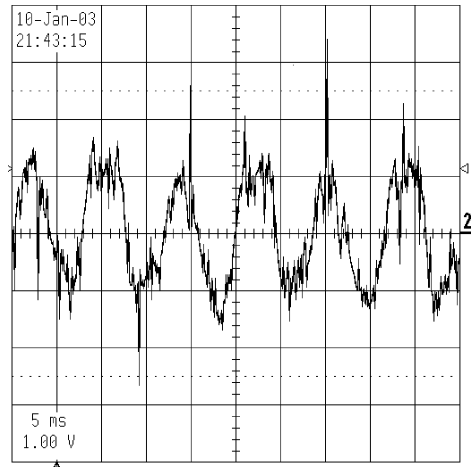

Fig. 11. Experimental waveforms:ΔV_m at no load. (Scale: 1 V/div), $F_s = 40$ Hz, $N = 7$, $P = 10$, $V_{dc} = 510$ V.

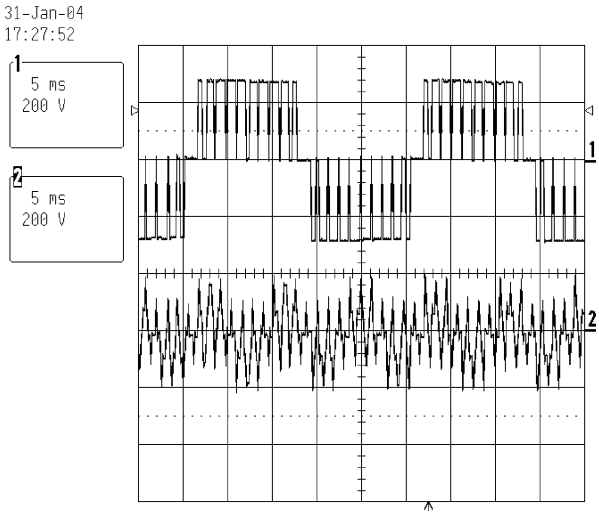

Fig. 12. v_{nm} at $F_s = 40$ Hz. Ch1: v_{Rm} (Scale: 200 V/div), Ch2: v_{nm} (Scale: 200 V/div).

simulation result given in Fig. 10 and verified experimentally, as shown in Fig. 11. This is an important result. Imbalance in dc bus capacitor voltages will result in loss of HWS, thereby even harmonics in motor, even if the sequences are designed to have HWS [13]. Perfect balancing of dc bus capacitor voltages helps in preserving HWS and thus even harmonics in the motor are eliminated. Compare to the other methods [13]–[18], the proposed SVPWM algorithm is simple, does not require any additional feedback signal as in [13] and [14] or0 additional computation as in [16]–[18], and neutral point voltage balance is built in to the algorithm.

C. Common Mode Voltage

The proposed SVPWM techniques make use of only *V*0(000) state; therefore, the maximum value of the voltage between dc bus midpoint (m) and motor neutral point (n) (v_{nm}), which contributes for the common mode voltage is limited to $(1/3)V_{dc}$. Also the change in v_{nm} is limited to $(1/6)V_{dc}$. The experimental waveforms of the variation of common mode voltage at $F_s = 40$ Hz is given in Fig. 12.

VI. Conclusion

The theory of the space vector based synchronized PWM method with HWS and TPS is explained. The experimental results are presented. The proposed algorithm is simple to implement on digital controllers and does not add to any computational complexity. It is shown that the proposed PWM technique will result in balanced dc link capacitor voltages. The performance results show that the V_{WTHD} of the proposed method is better compared to that of synchronized SPWM technique and synchronized SVPWM technique without symmetries. The experimental waveforms show HWS and TPS for any integer value of pulse number. The absence of triplen harmonics from the line voltage shows that the inverter output voltages have three-phase symmetry. Even though the focus is on low switching

frequency applications, the proposed technique can be used for high switching frequency applications also.

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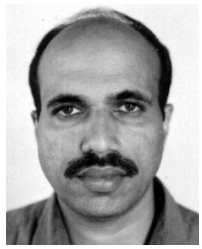

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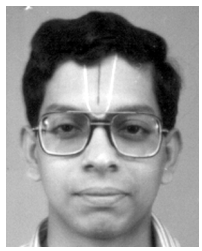

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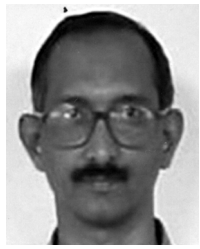

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