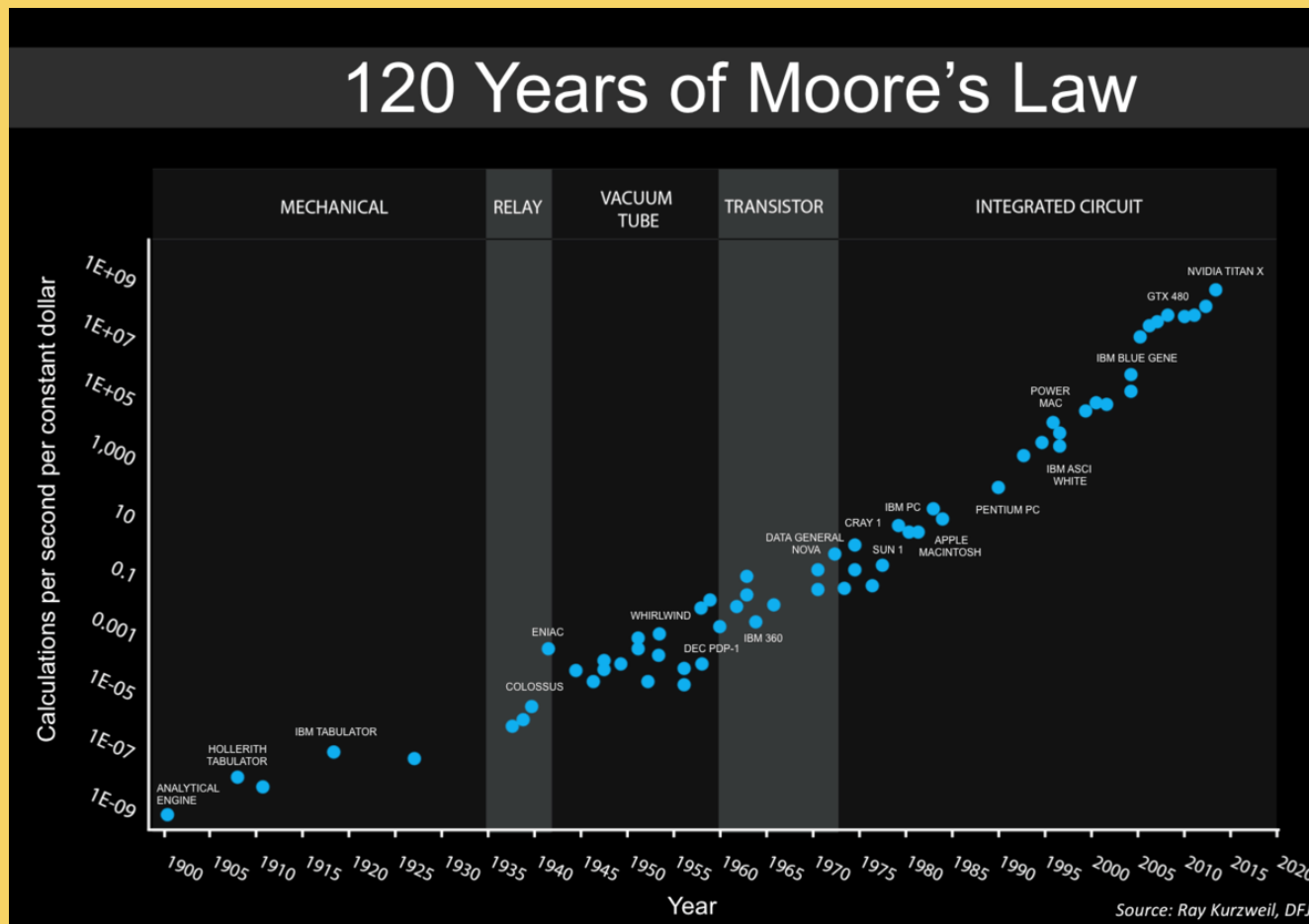


Problem Set 2 is due  
This Friday, Jan 31 (10pm)



Graph by Steve Jurvetson, extending a prior graph of Ray Kurzweil.

## Class 6: *Finite Computation*

University of Virginia  
cs3120: DMT2  
Wei-Kai Lin

# Recap: Boolean logical 'gates'

– OR(a, b): outputs 1 iff a=1 **or** b=1

– AND(a, b): outputs 1 iff a=1 **and** b=1

– NOT(b): outputs 1 iff b=0



Output 0  
otherwise

# Median using And/Or/Not

- Still a “math”-ish def/algorithm for 3-bit MED:

```
def MED(X[0],X[1],X[2]):  
    firstpair = AND(X[0],X[1])  
    secondpair = AND(X[1],X[2])  
    thirdpair = AND(X[0],X[2])  
    temp = OR(secondpair,thirdpair)  
    return OR(firstpair,temp)
```

# A formal programming language

- **AON Straightline** programs

- Python-like language
- Define “\_functions\_” that take Boolean inputs
- Use AND/OR/NOT within
- Assign results of AND/OR/NOT to variables
- The result of variables can be used later as inputs
- Return some of the obtained result(s) as output

$c = \text{AND}(a, b)$   
 $s = \text{OR}(a, b)$   
 $\textcircled{a} = \text{NOT}(a)$

# (PS2) More things to program

- NAND

a	b	NAND(a, b)
0	0	1
0	1	1
1	0	1
1	1	0

$c = \text{AND}(a, b)$   
 $\text{NOT}(c)$

- XOR

truth  
table

a	b	XOR(a, b)
0	0	0
0	1	1
1	0	1
1	1	0

$\text{OR}(\text{AND}(\text{NOT}(a), b), \text{AND}(a, \text{NOT}(b)))$

# More things to program

- 1-bit addition (mod 2)

~~ADD~~  
AND

$XOR(a, b)$

a	b	carry	ADD(a, b)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

- 1-bit addition with carry

$AND(a, b)$

# NAND Straightline Programs

- Like AON straightline programs

- Difference: we can only use NAND

Make ~~AND~~ <sup>using</sup> ~~NAND~~   
 OR   
 NOT   
  $\text{NAND}(a, a) = \text{NOT}(a)$

$\text{AND}(a, b)$    
  $\text{NOT}(\text{NAND}(a, b))$    
  $\text{NAND}(a, \text{NAND}(a, a))$

# NAND Straightline = AON Straightline

- What does it even mean? How to prove it?



# Equivalence of Computing Models?

- To show model 1 is "equivalent" to model 2
  - <sup>AON</sup> Show any algorithms implemented with model 1 can be converted to an equivalent algorithm written in model 2
  - <sup>NAND</sup> Show any algorithms implemented with model 2 can be converted to an equivalent algorithm written in model 1

# NAND Straightline $\Rightarrow$ AON Straightline

**Converting NAND to AON**

# NAND Straightline $\Leftarrow$ AON Straightline

**Converting AON to NAND**

# NAND Straightline = AON Straightline

## AON to NAND

$x = \text{NAND}(a, b)$

Becomes

$\text{temp} = \text{AND}(a, b)$

$x = \text{NOT}(\text{temp})$

$1(a) =$   
 $\text{NAND}(\text{NAND}(a, a), a)$

## NAND to AON

$x = \text{NOT}(a)$

Becomes

$x = \text{NAND}(a, a)$   
 $\text{NAND}(a, 1)$

$x = \text{AND}(a, b)$

Becomes

$\text{temp} = \text{NAND}(a, b)$

$x = \text{NAND}(\text{temp}, \text{temp})$

~~AON~~  
 $\text{NAND}, 1$

$x = \text{OR}(a, b)$

Becomes

$t1 = \text{NAND}(a, a)$

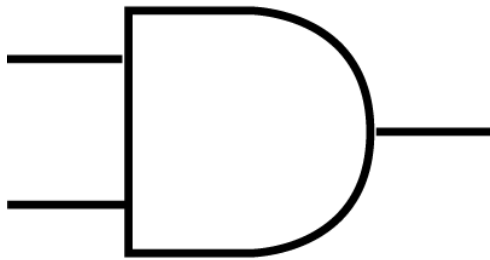
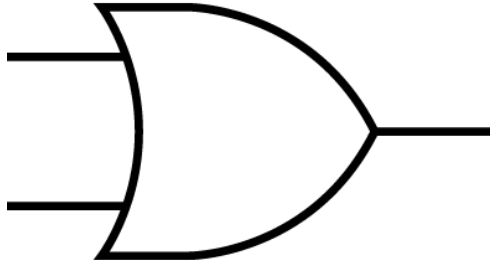
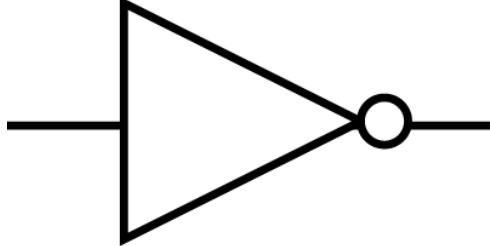
$t2 = \text{NAND}(b, b)$

$x = \text{NAND}(t1, t2)$

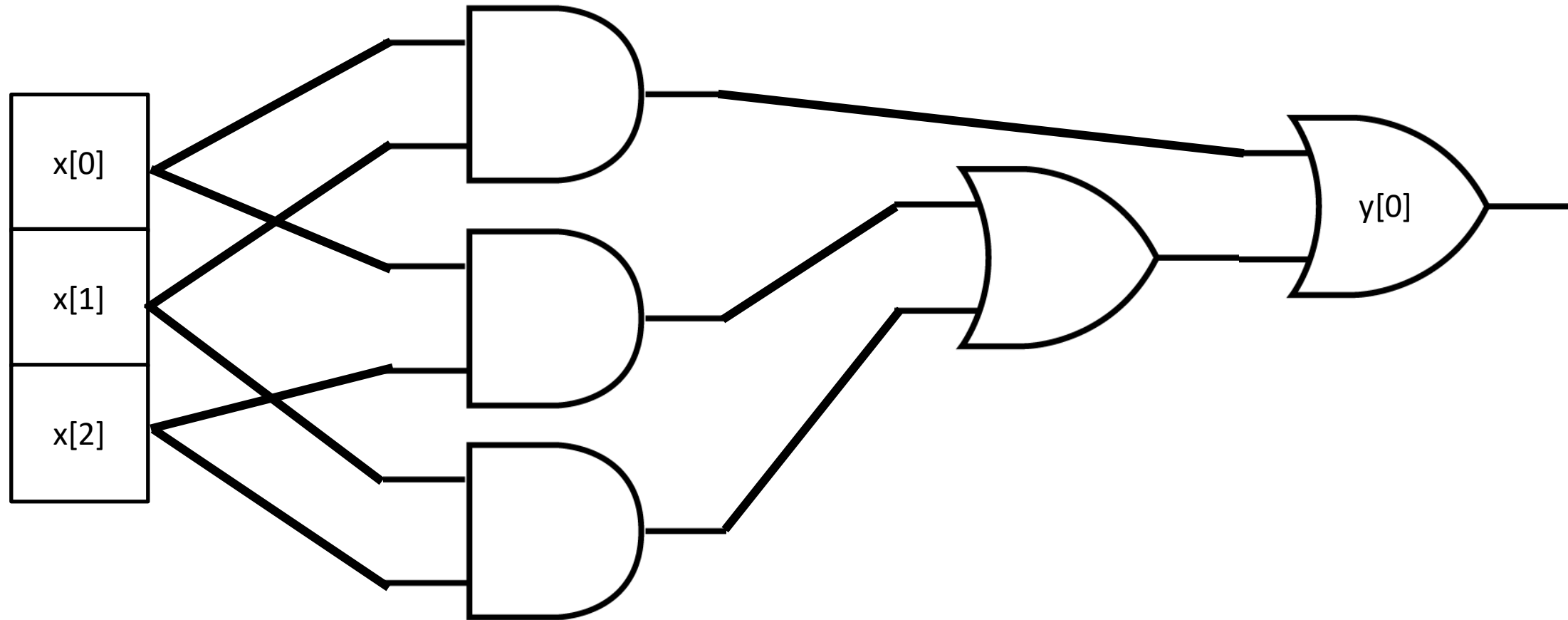
# NAND Straightline = AON Straightline

- What could be benefits of each of them?

# Another approach: Boolean Circuits

- AND The AND gate symbol is a D-shaped logic gate. It has two horizontal input lines on the left side and one horizontal output line on the right side. The top part of the gate is a semi-circle.
- OR The OR gate symbol is a logic gate with a curved input side on the left and a pointed output side on the right. It has two horizontal input lines on the left and one horizontal output line on the right.
- NOT The NOT gate symbol is a triangular logic gate. It has one horizontal input line on the left and one horizontal output line on the right. The output line ends in a small circle, known as a bubble, which indicates inversion.

# Median with Boolean Circuits



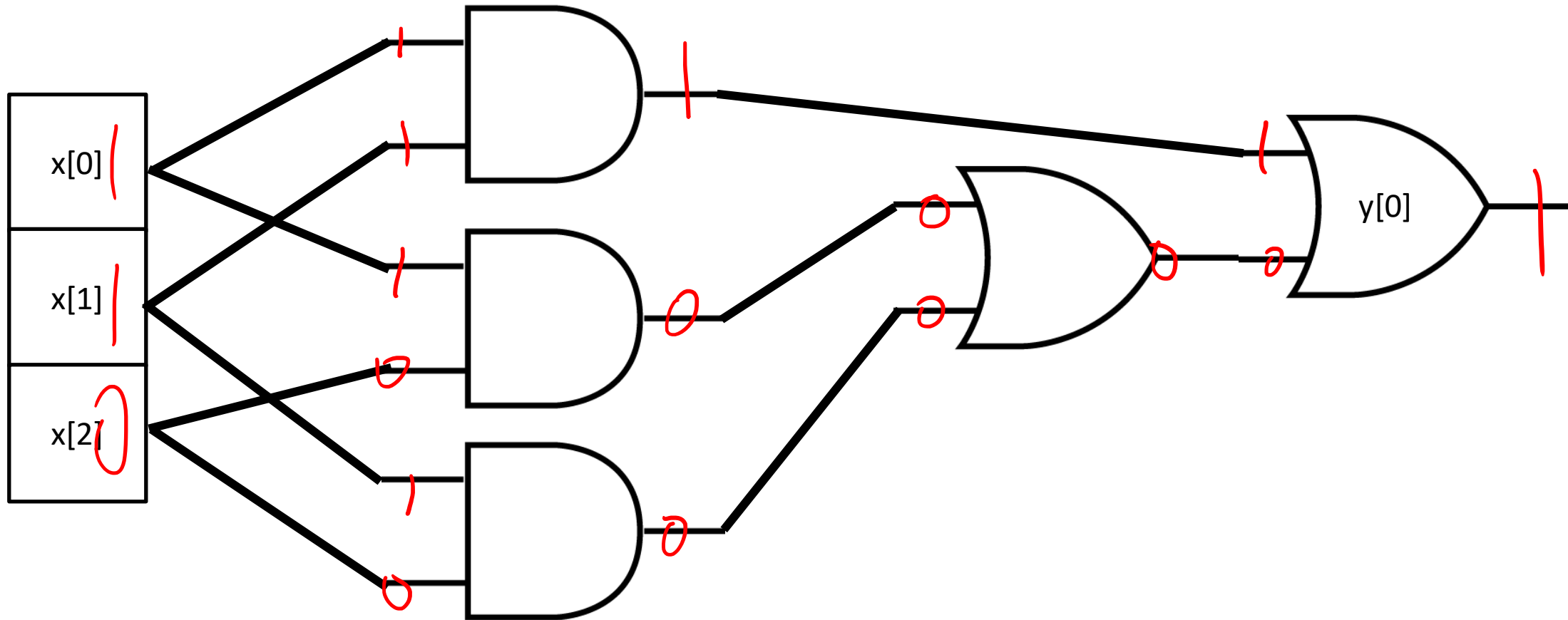
# Formal Definition of Boolean Circuits

- A Boolean circuit with  $n$  inputs,  $m$  outputs, and  $s$  gates is a *directed acyclic graph*
- Exactly  $n$  nodes have no in-neighbors (these are **inputs**, label them  $x[0], \dots, x[n-1]$ )
- All remaining  $s$  nodes have a label **AND**, **OR**, **NOT**. AND and OR gates have two in-neighbors, NOT gates have one in-neighbor
- Exactly  $m$  gates are denoted as outputs (label them  $y[0], \dots, y[m-1]$ )



# ~~Majority~~ with Boolean Circuits

Median

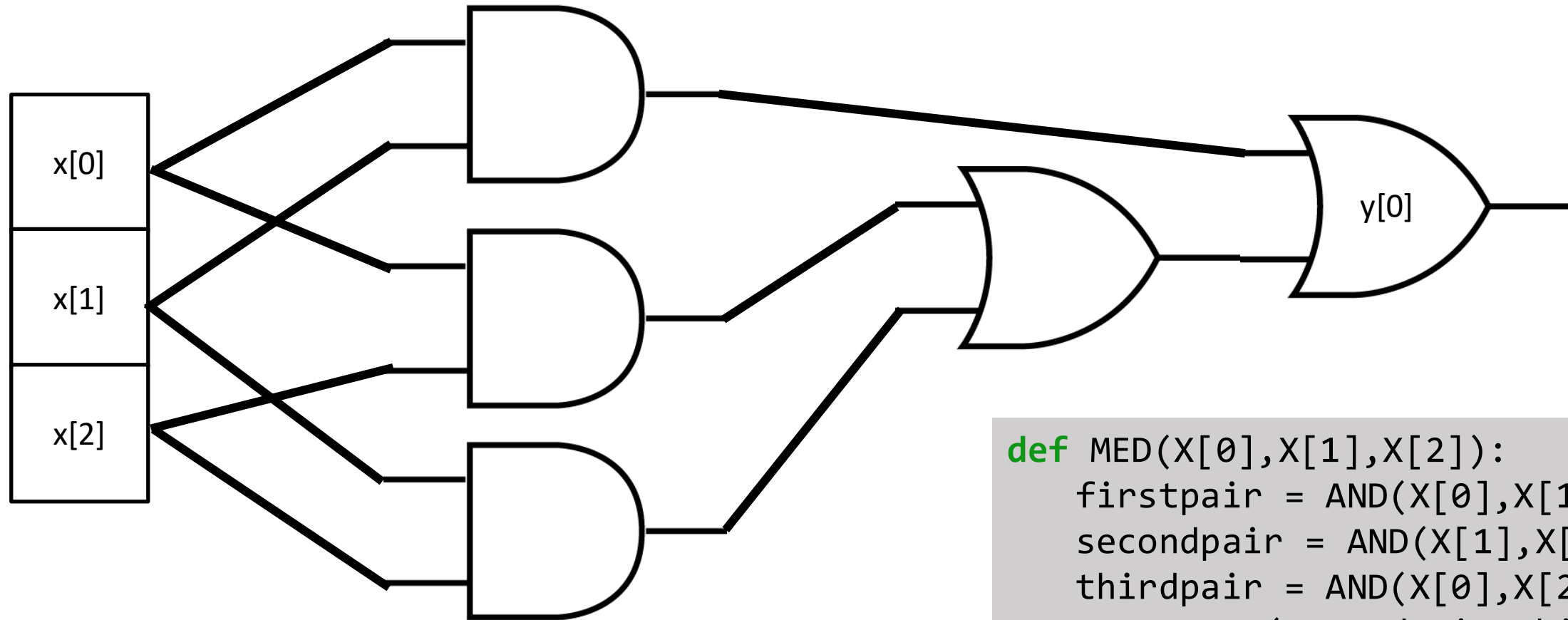


# Computing with a Boolean Circuit

- Assign gates into *layers* such that gate  $x$  appears before gate  $y$  whenever  $x$  has an outgoing edge that's an incoming edge of  $y$
- For each input node  $x[i]$ , assign its value to be bit  $i$  in the input
- For each gate (considered in order of layers), assign as its value the result of its labelled operation applied to its in-neighbor(s)
- The result is the bit-string given by the values of the output gates

# Median with Boolean Circuits

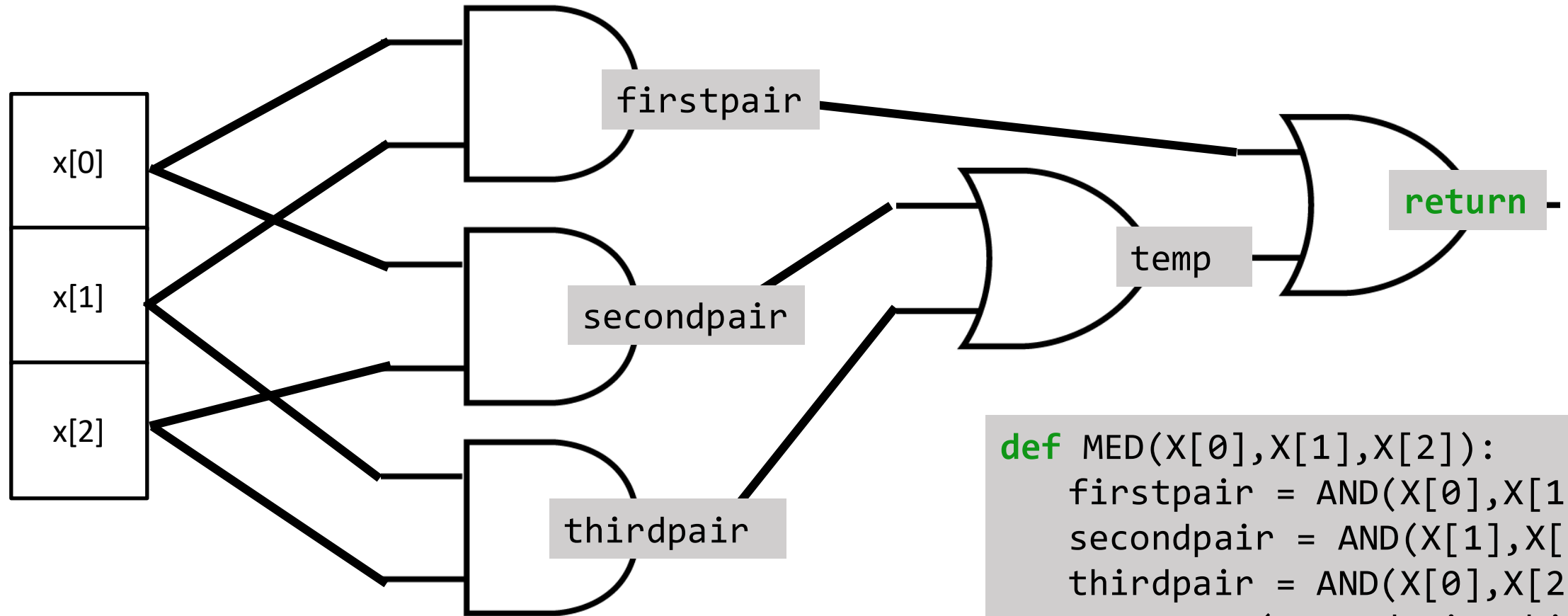
→ AON straightline program



```
def MED(X[0],X[1],X[2]):  
    firstpair = AND(X[0],X[1])  
    secondpair = AND(X[1],X[2])  
    thirdpair = AND(X[0],X[2])  
    temp = OR(secondpair,thirdpair)  
    return OR(firstpair,temp)
```

# Median with Boolean Circuits

→ AON straightline program



```
def MED(X[0],X[1],X[2]):  
    firstpair = AND(X[0],X[1])  
    secondpair = AND(X[1],X[2])  
    thirdpair = AND(X[0],X[2])  
    temp = OR(secondpair,thirdpair)  
    return OR(firstpair,temp)
```

# Circuits equivalent to AON Straightline

- How do we show this?
  - Show how to convert any circuit to an AON straightline that computes the same function
  - Show how to convert any AON straightline to a circuit that computes the same function

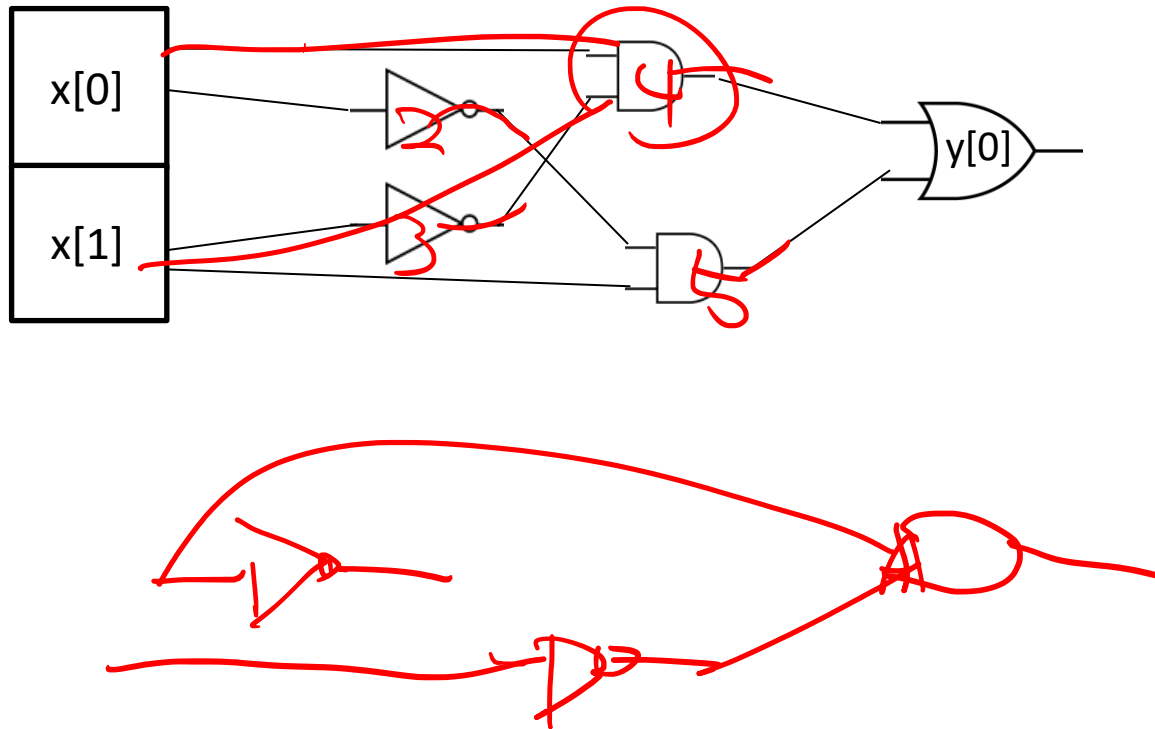
# Circuit to Straightline (saw an example)

*Topological Sort on gates of Circuit.*

- Circuit inputs are straightline inputs already
- Each gate gets a variable
- Value of that variable is result of applying the operation of that gate to the variables of the in-neighbors
- Output is variable values of the output gates

# Another example: XOR

Circuit



Program

```
V2 = NOT(x[0])
V3 = NOT(x[1])
V4 = AND(x[0], V3)
V5 = AND(x[1], V2)
ret OR(V4, V5)
```

# AON-Straightline to Circuit

- Straightline inputs become circuit inputs
- Each variable becomes a gate
- The type of gate is given by the RHS of the assignment in the AON program
- The in-neighbors of the gate are the gates represented by the operand variables
- The output gates are the ones represented by return variables



# Observations (2<sup>nd</sup> one as important)

- Everything function computable by a circuit is also computable by a straightline program (and vice-versa)
- Every function computable by a straightline program with  $s$  variables is computable by a circuit with  $s$  gates (and the converse)

# Universality

# What does it mean for a Gate Set to be *Universal*?

**Theorem 3.12 (NAND is a **universal** operation)**

*For every Boolean circuit  $C$  of  $s$  gates, there exists a NAND circuit  $C'$  of at most  $3s$  gates that computes the same function as  $C$ .*

**Definition 3.20 (General straight-line programs)**

Let  $\mathcal{F} = \{f_0, \dots, f_{t-1}\}$  be a finite collection of Boolean functions, such that  $f_i : \{0, 1\}^{k_i} \rightarrow \{0, 1\}$  for some  $k_i \in \mathbb{N}$ . An  $\mathcal{F}$  *program* is a sequence of lines, each of which assigns to some variable the result of applying some  $f_i \in \mathcal{F}$  to  $k_i$  other variables. As above, we use  $x[i]$  and  $y[j]$  to denote the input and output variables.

We say that  $\mathcal{F}$  is a **universal** set of operations (also known as a **universal** gate set) if there exists a  $\mathcal{F}$  program to compute the function *NAND*.

**(Informal) Definition.** We say a computation model is *universal* if for **any** finite function  $f: \{0,1\}^n \rightarrow \{0,1\}^m$ , there is an “instance” of the model that computes  $f$ .

Theorem:  
AON circuits is universal.

Corollary:  
NAND is universal.

Goal: Compute  $f: \{0,1\}^n \rightarrow \{0,1\}^m$

- Let  $f_1, f_2, \dots, f_m$  be functions such that
  - $f_i: \{0,1\}^n \rightarrow \{0,1\}$
  - $f_i(x)$  is the  $i$ th bit of  $f(x)$

# Goal: Compute $f: \{0,1\}^n \rightarrow \{0,1\}$

(Also called “Boolean” functions) *output 1 bit.*

- Represent  $f$  as a string  $s_f$ :

$$s_f = b_0 b_1 \dots b_{2^n-1}, \quad \underline{b_i = f(i)}$$

- We have  $f(i) = s_f[i]$

- Can we implement “array” using AON gates?

- Want: LOOKUP(s, i) outputs  $s[i]$

*AON*

# Gate: IF(cond, a, b)

- Output a if cond = 1
- Output b if cond = 0

cond	a	b	IF(cond, a, b)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

# Array: LOOKUP<sub>k</sub>(s, i)

- $k: 1, 2, 3, \dots$
- $s: 2^k$ -bit string,  $s = b_0 b_1 \dots b_{2^k-1}$
- $i: k$ -bit string, representing  $0, 1, \dots, 2^k - 1$
- LOOKUP<sub>k</sub>(s, i) outputs s[i] =  $b_i$



# Circuit: LOOKUP<sub>1</sub>(s, i)

$k: 1, 2, 3, \dots$

$s = b_0 b_1 \dots b_{2^k - 1}$

$i$  represent  $0, 1, \dots, 2^k - 1$

outputs  $s[i] = b_i$

- LOOKUP<sub>1</sub>(s, i) = LOOKUP<sub>1</sub>( $b_0 b_1$ , i)

$\bar{i} = 0$

$b_0$

$\bar{i} = 1$

$b_1$

IF ( Cond =  $\bar{i}$  ,  $b_1$  ,  $b_0$  )

# Circuit: LOOKUP<sub>2</sub>(s, i)

$k: 1, 2, 3, \dots$

$s = b_0 b_1 \dots b_{2^k-1}$

$i$  represent  $0, 1, \dots, 2^k - 1$

outputs  $s[i] = b_i$

- LOOKUP<sub>2</sub>(s, i) = LOOKUP<sub>2</sub>( $b_0 b_1 b_2 b_3$ , i)

# Circuit: LOOKUP<sub>k</sub>(s, i)

$k: 1, 2, 3, \dots$

$s = b_0 b_1 \dots b_{2^k-1}$

$i$  represent  $0, 1, \dots, 2^k - 1$

outputs  $s[i] = b_i$

- LOOKUP<sub>k</sub>(s, i) = LOOKUP<sub>k</sub>( $b_0 b_1 \dots b_{2^k-1}$ , i)
- Recurse!

# Circuit: LOOKUP<sub>k</sub>(s, i)

$k: 1, 2, 3, \dots$

$s = b_0 b_1 \dots b_{2^k-1}$

$i$  represent  $0, 1, \dots, 2^k - 1$

outputs  $s[i] = b_i$

LOOKUP<sub>k</sub>(s, i):

first\_half = LOOKUP<sub>k-1</sub>(s[0:2<sup>k-1</sup>], i[1:k])

second\_half = LOOKUP<sub>k-1</sub>(s[2<sup>k-1</sup>:2<sup>k</sup>], i[1:k])

return IF(i[0], second\_half, first\_half)

Theorem:

AON circuit is universal.

# PS2: Autograder Updated

Test cases shall be public.

If you passed all tests in the notebook and on Gradescope, you are good.

# Charge

## Computation Model

*AND, OR, NOT  
Universality*

PS2: due this Friday 10:00pm

PS3: to be released today, due next Friday 10:00pm

PRR3: due next Monday 10:00pm

