Enabling Parallel Abstraction Layer to DCA++ using HPX And GPUDirect

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To follow slides: http://tiny.cc/msdefense

Enabling High-Level Parallel Abstractions to DCA++ Using HPX and GPUDirect

Portion of this talk has been presented in:

- SCALA 2020, Feb 2020. Baton Rouge, LA. Link
- Theater Talk at SuperComputing 19, Nov 2019. Denver, CO. Link
- SciDAC CompFUSE annual all-hands meeting, Oct 2019. Oak Ridge, TN.

Accepted talk:

- P3HPC: 2020 Performance, Portability, and Productivity in HPC Forum. TBD. Link

SciDAC: Computational Framework for Unbiased Studies of Correlated Electron Systems

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Ying Wai Li (LANL) [former ORNL]

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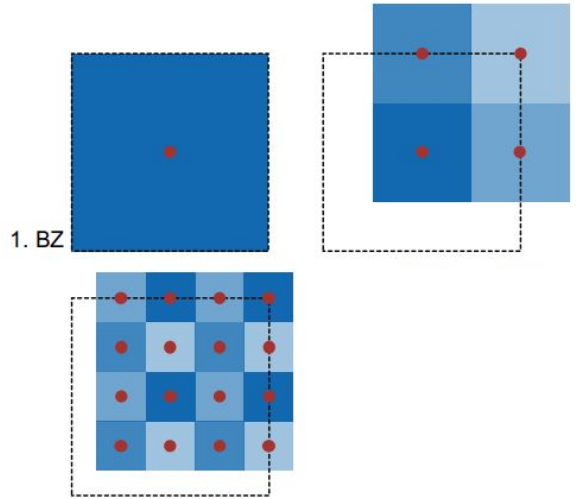
Outline

- What is DCA++? -- Scientific software for Dynamical Cluster Approximation
- Build threading abstraction layer using HPX
- Use GPUDirect to solve memory bound issue in DCA++

DCA ++ (Dynamical Cluster Approximation)

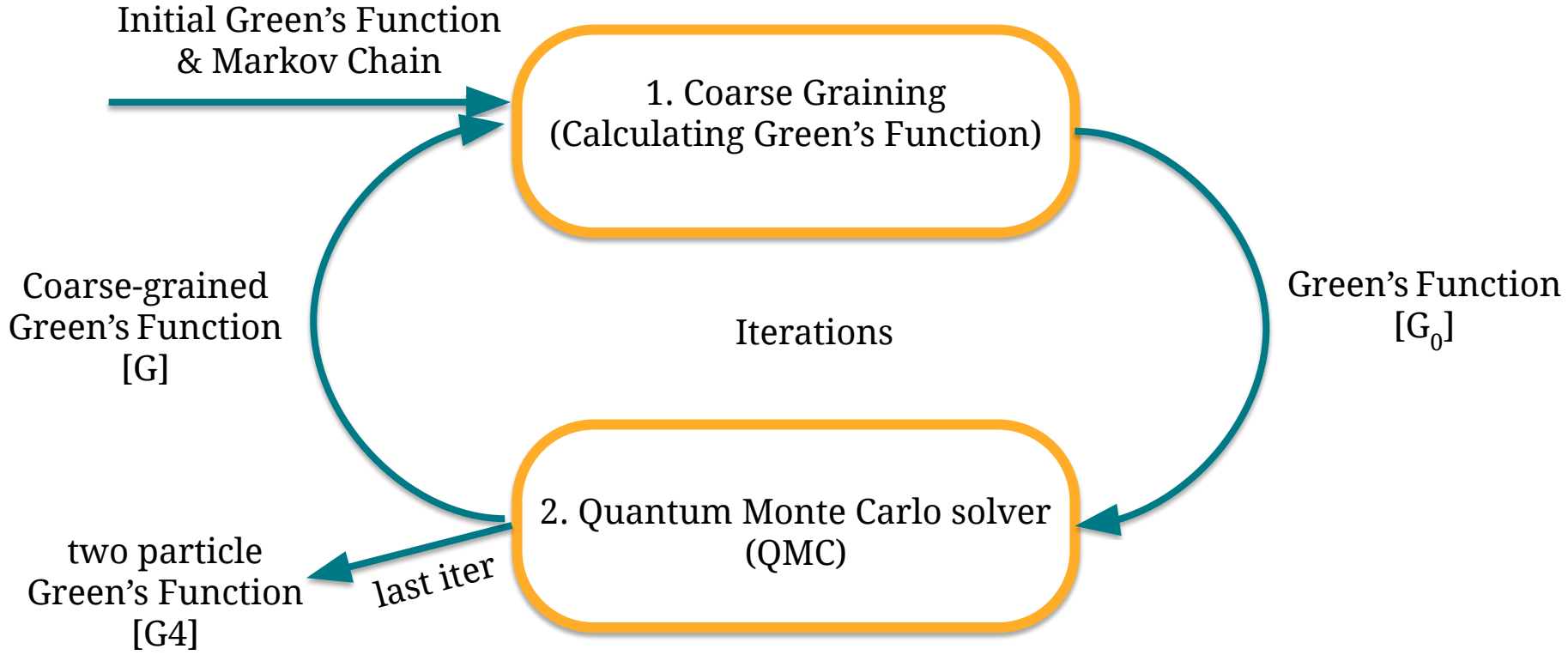
In the area of condensed matter physics, scientist would like to study some properties of materials, including high-temperature superconductivity, magnetism, and liquid behaviors. These behaviors are due to **strong electron-electron interaction** (mainly Coulomb repulsion).

DCA++ is a numerical simulation software to solve correlated electron problems with Quantum Monte Carlo method.



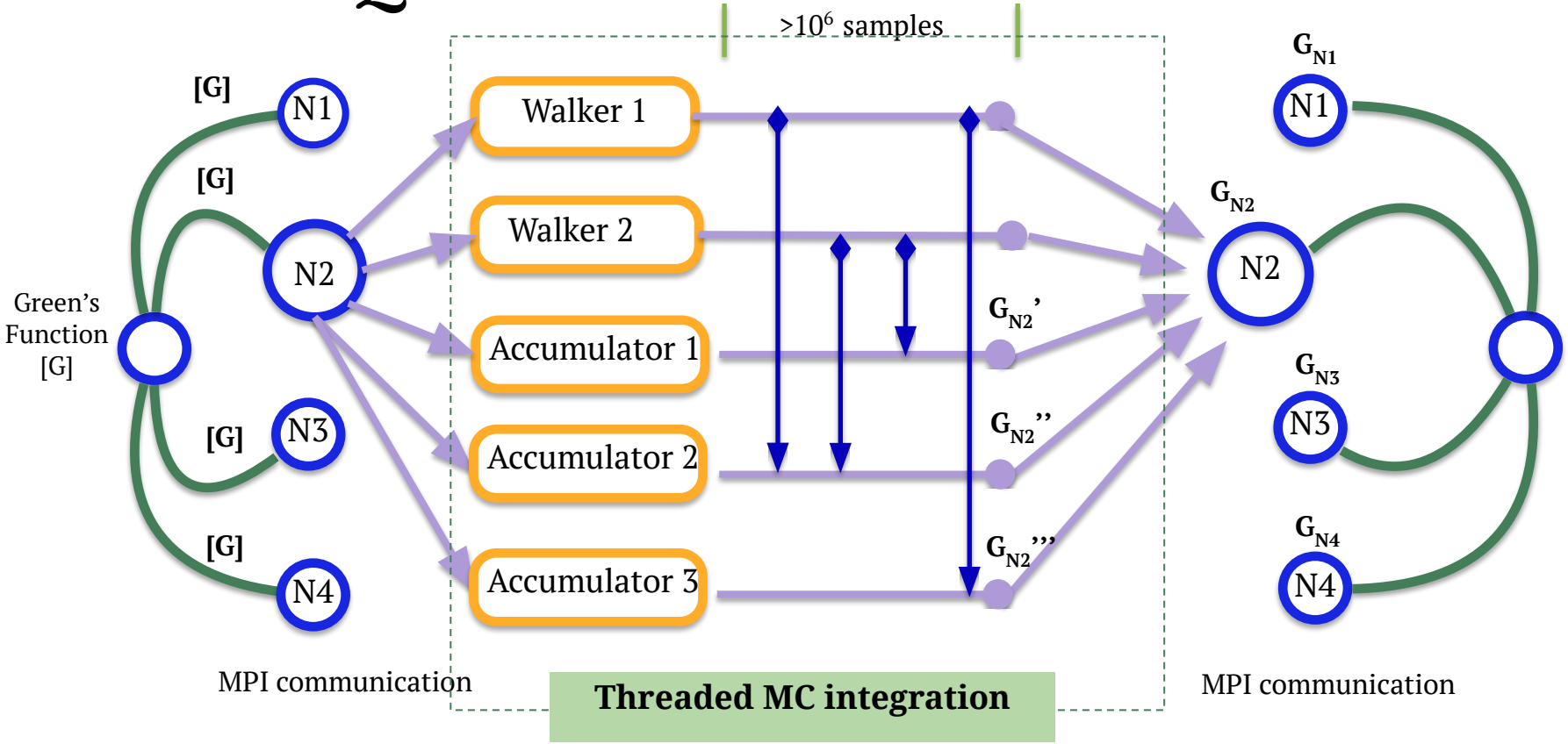
[1] DCA++ 2019. Dynamical Cluster Approximation. https://github.com/CompFUSE/DCA [Licensing provisions: BSD-3-Clause]
[2] Urs R. Hähner, Gonzalo Alvarez, Thomas A. Maier, Raffaele Solcà, Peter Staar, Michael S. Summers, and Thomas C. Schulthess, DCA++: A software framework to solve correlated electron problems with modern quantum cluster methods, Comput. Phys. Commun. 246 (2020) 106709.

DCA++: Primary kernels workflow



Balduzzi, Giovanni, Arghya Chatterjee, Ying Wai Li, Peter W. Doak, Urs Haehner, Ed F. D'Azevedo, Thomas A. Maier, and Thomas Schulthess. "Accelerating DCA++ (Dynamical Cluster Approximation) Scientific Application on the Summit Supercomputer." In *2019 28th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 433-444. IEEE, 2019.

DCA++ : Quantum Monte Carlo Solver



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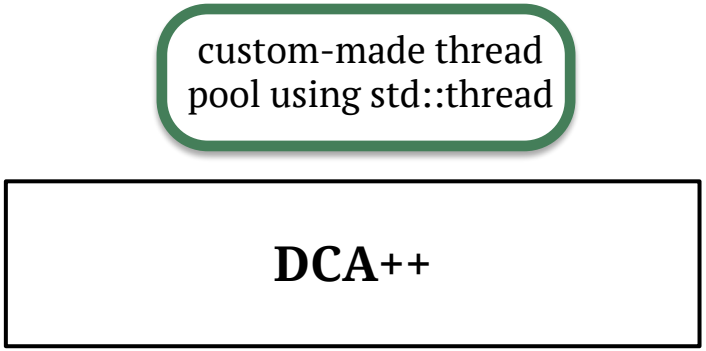
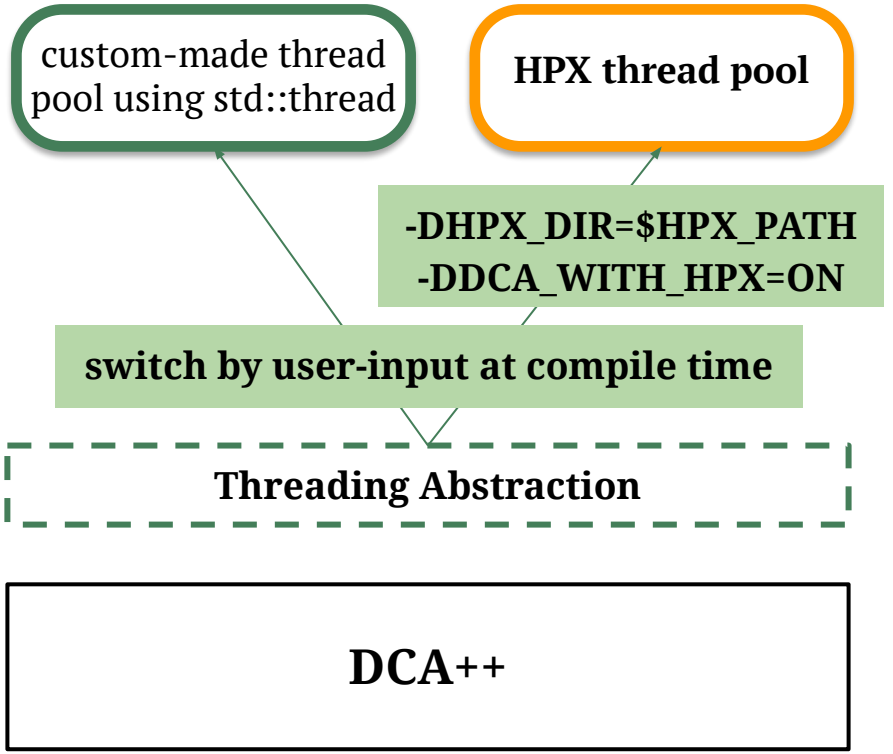
Threading Abstraction

Threading abstraction for QMC Solver

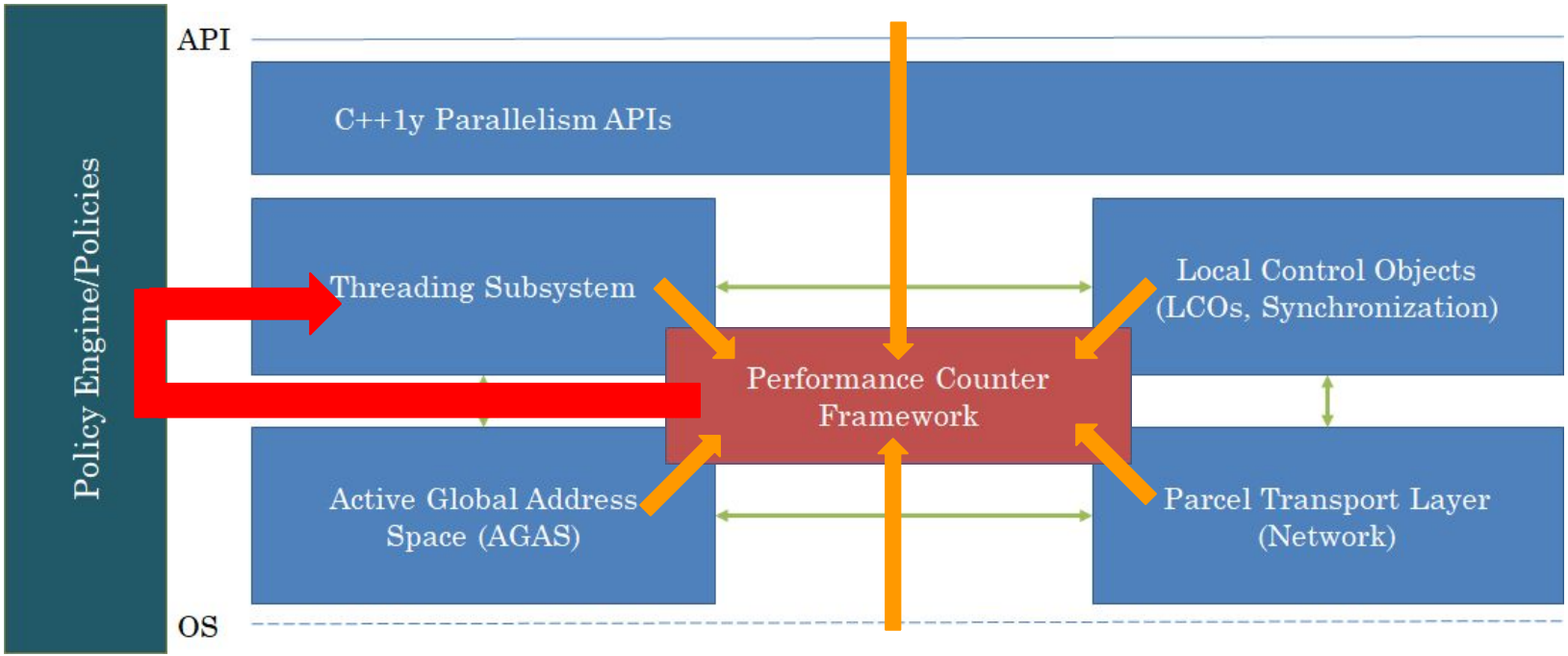
Original Implementation



New Implementation



HPX - High-Performance ParalleX



Kaiser, Hartmut, Thomas Heller, Bryce Adelstein-Lelbach, Adrian Serio, and Dietmar Fey. "Hpx: A task based programming model in a global address space." In Proceedings of the 8th International Conference on Partitioned Global Address Space Programming Models, pp. 1-11. 2014.

HPX - A General Purpose Runtime System

- Widely portable (raspberry pi → different OS → supercomputers)
- C++ standard compliant
- Opensource: 100+ developers over a decade
- Supported Distributed Machine Learning, Astrophysics, Coastal Modeling

OAK RIDGE National Laboratory **Open-sourced at GitHub: https://github.com/STEllAR-GROUP/hpx** STE||AR GROUP

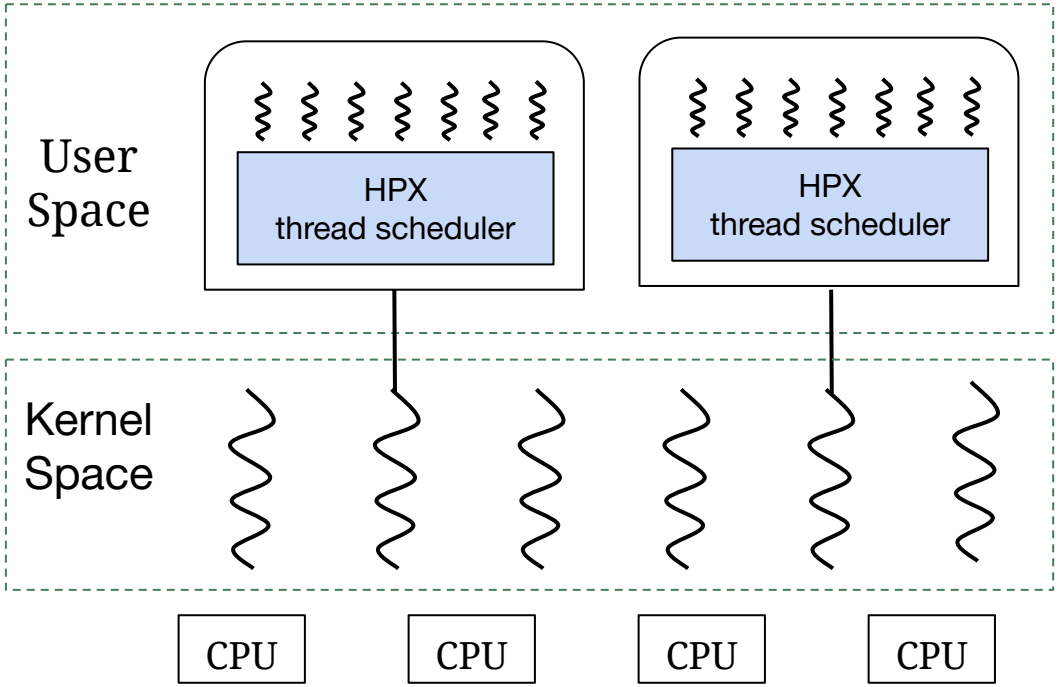
HPX - C++ standard compliant and more

- As close as possible to C++ standard library:

std::thread	hpx::thread
std::mutex	hpx::mutex
std::future	hpx::future
std::async	hpx::async
std::bind	hpx::bind
std::function	hpx::function
std::tuple	hpx::tuple
std::any	hpx::any
std::parallel::for_each, etc	hpx::parallel::for_each
std::cout	hpx::cout
std::vector	hpx::vector, hpx::partitioned_vector

- Extend standard APIs where needed (compatibility is preserved)

HPX thread pool



Nanosecond level

HPX thread is a lightweight user-level thread

- ~1000x faster context switch than OS thread

Microsecond level

Zhang, Tianyi, Shahrzad Shirzad, Patrick Diehl, R. Tohid, Weile Wei, and Hartmut Kaiser. "An Introduction to hpxMP: A Modern OpenMP Implementation Leveraging HPX, An Asynchronous Many-Task System." In Proceedings of the International Workshop on OpenCL, pp. 1-10. 2019.

QMC solver w/ std::thread

```
// original implementation w/ standard thread
vector<std::future<void>> futures;

auto& pool = ThreadPool::get_instance();

for (int i = 0; i < tasks.size(); ++i) {
   if (tasks.getTask(i) == "walker")
     futures.emplace_back(pool.enqueue(&ThisType::startWalker, this, i));

   // else if handle other conditions...
}
```

QMC solver w/ hpx

```
// new implementation w/ hpx
vector<hpx::future<void>> futures;

// auto& pool = ThreadPool::get_instance();

for (int i = 0; i < tasks.size(); ++i) {
   if (tasks.getTask(i) == "walker")
      futures.emplace_back(hpx::async(&ThisType::startWalker, this, i));

   // else if handle other conditions...
}
```

Threading Abstraction

std::thread

```
namespace dca {
namespace parallel {

struct thread_traits {
  template <typename T>
  using future_type          =        std::future<T>;
  using mutex_type           =        std::mutex;
  using condition_variable_type  =
                        std::condition_variable;
  using scoped_lock          =
                        std::lock_guard<mutex_type>;
  using unique_lock          =
                        std::unique_lock<mutex_type>;
}
} // namespace parallel
}; // namespace dca
```

HPX thread

```
namespace dca {
namespace parallel {

struct thread_traits {
  template <typename T>
  using future_type        =        hpx::future<T>;
  using mutex_type         =        hpx::mutex;
  using condition_variable_type  =
                        hpx::condition_variable;
  using scoped_lock        =
                        std::lock_guard<mutex_type>;
  using unique_lock        =
                        std::unique_lock<mutex_type>;
}
} // namespace parallel
}; // namespace dca
```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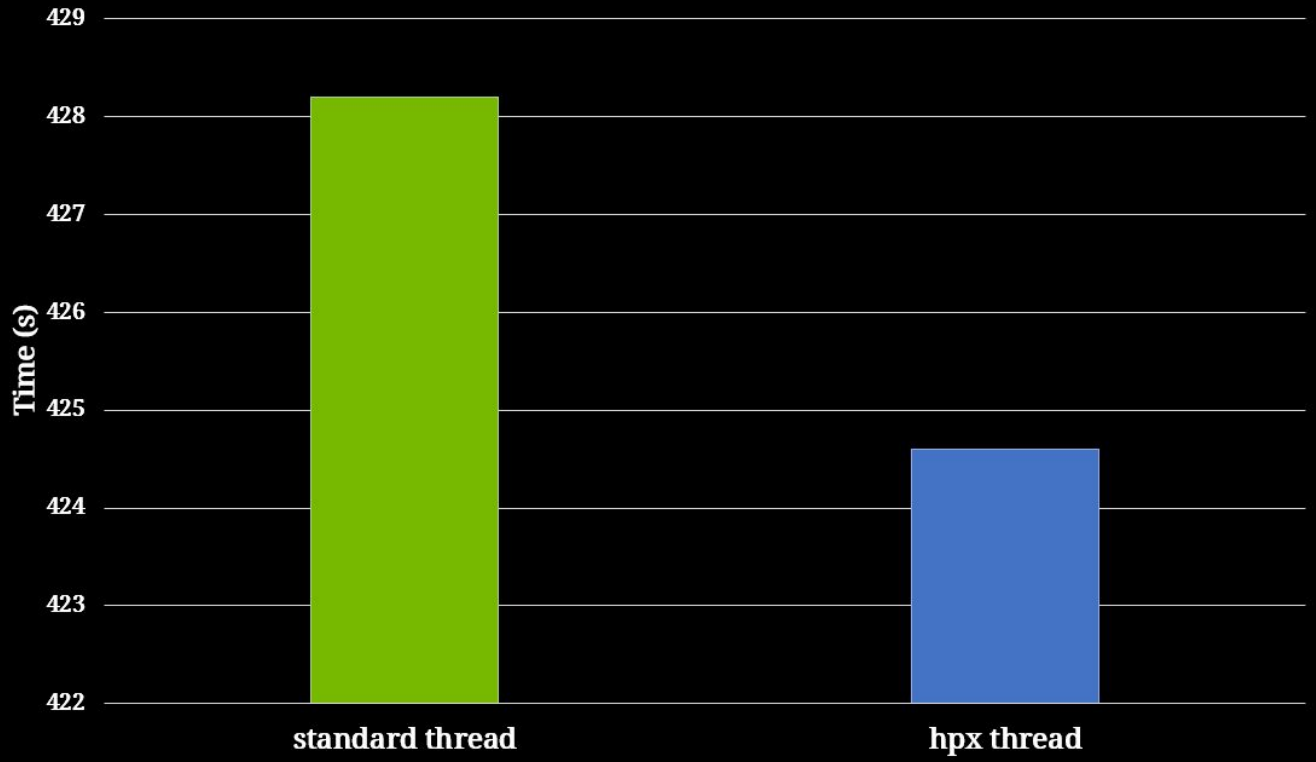
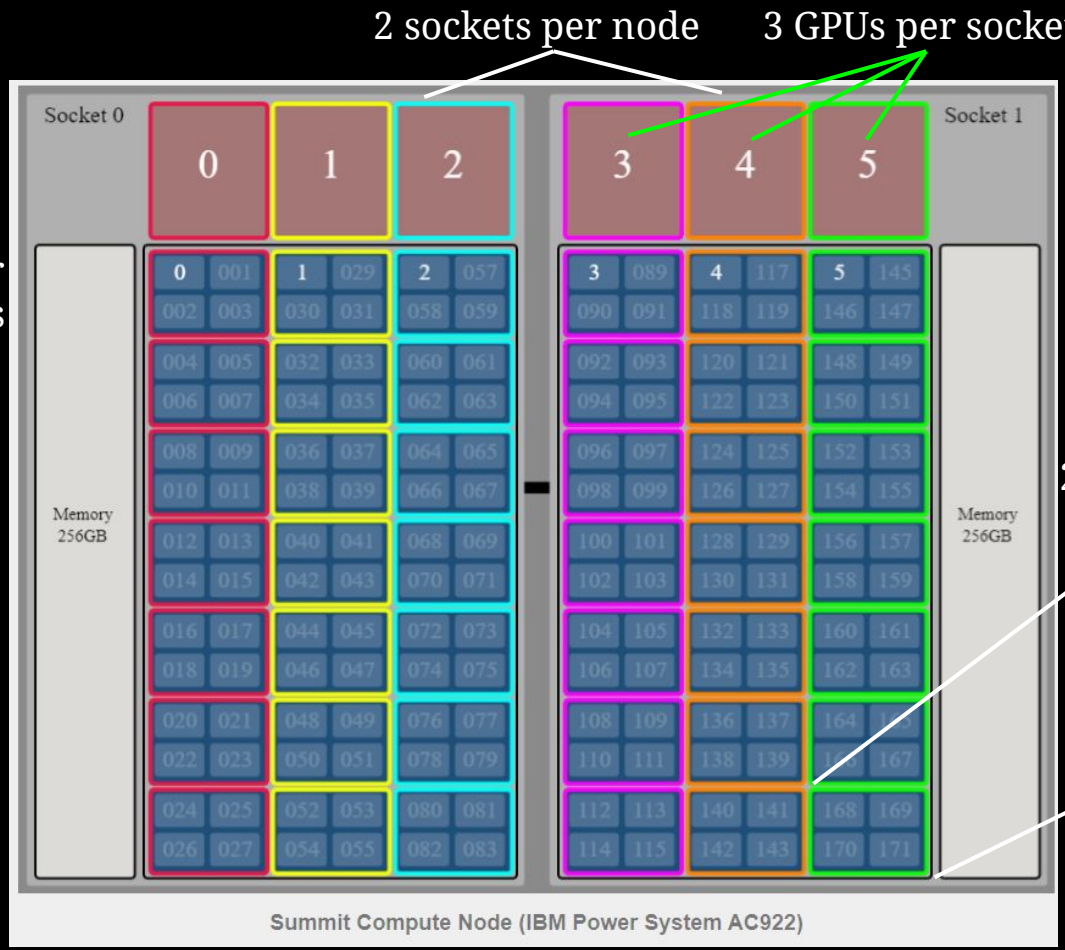
https://github.com/STEllAR-GROUP/DCA/tree/hpx_pr

Performance Measurement

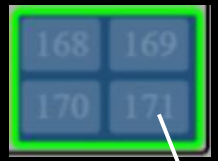
Compare DCA++ execution time between standard thread and hpx thread (threads=7)



- DCA only allows 1 GPU per rank
- Best strategy:
  - (1 gpu + 7 cpus) per rank, and 7 threads only



21 cores per socket

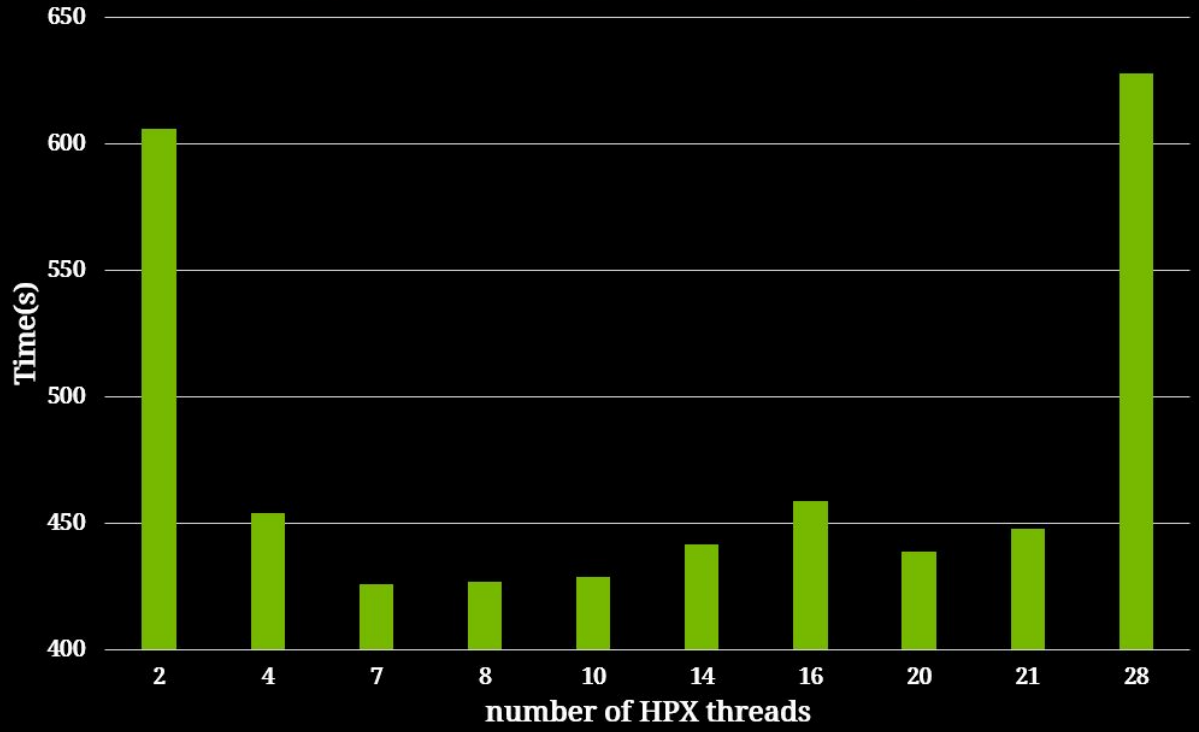


4 hardware threads per core

https://jsrunvisualizer.olcf.ornl.gov/?s1f1o01n6c7g1r11d1b21l0=

https://docs.olcf.ornl.gov/systems/summit_user_guide.html

Compare DCA++ execution time among different numbers of HPX threads



Sub-summary

- **Threading abstraction w/ HPX light-weight threads:**
  - Added threading abstraction
  - Profiled performance
  - Future work
    - To add more tasks continuation to fully utilize hardware resources

Memory Bound Issue and Solution

Memory bound issue and solution

- Memory bound issue caused by the size of G4

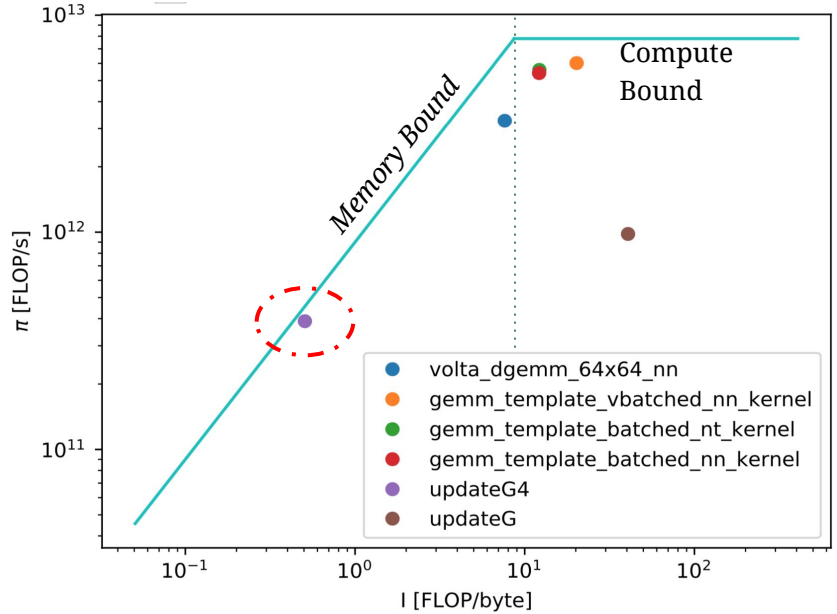


Fig. : Roofline plot of a NVIDIA V100 GPU running DCA++ at production level on Summit (OLCF)

Solution: *broadcasting* each G_2[][] matrix to all other ranks:

- Regular MPI method
- NVLink method

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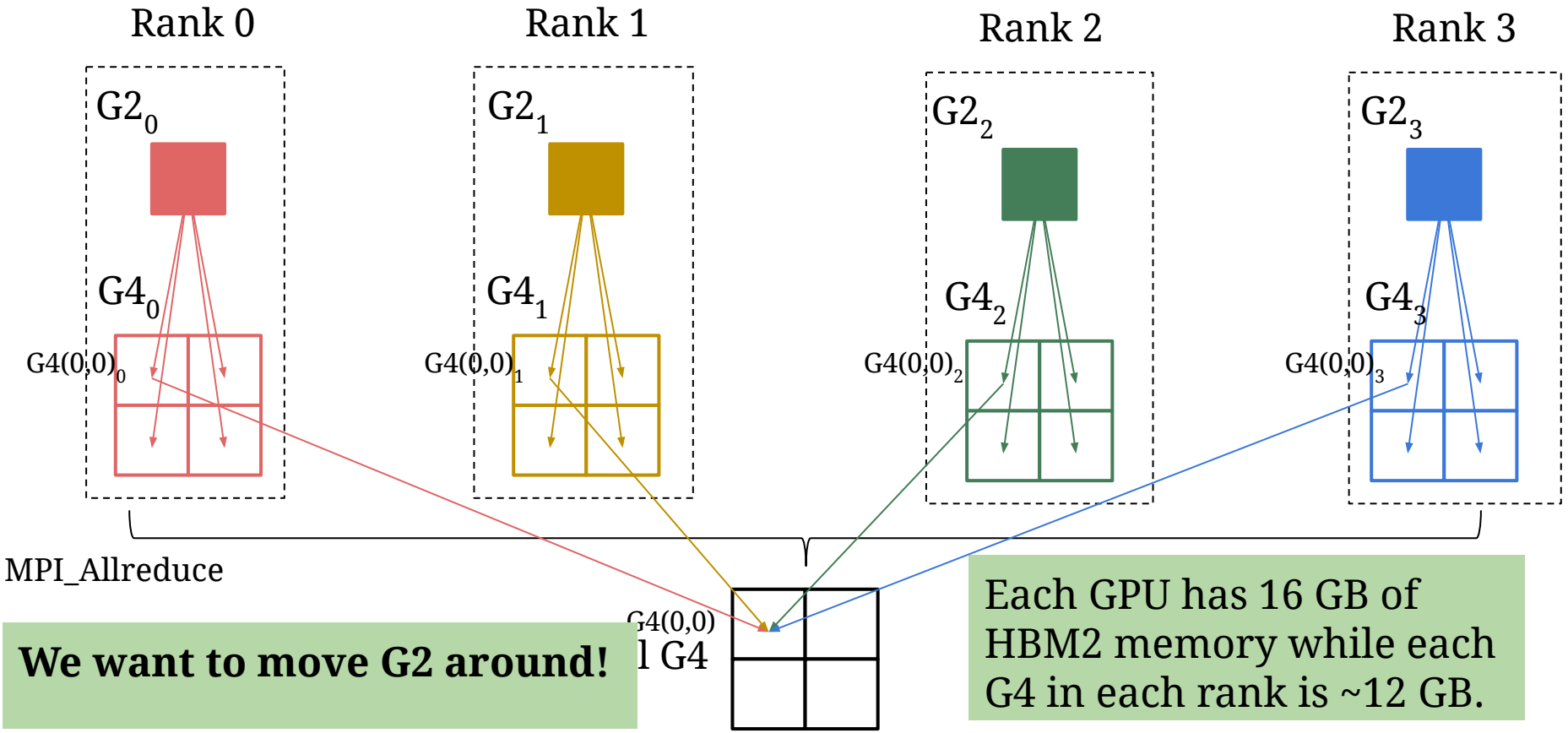
G. Balduzzi, A. Chatterjee, Y.W. Li, P. Doak, U. Haehner, Ed. Azevedo, T. Maier, T. Schulhess. *Accelerating DCA++ (Dynamical Cluster Approximation) Scientific Application on the Summit supercomputer*. **PACT 2019**.

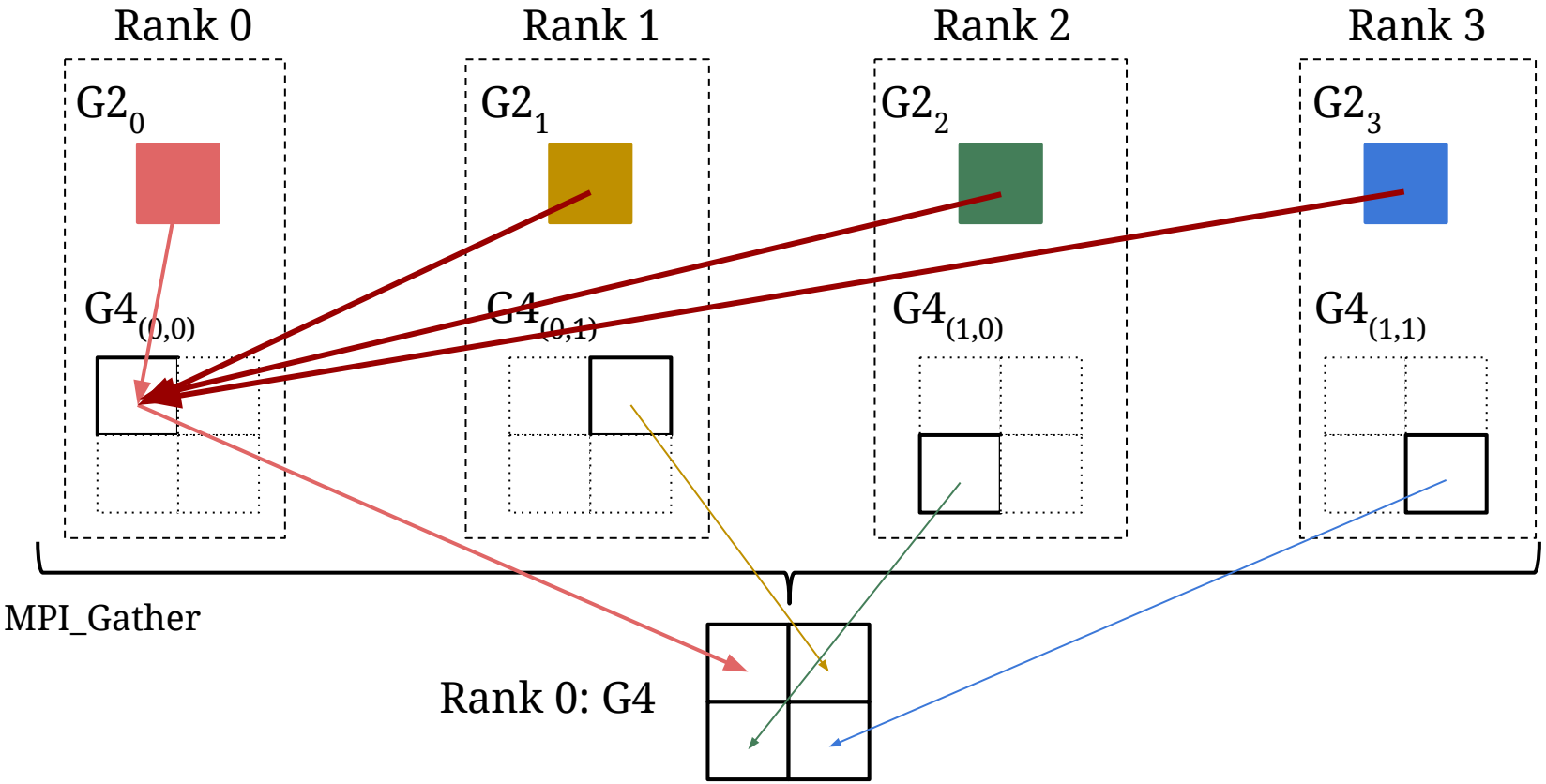
Memory bound issue w/ G4



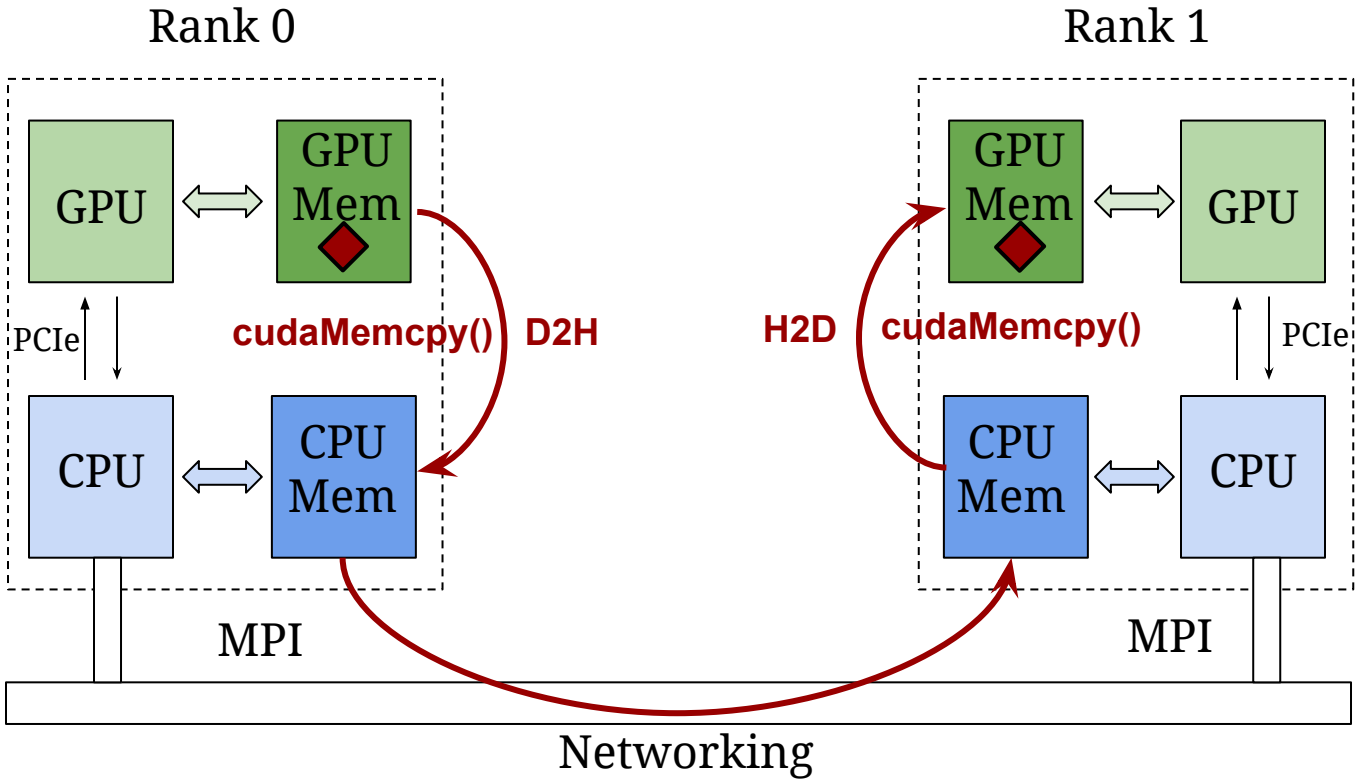
We want to move G2 around!

Each GPU has 16 GB of HBM2 memory while each G4 in each rank is ~12 GB.

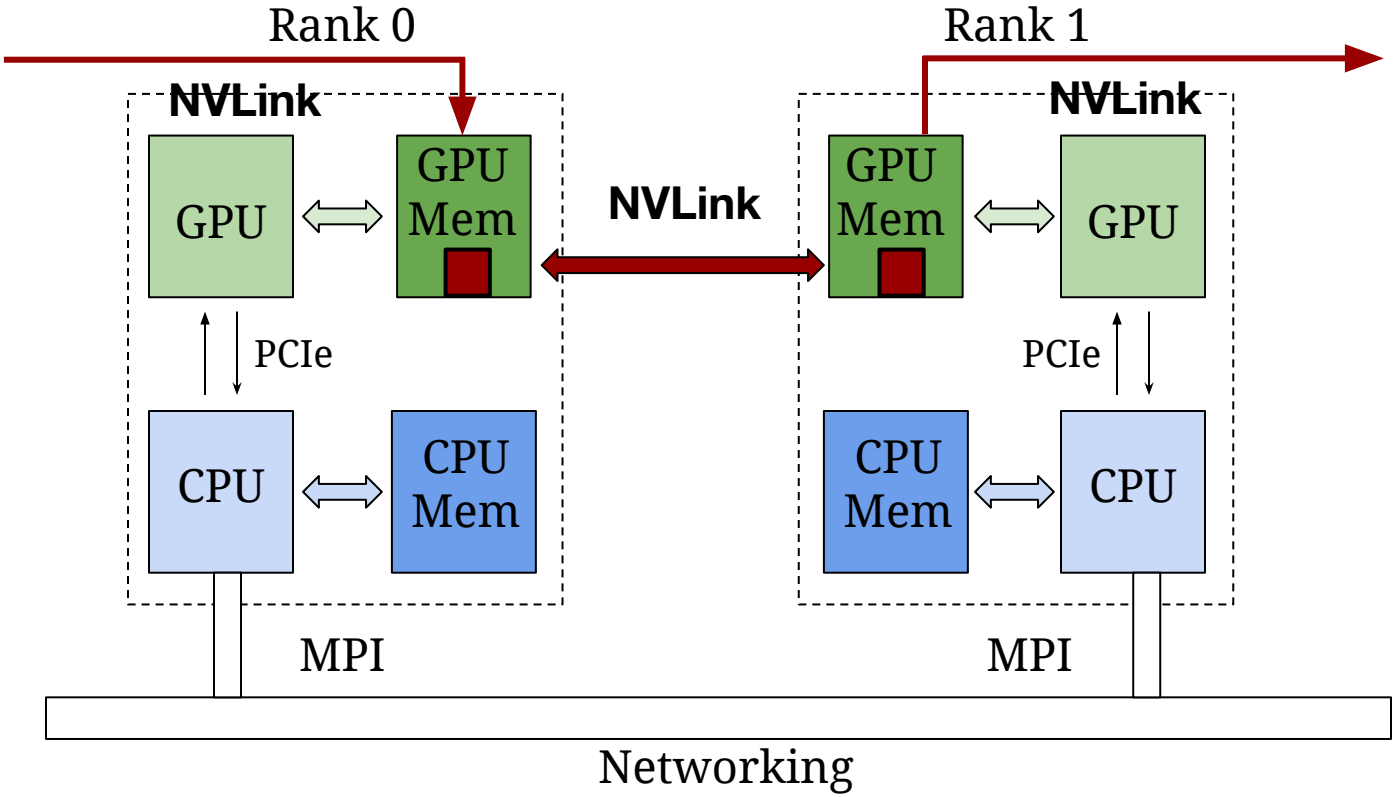
Move G2 around



Moving G2 around: Regular MPI method

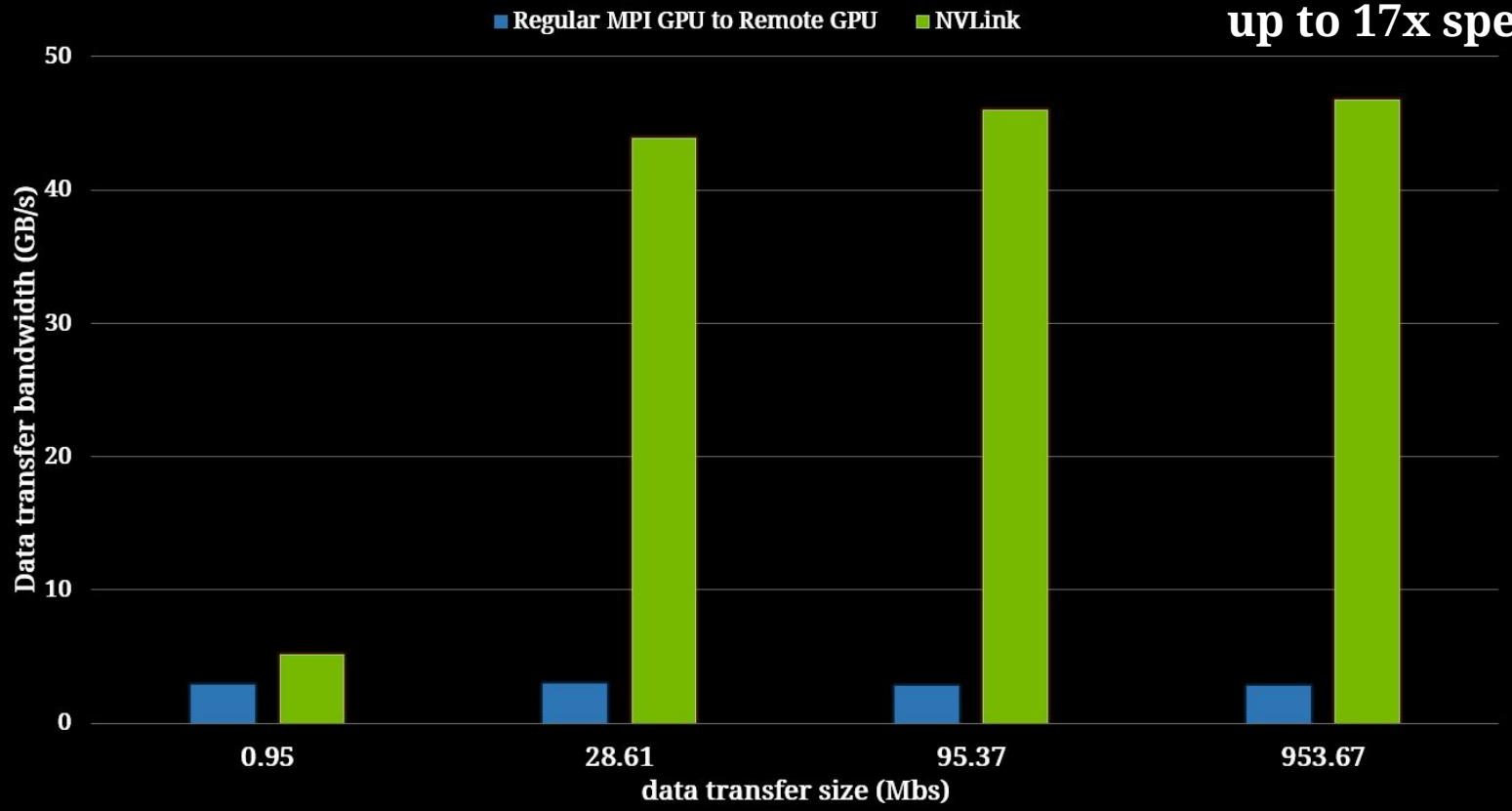


Moving G2 around: NVLink method



Bandwidth Measurement

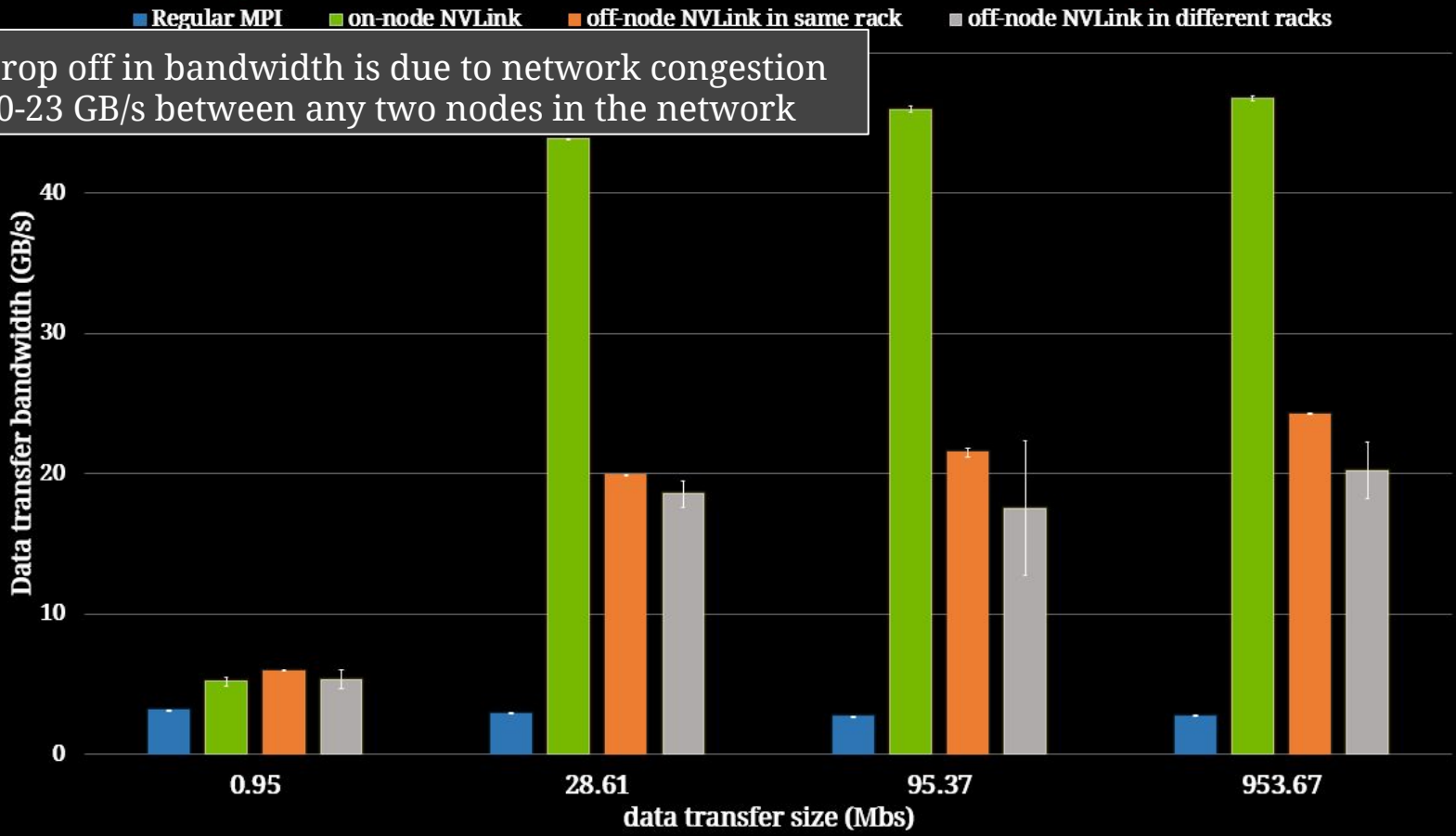
Compare on-node bandwidth of data transfer on Summit between NVLink and Regular MPI GPU to Remote GPU method



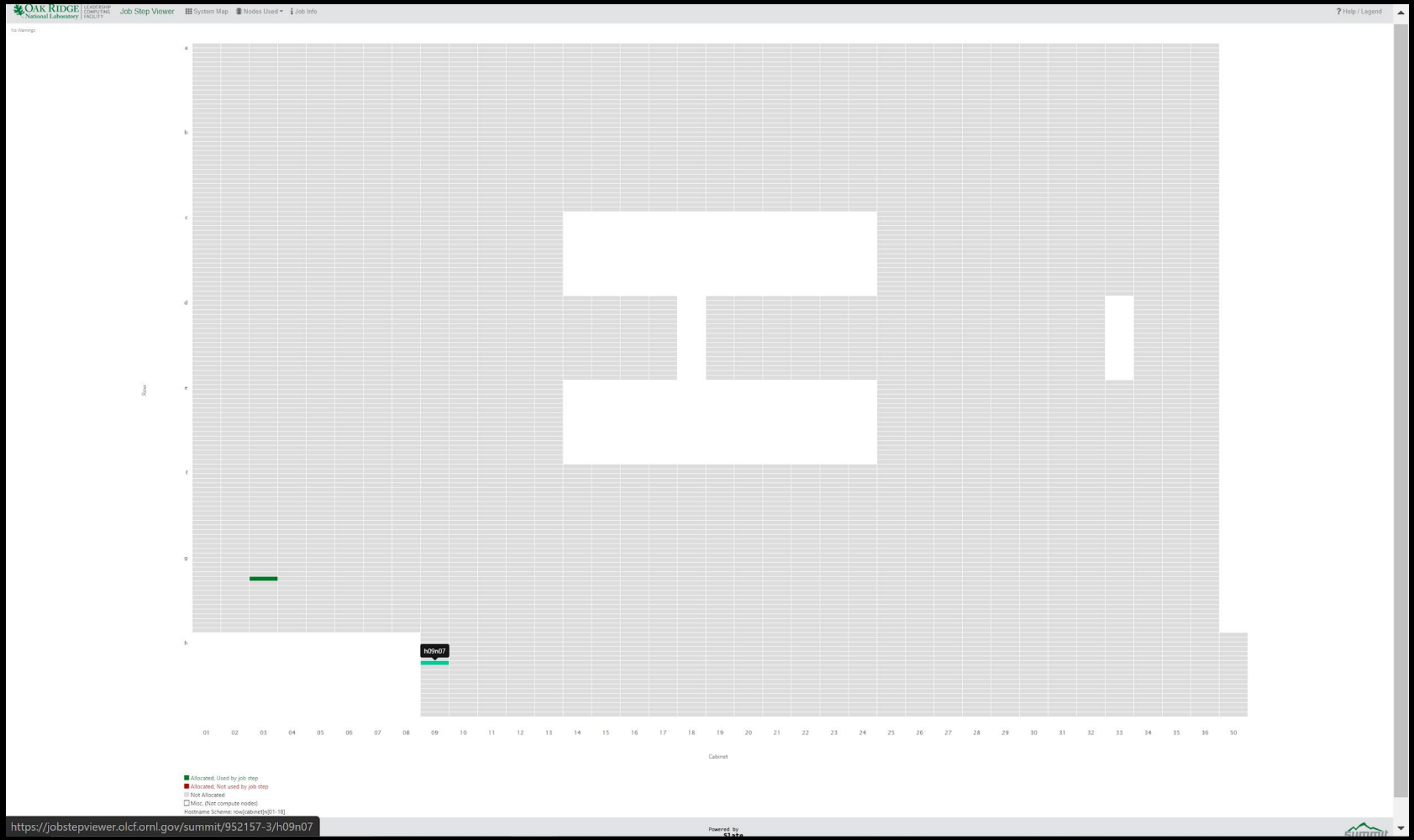
Ping-pong benchmark: https://github.com/weilewei/Ring_example_MPI_CUDA/blob/master/gpuDirect.cpp

Compare bandwidth of data transfer on Summit using NVLink

- Drop off in bandwidth is due to network congestion
- 20-23 GB/s between any two nodes in the network



Ping-pong benchmark: https://github.com/weilewei/Ring_example_MPI_CUDA/blob/master/gpuDirect.cpp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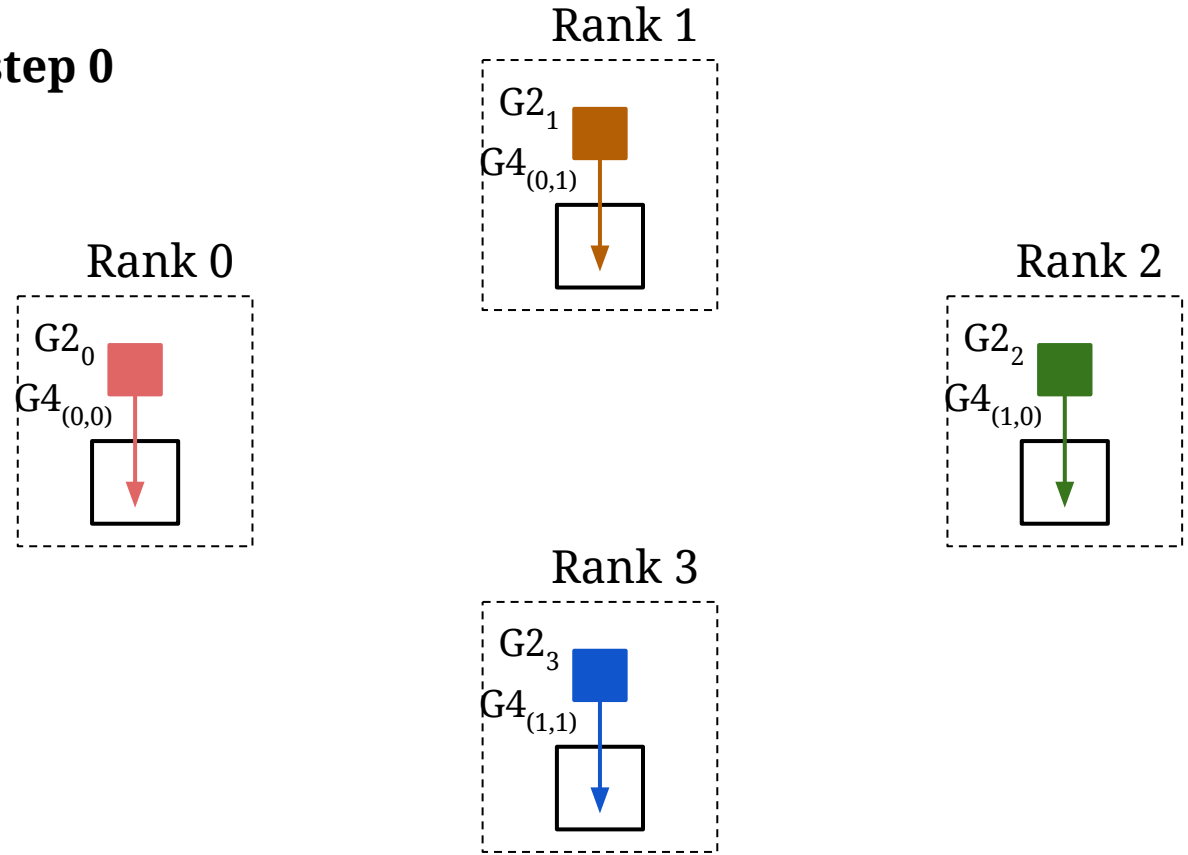
LEADERSHIP COMPUTING FACILITY
Job Step Viewer
System Map
Nodes Used
Job Info
Help / Legend
No Warnings
Row
a
b
c
d
e
f
g
h
h09n07
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 50
Cabinet
Allocated, Used by job step
Allocated, Not used by job step
Not Allocated
Misc. (Not compute nodes)
Hostname Scheme: row[cabinet][n][1-18]
Powered by
https://jobstepviewer.olcf.ornl.gov/summit/952157-3/h09n07

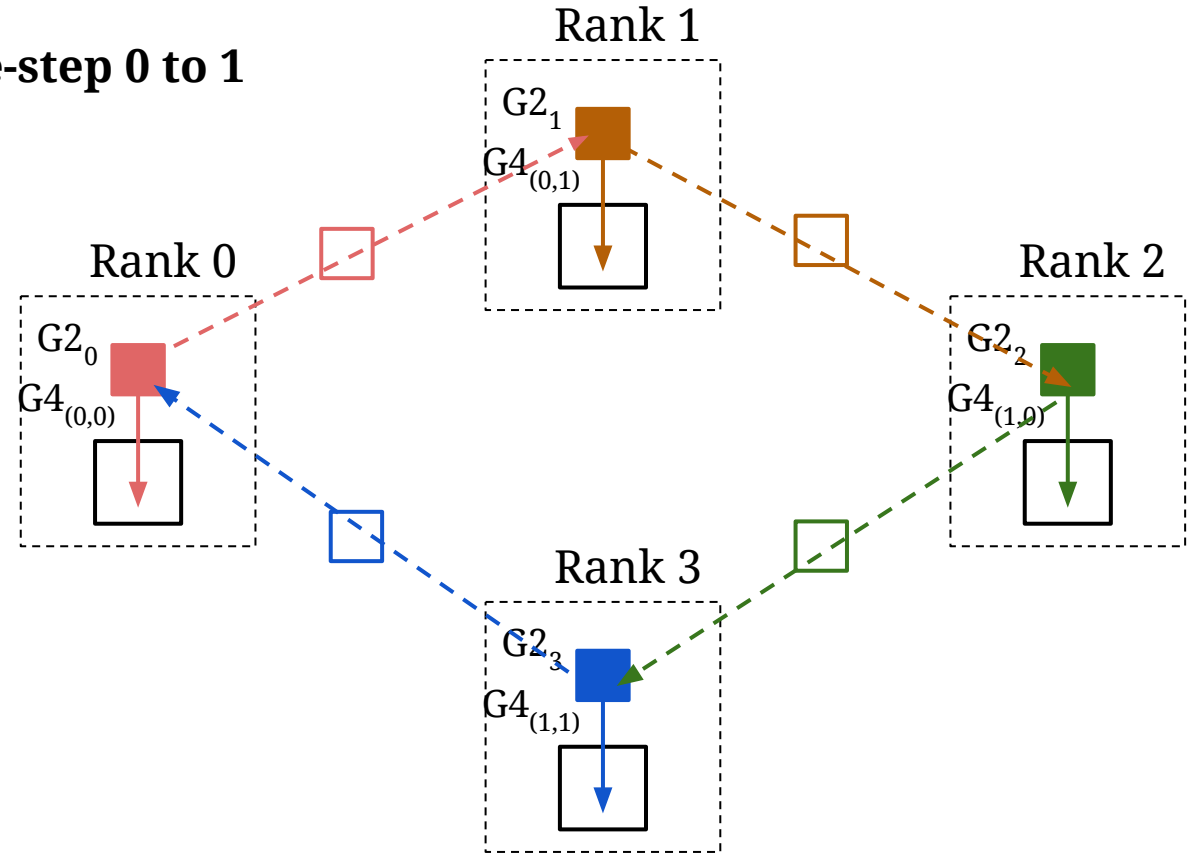
Pipelined Ring Algorithm

Time-step 0



code: https://github.com/weilewei/Ring_example_MPI_CUDA/blob/master/G2_ring.cpp

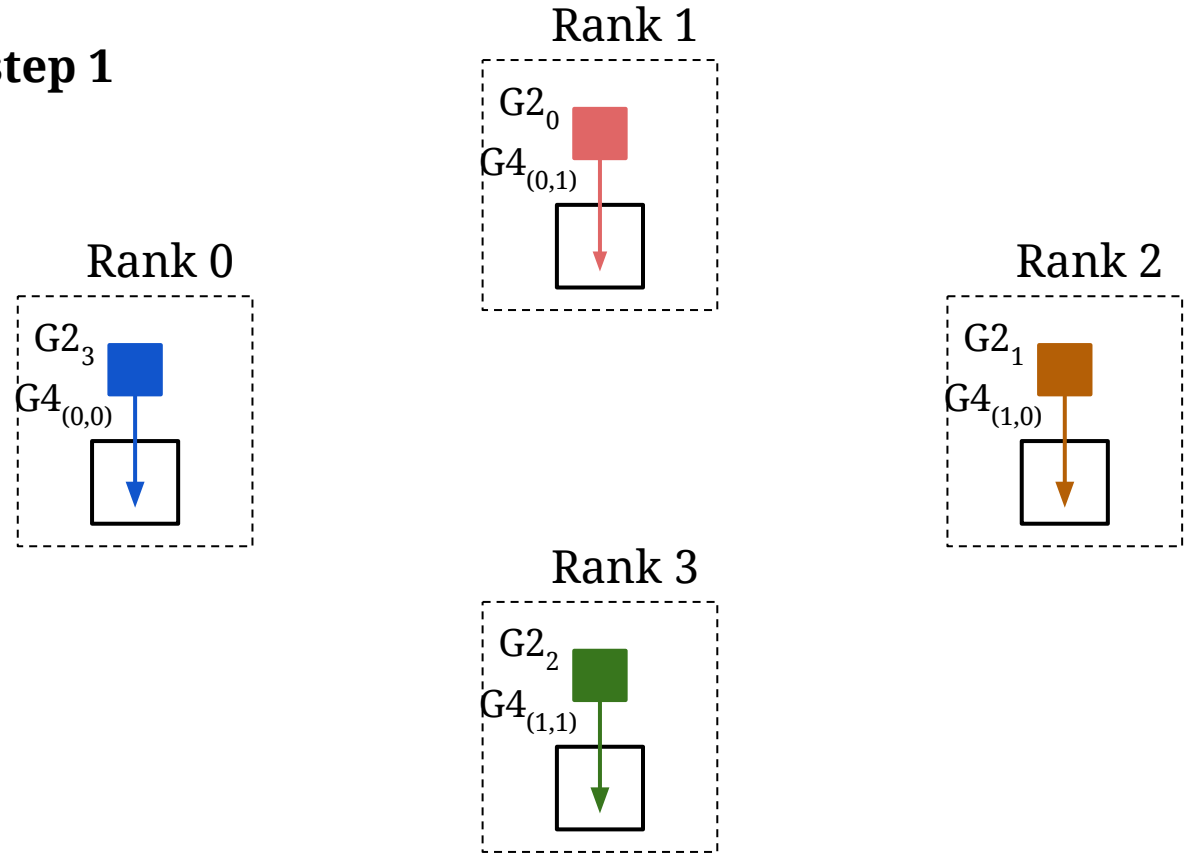
Pipelined Ring Algorithm



code: https://github.com/weilewei/Ring_example_MPI_CUDA/blob/master/G2_ring.cpp

Pipelined Ring Algorithm

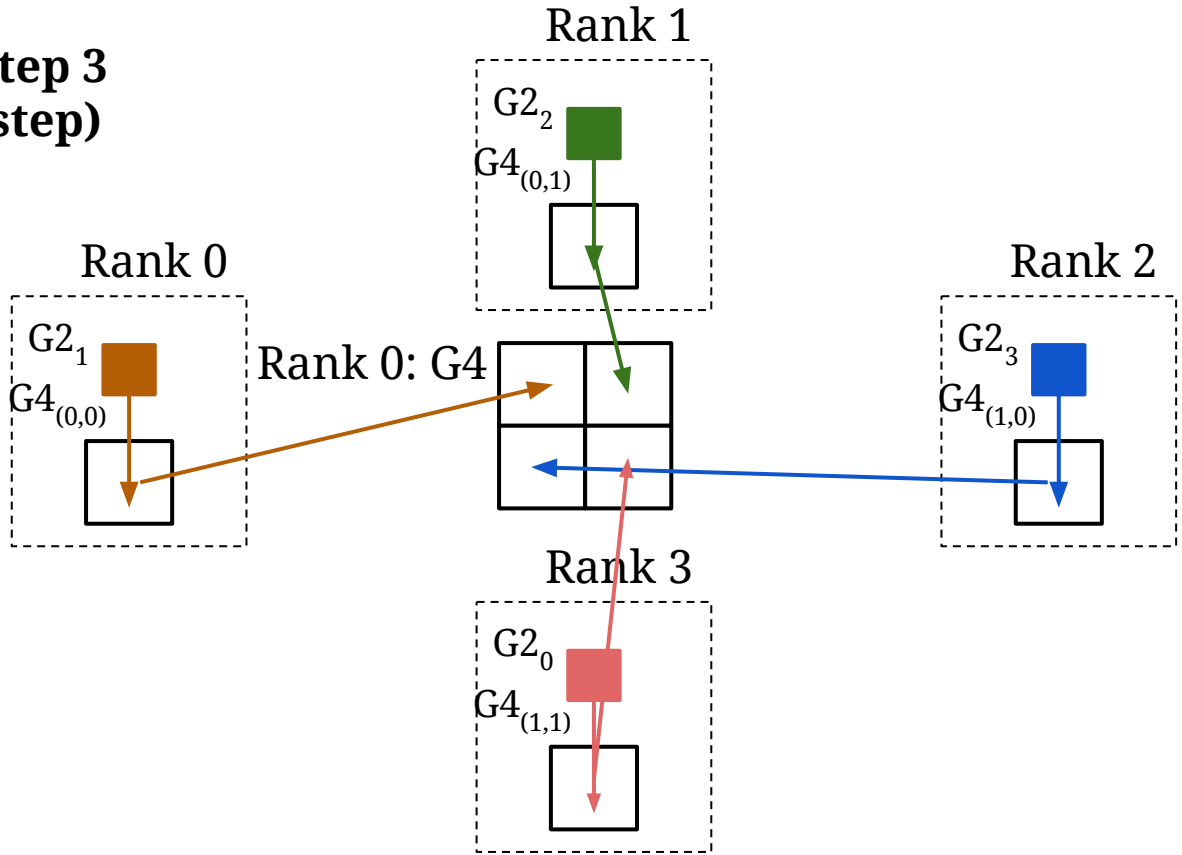
Time-step 1



code: https://github.com/weilewei/Ring_example_MPI_CUDA/blob/master/G2_ring.cpp

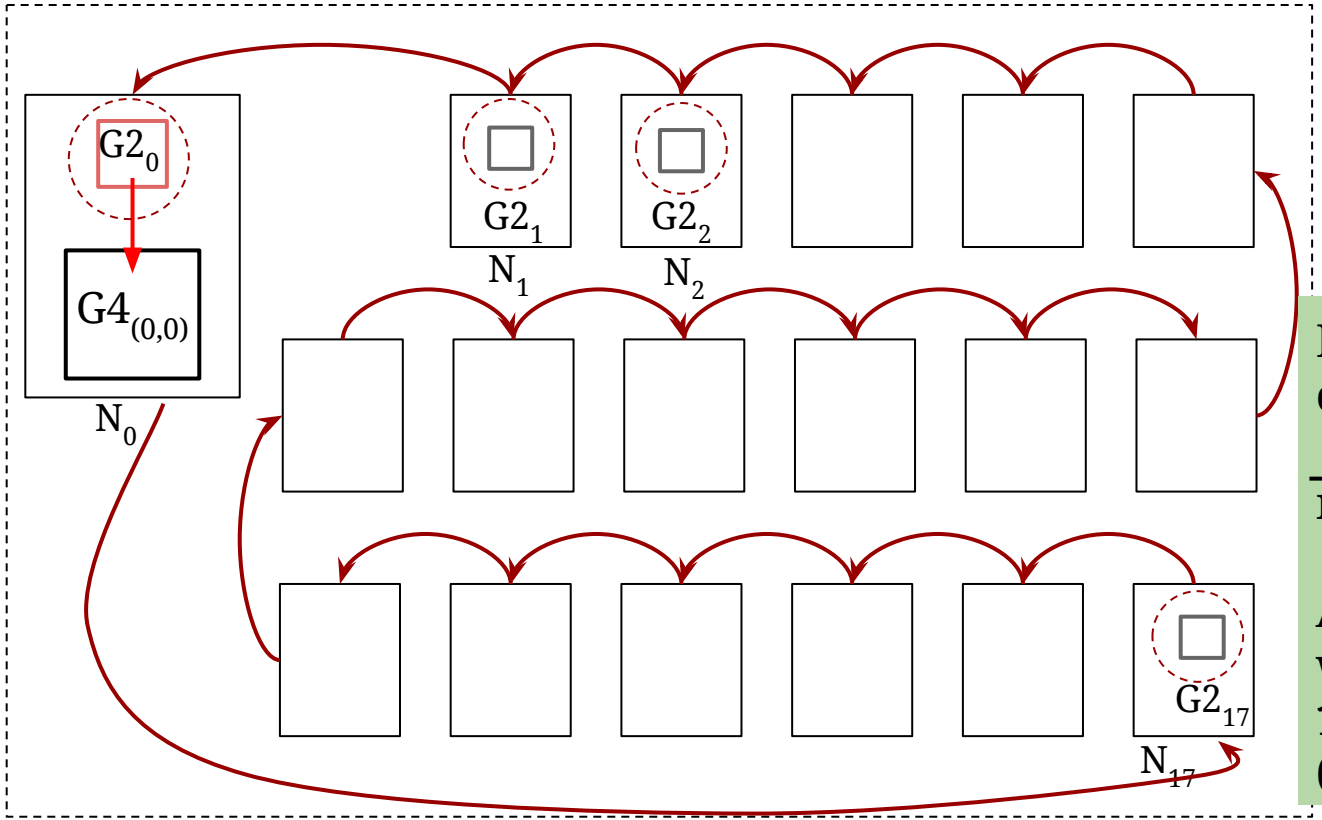
Pipelined Ring Algorithm

Time-step 3 (final step)



code: https://github.com/weilewei/Ring_example_MPI_CUDA/blob/master/G2_ring.cpp

Enabling MORE science



Each G4 cell/rank only carries

$$\frac{1}{\text{no. of GPUs}} * 12 \text{ GB}$$

Amount of GPU memory we can tap into:
144x more if needed
(6*16GB*18→ 1.7 TB)

Ring Fashion

Cabinet 0 (18 nodes)

Conclusion & Future Work

- Threading abstraction w/ HPX light-weight threads
- **DCA++ w/ GPUDirect:**
  - Conducted NVLink bandwidth measurement
  - Future work
    - To apply GPUDirect in DCA++ to solve memory bound issue
    - Wrap GPUDirect into HPX future

Pipelined Ring Algorithm using HPX

HPX-MPI

```
24
25  hpx::mpi::enable_user_polling enable_polling;
26  hpx::mpi::executor exec(MPI_COMM_WORLD);
27
```

. . .

```
69  for(int icount=0; icount < (mpi_size-1); icount++)
70  {
71  // encode the originator rank in the message tag as tag = 1 + originator_irank
72  int originator_irank = MOD(((rank-1)-icount + 2*mpi_size), mpi_size);
73  int recv_tag = 1 + originator_irank;
74  recv_tag = 1 + MOD(recv_tag-1, MPI_TAG_UB); // just to be safe, then 1 <= tag <= MPI_TAG_UB
75
76  hpx::future<int> f_send = hpx::async(exec, MPI_Irecv, recvbuff_G2, n_elems, MPI_FLOAT, left_neighbor,
    recv_tag);
77  hpx::future<int> f_recv = hpx::async(exec, MPI_Isend, sendbuff_G2, n_elems, MPI_FLOAT, right_neighbor,
    send_tag);
78
79  f_recv.get();
80  CudaMemoryCopy(G2, recvbuff_G2, n_elems);
81  update_local_G4(G2, G4, rank, n_elems);
82  f_send.get();
83
84  // get ready for send
85  CudaMemoryCopy(sendbuff_G2, G2, n_elems);
86  send_tag = recv_tag;
87  }
```

MPI

```
19
61  for(int icount=0; icount < (mpi_size-1); icount++)
62  {
63  // encode the originator rank in the message tag as tag = 1 + originator_irank
64  int originator_irank = MOD(((rank-1)-icount + 2*mpi_size), mpi_size);
65  int recv_tag = 1 + originator_irank;
66  recv_tag = 1 + MOD(recv_tag-1, MPI_TAG_UB); // just to be safe, then 1 <= tag <= MPI_TAG_UB
67
68  MPI_CHECK(MPI_Irecv(recvbuff_G2, n_elems, MPI_FLOAT, left_neighbor, recv_tag, MPI_COMM_WORLD,
    &recv_request));
69  MPI_CHECK(MPI_Isend(sendbuff_G2, n_elems, MPI_FLOAT, right_neighbor, send_tag, MPI_COMM_WORLD,
    &send_request));
70
71  MPI_CHECK(MPI_Wait(&recv_request, &status));
72  CudaMemoryCopy(G2, recvbuff_G2, n_elems);
73  update_local_G4(G2, G4, rank, n_elems);
74  MPI_CHECK(MPI_Wait(&send_request, &status)); // wait for sendbuf_G2 to be available again
75
76  // get ready for send
77  CudaMemoryCopy(sendbuff_G2, G2, n_elems);
78  send_tag = recv_tag;
79  }
```

code: https://github.com/weilewei/Ring_example_MPI_CUDA/blob/hpx_mpi_async/G2_ring_hpx.cpp

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