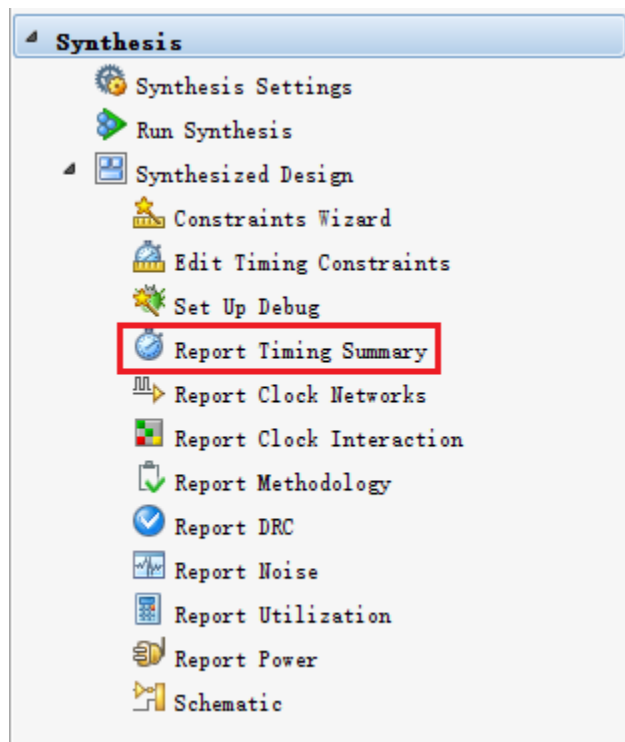


时序报告提交说明

参考课本 4.3 节或 PDF 文件“时序约束和逻辑分析仪使用”生成时序报告，并按下图的操作将结果保存为“学号_姓名_timing_report.txt”文件后，与代码、后仿真实验视频等按照文档“2022 年《计算机组成原理课程设计》考核”的要求，提交到助教邮箱。

时序报告生成步骤：

1. 进入时序报告生成入口



2. 设定保存路径等信息

Report Timing Summary

Generate a timing summary to understand if the design met timing.

Results name:

Options | Advanced | Timer Settings

Report

Path delay type:

☒ Report unconstrained paths

☐ Report datasheet

Path Limits

Maximum number of paths per clock or path group:

Maximum number of worst paths per endpoint:

Path Display

Display paths with slack less than: ☒ Use default (1e+30)

Significant digits:

Command: `constrained -check_timing_verbose -max_paths 10 -input_pins -name timing_3 -file D:/Xilinx/DOC/cpu_clkip/cpu31/timing_report.txt`

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Report Timing Summary

Generate a timing summary to understand if the design met timing.

Results name:

Options | **Advanced** | Timer Settings

Report

☐ Report from cell:

☒ Show input pins in path

☐ Report unique pins

File Output

☒ Write results to file:

☒ Overwrite ☐ Append

Miscellaneous

☐ Ignore command (quiet mode)

☐ Suspend message limits during command execution

Command: `constrained -check_timing_verbose -max_paths 10 -input_pins -name timing_1 -file D:/Xilinx/DOC/cpu_clkip/cpu31/timing_report.txt`

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3. 设定配置

Report Timing Summary

Generate a timing summary to understand if the design met timing.

Results name: timing_3

Options

Advanced

Timer Settings

Interconnect: actual (most accurate of routed and estimated delays)

Speed grade: -1 (default)

Multi-Corner Configuration

Corner name	Delay type
Slow	min_max
Fast	min_max

☐ Disable flight delays

Command: constrained -check_timing_verbose -max_paths 10 -input_pins -name timing_3 -file D:/Xilinx/DOC/cpu_clkip/cpu31/timing_report.txt

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?

OK

Cancel

Timing Summary - timing_1

Timing Summary - timing_2

Timing Summary - timing_1(1)