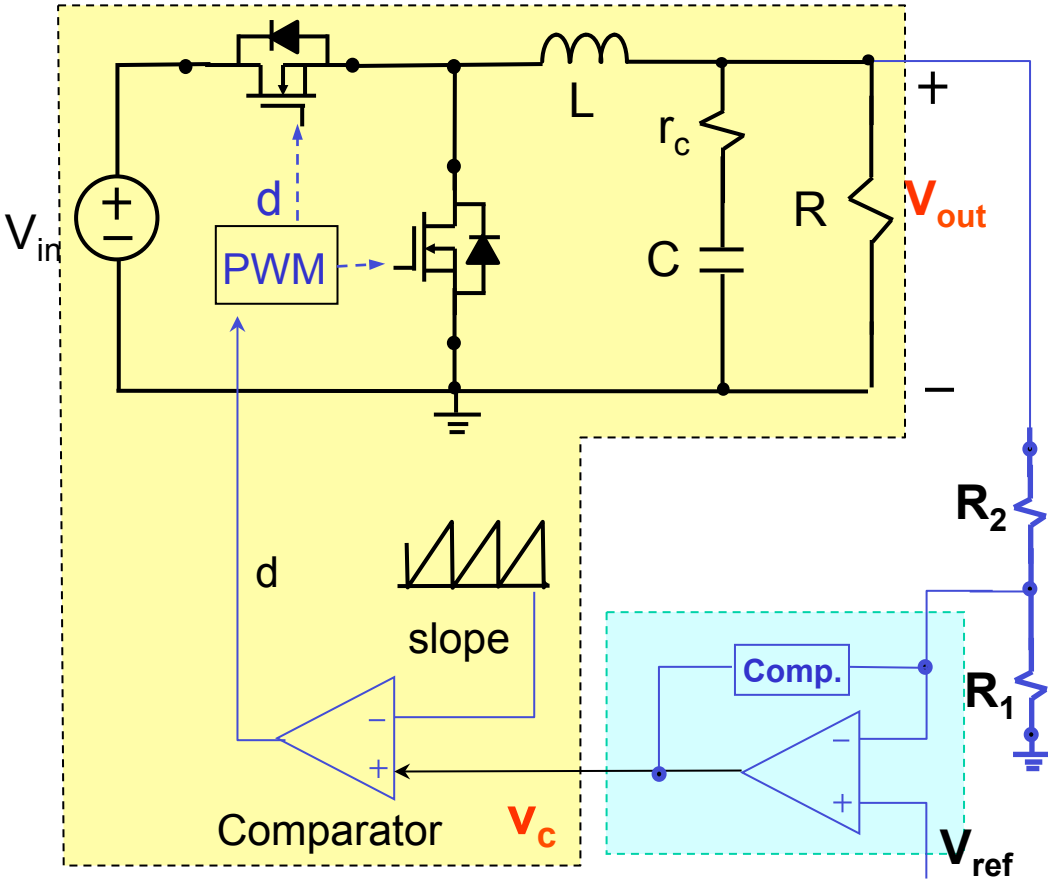
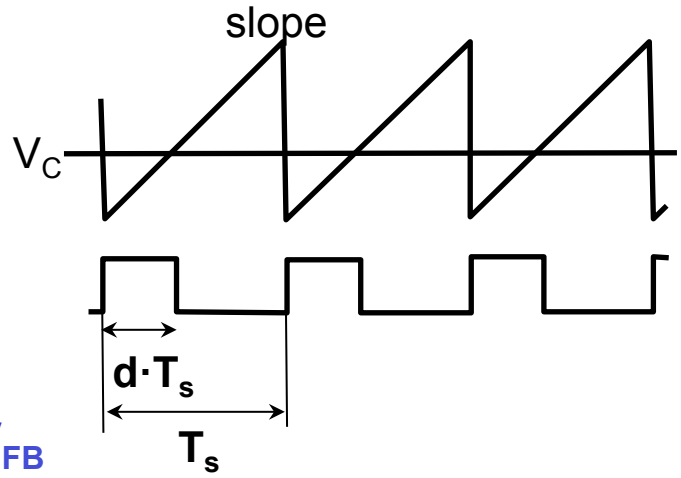
Loop Compensation Basics
Buck Converter CCM

More Details : AN76

Voltage-Mode Control

Voltage-Mode Controlled Buck Converter



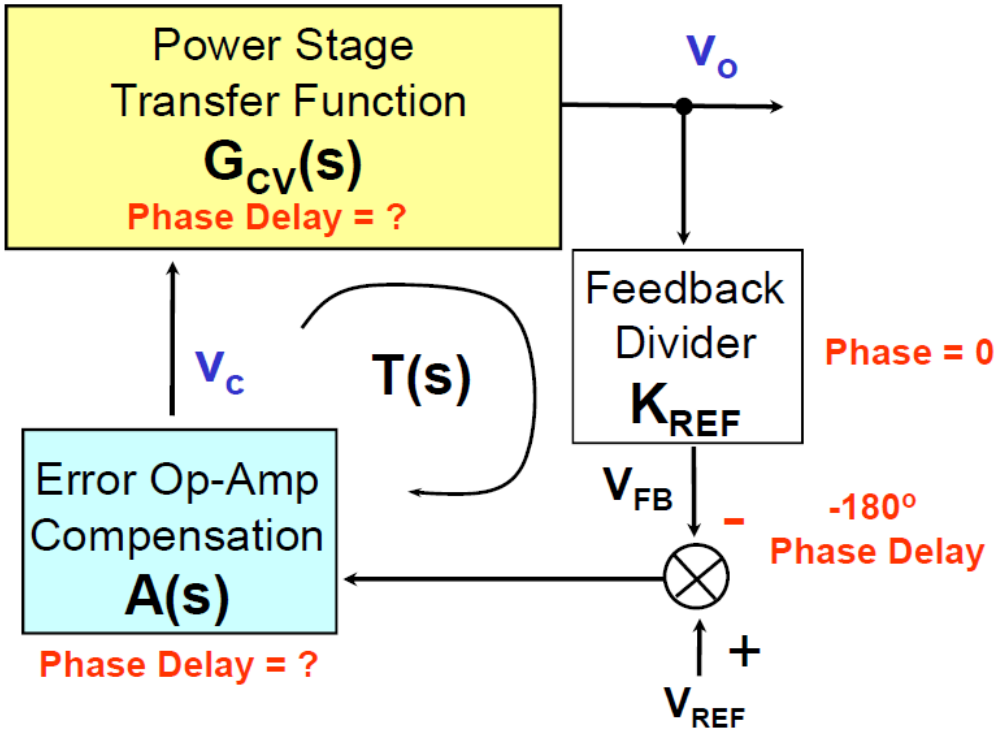


$d = k \cdot V_c$

Power Stage
Control-to-output

Error Amp
Compensation A(s)

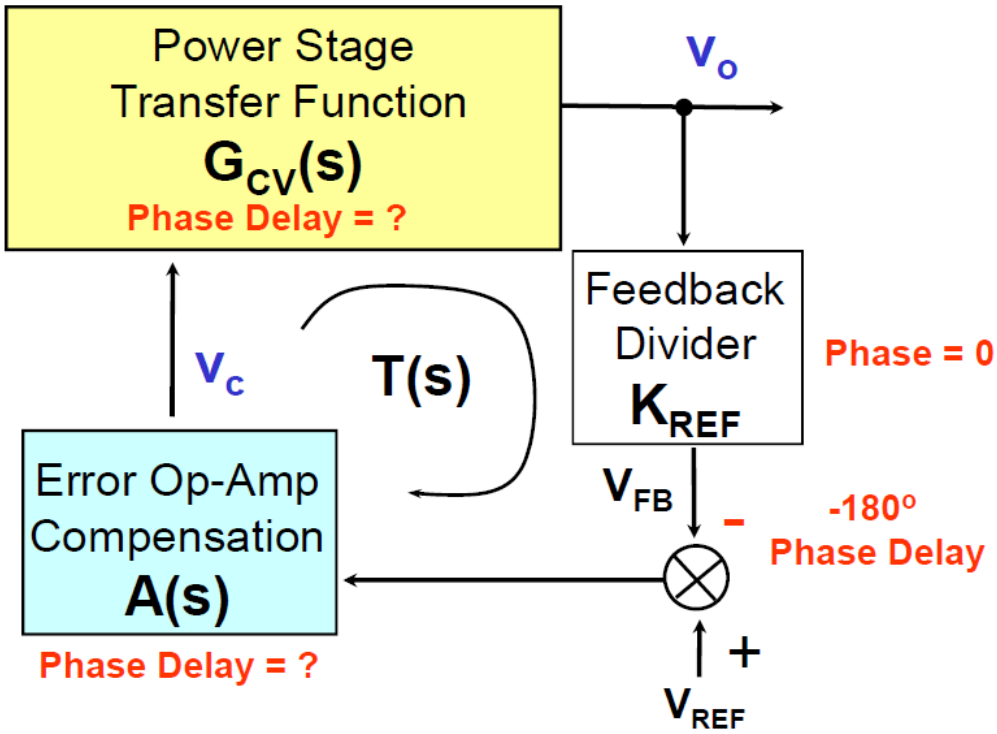
Control Block Diagram and Loop Gain



- Loop Gain: $T(s) = G_{CV}(s) \cdot K_{REF} \cdot A(s)$
- Bandwidth: crossover frequency f_c @ loop gain $|T(s)|=1$
- Stability: Total phase > -360° at crossover frequency

  Total Phase = $(-180° + \varphi[A(s)] + \varphi[G_{CV}(s)])_{f=fc} > -360°$

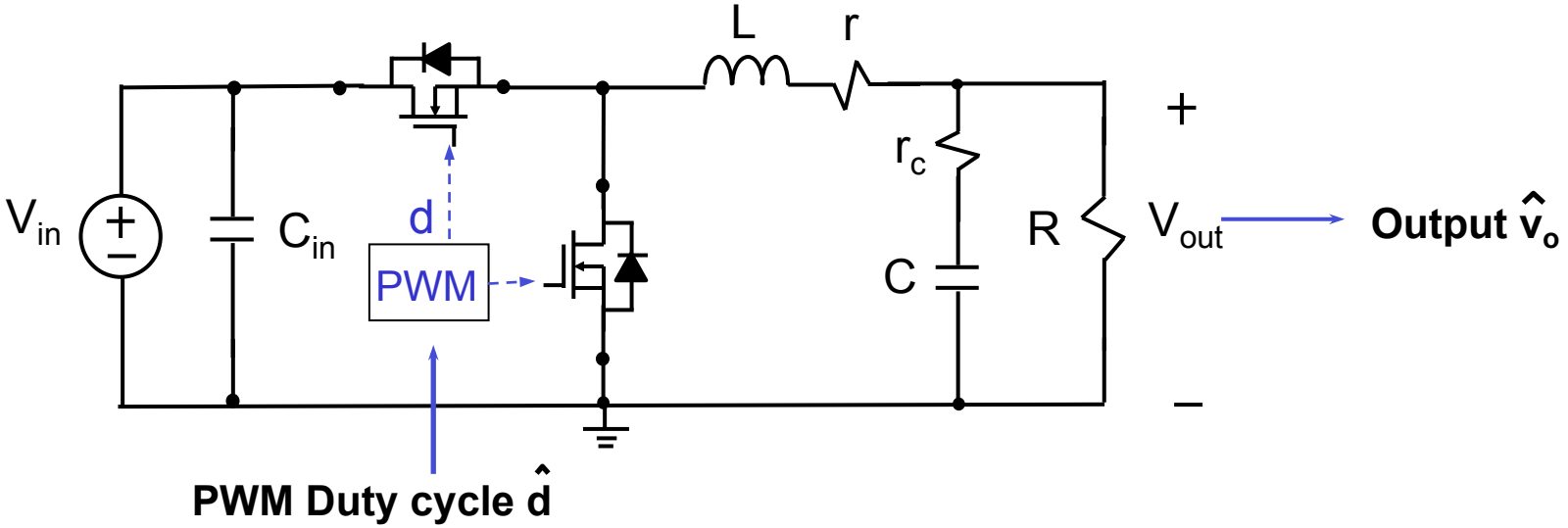
Control Block Diagram and Loop Gain



Design Targets:

- Regulation accuracy, line rejection, Z_{OUT}: $|T(s)| >> 1$ for $f < f_c$
- Bandwidth: high bandwidth for fast transient response
- Stability: phase margin > 45°

Buck Converter Power Stage Control-to-Output



Control-to-output transfer function:

$$G_{dv}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{V_{in} \cdot \left(1 + \dfrac{s}{\omega_{z\_ESR}}\right)}{1 + \dfrac{s}{\omega_{o\_p} \cdot Q} + \dfrac{s^2}{\omega_{o\_p}^2}}$$

ESR Zero:

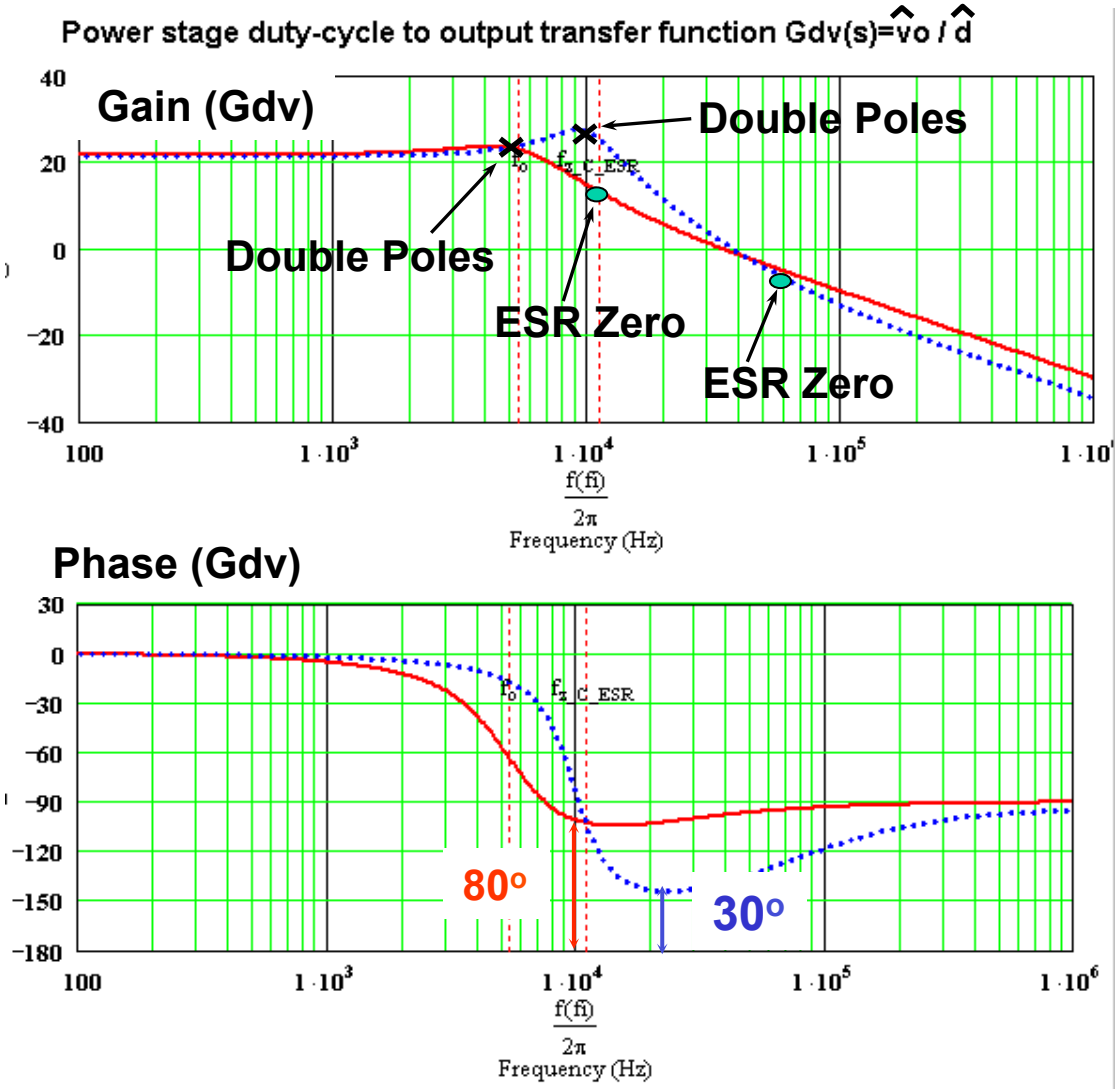
$$f_{Z\_ESR} = \frac{1}{2\pi} \cdot \frac{1}{r_C \cdot C}$$

Resonant double poles:

$$f_{o\_p} \approx \frac{1}{2\pi} \cdot \frac{1}{\sqrt{L \cdot C}}$$

- 1 zero, 2 poles system.

Power Stage Transfer Function With Voltage Mode Control



1 — **Reference design**
3X470uF Kemet Tantalum cap.
r_C=30mΩ

2 ····· **Customer design**
2 X 220uF Panasonic SP cap.
r_C=12mΩ

Double Poles: -180°
ESR Zero: +90°

Phase delay is a strong function of output capacitor ESR

ESR variation : tolerance, temperature, aging, …

Loop Compensation Design Of Voltage Mode Control

Voltage Loop Compensation Design

1. Select desired crossover frequency f_C

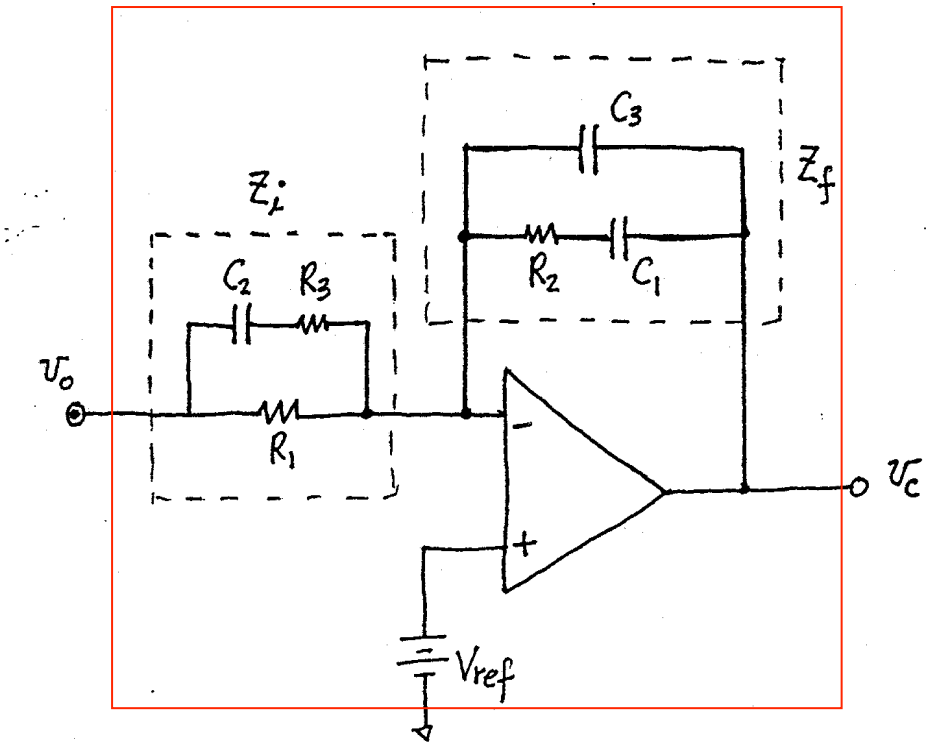
$$f_C(\min) > 3 \cdot f_{0\_p}(LC) \quad f_C(\max) < \frac{f_{SW}}{5}$$

2. Loop compensation – type 3 compensation network

- 1 pole, low frequency integrator for high DC gain
- 2 zeros located around L-C resonant double poles
- 2 high-frequency poles:
  - to attenuate high frequency noise
  - to ensure the magnitude of the loop gain keeps decreasing after the 0dB crossover

Type 3 Compensation Network

(Typical 3-Pole, 2-Zero system in Voltage Mode Control)



$$\frac{\hat{v}_c}{\hat{v}_o} = -\frac{Z_f}{Z_i}$$

$$Z_i = R_1 // \left(\frac{1}{sC_2} + R_3\right)$$

$$Z_f = \frac{1}{sC_3} // \left(\frac{1}{sC_1} + R_2\right)$$

$$\boxed{\frac{\hat{v}_c}{\hat{v}_o} = -\frac{\omega_I}{s}\frac{\left(1+s/\omega_{Z1}\right)\left(1+s/\omega_{Z2}\right)}{\left(1+s/\omega_{P1}\right)\left(1+s/\omega_{P2}\right)}}$$

where:

$$\omega_{Z1} = \frac{1}{R_2C_1}, \quad \omega_{Z2} = \frac{1}{(R_1+R_3)C_2} \sim \frac{1}{R_1C_2}$$

R1>>R3 C1>>C3

$$\omega_I = \frac{1}{R_1(C_1+C_3)} \sim \frac{1}{R_1C_1}$$

$$\omega_{P1} = \frac{1}{R_3C_2}, \quad \omega_{P2} = \frac{1}{R_2 \cdot \frac{C_1C_3}{C_1+C_3}} \sim \frac{1}{R_2C_3}$$

Type 3 Compensation Network

(Typical 3-Pole, 2-Zero system in Voltage Mode Control)

$$\frac{\hat{v}_c}{\hat{v}_o} = -\frac{\omega_I}{s}\frac{\left(1+s/\omega_{Z1}\right)\left(1+s/\omega_{Z2}\right)}{\left(1+s/\omega_{P1}\right)\left(1+s/\omega_{P2}\right)}$$

Quick recommendations :

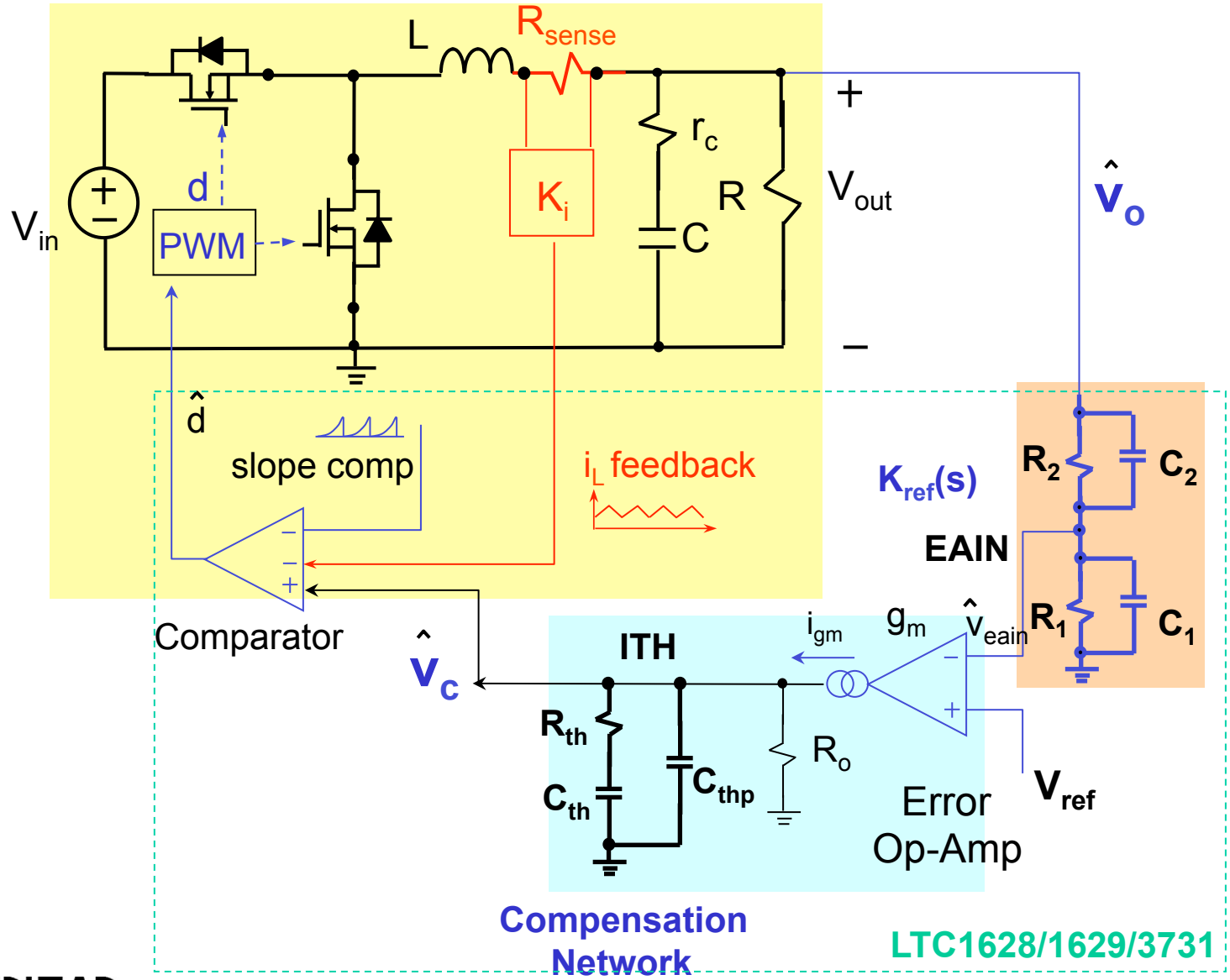
- $f_{p1} = f_{z\_ESR}$
- $f_{p2} \sim f_c$ to 10 x f_c
- $f_{z1} = f_{z2} = f_{0\_LC}$
- f_I to get desired crossover frequency f_c

Pros and Cons of Voltage Mode Regulators

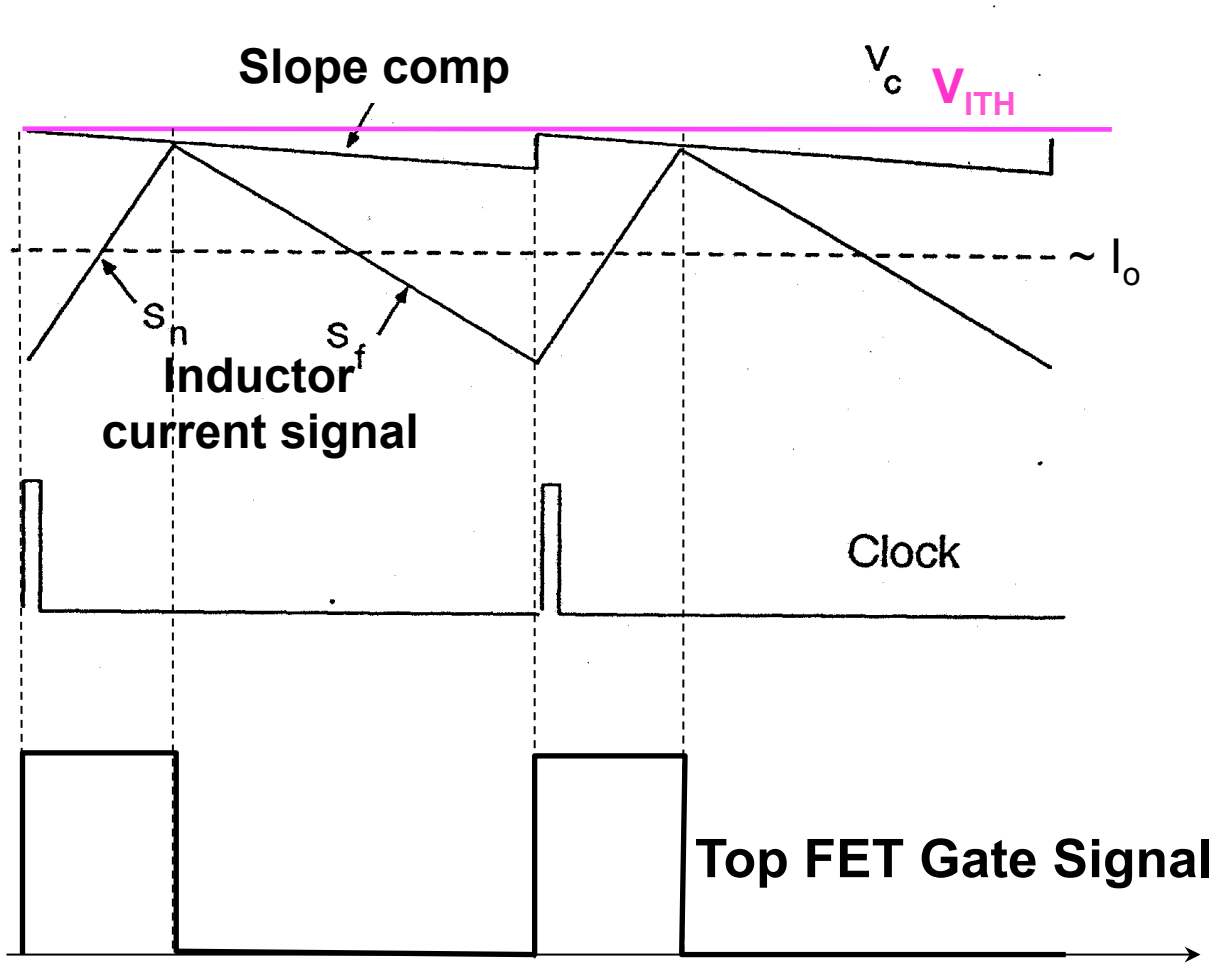
- **Pros:**
  - Don't need dedicated current sensing R : high efficiency and low cost solution
- **Cons:**
  - Loop gain is a function of Vin
    - Solution: Vin feed-forward compensation
  - Loop gain is a function of output ESR
    - Need carefully loop compensation design
  - Need to compensate for double resonant pole
  - The current sensing / limit is slow and not accurate
  - Need external loop for current sharing if two supplies / phases are in parallel

Current Mode Control

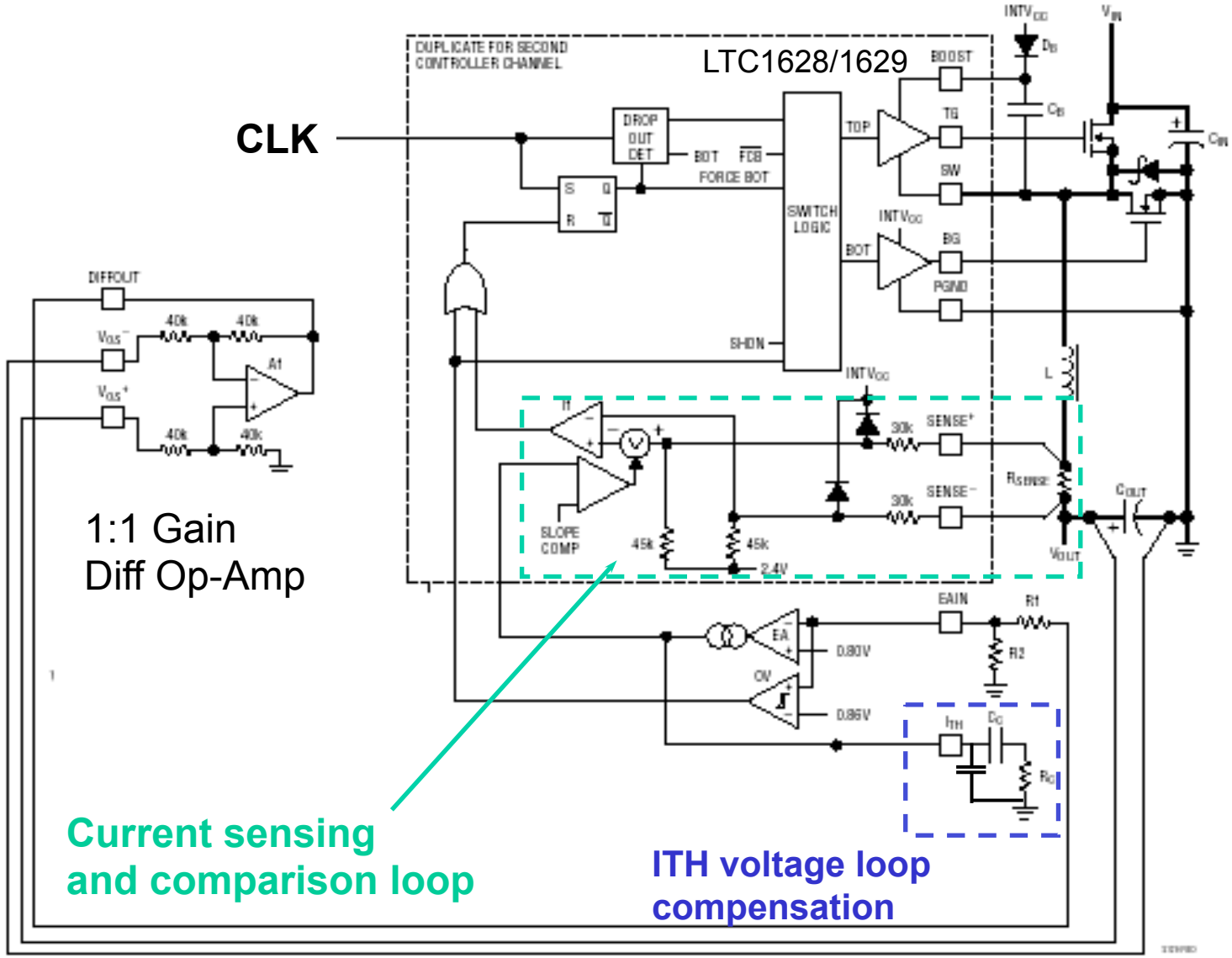
Simplified Block Diagram of Current Mode IC



Peak Current Mode Control

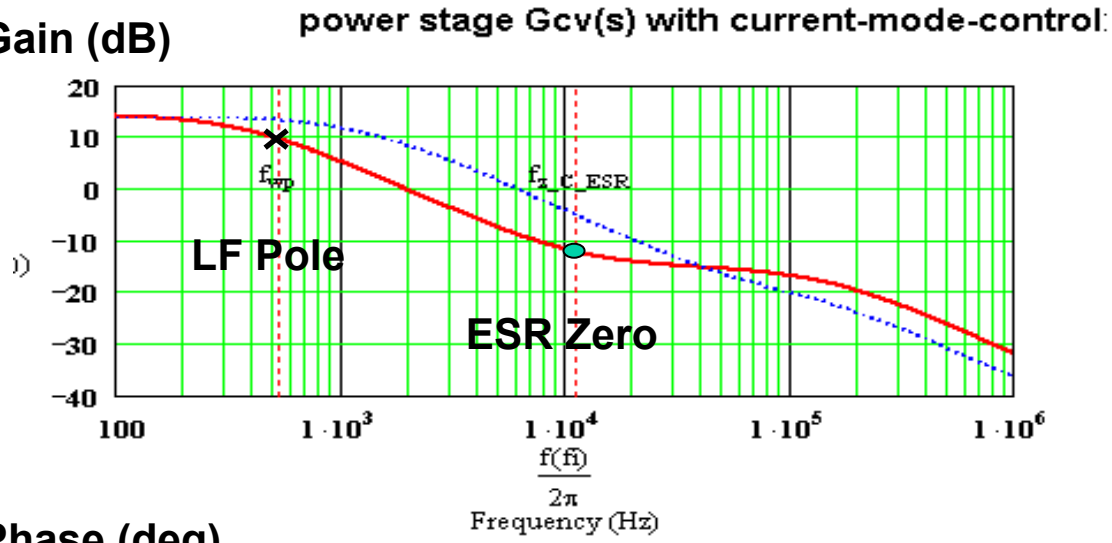


LTC's Current-Mode Controller Block Diagram

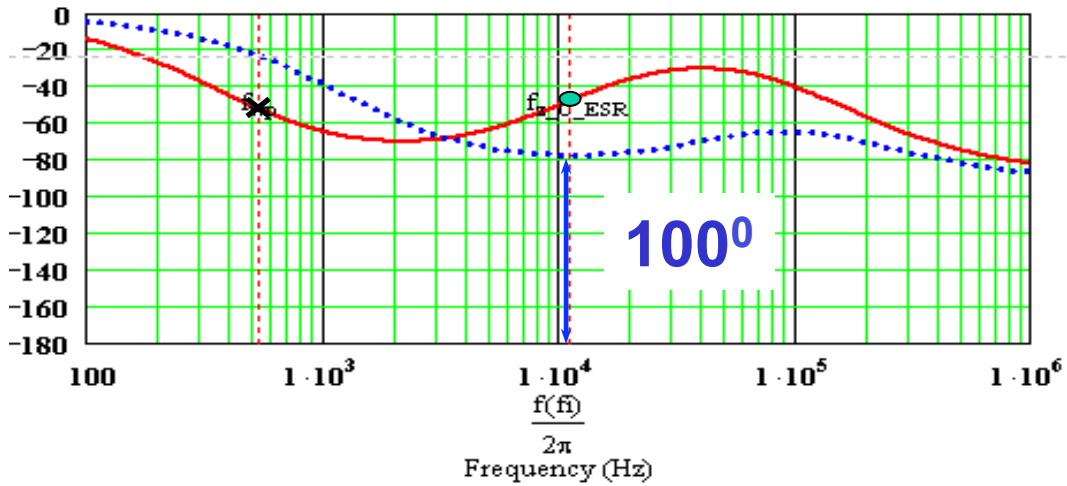


Power Stage Transfer Function With Current Mode Control

Gain (dB)



Phase (deg)

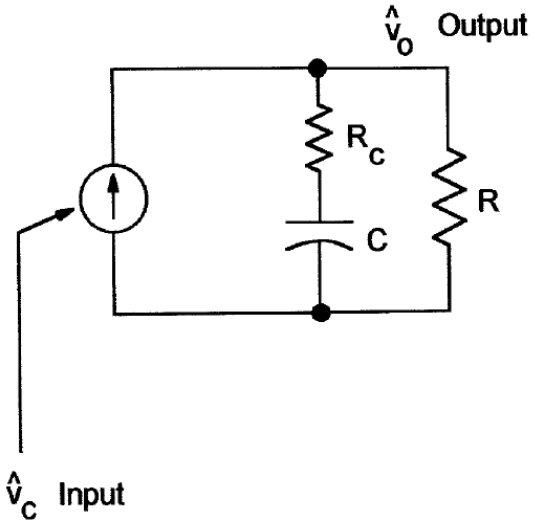


1 — Reference design
3X470uF Kemet cap.
r_C=30mΩ

2 ····· Customer design
2 X 220uF Panasonic cap.
r_C=12mΩ

- Reduce phase delay with different output capacitors
- Stable system with reduced output capacitors / cost.

Buck Converter Power Stage Control-to-Output



Simple small-signal model : current source feeding the load

Slope comp to avoid subharmonic oscillation not modeled

Control-to-output transfer function:

$$G_{cv}(s) = \frac{\hat{v}_o}{\hat{v}_c} = K \frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_p})}$$

$$f_Z = \frac{1}{2\pi} \cdot \frac{1}{R_C \cdot C}$$

$$f_P = \frac{1}{2\pi} \cdot \frac{1}{R \cdot C}$$

- 1 zero, 1 pole system.

Pros and Cons of Current Mode Control

- **Pros:**
  - **Accurate / fast cycle-by-cycle current limit**
  - **True soft-start of inductor current**
  - **Easy to parallel phases / converters for high current**
  - **Accurate / fast current sharing**
  - **Very good line ripple rejection**
  - **Simple loop compensation with wide range of COUT, including Ceramic**
  - **High reliability**
- **Cons:**
  - **Need current sensing Rsense or RDSON or DCR, noise immunity**
  - **Subharmonic instability (ramp compensation needed)**
  - **Duty cycle limitation (t_{ON}, t_{OFF}) due to current sensing delay**
  - **Higher output impedance at low frequency**

Loop Compensation Design Of Current Mode Control

Voltage Loop Compensation Design

1. Select desired cross over frequency f_C

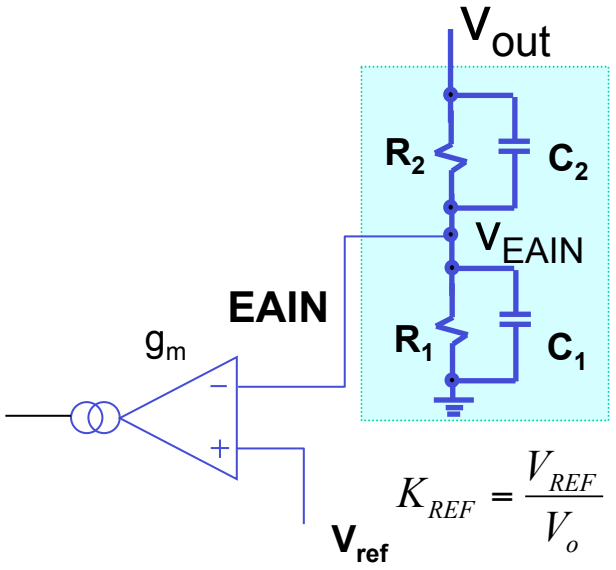
$$f_{C(\max)} < \frac{f_{SW}}{5}$$

2. Choose desired loop phase margin:

Phase margin > 45° for buck converter

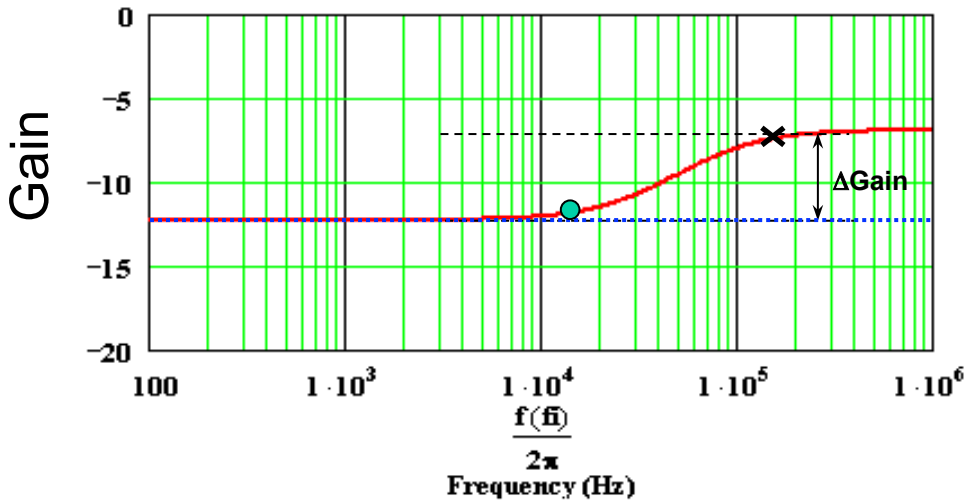
3. Choose optimum values of the resistor divider network $K_{REF}(s)$ and I_{TH} compensation network A(s)

Feedback Voltage Divider and Phase Boost

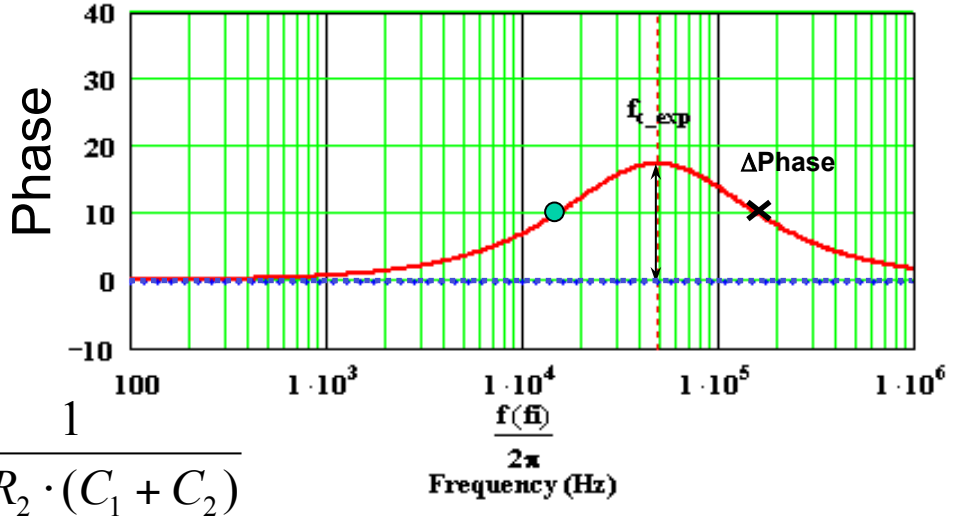


$K_{ref}(s)$

$$K_{REF} = \frac{V_{REF}}{V_o} = \frac{R_1}{R_1 + R_2}$$



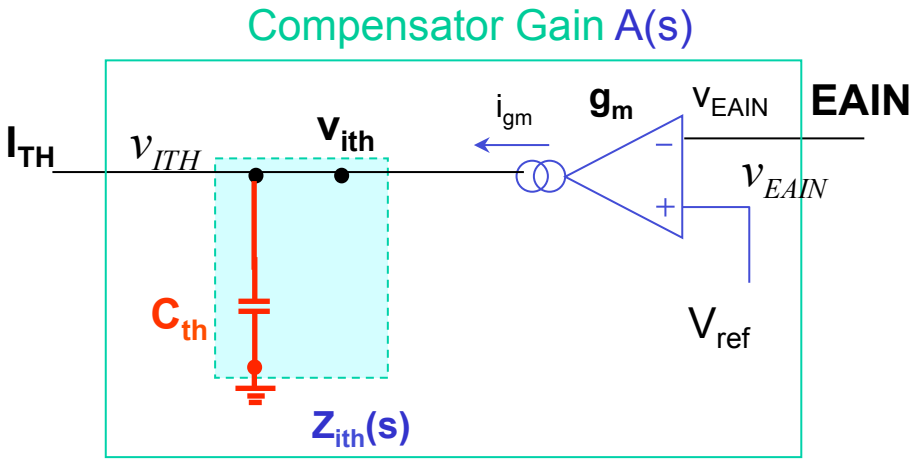
$$K_{REF}(s) = \frac{v_{EAIN}(s)}{v_o(s)} = K_{REF} \cdot \frac{1 + \frac{s}{2\pi \cdot f_{z\_ref}}}{1 + \frac{s}{2\pi \cdot f_{p\_ref}}}$$



$$f_{z\_ref} = \frac{1}{2\pi \cdot R_2 \cdot C_2} \qquad f_{p\_ref} = \frac{1}{K_{REF}} \cdot \frac{1}{2\pi \cdot R_2 \cdot (C_1 + C_2)}$$

C_1 and C_2 provide phase boost around the crossover frequency.

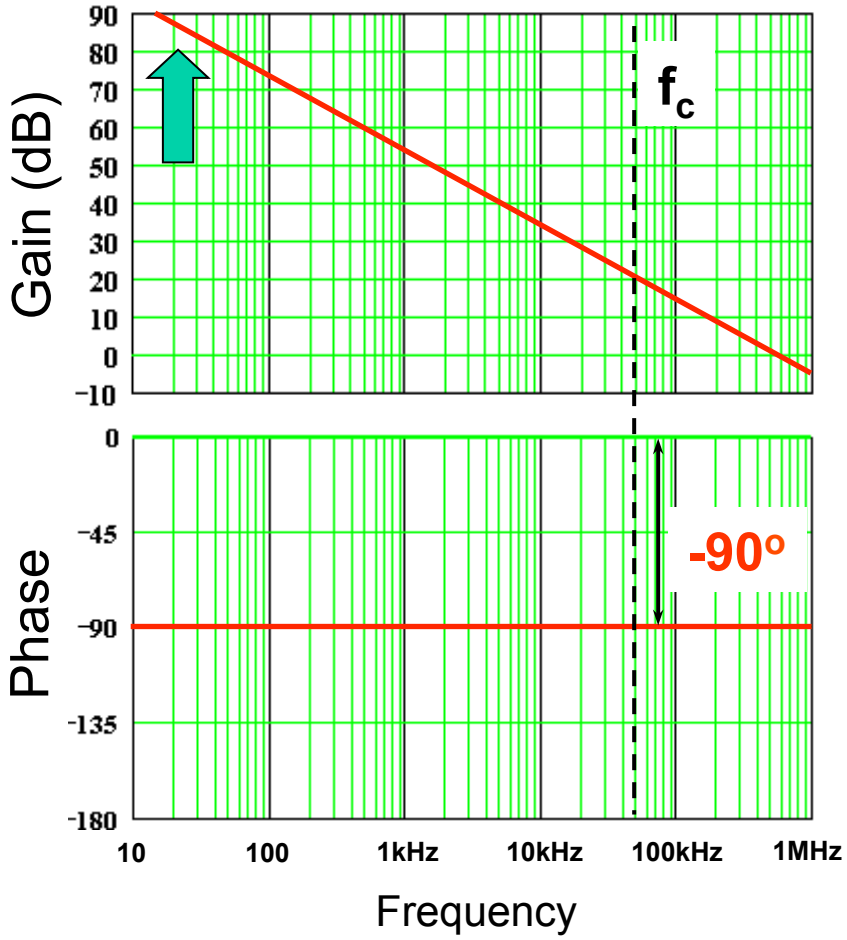
I_{TH} Compensation – High DC Gain



$$A(s) = \frac{v_{ITH}(s)}{v_{EAIN}(s)} = -g_m \cdot (Z_{ith}(s))$$

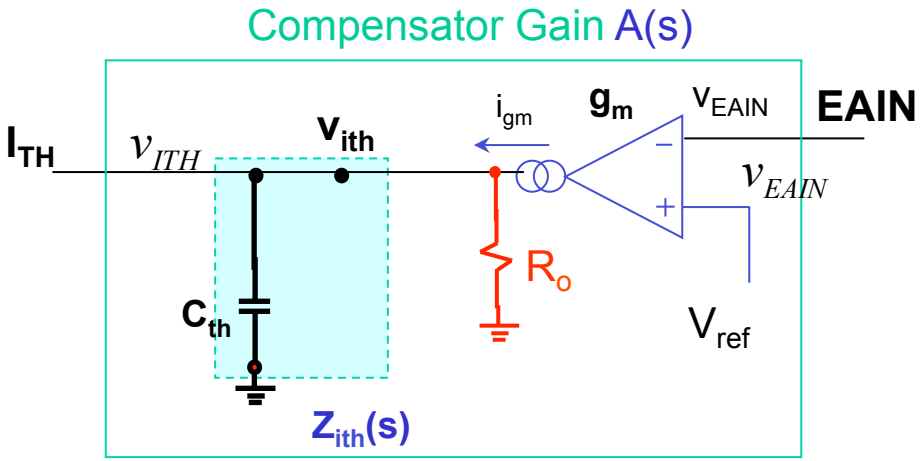
1. Simple Integrator:

$$A(s) = -g_m \cdot \frac{1}{C_{th} \cdot s}$$



- High low frequency gain for accurate DC Vout regulation
  - -90° phase delay @ expected cross-over frequency f_C

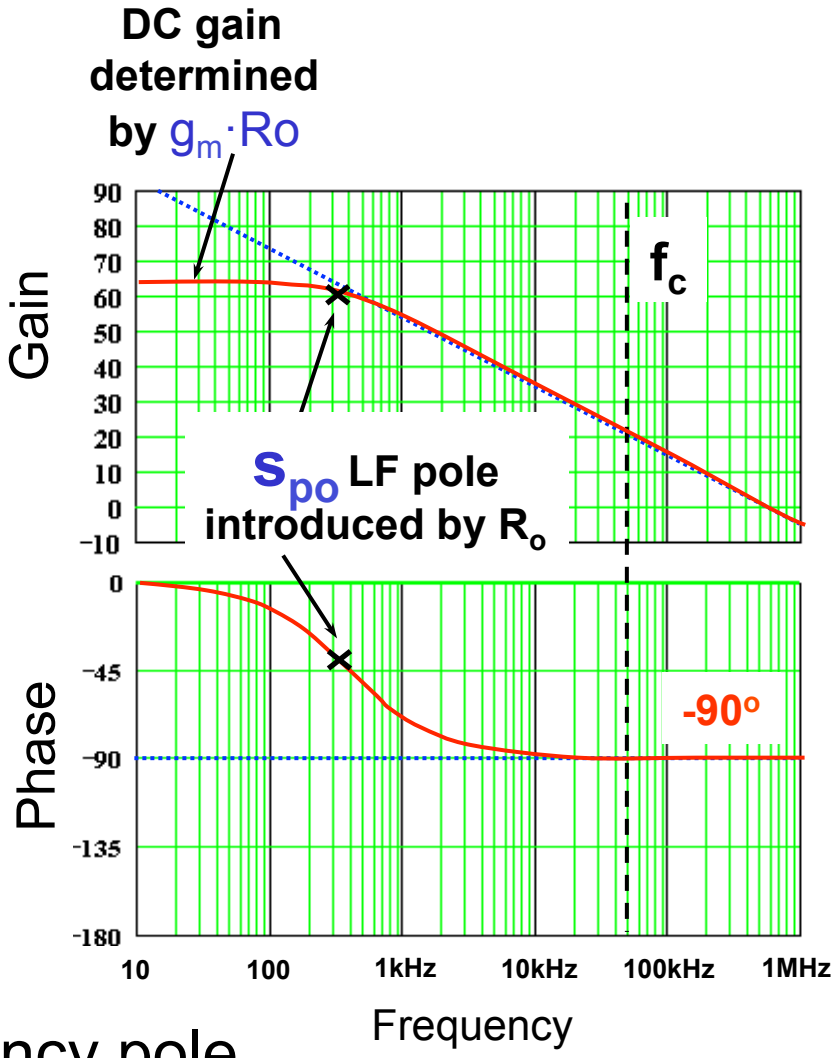
I_{TH} Compensation – LF Pole



$$A(s) = \frac{v_{ITH}(s)}{v_{EAIN}(s)} = -g_m \cdot (Z_{ith}(s))$$

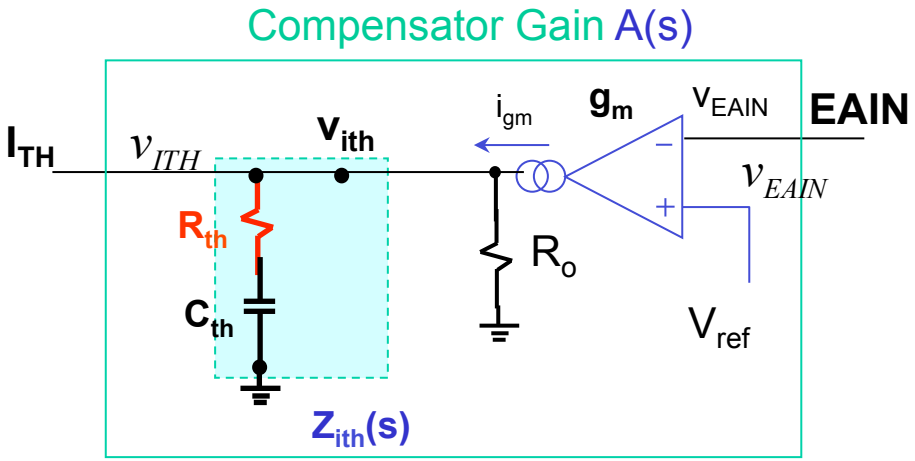
2. Simple Integrator with g_m Op-Amp Output Impedance R_o:

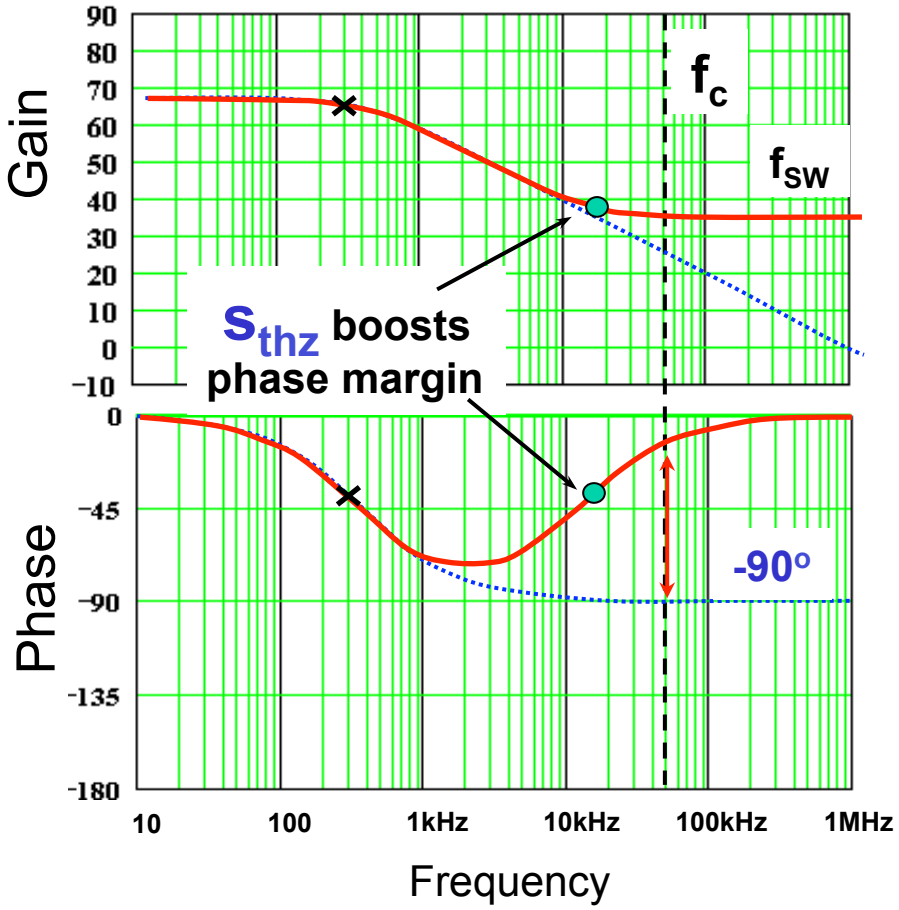
$$A(s) = -g_m \cdot R_o \cdot \frac{1}{(1 + \frac{s}{s_{po}})} \qquad s_{po} = \frac{1}{R_o \cdot C_{th}}$$



- g_m Op-Amp adds a low frequency pole
- Still -90° phase delay @ f_C

I_{TH} Compensation – Add Zero for Phase





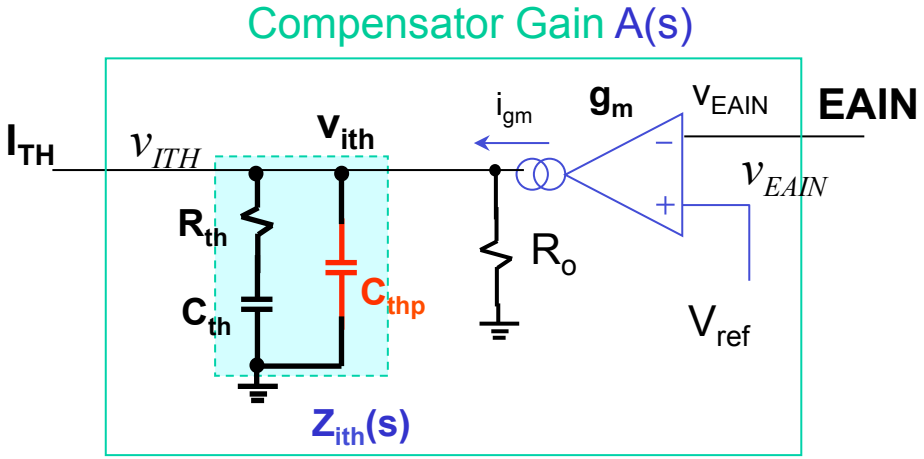
3. Add zero for Phase Compensation at cross over frequency:

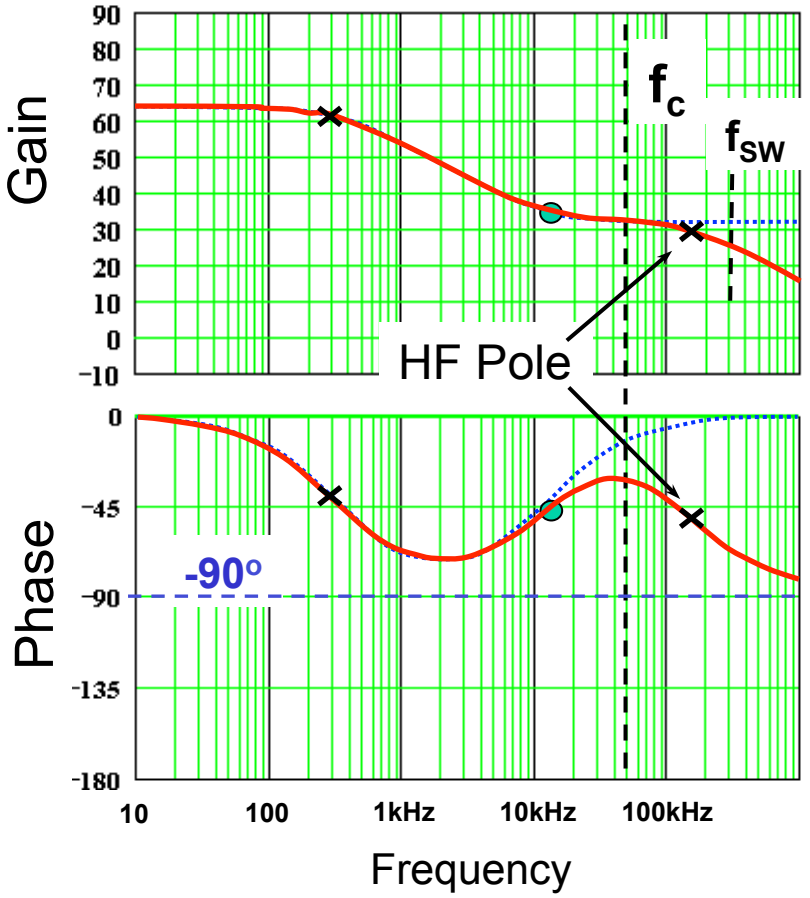
$$A(s) = -g_m \cdot R_o \cdot \frac{1 + \frac{s}{s_{thz}}}{(1 + \frac{s}{s_{po}})}$$

$$s_{thz} = \frac{1}{R_{th} \cdot C_{th}}$$

- Adds a zero before / around f_C to boost up phase
  - Increased gain @ high frequency

I_{TH} Compensation – HF Pole





4. Add a high frequency pole to attenuate high frequency noise:

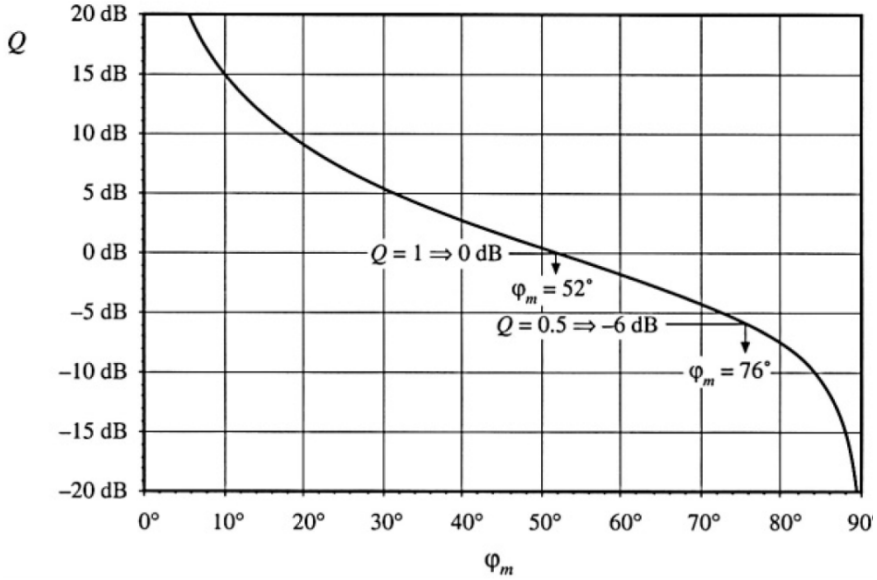
$$A(s) = -g_m \cdot R_o \cdot \frac{1 + \frac{s}{s_{thz}}}{(1 + \frac{s}{s_{po}}) \cdot (1 + \frac{s}{s_{thp}})}$$

$$s_{thp} = \frac{1}{R_{th} \cdot \frac{C_{th} \cdot C_{thp}}{C_{th} + C_{thp}}} \approx \frac{1}{R_{th} \cdot C_{thp}} \qquad (C_{th} >> C_{thp})$$

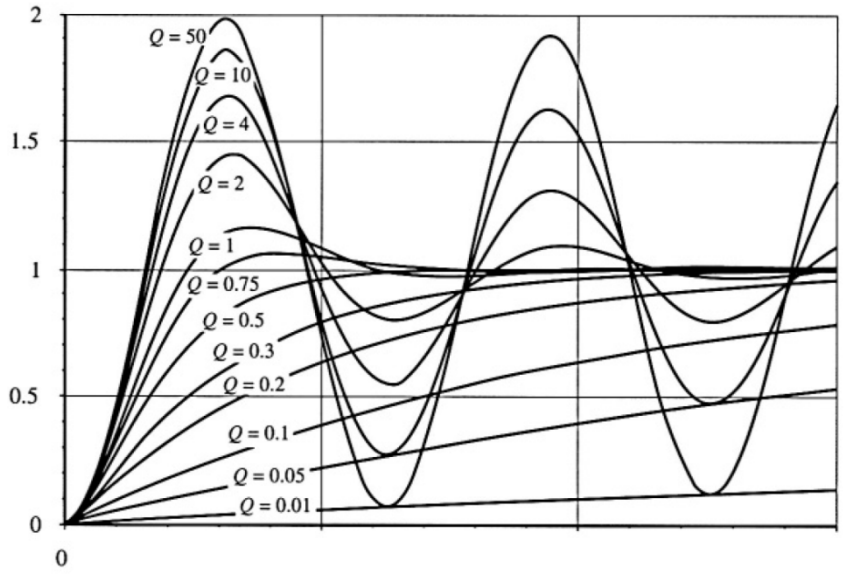
How much phase margin is necessary?

For a second-order system (good approximation near fc)

Closed-loop peaking factor Q vs. loop-gain phase margin φm



Unit-step response for various values of Q



Q<0.5 over-damping
Q=0.5 critical damping
Q>0.5 under-damping

No overshoot => Q≤0.5 => φm≥76°

How much phase margin is necessary?

Changes in line, load and temperature tend to degrade phase margin from the nominal value.

For commercial equipment, where the temperature variations are mild, a nominal phase margin of 60° is usually enough to accommodate manufacturing tolerances.

If external factors such as use of remote sensing or variable amounts of filter capacitance can affect phase margin then more than 60° of nominal phase margin may be desirable.

Military designs with their wide temperature swings should start with a higher nominal value, such as 75 °, to try to maintain 20-30° of phase margin in the worst case.

The penalty for high phase margin is reduced gain at low frequency (reducing the line-frequency ripple rejection) and slower transient response time.

The optimum choice of phase margin and bandwidth is determined by the application.

The important thing is to measure the bandwidth and margins rather than estimate them or ignore them.

(Source : VENABLE technical paper # 2)

How to choose crossover frequency f_c ?

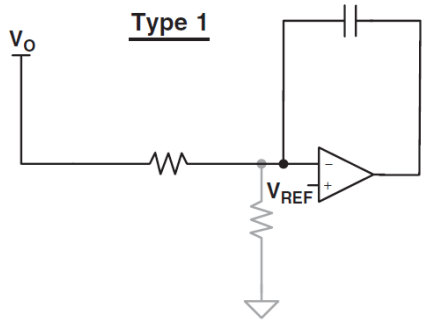
In closed loop, $|Z_{OUT}| \sim |Z(C_{OUT})|_{f=fc}$: $$\Delta V_{OUT} \sim \frac{\Delta I_{OUT}}{2 \cdot \pi \cdot fc \cdot C_{OUT}}$$

Valid only for : $$ESR(C_{OUT}) < \frac{1}{2 \cdot \pi \cdot fc \cdot C_{OUT}}$$

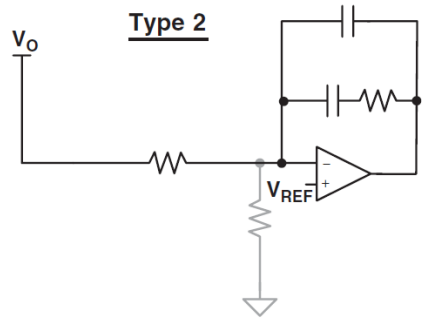
ΔI_{OUT} : output load step
ΔV_{OUT} : output voltage undershoot

Compensators type 1, 2, 3

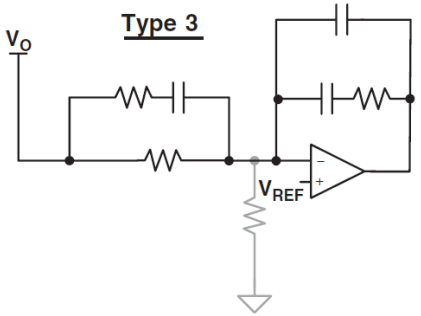
Type 1:
- DC pole only (integrator)
- No phase boost
- Used for power stage with small phase shift



Type 2:
- DC pole + 1 pole + 1 zero
- Phase boost < 90° (<75° in practice)
- Used for CCM current-mode and voltage-mode converters in DCM



Type 3:
- DC pole + 2 pole + 2 zero
- Phase boost < 180° (<160° in practice)
- Used for CCM voltage-mode buck or boost-derived types of converters

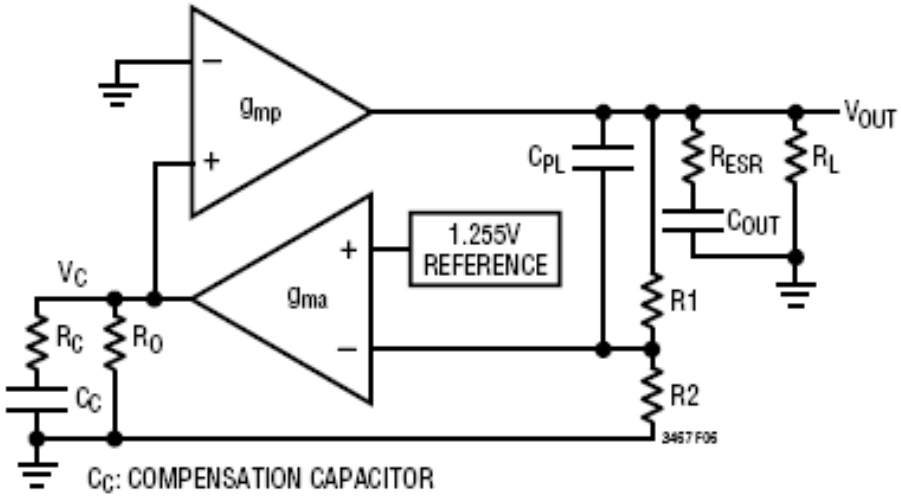


How to define compensation network

Simulation :

- Use LTspice to generate Bode plot
- Check:
  - crossover frequency (fc)
  - phase margin (φm)
- Adjust compensation values manualy or use Venable K-Factor method

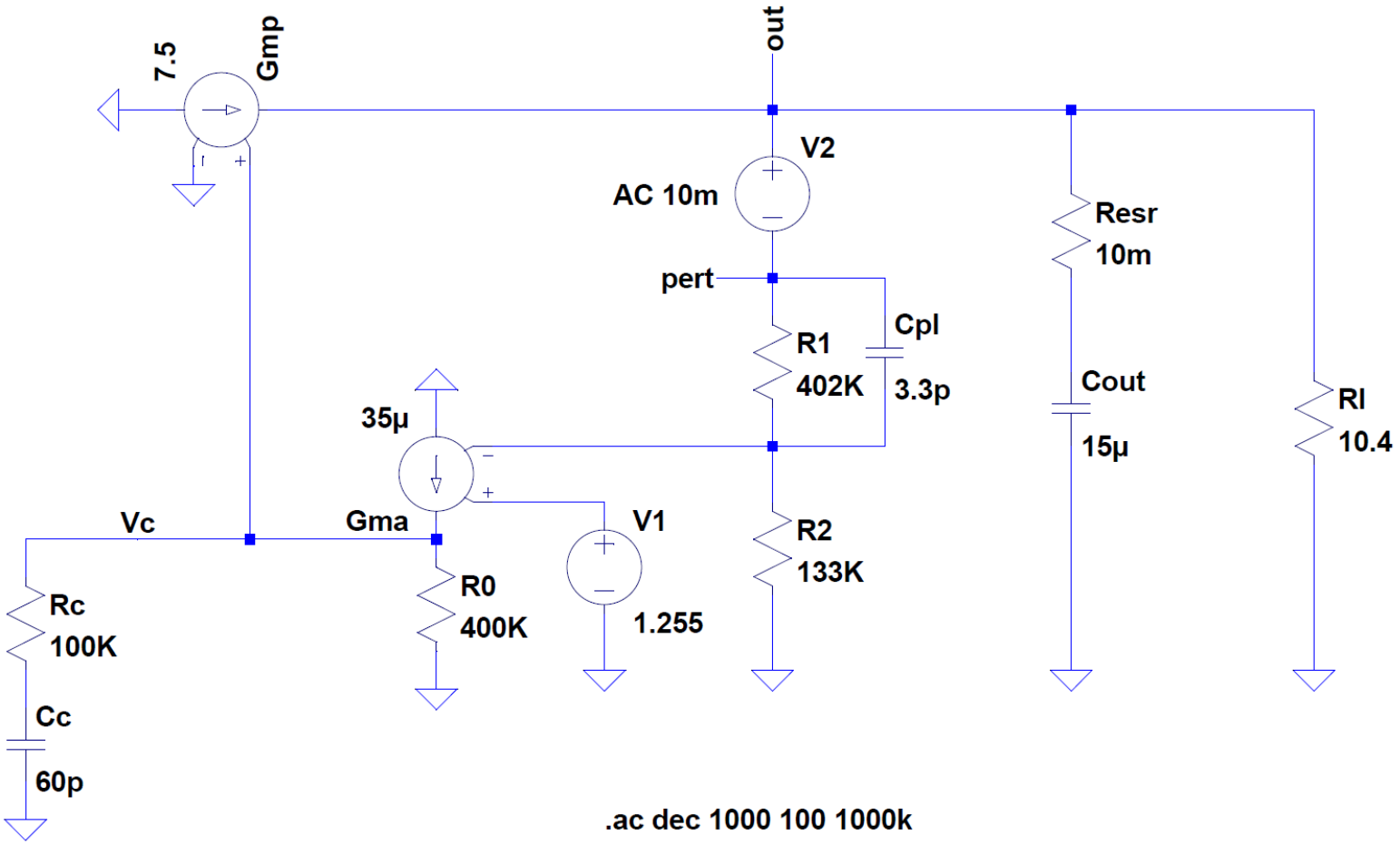
Extract from datasheet



CC: COMPENSATION CAPACITOR
COUT: OUTPUT CAPACITOR
CPL: PHASE LEAD CAPACITOR
gma: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
gmp: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
RC: COMPENSATION RESISTOR
RL: OUTPUT RESISTANCE DEFINED AS V_{OUT} DIVIDED BY $I_{LOAD(MAX)}$
RO: OUTPUT RESISTANCE OF gma
R1, R2: FEEDBACK RESISTOR DIVIDER NETWORK
RESR: OUTPUT CAPACITOR ESR

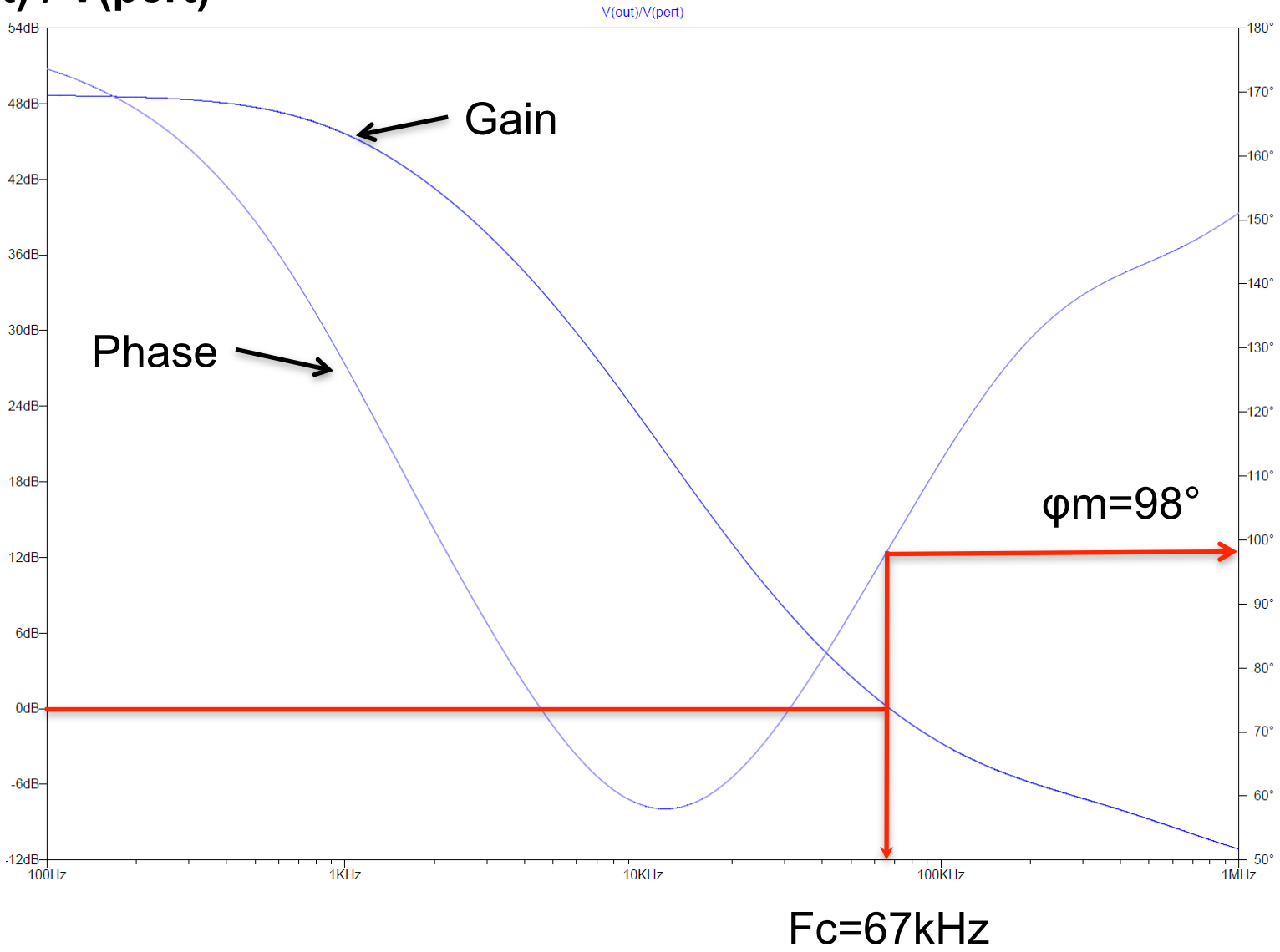
Parameter	Value	Units
R_L	10.4	Ω
C_{OUT}	15	µF
R_{ESR}	10	mΩ
R_O	0.4	MΩ
C_C	60	pF
C_{PL}	3.3	pF
R_C	100	kΩ
R1	402	kΩ
R2	133	kΩ
V_{OUT}	5	V
V_{IN}	3.3	V
g_{ma}	35	µmho
g_{mp}	7.5	mho
L	2.7	µH
f_S	1.3*	MHz

LTspice to generate Bode plot

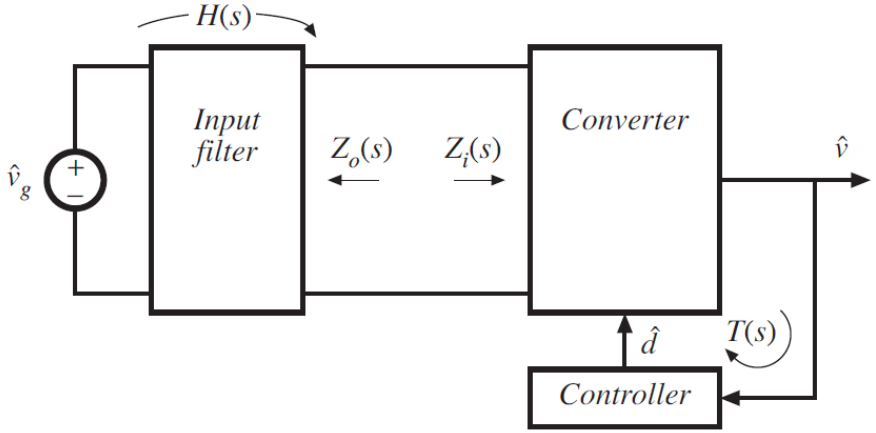


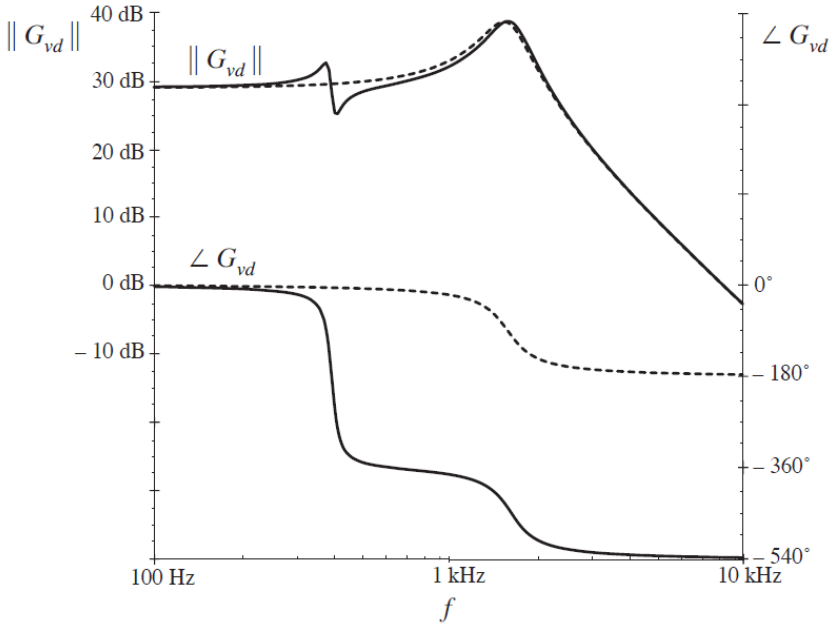
LTspice to generate Bode plot

V(out) / V(pert)



Input Filter & Cascaded DC/DC





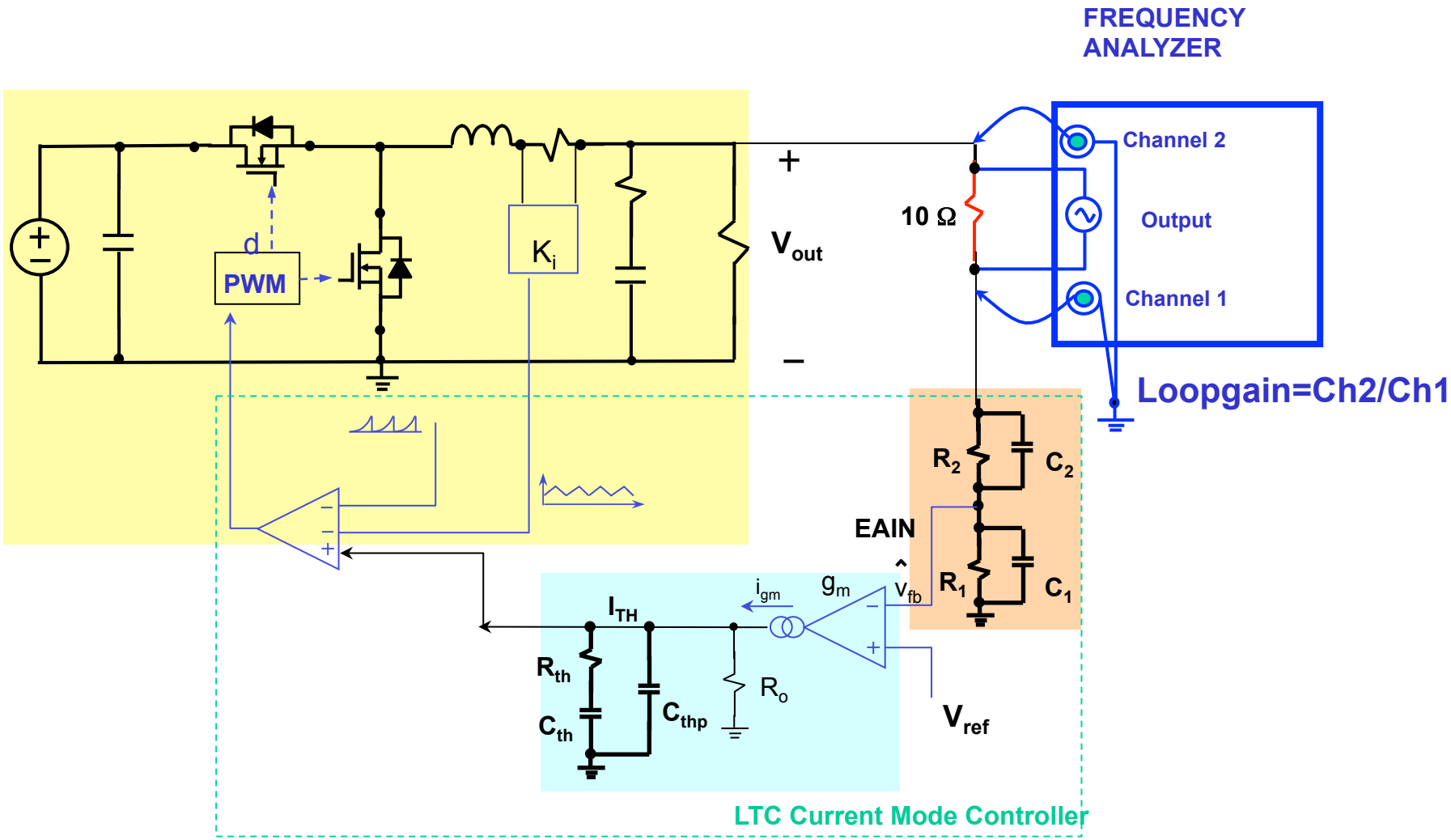
--- no input filter — with input filter

- Filter can seriously degrade converter control system behavior
- Check that converter dynamics is not affected by input filter
- Not affected if |Zo(s)| < |Zi(s)| at all frequencies

- Also check stability of cascaded DC/DC
- 2 stable converters can make an unstable system when cascaded

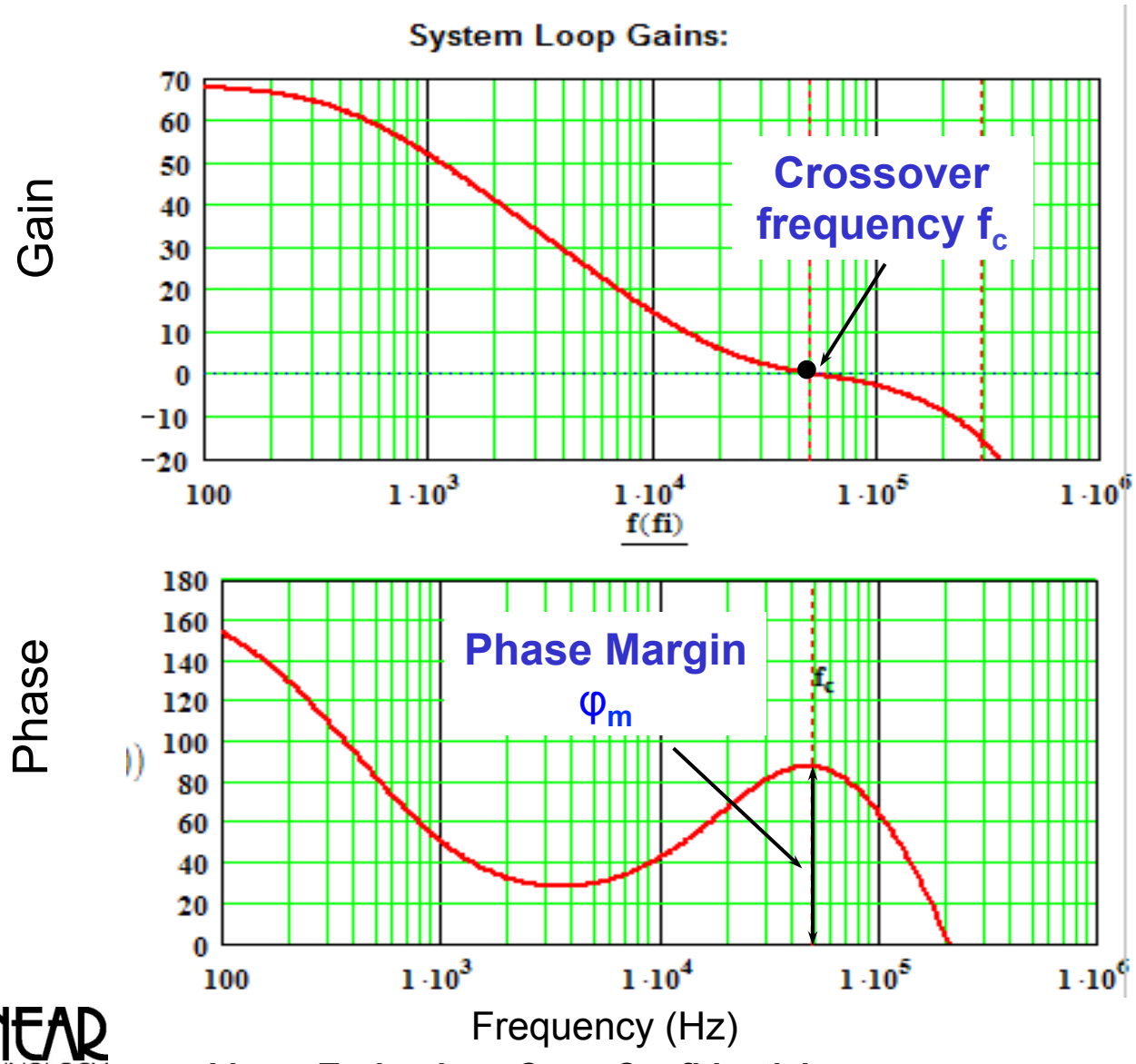
Practical Tests

Measure the Voltage Loop Gain

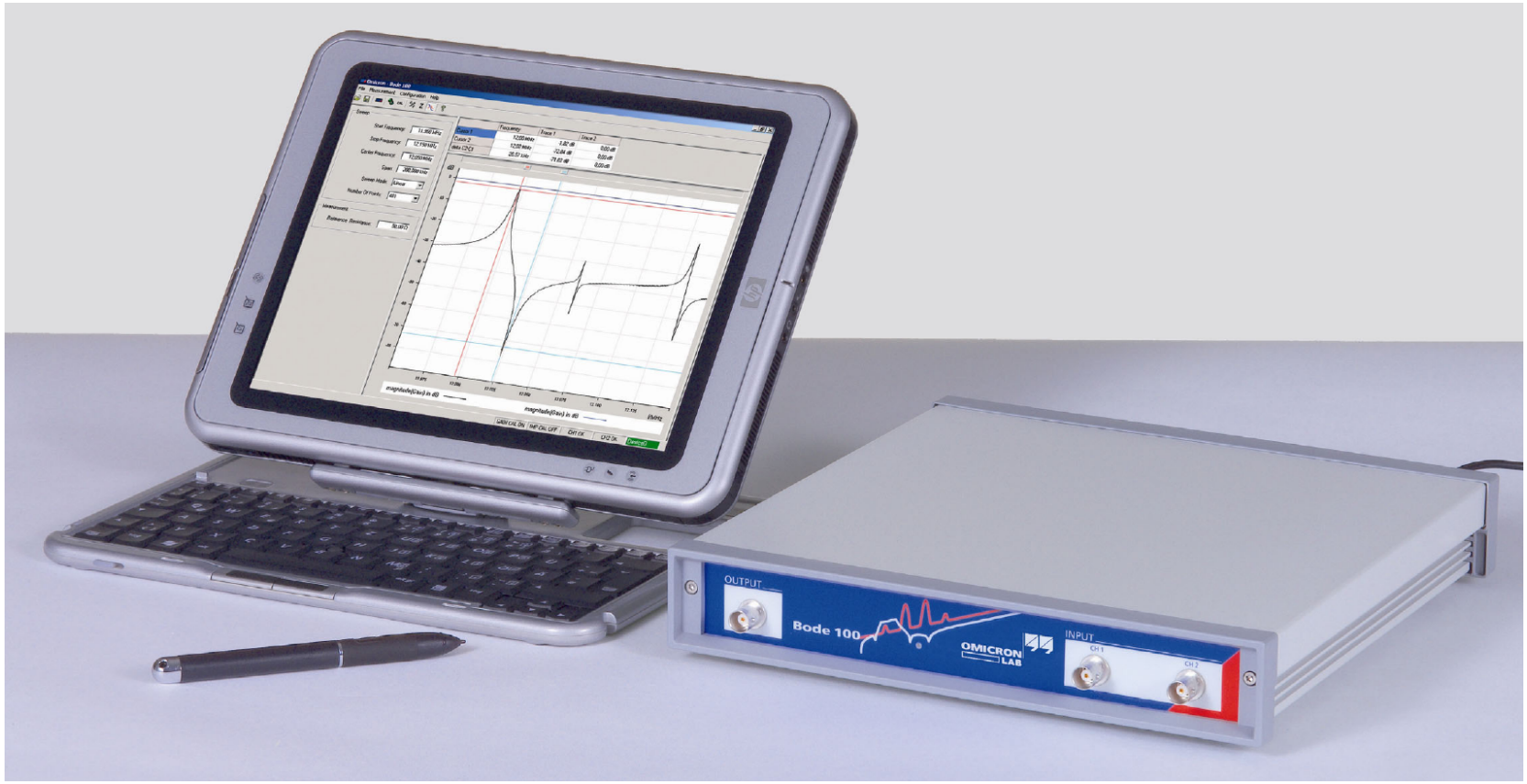


Typical Loop Gain and Phase Margin

LTC3729 Current Mode Buck Converter



Frequency Analyser - Bode 100 by Omicron Lab



1Hz to 40MHz frequency range