ANALOG DEVICES

EVAL-AD5753SDZ User Guide

UG-1492

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Evaluating the AD5753 Single-Channel, 16-Bit Current and Voltage Output DAC with Dynamic Power Control and HART Connectivity

FEATURES

Fully featured evaluation board for the AD5753
On-board, 2.5 V ADR4525 reference
SPI communication

EVALUATION KIT CONTENTS

EVAL-AD5753SDZ evaluation board
Analog Devices, Inc., EVAL-SDP-CS1Z (SDP-S) board

EQUIPMENT NEEDED

PC
EVAL-SDP-CS1Z (SDP-S) board
Bench top power supply and connector cables

DOCUMENTS NEEDED

AD5753 data sheet
EVAL-AD5753SDZ board user guide
ACE user manual

SOFTWARE NEEDED

ACE software

GENERAL DESCRIPTION

This user guide explains how to use the EVAL-AD5753SDZ to evaluate the AD5753, a single-channel, 16-bit voltage and current output, digital-to-analog converter (DAC) with on-chip positive and negative dynamic power control (DPC) that minimizes package power dissipation.

The EVAL-SDP-CS1Z system demonstration platform (SDP-S) board is required when using the EVAL-AD5753SDZ board. The EVAL-AD5753SDZ (see Figure 1) interfaces to the USB port of the PC via the EVAL-SDP-CS1Z (SDP-S). Analysis Control Evaluation (ACE) software is available to use with the EVAL-AD5753SDZ, and allows the programming of the AD5753.

For full details on the AD5753, refer to the AD5753 data sheet. Consult the AD5753 data sheet in conjunction with this user guide when using the EVAL-AD5753SDZ. The configuration of the various link options is explained in the Evaluation Board Hardware section. The installation of the companion software is discussed in the Software Quick Start Procedures section.

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REVISION HISTORY

5/2019—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

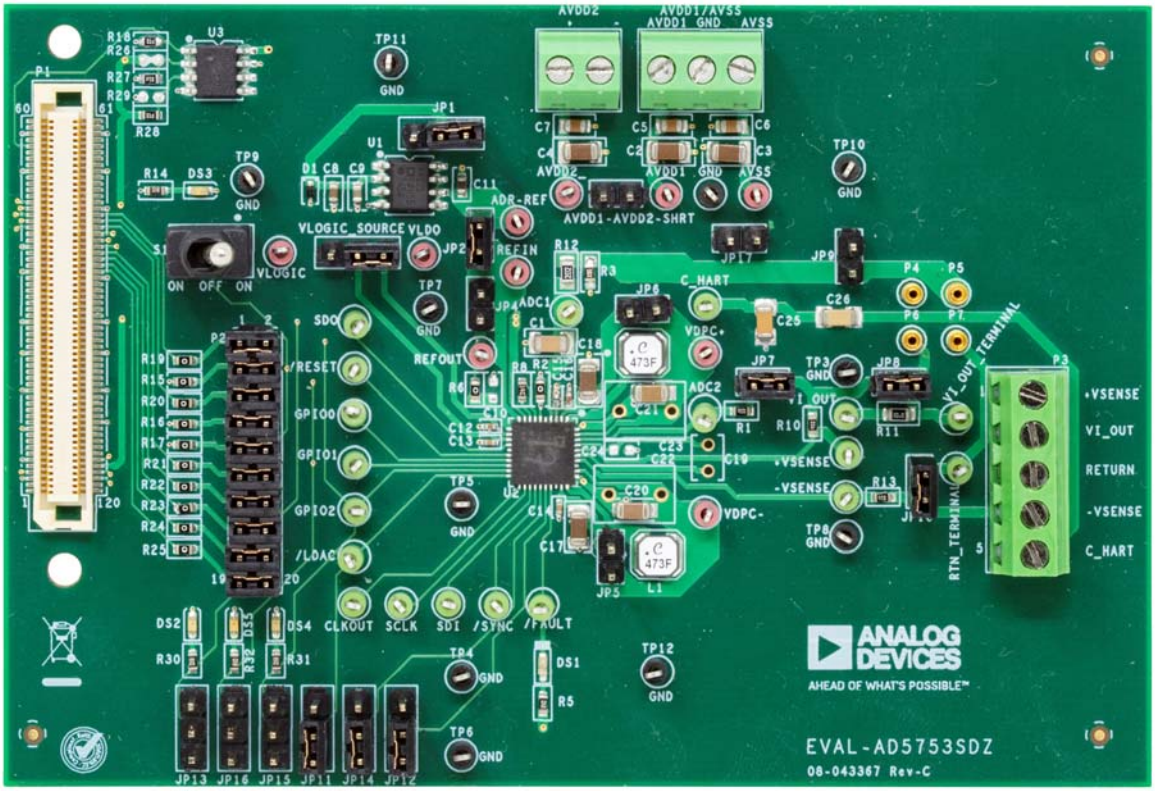

Figure 1.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-AD5753SDZ requires power supply inputs for the AV_{DD1}, AV_{DD2}, AV_{SS}, and V_{LOGIC} supplies. If there is only one positive rail available, connect the AV_{DD2} pin to the AV_{DD1} pin via the AVDD1-AVDD2-SHRT link. Select the V_{LOGIC} supply from the 3.3V_SDP evaluation board pin or the V_{LDO} pin through the VLOGIC_SOURCE link. See Table 1 for the default link positions and see Table 2 for more linking options.

The EVAL-AD5753SDZ operates with a power supply range of −33 V on AV_{SS} to +33 V on AV_{DD1}, with a maximum voltage of 60 V between the two rails. AV_{DD2} requires a voltage between 5 V and 33 V. To bypass the positive dc-to-dc circuitry, connect the V_{DPC+} pin directly to AV_{DD1} via the JP6 jumper. To bypass the negative dc-to-dc circuitry, connect the V_{DPC-} pin directly to the AV_{SS} pin via the JP5 jumper. The recommended supply voltages are AV_{DD2} = +5 V, AV_{DD1} = +24 V, and AV_{SS} = −24 V.

SERIAL COMMUNICATION

The EVAL-SDP-CS1Z (SDP-S) handles communication to the EVAL-AD5753SDZ via the PC. The EVAL-SDP-CS1Z (SDP-S) handles the serial port interface (SPI) communication, controls the $\overline{\text{RESET}}$ pin and the $\overline{\text{LDAC}}$ pin, and monitors the $\overline{\text{FAULT}}$ pin of the AD5753.

Remove the appropriate links on P2 to disconnect the EVAL-AD5753SDZ from the EVAL-SDP-CS1Z (SDP-S) and drive the digital signals from an external source. The S1 link and the JP11 link allow the user to tie $\overline{\text{RESET}}$ and $\overline{\text{LDAC}}$ to high or low levels.

AD5753 ADDRESS PINS

The AD0 address pin and the AD1 address pin are used in conjunction with the address bits within the SPI frame to determine which AD5753 device is being addressed by the system controller. Configure the AD0 pin and the AD1 pin through the JP12 link and the JP14 link.

Table 1. EVAL-AD5753SDZ Link Option Functions

Link	Default Position	Function
AVDD1-AVDD2-SHRT	Not inserted	Connects AV_{DD2} to AV_{DD1}.
VLOGIC_SOURCE	A	Position A selects 3.3 V from the EVAL-SDP-CS1Z (SDP-S). Position B selects 3.3 V from the V_{LDO} pin of the AD5753.
JP1	A	Position A powers the ADR4525 reference (ADR-REF) from the V_{LDO} pin. Position B powers the ADR-REF from AV_{DD2}. The maximum supply for the ADR4525 is 15 V.
JP2	Inserted	Selects the ADR-REF pin as the input to the REFIN pin.
JP4	Not inserted	Selects the REFOUT pin as the input to the REFIN pin.
JP5	Not inserted	Shorts the V_{DPC-} pin to the AV_{SS} pin to bypass the negative dc-to-dc circuitry.
JP6	Not inserted	Shorts the V_{DPC+} pin to the AV_{DD1} pin to bypass the positive dc-to-dc circuitry.
JP7	Inserted	Shorts the ADC2 pin to the $+V_{SENSE}$ pin.
JP8	Inserted	Connects the V_{IOUT} pin to the $+V_{SENSE}$ pin.
JP9	Not inserted	Connects the RETURN signal to the GND position on the EVAL-AD5753SDZ.
JP10	Inserted	Connects the $-V_{SENSE}$ pin to the RETURN signal.
JP11	A	Position A connects the $\overline{\text{LDAC}}$ pin to the GND position. Position B connects the $\overline{\text{LDAC}}$ pin to the V_{LOGIC} pin.
JP12	A	Position A connects the AD0 pin to the GND position. Position B connects the AD0 pin to the V_{LOGIC} pin.
JP13	B	Position A connects the GPIO_0 pin to the GND position. Position B connects the GPIO_0 pin to the V_{LOGIC} pin.
JP14	A	Position A connects the AD1 pin to the GND position. Position B connects the AD1 pin to the V_{LOGIC} pin.
JP15	B	Position A connects the GPIO_2 pin to the GND position. Position B connects the GPIO_2 pin to the V_{LOGIC} pin.
JP16	B	Position A connects the GPIO_1 pin to the GND position. Position B connects the GPIO_1 pin to the V_{LOGIC} pin.
JP17	Not inserted	Connects the AV_{SS} pin to the GND position for the unipolar supply option (current output only).
P2	Inserted	Provides options to disconnect from the EVAL-SDP-CS1Z (SDP-S) and to drive digital signals from an external source. See Table 2 for the specific link options.
S1	2-3	Position 2-1 (on position to the right of off) connects the $\overline{\text{RESET}}$ pin to the GND position. Position 2-3 (on position to the left of off) connects the $\overline{\text{RESET}}$ pin to the V_{LOGIC} pin.

Table 2. Link Options for P2

Pin Number	Position	Function
1, 2	Inserted	Connects the $\overline{\text{FAULT}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{FAULT}}$ pin on the AD5753.
	Not inserted	Disconnects the $\overline{\text{FAULT}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{FAULT}}$ pin on the AD5753.
3, 4	Inserted	Connects the $\overline{\text{RESET}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{RESET}}$ pin on the AD5753.
	Not inserted	Disconnects the $\overline{\text{RESET}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{RESET}}$ pin on the AD5753.
5, 6	Inserted	Connects the $\overline{\text{LDAC}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{LDAC}}$ pin on the AD5753.
	Not inserted	Disconnects the $\overline{\text{LDAC}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{LDAC}}$ pin on the AD5753.
7, 8	Inserted	Connects the SCLK signal from the EVAL-SDP-CS1Z (SDP-S) to the SCLK pin on the AD5753.
	Not inserted	Disconnects the SCLK signal from the EVAL-SDP-CS1Z (SDP-S) to the SCLK pin on the AD5753.
9, 10	Inserted	Connects the SDO signal from the EVAL-SDP-CS1Z (SDP-S) to the SDO pin on the AD5753.
	Not inserted	Disconnects the SDO signal from the EVAL-SDP-CS1Z (SDP-S) to the SDO pin on the AD5753.
11, 12	Inserted	Connects the SDI signal from the EVAL-SDP-CS1Z (SDP-S) to the SDI pin on the AD5753.
	Not inserted	Disconnects the SDI signal from the EVAL-SDP-CS1Z (SDP-S) to the SDI pin on the AD5753.
13, 14	Inserted	Connects the $\overline{\text{SYNC}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{SYNC}}$ pin on the AD5753.
	Not inserted	Disconnects the $\overline{\text{SYNC}}$ signal from the EVAL-SDP-CS1Z (SDP-S) to the $\overline{\text{SYNC}}$ pin on the AD5753.

SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND AD5753 PLUGINS

The EVAL-AD5753SDZ software uses the Analog Devices ACE software. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

When the installation is finished, open the ACE software to open the EVAL-AD5753SDZ plugin (see Figure 2).

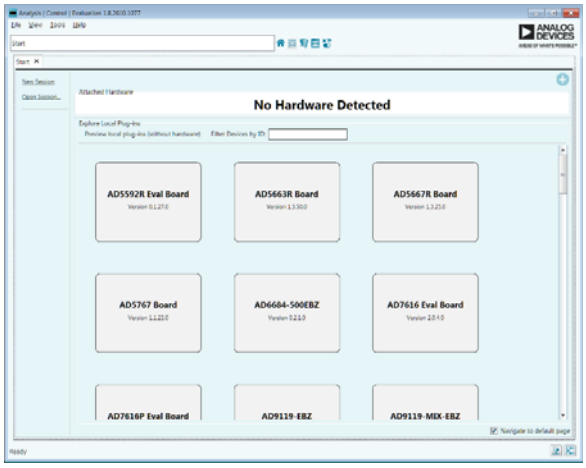

Figure 2. EVAL-AD5753SDZ Plugin Window

INITIAL SETUP

To set up the EVAL-AD5753SDZ with the ACE software, take the following steps:

1. Connect one end of the USB cable to the PC, and connect the other end to the EVAL-SDP-CS1Z (SDP-S).
2. Connect the EVAL-SDP-CS1Z (SDP-S) to the EVAL-AD5753SDZ. The PC recognizes the EVAL-AD5753SDZ.
3. Power up the EVAL-AD5753SDZ with the power supplies described in the Power Supplies section.
4. If not opened already, open the ACE software. The EVAL-AD5753SDZ appears in the **Attached Hardware** section of the ACE software window.
5. The first time the EVAL-AD5753SDZ is set up, the plugin may need to be installed. If the plugin appears as shown in Figure 6, then go to Step 7. If the plugin appears as shown in Figure 3, click on the button circled in red to open the pop-up window shown in Figure 4, then click **Yes**.
6. A new window (see Figure 5) opens. Select the **Board.AD5753** plugin and click the **Install Selected** button. The installed EVAL-AD5753SDZ plugin displays as shown in Figure 6.

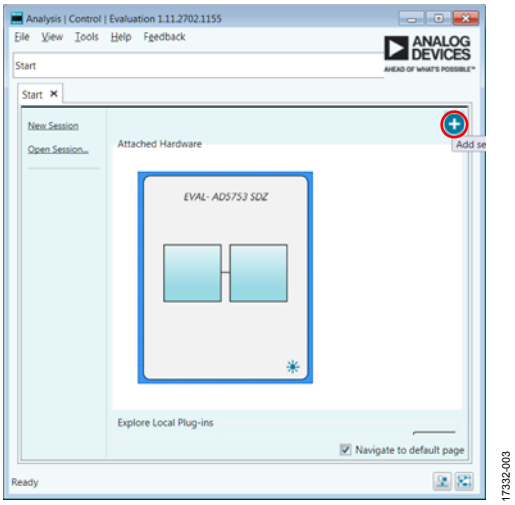

Figure 3. EVAL-AD5753SDZ Plugin Not Installed

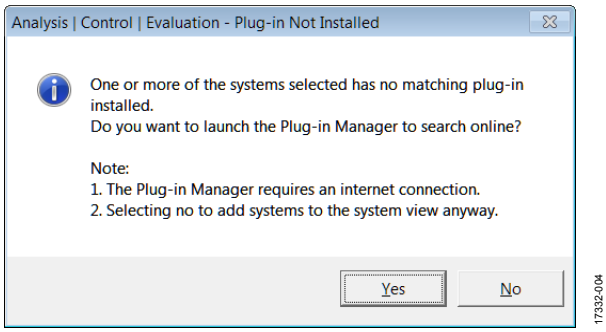

Figure 4. Installing the Plugin Pop-Up Window

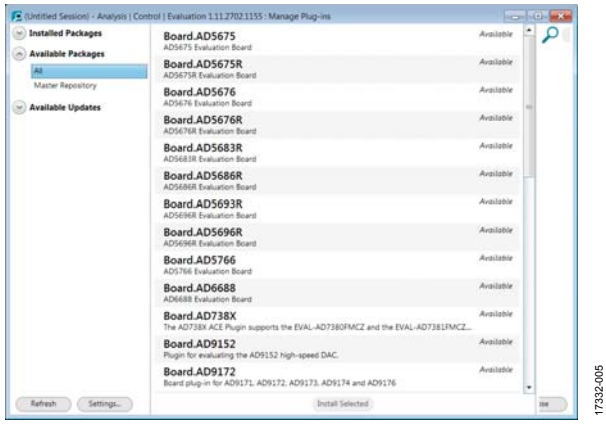

Figure 5. Plugin Manager Window

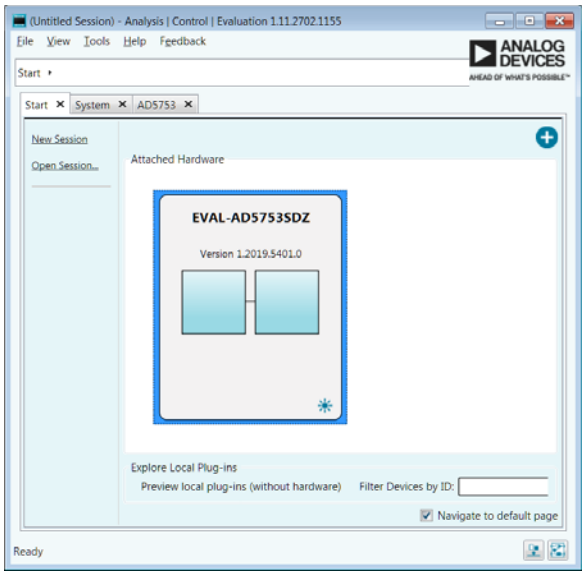

*Figure 6. **Attached Hardware** Section with Connected EVAL-AD5753SDZ*

7. Double-click **EVAL-AD5753SDZ** to open the AD5753 block diagram (see Figure 7). The **INITIAL CONFIGURATION** menu appears on the left side of the window. Several register settings can be configured under this menu, and are written to the device in the appropriate order. The **DIG_DIAG_STATUS**, **RESET_OCCURED**, and **CAL_MEM_UNREFRESHEDLED** indicators are highlighted red. Write the initial configuration values to clear the error flags. If the device is power cycled, or if the USB cable is disconnected and reconnected while the ACE software is open, contact with the EVAL-AD5753SDZ is lost. If contact is lost, click the **System** tab, click the USB symbol on the EVAL-AD5753SDZ, and then click **Acquire** to restore communication with the EVAL-AD5753SDZ.

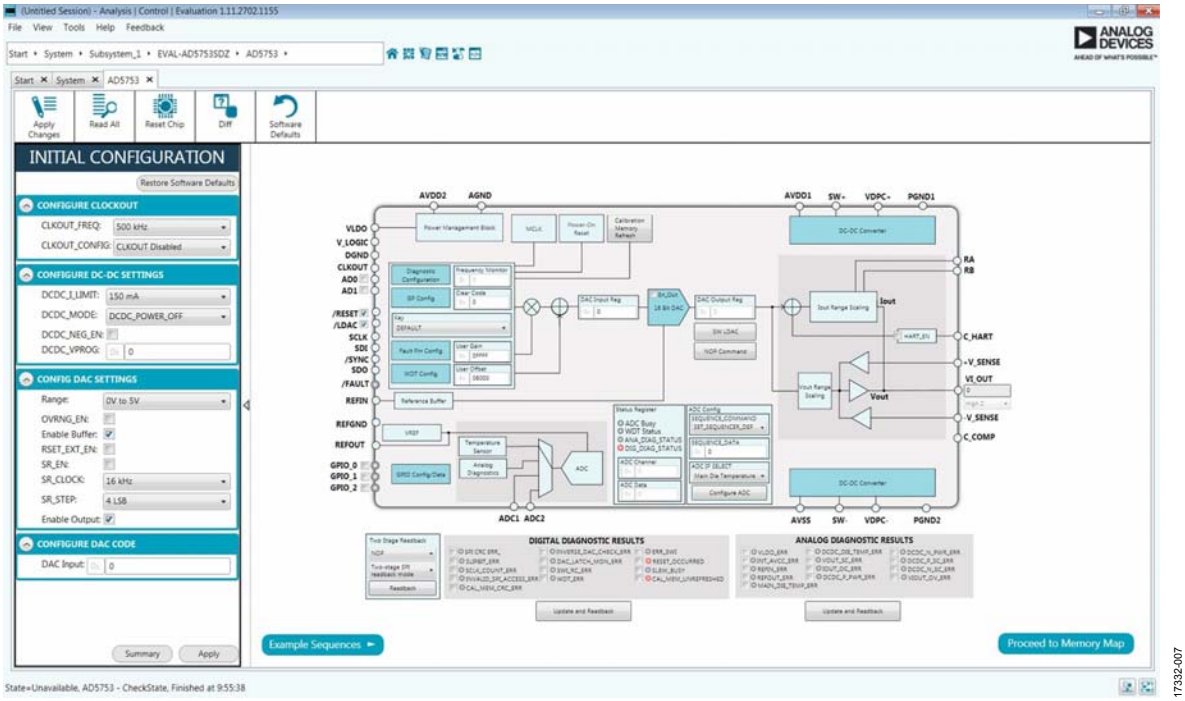

Figure 7. AD5753 Block Diagram in ACE Software

AD5753 BLOCK DIAGRAM AND FUNCTIONS

The AD5753 ACE plugin appears similar to the block diagram shown in the AD5753 data sheet. This similarity allows the user to correlate the functions on the EVAL-AD5753SDZ to the descriptions in the AD5753 data sheet.

A full description of each block and register setting is available in the AD5753 data sheet. The full screen AD5753 block diagram is shown in Figure 8 with all blocks labeled. Table 3 describes the functionality of each block.

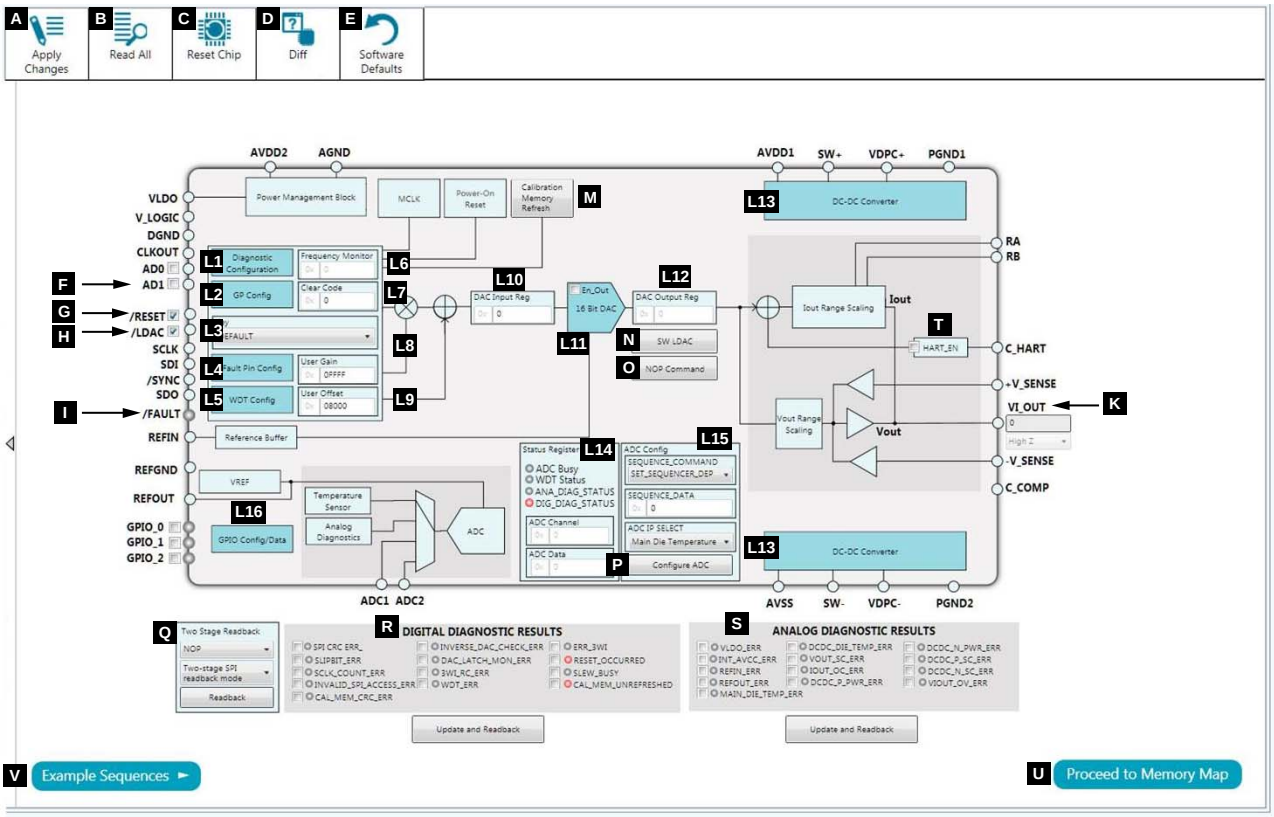

Figure 8. AD5753 Block Diagram with Labels

Table 3. AD5753 Block Diagram Label Functions (See Figure 8)

Label	Function
A	**Apply Changes**. Applies any changes made to the block diagram or to register values in the memory map to the device.
B	**Read All**. Click to read back all of the registers of the device.
C	**Reset Chip**. Click to reset the AD5753. **Reset Chip** has the same functionality as the software reset of the AD5753.
D	**Diff**. Click to show the registers that are different from the data stored on the device. This function shows changes from the last time the registers were read.
E	**Software Defaults**. Click to load the software defaults of the device. These values are not written to the hardware. Click **Apply Changes** (Label A) to write the software default values to the hardware.
F	**AD0** and **AD1**. These check boxes set the address of the device and must correspond to the JP12 link and the JP14 link on the hardware. When either box is checked, this represents a high state. When either box is unchecked, this represents a low state.
G	**/RESET**. Check the EVAL-SDP-CS1Z (SDP-S) to set the $\overline{\text{RESET}}$ pin high. Otherwise, the EVAL-SDP-CS1Z (SDP-S) pulls $\overline{\text{RESET}}$ low.
H	**/LDAC**. Check the EVAL-SDP-CS1Z (SDP-S) to set the $\overline{\text{LDAC}}$ pin high. Otherwise, the EVAL-SDP-CS1Z (SDP-S) pulls $\overline{\text{LDAC}}$ low.
I	**/FAULT**. Indicator LED lights up red if the $\overline{\text{FAULT}}$ pin is low. The ACE plugin monitors the $\overline{\text{FAULT}}$ pin.
K	**VI_OUT**. Displays the calculated output at VI_OUT and shows if the output is in voltage, milliamps, or is high impedance (high-Z).
Lx	Graphical user interface (GUI) access on several registers. Pop-up windows, dropdown menus, and hexadecimal textboxes are available in the GUI to configure several registers of the AD5753. To write the changes to the device, click the **Apply Changes** button (Label A). The functions within the GUI that control various registers (Label L1 through Label L15) are described in Table 4.
M	**Calibration Memory Refresh** button. Initiates a write to the key register to perform a calibration memory refresh.
N	**SW LDAC** button. Initiates a write to the key register to perform a software $\overline{\text{LDAC}}$ command.
O	**NOP Command** button. Initiates a write to Address 0x00 for a no operation (NOP) command.
P	**Configure ADC** button. Writes the data selected in the **ADC Config** menu (Label L15) to the ADC configuration register.
Q	**Two Stage Readback** menu. Initiate two-stage readback through the two-stage readback select register. Click the **Readback** button to initiate a write to the two-stage readback select register and issue a no operation command.
R	**DIGITAL DIAGNOSTIC RESULTS** menu. Click the **Update and Readback** digital diagnostic result button to trigger a write of 1 to clear operation and a readback from the digital diagnostic results register.
S	**ANALOG DIAGNOSTIC RESULTS** menu. Click the **Update and Readback** analog diagnostic result button to trigger a write of 1 to clear operation and a readback from the analog diagnostic results register.
T	**HART_EN** box. Check this box to allow the HART_EN bit = 1 in the General-Purpose Configuration 1 register.
U	**Proceed to Memory Map** button. Click this button to open the AD5753 memory map (see Figure 9).
V	**Example Sequences** button. Click this button to open the example sequences window (see Figure 15).

Table 4. Register Controls Accessible via the GUI (See Label Lx in Table 3 and in Figure 8)

Label	Function
L1	**Diagnostic Configuration** button. Click this button to open the associated pop-up menu.
L2	**GP Config** menu. Click this menu to open the associated pop-up menu.
L3	**Key** register menu. Click this menu to open the associated dropdown menu.
L4	**Fault Pin Config** button. Click this button to open the associated pop-up menu.
L5	**WDT Config** button. Click this button to open the associated pop-up menu.
L6	**Frequency Monitor** menu. This menu displays the value in the frequency monitor when read.
L7	**Clear Code** menu. Use the textbox in this menu to insert a clear code value in hexadecimal format.
L8	**User Gain** menu. Use the textbox in this menu to insert a user gain value in hexadecimal format.
L9	**User Offset** menu. Use the textbox in this menu to insert a user offset value in hexadecimal format.
L10	**DAC Input Reg** menu. Use the textbox in this menu to insert the DAC value in hexadecimal format.
L11	**16 Bit DAC** symbol. Click this button to open the associated pop-up menu.
L12	**DAC Output Reg** menu. This menu displays the hexadecimal value currently set in the DAC output register.
L13	**DC-DC Converter**. Click this button to open the dc-to-dc configuration pop-up menu.
L14	**Status Register** menu. This menu displays the contents of the status register.
L15	**ADC Config** menu. This menu contains a combination of dropdown menus and a textbox to enter the sequence data.
L16	**GPIO Config/Data**. Click this button to bring up a pop-up menu that allows control of the GPIOs.

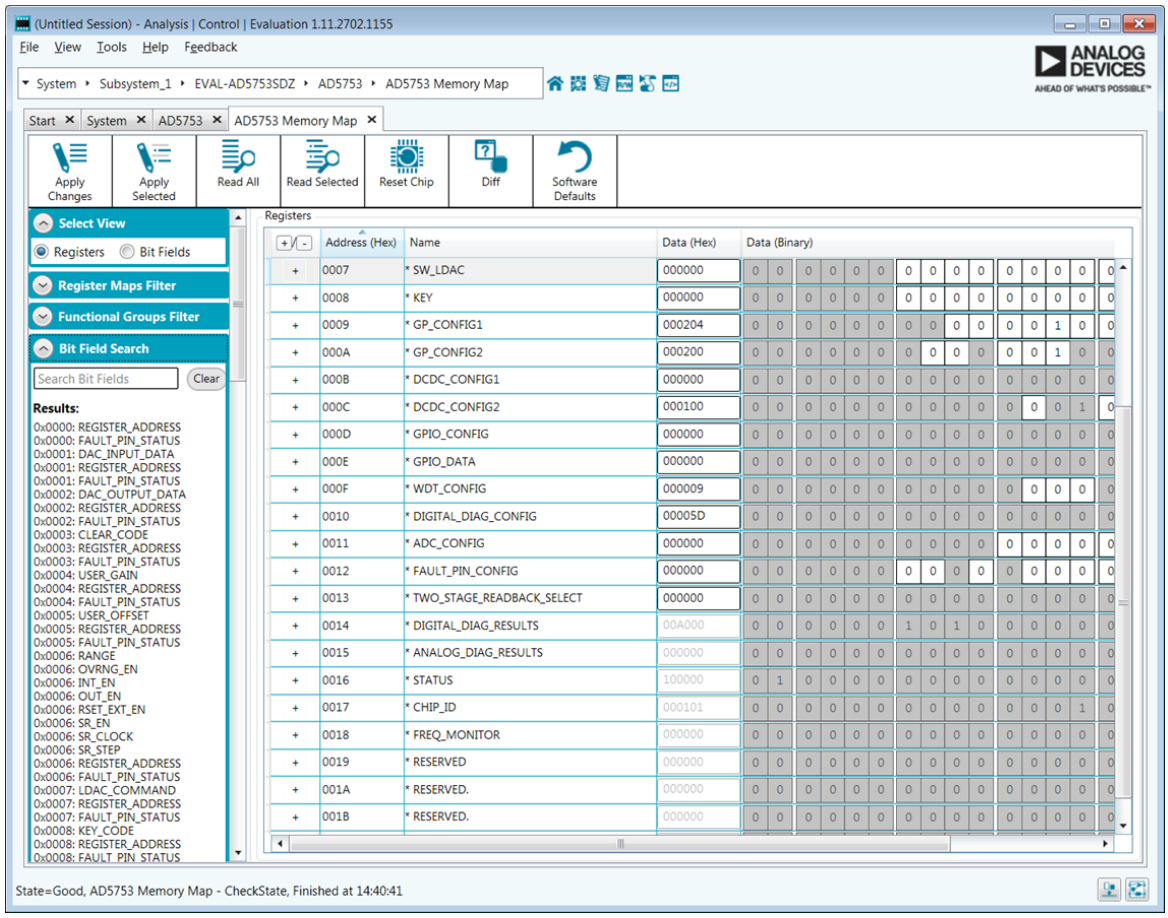

Figure 9. AD5753 Memory Map in ACE Software

CONFIGURING THE EVALUATION BOARD

An initial configuration wizard is available when opening the AD5753 plugin. The initial configuration wizard allows configuration of the AD5753 and provides configuration of the clock output in the General-Purpose Configuration Register 1, the dc-to-dc settings, the DAC configuration, and the DAC input register. Click the **Apply** button to initiate the configured settings in the order of the recommended power-up sequence described in the AD5753 data sheet.

DC-TO-DC CONVERTER SETTINGS

If the V_{DPC+} pin is not tied directly to the AVDD1 pin, enable the dc-to-dc converter for correct operation. Complete this step before configuring the DAC output. The **DC-DC Configuration** pop-up menu, shown in Figure 10, contains the dc-to-dc settings required to configure the AD5753 output correctly. After the proper settings are selected, click the **Close** button and then click **Apply Changes.**

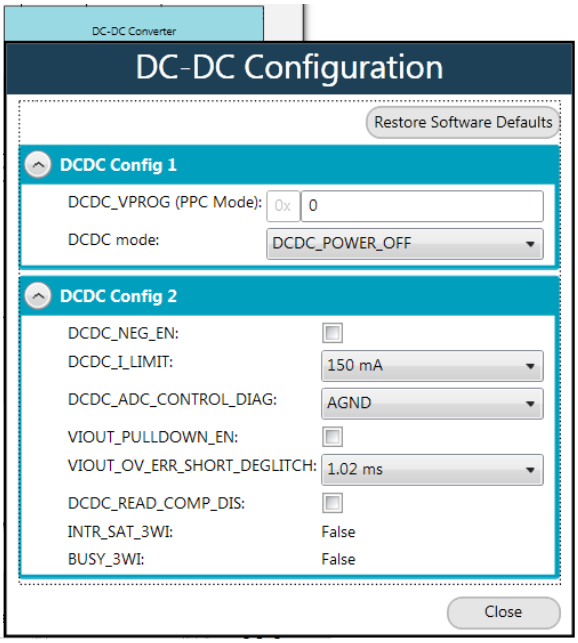

*Figure 10. **DC-DC Configuration** Pop-Up Menu*

CONFIGURING THE DAC OUTPUT

To configure the DAC output, use the pop-up menu for the DAC configuration register (see Figure 11), available in the GUI. Click the **16 Bit DAC** (Label L11, Figure 8) symbol in the GUI to display the DAC configuration register. Select the appropriate settings and then click **Apply Changes** (Label A, Figure 8). It is recommended to disable the output until the correct value in the DAC input register is written to the device.

To change the DAC voltage or current output level, write the appropriate hexadecimal code to the DAC input register and then click **Apply Changes**. Issue a software LDAC command using the **SW LDAC** (Label N, Figure 8) button, or pull the LDAC pin low to update the DAC output register with the values in the DAC input register. Select the **OUT_EN** checkbox to enable the DAC output and then click **Apply Changes.** The programmed voltage or current is reflected at the V_{IOUT} pin.

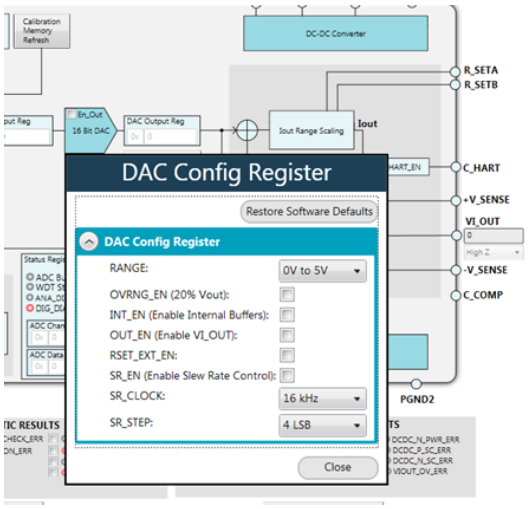

*Figure 11. AD5753 **DAC Config Register** Pop-Up Menu*

WRITING TO THE ADC CONFIGURATION REGISTER

The procedure to set up and configure the ADC sequencer is discussed in the AD5753 data sheet. Writing to the ADC configuration register is simplified because of the multiple configuration modes.

Dropdown menus and a hexadecimal textbox are available within the GUI (see Figure 12) to access the ADC configuration register. Click the **Configure ADC** button instead of the **Apply Changes** button to write to the ADC configuration register.

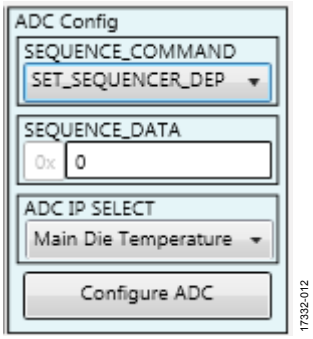

Figure 12. AD5753 ADC Configuration Register

UPDATING DIAGNOSTIC RESULTS

The AD5753 has a digital diagnostic results register and an analog diagnostic results register, both of which contain error flags for the on-chip digital and analog diagnostic features. Write 1 to the respective error flags to update the error flag status.

The **Update and Readback** button shown in Figure 13 is available on the ACE GUI to update the digital and analog diagnostic results registers. Click this button to initiate a write of 1 (by selecting the box) to the selected error flag, and then read back the updated diagnostic result. Figure 13 shows the digital diagnostic results register. Figure 14 shows the analog diagnostic results register.

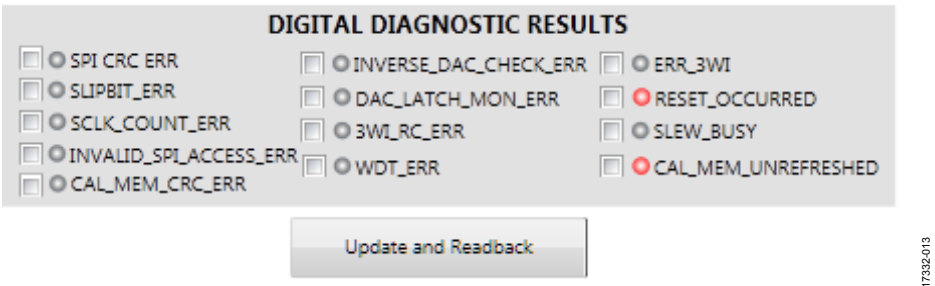

Figure 13. AD5753 Digital Diagnostic Results Register

Figure 14. AD5753 Analog Diagnostic Results Register

EXAMPLE SEQUENCES

There are several example sequences available. Click the **Example Sequences** button (Label V, Figure 8) and the window shown in Figure 15 appears. To enable any of the sequences, click on the relevant sequence button, as shown in Figure 16. The sequence runs immediately and the output changes accordingly. To return to the main window, click the **Back to AD5753** button.

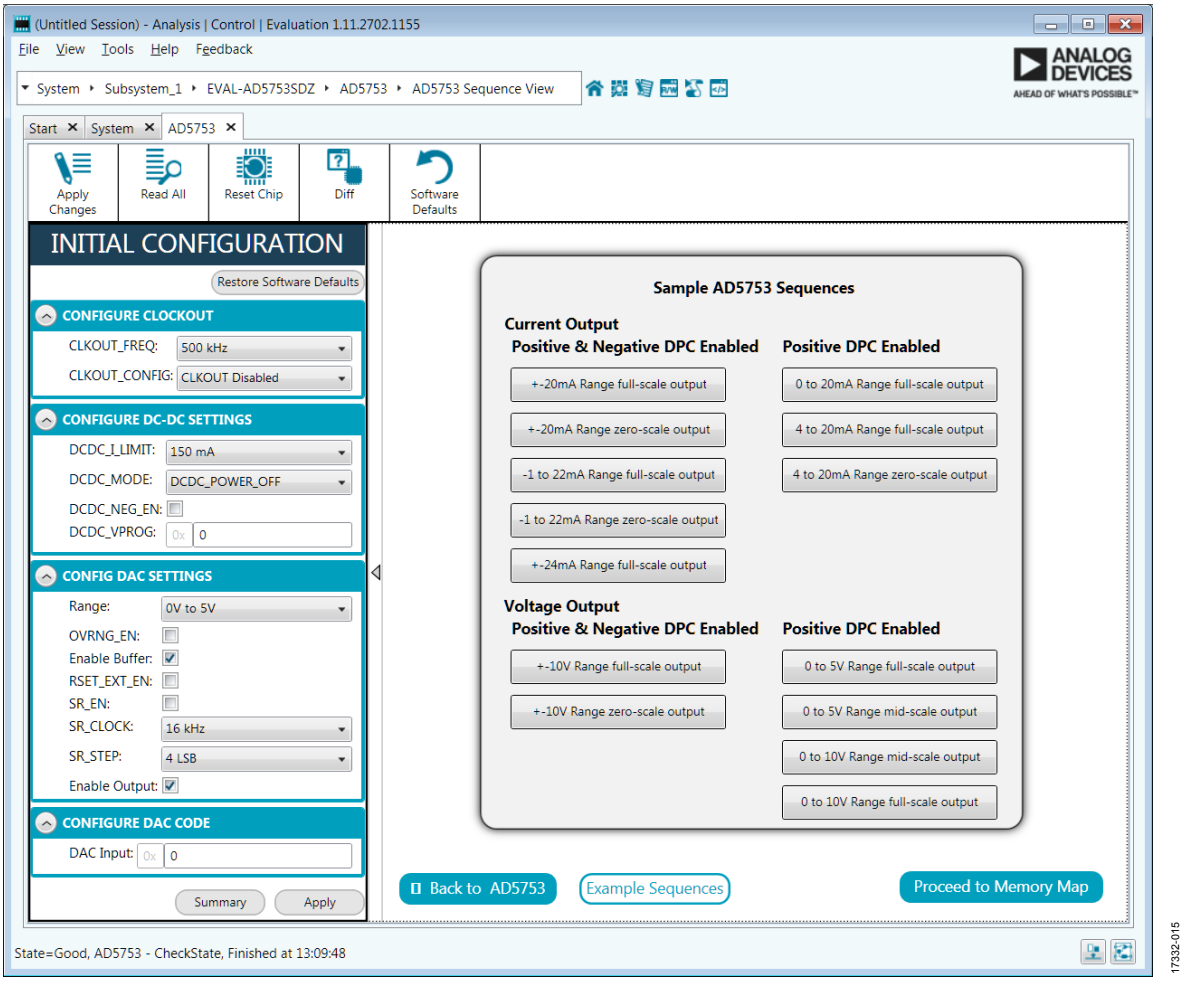

Figure 15. Example Sequences Window

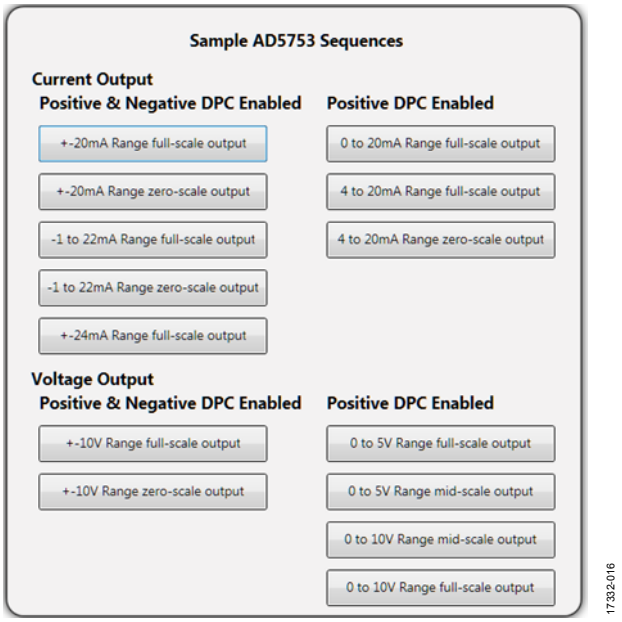

Figure 16. Selecting an Example Sequence

ACE TOOL VIEWS

The ACE software provides additional functionality to the main view described in this user guide. Open these views from the view menu item on the application toolbar. The ACE software features a macro tool, a register debugger tool, and an events tool.

MACRO TOOL

The macro tool records and saves commands as an ACE macro file. This feature is useful when sharing macros with other users to perform the same task multiple times. The user can import and run an ACE macro file.

REGISTER DEBUGGER TOOL

The register debugger tool performs raw writes to, and reads from, the device. The register debugger only affects the hardware and does not write to the memory map of the ACE software.

EVENTS TOOL

The events tool view contains a list of errors, warnings, and information messages generated within the application software.

EVALUATION BOARD SCHEMATICS AND ARTWORK

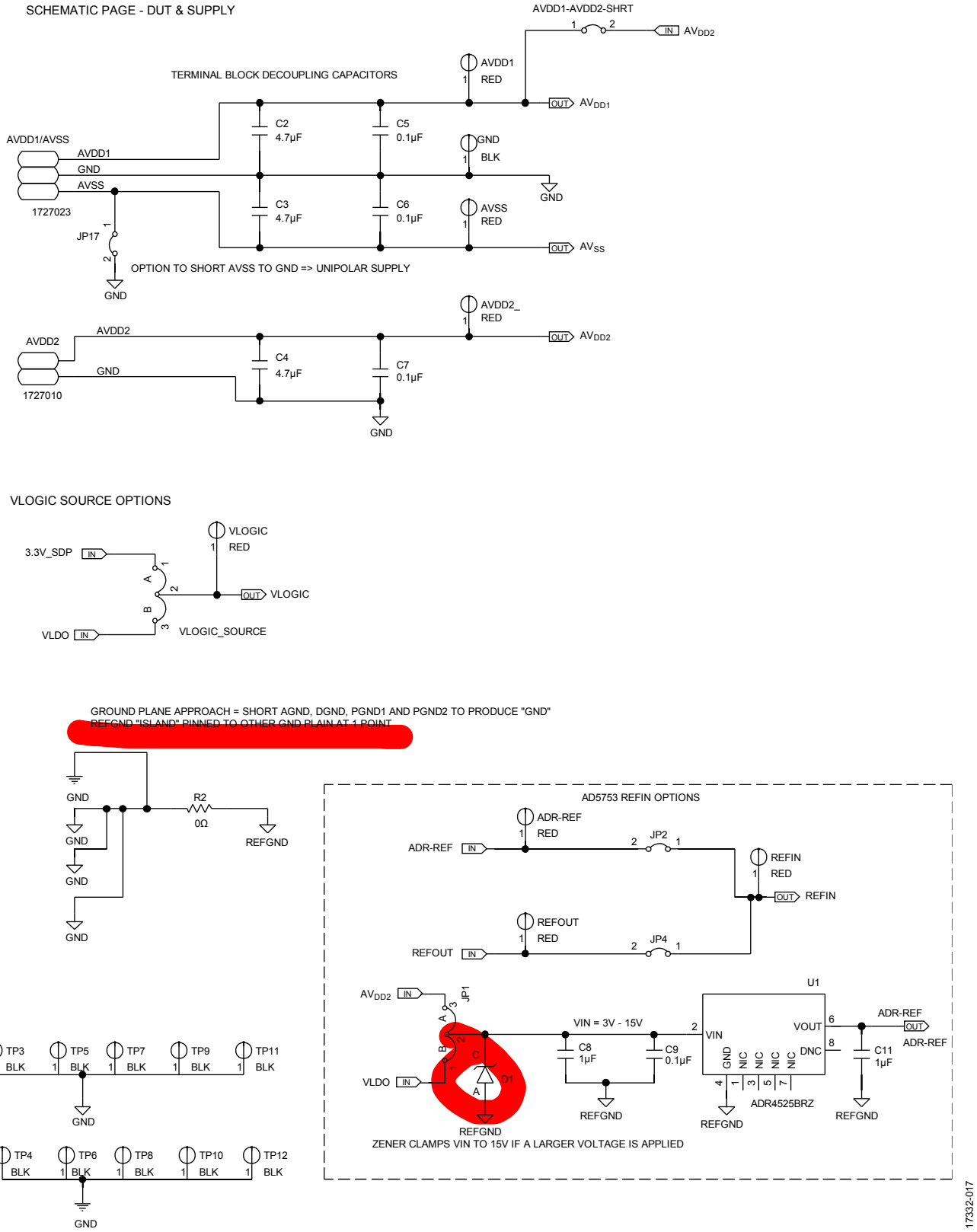

Figure 17. AD5753 Supplies and Reference Options

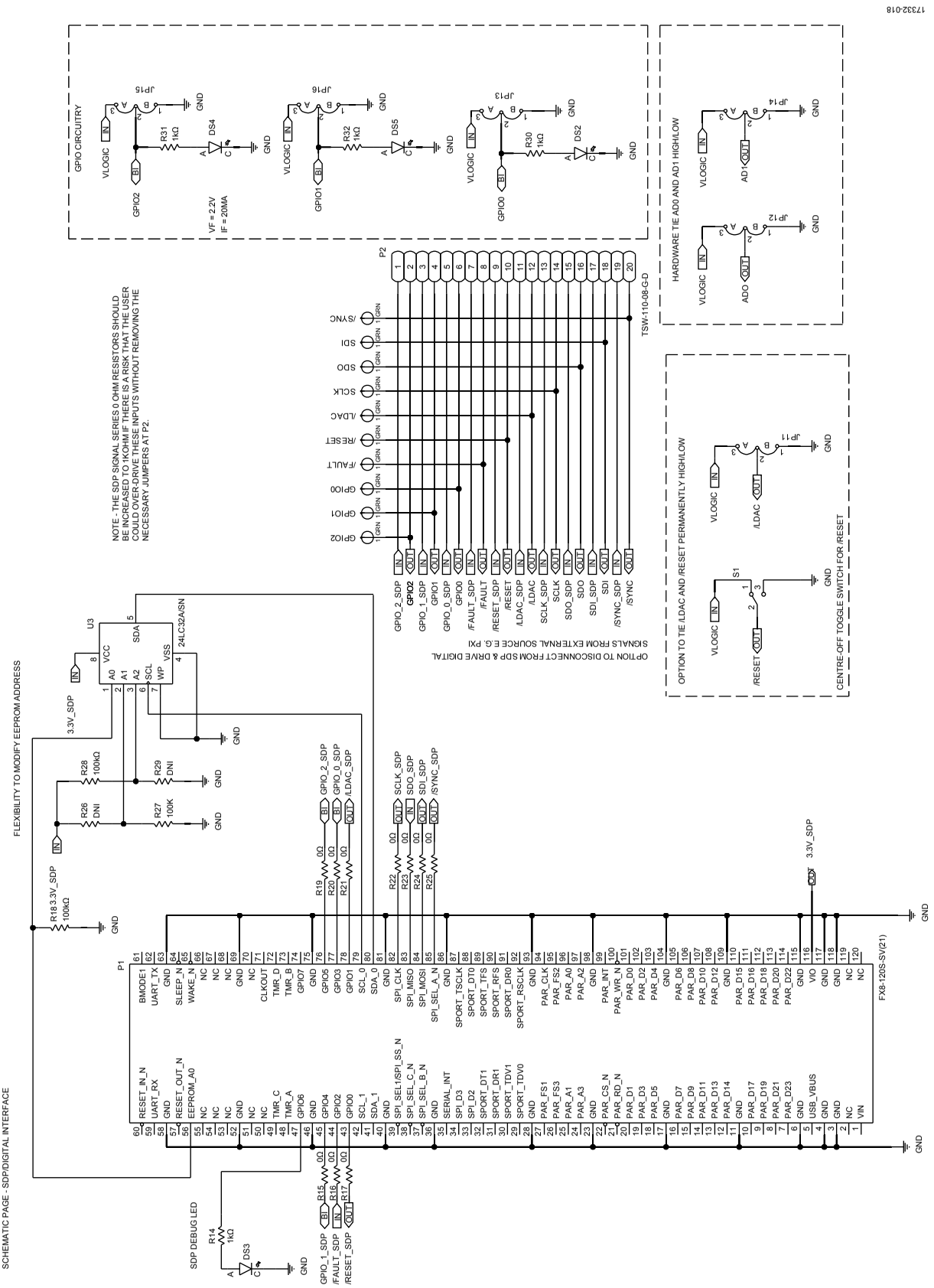

Figure 18. EVAL-SDP-CS1Z (SDP-S) Board Connections, Address Pins, $\overline{LDAC}$ Pins, and $\overline{RESET}$ Pins

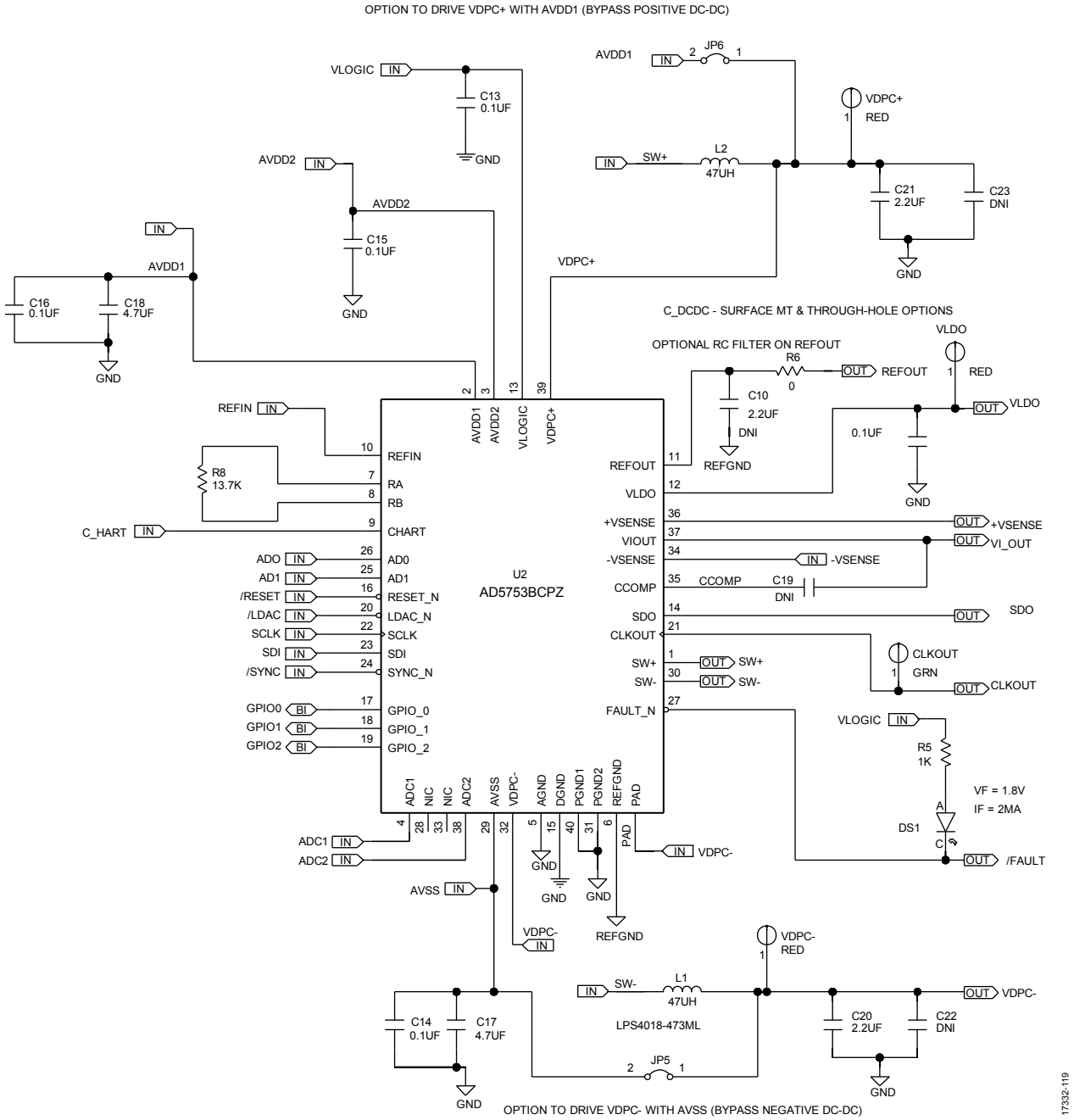

Figure 19. AD5753 Device

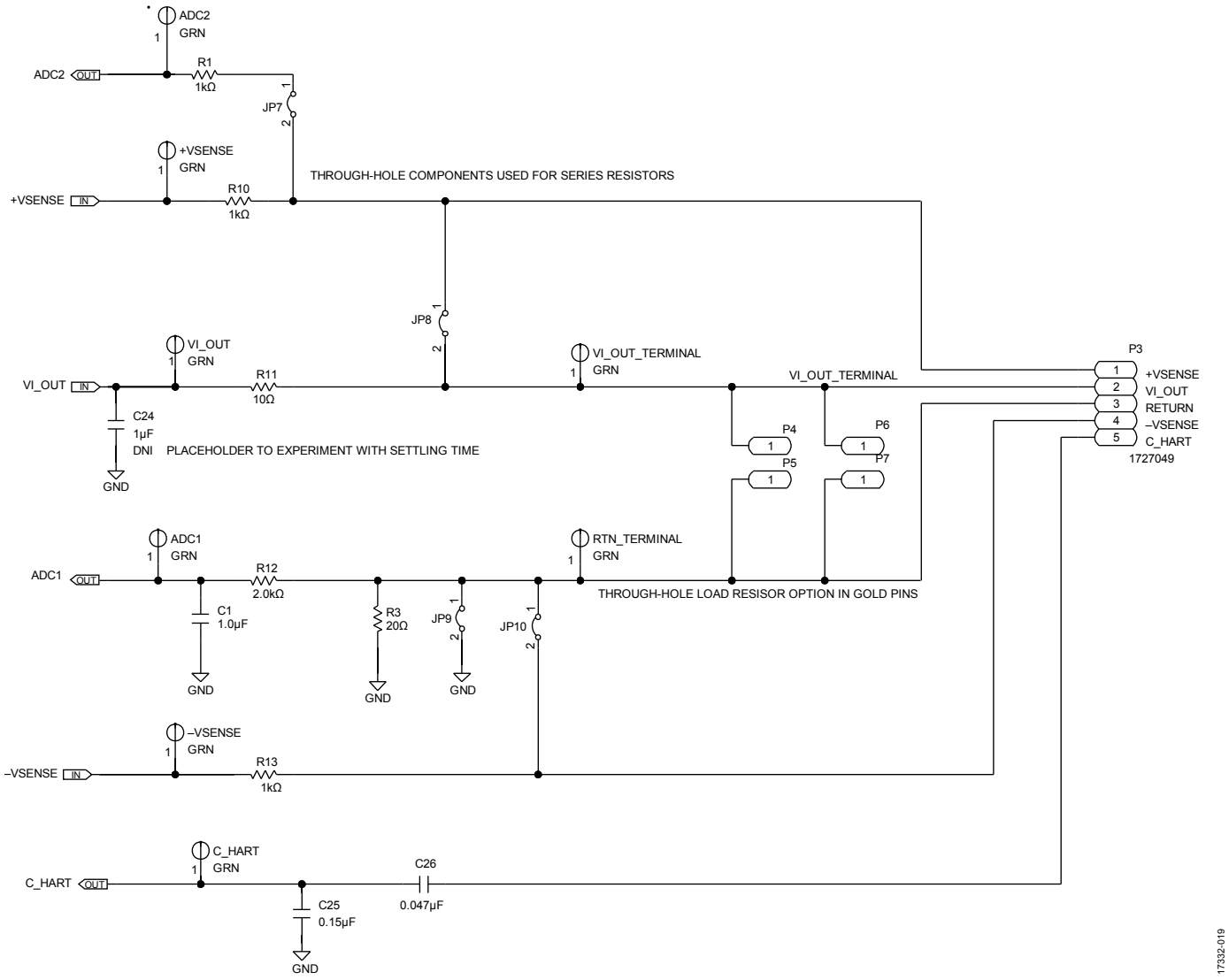

Figure 20. AD5753 Output Stage

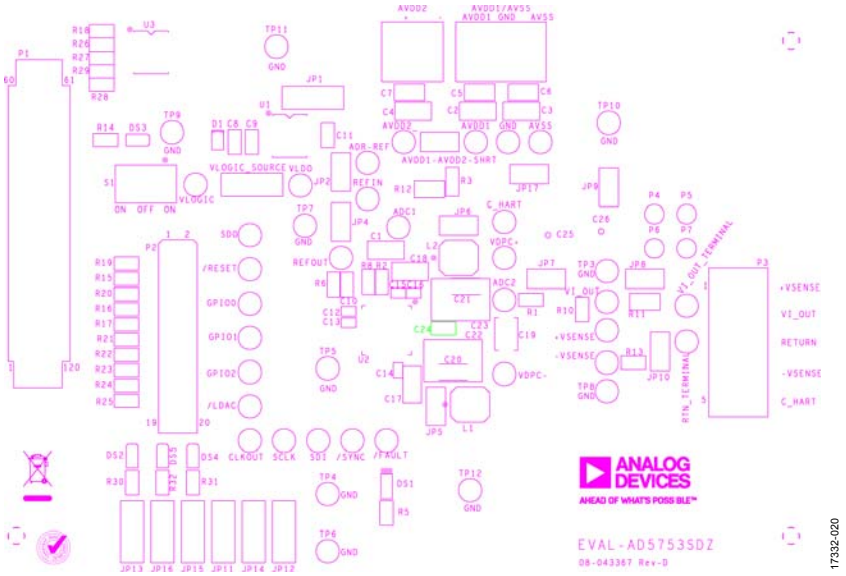

Figure 21. Silkscreen

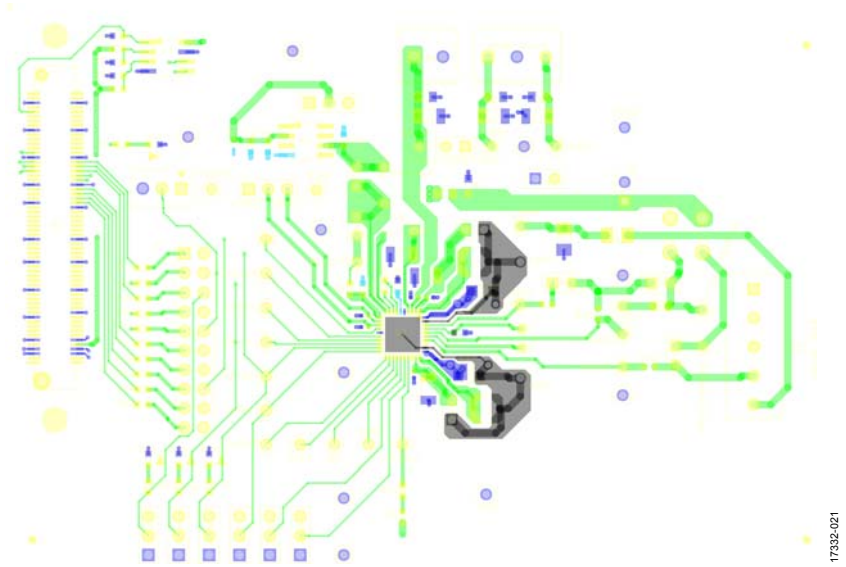

Figure 22. Layer 1

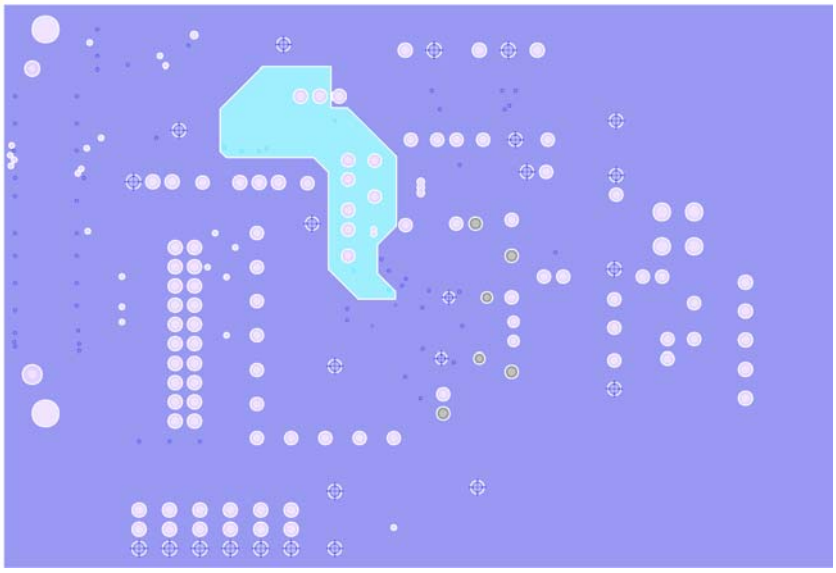

Figure 23. Ground and Power Plane, Layer 2, and Layer 3

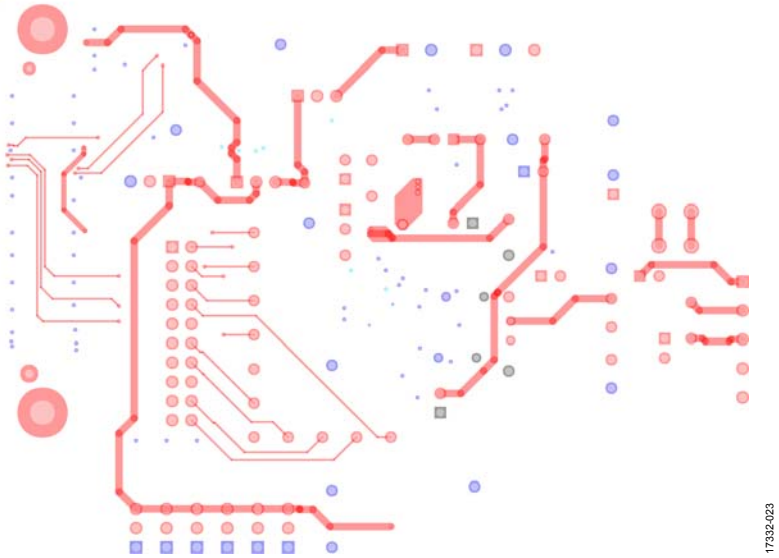

Figure 24. Layer 4 (Secondary)

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
+VSENSE, –VSENSE, $\overline{\text{FAULT}}$, $\overline{\text{LDAC}}$, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, ADC1, ADC2, CLKOUT, C_HART, GPIO0, GPIO1, GPIO2, RTN_TERMINAL, SCLK, SDI, SDO, VI_OUT, VI_OUT_TERMINAL	Test points, green	Vero Technologies	20-313138
ADR-REF, AVDD1, AVDD2_, AVSS, REFIN, REFOUT, VDPC+, VDPC–, VLDO, VLOGIC	Test points, red	Vero Technologies	20-313137
AVDD1-AVDD2-SHRT, JP2, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP17	Jumpers, male, 2-position, 1X M000385	Amphenol FCI	69157-102
AV_{DD1}/AV_{SS}	Terminal block, 3-position	Phoenix Contact	1727023
AV_{DD2}	Terminal block, 2-position, green	Phoenix Contact	1727010
C1	Ceramic capacitor, X7R, general-purpose	Yageo	CC1206KKX7R9BB105
C8, C11	Ceramic capacitors, X5R, general-purpose	AVX Corporation	06033D105KAT2A
C12, C13, C14, C15, C16	Ceramic capacitors, X7R	TDK	CGA2B3X7R1H104K050BB
C2, C3, C4, C17, C18	Ceramic capacitors, X7R, general-purpose	Murata	GRM31CR71H475KA12L
C20, C21	Ceramic capacitors, 2.2 µF, 50 V, 10%, X7R, 1206, automotive	Murata	GCM31CR71H225KA55K
C25	Ceramic capacitor, X7R, 1206	AVX Corporation	12065C154KAT2A
C26	Ceramic capacitor, X7R, 1206	AVX Corporation	12065C473JAT2A
C5, C6, C7	Ceramic capacitors, X7R	KEMET	C0805C104J5RACTU
C9	Ceramic capacitor, 0603 X7R	KEMET	C0603C104K3RACTU
D1	Zener voltage regulator	NXP Semiconductors	BZX585-C15
DS1	LED surface mount device (SMD), 0603, red	Vishay	TLMS1000-GS08
DS2, DS3, DS4, DS5	LED SMD, 0603, green	Lumex	SML-LX0603GW-TR
GND, TP3 to TP12	Test points, black	Vero Technologies	20-2137
JP1, JP11 to JP16, VLOGIC_SOURCE	Position male HDR unshrouded, single row, 2.54 mm pitch, 3 mm solder tail	Harwin	M20-9990345
L1, L2	Inductors, shielded power	Coilcraft, Inc.	LPS4018-473MRB
P1	Vertical type for SDP-S breakout board	HRS	FX8-120S-SV(21)
P2	Header, male 20-position	Samtec	TSW-110-08-G-D
P3	Term block, 5-position, green	Phoenix Contact	1727049
P4, P5, P6, P7	Pin sockets	Vero Technologies	66-3472
R1, R10, R13	Thick film chip resistors	Multicomp	MC0063W060311K
R11	Precision thick film chip resistor	Panasonic	ERJ-6ENF10R0V
R12	Thin film chip resistor, high reliability	Panasonic	ERA-6AEB202V
R5, R14, R30, R31, R32	Thick film chip resistors	Vishay	CRCW06031K00FKEAHP
R2, R15 to R17, R19 to R25	Film resistors, SMD, 0603	Multicomp	MC0603WG00000T5E-TC
R18, R27, R28	Thick film chip resistors, 0603, 1%, 100 kΩ	Multicomp	MC 0.063W
R3	Precision thin film chip resistor	TE Connectivity	CPF0603B20RE1
R6	Chip SMD resistor, precision power	Vishay	CRCW06030000Z0EA
R8	Thin film precision resistor	TE Connectivity	RN73C1J13K7BTG
S1	Switch tiny washable toggle switches	Apem Components	TL39P0050
U1	IC, Analog Devices ultralow noise, high accuracy VREF	Analog Devices	AD5752BRZ
U2	IC-ADI single-channel, 16-bit current or voltage output DAC, dynamic power control, highway addressable remote transducer (HART)® connectivity	Analog Devices	AD5753BCPZ-RL7
U3	IC 32-kBit serial EEPROM	Microchip Technology	24LC32A/SN

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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