EVAL-AD5758 User Guide
UG-1268

Evaluating the AD5758 Single-Channel, 16-Bit Current and Voltage Output DAC with Dynamic Power Control and HART Connectivity

FEATURES

Full featured evaluation board for the AD5758
On-board 2.5 V ADR4525 reference
On-board ADP1031-1 isolated PMU with integrated
   SPI signal isolation channels
ACE software for control

EVALUATION KIT CONTENTS

EVAL-AD5758SDZ evaluation board

EQUIPMENT NEEDED

EVAL-SDP-CS1Z board
Bench top power supply and connector cables

ADDITIONAL DOCUMENTS REQUIRED

AD5758 data sheet
ACE User Manual

SOFTWARE REQUIRED

ACE software for control

GENERAL DESCRIPTION

This user guide describes the evaluation board for the AD5758, a single-channel, voltage and current output, digital-to-analog converter (DAC) with on-chip dynamic power control (DPC) to minimize package power dissipation.

For full details, refer to the AD5758 data sheet. Consult the data sheet when using the EVAL-AD5758SDZ. The configuration of the various link options is explained in the Evaluation Board Hardware section. The installation of the companion software is discussed in the Evaluation Software Quick Start Procedures section.

The EVAL-AD5758SDZ, as shown in Figure 1, requires the EVAL-SDP-CS1Z board. The EVAL-AD5758SDZ interfaces to the USB port of the PC via the EVAL-SDP-CS1Z board. The Analysis|Control|Evaluation (ACE) software allows simplified programming of the AD5758, and is available with the EVAL-AD5758SDZ evaluation board.
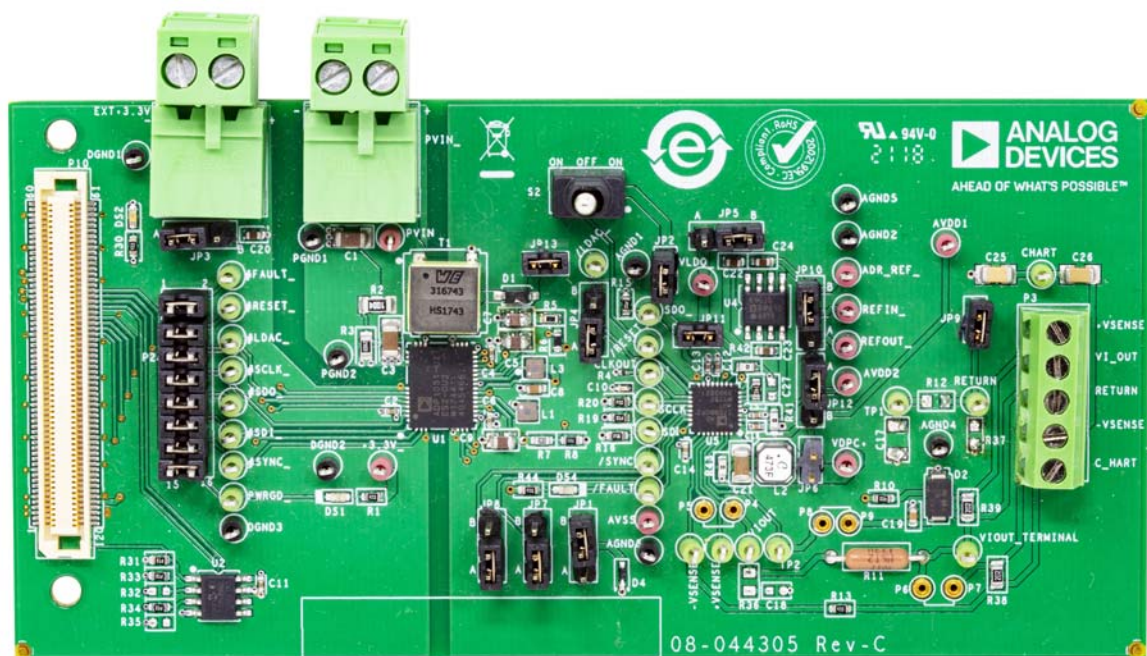
EVALUATION BOARD PHOTOGRAPH

Figure 1. EVAL-AD5758SDZ Evaluation Board

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REVISION HISTORY

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-AD5758SDZ evaluation board contains the ADP1031-1 power management unit (PMU), which generates three of four power supply inputs required by the AD5758: AV_{DD1} (+26.7 V), AV_{DD2} (+5.15 V), and AV_{SS} (−15.4 V), device. V_{LOGIC} is the fourth power supply required by the AD5758. The JP11 link provides the 3.3 V supply to the V_{LOGIC} input via the V_{LDO} output of the AD5758. The AV_{DD2} input can be connected to the AV_{DD1} input via the JP12 link if the V_{OUT2} supply from the ADP1031-1 is not in use. See Table 1 for link options and the default link positions.

The EVAL-AD5758SDZ evaluation board operates with a power supply range from −33 V on AV_{SS} to +33 V on AV_{DD1}, with a maximum voltage of 60 V between the two rails. AV_{DD2} requires a voltage between 5 V and 33 V. The V_{DPC+} pin of the AD5758 can be driven by AV_{DD1} via the JP6 link. The JP6 link bypasses the dc-to-dc circuitry.

SERIAL COMMUNICATION

The SDP-S system demonstration platform handles communication to the EVAL-AD5758SDZ via the PC. By default, the SDP-S board handles the serial port interface (SPI) communication, controls the $\overline{\text{RESET}}$ and $\overline{\text{LDAC}}$ pins, and monitors the $\overline{\text{FAULT}}$ pin of the AD5758.

The EVAL-AD5758SDZ evaluation board can disconnect from the SDP-S board and drive the digital signals from an external source by removing the appropriate links on the P10 link. The option to tie the $\overline{\text{RESET}}$ and $\overline{\text{LDAC}}$ pins to high or low levels can be accessed through the S2 and JP4 links.

AD5758 ADDRESS PINS

The AD5758 address pins, AD0 and AD1, are used in conjunction with the address bits within the SPI frame to determine which AD5758 device is being addressed by the system controller. The AD0 and AD1 pins can be configured through the JP7 and JP8 links.

Table 1. EVAL-AD5758SDZ Link Option Functions

Link	Default Link Position	Function
JP1	B	Position A selects the AV_{SS} pin to GND for the unipolar supply option (current output only).
		Position B selects the V_{OUT3} pin of the ADP1031-1.
JP2	Inserted	Connects the V_{LOGIC} pin of the AD5758 to the SVDD1 pin of the ADP1031-1.
JP3	A	Position A selects the 3.3 V output from the SDP-S to the MVDD pin of the ADP1031-1.
		Position B selects the 3.3 V input via the EXT+3.3V_ header to the MVDD pin of the ADP1031-1.
JP4	A	Position A connects the $\overline{\text{LDAC}}$ pin to GND. Position B connects the $\overline{\text{LDAC}}$ pin to the V_{LOGIC} pin.
JP5	A	Position A selects V_{OUT2} of the ADP1031-1 as the input voltage to the ADR4525.
		Position B selects the V_{LDO} pin as the input voltage to the ADR4525.
JP6	Not inserted	Shorts the V_{DPC+} pin to the AV_{DD1} pin, bypassing the positive dc-to-dc circuitry.
JP7	A	Position A connects the AD0 pin to GND. Position B connects the AD0 pin to the V_{LOGIC} pin.
JP8	A	Position A connects the AD1 pin to GND. Position B connects the AD1 pin to the V_{LOGIC} pin.
JP9	Inserted	Connects the return signal to GND.
JP10	B	Position A selects the REFOUT pin of the AD5758 as the input to the REFIN pin of the AD5758.
		Position B selects the ADR4525 output as the input to the REFIN pin.
JP11	Inserted	Selects 3.3 V output of the V_{LDO} pin to the V_{LOGIC} pin.
JP12	A	Position A selects V_{OUT2} of the ADP1031-1 as the input voltage to the AV_{DD2} pin.
		Position B selects the AV_{DD1} pin as the input voltage to the AV_{DD2} pin.
JP13	Inserted	Connects V_{OUT1} of the ADP1031-1 to the AV_{DD1} pin.
P10	Inserted	Provides options to disconnect from the SDP-S board and to drive digital signals from an external source. See Table 2 for the specific link options.
S2	Left	In the left position, this link connects the $\overline{\text{RESET}}$ pin to the V_{LOGIC} pin.
	Middle (default)	In the middle position (default), this link controls the $\overline{\text{RESET}}$ pin via the SDP-S board.
	Right	In the right position, this link connects the $\overline{\text{RESET}}$ pin to GND.

Table 2. Link Options for the P2_ Header

Pin No.	Position	Function
1, 2	Inserted	Connects the $\overline{\text{FAULT}}$ signal from the SDP-S to the MGP03 pin on the ADP1031-1.
	Not inserted	Disconnects the $\overline{\text{FAULT}}$ signal from the SDP-S to the MGP03 pin on the ADP1031-1
3, 4	Inserted	Connects the $\overline{\text{RESET}}$ signal from the SDP-S to the MGPI2 pin on the ADP1031-1.
	Not inserted	Disconnects the $\overline{\text{RESET}}$ signal from the SDP-S to the MGPI2 pin on the ADP1031-1.
5, 6	Inserted	Connects the $\overline{\text{LDAC}}$ signal from the SDP-S to the MGPI1 pin on the ADP1031-1.
	Not inserted	Disconnects the $\overline{\text{LDAC}}$ signal from the SDP-S to the MGPI1 pin on the ADP1031-1.
7, 8	Inserted	Connects the SCLK signal from the SDP-S to the MCK pin on the ADP1031-1.
	Not inserted	Disconnects the SCLK signal from the SDP-S to the MCK pin on the ADP1031-1.
9, 10	Inserted	Connects the SDO signal from the SDP-S to the MI pin on the ADP1031-1.
	Not inserted	Disconnects the SDO signal from the SDP-S to the MI pin on the ADP1031-1.
11, 12	Inserted	Connects the SDI signal from the SDP-S to the MO pin on the ADP1031-1.
	Not inserted	Disconnects the SDI signal from the SDP-S to the MO pin on the ADP1031-1.
13, 14	Inserted	Connects the $\overline{\text{SYNC}}$ signal from the SDP-S to the $\overline{\text{MSS}}$ pin on the ADP1031-1.
	Not inserted	Disconnects the $\overline{\text{SYNC}}$ signal from the SDP-S to the $\overline{\text{MSS}}$ pin on the ADP1031-1.
15, 16	Inserted	Connects the PWRGD signal from the SDP-S to the PWRGD pin on the ADP1031-1.
	Not inserted	Disconnects the PWRGD signal from the SDP-S to the PWRGD pin on the ADP1031-1.

EVALUATION SOFTWARE QUICK START PROCEDURES

INSTALLING THE ANALYSIS|CONTROL| EVALUATION (ACE) SOFTWARE AND AD5758 PLUG-INS

The EVAL-AD5758SDZ software uses the Analog Devices, Inc., ACE software. For instructions the use of the ACE software, see the www.analog.com/ACE product page.

When the installation completes, the EVAL-AD5758SDZ evaluation board plug-in appears when the ACE software opens (see Figure 2).
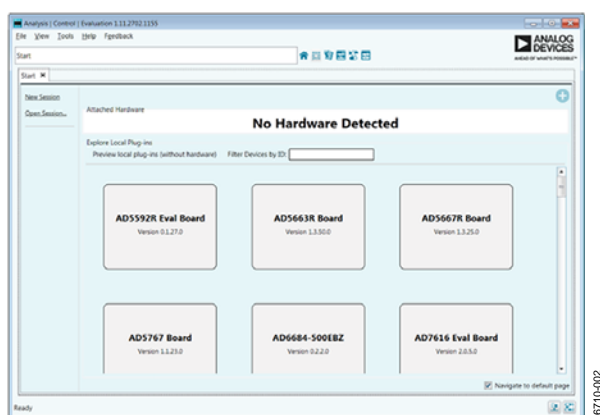
Figure 2. EVAL-AD5758SDZ Evaluation Board Plug-In Window after Opening the ACE Software

INITIAL SETUP

To set up the EVAL-AD5758SDZ, take the following steps:

1. Connect a USB cable to the PC and then to the SDP-S board.
2. Connect the SDP-S board to the EVAL-AD5758SDZ. The PC recognizes the EVAL-AD5758SDZ.
3. Power up the EVAL-AD5758SDZ with the relevant power supplies.
4. If not opened already, open the ACE software. The EVAL-AD5758SDZ appears in the **Attached Hardware** pane.
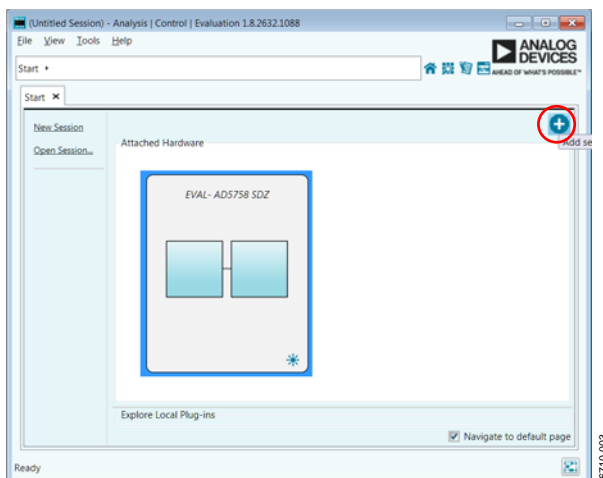
Figure 3. EVAL-AD5758SDZ Plug-In Not Installed

5. When setting up the evaluation board for the first time, the EVAL-AD5758SDZ plug-in may need to be installed. If the plug-in appears as shown in Figure 6, go to Step 7. If the plug-in appears as shown in Figure 3, click the button that is circled in red in Figure 3. After clicking this button, the pop-up window shown in Figure 4 appears. Click **Yes**.
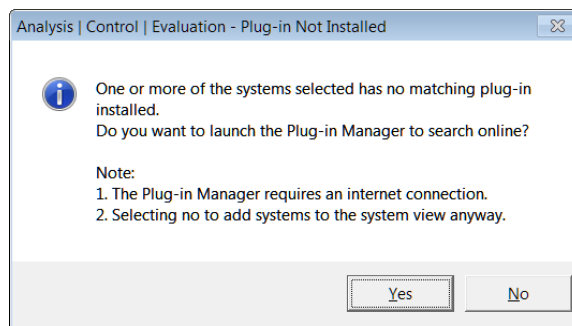
Figure 4. Installing Plug-In Pop-Up Window

6. A new window appears, as shown in Figure 5. Navigate to the **Board.AD5758** plug-in and click **Install Selected**. The EVAL-AD5758SDZ plug-in installs and is displays, as shown in Figure 6.
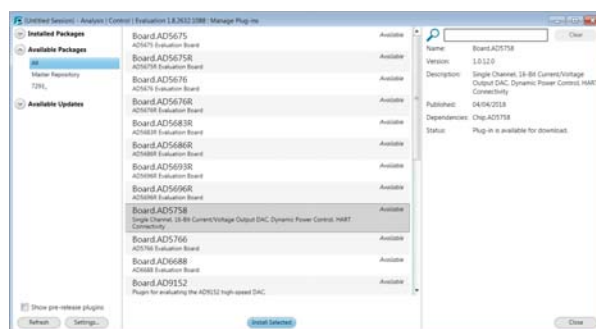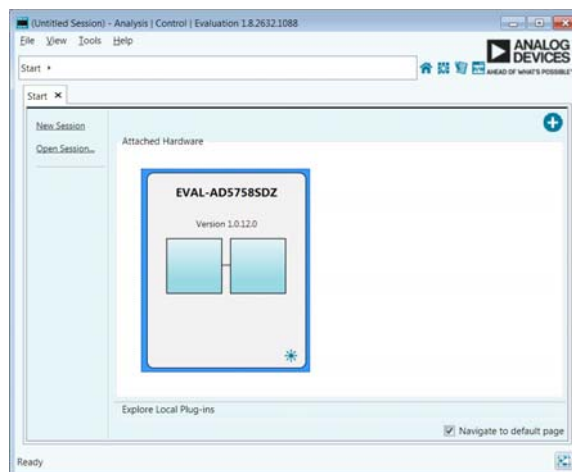
Figure 5. Plug-In Manager Window

Figure 6. Attached Hardware Pane with EVAL-AD5758SDZ Connection

7. Double-click **EVAL-AD5758SDZ** to open the AD5758 block diagram (see Figure 7). The **INITIAL CONFIGURATION** pane appears on the left side of the window. Several register settings can be configured in this pane and are written to the device in the appropriate order. The **DIG_DIAG_STATUS**, **RESET_OCCURED**, and **CAL_MEM_UNREFRESHED** LED indicators in the window are illuminated red by default.

Writing the initial configuration values clears these error flags. If the device is power cycled, or if the USB cable is disconnected and reconnected while the ACE software is open, contact with the EVAL-AD5758SDZ can be lost. If contact is lost, click the **System** tab, click the USB symbol on the **EVAL-AD5758SDZ**, and then click **Acquire** to communicate with the EVAL-AD5758SDZ.
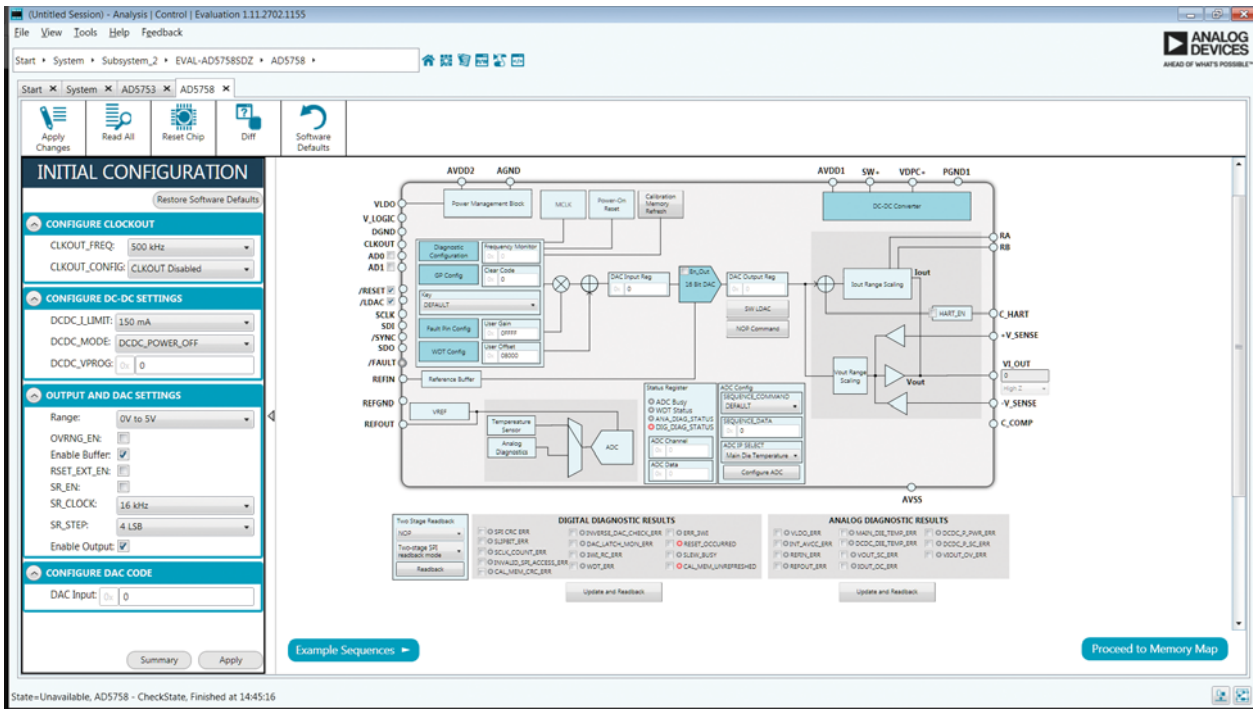

Figure 7. AD5758 Block Diagram in the ACE Software

AD5758 BLOCK DIAGRAM AND FUNCTIONS

The AD5758 ACE block diagram, as shown in Figure 8, appears similar to the block diagram shown in the AD5758 data sheet for simplified correlation to the functions on the EVAL-AD5758SDZ evaluation board with the descriptions given in the AD5758 data sheet.

A full description of each block and register setting is available in the AD5758 data sheet. The full screen AD5758 block diagram, with labels, is shown in Figure 8. Table 3 describes the functionality of each block.
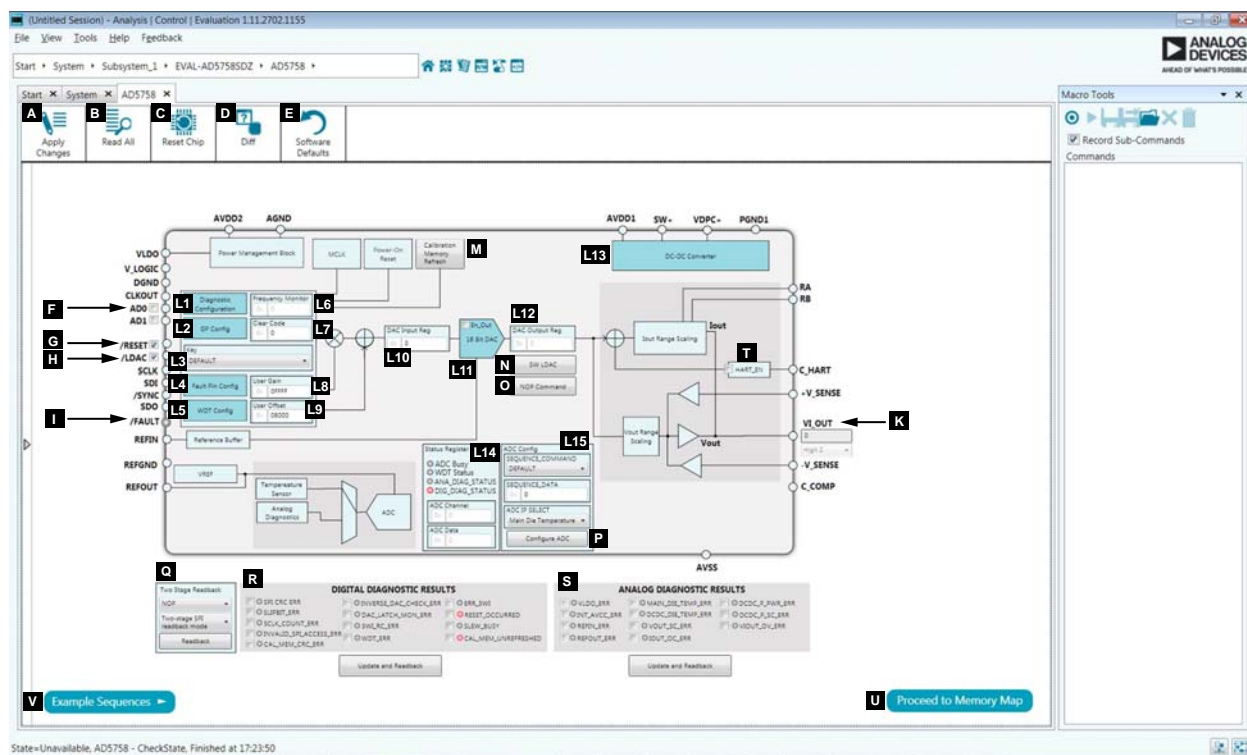

Figure 8. AD5758 Block Diagram with Labels

Table 3. AD5758 Block Diagram Label Functions (See Figure 8)

Label	Function Description
A	To apply any changes made to the block diagram or to register values in the memory map to the device, click **Apply Changes**.
B	To read back all of the registers of the device, click **Read All**.
C	Click **Reset Chip** to reset the AD5758. The **Reset Chip** button has the same functionality as the software reset of the AD5758.
D	Click **Diff** to show the registers that are different from the data stored on the device. This function shows what has changed since the last time the registers were read.
E	Click **Software Defaults** to load the software defaults of the device. These values are not written to the hardware. Click **Apply Changes** (Label A in Figure 8) to write the software default values to the hardware.
F	The **AD0** and **AD1** check boxes set the device under test (DUT) address of the device and must correspond to the JP12 and JP14 links on the hardware. If either box is checked, this represents a high state. If either box is unchecked, this represents a low state.
G	If the **/RESET** box is checked, the SDP-S sets the $\overline{RESET}$ pin high. Otherwise, the SDP-S pulls $\overline{RESET}$ low.
H	If the **/LDAC** box is checked, the SDP-S sets the $\overline{LDAC}$ pin high. Otherwise, the SDP-S pulls $\overline{LDAC}$ low.
I	The ACE plug-in monitors the $\overline{FAULT}$ pin. If the $\overline{FAULT}$ pin is low, the **/FAULT** indicator LED illuminates red.
K	The **VI_OUT** field displays the calculated output at the VI$_{OUT}$ pin and displays if the output is in volts, milliamperes, or is high impedance (high-Z).
Lx	The graphical user interface (GUI) access on several registers. Pop-ups, dropdown menu, and hexadecimal text fields are available in the GUI to configure several registers of the AD5758. To write the changes to the device, click **Apply Changes**. The functions within the GUI that control various registers (Label L1 through Label L15 in Figure 8) are described in Table 4.
M	The **Calibration Memory Refresh** button initiates a write to the key register to perform a calibration memory refresh.
N	The **SW LDAC** button initiates a write to the key register to perform a software $\overline{LDAC}$ command.
O	The **NOP Command** button initiates a write to Address 0x00 for a no operation (NOP) command.
P	The **Configure ADC** button writes the data selected in the **ADC Config** pane (Label L15) to the ADC configuration register.

Label	Function Description
Q	The **Two Stage Readback** pane initiates two-stage readback through the two-stage readback select register. Click **Readback** to initiate a write to the two-stage readback select register and issue a NOP command.
R	In the **DIGITAL DIAGNOSTIC RESULTS** pane, click **Update and Readback Digital Diagnostic Result** button to trigger a write 1 to clear operation and initiate a readback from the digital diagnostic result register.
S	In the **ANALOG DIAGNOSTIC RESULTS** pane, click **Update and Readback Analog Diagnostic Result** button to trigger a write 1 to clear operation and initiate a readback from the analog diagnostic result register.
T	If the **HART_EN** box is checked, the HART_EN bit = 1 in the General-Purpose Configuration 1 register.
U	Click **Proceed to Memory Map** to open the AD5758 memory map (see Figure 9).
V	Click **Example Sequences** to open the example sequences window (see Figure 15).

Table 4. Register Controls Accessible via the GUI (See Label Lx in Table 3 and in Figure 8)

| Label	Function Description
L1	The **Diagnostic Configuration** button activates the associated pop-up menu.
L2	When the **GP Config** button clicked, a pop-up menu appears.
L3	When the **Key** register menu is clicked, a dropdown list appears.
L4	When the **Fault Pin Config** button is clicked, a pop-up menu appears.
L5	When the **WDT Config** button is clicked, a pop-up menu appears.
L6	The **Frequency Monitor** text field displays the value in the frequency monitor when read.
L7	The **Clear Code** text field inserts a clear code value in hexadecimal format.
L8	The **User Gain** text field inserts a user gain value in hexadecimal format.
L9	The **User Offset** text field inserts a user offset value in hexadecimal format.
L10	The **DAC Input Reg** text field inserts the DAC value in hexadecimal format.
L11	The **16 Bit DAC** block opens a pop-up menu when clicked.
L12	The **DAC Output Reg** control displays the hexadecimal value currently set in the DAC output register.
L13	The **DC-DC Converter** block opens the dc-to-dc configuration pop-up menu.
L14	The **Status Register** pane displays the contents of the status register including any ADC conversion result.
L15	The **ADC Config** pane contains a combination of dropdown menus and a text field to enter the ADC input data.
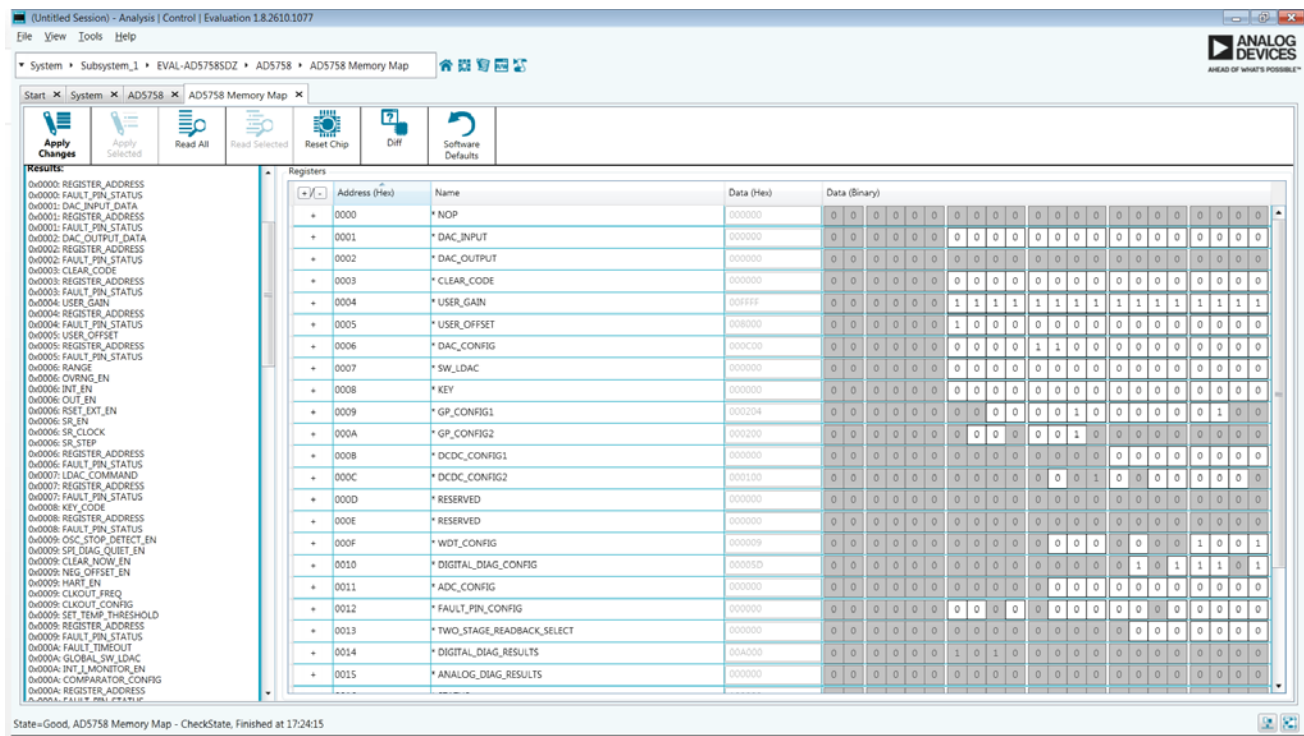
Figure 9. AD5758 Memory Map in the ACE Software

INITIAL CONFIGURATION

An initial configuration wizard is available when opening the AD5758 plug-in. The initial configuration wizard allows quick configuration of the AD5758 and provides configuration of the clock output in the general-purpose configuration register, the dc-to-dc settings, DAC configuration, and the DAC input register. Clicking the **Apply** button initiates the configured settings in the order of the recommended power-up sequence described in the AD5758 data sheet.

DC-TO-DC CONVERTER SETTINGS

If the V_{DPC+} pin is not tied directly to AV_{DD1}, enable the dc-to-dc converter for proper operation. This step must be completed before configuring the DAC output. The **DC-DC Configuration** pop-up menu, as shown in Figure 10, contains the dc-to-dc settings required to configure the AD5758 output properly. After the desired settings are selected, click the **Close** button and then click **Apply Changes**.
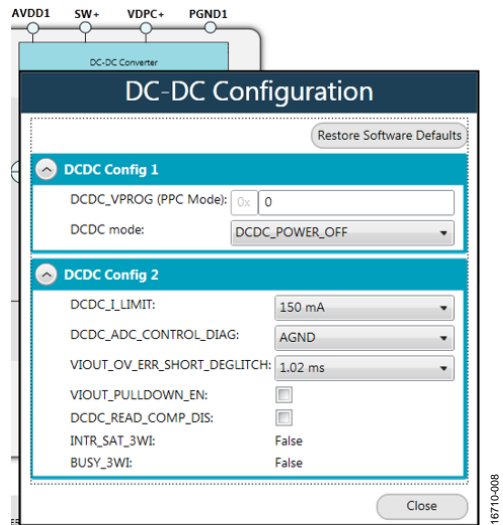

*Figure 10. **DC-DC Configuration** Pop-Up Menu*

SETTING THE DAC OUTPUT

To configure the DAC output, use the **DAC Config Register** pop-up menu (see Figure 11). Click the **16 Bit DAC** block in the block diagram to display the DAC configuration register. Select the appropriate settings, and then click **Apply Changes**. It is recommended to disable the output until the correct value in the DAC input register is written to the device.

To change the DAC voltage or current output level, write the appropriate hexadecimal code to the DAC input register, and then click **Apply Changes**. Click **SW LDAC** to issue a software LDAC command, or pull the LDAC pin low to update the DAC output register with the values in the DAC input register. Enable the DAC output by checking the **OUT_EN (Enable VI_OUT)** checkbox, and then click **Apply Changes**. The programmed voltage or current is then reflected at the VI$_{OUT}$ pin.
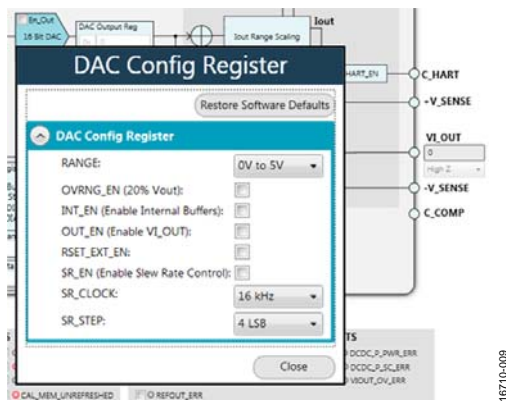

Figure 11. AD5758 **DAC Config Register** Pop-Up Menu

WRITING TO THE ADC CONFIGURATION REGISTER

The procedure to set up and configure the ADC input node is discussed in the AD5758 data sheet. For this reason, writing to the ADC configuration register through the **Apply Changes** function is disabled.

The dropdown list in the **SEQUENCE_COMMAND** pane contains only an initiate single conversion command. The hexadecimal tex field in the **SEQUENCE_DATA** pane is unused and remains at 0. The dropdown list in the **ADC_IP_SELECT** pane is used to select the desired input node for the ADC to conveirt. Click **Configure ADC** to initiate a write to the ADC configuration register. A register read must be performed to see the ADC result in the status register.
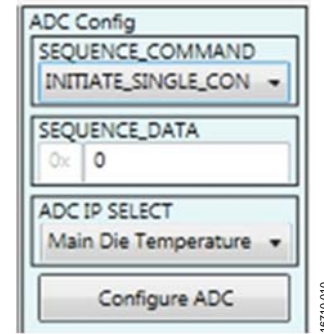

Figure 12. AD5758 ADC Configuration Register

UPDATING DIAGNOSTIC RESULTS

The AD5758 has a digital diagnostic results register and an analog diagnostic results register, which contain error flags for the on-chip digital and analog diagnostic features. Writing 1 to the respective error flags updates the error flag status.

To update the digital and analog diagnostic result registers, click **Update and Readback**. This button initiates the writing of a 1 to the selected error flag and then reads back the updated diagnostic result. Figure 13 shows the digital diagnostic results register. Figure 14 shows the analog diagnostic results register.
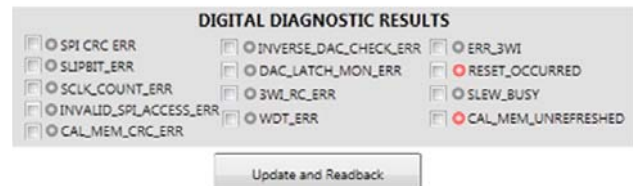

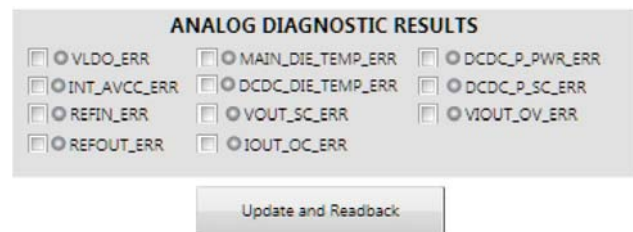Figure 13. AD5758 Digital Diagnostic Register

Figure 14. AD5758 Analog Diagnostic Register

EXAMPLE CONFIGURATION SEQUENCES

Several example configuration sequences are available. Click
Example Sequences, and the window shown in Figure 15 appears.
To enable any of the sequences, click the relevant sequence button,
as shown in Figure 16. The sequence runs immediately and the
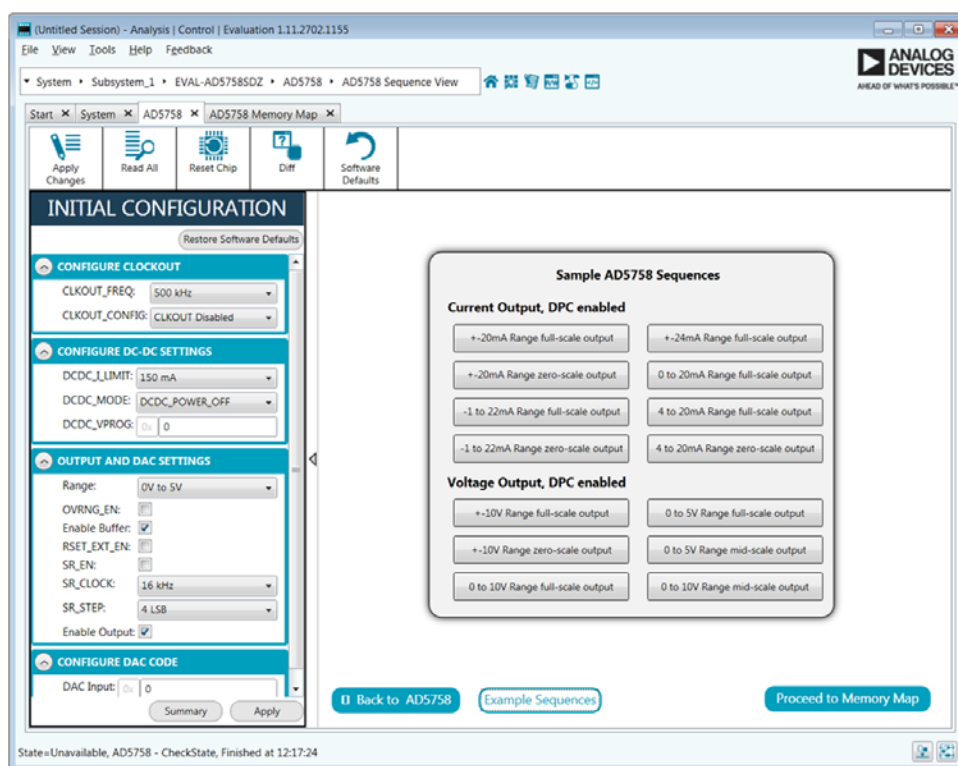output changes accordingly. To return to the main window, click
Back to AD5758.

Figure 15. Example Sequences Window

Figure 16. Selecting an Example Sequence

ACE TOOL VIEWS

The ACE software provides additional functionality to the main view described in this user guide. Open these views from the **View** menu on the application toolbar. The ACE software features a macro tool, a register debugger tool, and an events tool.

MACRO TOOL

The macro tool records and saves commands as an ACE macro file. This feature is useful when sharing macros with other users to perform the same task multiple times. The user can import and run an ACE macro file.

REGISTER DEBUGGER TOOL

Use the register debugger tool to perform raw writes to and reads from the device. The register debugger affects only the hardware and does not write to the memory map of the ACE software.

EVENTS TOOL

The events tool view contains a list of errors, warnings, and information messages generated within the application software.
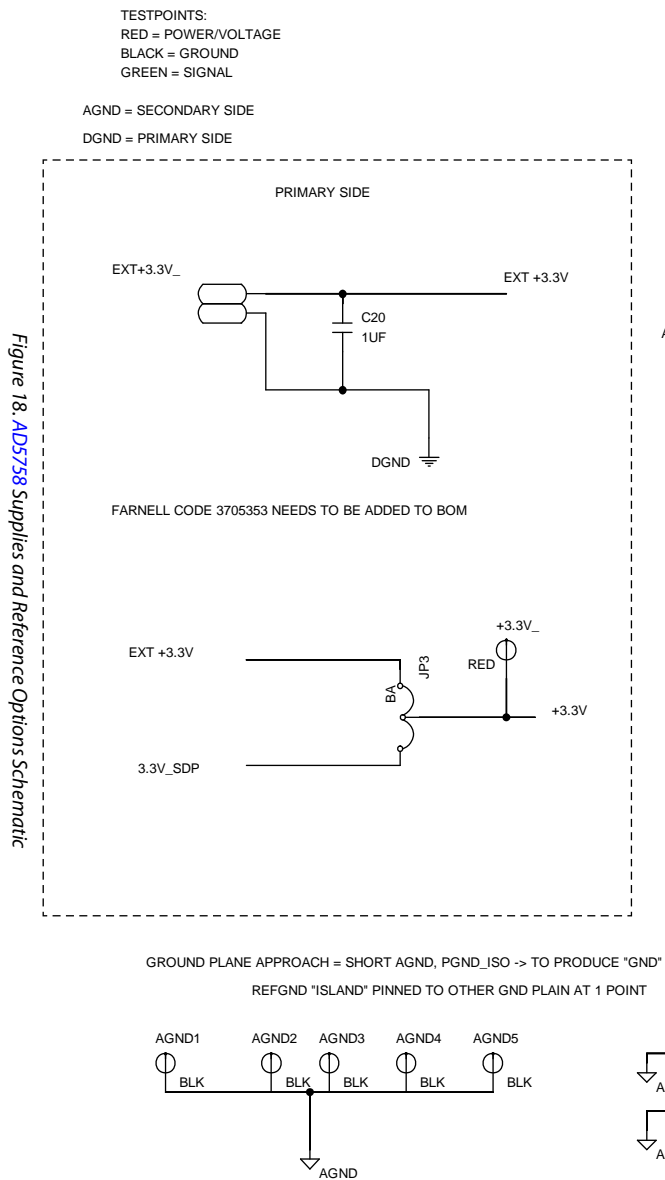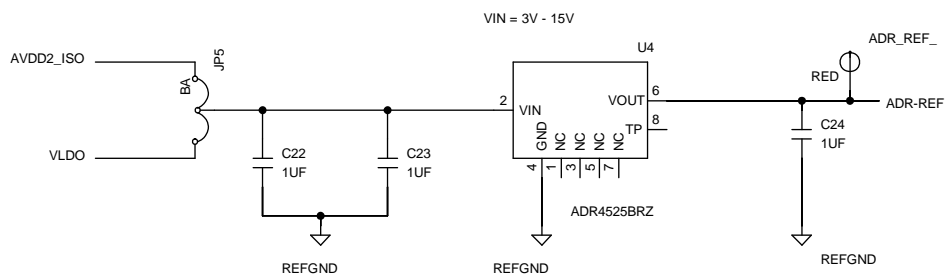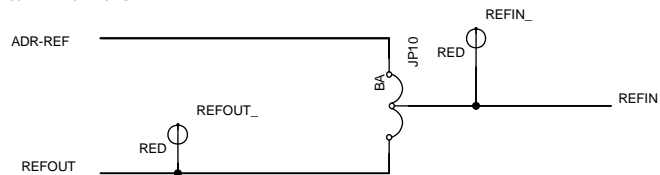
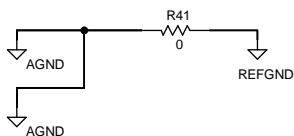Figure 17. AD5758 Schematic

TESTPOINTS:
RED = POWER/VOLTAGE
BLACK = GROUND
GREEN = SIGNAL

AGND = SECONDARY SIDE

DGND = PRIMARY SIDE

PRIMARY SIDE

EXT+3.3V_

EXT +3.3V

C20
1UF

DGND

FARNELL CODE 3705353 NEEDS TO BE ADDED TO BOM

EXT +3.3V

JP3

BA

RED

+3.3V_

+3.3V

3.3V_SDP

GROUND PLANE APPROACH = SHORT AGND, PGND_ISO -> TO PRODUCE "GND"

REFGND "ISLAND" PINNED TO OTHER GND PLAIN AT 1 POINT

AGND1   AGND2   AGND3   AGND4   AGND5

BLK   BLK   BLK   BLK   BLK

AGND

AGND

AGND

R41
0

REFGND

AD5758 REFIN OPTIONS

ADR-REF

JP10

BA

RED

REFIN_

REFIN

REFOUT_

RED

REFOUT

VIN = 3V - 15V

AVDD2_ISO

JP5

BA

VLDO

C22
1UF

C23
1UF

REFGND

U4

2   VIN

VOUT   6

GND   TP   8

NC   NC   NC   NC

4   1   3   5   7

ADR4525BRZ

REFGND

ADR_REF_

RED

ADR-REF

C24
1UF

REFGND

OPTION TO TIE /LDAC LOW & AD PINS PERMANENTLY HIGH/LOW

/LDAC

JP4

B

A

LDAC_N

AGND

VLOGIC

JP7

B

A

AD0

AGND

VLOGIC

JP8

B

A

AD1

AGND

RESET TOGGLE SWITCH

VLOGIC

/RESET

S2

TL39P0050

AGND
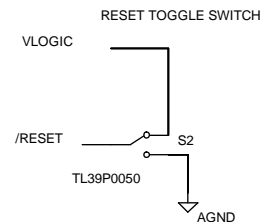
Figure 18. AD5758 Supplies and Reference Options Schematic
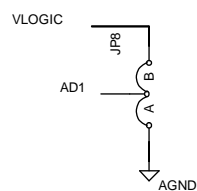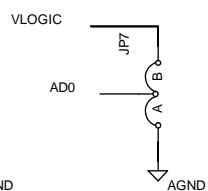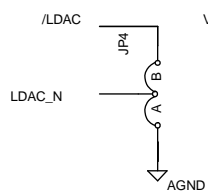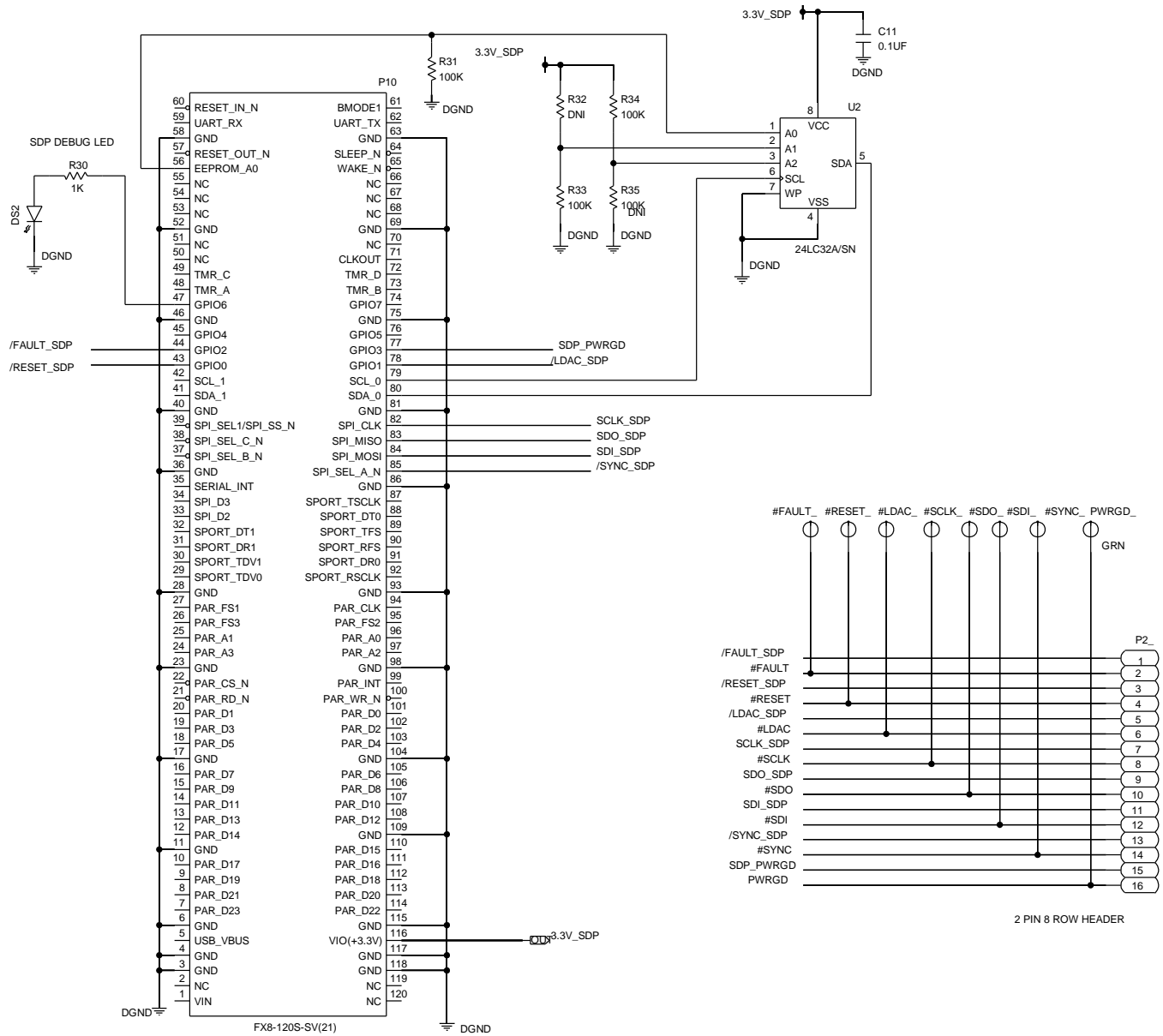
16710-014

Figure 19. SDP-S Board Connections, Address Pins, and $\overline{LDAC}$ and $\overline{RESET}$ Pins Schematic
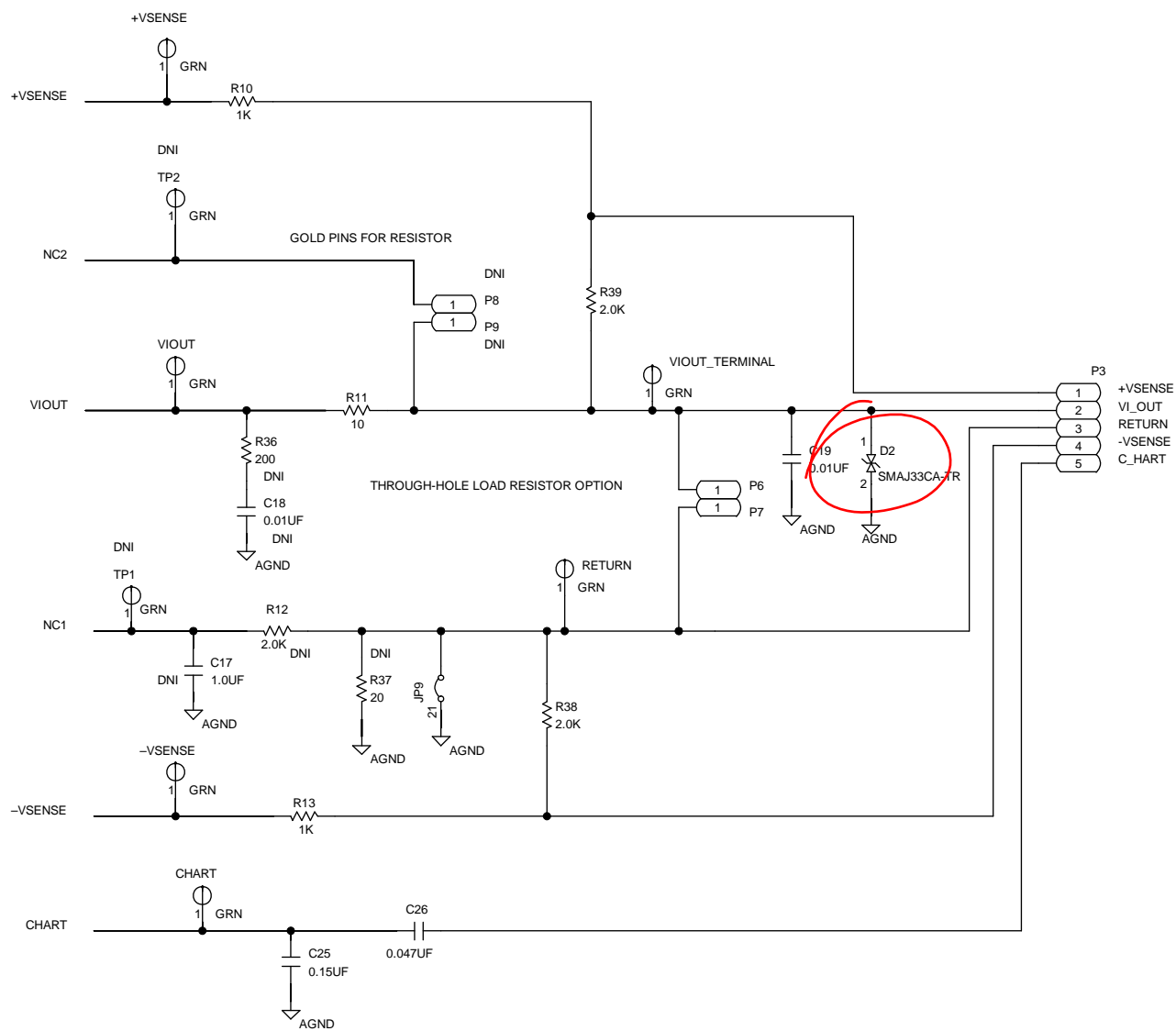
Figure 20. *AD5758 Output Stage Schematic*

FARNELL 3705353 NEEDS TO BE ADDED TO BOM

MINIMUM SUPPLY = 7V
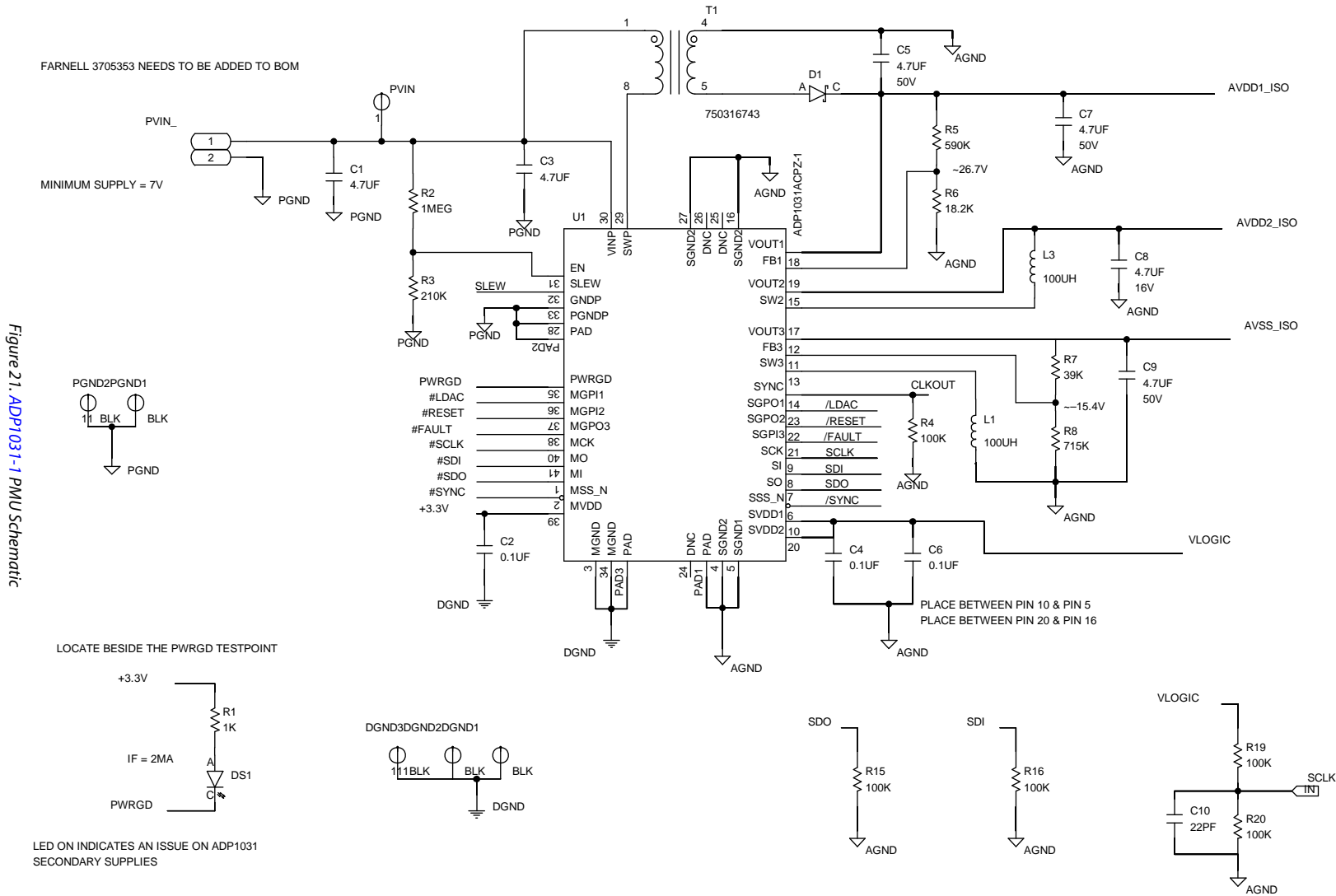
Figure 21. ADP1031-1 PMU Schematic

LOCATE BESIDE THE PWRGD TESTPOINT

IF = 2MA

LED ON INDICATES AN ISSUE ON ADP1031
SECONDARY SUPPLIES

PLACE BETWEEN PIN 10 & PIN 5
PLACE BETWEEN PIN 20 & PIN 16

16710-121

Figure 22. EVAL-AD5758, Silkscreen

Figure 23. EVAL-AD5758, Primary Layer

Figure 24. EVAL-AD5758 Ground Planes, Layer 2

Figure 25. EVAL-AD5758 Ground and Power Plane, Layer 3

Figure 26. EVAL-AD5758, Layer 4 (Secondary)

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Bill of Materials

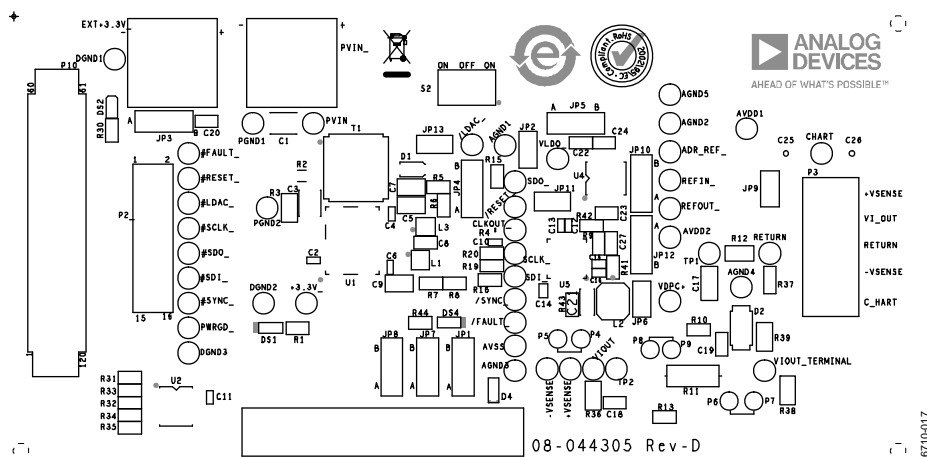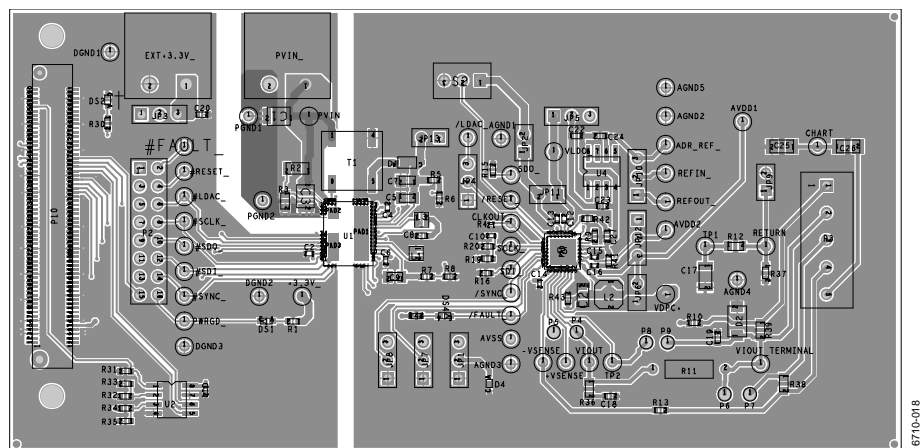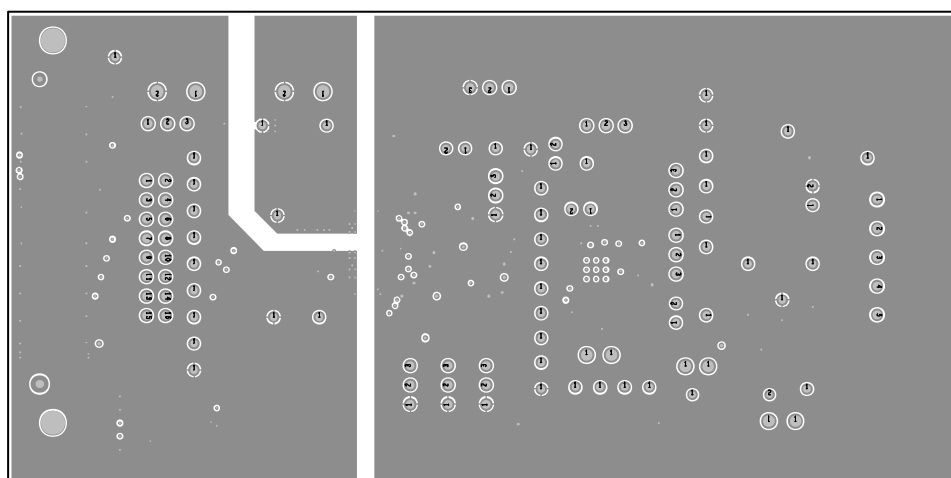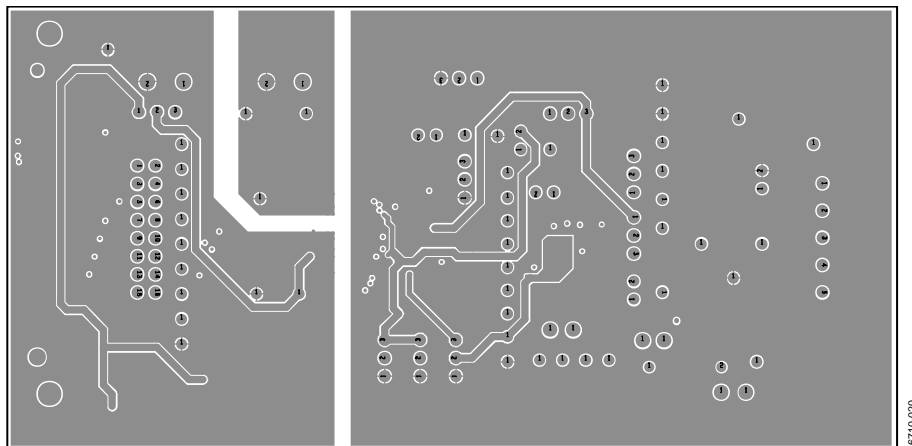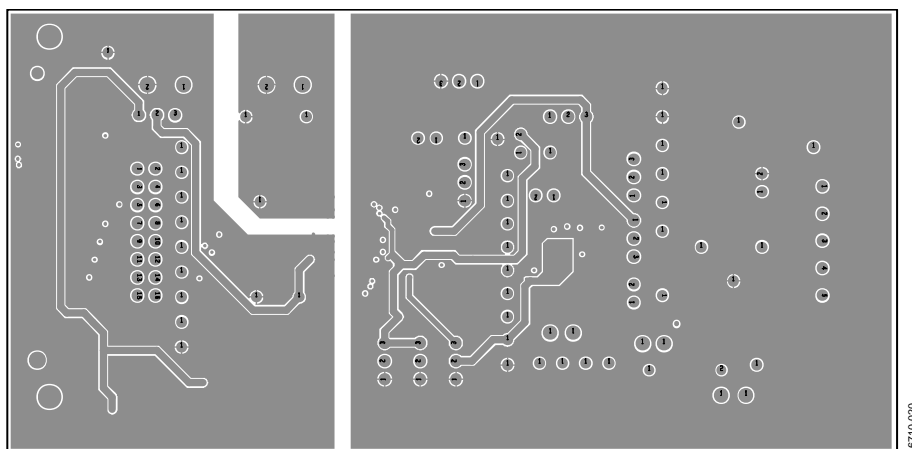| Reference Designator	Description	Manufacturer	Part Number
#FAULT_, #LDAC_, #RESET_, #SCLK_, #SDI_, #SDO_, #SYNC_, +VSENSE, VSENSE, /FAULT_, /LDAC_, /RESET_, /SYNC_, CHART, CLKOUT_, PWRGD_, RETURN, SCLK_, SDI_, SDO_, VIOUT, VIOUT_TERMINAL	Test point, green	Vero Technologies	20-313138
+3.3V_, ADR_REF_, AVDD1, AVDD2, AVSS, PVIN, REFIN_, REFOUT_, VDPC+, VLDO_	Test point, red	Vero Technologies	20-313137
AGND1, AGND2, AGND3, AGND4, AGND5, DGND1, DGND2, DGND3, PGND1, PGND2	Test point, black	Vero Technologies	20-2137
C1, C3	Multilayer ceramic capacitor (MLCC), X7S	TDK	CGA6M3X7S2A475K200AB
C10	Capacitor, ceramic, NP0	Yageo	CC0402JRNPO9BN220
C2, C4, C6, C11, C12, C13	Capacitor, ceramic, X5R	Taiyo Yuden	LMK105BJ104KV-F
C14, C15, C16	Capacitor, ceramic, X7R	TDK	CGA2B3X7R1H104K050BB
C19	Capacitor, ceramic, X7R	Yageo	CC0603KRX7R9BB103
C20, C22, C23, C24	Capacitor, ceramic, X7R	AVX	0603YC105KAT2A
C21	Capacitor, ceramic, 2.2 µF, 50 V, 10% X7R, 1206	Murata	GCM31CR71H225KA55K
C25	Capacitor, ceramic, X7R, 1206	AVX	12065C154KAT2A
C26	Capacitor, ceramic, X7R, 1206	AVX	12065C473JAT2A
C5, C7, C9	Capacitor, ceramic, X7R, general-purpose	Murata	GRM21BZ71H475KE15L
C8	Capacitor, ceramic, X6S, general-purpose	Murata	GRM188C81C475KE11D
D1	Diode, Schottky, rectifier, SMD	Diodes Incorporated	BAT46W-7-F
D2	Diode, TVS, bidirectional	STMicroelectronics	SMAJ33CA-TR
D4	Diode, Schottky, small signal	STMicroelectronics	BAT54KFILM
DS1, DS4	LED, SMD, 0603, red	Vishay	TLMS1000-GS08
DS2	LED, SMD, 0603, green	Lumex	SML-LX0603GW-TR
EXT+3.3V_, PVIN_	Connector, printed circuit board (PCB), two position terminal block header, single-row, 5.08 mm pitch	Phoenix Contact	1757242
JP1, JP3, JP4, JP5, JP7, JP8, JP10, JP12	Connector, PCB, three position, male, header, unshrouded, single-row, 2.54 mm pitch	Harwin	M20-9990345
JP2, JP6, JP9, JP11, JP13	Connector, PCB, BERG, male, two position, single-row, M000385	Amphenol	69157-102
L1, L3	Inductor, shielded power, 12.25 Ω dc resistance, 0.135 A	Coilcraft Inc.	XFL2006-104MEB
L2	Inductor, shielded power	Coilcraft Inc.	LPS4018-473MRB
P10	Vertical type receptacle for SDP breakout board	Hirose	FX8-120S-SV(21)
P2_	Connector, PCB, header, square post, straight, dual-row	Samtec	TSW-108-14-T-D
P3	Terminal block, five position, green	Phoenix Contact	1727049
P4, P5, P6, P7	Connector, PCB, pin socket	Vero Technologies	66-3472
R1, R10, R13, R30, R44	Resistor, thick film, chip	Multicomp	MC0063W060311K
R11	Resistor, metal film, industrial precision	Vishay	CMF5510R000FHEB
R15, R16, R20, R31, R33, R34	Resistor, thick film, chip	Multicomp	MC0063W06031100K
R2	Resistor, precision, thick film, chip, R1206	Panasonic	ERJ-8ENF1004V
R3	Resistor, precision, thick film, chip	Panasonic	ERJ-6ENF2103V
R38,R39	Resistor, thin film, chip, high reliability	Panasonic	ERA-6AEB202V
R4	Resistor, precision, thick film, chip	Panasonic	ERJ-1GNF1003C
R41, R42, R43	Resistor, chip, SMD	Vishay	CRCW06030000Z0EA

Reference Designator	Description	Manufacturer	Part Number
R5	Resistor, precision, thick film, 0603	Panasonic	ERJ-3EKF5903V
R6	Resistor, precision, thick film, R0603	Panasonic	ERJ-3EKF1822V
R7	Resistor, film, SMD, 0603	Multicomp	MC0063W0603139K
R8	Resistor, thick film, chip	Vishay	CRCW0603715KFKEA
R9	Resistor, thin film, precision	TE Connectivity	RN73C1J13K7BTG
S2	Switch, tiny, washable, toggle switches	Apem Components	TL39P0050
T1	Flyback transformer, EPX6, SMT	Wurth Elektronik	750316743
U1	Three-channel, isolated micropower management unit, seven digital isolators	Analog Devices	ADP1031ACPZ-1
U2	IC, 32 kb serial EEPROM	Microchip Technology	24LC32A/SN
U4	Ultralow noise, high accuracy voltage reference	Analog Devices	ADR4525BRZ
U5	16-bit, current and voltage output DAC, dynamic power control, HART connectivity	Analog Devices	AD5758BCPZ-REEL

Table 6. Bill of Materials (Uninserted Components)

Reference Designator	Description	Manufacturer	Part Number
C17	Capacitor, ceramic, X7R, general-purpose	Yageo	CC1206KKX7R9BB105
C18	Capacitor, ceramic, X7R	Yageo	CC0603KRX7R9BB103
C27	Capacitor, ceramic, X7R, general-purpose	Murata	GRM188R71A225KE15D
P8, P9	Connector, PCB, pin socket	Vero Technologies	66-3472
R12	Resistor, thin film, chip, high reliability	Panasonic	ERA-6AEB202V
R19, R32, R35	Resistor, thick film, chip	Multicomp	MC0063W06031100K
R36	Resistor, precision, thick film, chip	Panasonic	ERJ-6ENF2000V
R37	Resistor, precision, thin film, chip	TE Connectivity	CPF0603B20RE1
TP1, TP2	Connector, PCB test point, green	Vero Technologies	20-313138

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