Weiwei Chen

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EDUCATION

Ph.D. in Computer System and Software *Summer 2013 (expected)*
Department of Electrical Engineering and Computer Science GPA: 4.0/4.0
University of California, Irvine
Committee: Prof. Rainer Dömer, Prof. Daniel D. Gajski, Prof. Brian Demsky

M.S. in Computer Engineering *2007*
School of Microelectronics GPA: 3.88/4.0
Shanghai Jiao Tong University, China (National Entrance Exam Waiver)

B.Eng. in Computer Science and Engineering *2004*
Department of Computer Science and Engineering GPA: 3.7/4.0
Teaching Reform Class, Shanghai Jiao Tong University, China (National Entrance Exam Waiver)

International Exchange Student *2003*
School of Electrical and Computer Engineering GPA: 3.75/4.0
Purdue University, West Lafayette, Indiana (Dean's List and Semester Honor)

ACADEMIC EXPERIENCE

University of California, Irvine Irvine, CA
Graduate Student Researcher September 2007 - Present
Department of Electrical Engineering and Computer Science

- *Multi-core parallel simulation for System-Level Description Languages* **(9 publications)** Jun. 2009 - Present
  Platform/Languages/Technology: Linux / C/C++, SpecC / Multithreaded Programming,
  Design a synchronous parallel discrete event simulator which is scalable to run on multi-core platforms
  Propose an out-of-order parallel simulation approach which can achieve close to theoretic maximum speedup
  Propose an optimized compiler for static code analysis on system-level models for efficient parallel simulation
  Propose the concept of Segment Graph for C-based system-level description languages based on the control flow graph and language internal representation for simulation conflict checking and race condition detection

- *A SystemC System-level Description Language Frond-end Tool* Feb. 2013 - Present
  Platform/Languages/Technology: Linux / C/C++, SystemC / LLVM+Clang
  Design the software architecture of a SystemC front-end tool by using the *LLVM+Clang* compiler infrastructure, aiming at model analysis and code transformation for simulation on multi-core/many-core platforms
  Design and build the compiler internal representation for SystemC models, including the structural hierarchy, port binding information, simulation primitives, and so on

- *Recoding diagnosis for parallel system-level embedded application models* **(2 publications)** Jan. 2012 - Present
  Platform/Languages/Technology: Linux / C/C++, SpecC / Static Code Analysis
  Design and develop a dynamic race condition diagnosis tool for embedded system-level models
  Design and develop a static conflict detection kernel for an Eclipse-based recoding tool

- *System-level modeling and synthesis for embedded standard applications* **(3 publications)** Sept. 2007 - Present
  Platform/Languages/Technology: Linux / SpecC / System-Level Modeling
  Design and develop parallel system-level models for industrial-sized applications, such as a H.264 video decoder, a Mandelbrot / Julia set graphics application, a JPEG image encoder, a video edge detector, and a DES cipher chip

Pedagogical Fellow Academic year 2012-13
Teaching, Learning and Technology Center (TLTC)
The Henry Samueli School of Engineering

- *Henry Samueli Teaching Assistant Consultant* Sept. 2012 - Present
  Conduct teaching consultations with Teaching Assistants to help them reflect on their teaching experience, and identify the effective teaching methods and strategies

- *Teaching Assistant Professional Development Program (TAPDP 2012)* Sept 25 - 26, 2012
  Designed the curriculum and led this day-and-a-half discipline-specific, interactive workshop series to prepare graduate students with their instructional careers in UC Irvine. The workshops topics included TA responsibilities, learning styles, active learning strategies, problem solving skills, grading, leading discussion sessions, office hours, and so on

Teaching Assistant and Substitute Instructor September 2008 - Present
Department of Electrical Engineering and Computer Science

- *Advanced C Programming (EECS 22, EECS 22L)* Fall 2011, 2012, Winter 2013
  Computational Methods in Electrical and Computer Eng (EECS 10) Fall 2008, 2009, 2010, Summer 2012
  Led discussion and laboratory sections, designed learning activities, designed grading rubrics and scripts for automatic grading programming assignments, held office hours, managed online course message board, prepared the course accreditation (ABET) materials

- *Advanced System Software (EECS 211)* Winter 2011
  Gave two lectures for memory management in computer systems to graduate students as the substitute instructor

Shanghai Jiao Tong University Shanghai, China
Graduate Research Assistant December 2004 - January 2007

- Developed a symbolic analog circuit simulation using graph reduction approaches
- Researched on simulation for heterogeneous multiprocessor systems based on the SimpleScalar toolset
- Optimized MP3 decoder algorithm and developed an in-house operating system on the ARM9 platform
- Designed the digital circuit for a reconfigurable cache controller and external memory interface module in VerilogHDL

Teaching Assistant Spring 2005 - Fall 2006

- *FPGA Training Workshop*
  Gave lectures and designed the laboratory exercises on embedded system design by using the Xilinx FPGA Embedded Development Kit

- *Embedded System Design, Digital Integrated Circuit Design, Design Automation for Integrated Circuit*
  Mentored undergraduate students for embedded system design projects; prepared exam, homework, and laboratory assignments for the courses

INDUSTRY EXPERIENCE

Microsoft Seattle, WA
Software Development Engineer Intern June 2011 - September 2011

- Developed a Windows store application for secure banking with cloud roaming features on the Windows 8 Platform in Javascript (Windows 8 banking app with strong authentication sample)

IBM China System and Technology Lab (CSTL) Shanghai, China
R&D Engineer Intern June 2006 - April 2007

- Developed parallel high-performance sorting algorithms on the CELL Broadband Engine platform
- Research and development for system software for storage devices (C++ and Java) based on the OpenPegasus project

HONORS AND AWARDS

- Pedagogical Fellowship, UC Irvine, 2012-13 academic year
- Henry Samueli Endowed Fellowship, The Henry Samueli School of Engineering, UC Irvine, 2007
- Travel grants, Design Automation Conference (DAC) 2012 and Asia and South Pacific Design Automation Conference (ASP-DAC) 2010
- Young Student Support Award, Design Automation Conference (DAC), Anaheim, CA, 2010
- Excellent Teaching Assistant Award, School of Microelectronics, Shanghai Jiao Tong University, 2006
- National Scholarship for Academic Excellence, China, 2006
- First-round and second-round Exceptional Undergraduate Student, SJTU, 2001, 2003

SKILLS

Computer Languages	Proficient in C/C++, SpecC; Project experience in SystemC, Latex, Java, JavaScript, shell scripting, VerilogHDL, ARM and Motorola DSP assembly, Scheme
Programming Methods	Data Structure and Algorithms, Computational Complexity, Multithreaded Programming
Operating System	Linux / UNIX, Windows, Mac OS X
Applications	GCC, GDB, CVS, Git, Eclipse, Vim, etc.
Foreign Languages	speaks and writes fluently in Mandarin Chinese

SOFTWARE RELEASES

- *SpecC compiler version 2.2.2, Developer Release*
  Provided the parallel simulation kernel, the out-of-order parallel simulation kernel, the static code analyzer in the compiler, the race condition diagnosis tool, and extended the simulator support for the SoC Environment (SCE) toolset
- *Tool support, System-on-Chip Description and Modeling course (EECS222A), UC Irvine*
  Provided the compiler and simulator infrastructure for the Eclipse IDE tool for the recoding projects of this course
- *Embedded application models in the example repository for the SoC Environment (SCE) toolset*
  Designed an H.264 video decoder model (40k+ lines of code), a JPEG image encoder (2.5k+ lines of code), a video edge detector, and a DES cipher chip model

PUBLICATIONS

Journal Articles (peer reviewed)

J1. **Weiwei Chen**, Xu Han, Rainer Dömer, "Multi-Core Simulation of Transaction Level Models using the System-on-Chip Environment", *IEEE Design & Test of Computers*, vol.28, no.3, pp.20-31, May-June 2011

J2. **Weiwei Chen**, Xu Han, Che-Wei Chang, Rainer Dömer, "Advances in Parallel Discrete Event Simulation for Electronic System-Level Design", accepted for publication in *IEEE Design & Test of Computers*, to appear in 2013

J3. **Weiwei Chen**, Xu Han, Che-Wei Chang, Rainer Dömer, "Out-of-Order Parallel Discrete Event Simulation for Transaction Level Models", in preparation for submission to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2013

Conference Papers (peer reviewed)

C1. **Weiwei Chen**, Guoyong Shi, "Implementation of a Symbolic Circuit Simulator for Topological Network Analysis", in Proceedings of *the IEEE Asia Pacific Conference on Circuit and System (APCCAS)*, pp.1368-1372, Singapore, December 2006

C2. Guoyong Shi, **Weiwei Chen**, C.-J. Richard Shi, "A Graph Reduction Approach to Symbolic Circuit Analysis", in Proceedings of *the 12th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.197-202, Yokohama, Japan, January 2007

C3. Rongrong Zhong, Yongxin Zhu, **Weiwei Chen**, Mingliang Lin, Weng Fai Wong, "An Inter-core Communication Enabled Multi-core Simulator Based on SimpleScalar", in Proceedings of *the 21st International Conference on Advanced Information Networking and Applications Workshops (AINAW)*, pp.758-763, Niagara Falls, Canada, April 2007

C4. **Weiwei Chen**, Rainer Dömer, "A Fast Heuristic Scheduling Algorithm for Periodic ConcurrenC Models", in Proceedings of *the 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.161-166, Taipei, Taiwan, January 2010

C5. **Weiwei Chen**, Xu Han, Rainer Dömer, "ESL Design and Multi-Core Validation using the System-on-Chip Environment", in Proceedings of *the 15th IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.142-147, Anaheim, USA, June 2010

C6. Rainer Dömer, **Weiwei Chen**, Xu Han, Andreas Gerstlauer, "Multi-Core Parallel Simulation of System-Level Description Languages", invited paper, in Proceedings of *the 16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.311-316, Yokohama, Japan, January 2011

C7. **Weiwei Chen**, Rainer Dömer, "An Optimizing Compiler for Out-of-Order Parallel ESL Simulation Exploiting Instance Isolation", in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.461-466, Sydney, Australia, January 2012

C8. Rainer Dömer, **Weiwei Chen**, Xu Han, "Parallel Discrete Event Simulation of Transaction Level Models", invited paper, in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.227-231, Sydney, Australia, January 2012

C9. **Weiwei Chen**, Xu Han, Rainer Dömer, "Out-of-order Parallel Simulation for ESL design", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.141-146, Dresden, Germany, March 2012

C10. **Weiwei Chen**, Che-Wei Chang, Xu Han, Rainer Dömer, "Eliminating Race Conditions in System-Level Models by using Parallel Simulation Infrastructure", in Proceedings of *the IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.118-123, Huntington Beach, USA, November 2012

C11. **Weiwei Chen**, Rainer Dömer, "Optimized Out-of-Order Parallel Discrete Event Simulation Using Predictions", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.3-8, Grenoble, France, March 2013

C12. Xu Han, **Weiwei Chen**, Rainer Dömer, "Designer-in-the-Loop Recoding of ESL Models using Static Parallel Access Conflict Analysis", accepted for publication in *the workshop on Software and Compilers for Embedded Systems (SCOPES)*, June 2013

Book Chapters

BC1. **Weiwei Chen**, Guoyong Shi, "Symbolic Analysis of Analog Integrated Circuits", *Embedded Systems and Materials Research for Advanced Applications, the 1st Chinese-German Summer School in Shanghai*, September, 2006, ISBN-10: 3-00-019576-9 / ISBN-13: 978-3-00-019576-1

BC2. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A New Approach towards Effective Abstraction of C-based SLDLs", *Analysis, Architectures and Modeling of Embedded Systems (ed. A. Rettberg, M. Zanella, M. Amann, M. Keckeisen, F. Rammig)*, Springer, 2009, ISBN 978-3-642-04283-6

Technical Reports

TR1. **Weiwei Chen**, Rainer Dömer, "System Specification of a DES Cipher Chip", *TR-08-01*, Center for Embedded Computer System, UC Irvine, January 2008

TR2. **Weiwei Chen**, Siwen Sun, Bin Zhang, Rainer Dömer, "System Level Modeling of a H.264 Decoder", *TR-08-10*, Center for Embedded Computer System, UC Irvine, August 2008

TR3. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A Novel Model of Computation for Effective Abstraction of C-based SLDLs", *TR-09-07*, Center for Embedded Computer System, UC Irvine, May 2009

TR4. **Weiwei Chen**, Rainer Dömer, "A Distributed Parallel Simulator for Transaction Level Models with Relaxed Timing", *TR-11-02*, Center for Embedded Computer Systems, UC Irvine, May 2011

TR5. Xu Han, **Weiwei Chen**, Rainer Dömer, "A Parallel Transaction-Level Model of H.264 Video Decoder", *TR-11-03*, Center for Embedded Computer Systems, UC Irvine, June 2011

Presentations

- *IESS'09, ASP-DAC'10, ASP-DAC'12, DATE'12, DAC'12, HLDVT'12, DATE'13*

ASSOCIATION MEMBERSHIP AND ACTIVITIES

- IEEE Computer Society Student Member, since 2008
- Vice Commodore and Capri Skipper, UCI Sailing Association

WORKING STATUS

- International student, F-1 visa

References are available upon request!