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A Symbolic Analog Circuit Simulator

Author： CHEN, Weiwei

Advisor Ⅰ: Prof. SHI, Guoyong

Advisor Ⅱ: Prof. FU, Yuzhuo

ABSTRACT

Many topological approaches to symbolic network analysis have been proposed in the literature, but none are implemented ultimately as a simulator for large network analysis due to their complexity and exponentially increasing number of terms. A novel methodology adopted in this paper uses a graph reduction approach based on a set of graph reduction rules developed recently. A Binary Decision Diagram (BDD) is used in the implementation of the symbolic circuit simulator described in this thesis. With sharing and other manipulations of BDD, high simulation and evaluation performance is achieved.

The thesis is organized as follows. A brief introduction to symbolic analysis is in Chapter 1. The graph reduction rules and corresponding algorithms are presented in Chapter 2. Implementation details on the symbolic simulator are discussed in Chapter 3. Experimental results are reported in Chapter 4. In Chapter 5, approximate circuit analysis approaches are introduced. Conclusions and future work are reported in Chapter 6.

The simulator in this thesis is probably the first one ever capable of analyzing large analog circuits directly from the circuit topology.

KEYWORDS: Symbolic Analysis, Binary Decision Diagram, Graph Reduction, Heuristic Ordering

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