Weiwen Jiang

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Research Interests and Specialties

- **Co-Design of Neural Architecture and Hardware Accelerators:** we are the first propose co-design frameworks to explore neural architectures and FPGAs, ASICs, CiM, and Quantum Computing Platforms [1][2][4][5][6][7][8][10][11][12][13][24][25][26][27][28][29][30][31].
- **General Embedded System Design and Optimization:** especially for (1) heterogeneous pipelined MPSoCs [3][15][32][33][38]; (2) asynchronous embedded systems [14][17][18][19][34][35][36][37]; (3) NoC-based MPSoCs [20][21][22][42].
- **Emerging Techniques:** especially for non-violate memory based system design and optimization [9][11][16][23][24][40][43].

Employment

University of Notre Dame (PI: Dr. Yiyu Shi) JUN. 2019 – NOW. NOTRE DAME, U.S.
- **Postdoctoral Researcher in the Department of Computer Science and Engineering**. Focus on the co-exploration of neural architectures and hardware design, including qauntum computer.

University of Notre Dame JAN. 2020 – MAY. 2020 NOTRE DAME, U.S.
- **Teaching Assisitant**. CSE20221, Logical Design and Sequential Circuit.

East China Normal University APR. 2019 – APR. 2020 SHANGHAI, CHINA
- **Guest Research Fellows** in Big Data and Intelligent System Lab.

Education

University of Pittsburgh (PI: Dr. Jingtong Hu) OCT. 2017 – JUN. 2019 PITTSBURGH, U.S.
- **Joint Ph.D. program in the Department of Electrical and Computer Engineering**. Focus on the co-exploration of neural architecture and hardware design.

Chongqing University (Advisor: Dr. Edwin Sha) SEP. 2013 – JUN. 2019 CHONGQING, CHINA
- **Ph.D. degree in Computer Science**. Focus on the embedded system design and optimizations: designing high-performance and low-cost heterogeneous pipelining systems.

Nanjing Agriculture University SEP. 2008 – JUN. 2012. JIANGSU, CHINA
- **Bachelor degree in Computer Science**. Major in Network Engineering.

Awards

Best Paper Nomination in ASP-DAC 2020 (12 out of 263 submissions) 01/2020. BEIJING

Best Paper Nomination in CODES+ISSS 2019 (3 out of 74 submissions) 10/2019. NEW YORK

Best Paper Nomination in DAC 2019 (5 out of 815 submissions) 06/2019. LAS VEGAS

Best Paper Award in ICCD 2017 (5 out of 258 submissions)	11/2017. BOSTON
Best Student Paper in ESTC 2017	11/2017. CHINA
Best Paper Nomination in ASP-DAC 2016	01/2016. MACAO
Best Paper Award in NVMSA 2015	08/2015. HONGKONG
Editor's pick of the year 2016 in IEEE TC	12/2016. USA
China National Scholarship (1% among all postgraduate students)	11/2017. CHINA

Research & Other Grants

- **Co-PI, NSF-IIS**, "RAPID: Collaborative Research: Independent Component Analysis Inspired Statistical Neural Networks for 3D CT Scan Based Edge Screening of COVID-19", 07/01/2020 - 06/30/2021, $98,349
- **Co-PI, Facebook Research Funding** - Towards On-Device AI, "Hardware/Software Co-Exploration of Multi-Modal Neural Architectures Targeting AR/VR Glasses", 04/01/20 - 04/01/21, $75,000
- **PI, NSF-I/UCRC**, "Software Defined FPGA Hardware and Co-Exploration for Real-Time Applications", from EdgeCortix Inc. via NSF IUCRC ASIC center, 10/01/19 - 09/30/20, $100,000
- **PI, IBM-ND**, "Co-Design Neural Netwok and Quantum Circuit Towards Quantum Advantage", IBM & University of Notre Dame Quantum program, 11/01/19 - now, accessing to IBM Q system
- Research Opportunities Week (ROW) at the Technical University of Munich (TUM), 04/20/2020-04/27/2020 (Cancelled due to COVID-19)
- IEEE Council on Electronic Design Automation (CEDA) for ESWEEK'19, $1,000
- Grants from ACM SIGDA to participate the HALO workshop in ICCAD'19
- Travel grants from ACM to attend FPGA'19
- Scholarship from SIGDA and IEEE CEDA to attend PhD Forum at DAC'18
- Scholarship from SIGDA and Microsoft to participate Student Research Competition at ICCAD'17

Proposal Writing

NSF CCF-SPX (2019): Collaborative Research: Scalable Neural Network Paradigms to Address Variability in Emerging Device based Platforms for Large Scale Neuromorphic Computing (Awarded $344,132, PI: Yiyu Shi, No. 1919167)

NSF CNS Core: Small (2020): Intermittent and Incremental Inference with Statistical Neural Network for Energy-Harvesting Powered Devices (Awarded $480,272, PI: Yiyu Shi, No. 2007302 and PI: Jingtong Hu, No. 2007274)

NSFC (2019): On the Design and Optimization of Efficient Intelligent Heterogeneous Computing Pipelining Systems (Awarded $100,000, PI: Edwin Sha, No. 61972154)

Teaching Experience

High-Performance Parallel Computing (TA for Dr. Edwin Sha)	2014 – 2015. CHONGQING UNIV.
INVESTING NOW summer program (Volunteer)	JULY 2018. UNIV. OF PITTSBURGH.
Logic Design and Sequential Circuits (TA, CSE20221)	2020. UNIV. OF NOTRE DAME
Machine Learning for Embedded Systems (Instructor, CSE60685)	2020. UNIV. OF NOTRE DAME

Mentor of Students

- Hailiang Dong (Master) [3][16][33][38][39], First Employer: Ph.D at University of Texas at Dallas

- Xinchi Li (Master) [39], First Employer: Tencent in Chengdu
- Yutong Liang (Master) [41], First Employer: PingCAP Inc. in Beijing
- Zhulin Ma (Ph.D. candidate) [16]
- Xinyi Zhang, 2017-Now. (Ph.D. candidate at University of Pittsburgh) [1][2][30]
- Qing Lu, 2018-Now. (Ph.D. candidate at University of Notre Dame) [28][31]
- Zheyu Yan, 2019-Now. (Ph.D. candidate at University of Notre Dame) [11][27]
- Dewen Zeng, 2020-Now. (Ph.D. candidate at University of Notre Dame)
- Zhuorui Zhao, 2020-Now. (Ph.D. candidate at University of Notre Dame)
- Hanjing Zhu, 2020-Now. (Undergraduate student at University of Notre Dame)
- Yuhong Song, 2020-Now. (Master student at East China Normal University)
- Panjie Qi, 2020-Now. (Master student at East China Normal University)
- Shan Hao, 2020-Now. (Master student at East China Normal University)

Refereed Publications

Three Representative Papers

[1] **W. Jiang**, X. Zhang, E. H.-M. Sha, L. Yang, Q. Zhuge, Y. Shi, and J. Hu, "Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search," *Proc. Design Automation Conference* (***DAC***), Las Vegas, NV, USA, June. 2019. (5 out of 815 submissions, **BEST PAPER NOMINATION**)

[2] **W. Jiang**, E. H.-M. Sha, X. Zhang, L. Yang, Q. Zhuge, Y. Shi and J. Hu, "Achieving Super-Linear Speedup across Multi-FPGA for Real-Time DNN Inference", International Conference on Hardware/Software Co-design and System Synthesis (CODE+ISSS@New York), also appears at ACM Transactions on Embedded Computing Systems (TECS), 2019. (3 out of 74 submissions, **BEST PAPER NOMINATION**)

[3] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, H. Dong and X. Chen, "On the Design of Minimal-Cost Pipeline Systems Satisfying Hard/Soft Real-Time Constraints," *IEEE International Conference on Computer Design* (***ICCD@Boston***) and *in IEEE Transactions on Emerging Topics in Computing* (***TETC***), Jan. 2018. (5 out of 258 submissions, **BEST PAPER AWARD**)

Under Review and Work-in-Progress

[4] **W. Jiang**, J. Xiong, and Y. Shi, "A Co-Design Framework of Neural Networks and Quantum Circuits Towards Quantum Advantage", *undergoing second-round review in* ***Nature Communications***.

[5] **W. Jiang**, Y. Ding, J. Xiong, and Y. Shi, "Universal Approximability of Quantum Neural Networks with Quantum Advantages Demonstrated by Complexity Bound Analysis", *working towards a submission to* ***ICLR-2021***.

[6] Q. Lu, **W. Jiang**, X. Xu, Sakyasingha Dasgupta, Jingtong Hu and Yiyu Shi, "Weightless Neural Architecture Search: Rethinking Quantization-Aware Training of Neural Networks", *submitting to Conference on Artificial Intelligence* (***AAAI-21***).

[7] Y. Song, **W. Jiang**, B. Li, Q. Zhuge, E. H.-M. Sha, S. Dasgupta, Y. Shi, C. Ding, "Dancing along Battery: Enabling Transformer with Run-time Reconfigurability", *submitting to Conference on Artificial Intelligence* (***AAAI-21***).

Journal Paper

[8] Y. Ding, **W. Jiang**, Q. Lou, J. Liu, J. Xiong, X. Sharon Hu, X. Xu, and Y. Shi, "The Impact of Neural Networks' Competency-Awareness on Hardware Design", *accepted by* ***Nature Electronics***, *Aug. 2020*

[9] **W. Jiang**, B. Xie, C-C Liu and Y. Shi, "Integrating Memristors and CMOS for Better AI", *accepted by **Nature Electronics** (**News and Views**)*, Sep. 2019

[10] **W. Jiang**, L. Yang, S. Dasgupta, J. Hu, and Y. Shi, "Standing on the Shoulders of Giants: Hardware and Neural Architecture Co-Search with Hot Start", Accepted by International Conference on Hardware/Software Co-design and System Synthesis (CODE+ISSS), also appears at IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), 2020.

[11] **W. Jiang**, Q. Lou, Z. Yan, L. Yang, J. Hu, X. Hu, and Y. Shi, "Device-Circuit-Architecture Co-Exploration for Computing-in-Memory Neural Accelerators", *submitted to IEEE Transactions on Computers (**TC**)*.

[12] **W. Jiang**, L. Yang, E. H.-M Sha, Q. Zhuge, S. Gu, S. Dasgupta, Y. Shi and J. Hu, "Hardware/Software Co-Exploration of Neural Architectures", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), Mar. 2020*.

[13] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "Heterogeneous FPGA-based Cost-Optimal Design for Timing-Constrained CNNs", *accepted by CASES 2018 (in ESWEEK)* and *appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*.

[14] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines", *in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, May. 2018.

[15] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Yang, L. Zhou and Q. Zhuge, "Optimal Functional-Unit Assignment for Heterogeneous Systems under Timing Constraint," *in IEEE Transactions on Parallel and Distributed Systems (**TPDS**)*, 28(9): 2567-2580, 2017.

[16] E. H.-M. Sha, **W. Jiang**, H. Dong, Z. Ma, R. Zhang, X. Chen and Q. Zhuge, "Towards the Design of Efficient and Consistent Index Structure with Minimal Write Activities for Non-Volatile Memory", *in IEEE Transactions on Computers (**TC**)*, 67(3): 432-448, 2018.

[17] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and Lin Wu, "Efficient Assignment Algorithms to Minimize Operation Cost for Supply Chain Networks in Agile Manufacturing," *in Computers & Industrial Engineering*, 108: 225-239, 2017.

[18] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Wu and Q. Zhuge, "Synthesizing Distributed Pipelining Systems with Timing Constraints via Optimal Functional Unit Assignment and Communication Selection," *in Journal of Computational Science*, 26: 332-343, 2018.

[19] **W. Jiang**, Q. Zhuge, X. Chen, L. Yang, J. Yi and E. H.-M. Sha, "Properties of Self-Timed Ring Architectures for Deadlock-Free and Consistent Configuration Reaching Maximum Throughput," *in Journal of Signal Processing Systems*, 84(1): 123-137, 2016.

[20] W. Liu, L. Yang, **W. Jiang**, L. Feng, N. Guan, W. Zhang and N. Dutt, "Thermal-aware Task Mapping on Dynamically Reconfigurable Network-on-Chip based Multiprocessor System-on-Chip", *in IEEE Transactions on Computers (**TC**)*, 2018.

[21] L. Yang, W. Liu, **W. Jiang**, M. Li, P. Chen and E. H.-M. Sha, "FoToNoC: A Folded Torus-Like Network-on-Chip based Many-Core Systems-on-Chip in the Dark Silicon Era," *in IEEE Transactions on Parallel and Distributed Systems*, Dec. 2016. DOI:10.1109/TPDS.2016.2643669.

[22] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip-Based Multiprocessor System-on-Chip With Fine-Grain Communication Optimization" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 24(10): 3027-3040, Oct. 2016.

[23] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "A New Design of In-Memory File System Based on File Virtual Address Framework," *in IEEE Transactions on Computers*, 65(10):2959-2972, Oct. 2016.

[24] X. Chen, E. H.-M. Sha, Q. Zhuge, C. J. Xue, **W. Jiang** and Y. Wang, "Efficient data placement for improving data access performance on domain-wall memory" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 24(10): 3094-3104, 2016.

Conference Paper

[24] D. Zeng, **W. Jiang**, T. Wang, X. Xu, H. Yuan, M. Huang, J. Zhuang, J. Hu and Y. Shi, "Towards Cardiac Intervention Assistance: Hardware-Aware Neural Architecture Exploration for Real-Time 3D Cardiac Cine MRI Segmentation," *Proc. of IEEE/ACM International Conference on Computer-Aided Design* (***ICCAD***), 2020 (Invited Paper)

[25] S. Bian, X. Xu, **W. Jiang**, Y. Shi and T. Sato, "BUNET: Blind Medical Image Segmentation Based on Secure UNET", *Proc. Medical Image Computing and Computer Assisted Interventions* (***MICCAI***), Lima, Peru, 2020

[26] X. Yan, **W. Jiang**, Y. Shi and C. Zhuo, "MS-NAS: Multi-Scale Neural Architecture Search for Medical Image Segmentation", *Proc. Medical Image Computing and Computer Assisted Interventions* (***MICCAI***), Lima, Peru, 2020

[27] L. Yang, Z. Yan, M. Li, H. Kwon, L. Lai, T. Krishna, V. Chandra, **W. Jiang***, Y. Shi, "Co-Exploration of Neural Architectures and Heterogeneous ASIC Accelerator Designs Targeting Multiple Tasks", *Proc. Design Automation Conference* (***DAC***), San Francisco, July 19-23. (* corresponding author)

[28] S. Bian, **W. Jiang**, Q. Lu, Y. Shi, and T. Sato, "NASS: Optimizing Secure Inference via Neural Architecture Search", *submitted to 24th European Conference on Artificial Intelligence* (***ECAI'20***)

[29] L. Yang, **W. Jiang**, W. Liu, E. H.-M. Sha, Y. Shi and J. Hu, "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence," *Proc. Asia and South Pacific Design Automation Conference* (***ASP-DAC***), Beijing, Jan. 2020. (**BEST PAPER NOMINATION**)

[30] X. Zhang, **W. Jiang**, Y. Shi and J. Hu, "When Neural Architecture Search Meets Hardware Implementation: from Hardware Awareness to Co-Design," *Proc. IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI*), Miami, Florida, USA, Aug. 2019. (Invited Paper)

[31] Q. Lu, , **W. Jiang**, X. Xiao, J. Hu and Y. Shi, "On Neural Architecture Search for Resource-Constrained Hardware Platforms," *Proc. IEEE/ACM International Conference On Computer-Aided Design* (*ICCAD*), Westminster, CO, 2019. (Invited paper)

[32] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and X. Chen, "Optimal Functional-Unit Assignment and Buffer Placement for Probabilistic Pipelines," *Proc. International Conference on Hardware/Software Co-design and System Synthesis* (***CODES+ISSS***), Pittsburgh, PA, USA, Oct. 2016.

[33] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, H. Dong and X. Chen, "Optimal Functional Unit Assignment and Voltage Selection for Pipelined MPSoC with Guaranteed Probability on Time Performance," *Proc. Languages, Compilers, and Tools for Embedded Systems* (***LCTES***), Barcelona, Spain, Jun. 2017.

[34] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, L. Yang and X. Chen, "On the Design of High-Performance and Energy-Efficient Probabilistic Self-Timed Systems," *Proc. High Performance Computing and Communications* (***HPCC***), NewYork, NY, USA, Aug. 2015.

[35] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "Prevent Deadlock and Remove Blocking for Self-Timed Systems," *Proc. International Conference on Algorithms and Architectures for Parallel Processing* (***ICA3PP***), Zhangjiajie, China, Nov. 2015.

[36] **W. Jiang**, E. H.-M. Sha, X. Chen, Q. Zhuge and L. Wu, "Optimal Functional Assignment and Communication Selection under Timing Constraint for Self-Timed Pipelines," *Proc. IEEE International Conference on Embedded Software and Systems* (***ICESS***), Chengdu, China, Aug. 2016.

[37] **W. Jiang**, Q. Zhuge, J. Yi, L. Yang and E. H.-M. Sha, "On self-timed ring for consistent mapping and maximum throughput," *Proc. Embedded and Real-Time Computing Systems and Applications* (***RTCSA***), Chongqing, China, Aug. 2014.

[38] E. H.-M. Sha, H. Dong, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "On the Design of Reliable Heterogeneous Systems via Checkpoint Placement and Core Assignment," *Proc. Great Lakes Symposium on VLSI* (*GLSVLSI*), Chicago, IL, USA, May. 2018.

[39] X. Li, Q. Zhuge, **W. Jiang**, H. Dong, W. Lin, X. Chen and E. H.-M. Sha, "A Research of Reducing Write Activities in Multi-table Join for Non-Volatile Memories," *Proc. 15th CCF Annual Conference on Embedded Systems* (*ESTC*), Shenyang, China, Nov. 2017. (**BEST STUDENT PAPER AWARD**)

[40] X. Chen, E. H.-M. Sha, **W. Jiang**, Q. Zhuge, J. Chen, J. Qin, Y. Zeng, "The Design of an Efficient Swap Mechanism for Hybrid DRAM-NVM Systems," *Proc. International Conference on Embedded Software* (***EMSOFT***), Pittsburgh, PA, USA, Oct. 2016.

[41] E. H.-M. Sha, Y. Liang, **W. Jiang**, X. Chen and Q. Zhuge, "Optimizing Data Placement of MapReduce on Ceph-Based Framework under Load-Balancing Constraint," *Proc. International Conference on Parallel and Distributed Systems* (***ICPADS***), Wuhan, China, Dec. 2016.

[42] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H.-M. Sha, "FoToNoC: A hierarchical management strategy based on folded lorus-like Network-on-Chip for dark silicon many-core systems," *Proc. 2016 21st Asia and South Pacific Design Automation Conference* (***ASP-DAC***), Macao, Jan. 2016. (**BEST PAPER NOMINATION**)

[43] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "Designing an Efficient Persistent In-Memory File System," *Proc. the 4th IEEE Non-Volatile Memory System and Applications Symposium* (***NVMSA***), Hongkong, Aug. 2015. (**BEST PAPER AWARD**)

Invited Talks

- Rice University (host: Prof. Yingyan Lin), Nov. 2020
- Workshop on Research Open Automatic Design for Neural Networks (ROAD4NN), July, 2020
- Workshop on Hardware and Algorithms for Learning On-a-chip (HALO), Nov. 2019
- Northeastern University (host: Prof. Yanzhi Wang), Oct. 2019
- Technical Webinar of NSF IUCRC for ASIC, Aug. 2019

Professional Services

Journal Reviewer

- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration (TVLSI)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
- IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)
- IEEE Embedded System Letter (ELS)
- IEEE Access
- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Journal on Emerging Technologies in Computing (JETC)
- Journal of Computer Science and Technology (JCST)
- Communications in Statistics - Simulation and Computation
- Microprocessors and Microsystems (MICPRO)

- SPRINGER Journal of Signal Processing Systems (JSPS)
- HINDAWI Complexity (Complexity)

Conference Technical Program Committee:

- Late Break Results in Design Automation Conference (DAC 2020)
- IEEE Computer Society Annual Symposium on VLSI (ISLVLSI 2020)
- ACM Great Lakes Symposium on VLSI (GLSVLSI 2020)
- Student Research Forum at Asia and South Pacific Design Automation Conference (ASP-DAC 2020)
- ACM/SIGAPP Symposium On Applied Computing (SAC 2020,2021)
- 33rd IEEE International System-on-Chip Conference (IEEE SOCC 2020)
- 40th IEEE Real-Time Systems Symposium (RTSS 2019, Artifact Evaluation Committee)

Conference Review

- Reviewer of 2019 MICCAI Workshop on Hardware Aware Learning for Medical Imaging and Computer Assisted Intervention
- Design Automation Conference 2018, 2019, Expert Reviewers (DAC)
- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems 2018, External Reviewer (CASES)

References on Request

- **Edwin H.-M. Sha, Ph.D. Advisor** (edwinsha@cs.ecnu.edu.cn), Distinguished Professor, East China Normal University, Shanghai, China.
  `Changjiang Scholar, National Thousand People Plan Specially-invited Expert`
  Website: https://faculty.ecnu.edu.cn/s/3741/t/37453/main.jspy
- **Jingtong Hu, Ph.D. Co-Advisor** (jthu@pitt.edu). Associate Professor, University of Pittsburgh, Pittsburgh, PA, USA.
  Website: http://pitt.edu/~jthu/
- **Yiyu Shi, Postdoc PI** (yshi4@nd.edu), Associate Professor, University of Notre Dame, Notre Dame, IN, USA
  `Site Director of NSF I/UCRC ASIC Center`
  Website: https://www3.nd.edu/~scl/index.html
- **Jinjun Xiong** (jinjun@us.ibm.com). Program Director, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA; Adjunct Research Professor, University of Illinois Urbana-Champaign, IL, USA
  `Program Director, Cognitive Computing Systems Research`
  Website: https://researcher.watson.ibm.com/view.php?person=us-jinjun
- **Nikil Dutt** (dutt@ics.uci.edu). Chancellor's Professor, University of California, Irvine, CA, USA.
  `IEEE Fellow and ACM Fellow`
  Website: https://www.ics.uci.edu/~dutt/
- **Xiaobao Sharon Hu** (shu@nd.edu). Professor, University of Notre Dame, Notre Dame, IN, USA.
  `IEEE Fellow and ACM Fellow`
  Website: https://www3.nd.edu/~shu/
- **Tei-wei Kuo** (teiwkuo@cityu.edu.hk), Professor, City University of Hong Kong, Kowloon, Hong Kong.
  `IEEE Fellow and ACM Fellow, Dean of College of Engineering`
  Website: http://www.cityu.edu.hk/stfprofile/teiwei.kuo.htm