Weiwen Jiang

Ph.D. Candidate
College of Computer Science
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Research Scholar
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Weiwen Jiang received the B.E. degree in the College of Computer Science from Nanjing Agriculture University, Jiangsu, China, in 2012. He is currently working towards the Ph.D. degree in the College of Computer Science from Chongqing University, Chongqing, China. Since September 31, 2017, he has been a research scholar in the Department of Electrical and Computer Engineering at the University of Pittsburgh, Pittsburgh, USA. The estimated date of graduation will be in **June 2019**.

He has published **more than 40** research articles in refereed international conferences and premier journals, including 10 IEEE Transactions papers. He was a reviewer of international conferences and journals, including DAC'18, CASES'18, IEEE Transactions on Computers (TC), IEEE Transactions on Emerging Topics in Computing (TETC), ACM Transactions on Design Automation of Electronic Systems (TODAES), etc. He received the **ICCD'17 Best Paper Award in EDA Track**, **NVMSA'15 Best Paper Award**, **ASP-DAC'16 Best Paper Nomination**, China National Scholarship for Ph.D., Scholarship from Microsoft Research and ACM Sigda to participate Student Research Competition at ICCAD'17, and Scholarship from ACM Sigda to participate PhD Forum at DAC'18.

He is good at cooperating. He was the main member in many research projects, including National High-tech R&D Program of China (863 Program), National Natural Science Foundation of China, and Huawei Aroma Lab's project. He was the mentor of 3 master students. One of them is now pursuing Ph.D. in University of Texas at Dallas (UTD), and two of them is now working for high-tech companies. Now, he is the mentor of 3 Ph.D. students in University of Pittsburgh and Chongqing University.

He is active in international academic activities. He attended **more than 10** international conferences, including *DAC'18* at San Francisco, U.S.; *GLSVLSI'18* at Chicago, U.S.; *IGSC'18* at Pittsburgh, U.S.; *ICACD'17* at Irvine, U.S.; *ICCD'17* at Boston, U.S.; *LCTES'17* at Barcelona, Spain; *RTCSA'17* at Hsinchu, Taiwan; *ESWEEK'16* at Pittsburgh, U.S.; *ICPADS'16* at Wuhan, China; *HPCC'15* at New York, U.S.; *ICA3PP'15* at Zhangjiajie, China; *RTCSA'14* at Chongqing, China.

Research Interests and Specialties

- **Neural Network:** especially for SW/HW co-design for FPGA-based NN accelerator **[1]**[18-19][44][45].
- **Non-Volatile Memories:** especially for the framework designs of file systems and databases **[2]**[13-17][25][28][31-33][37][39-42].
- **Systems-Level Optimizations:** especially for (1) optimizations of heterogeneous pipelined MPSoCs **[3]**[20-21][27][30]; (2) fundamental studies and optimizations of asynchronous embedded systems **[4]**[7][8][22-24][26]; (3) optimizations of NoC-based MPSoCs [9-12][29][35-36][38][44]; and (4) optimizations of distributed systems [5][6][34][43].

Education

University of Pittsburgh (Advisor: Dr. Jingtong Hu) 2017 – NOW. PITTSBURGH, U.S.

• **Research Scholar in Department of Electrical and Computer Engineering**. Focus on the design of heterogeneous computing platforms for neural networks.

Chongqing University (Advisor: Dr. Edwin Hsing-Mean Sha) 2014 – NOW. CHONGQING, CHINA

• **Ph.D Candidate in Computer Science**. Focus on the design of high-performance and low-cost heterogeneous systems. Specifically, I devise efficient optimal algorithms to explore the design space for assignment problems.

Chongqing University (Advisor: Dr. Edwin Hsing-Mean Sha) 2013 – 2014. CHONGQING, CHINA

• **Master degree in Computer Science**. Focus on the design of parallel architecture. Specifically, I study the fundamental properties of self-timed systems and pipelining systems.

Nanjing Agriculture University 2008 – 2012. JIANGSU, CHINA

• **Bachelor degree in Computer Science**. Major in Network Engineering.

Research Projects& Experience

National High-tech R&D Program of China (863 Program)/(No. 2013AA013202) 03/2013 – 01/2015

Main Member. Key Technologies of Unified Memory Systems in Non-Volatile Memory based Architectures

National High-tech R&D Program of China (863 Program)/(No. 2015AA015304) 01/2015 – 12/2017

Main Member. Key Technologies of Big Data Applications for New Memory Systems

National Natural Science Foundation of China/(No. 61472052) 01/2015 – 12/2018

Main Member. Key Technologies of System Optimization based on New Architectures of Non-Volatile Memories

Honors& Awards

Best Paper Award in ICCD 2017	11/2017. BOSTON
Scholarship to attend PhD Forum at DAC 2018	06/2018. SAN FRANCISCO
China National Scholarship (1% among all postgraduate students)	11/2017. CHINA
Scholarship to participate Student Research Competition at ICCAD 2017	11/2017. IRVINE
Best Student Paper Award in ESTC 2017	11/2017. CHINA
Chinese Government Scholarship (Chinese Scholarship Council)	05/2017. CHINA
Best Paper Award Nomination in ASP-DAC 2016	01/2016. MACAO
Best Paper Award in NVMSA 2015	08/2015. HONGKONG
Excellent Student Cadre in Nanjing Agriculture University	12/2011. CHINA
Merit Student in Nanjing Agriculture University	12/2009,12/2010. CHINA

Proposal Writing Experience

NSF CCF-SPX: Collaborative Research: Cross-Layer Exploration and Co-Optimization of Deep Neural Network Inference in Heterogeneous FPGA based Cloud (PI: Dr. Jingtong Hu and Dr. Yiyu Shi, Co-PI: Dr. Youtao Zhang) - *Revise and Resubmit* 12/2017

NSF CCF-SHF: Medium: Collaborative Research: Cross-Layer Exploration and Co-Optimization of Deep Neural Network Inference in Heterogeneous FPGA based Cloud (PI: Dr. Jingtong Hu and Dr. Yiyu Shi, Co-PI: Dr. Youtao Zhang) - *Under Review* 09/2018

NSFC: Optimizing Heterogeneous Pipelining Systems for Real-Time Applications (PI: Edwin Sha) - *Work in Progress* 10/2018

Refereed Publications

Three Representative Papers

[1] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "Heterogeneous FPGA-based Cost-Optimal Design for Timing-Constrained CNNs", *accepted by ESWEEK-CASES 2018@Torino* and *appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, 37(11): 2542-2554, 2018.

• **Most recent research: deploying CNNs onto multiple heterogeneous FPGAs.**

[2] E. H.-M. Sha, **W. Jiang**, H. Dong, Z. Ma, R. Zhang, X. Chen and Q. Zhuge, "Towards the Design of Efficient and Consistent Index Structure with Minimal Write Activities for Non-Volatile Memory", *in IEEE Transactions on Computers (**TC**)*, 67(3): 432-448, 2018.

• **OS-related research: designing the framework to support NVM-based database systems.**

[3] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, H. Dong and X. Chen, "On the Design of Minimal-Cost Pipeline Systems Satisfying Hard/Soft Real-Time Constraints," *accepted by IEEE International Conference on Computer Design (**ICCD 2017@Boston**)* (**BEST PAPER AWARD**) and *appear in IEEE Transactions on Emerging Topics in Computing (**TETC**)*, Jan. 2018.

• **Featured research: synthesizing systems considering the probabilistic execution time.**

Journal Paper

[4] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines", *in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, May. 2018.

• **Theoretical research: studying fundamental properties of asynchronous systems.**

[5] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Yang, L. Zhou and Q. Zhuge, "Optimal Functional-Unit Assignment for Heterogeneous Systems under Timing Constraint," *in IEEE Transactions on Parallel and Distributed Systems (**TPDS**)*, 28(9): 2567-2580, 2017.

[6] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and Lin Wu, "Efficient Assignment Algorithms to Minimize Operation Cost for Supply Chain Networks in Agile Manufacturing," *in Computers & Industrial Engineering*, 108: 225-239, 2017.

[7] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Wu and Q. Zhuge, "Synthesizing Distributed Pipelining Systems with Timing Constraints via Optimal Functional Unit Assignment and Communication Selection," *in Journal of Computational Science*, 26: 332-343, 2018.

[8] **W. Jiang**, Q. Zhuge, X. Chen, L. Yang, J. Yi and E. H.-M. Sha, "Properties of Self-Timed Ring Architectures for Deadlock-Free and Consistent Configuration Reaching Maximum Throughput," *in Journal of Signal Processing Systems*, 84(1): 123-137, 2016.

[9] W. Liu, L. Yang, **W. Jiang**, L. Feng, N. Guan, W. Zhang and N. Dutt, "Thermal-aware Task Mapping on Dynamically Reconfigurable Network-on-Chip based Multiprocessor System-on-Chip", *in IEEE Transactions on Computers (**TC**)*, 2018.

[10] L. Yang, W. Liu, **W. Jiang**, M. Li, P. Chen and E. H.-M. Sha, "FoToNoC: A Folded Torus-Like Network-on-Chip based Many-Core Systems-on-Chip in the Dark Silicon Era," *in IEEE Transactions on Parallel and Distributed Systems*, Dec. 2016. DOI:10.1109/TPDS.2016.2643669.

[11] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip-Based Multiprocessor System-on-Chip With Fine-Grain Communication Optimization" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 24(10): 3027-3040, Oct. 2016.

[12] L. Yang, W. Liu, **W. Jiang**, C. Chen, M. Li, P. Chen and E. H.-M. Sha, "Hardware-software collaboration for dark silicon heterogeneous many-core systems," *in Future Generation Computer systems*, 68: 234-247, 2017.

[13] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "A New Design of In-Memory File System Based on File Virtual Address Framework," *in IEEE Transactions on Computers*, 65(10):2959-2972, Oct. 2016.

[14] X. Chen, E. H.-M. Sha, **W. Jiang**, C. Yang, T. Wu and Q. Zhuge, "Refinery swap: An efficient swap mechanism for hybrid DRAM-NVM systems," *in Future Generation Computer systems*, 2017.

[15] X. Chen, E. H.-M. Sha, Q. Zhuge, **W. Jiang**, J. Chen and J. Xu A unified framework for designing high performance in-memory and hybrid memory file systems *Journal of Systems Architecture - Embedded Systems Design*, 68: 51-64, 2016.

[16] X. Chen, E. H.-M. Sha, Q. Zhuge, C. J. Xue, **W. Jiang** and Y. Wang, "Efficient data placement for improving data access performance on domain-wall memory" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 24(10): 3094-3104, 2016.

[17] P. Dai, Q. Zhuge, X. Chen, **W. Jiang** and E. H.-M. Sha, "Effective file data-block placement for different types of page cache on hybrid main memory architectures," *in Design Automation for Embedded Systems*, 17(3-4): 485-506, 2013.

Conference Paper

[18] **W. Jiang**, X. Zhang, E. H.-M. Sha, L. Yang, Q. Zhuge, Y. Shi and J. Hu, "Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search," *Proc. Design Automation Conference (**DAC 2019**)*, Las Vegas, NV, Jun. 2019.

[19] **W. Jiang**, X. Zhang, E. H.-M. Sha, Q. Zhuge, L. Yang, Y. Shi and J. Hu, "XFER: A Novel Design to Achieve Super-Linear Performance on Multiple FPGAs for Real-Time AI (Abstract Only)," *Proc. ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2019**)*, Seaside, California, Feb. 2019.

[20] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and X. Chen, "Optimal Functional-Unit Assignment and Buffer Placement for Probabilistic Pipelines," *Proc. International Conference on Hardware/Software Co-design and System Synthesis (**CODES+ISSS**)*, Pittsburgh, PA, USA, Oct. 2016.

[21] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, H. Dong and X. Chen, "Optimal Functional Unit Assignment and Voltage Selection for Pipelined MPSoC with Guaranteed Probability on Time Performance," *Proc. Languages, Compilers, and Tools for Embedded Systems (**LCTES**)*, Barcelona, Spain, Jun. 2017.

[22] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, L. Yang and X. Chen, "On the Design of High-Performance and Energy-Efficient Probabilistic Self-Timed Systems," *Proc. High Performance Computing and Communications (**HPCC**)*, NewYork, NY, USA, Aug. 2015.

[23] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "Prevent Deadlock and Remove Blocking for Self-Timed Systems," *Proc. International Conference on Algorithms and Architectures for Parallel Processing (**ICA3PP**)*, Zhangjiajie, China, Nov. 2015.

[24] **W. Jiang**, E. H.-M. Sha, X. Chen, Q. Zhuge and L. Wu, "Optimal Functional Assignment and Communication Selection under Timing Constraint for Self-Timed Pipelines," *Proc. IEEE International Conference on Embedded Software and Systems (**ICESS**)*, Chengdu, China, Aug. 2016.

[25] X. Chen, E. H.-M. Sha, Z. Sun, Q. Zhuge and **W. Jiang**, "The Design and Implementation of an Efficient Data Consistency Mechanism for In-Memory File Systems," *Proc. IEEE International Conference on Embedded Software and Systems (**ICESS**)*, Chengdu, China, Aug. 2016.

[26] **W. Jiang**, Q. Zhuge, J. Yi, L. Yang and E. H.-M. Sha, "On self-timed ring for consistent mapping and maximum throughput," *Proc. Embedded and Real-Time Computing Systems and Applications (**RTCSA**)*, Chongqing, China, Aug. 2014.

[27] E. H.-M. Sha, H. Dong, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "On the Design of Reliable Heterogeneous Systems via Checkpoint Placement and Core Assignment," *Proc. Great Lakes Symposium on VLSI (GLSVLSI)*, Chicago, IL, USA, May. 2018.

[28] X. Chen, E. H.-M. Sha, Y. Zeng, C. Yang, **W. Jiang** and Q. Zhuge, "Efficient wear leveling for inodes of file systems on persistent memories," *Proc. Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany, Mar. 2018.

[29] W. Liu, L. Yang, **W. Jiang** and N. Guan, "Work In Progress : Communication Optimization for Thermal Reliable Many-core Systems," *Proc. International Conference on Hardware/Software Co-design and System Synthesis (**CODES+ISSS**)*, Seoul, South Korea, Oct. 2017.

[30] H. Dong, E. H.-M. Sha, **W. Jiang**, X. Chen, R. Zhang and Q. Zhuge, "Towards the Design of Optimal Range Assignment for Elevator Groups under Fluctuant Traffic Loads," *Proc. Embedded and Real-Time Computing Systems and Applications (**RTCSA**)*, Hsinchu, Taiwan, Aug. 2017.

[31] X. Chen, E. H.-M. Sha, A. Abdulah, Q. Zhuge, L. Wu, C. Yang and **W. Jiang**, "The Design and Implementation of an Efficient User-space In-memory File System," *Proc. IEEE Non-Volatile Memory System and Applications Symposium (**NVMSA**)*, Hsinchu, Taiwan, Aug. 2017.

[32] X. Li, Q. Zhuge, **W. Jiang**, H. Dong, W. Lin, X. Chen and E. H.-M. Sha, "A Research of Reducing Write Activities in Multi-table Join for Non-Volatile Memories," *Proc. 15th CCF Annual Conference on Embedded Systems (ESTC)*, Shenyang, China, Nov. 2017.

[33] X. Chen, E. H.-M. Sha, **W. Jiang**, Q. Zhuge, J. Chen, J. Qin, Y. Zeng, "The Design of an Efficient Swap Mechanism for Hybrid DRAM-NVM Systems," *Proc. International Conference on Embedded Software (**EMSOFT**)*, Pittsburgh, PA, USA, Oct. 2016.

[34] E. H.-M. Sha, Y. Liang, **W. Jiang**, X. Chen and Q. Zhuge, "Optimizing Data Placement of MapReduce on Ceph-Based Framework under Load-Balancing Constraint," *Proc. International Conference on Parallel and Distributed Systems (**ICPADS**)*, Wuhan, China, Dec. 2016.

[35] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H.-M. Sha, "FoToNoC: A hierarchical management strategy based on folded lorus-like Network-on-Chip for dark silicon many-core systems," *Proc. 2016 21st Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, Macao, Jan. 2016. (**BEST PAPER NOMINATION**)

[36] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Wang, "Isolation of Physical and Logical Views of Dark-Silicon Many-Core Systems for Reliability and Performance Co-Optimization", *Embedded System Technology*, Springer Singapore, 2015.

[37] X. Chen, E. H.-M. Sha, Q. Zhuge, P. Dai and **W. Jiang**, "Optimizing data placement for reducing shift operations on domain wall memories," *Proc. Design Automation Conference (**DAC**)*, San Francisco, California, USA, Jun. 2015.

[38] L. Yang, W. Liu, **W. Jiang**, W. Zhang, M. Li, J. Yi, D. Liu and E. H.-M. Sha, "Traffic-Aware Application Mapping for Network-on-Chip Based Multiprocessor System-on-Chip," *Proc. High Performance Computing and Communications (**HPCC**)*, NewYork, NY, USA, Aug. 2015.

[39] E. H.-M. Sha, Y. Jia, X. Chen, Q. Zhuge, **W. Jiang** and J. Qin "The Design and Implementation of an Efficient User-space In-memory File System," *Proc. the 5th IEEE Non-Volatile Memory System and Applications Symposium (**NVMSA**)*, Daegu, Korea, Aug. 2016.

[40] Z. Liu, E. H.-M. Sha, X. Chen, **W. Jiang**, and Q. Zhuge "Performance Optimization for In-Memory File Systems on NUMA Machines," *Proc. International Conference on Parallel and Distributed Computing, Applications and Technologies (PDCAT)*, Guangzhou, China, Dec. 2016.

[41] E. H.-M. Sha, J. Chen, X. Chen, **W. Jiang**, and Q. Zhuge "The Design and Implementation of a High-Performance Hybrid Memory File System," *Proc. International Conference on Advanced Cloud and Big Data (CDB)*, Chengdu, China, Dec. 2016.

[42] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "Designing an Efficient Persistent In-Memory File System," *Proc. the 4th IEEE Non-Volatile Memory System and Applications Symposium (**NVMSA**)*, Hongkong, Aug. 2015. (**BEST PAPER AWARD**)

[43] J. Yi, W. Liu, **W. Jiang**, M. Qin, L. Yang, D. Liu, C. Xiao, L. Du and E. H.-M. Sha, "An Improved Thermal Model for Static Optimization of Application Mapping and Scheduling in Multiprocessor System-on-Chip," *Proc. IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**)*, Tampa, Florida, USA, Jul. 2014.

[44] L. Yang, W. Liu, **W. Jiang**, J. Yi, D. Liu and Q. Zhuge, "Contention-aware task and communication co-scheduling for network-on-chip based Multiprocessor System-on-Chip," *Proc. Embedded and Real-Time Computing Systems and Applications (**RTCSA**)*, Chongqing, China, Aug. 2014.

Working-in-Progress

[44] **W. Jiang**, about designing multi-FPGA clusters for DNNs with real-time requirements, *for ISCA 2019*.

[45] **W. Jiang**, about hardware/software co-exploration of neural architecture search, *for ICML 2019*.

Mentor of Students

- Hailiang Dong (Master) [25,28], First Employer: University of Texas at Dallas (UTD) for Ph.D.
- Xinchi Li (Master) [30], First Employer: Tencent in Chengdu
- Yutong Liang (Master) [32], First Employer: PingCAP Inc. in Beijing
- Zhulin Ma (Ph.D Candidate): One paper is prepared for FGCS
- Runyu Zhang (Ph.D Candidate): One paper is prepared for DAC'19

Professional Services

Journal Reviewer

- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Embedded Systems Letters (ESL)
- Journal of Signal Processing Systems
- Hindawi Complexity

Conference Reviewer

- Intl. Conference on Compilers, Architecture, and Synthesis for Embedded Systems 2018 (CASES)
- Design Automation Conference 2018, 2019 (DAC)

Additional Skills

- Operating Systems: Windows and Linux (familiar with the memory and process parts in kernel)
- Algorithms: Integer Linear Programming, Dynamic Programming, Pareto Analysis, Proof of NP-hard
- Hardware Related Tools/Languages: Vivado, Vivado HLS, SystemC
- Programming Languages: C/C++, Python, Matlab
- Deep Learning Tool: Caffe, Tensorflow, Keras

References on Request

- **Edwin H.-M. Sha** (edwinsha@cs.ecnu.edu.cn), Tenured Distinguished Professor, East China Normal University, Shanghai, China.
  `Changjiang Scholar, National Thousand People Plan Specially-invited Expert`
- **Nikil Dutt** (dutt@ics.uci.edu). Chancellor's Professor, University of California, Irvine, CA, USA.
  `IEEE Fellow and ACM Fellow`
- **Jingtong Hu** (jthu@pitt.edu). Assistant Professor, University of Pittsburgh, PA, USA.