Weiwen Jiang June 27, 1990

College of Computer Science • Chongqing University
No.174 Shazheng Street, Shapingba District, Chongqing, China (400044)
Department of Electrical and Computer Engineering • University of Pittsburgh
4420 Bayard St, Bayard Street, Pittsburgh, PA, U.S. (15261)
Email: jiang.wwen@pitt.edu
Tel: +1 (412)427-0695
Home Page: http://pitt.edu/~wej23/

RESEARCH INTERESTS

Embedded Systems, Heterogeneous Architectures, FPGAs, Neural Networks, Optimization Algorithm Design, Non-Volatile Memories, Databases

EDUCATION

University of Pittsburgh (Advisor: Dr. Jingtong Hu) 2017 – now. Pittsburgh, U.S.
• **Visiting Scholar in Department of Electrical and Computer Engineering**. Focus on the design of heterogeneous computing platforms for neural networks.

Chongqing University (Advisor: Dr. Edwin Hsing-Mean Sha) 2014 – now. Chongqing, China
• **Ph.D Candidate in Computer Science**. Focus on the design of high-performance and low-cost heterogeneous systems. Specifically, I devise efficient optimal algorithms to explore the design space for assignment problems.

Chongqing University (Advisor: Dr. Edwin Hsing-Mean Sha) 2013 – 2014. Chongqing, China
• **Master Candidate in Computer Science**. Focus on the design of parallel architecture. Specifically, I study the fundamental properties of self-timed systems and pipelining systems.

Nanjing Agriculture University 2008 – 2012. Jiangsu, China
• **Bachelor degree in Computer Science**. Major in Network Engineering.

RESEARCH PROJECTS & EXPERIENCE

National High-tech R&D Program of China (863 Program)/(No. 2013AA013202) 03/2013 – 01/2015
Main Member. Key Technologies of Unified Memory Systems in Non-Volatile Memory based Architectures

National High-tech R&D Program of China (863 Program)/(No. 2015AA015304) 01/2015 – 12/2017
Main Member. Key Technologies of Big Data Applications for New Memory Systems

National Natural Science Foundation of China/(No. 61472052) 01/2015 – 12/2018
Main Member. Key Technologies of System Optimization based on New Architectures of Non-Volatile Memories

HONORS & AWARDS

Best Paper Award in ICCD 2017 11/2017. Boston
Scholarship to attend PhD Forum at DAC 2018 06/2018. San Francisco
China National Scholarship (1% among all postgraduate students) 11/2017. China
Scholarship to participate Student Research Competition at ICCAD 2017 11/2017. Irvine
Best Student Paper Award in ESTC 2017 11/2017. China
Chinese Government Scholarship (Chinese Scholarship Council) 05/2017. China
Best Paper Award Nomination in ASP-DAC 2016 01/2016. Macao
Best Paper Award in NVMSA 2015 08/2015. Hongkong

PROPOSAL WRITING EXPERIENCE

NSF CCF-SPX: Collaborative Research: Cross-Layer Exploration and Co-Optimization of Deep Neural Network Inference in Heterogeneous FPGA based Cloud (PI: Dr. Jingtong Hu and Dr. Yiyu Shi, Co-PI: Dr. Youtao Zhang) - *Revise and Resubmit* 12/2017

NSF CCF-SHF: Medium: Collaborative Research: Cross-Layer Exploration and Co-Optimization of Deep Neural Network Inference in Heterogeneous FPGA based Cloud (PI: Dr. Jingtong Hu and Dr. Yiyu Shi, Co-PI: Dr. Youtao Zhang) - *Under Review* 09/2018

NSFC (Chinese): Optimizing Heterogeneous Pipelining Systems for Real-Time Applications (PI: Edwin H.-M. Sha) - *Work in Progress* 10/2018

SELECTED PUBLICATIONS

I have published more than 40 refereed papers, including 4 first-authored IEEE Trans papers, and 1 second-authored (advisor is the first author) IEEE Trans paper. Full list can be found at http://pitt.edu/~wej23/categories/paper.

Journal Paper

1. **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "Heterogeneous FPGA-based Cost-Optimal Design for Timing-Constrained CNNs", *accepted by ESWEEK-CASES 2018@Torino* and *appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, 37(11): 2542-2554, 2018.
2. **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines", *accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, May. 2018.
3. **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, H. Dong and X. Chen, "On the Design of Minimal-Cost Pipeline Systems Satisfying Hard/Soft Real-Time Constraints," *IEEE International Conference on Computer Design (**ICCD 2017@Boston**)* (**BEST PAPER AWARD**) and *appear in IEEE Transactions on Emerging Topics in Computing (**TETC**)*, Jan. 2018.
4. **W. Jiang**, E. H.-M. Sha, X. Chen, L. Yang, L. Zhou and Q. Zhuge, "Optimal Functional-Unit Assignment for Heterogeneous Systems under Timing Constraint," *in IEEE Transactions on Parallel and Distributed Systems (**TPDS**)*, 28(9): 2567-2580, 2017.
5. E. H.-M. Sha, **W. Jiang**, H. Dong, Z. Ma, R. Zhang, X. Chen and Q. Zhuge, "Towards the Design of Efficient and Consistent Index Structure with Minimal Write Activities for Non-Volatile Memory", *in IEEE Transactions on Computers (**TC**)*, 67(3): 432-448, 2018.
6. **W. Jiang**, E. H.-M. Sha, Q. Zhuge and Lin Wu, "Efficient Assignment Algorithms to Minimize Operation Cost for Supply Chain Networks in Agile Manufacturing," *in Computers & Industrial Engineering (**CAIE**)*, 108: 225-239, 2017. (*JCR Ranking: Q1*)

Conference Paper

1. **W. Jiang**, X. Zhang, E. H.-M. Sha, L. Yang, Q. Zhuge, Y. Shi and J. Hu, "Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search," *Proc. Design Automation Conference (**DAC 2019**)*, Las Vegas, NV, Jun. 2019.
2. **W. Jiang**, X. Zhang, E. H.-M. Sha, Q. Zhuge, L. Yang, Y. Shi and J. Hu, "XFER: A Novel Design to Achieve Super-Linear Performance on Multiple FPGAs for Real-Time AI (Abstract Only)," *Proc. ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2019**)*, Seaside, California, Feb. 2019.
3. **W. Jiang**, E. H.-M. Sha, Q. Zhuge and X. Chen, "Optimal Functional-Unit Assignment and Buffer Placement for Probabilistic Pipelines," *Proc. International Conference on Hardware/Software Co-design and System Synthesis (**CODES+ISSS**)*, Pittsburgh, PA, USA, Oct. 2016.
4. **W. Jiang**, E. H.-M. Sha, Q. Zhuge, H. Dong and X. Chen, "Optimal Functional Unit Assignment and Voltage Selection for Pipelined MPSoC with Guaranteed Probability on Time Performance," *Proc. Languages, Compilers, and Tools for Embedded Systems (**LCTES**)*, Barcelona, Spain, Jun. 2017.
5. E. H.-M. Sha, **W. Jiang**, Q. Zhuge, L. Yang and X. Chen, "On the Design of High-Performance and Energy-Efficient Probabilistic Self-Timed Systems," *Proc. High Performance Computing and Communications (**HPCC**)*, NewYork, NY, USA, Aug. 2015.
6. E. H.-M. Sha, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "Prevent Deadlock and Remove Blocking for Self-Timed Systems," *Proc. International Conference on Algorithms and Architectures for Parallel Processing (**ICA3PP**)*, Zhangjiajie, China, Nov. 2015.
7. **W. Jiang**, Q. Zhuge, J. Yi, L. Yang and E. H.-M. Sha, "On self-timed ring for consistent mapping and maximum throughput," *Proc. Embedded and Real-Time Computing Systems and Applications (**RTCSA**)*, Chongqing, China, Aug. 2014.

Working-in-Progress

1. **W. Jiang**, about designing multi-FPGA clusters for DNNs with real-time requirements, *for ISCA 2019*.
2. **W. Jiang**, about hardware/software co-exploration of neural architecture search, *for ICML 2019*.

PROFESSIONAL ACTIVITIES

Journal IEEE TC, IEEE TCAD, IEEE TETC, ACM TODAES, IEEE ELS, JSPS, Complexity
Conference Secondary Reviewer of CASES 2018, Expert Reviewers of DAC 2018, 2019