CS3120

Introduction of Integrated Circuit Design

Introduction to Virtuoso

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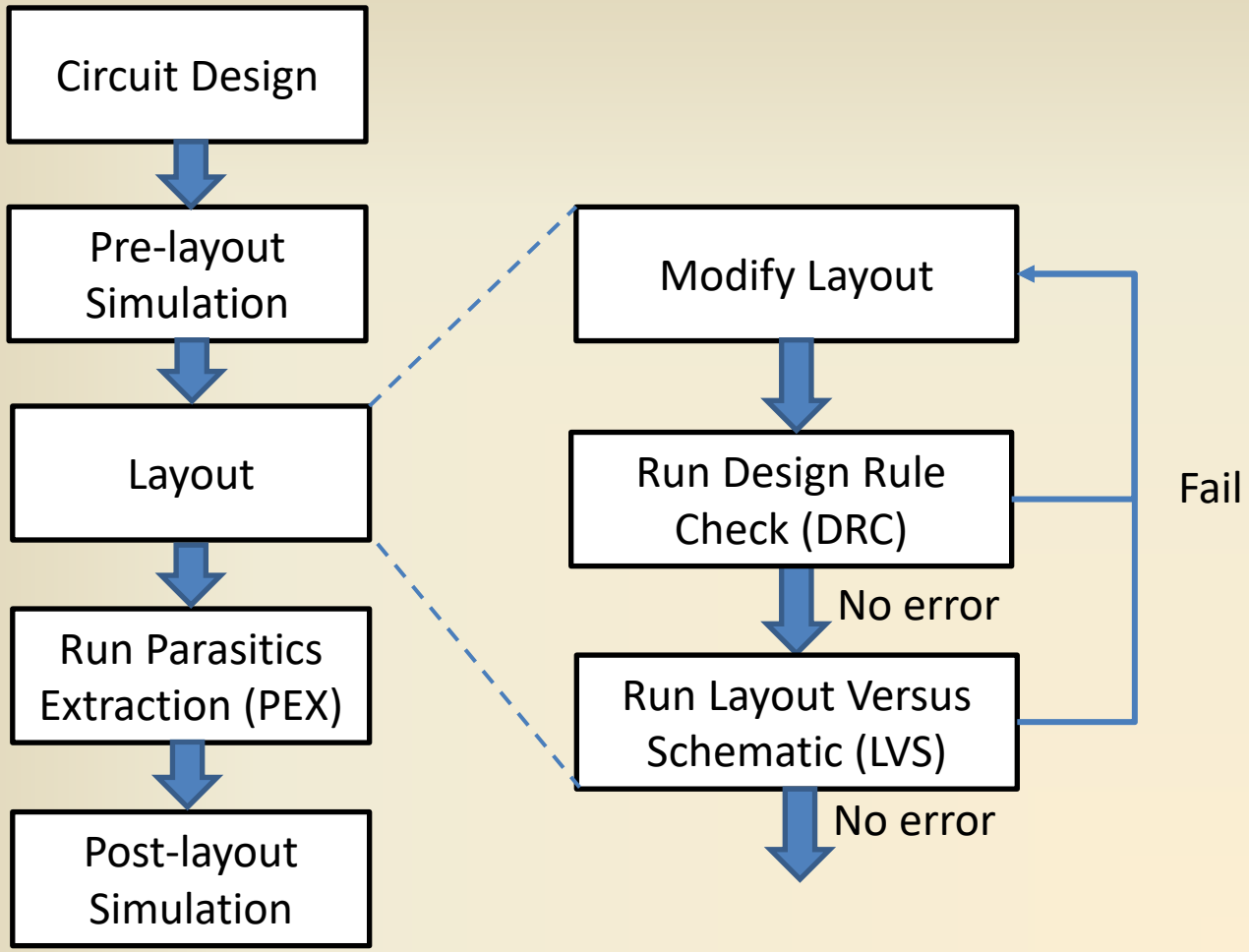
Introduction



Outline

- Step 1 Download Files
- Step 2 Files Setting

} Just do it once

- Step 3 Source
- Step 4 Complete Pre-layout Simulation
- Step 5 Construct New Library in Virtuoso
- Step 6 Construct New Cell View
- Step 7 Run DRC
- Step 8 Run LVS
- Step 9 Run PEX
- Step 10 Run Post-layout Simulation

Step 1 Download Files

1. Download spice_layout.tar from eecalss
2. Upload to your home directory
3. Unzip the file: **tar xvf spice_layout.tar**

```
spice/
spice/pre_sim/
spice/pre_sim/cic018.l
spice/pre_sim/hw3/
spice/pre_sim/hw2/
spice/pre_sim/final_project/
spice/post_sim/
spice/post_sim/cic018.l
spice/post_sim/hw3/
spice/post_sim/hw2/
spice/post_sim/final_project/
layout/
layout/calibre/
layout/calibre/Rule.lvs
layout/calibre/Rule_08KA.rc
layout/calibre/Rule_20KA.rc
layout/calibre/Rule.rce
layout/calibre/rule.drc
layout/.cdsinit
layout/display.drf
layout/cic18.tf
```

Directory and files

```
spice/
spice/pre_sim/
spice/pre_sim/cic018.l
spice/pre_sim/hw3/
spice/pre_sim/hw2/
spice/pre_sim/final_project/
spice/post_sim/
spice/post_sim/cic018.l
spice/post_sim/hw3/
spice/post_sim/hw2/
spice/post_sim/final_project/
layout/
layout/calibre/
layout/calibre/Rule.lvs
layout/calibre/Rule_08KA.rc
layout/calibre/Rule_20KA.rc
layout/calibre/Rule.rce
layout/calibre/rule.drc
layout/.cdsinit
layout/display.drf
layout/cic18.tf
```

- cic018.l: spice simulation process file
- ./cdsinit: virtuoso initialize file
- display.trf: layout display reference file
- cic18.tf: layout used process file
- rule.drc: DRC rule file
- Rule.lvs: LVS rule file
- Rule.rce: PEX rule file
- Rule_08KA.rc and Rule_20KA.rc: RC information for different metal thickness condition

Step2 Files Setting

1. Open /layout/calibre/Rule.rce
2. Copy the file path of Rule_20KA.rc and Rule_08KA.rc
3. Find Rule_20KA.rc and Rule_08KA.rc in Rule.rce, and change it to the copied file path

Step2 Files Setting

MobaTextEditor

File Edit Search View Format Encc

Rule.rce

```
304
305 SEPGND:1 = SIZE SEPGND BY 0.01
306 SEPGND:2 = SEPGND:1 NOT SEPGND
307 PSUB_ALL = (BULK   NOT NWEL) NOT TWE
308 PSUB     = PSUB_ALL NOT SEPGND:2
309
310 BPDIFF = DIFF   AND PPLUS
311 BNDIFF = DIFF   AND NPLUS
312 PGATE  = BPDIFF AND PO1
313 NGATE  = BNDIFF AND PO1
314 BPGATE = size (size (PGATE  NOT PSYM
315 BNGATE = size (size (NGATE  NOT PSYM
316 NWELL  = NWEL   NOT TWEL
317
318 PTAP   = PSUB  AND  PSD
319 NTAP   = WEL   AND  NSD
320 TNTAP  = PSD   AND  (NWEL AND TWEL)
321
322
323
324 ////////////////////////
325 // Setup Defaults for PEX
326 ////////////////////////
327 #IFDEF PEXRUN
328 #IFDEF TOP_METAL_THICKNESS_20K
329  INCLUDE "Rule_20KA.rc"
330 #ELSE
331   INCLUDE "Rule_08KA.rc"
332 #ENDIF
```

MobaTextEditor

File Edit Search View Format Encoding Syntax Special Tools

* Rule.rce

```
304
305 SEPGND:1 = SIZE SEPGND BY 0.01
306 SEPGND:2 = SEPGND:1 NOT SEPGND
307 PSUB_ALL = (BULK   NOT NWEL) NOT TWEL
308 PSUB     = PSUB_ALL NOT SEPGND:2
309
310 BPDIFF = DIFF   AND PPLUS
311 BNDIFF = DIFF   AND NPLUS
312 PGATE  = BPDIFF AND PO1
313 NGATE  = BNDIFF AND PO1
314 BPGATE = size (size (PGATE  NOT PSYMBOL) by -0.05) by 0.05
315 BNGATE = size (size (NGATE  NOT PSYMBOL) by -0.05) by 0.05
316 NWELL  = NWEL   NOT TWEL
317
318 PTAP   = PSUB  AND  PSD
319 NTAP   = WEL   AND  NSD
320 TNTAP  = PSD   AND  (NWEL AND TWEL)
321
322
323
324 ////////////////////////
325 // Setup Defaults for PEX
326 ////////////////////////
327 #IFDEF PEXRUN
328 #IFDEF TOP_METAL_THICKNESS_20K
329  INCLUDE "/users/course/2023F/cs312000110001/yyhuang/layout/calibre/Rule_20KA.rc"
330 #ELSE
331   INCLUDE "/users/course/2023F/cs312000110001/yyhuang/layout/calibre/Rule_08KA.rc"
332 #ENDIF
333 PEX FDB allnets GLOBAL 5000  EXCLUDE SOURCE VCC GND
```

Step2 back up

- **tar cvf spice_layout_backup.tar spice layout**

```
[ta112521030@linuxcad30 ~/HW2]$ tar cvf spice_layout_backup.tar spice layout
```

Step 3 Source

- HSPICE
  - source /usr/cad/synopsys/CIC/hspice.cshrc
- Waveview
  - source /usr/cad/synopsys/CIC/customexplorer.cshrc
- Virtuoso
  - source /usr/cad/cadence/CIC/ic.cshrc
  - source /usr/cad/mentor/CIC/calibre.cshrc

Step 4 Complete Pre-layout Simulation

1. Put your pre-sim files (inv.sp/hw2.sp/tb.sp…)in /spice/pre_sim/hw2
2. Run pre-sim to check the correctness of your circuit

Step 5 Open Virtuoso

1. **cd layout**
2. **icfb &**

```
[ta112521030@linuxcad30 ~/HW2]$ cd layout
[ta112521030@linuxcad30 layout]$ icfb &
[1] 19494
```

```
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         © 1992-2009  UNIX SYSTEMS Laboratories INC.,
                        Reproduced with permission.
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proprietary/confidential information and may be disclosed/used only
as authorized in a license agreement controlling such use and disclosure.
         RESTRICTED RIGHTS NOTICE (SHORT FORM)
Use/reproduction/disclosure is subject to restriction
set forth at FAR 1252.227-19 or its equivalent.
Program:                @(#)$CDS: icfb.exe version 5.1.0 11/22/2011 01:38 (cicln04) $
Sub version:            sub-version 5.10.41.500.6.151 (32-bit addresses)
Loading PRshare.cxt
Loading LVS.cxt
Loading layerProc.cxt
Loading ams.cxt
Loading acv.cxt
Loading auCore.cxt
Loading schView.cxt
Loading selectSv.cxt
Loading seismic.cxt
END OF SITE CUSTOMIZATION
Loading ./.cdsinit init file from the site init file.
//
//  Calibre Skill Interface * (v2020.2_14.12) *
//
//                Copyright Mentor Graphics Corporation 2005
//                            All Rights Reserved.
//        THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//           WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//             OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//
```
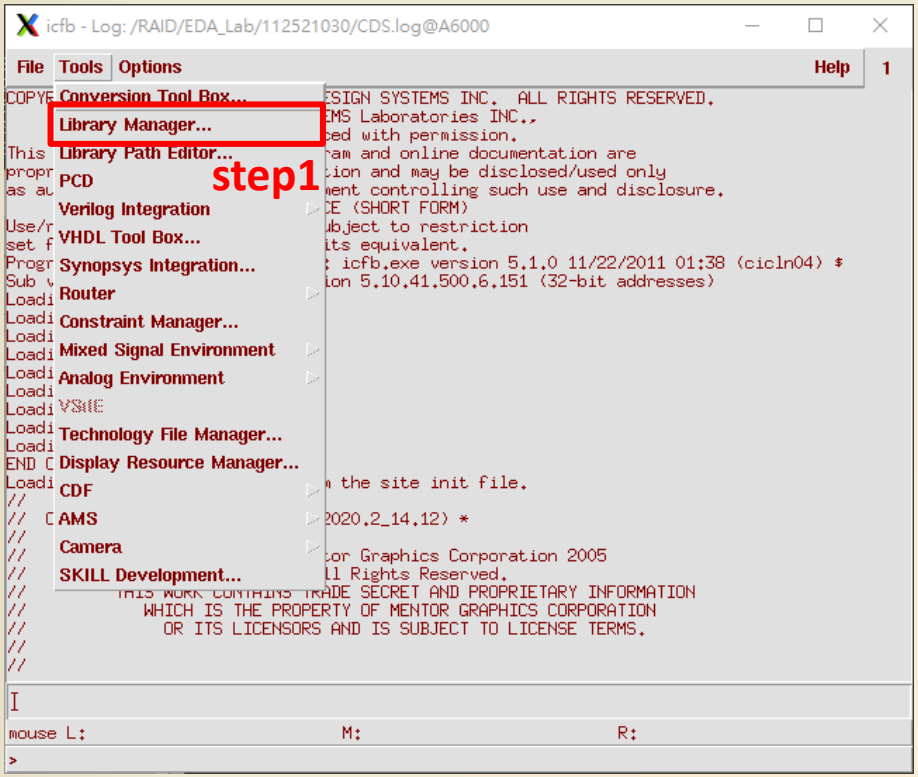
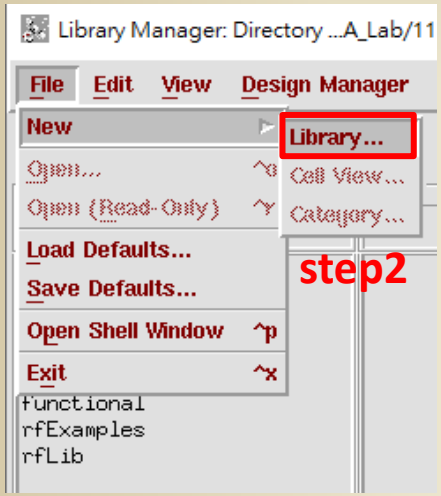

Calibre opened successfully

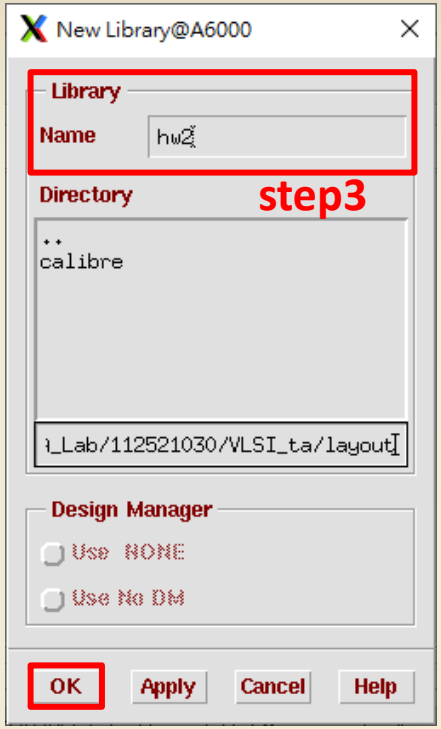
Step 5-1 Construct New Library

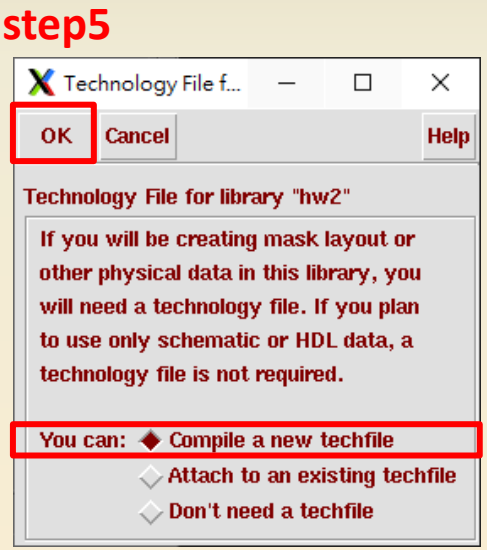
- Construct one library for each homework or project (ex: hw2, hw3, final_project)



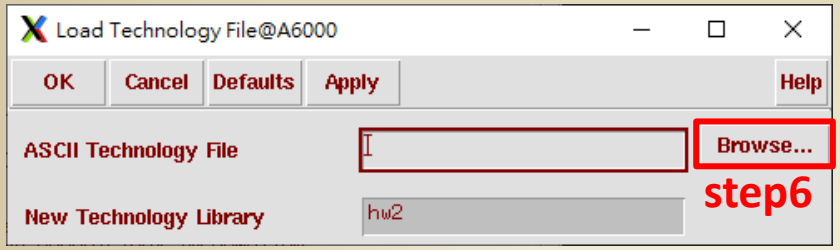
Step 5-2


Library Manager: Directory ...A_Lab/11
File Edit View Design Manager
New
Open...
Open (Read-Only)
Load Defaults...
Save Defaults...
Open Shell Window ^p
Exit ^x
Library...
Cell View...
Category...
step2
functional
rfExamples
rfLib

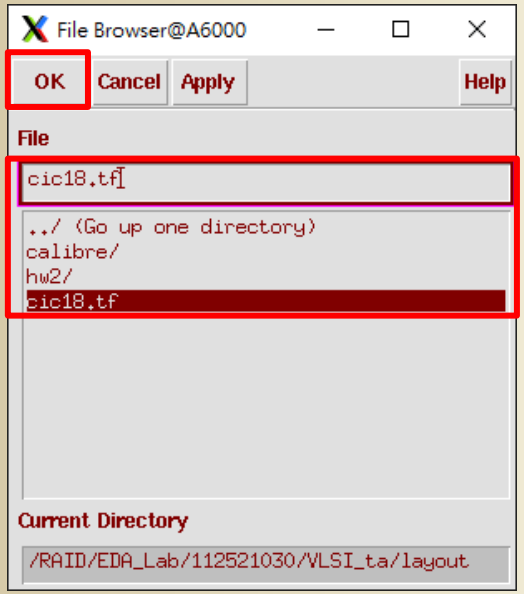

New Library@A6000
Library
Name
hw2
Directory
step3
..
calibre
_Lab/112521030/VLSI_ta/layout
Design Manager
Use NONE
Use No DM
OK
Apply
Cancel
Help
step4


step5
Technology File f...
OK
Cancel
Help
Technology File for library "hw2"
If you will be creating mask layout or other physical data in this library, you will need a technology file. If you plan to use only schematic or HDL data, a technology file is not required.
You can:
Compile a new techfile
Attach to an existing techfile
Don't need a techfile

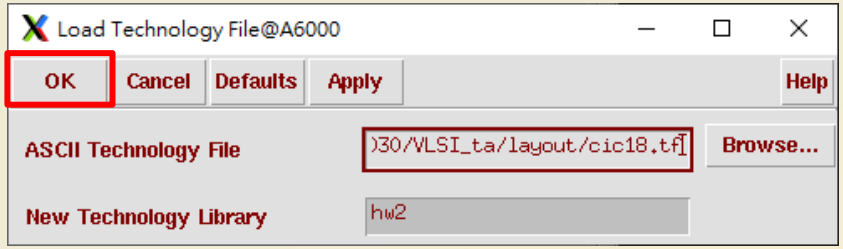
Step 5-3



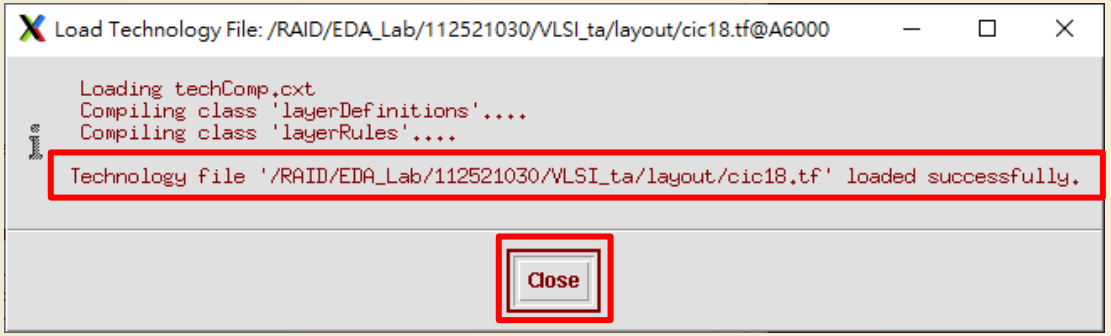
step7



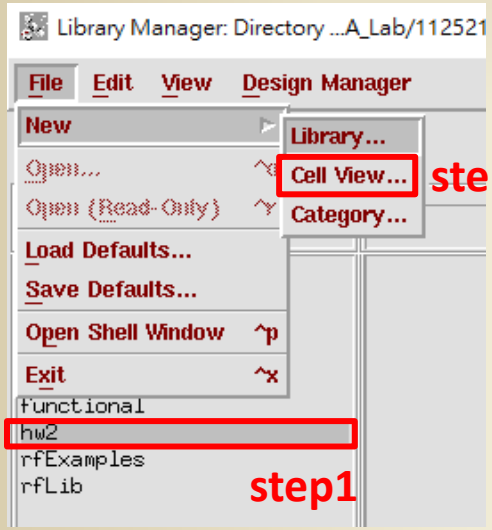
step8



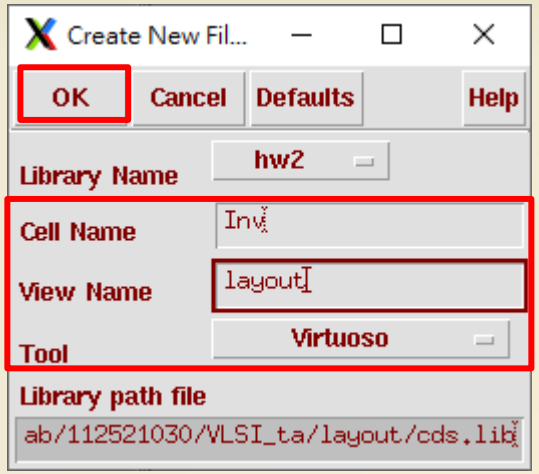
step9



Step 6-1 Construct New Cell View

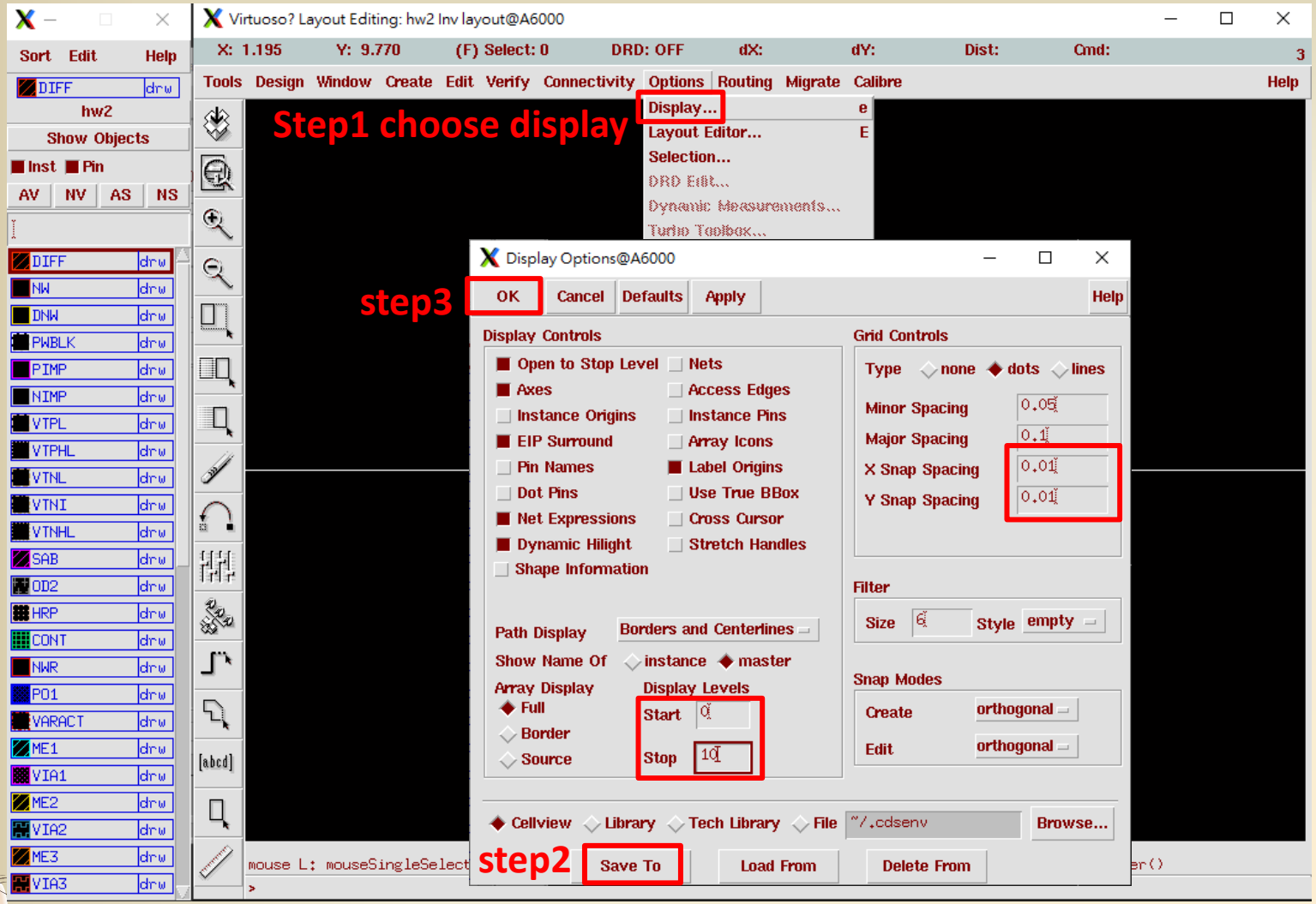


step3



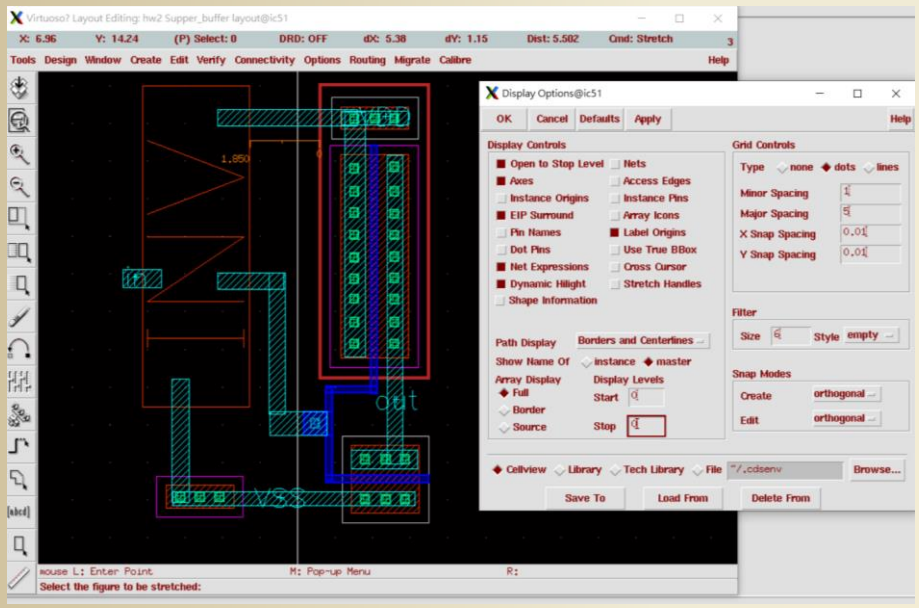
Cell name: enter cell name, ex: INV, NAND, buffer
View name: layout
Tool: Virtuoso

Step 6-2

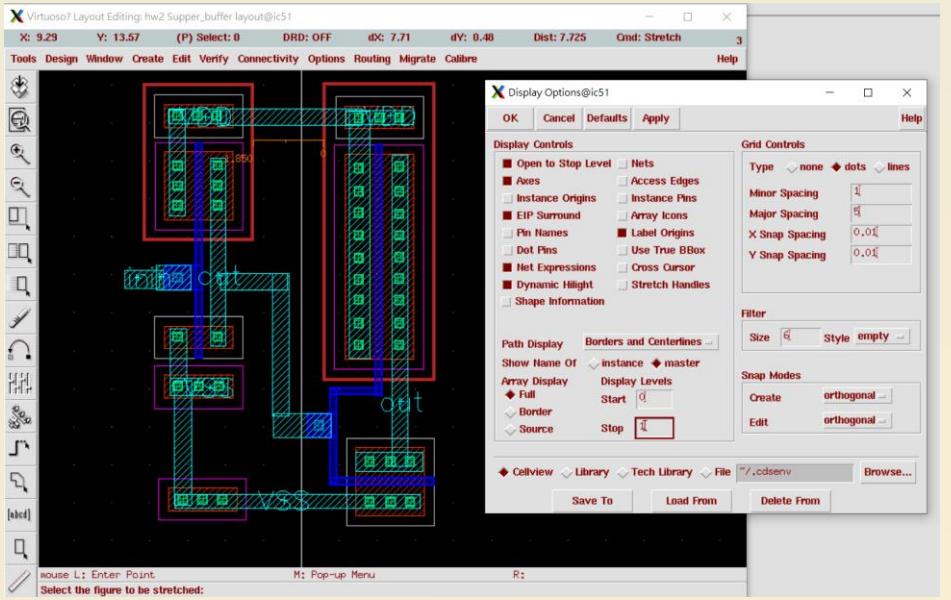

Virtuoso? Layout Editing: hw2 Inv layout@A6000
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre Help
Display...
Layout Editor...
Selection...
Step1 choose display
step3
Display Options@A6000
OK Cancel Defaults Apply Help
Display Controls
Grid Controls
Filter
Snap Modes
Path Display
Show Name Of
Array Display
Display Levels
Start
Stop
step2
Save To
Load From
Delete From

Different in Display Level

- When using instances

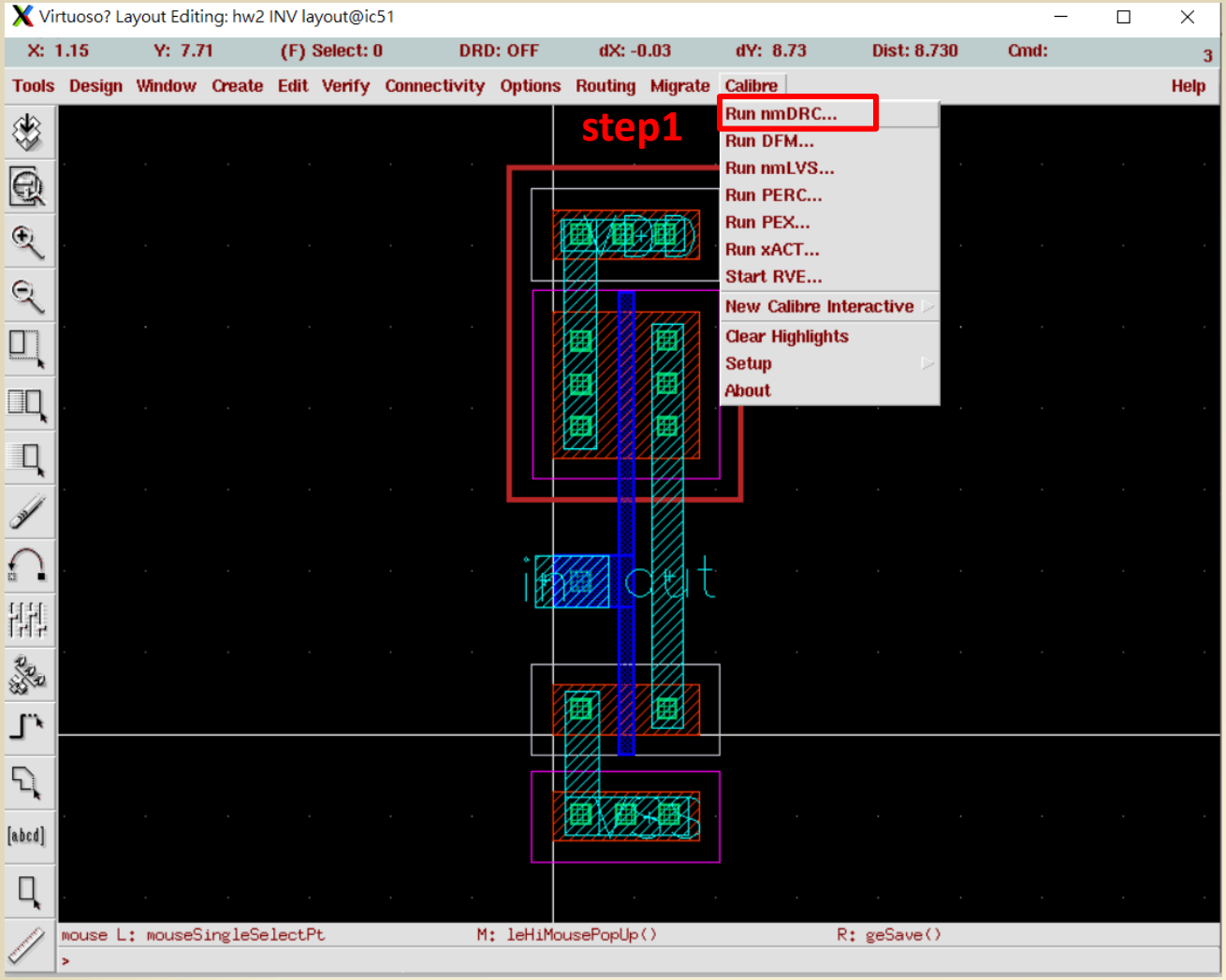


Stop: 0

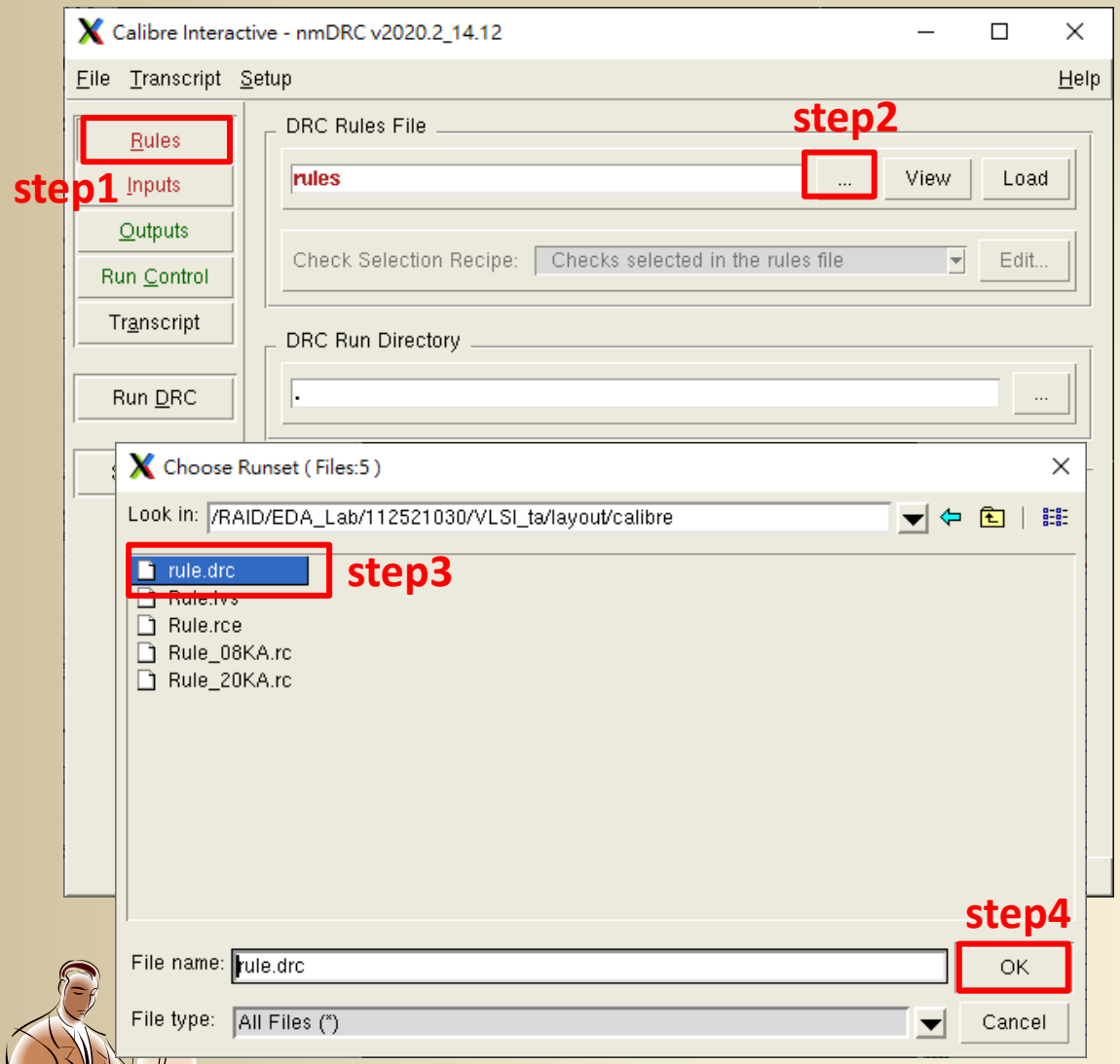


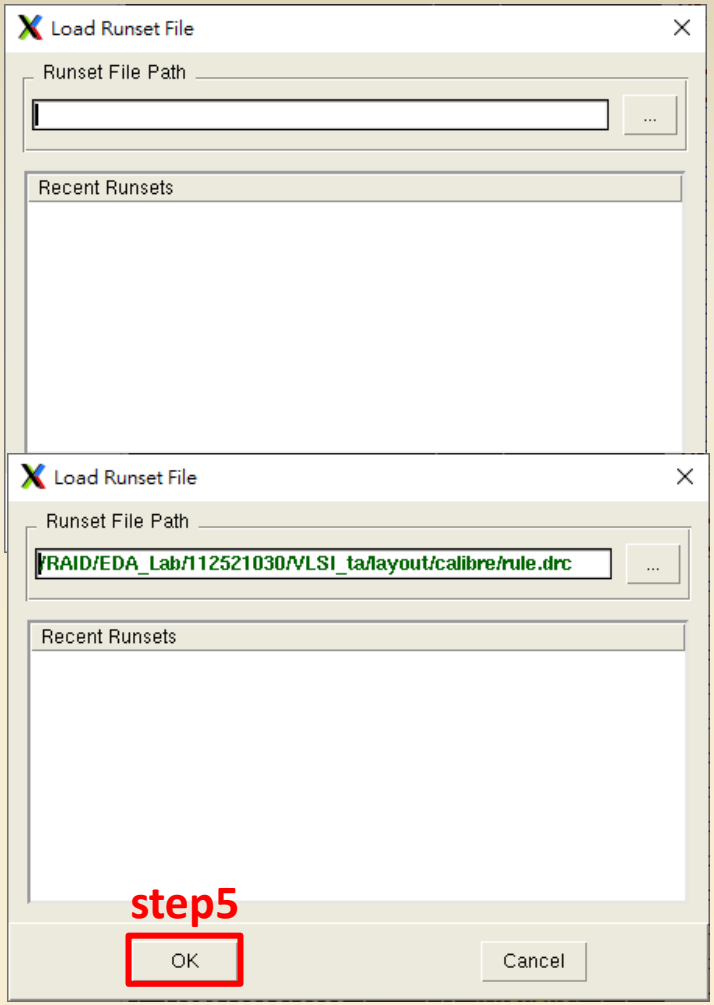
Stop: 1

Step 7 Run DRC



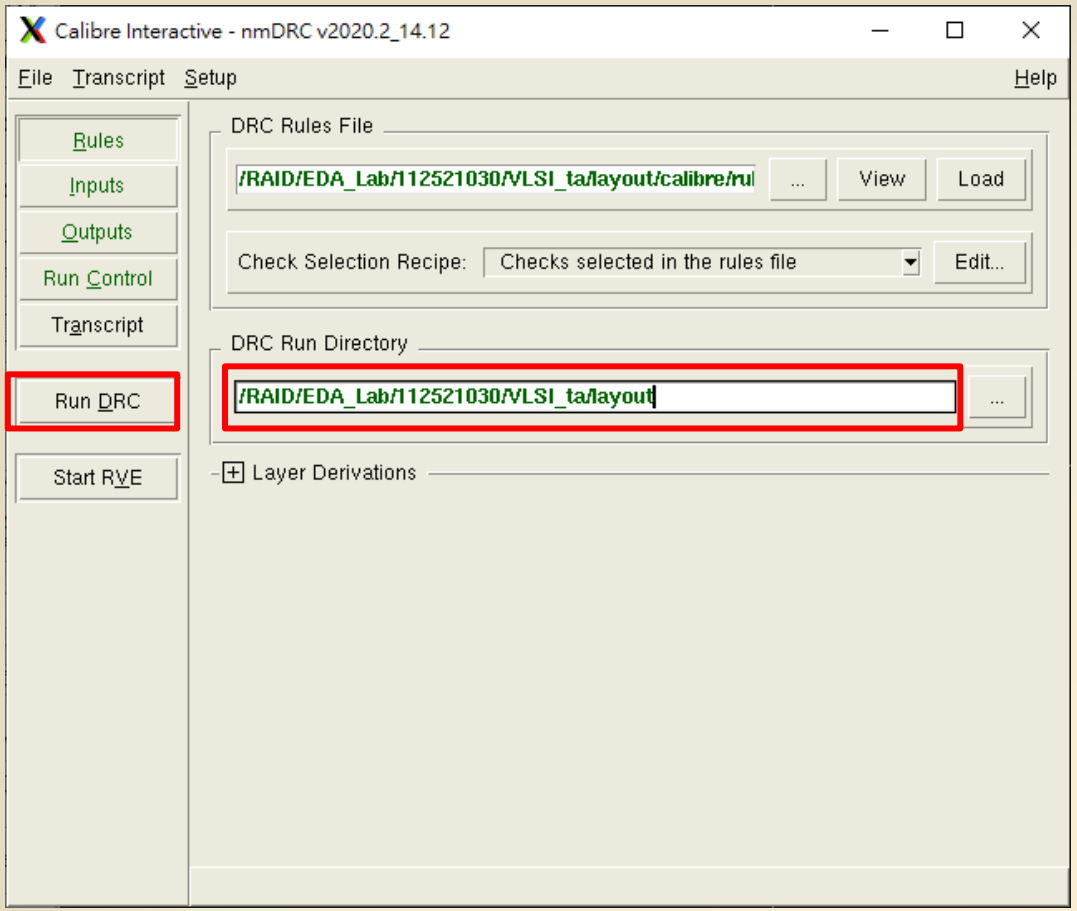
Step 7-1


Calibre Interactive - nmDRC v2020.2_14.12
File Transcript Setup Help
Rules
Inputs
Outputs
Run Control
Transcript
Run DRC
step1
DRC Rules File
rules
...
View
Load
step2
Check Selection Recipe:
Checks selected in the rules file
Edit...
DRC Run Directory
.
...
Choose Runset (Files:5)
Look in: /RAID/EDA_Lab/112521030/VLSI_ta/layout/calibre
rule.drc
Rule.rce
Rule_08KA.rc
Rule_20KA.rc
step3
File name: rule.drc
File type: All Files (*)
OK
Cancel
step4


Load Runset File
Runset File Path
...
Recent Runsets
Load Runset File
Runset File Path
/RAID/EDA_Lab/112521030/VLSI_ta/layout/calibre/rule.drc
...
Recent Runsets
step5
OK
Cancel

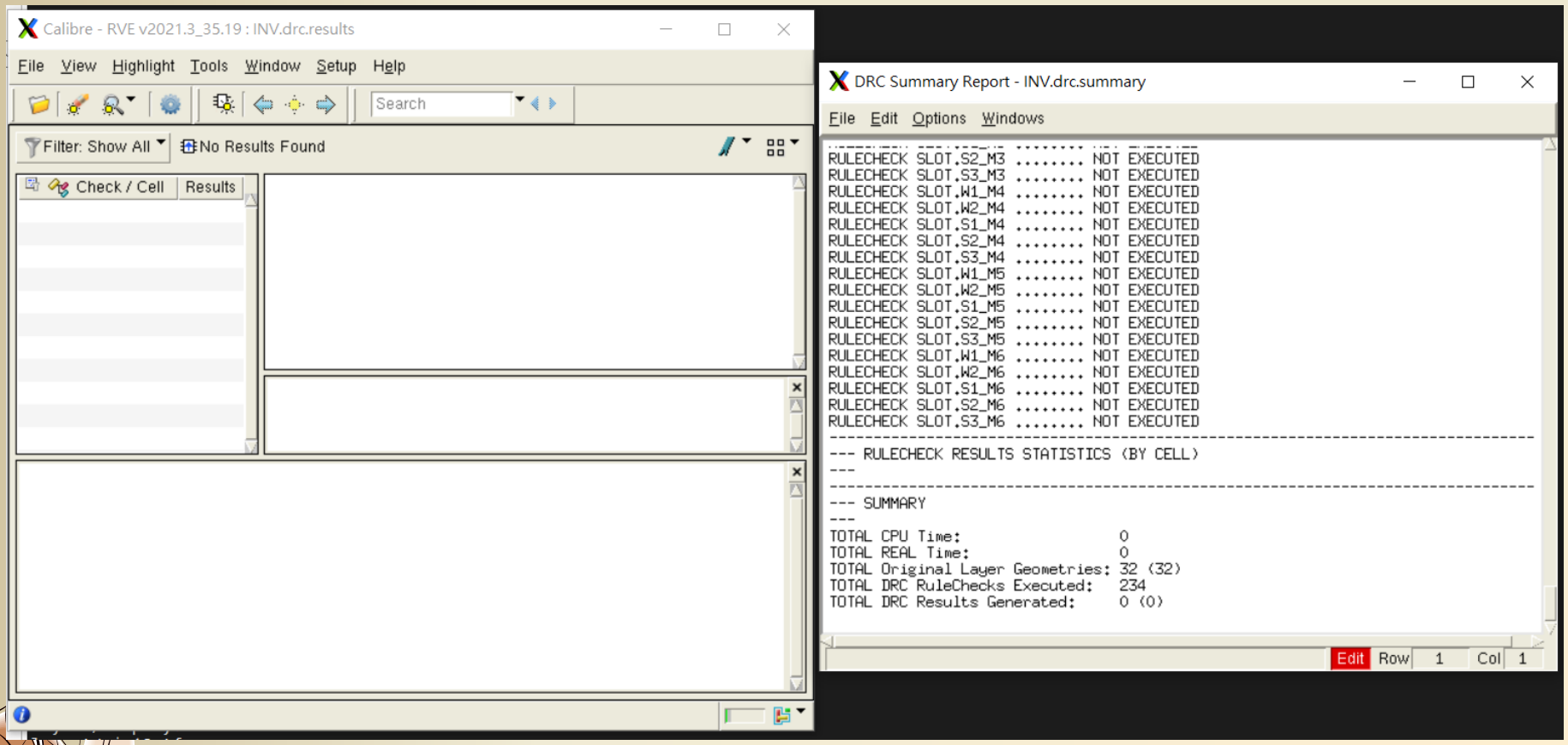
Step 7-2

step6

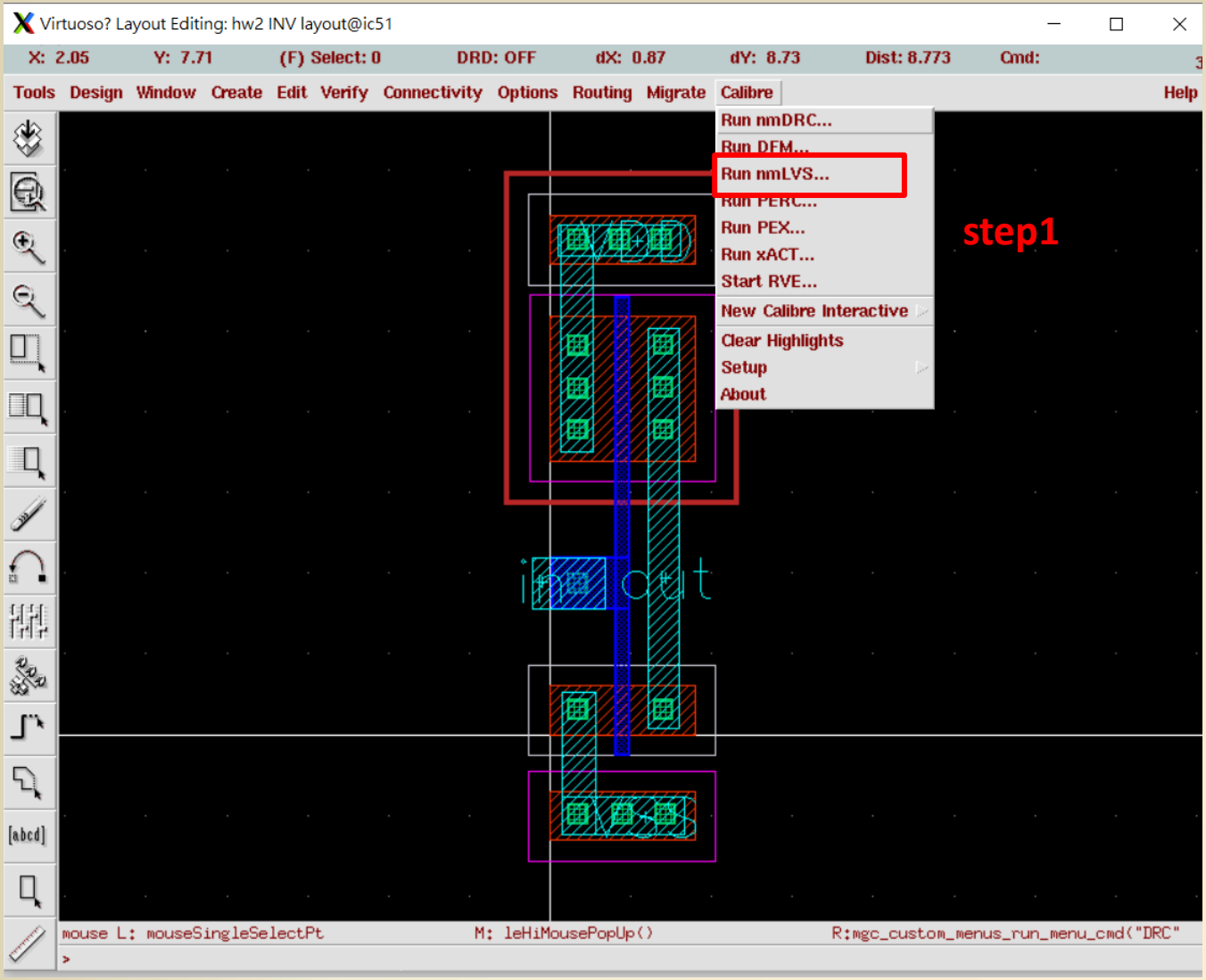


Step 7-3

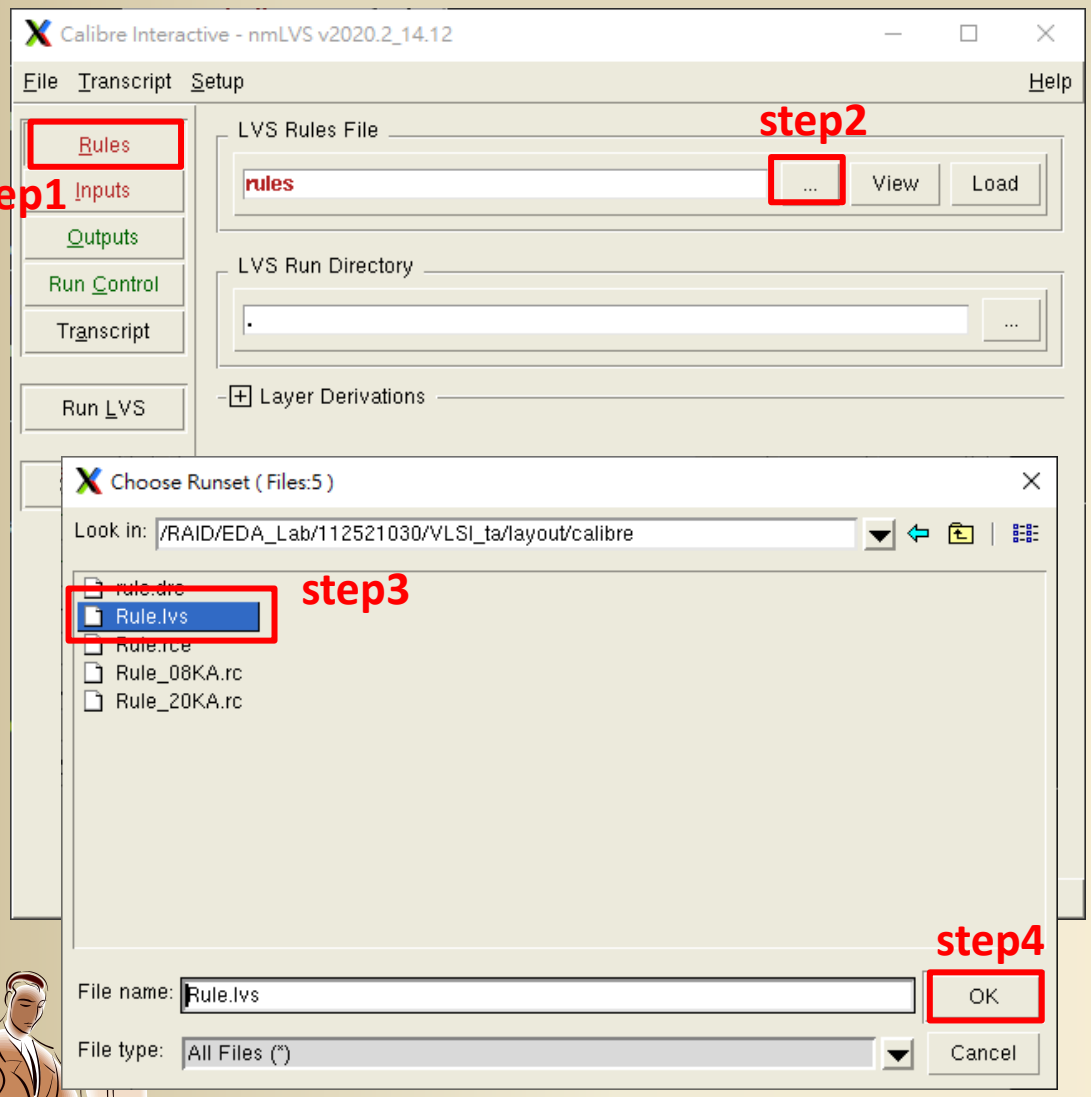
- No DRC results generated → DRC done

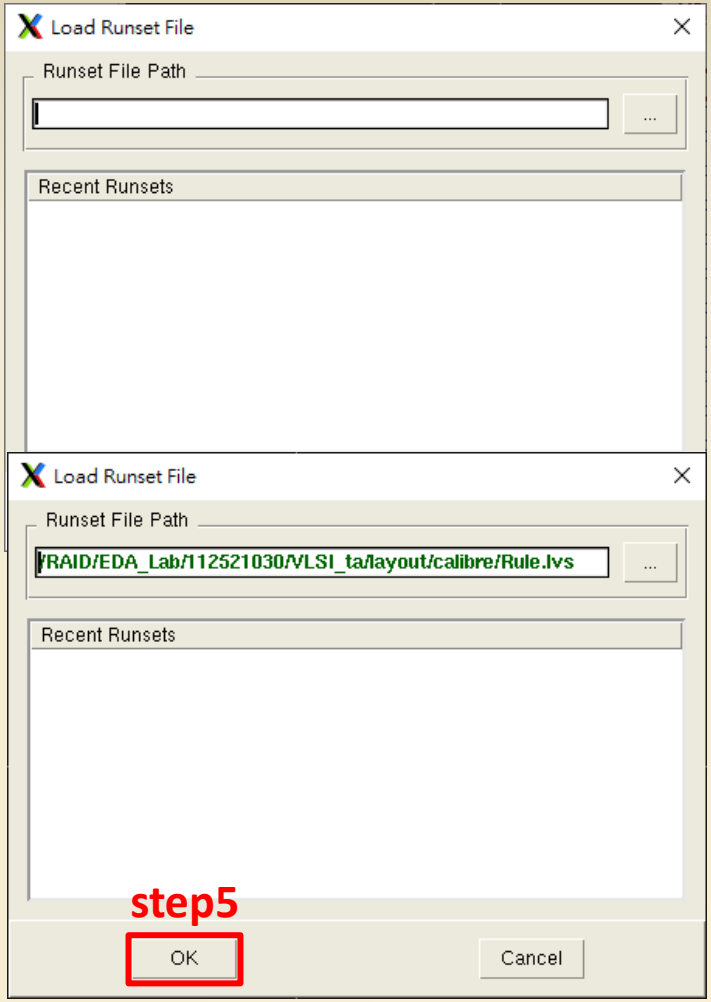


Step 8 Run LVS

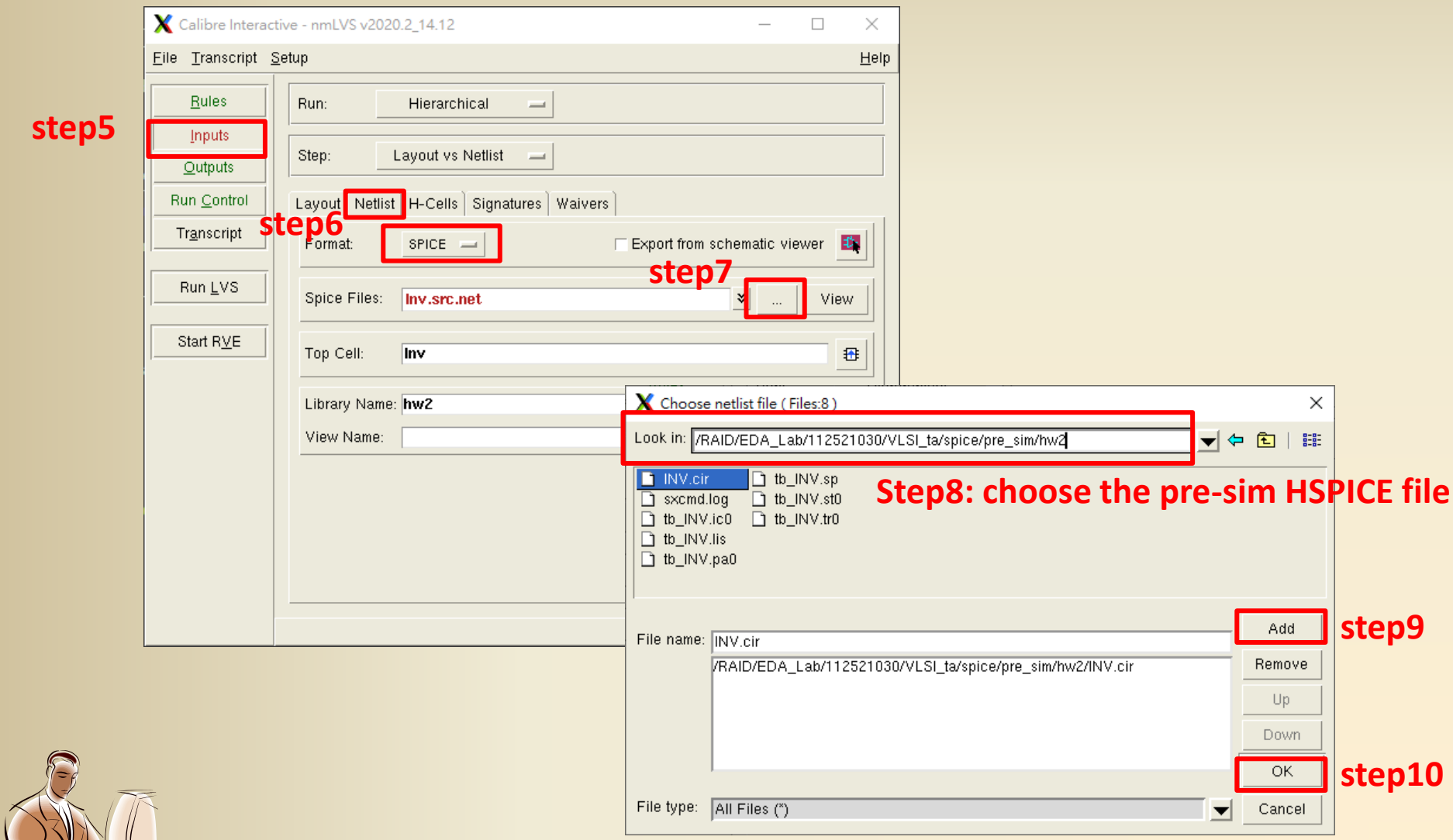


Step 8-1


Calibre Interactive - nmLVS v2020.2_14.12
File Transcript Setup Help
Rules
Inputs
Outputs
Run Control
Transcript
Run LVS
step1
LVS Rules File
rules
...
View
Load
step2
LVS Run Directory
.
...
Layer Derivations
Choose Runset (Files:5)
Look in: /RAID/EDA_Lab/112521030/VLSI_ta/layout/calibre
Rule.lvs
Rule_08KA.rc
Rule_20KA.rc
step3
File name: Rule.lvs
File type: All Files (*)
OK
Cancel
step4


Load Runset File
Runset File Path
Recent Runsets
Load Runset File
Runset File Path
/RAID/EDA_Lab/112521030/VLSI_ta/layout/calibre/Rule.lvs
Recent Runsets
step5
OK
Cancel

Step 8-2

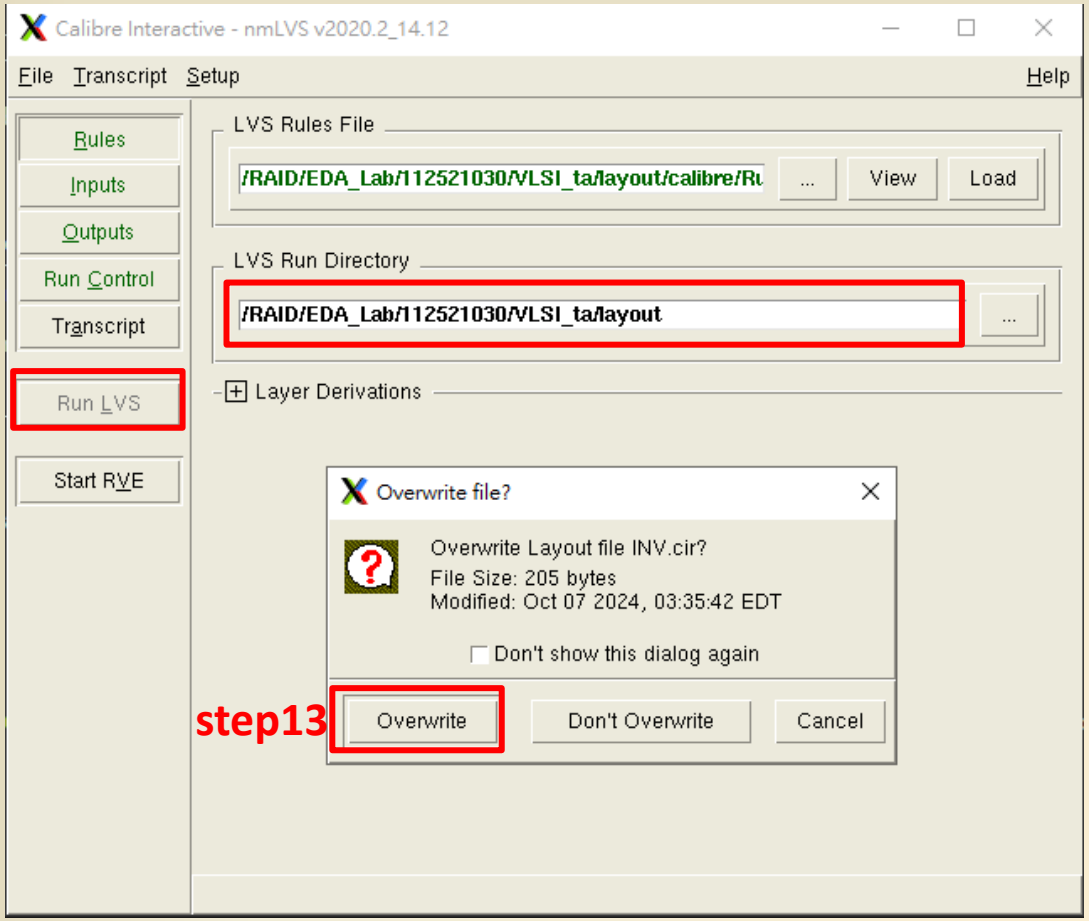

Calibre Interactive - nmLVS v2020.2_14.12
File Transcript Setup Help
Rules
Inputs
Outputs
Run Control
Transcript
Run LVS
Start RVE
Run: Hierarchical
Step: Layout vs Netlist
Layout Netlist H-Cells Signatures Waivers
Format: SPICE
Export from schematic viewer
Spice Files: lnv.src.net
...
View
Top Cell: lnv
Library Name: hw2
View Name:
step5
step6
step7
Choose netlist file (Files:8)
Look in: /RAID/EDA_Lab/112521030/VLSI_ta/spice/pre_sim/hw2
INV.cir
sxcmd.log
tb_INV.ic0
tb_INV.lis
tb_INV.pa0
tb_INV.sp
tb_INV.st0
tb_INV.tr0
Step8: choose the pre-sim HSPICE file
File name: INV.cir
/RAID/EDA_Lab/112521030/VLSI_ta/spice/pre_sim/hw2/INV.cir
Add
Remove
Up
Down
OK
Cancel
File type: All Files (*)
step9
step10

Step 8-2 Pre-sim HSPICE File

No other instances in circuit EX: inv.sp	Add other instances in circuit EX: Supper_buffer.sp
.subckt INV out in # NMOS PMOS description .ends INV	.subckt Supper_buffer out in **XINV out1 in INV** # NMOS PMOS description .ends Supper_buffer .subckt INV out in # NMOS PMOS description .ends INV

Step 8-3

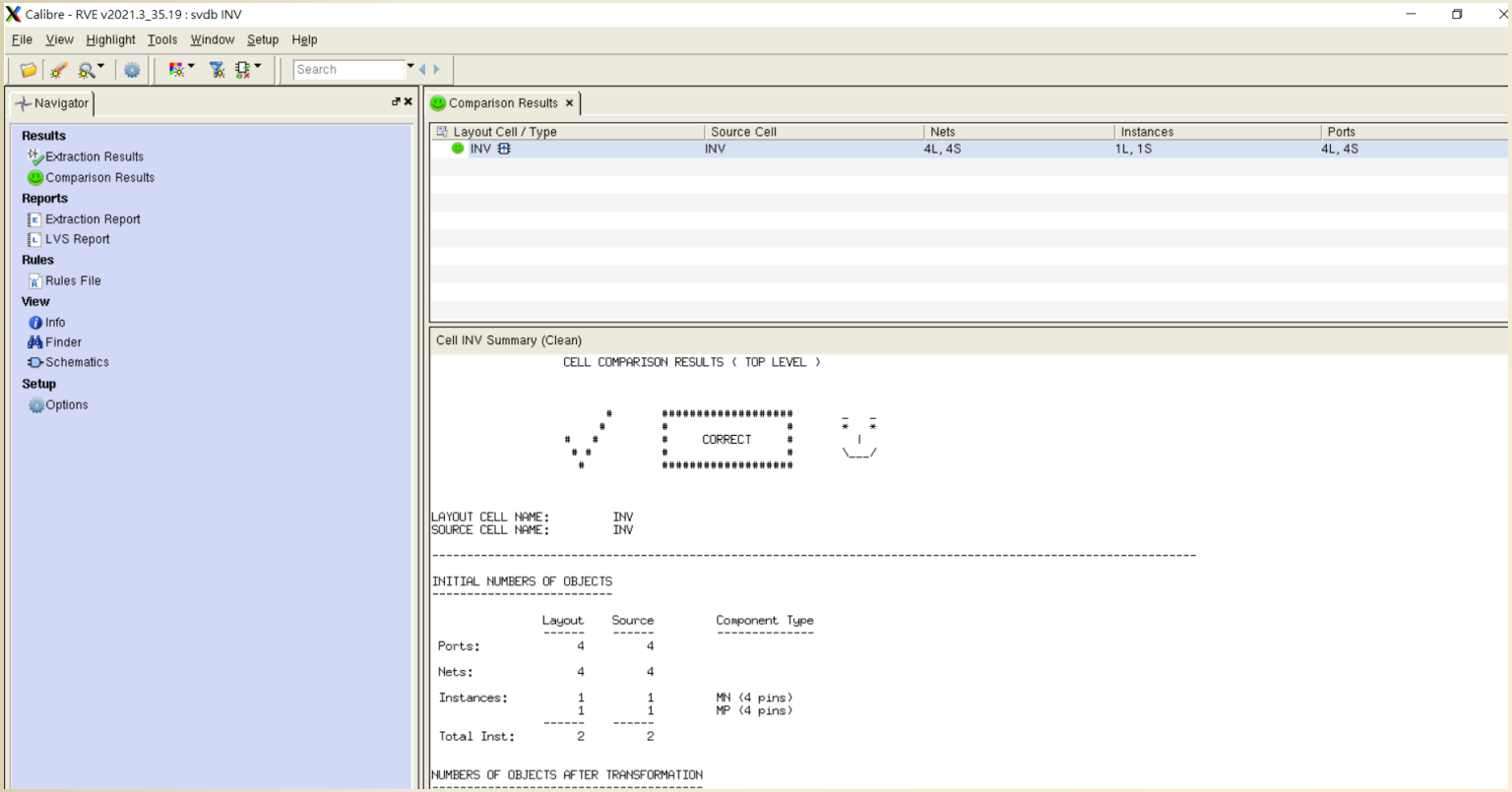
step12



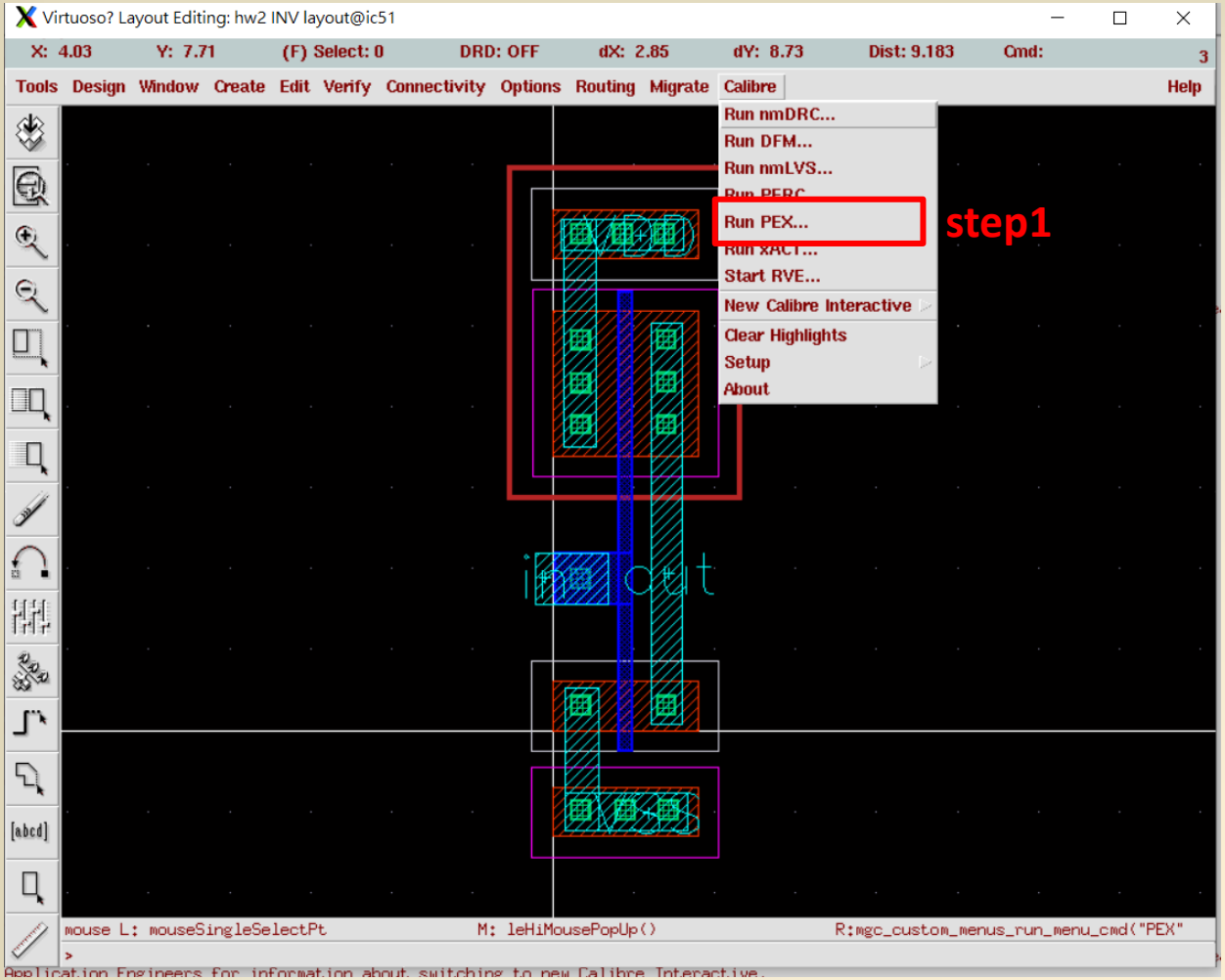
step13

Step 8-4

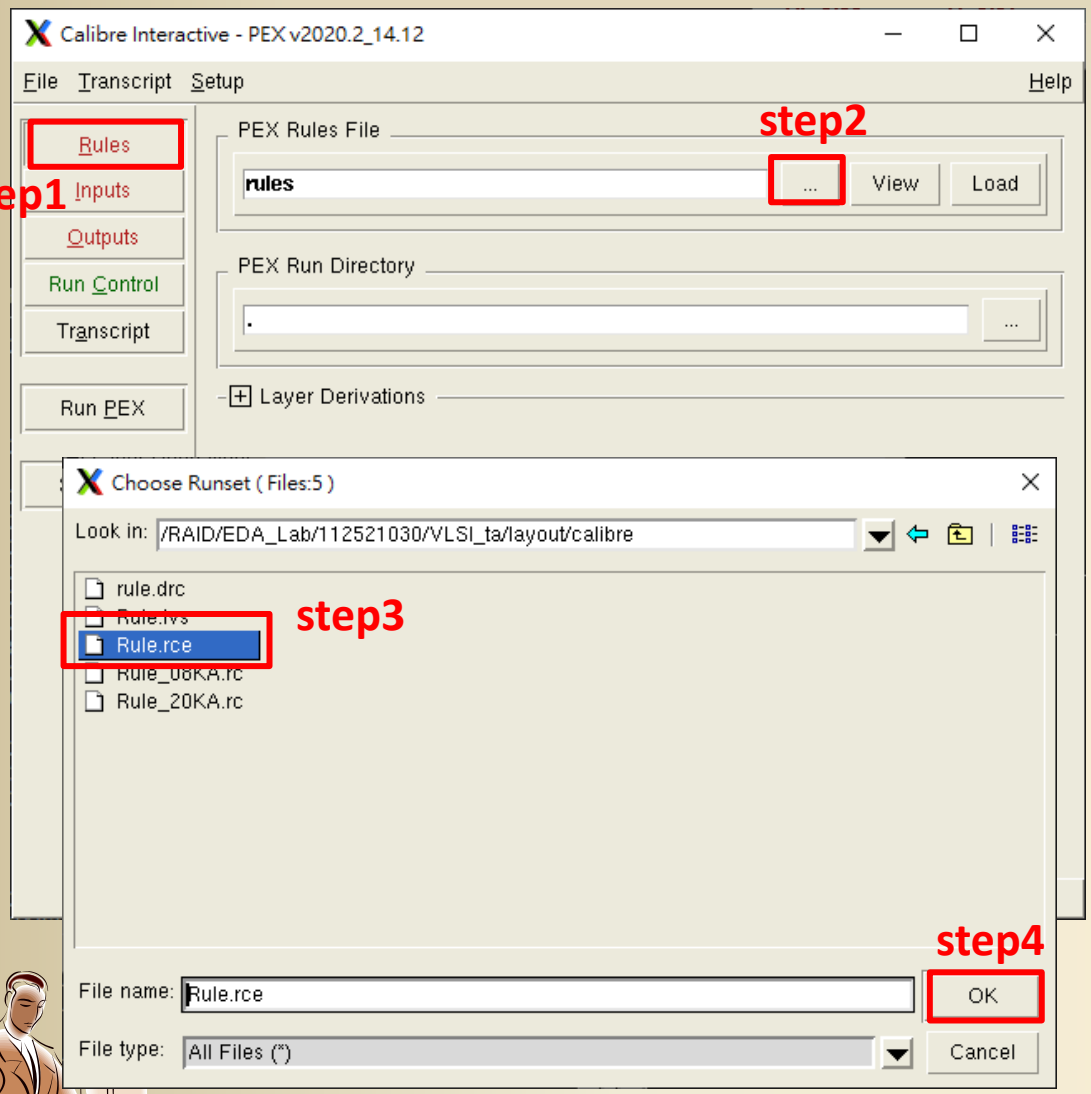
- LVS correct → LVS done

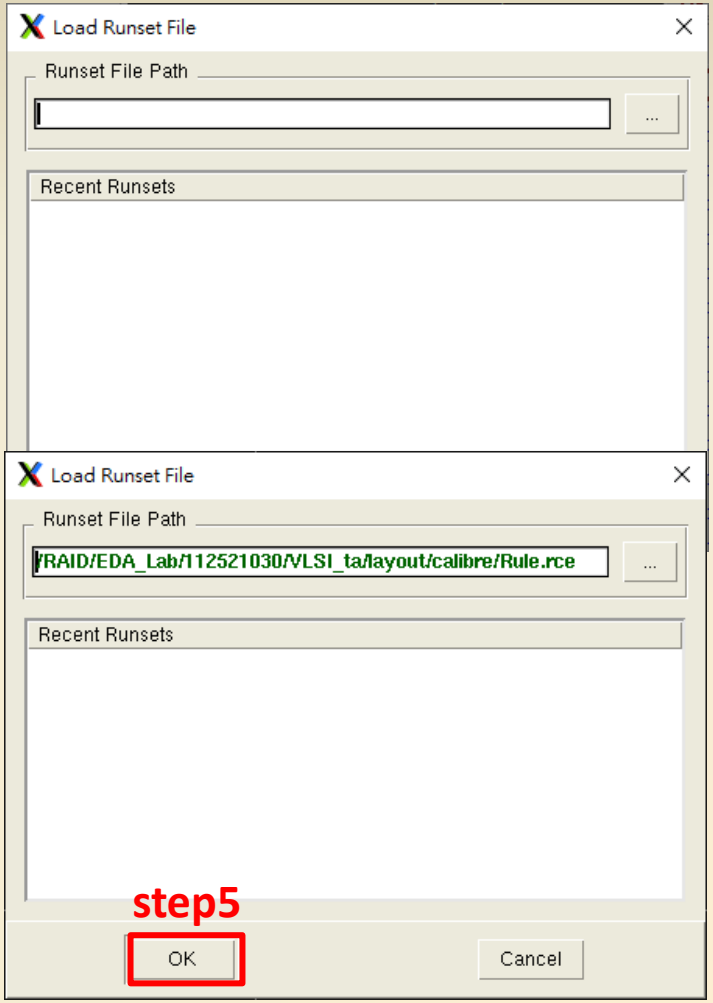


Step 9 Run PEX

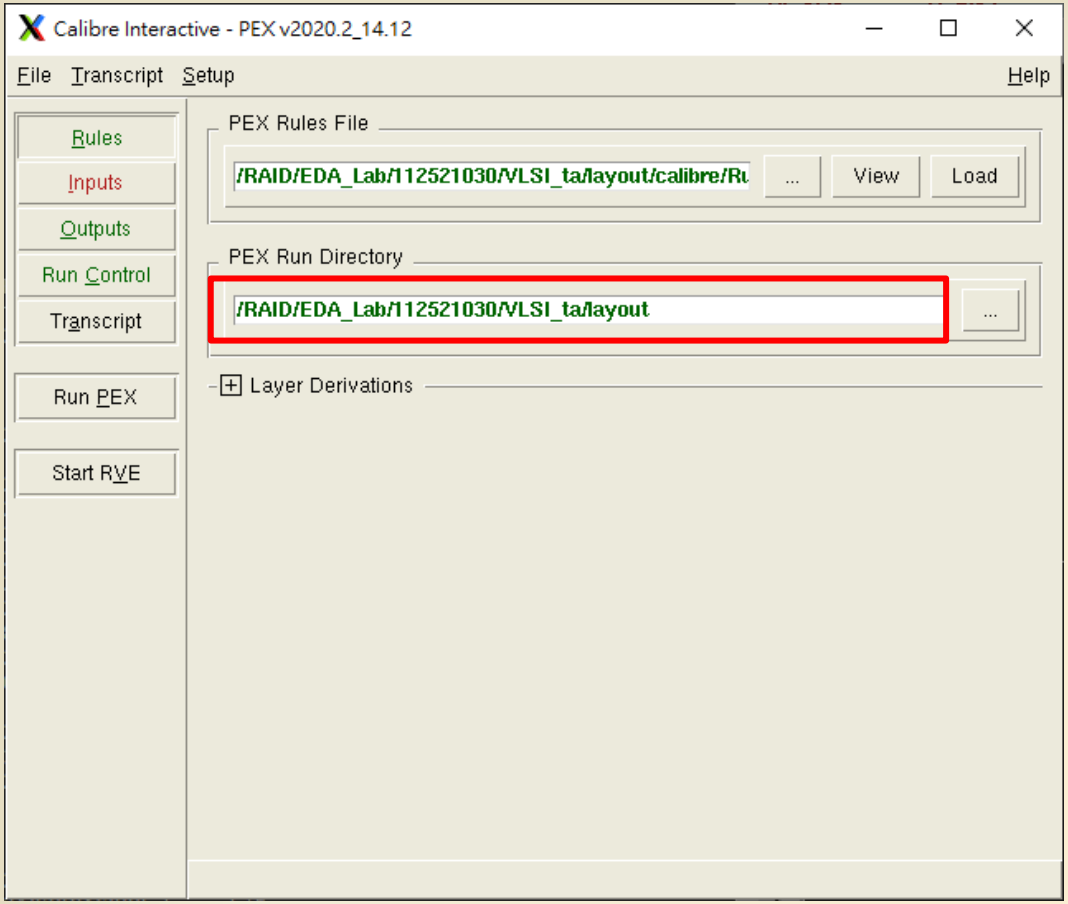


Step 9-1

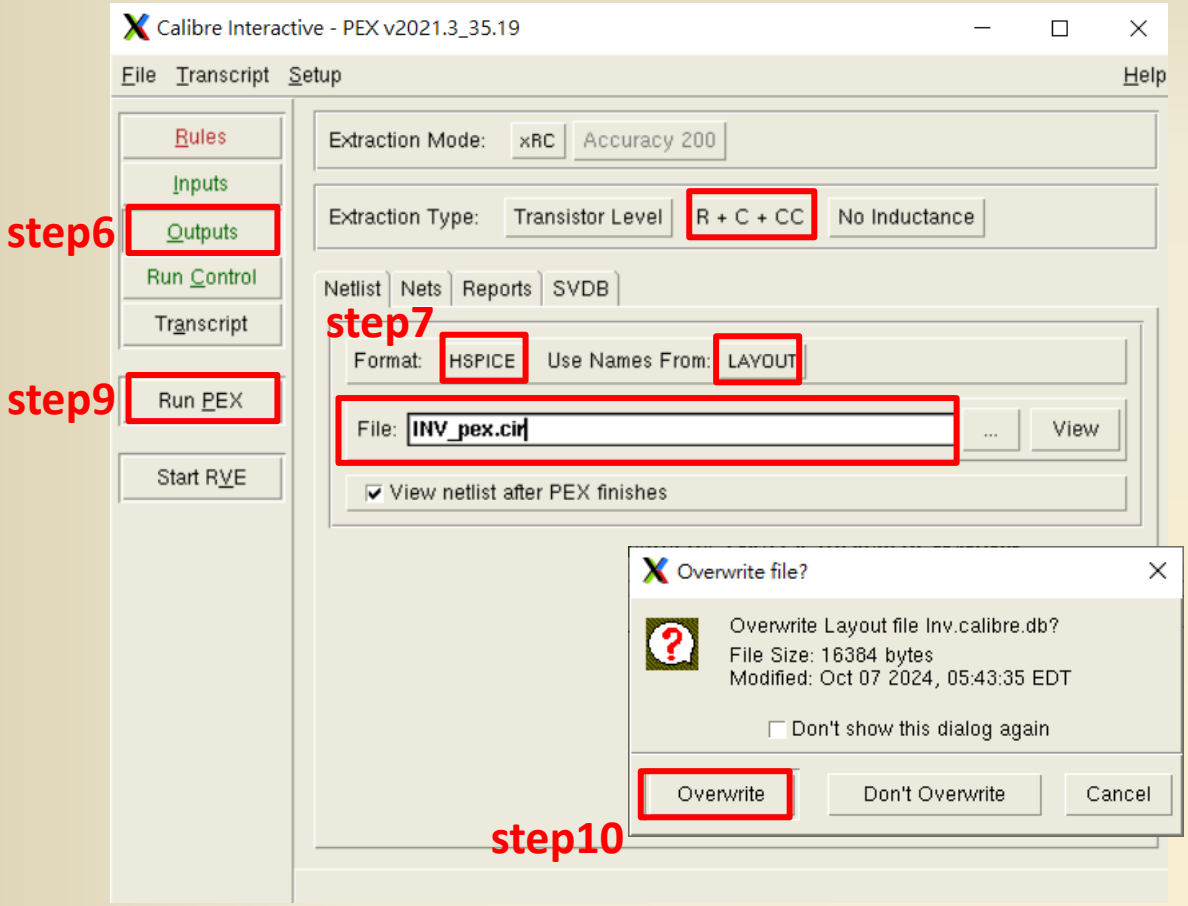

Calibre Interactive - PEX v2020.2_14.12
File Transcript Setup Help
Rules
Inputs
Outputs
Run Control
Transcript
Run PEX
step1
PEX Rules File
rules
...
View
Load
step2
PEX Run Directory
.
Layer Derivations
Choose Runset (Files:5)
Look in: /RAID/EDA_Lab/112521030/VLSI_ta/layout/calibre
rule.drc
Rule.rce
Rule_20KA.rc
step3
File name: Rule.rce
File type: All Files (*)
OK
Cancel
step4


Load Runset File
Runset File Path
Recent Runsets
Load Runset File
Runset File Path
/RAID/EDA_Lab/112521030/VLSI_ta/layout/calibre/Rule.rce
Recent Runsets
step5
OK
Cancel

Step 9-2

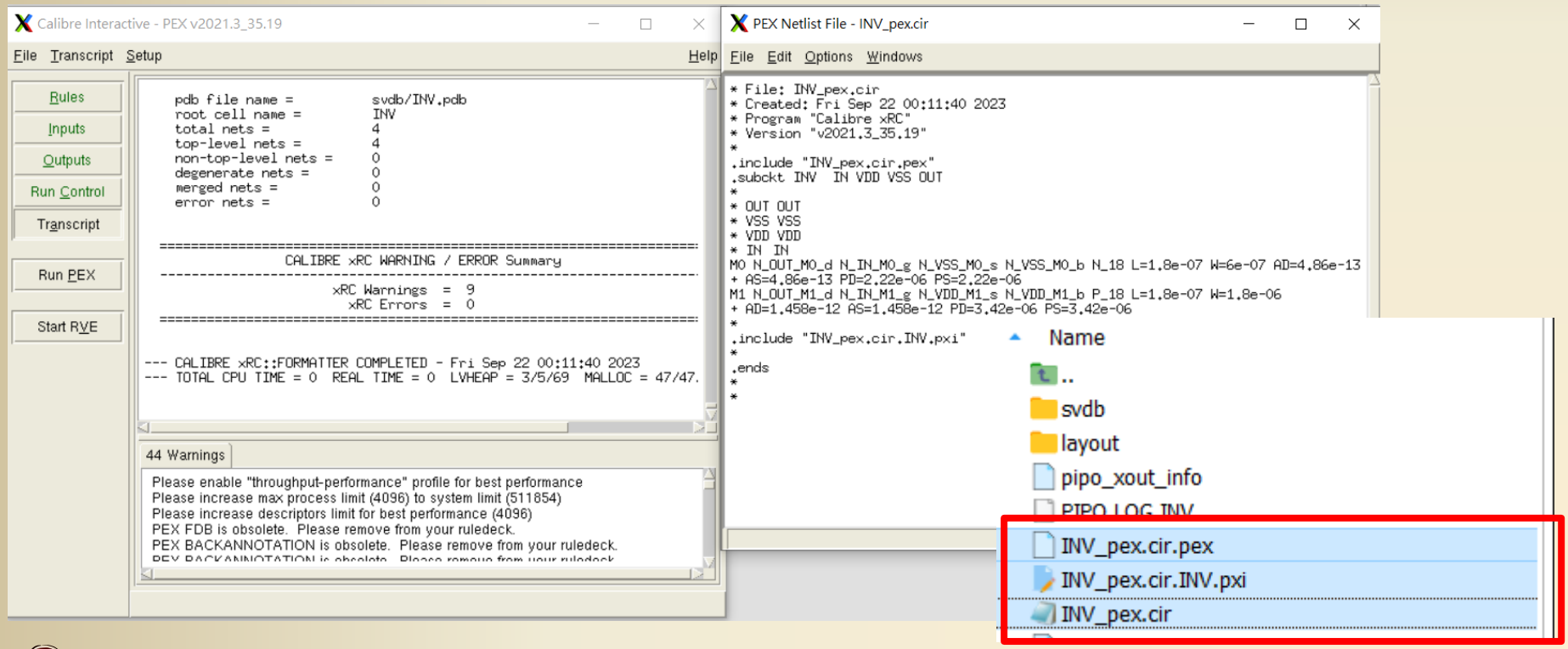

Calibre Interactive - PEX v2020.2_14.12
File
Transcript
Setup
Help
Rules
Inputs
Outputs
Run Control
Transcript
Run PEX
Start RVE
PEX Rules File
/RAID/EDA_Lab/112521030/VLSI_ta/layout/calibre/Ru
...
View
Load
PEX Run Directory
/RAID/EDA_Lab/112521030/VLSI_ta/layout
...
Layer Derivations

Step 9-4


Calibre Interactive - PEX v2021.3_35.19
File Transcript Setup Help
Rules
Inputs
step6
Outputs
Run Control
Transcript
step9
Run PEX
Start RVE
Extraction Mode: xRC Accuracy 200
Extraction Type: Transistor Level R + C + CC No Inductance
Netlist Nets Reports SVDB
step7
Format: HSPICE Use Names From: LAYOUT
File: INV_pex.cir ... View
View netlist after PEX finishes
Overwrite file?
Overwrite Layout file Inv.calibre.db?
File Size: 16384 bytes
Modified: Oct 07 2024, 05:43:35 EDT
Don't show this dialog again
Overwrite
Don't Overwrite
Cancel
step10

Step 9-5

- PEX done



It will generate three files under /INV

PEX Files

- Netlist(.cir, .sp, …)
- .pex
  - The metal routing traces corresponding to each node are extracted as a subcircuit, which contains the parasitic RC of these routing traces
- .pix
  - Call the subcircuit in .pex as an instance. This instance connects all the devices on the node.

Step 10 Run Post-sim

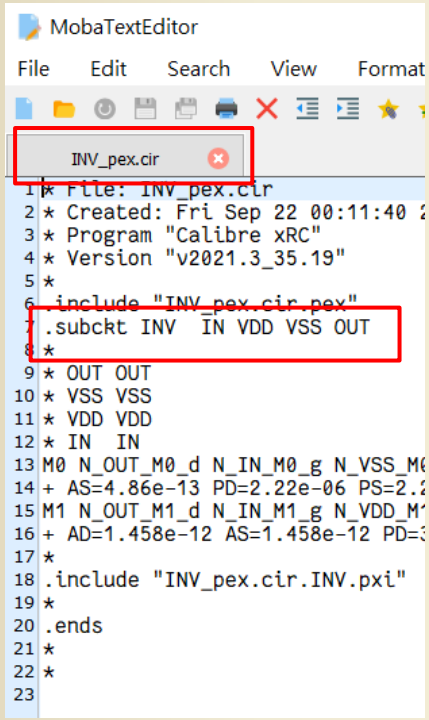
- You can copy the three files into directory post_sim to run post-layout simulation

```
[ta112521030@linuxcad30 layout]$ cd ../spice/post_sim/hw2
```

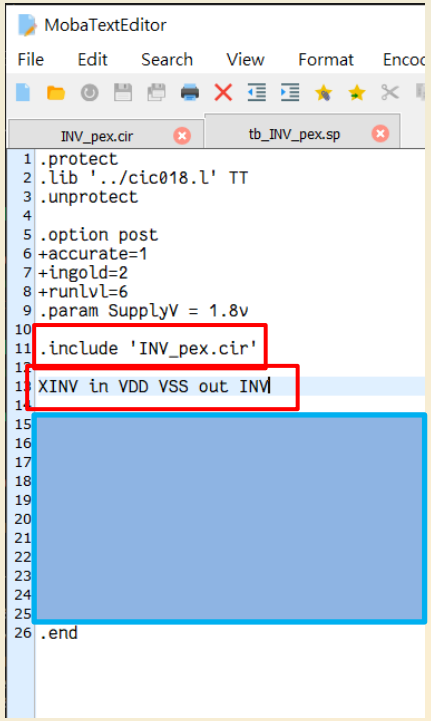
```
[ta112521030@linuxcad30 hw2]$ cp ../../../layout/hw2/INV/INV_pex.cir.pex INV_pex.cir.pex
[ta112521030@linuxcad30 hw2]$ cp ../../../layout/hw2/INV/INV_pex.cir.INV.pxi INV_pex.cir.INV.pxi
[ta112521030@linuxcad30 hw2]$ cp ../../../layout/hw2/INV/INV_pex.cir INV_pex.cir
```

Step 10-1

- Make sure your post-sim testbench include the netlist generated by PEX



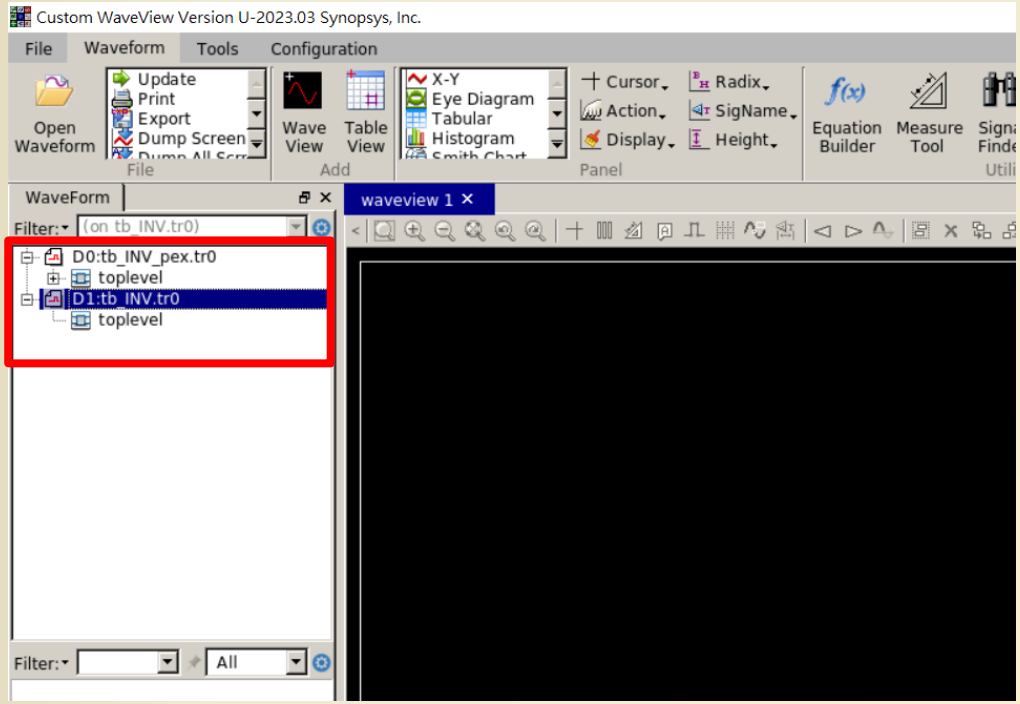
INV_pex.cir



Testbench.sp

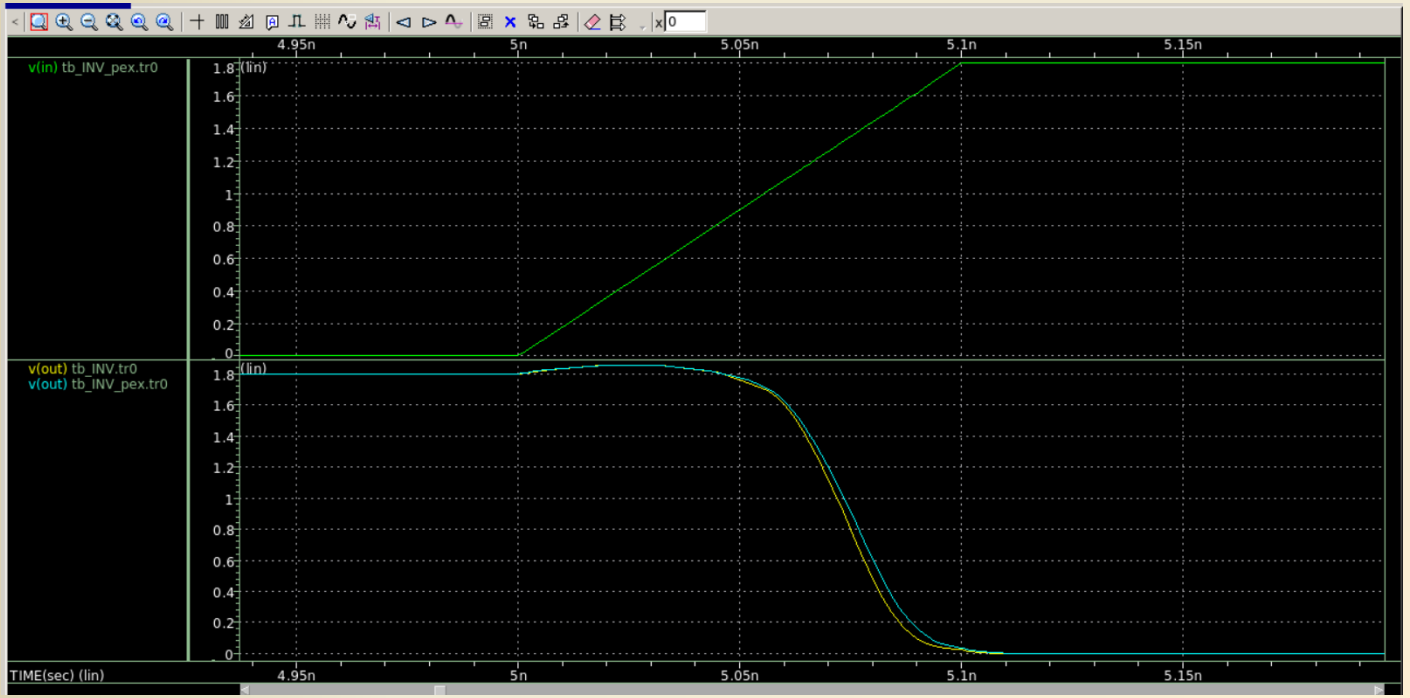
Step 10-2

- Open waveview and open both pre-sim waveform and post-sim waveform



Step 10-3

- There will be some differences between two waveforms



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