CS3120

Introduction of Integrated Circuit Design

Virtuoso Layout Tutorial

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Outline

- Virtuoso
- User Interface
- Shortcut Key
- Inverter
- Design Rule Check
- Layout Versus Schematic
- Reference

Outline

- **Virtuoso**
- User Interface
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Virtuoso

- The full custom IC layout suite of the Cadence Virtuoso Studio
- The Virtuoso Layout Suite supports custom analog, digital, RF, and mixed-signal designs at the device, cell, block, and chip levels
- The Virtuoso Layout Suite enables the creation of differentiated custom silicon that is both fast and silicon accurate

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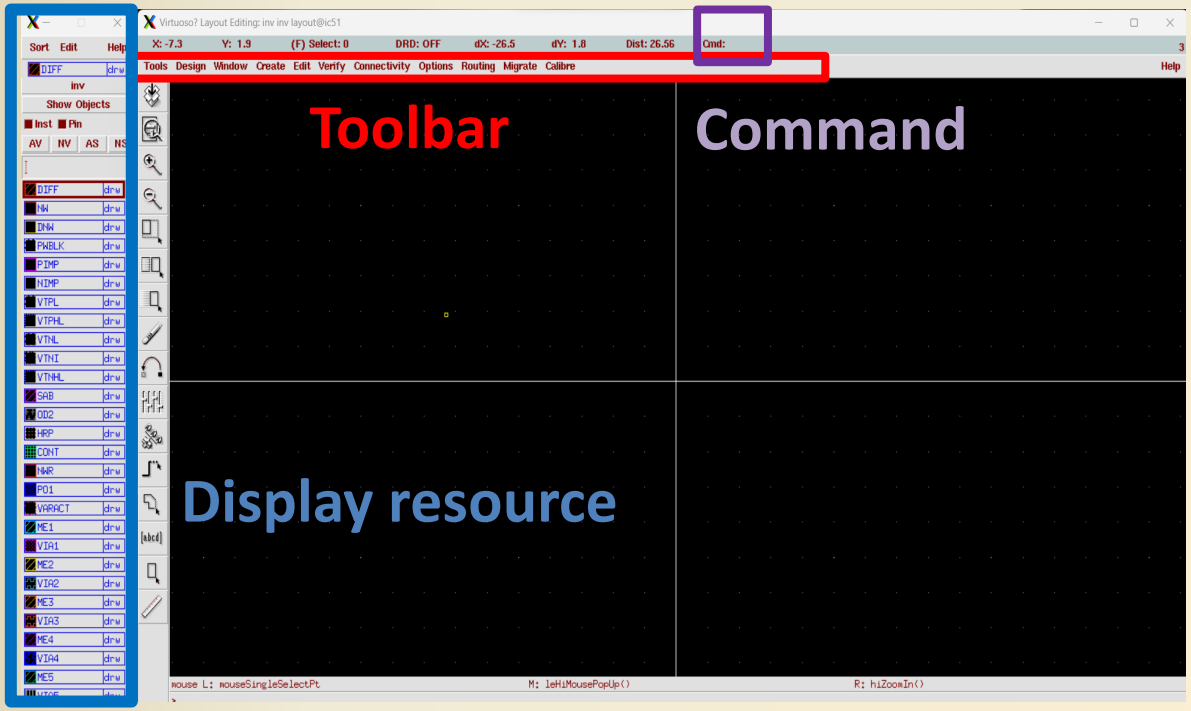
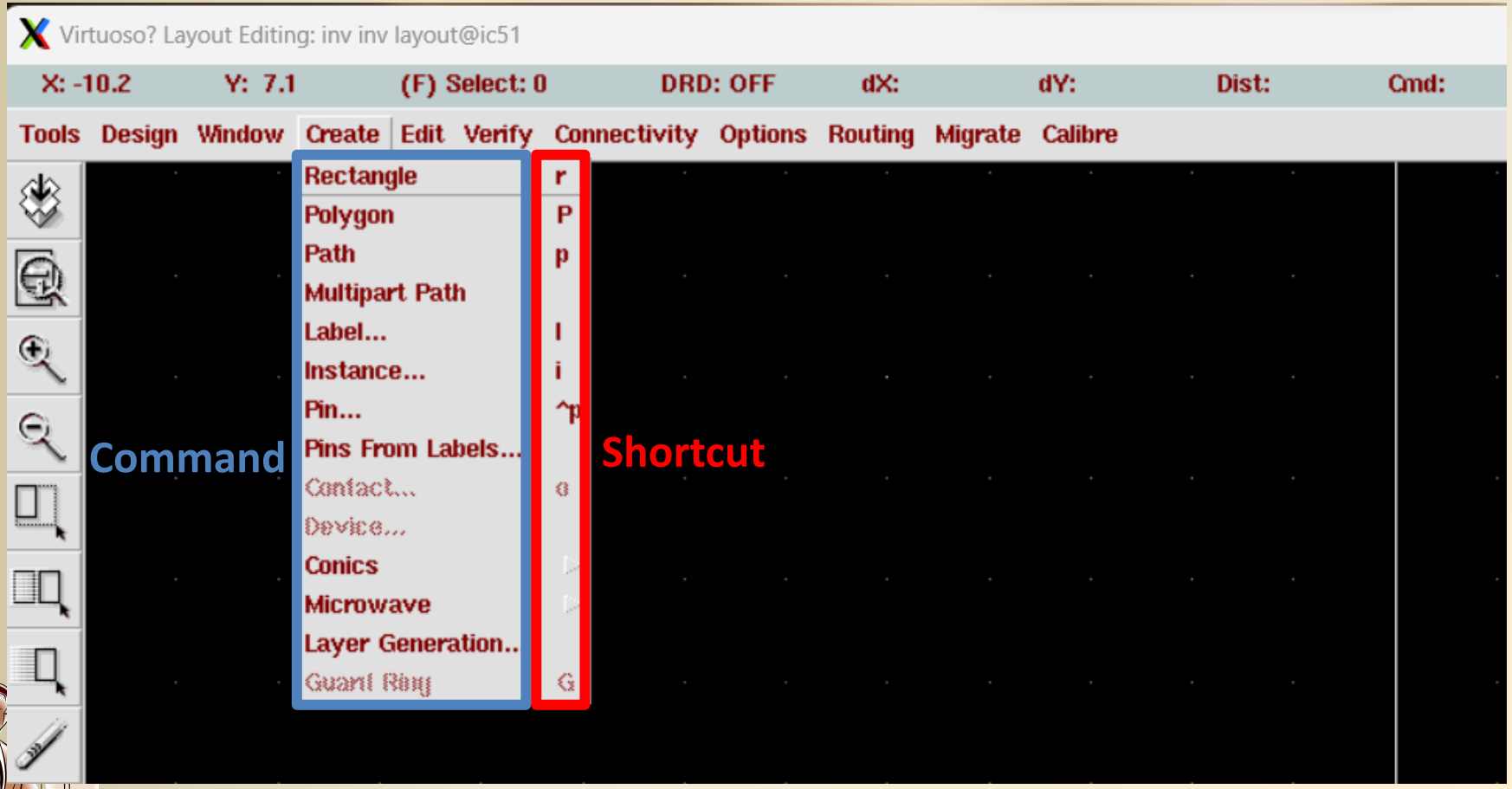
User interface

- Toolbar: Use the tool and start simulation
- Command: Show the current status
- Display resource: Change used resource

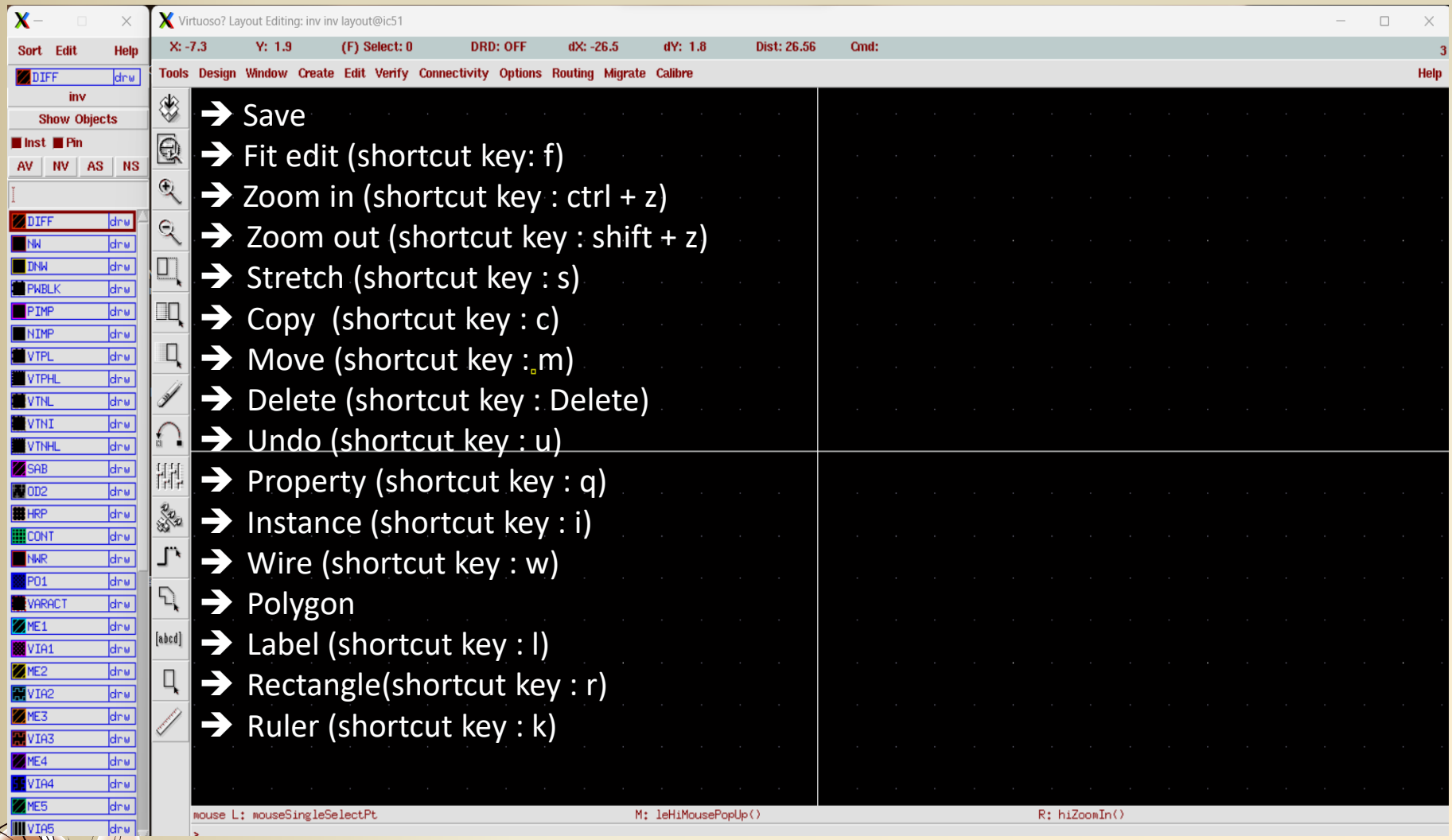


User interface

- You can use tools and check shortcut keys in the toolbar



User interface



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Shortcut Key

- Take “Rectangle” mode for example
- Tap the shortcut key “r” on the keyboard
- Check the status from “Cmd”

- Tap “Esc” on the keyboard to exit the mode

Shortcut Key

- K(and Shift +K)➔add rules to measure distance (delete all the rules)
- e ➔ options
- r ➔ add a rectangle
- p ➔ add a path
- l ➔ add a label
- c ➔ copy selected cell
- m ➔ move selected cell
- q ➔ edit properties
- Shift+o ➔ rotate the cell
- u ➔ undo
- f ➔ fit to window
- Ctrl +Z or Shift +Z (also mouse wheel) ➔ zoom in/out
- z ➔ Zoom in to your selected area
- Ctrl+F or Shift+F ➔ switch between visible and invisible instance layouts

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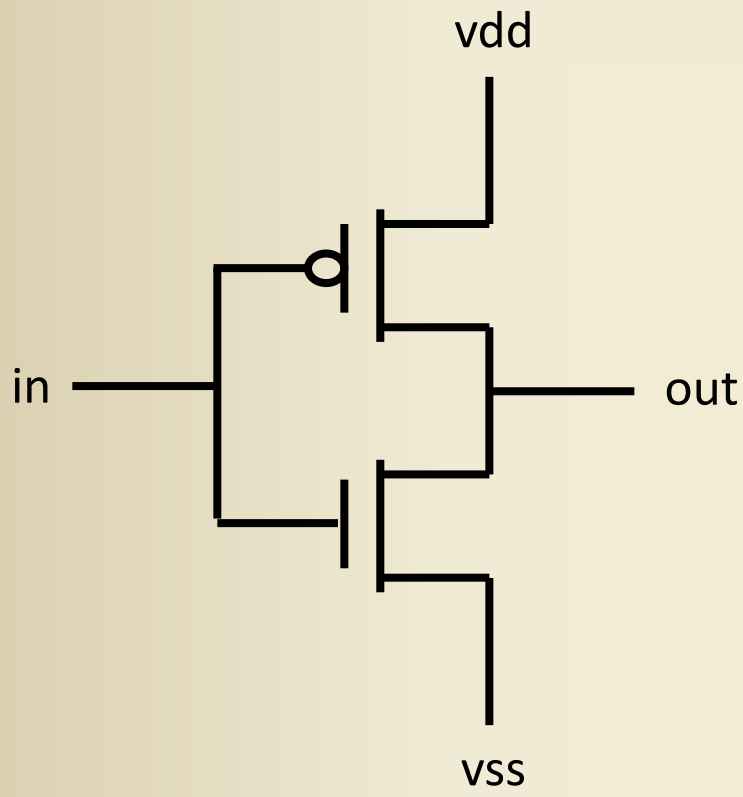
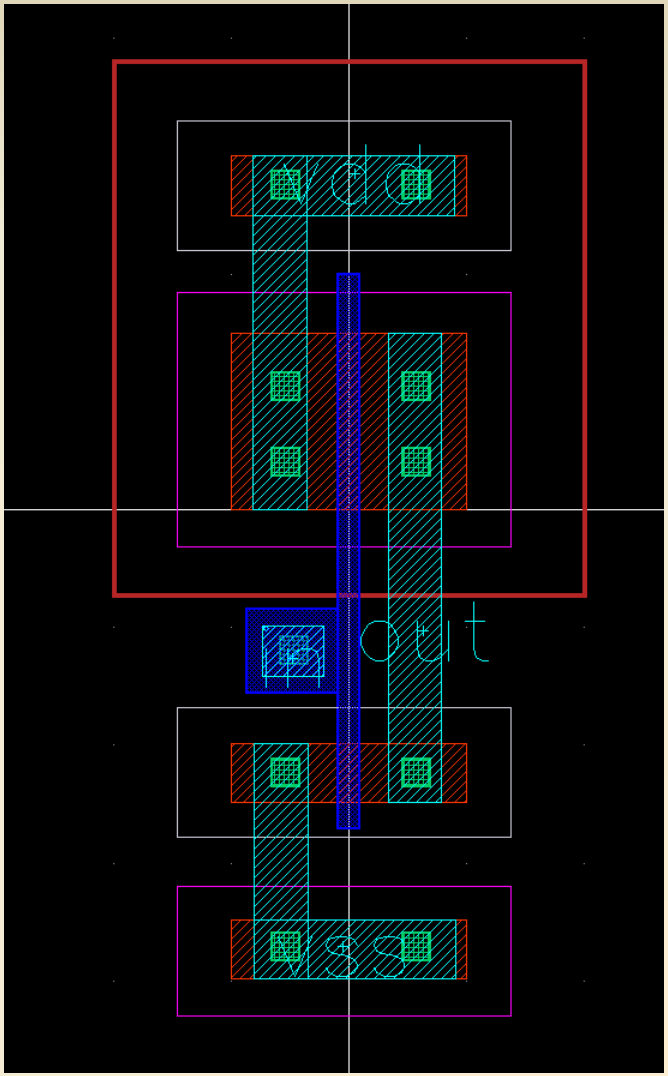
- **Inverter**
- Design Rule Check
- Layout Versus Schematic
- Reference

Inverter

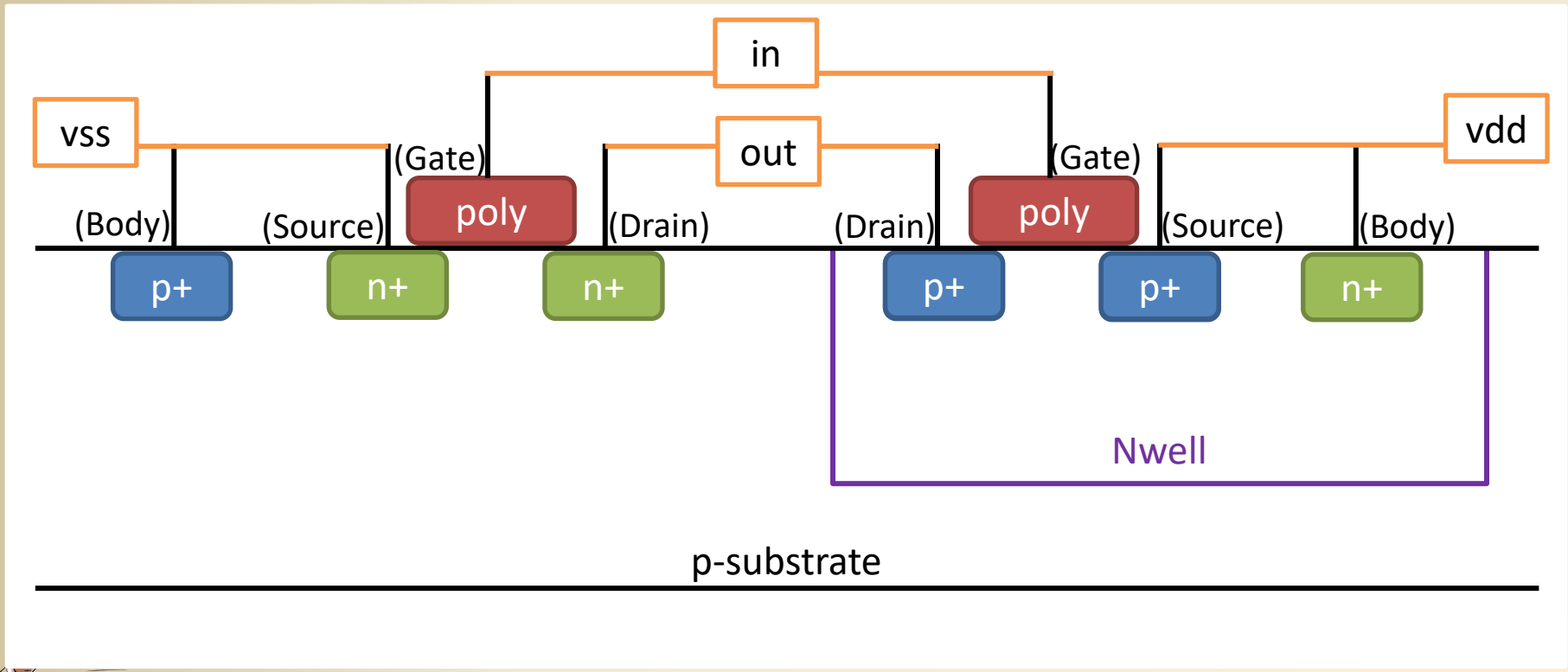
- .subckt inv in out vdd vss





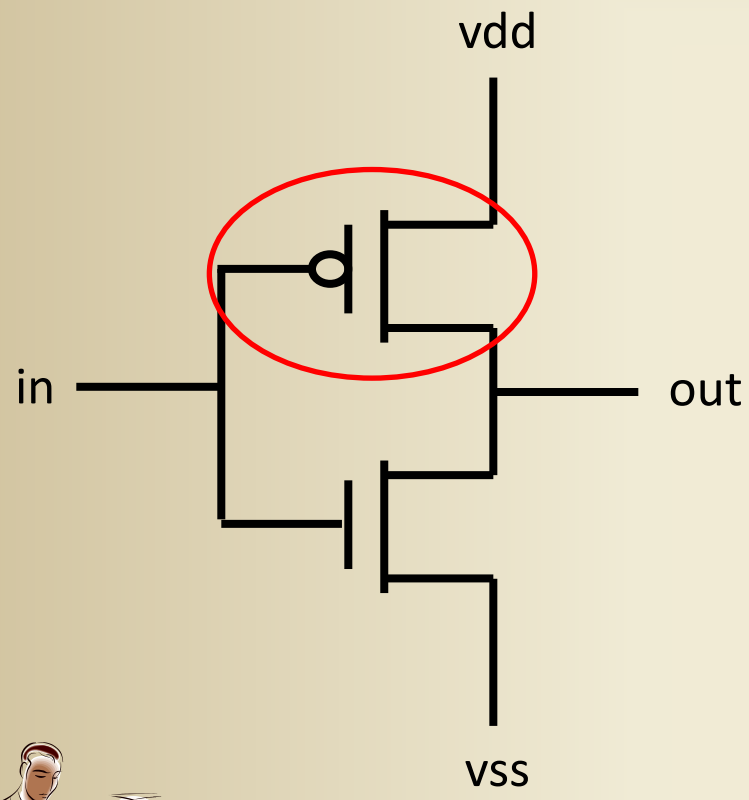
Inverter

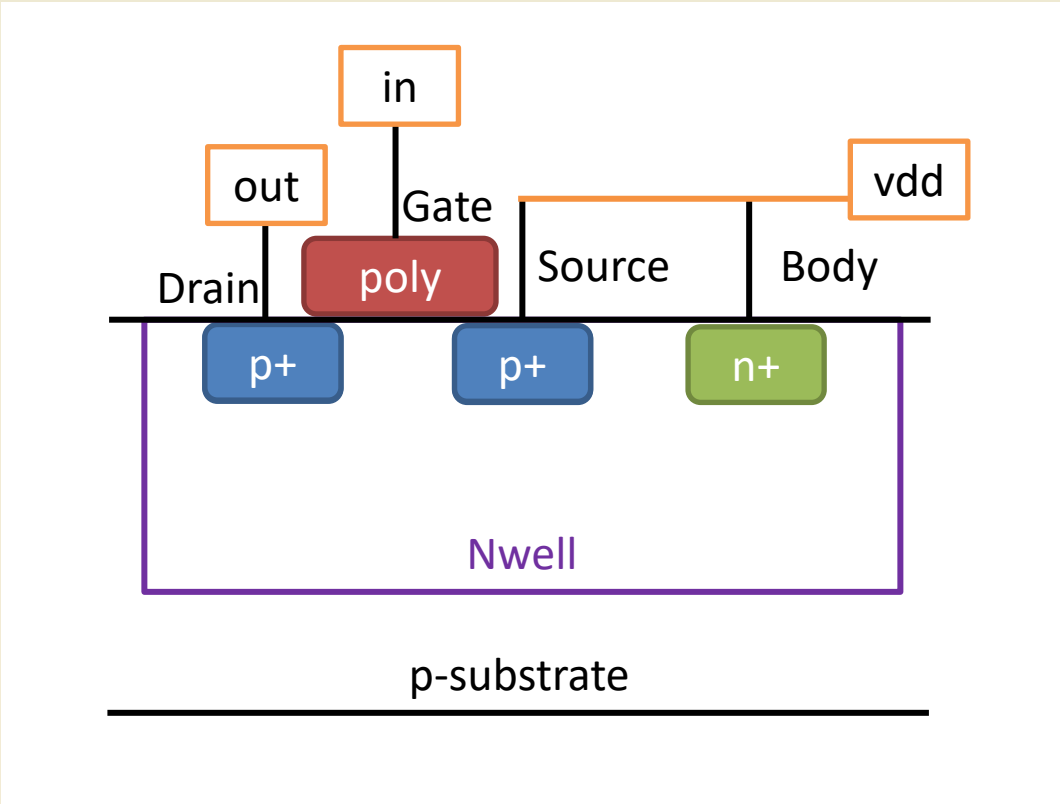
NMOS PMOS



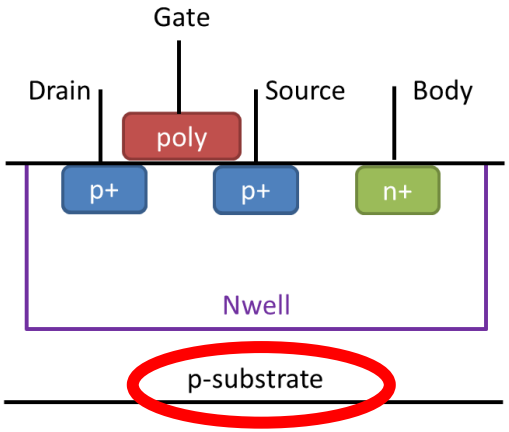
Inverter

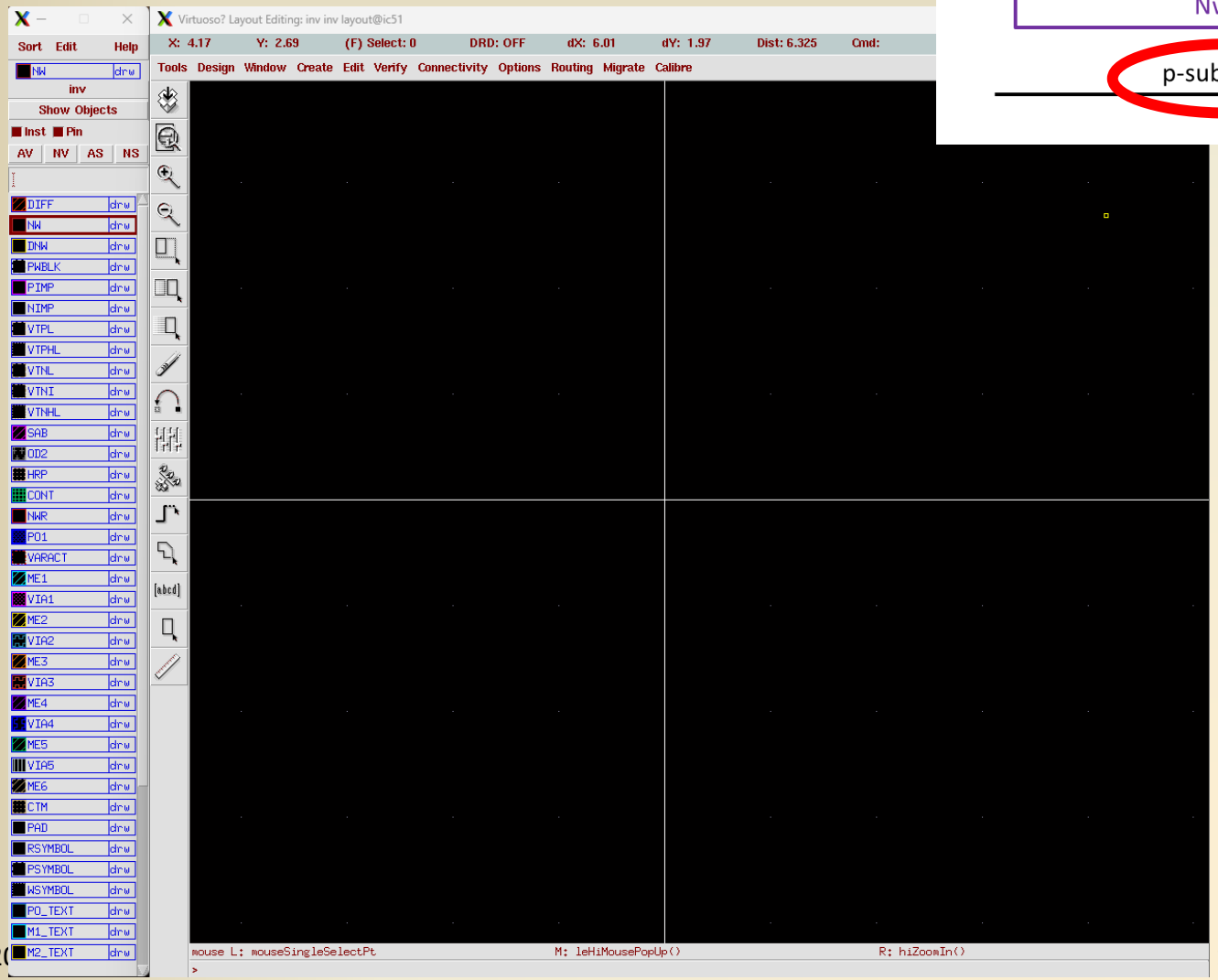
- PMOS



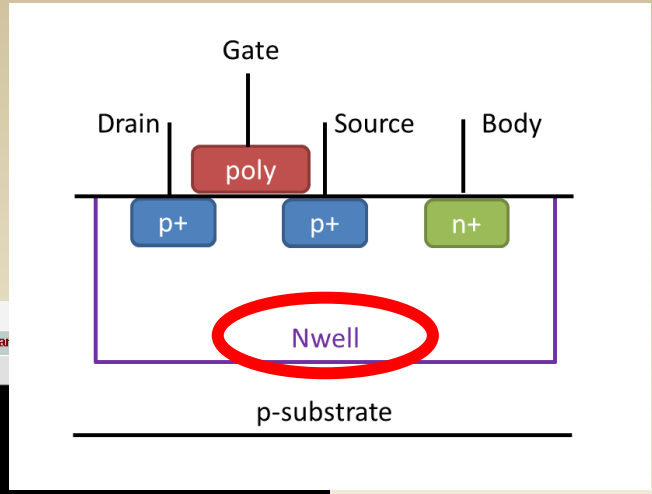


p-substrate

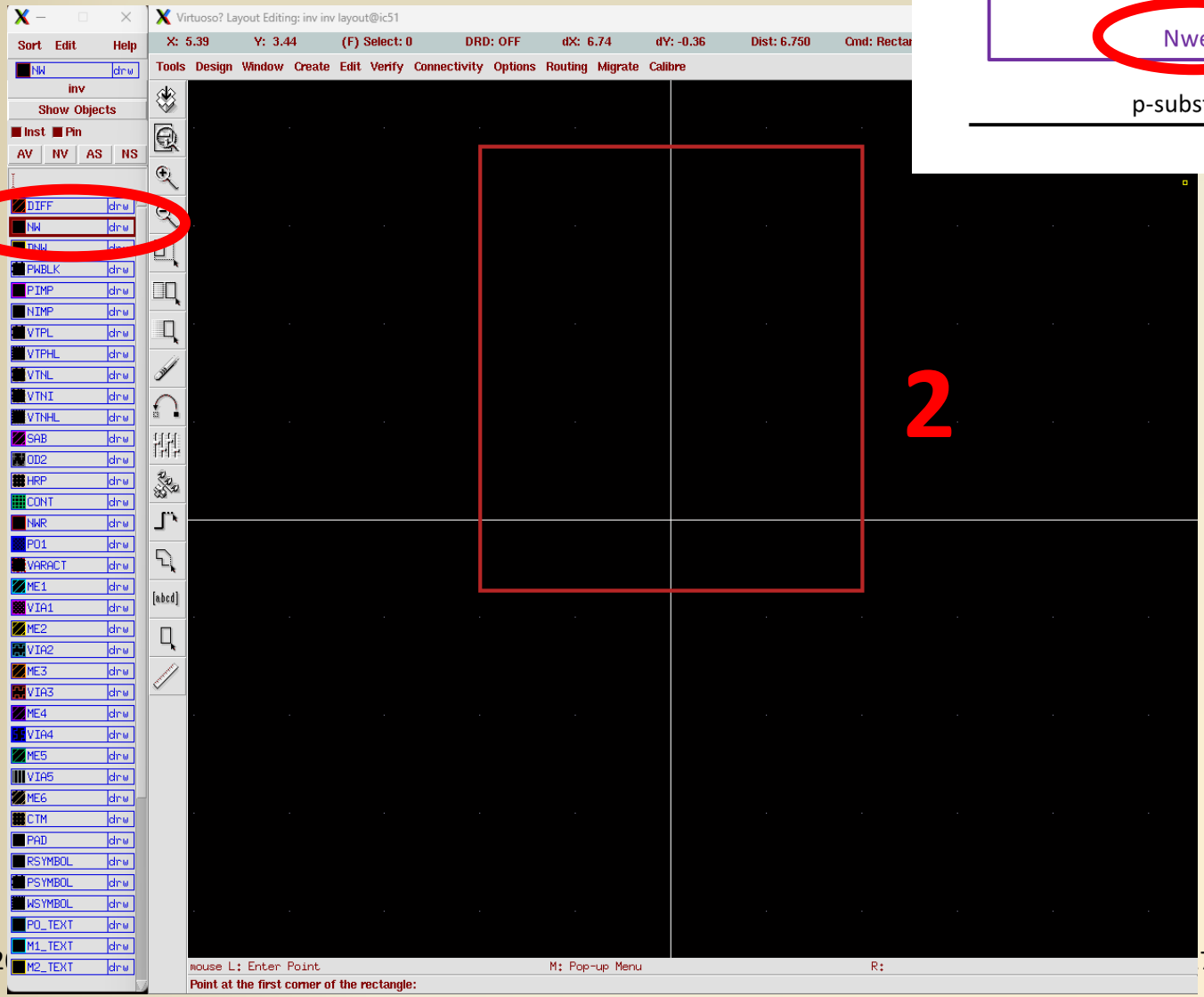

Gate
Drain
Source
Body
poly
p+
p+
n+
Nwell
p-substrate


Virtuoso? Layout Editing: inv inv layout@ic51
X: 4.17
Y: 2.69
(F) Select: 0
DRD: OFF
dX: 6.01
dY: 1.97
Dist: 6.325
Cmd:
Sort Edit Help
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre
Show Objects
Inst Pin
AV NV AS NS
DIFF
NW
DNW
PWBLK
PIMP
NIMP
VTPL
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
M2_TEXT
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: hiZoomIn()

n-well (NW)

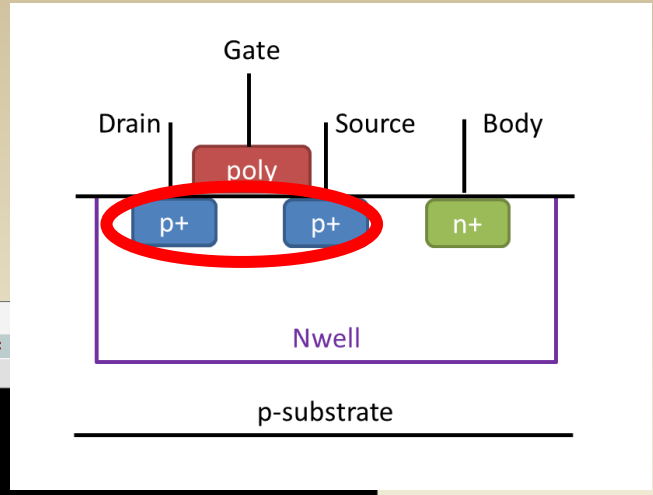

Gate
Drain
Source
Body
poly
p+
p+
n+
Nwell
p-substrate

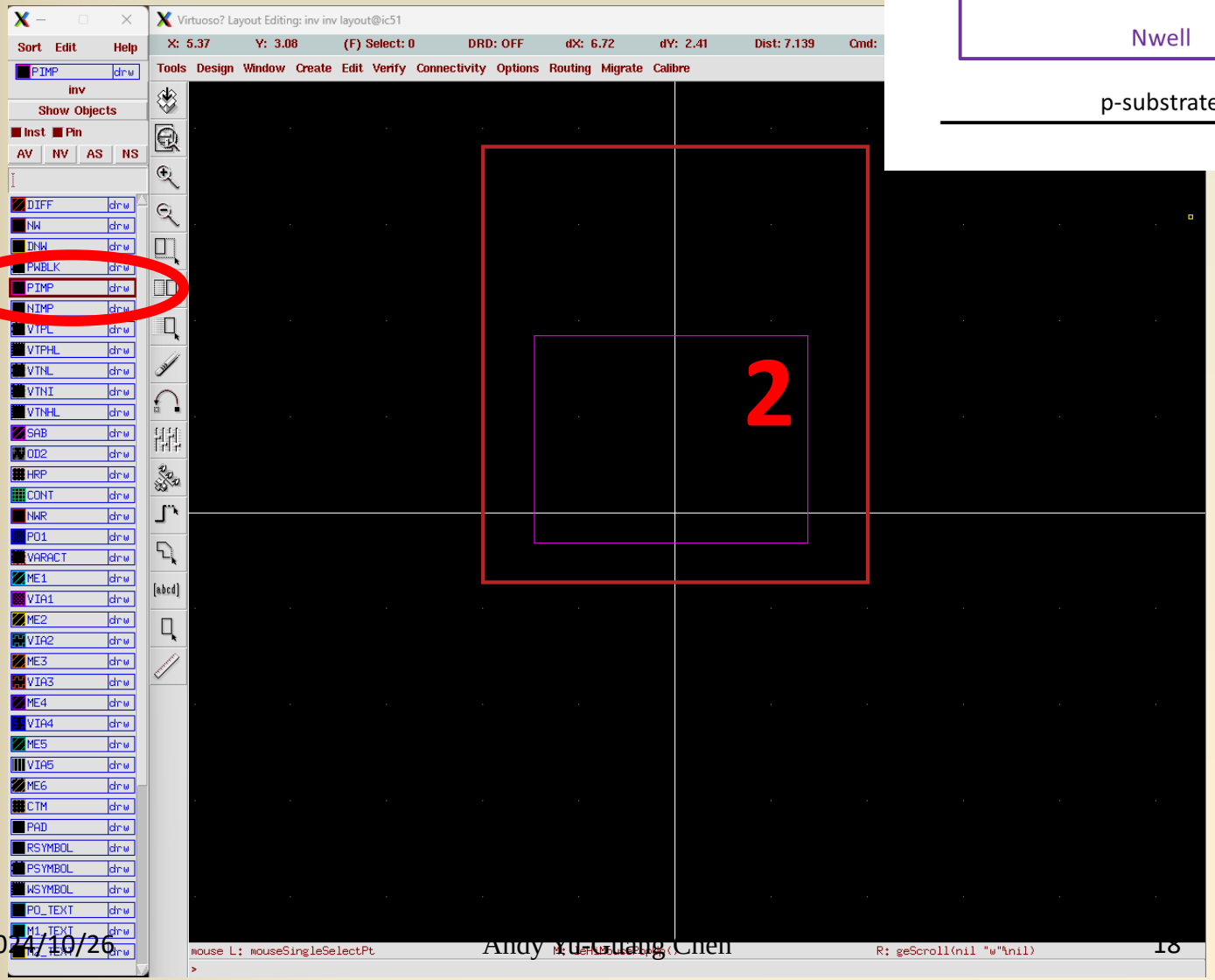
1


Virtuoso? Layout Editing: inv inv layout@ic51
X: 5.39
Y: 3.44
(F) Select: 0
DRD: OFF
dX: 6.74
dY: -0.36
Dist: 6.750
Sort
Edit
Help
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Migrate
Calibre
Show Objects
Inst
Pin
AV
NV
AS
NS
DIFF
NW
PWBLK
PIMP
NIMP
VTPL
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
M2_TEXT
mouse L: Enter Point
M: Pop-up Menu
R:
Point at the first corner of the rectangle:

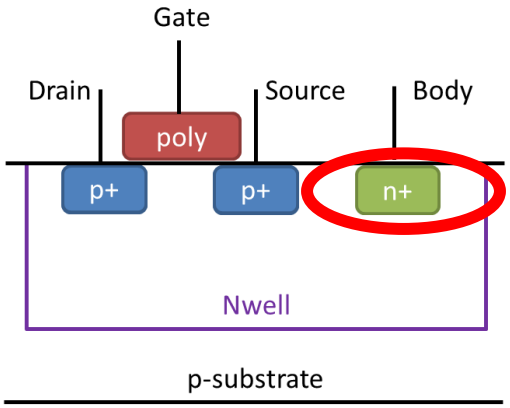
2

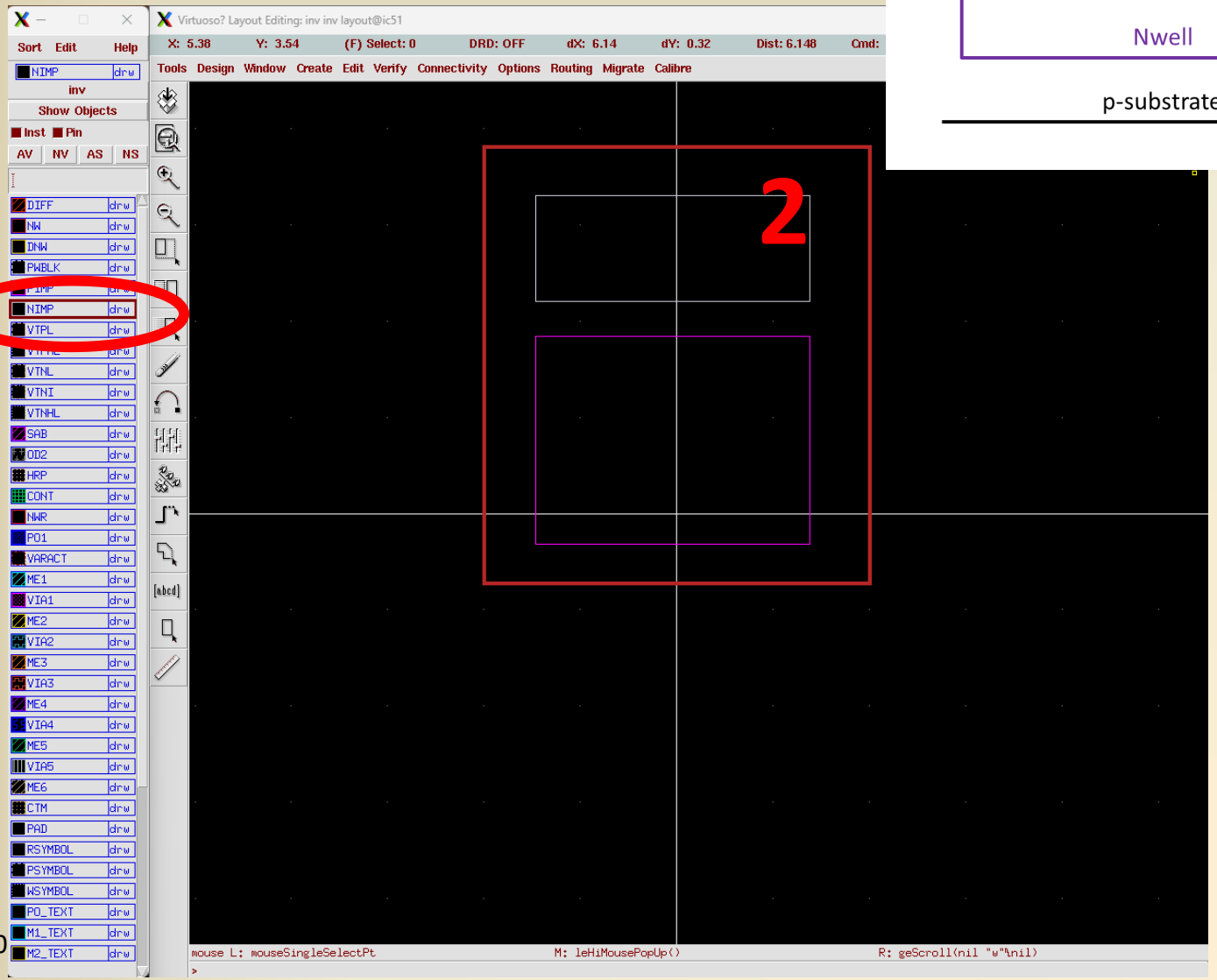
P+ (PIMP)


Gate
Drain
Source
Body
poly
p+
p+
n+
Nwell
p-substrate

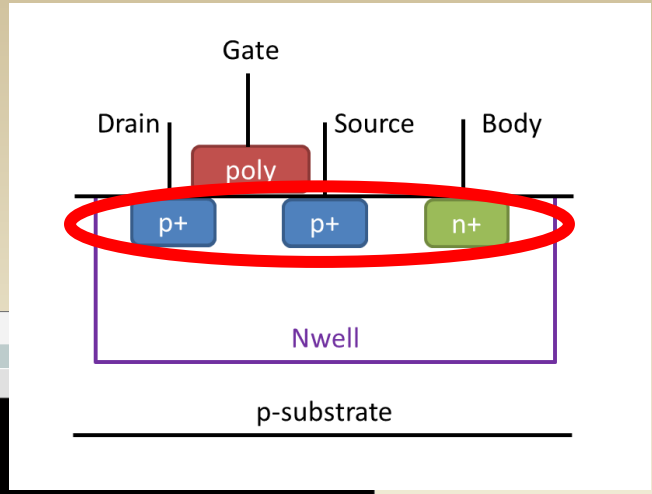

Virtuoso? Layout Editing: inv inv layout@ic51
X: 5.37
Y: 3.08
(F) Select: 0
DRD: OFF
dX: 6.72
dY: 2.41
Dist: 7.139
Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre
Sort Edit Help
PIMP
inv
Show Objects
Inst Pin
AV NV AS NS
DIFF
NW
DNW
PWBLK
PIMP
NIMP
VTPL
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
1
2
mouse L: mouseSingleSelectPt
R: geScroll(nil "w"\nil)

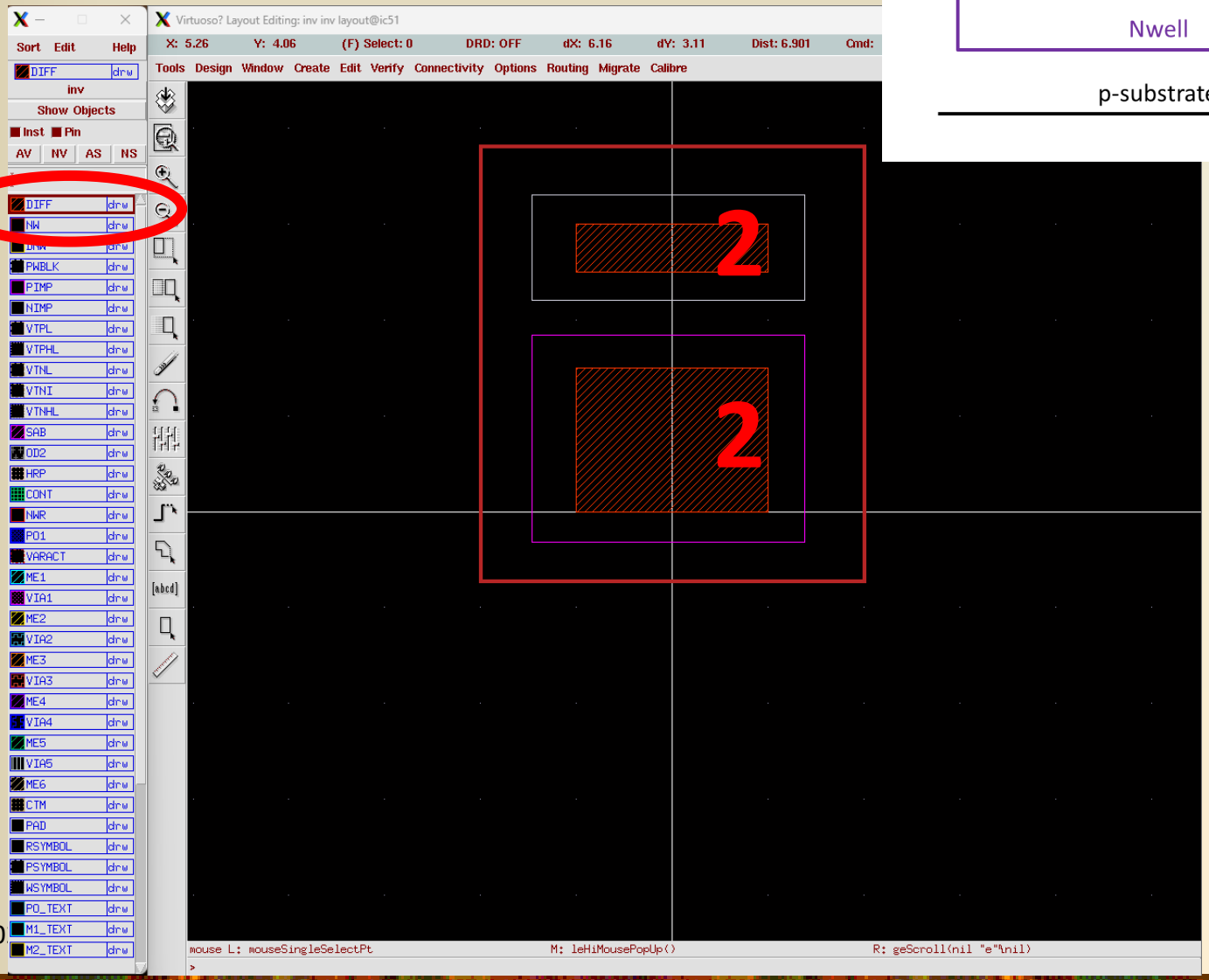
N+ (NIMP)


Gate
Drain
Source
Body
poly
p+
p+
n+
Nwell
p-substrate

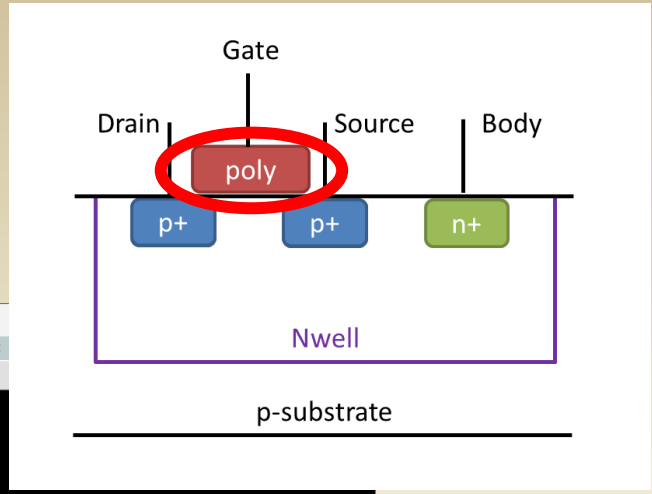

Virtuoso? Layout Editing: inv inv layout@ic51
X: 5.38
Y: 3.54
(F) Select: 0
DRD: OFF
dX: 6.14
dY: 0.32
Dist: 6.148
Cmd:
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Migrate
Calibre
Sort
Edit
Help
NIMP
inv
Show Objects
Inst
Pin
AV
NV
AS
NS
DIFF
NW
DNW
PWBLK
NIMP
VTPL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
M2_TEXT
1
2
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: geScroll(nil "w"nil)

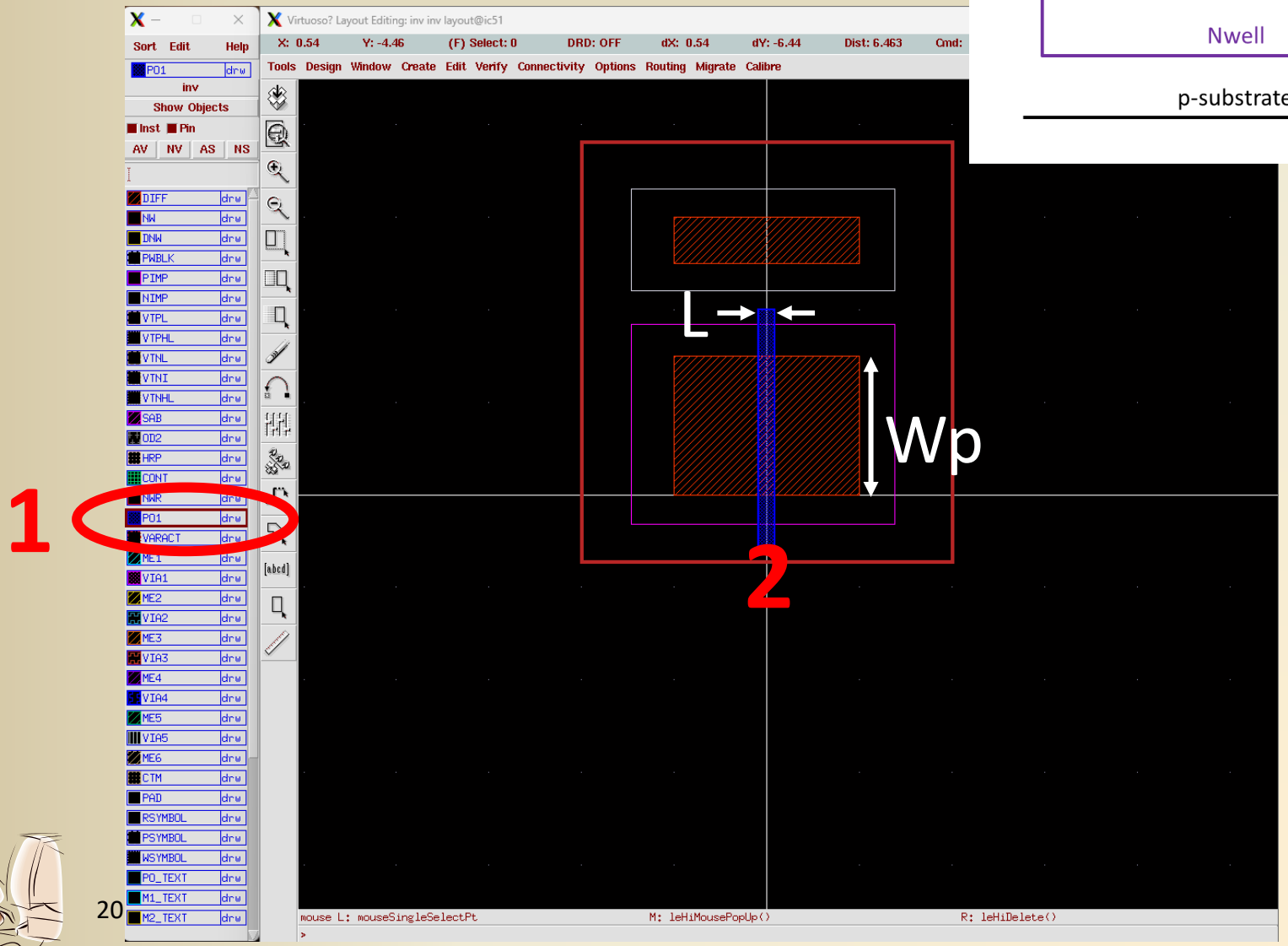
Active (DIFF)


Gate
Drain
Source
Body
poly
p+
p+
n+
Nwell
p-substrate


1
Virtuoso? Layout Editing: inv inv layout@ic51
Sort Edit Help
DIFF drw
inv
Show Objects
Inst Pin
AV NV AS NS
DIFF drw
NW drw
PWBLK drw
PIMP drw
NIMP drw
VTPL drw
VTPHL drw
VTNL drw
VTNI drw
VTNHL drw
SAB drw
OD2 drw
HRP drw
CONT drw
NWR drw
PO1 drw
VARACT drw
ME1 drw
VIA1 drw
ME2 drw
VIA2 drw
ME3 drw
VIA3 drw
ME4 drw
VIA4 drw
ME5 drw
VIA5 drw
ME6 drw
CTM drw
PAD drw
RSYMBOL drw
PSYMBOL drw
WSYMBOL drw
PO_TEXT drw
M1_TEXT drw
M2_TEXT drw
X: 5.26 Y: 4.06 (F) Select: 0 DRD: OFF dX: 6.16 dY: 3.11 Dist: 6.901 Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre
2
2
mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: geScroll(nil "e"\nil)

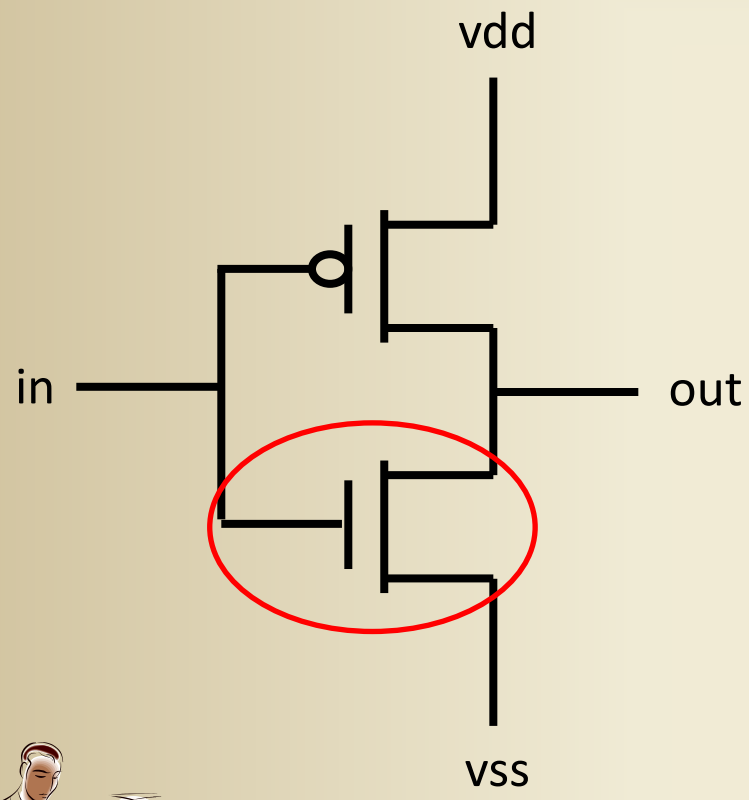
Poly (PO1)

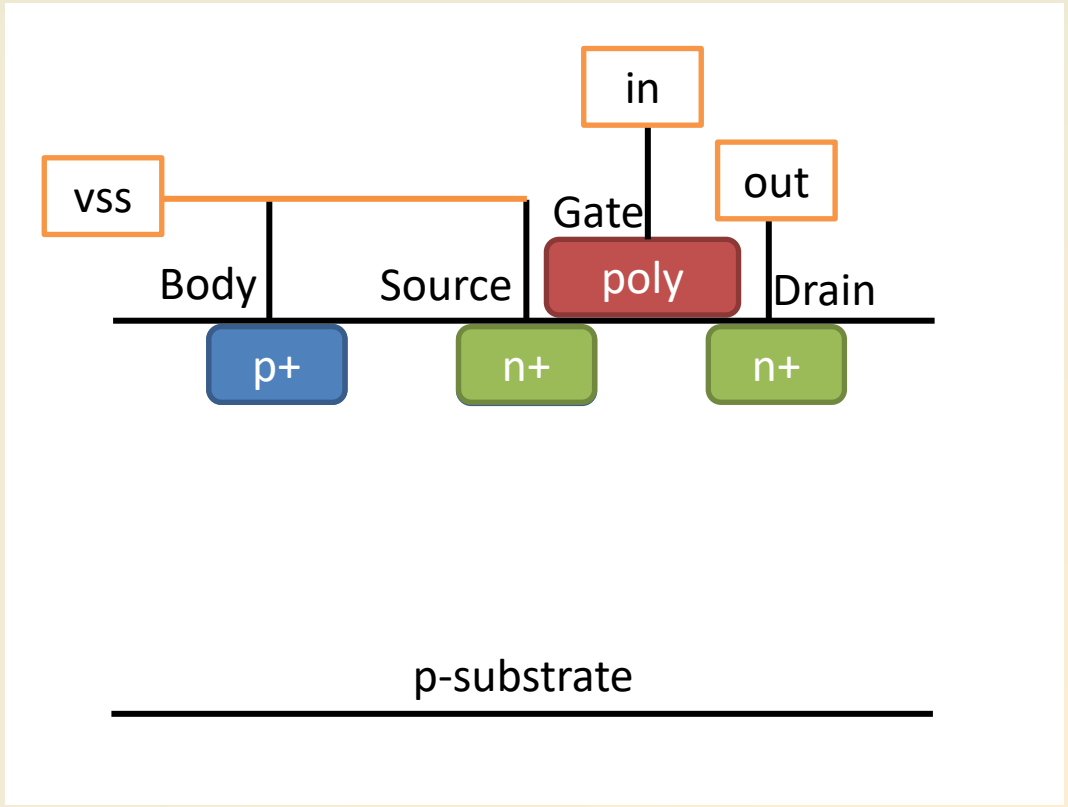

Gate
Drain
Source
Body
poly
p+
p+
n+
Nwell
p-substrate


Virtuoso? Layout Editing: inv inv layout@ic51
X: 0.54
Y: -4.46
(F) Select: 0
DRD: OFF
dX: 0.54
dY: -6.44
Dist: 6.463
Cmd:
Sort
Edit
Help
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Migrate
Calibre
PO1
inv
Show Objects
Inst
Pin
AV
NV
AS
NS
DIFF
NW
DNW
PWBLK
PIMP
NIMP
VTPL
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
M2_TEXT
L
Wp
1
2
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: leHiDelete()

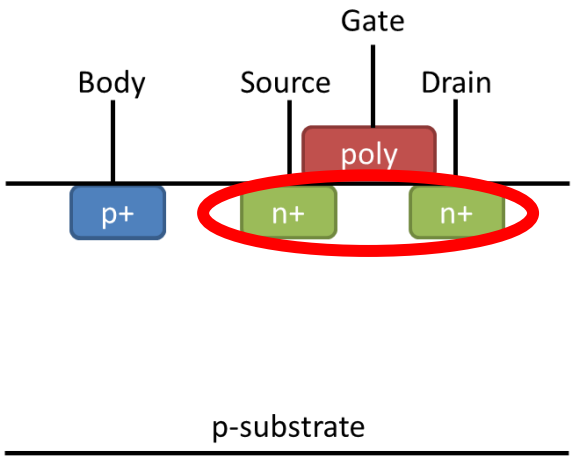
Inverter

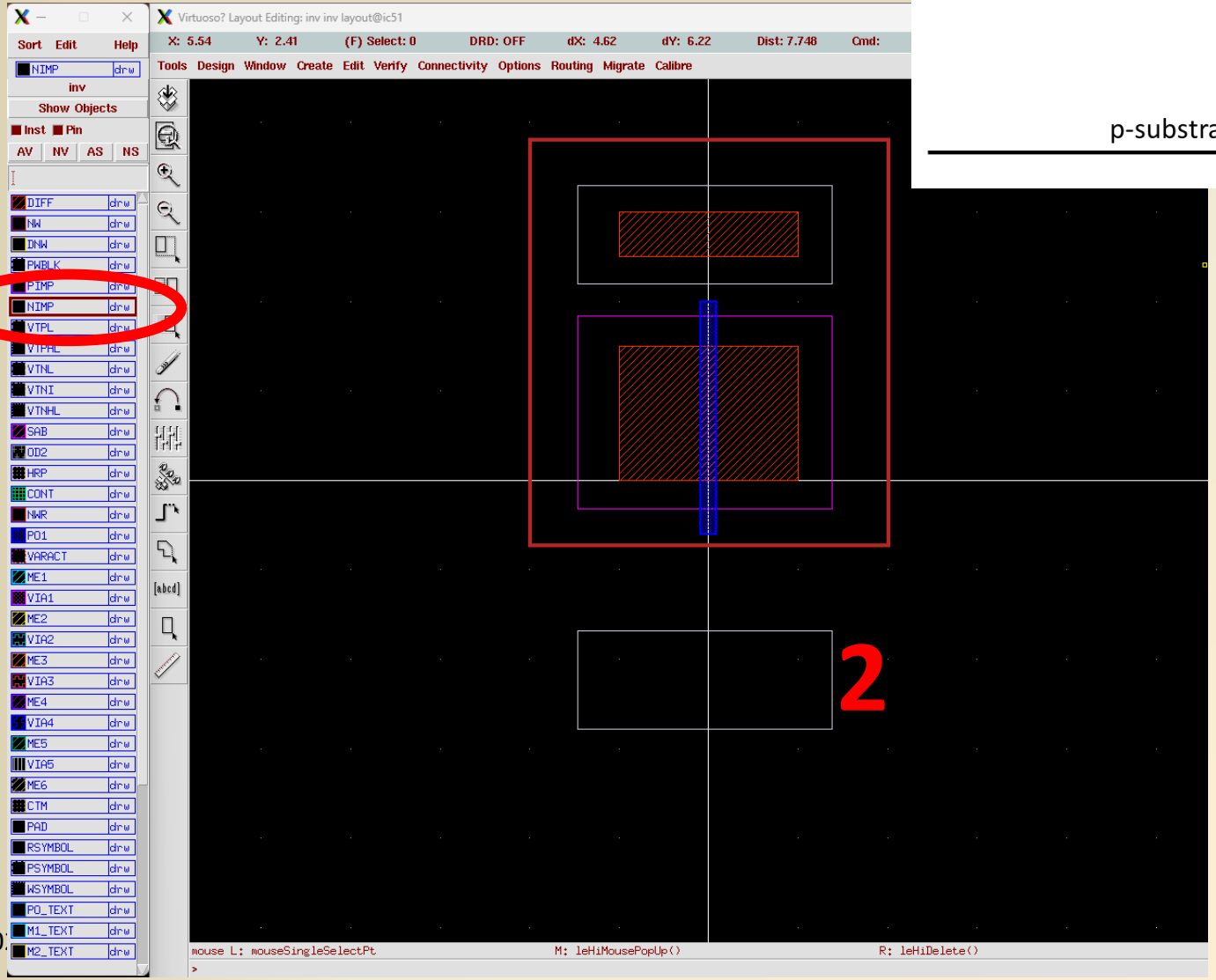
- NMOS



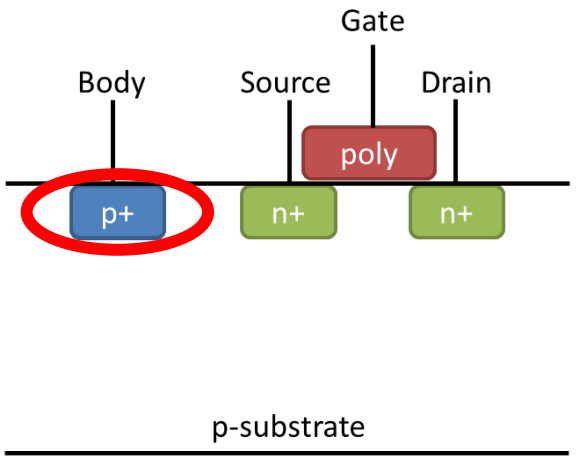


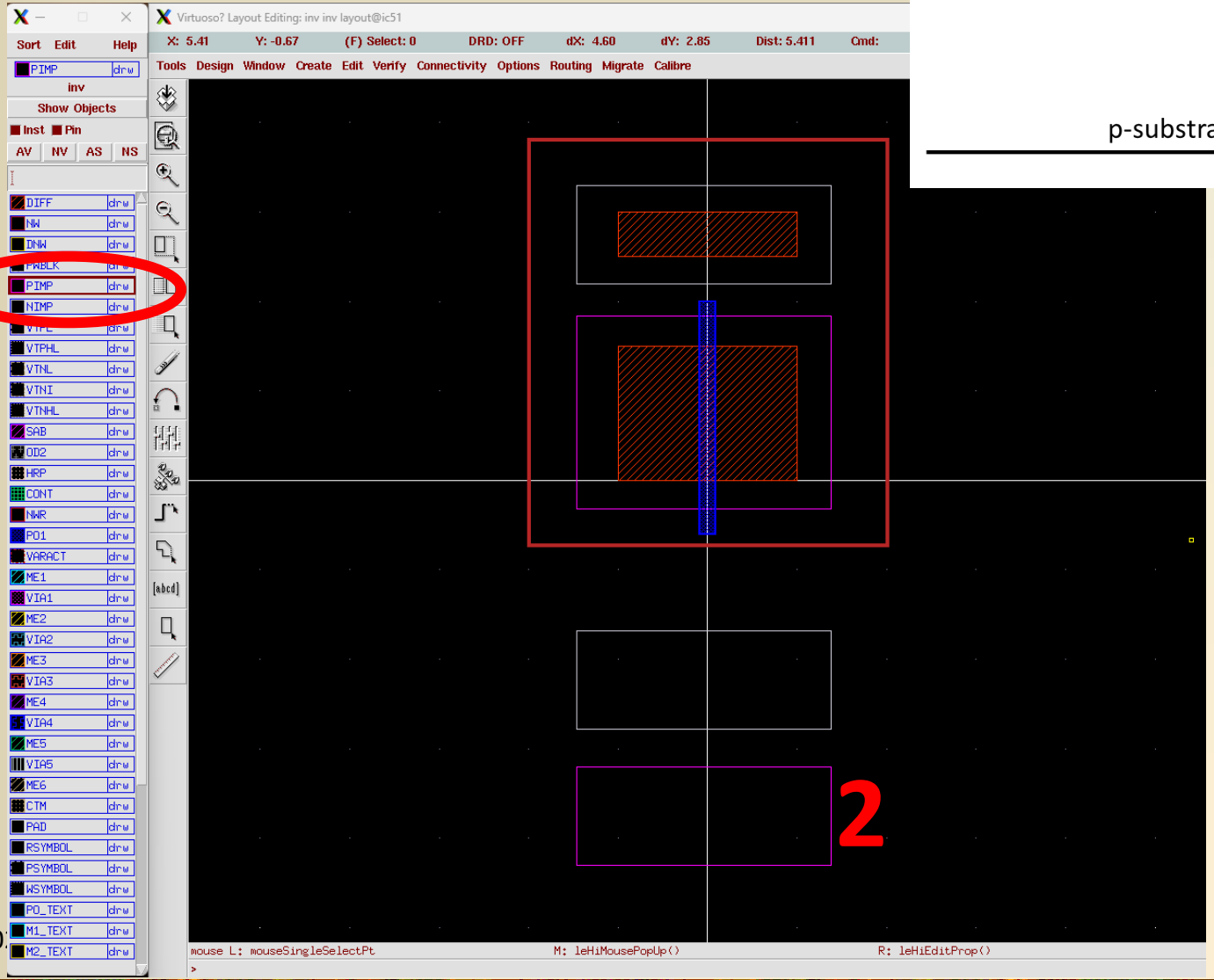
N+ (NIMP)


Gate
Body
Source
Drain
poly
p+
n+
n+
p-substrate

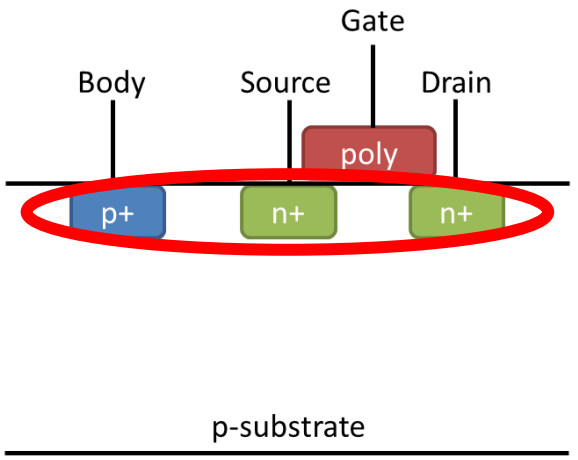

Virtuoso? Layout Editing: inv inv layout@ic51
X: 5.54
Y: 2.41
(F) Select: 0
DRD: OFF
dX: 4.62
dY: 6.22
Dist: 7.748
Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre
Sort Edit Help
NIMP
inv
Show Objects
Inst Pin
AV NV AS NS
DIFF
NW
DNW
PWBLK
PIMP
NIMP
VTPL
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
M2_TEXT
1
2
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: leHiDelete()

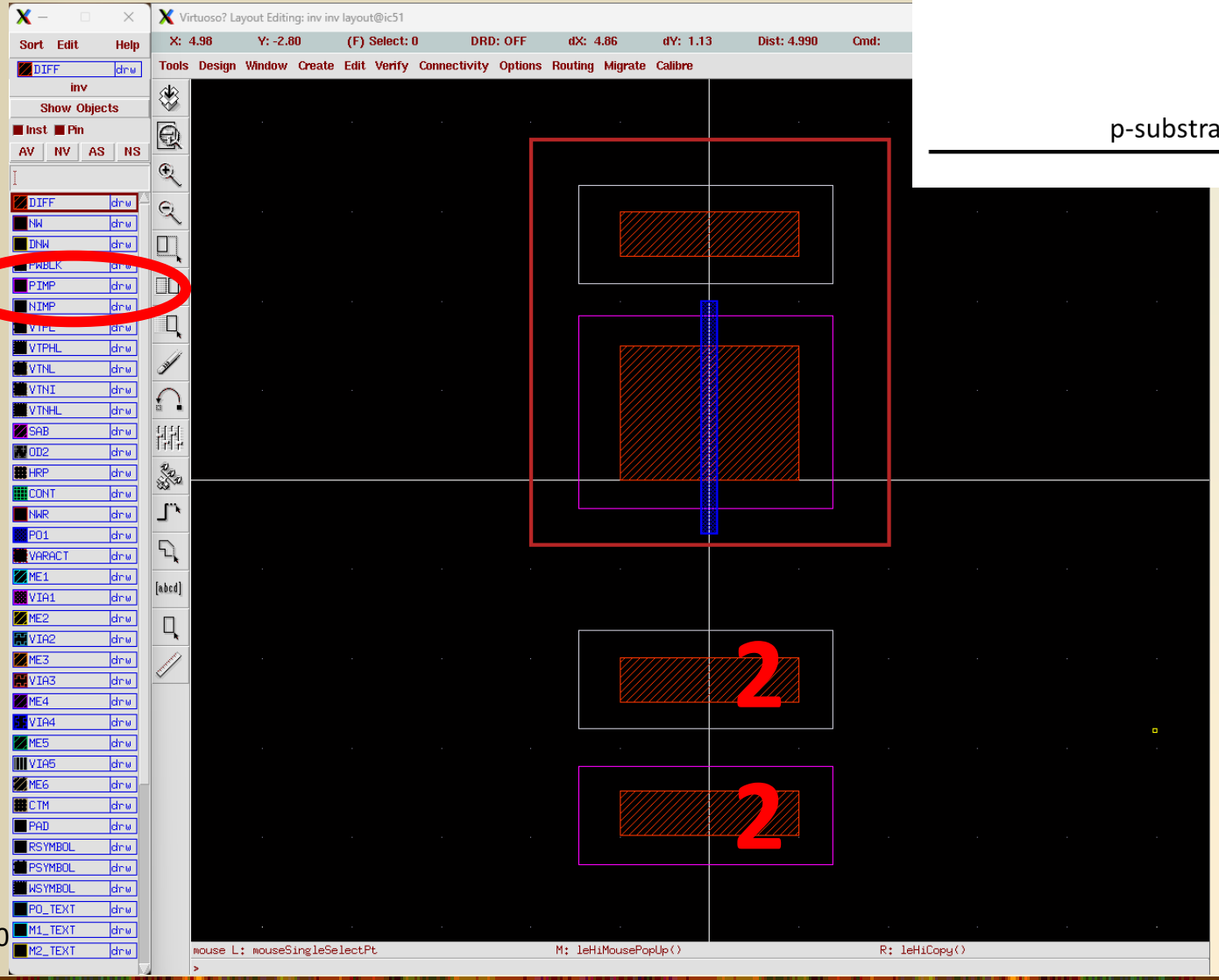
P+ (PIMP)


Gate
Body
Source
Drain
poly
p+
n+
n+
p-substrate

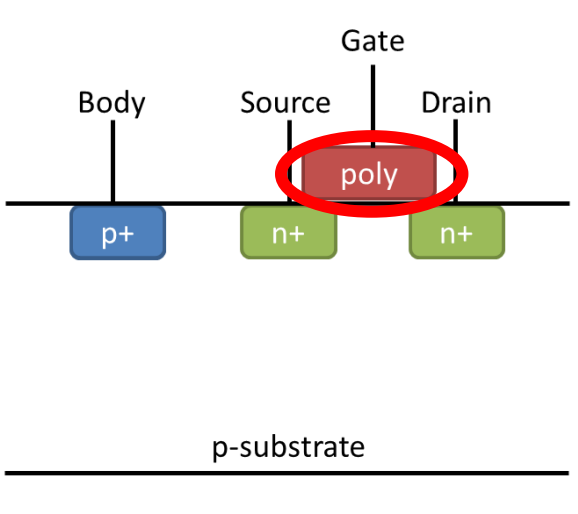

Virtuoso? Layout Editing: inv inv layout@ic51
X: 5.41
Y: -0.67
(F) Select: 0
DRD: OFF
dX: 4.60
dY: 2.85
Dist: 5.411
Cmd:
Sort
Edit
Help
PIMP
inv
Show Objects
Inst
Pin
AV
NV
AS
NS
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Migrate
Calibre
DIFF
NW
DNW
PWBLK
PIMP
NIMP
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
M2_TEXT
1
2
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: leHiEditProp()

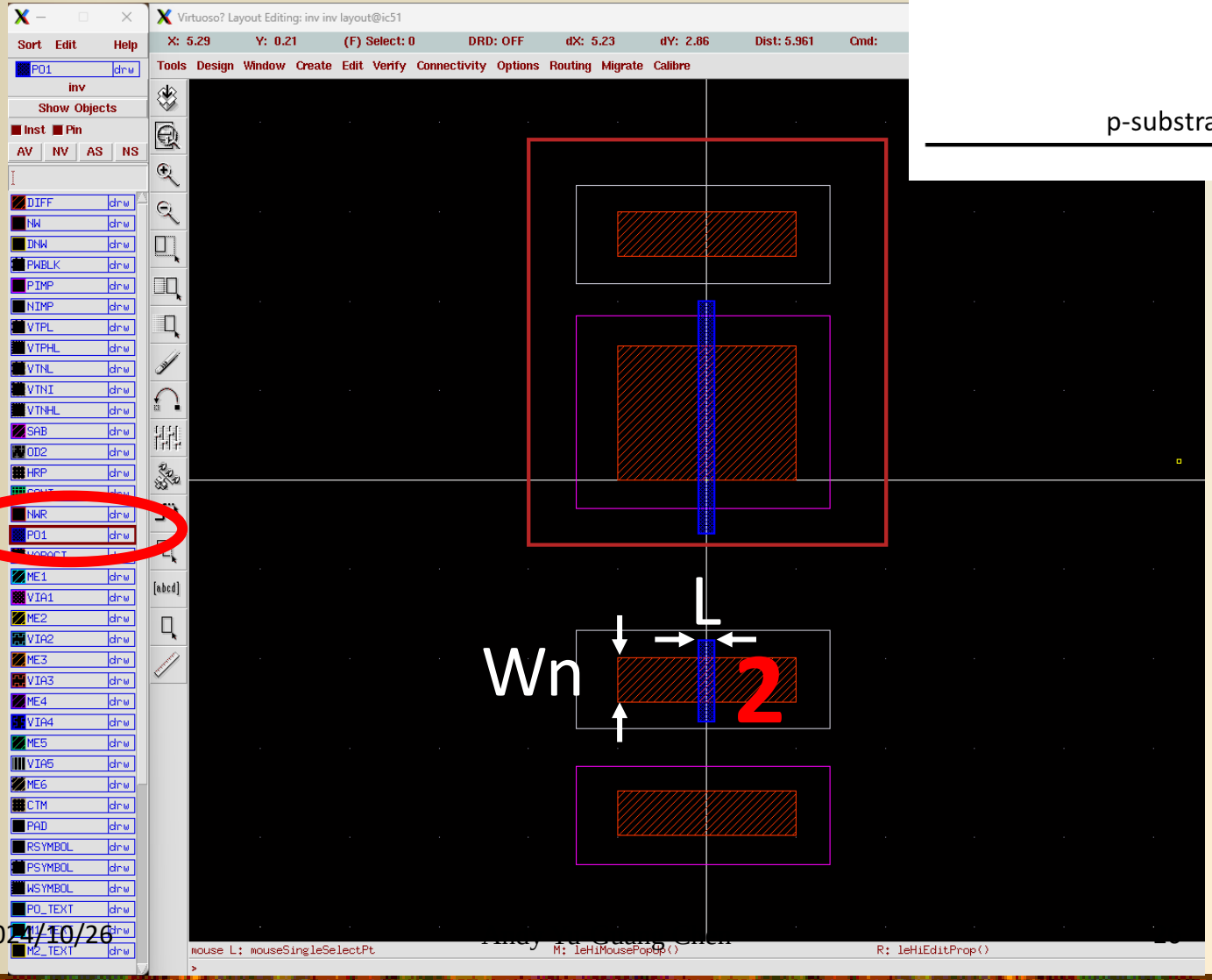
Active (DIFF)


Gate
Body
Source
Drain
poly
p+
n+
n+
p-substrate


Virtuoso? Layout Editing: inv inv layout@ic51
X: 4.98
Y: -2.80
(F) Select: 0
DRD: OFF
dX: 4.86
dY: 1.13
Dist: 4.990
Cmd:
Sort
Edit
Help
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Migrate
Calibre
DIFF
inv
Show Objects
Inst
Pin
AV
NV
AS
NS
NW
DNW
PIMP
NIMP
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
CONT
NWR
PO1
VARACT
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M1_TEXT
M2_TEXT
1
2
2
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: leHiCopy()

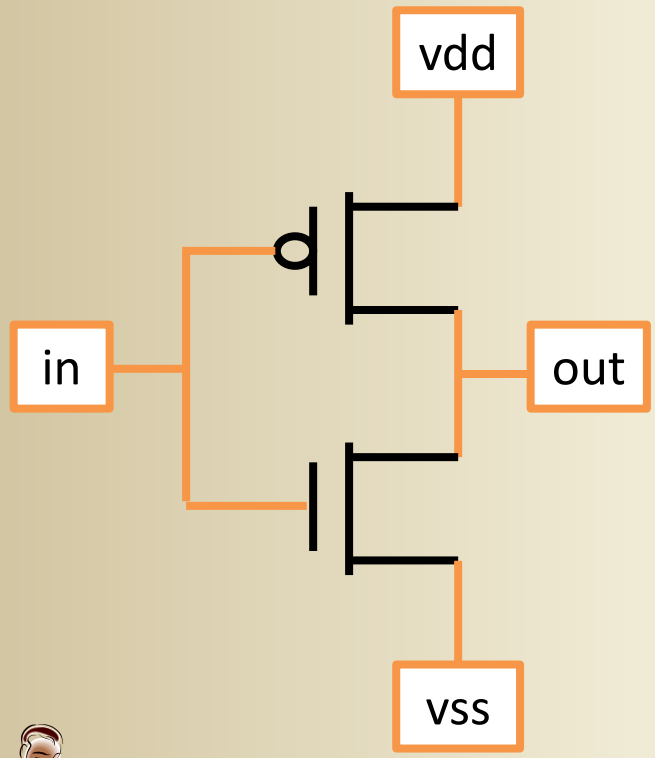
Poly (PO1)

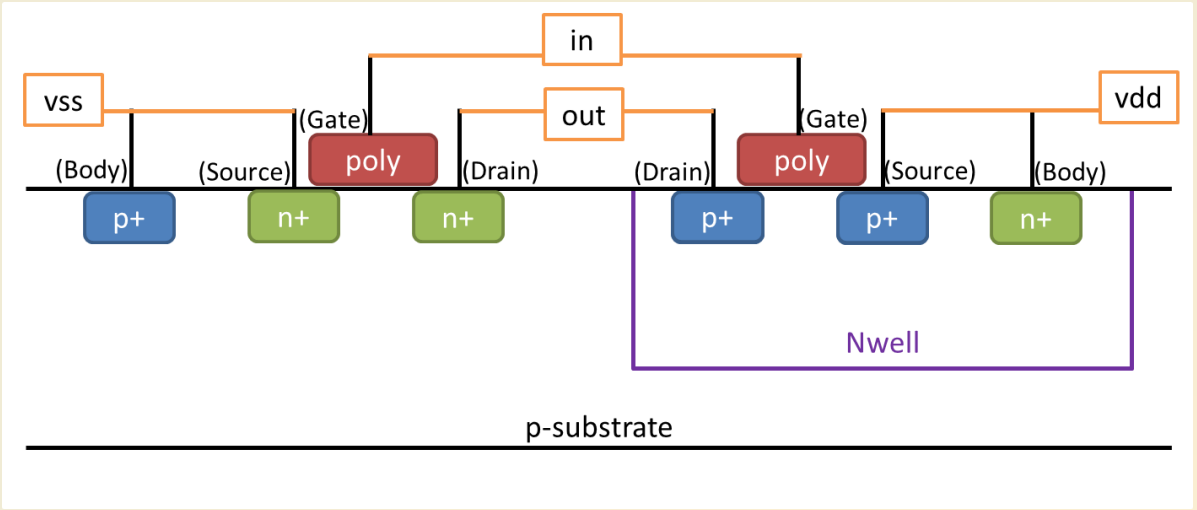

Gate
Body
Source
Drain
poly
p+
n+
n+
p-substrate


Virtuoso? Layout Editing: inv inv layout@ic51
X: 5.29
Y: 0.21
(F) Select: 0
DRD: OFF
dX: 5.23
dY: 2.86
Dist: 5.961
Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre
Sort Edit Help
PO1
inv
Show Objects
Inst Pin
AV NV AS NS
DIFF
NW
DNW
PWBLK
PIMP
NIMP
VTPL
VTPHL
VTNL
VTNI
VTNHL
SAB
OD2
HRP
NWR
PO1
ME1
VIA1
ME2
VIA2
ME3
VIA3
ME4
VIA4
ME5
VIA5
ME6
CTM
PAD
RSYMBOL
PSYMBOL
WSYMBOL
PO_TEXT
M2_TEXT
1
L
Wn
2
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: leHiEditProp()

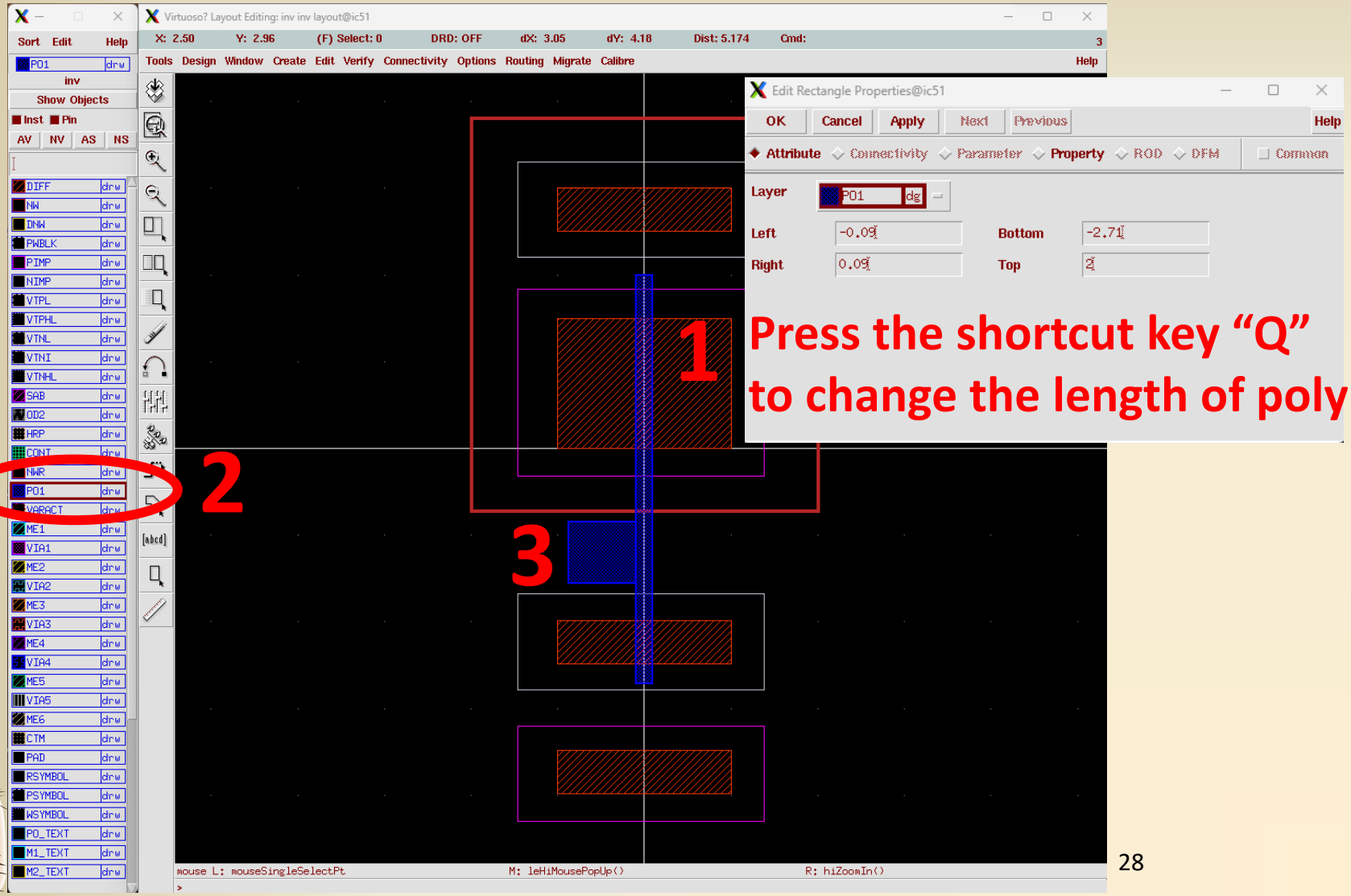
Inverter

- Connect PMOS and NMOS to inputs

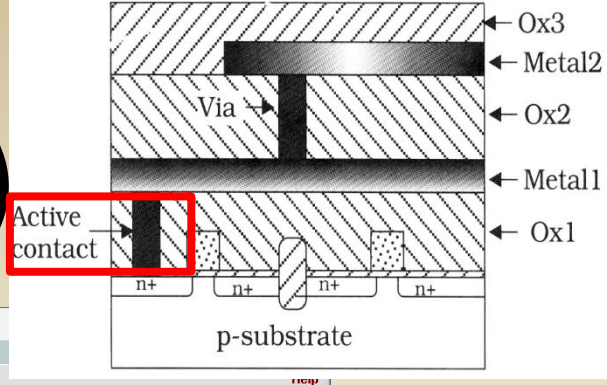


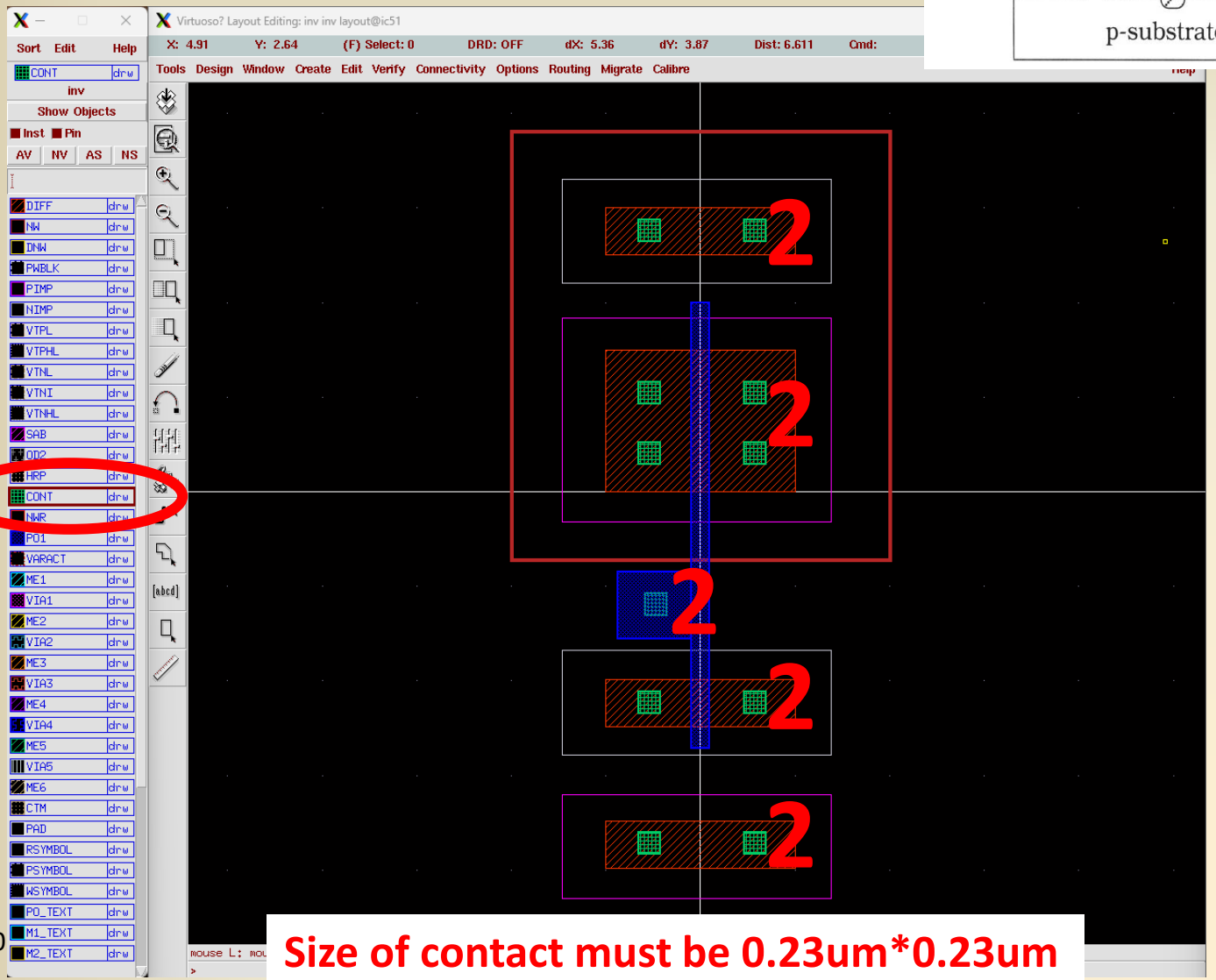


Poly (PO1)


Virtuoso? Layout Editing: inv inv layout@ic51
Edit Rectangle Properties@ic51
OK
Cancel
Apply
Next
Previous
Help
Attribute
Connectivity
Parameter
Property
ROD
DFM
Common
Layer
PO1
Left
-0.09
Bottom
-2.71
Right
0.09
Top
2
Press the shortcut key “Q”
to change the length of poly
1
2
3

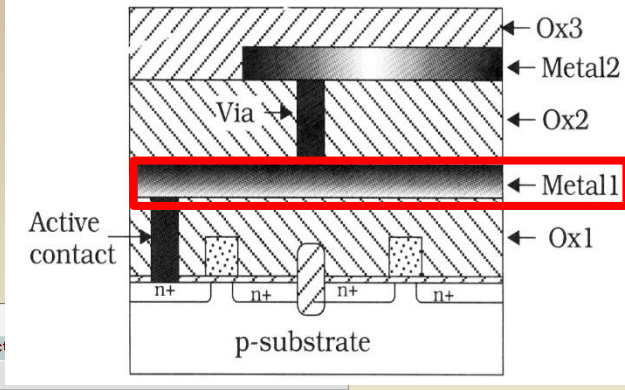
Contact (CONT)

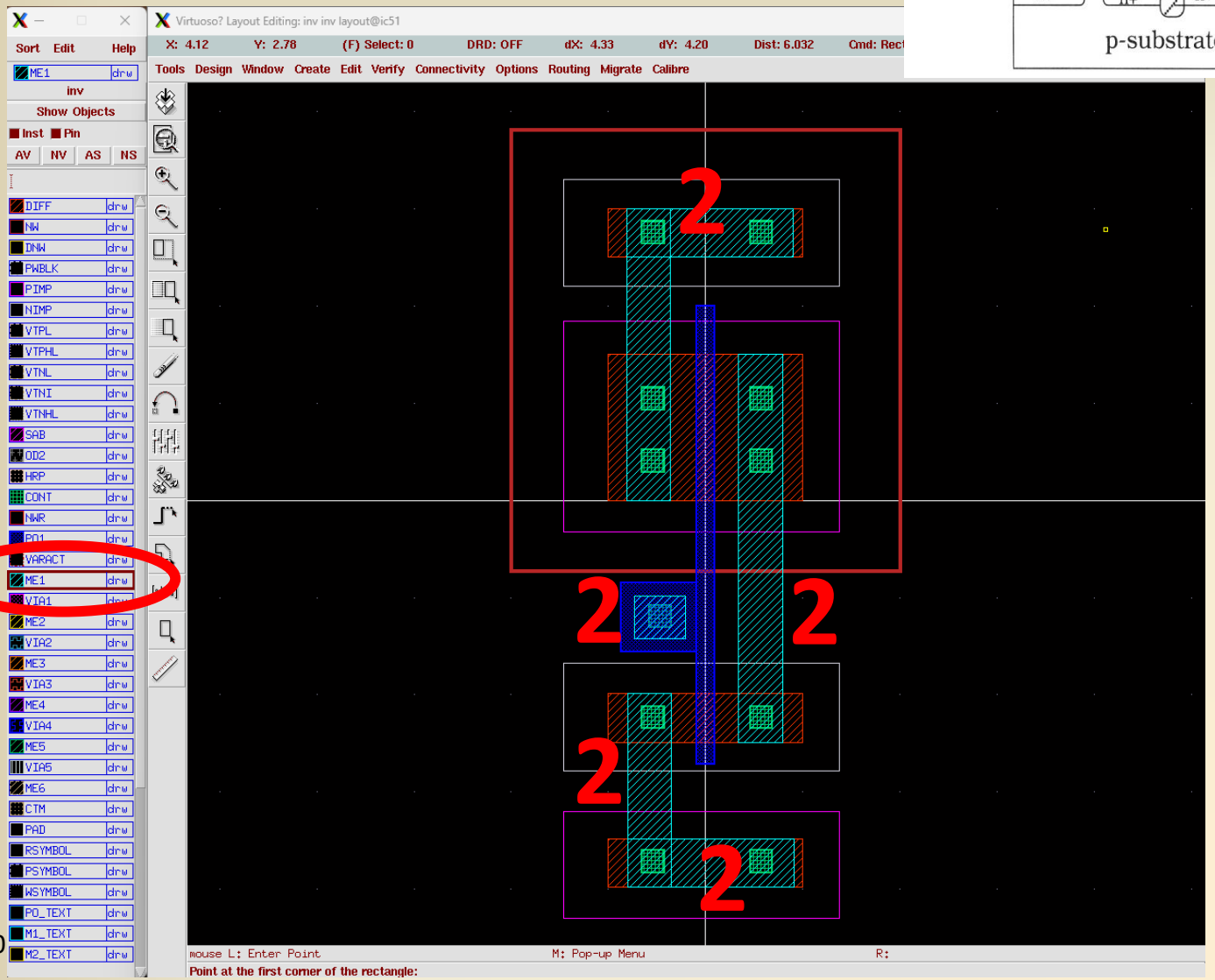




Size of contact must be 0.23um*0.23um

Metal1 (ME1)

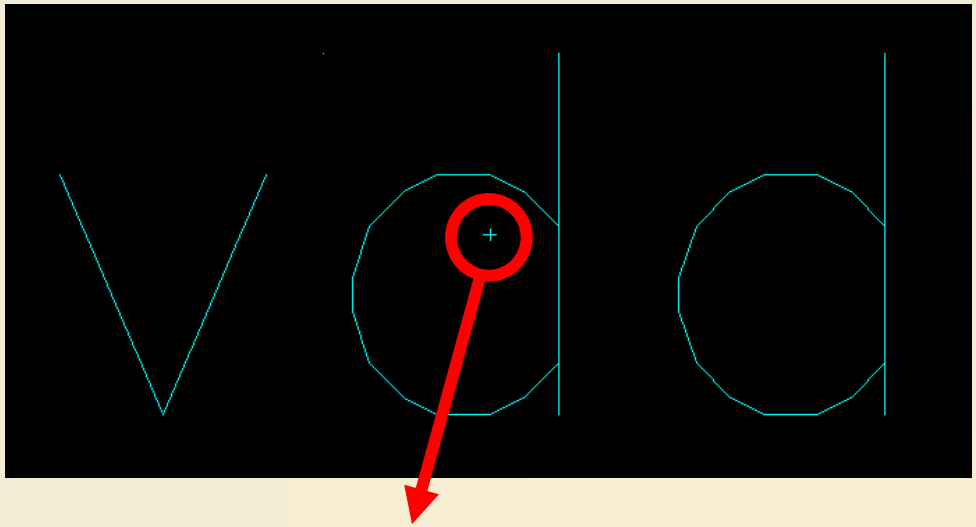

Ox3
Metal2
Via
Ox2
Metal1
Active contact
Ox1
n+
n+
n+
n+
p-substrate


Virtuoso? Layout Editing: inv inv layout@ic51
X: 4.12
Y: 2.78
(F) Select: 0
DRD: OFF
dX: 4.33
dY: 4.20
Dist: 6.032
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre
Sort Edit Help
ME1 drw
inv
Show Objects
Inst Pin
AV NV AS NS
DIFF drw
NW drw
DNW drw
PWBLK drw
PIMP drw
NIMP drw
VTPL drw
VTPHL drw
VTNL drw
VTNI drw
VTNHL drw
SAB drw
OD2 drw
HRP drw
CONT drw
NWR drw
PO1 drw
VARACT drw
ME1 drw
VIA1 drw
ME2 drw
VIA2 drw
ME3 drw
VIA3 drw
ME4 drw
VIA4 drw
ME5 drw
VIA5 drw
ME6 drw
CTM drw
PAD drw
RSYMBOL drw
PSYMBOL drw
WSYMBOL drw
PO_TEXT drw
M1_TEXT drw
M2_TEXT drw
1
2
2
2
2
2
mouse L: Enter Point
M: Pop-up Menu
R:
Point at the first corner of the rectangle:

Label

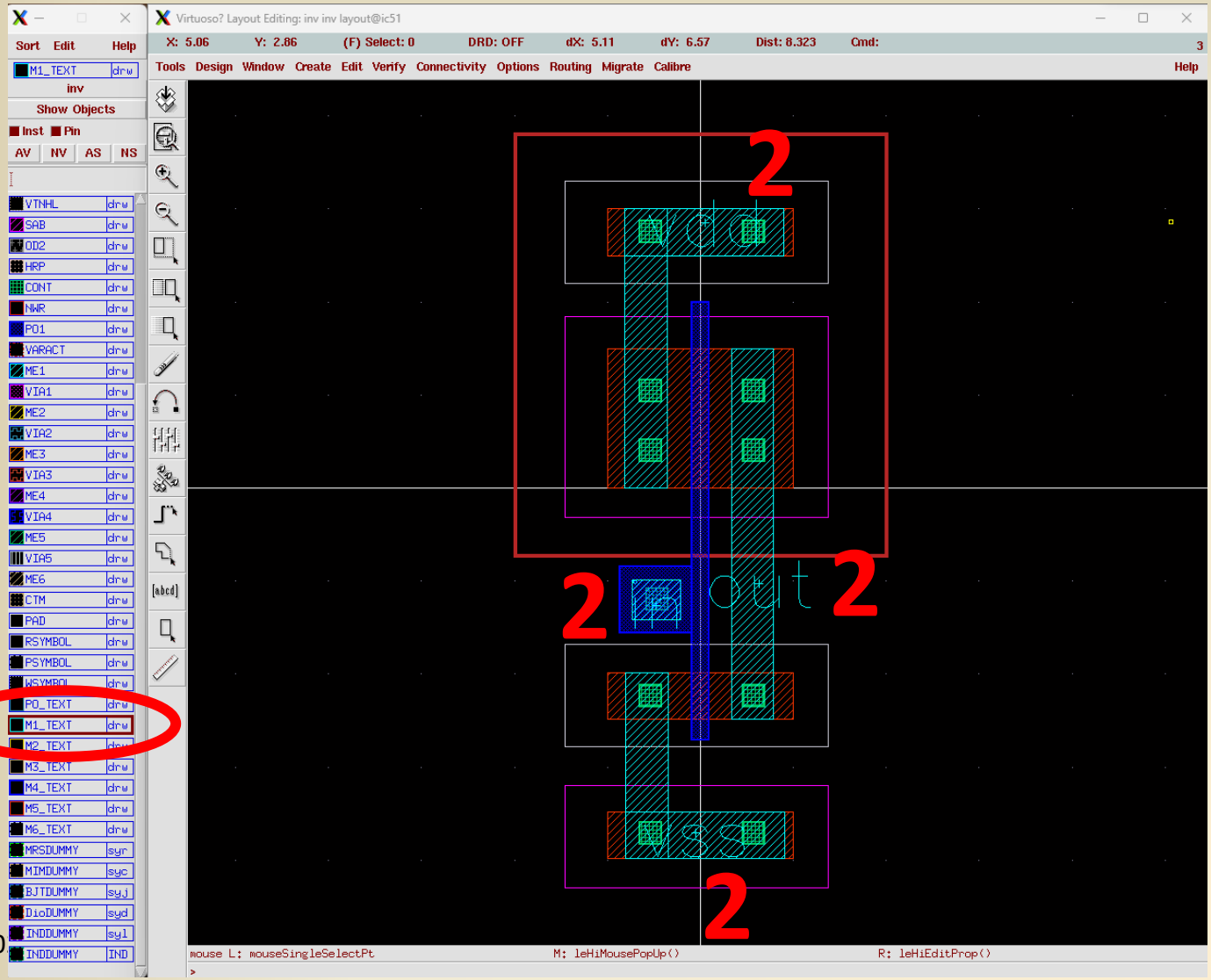
1. Create label

2. Place the label on the metal 1



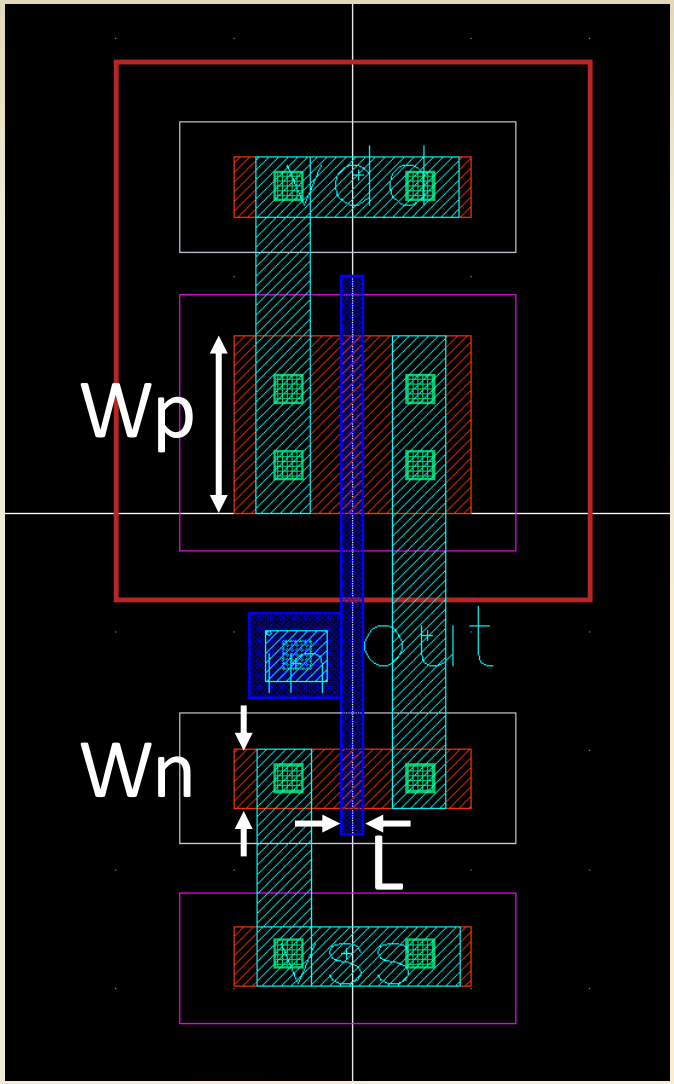
The center of label must be on the metal

Label


Virtuoso? Layout Editing: inv inv layout@ic51
X: 5.06
Y: 2.86
(F) Select: 0
DRD: OFF
dX: 5.11
dY: 6.57
Dist: 8.323
Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre Help
Sort Edit Help
M1_TEXT drw
inv
Show Objects
Inst Pin
AV NV AS NS
VTNHL drw
SAB drw
OD2 drw
HRP drw
CONT drw
NWR drw
PO1 drw
VARACT drw
ME1 drw
VIA1 drw
ME2 drw
VIA2 drw
ME3 drw
VIA3 drw
ME4 drw
VIA4 drw
ME5 drw
VIA5 drw
ME6 drw
CTM drw
PAD drw
RSYMBOL drw
PSYMBOL drw
WSYMBOL drw
PO_TEXT drw
M1_TEXT drw
M2_TEXT drw
M3_TEXT drw
M4_TEXT drw
M5_TEXT drw
M6_TEXT drw
MRSDUMMY syr
MIMDUMMY syc
BJTDUMMY syj
DioDUMMY syd
INDDUMMY syl
INDDUMMY IND
2
2
out
2
2
1
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R: leHiEditProp()

Inverter

- Overall layout



Outline

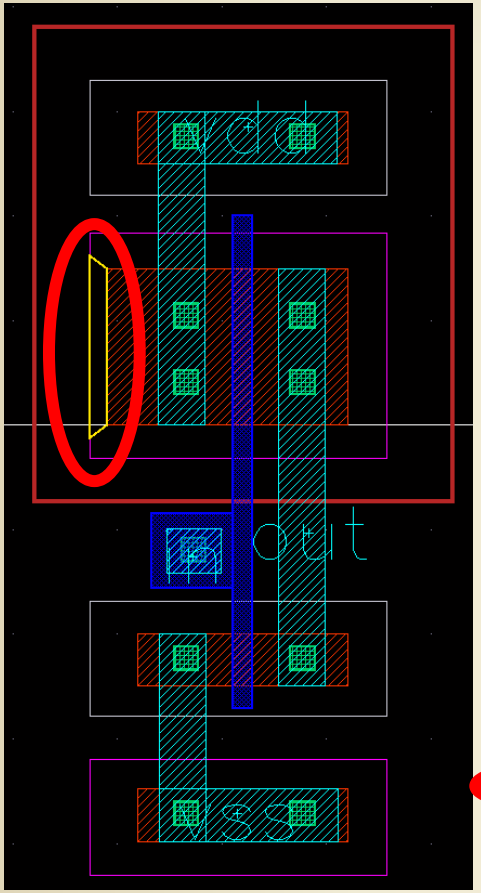
- Virtuoso
- User Interface
- Shortcut Key
- Inverter
- **Design Rule Check**
- Layout Versus Schematic
- Reference

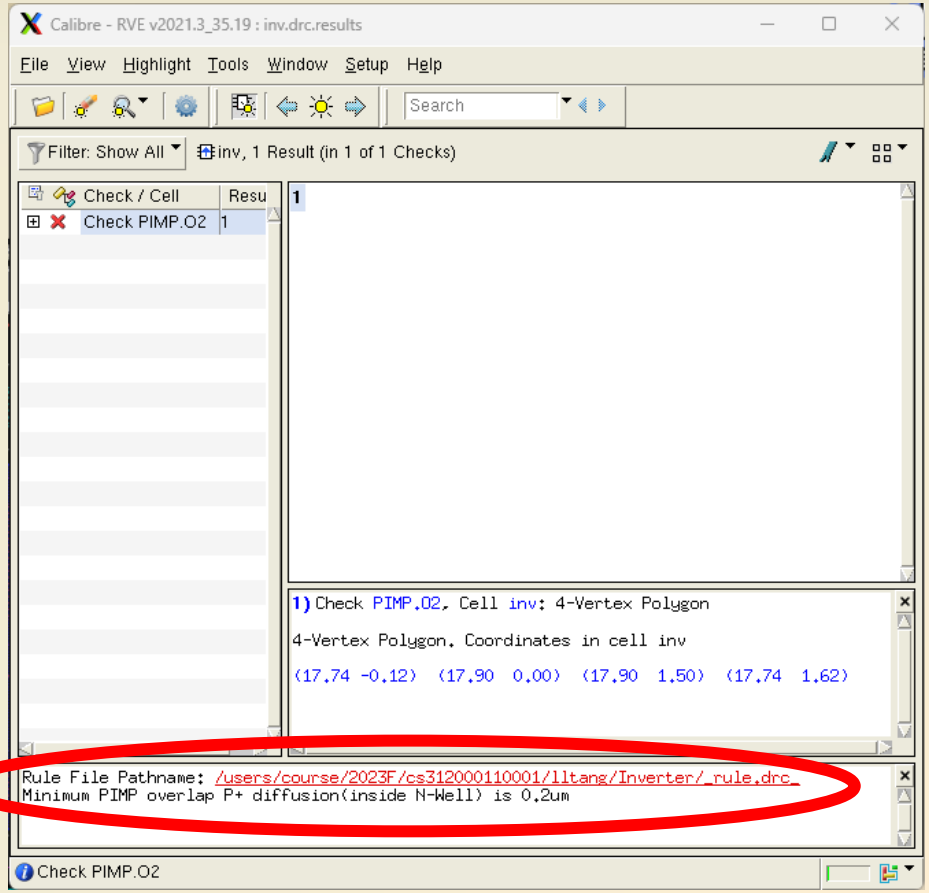
Design Rule Check

- Design Rule Check (DRC)
- Make sure no resource violate the design rule
- Examples of DRC error
  - The space of two resource
  - Minimum metal overlap
  - Minimum area of resource

DRC error

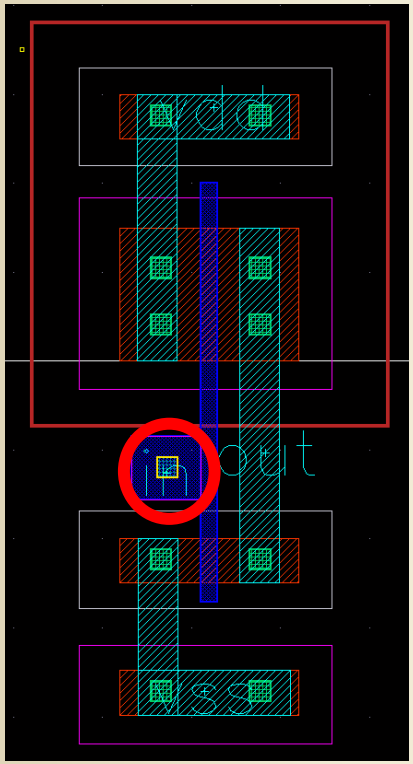
- The space of two resource

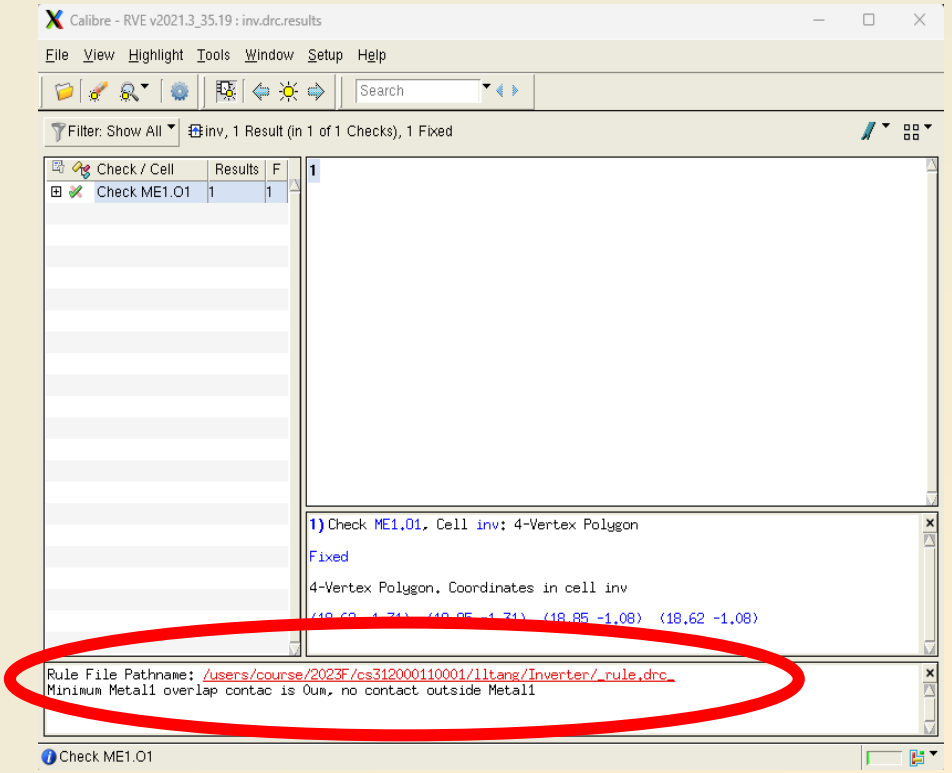




DRC error

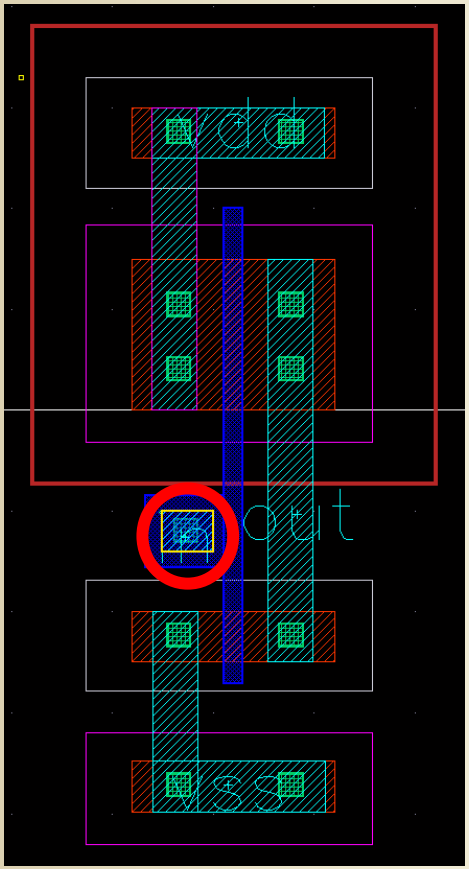
- Minimum metal overlap
  - Miss metal1

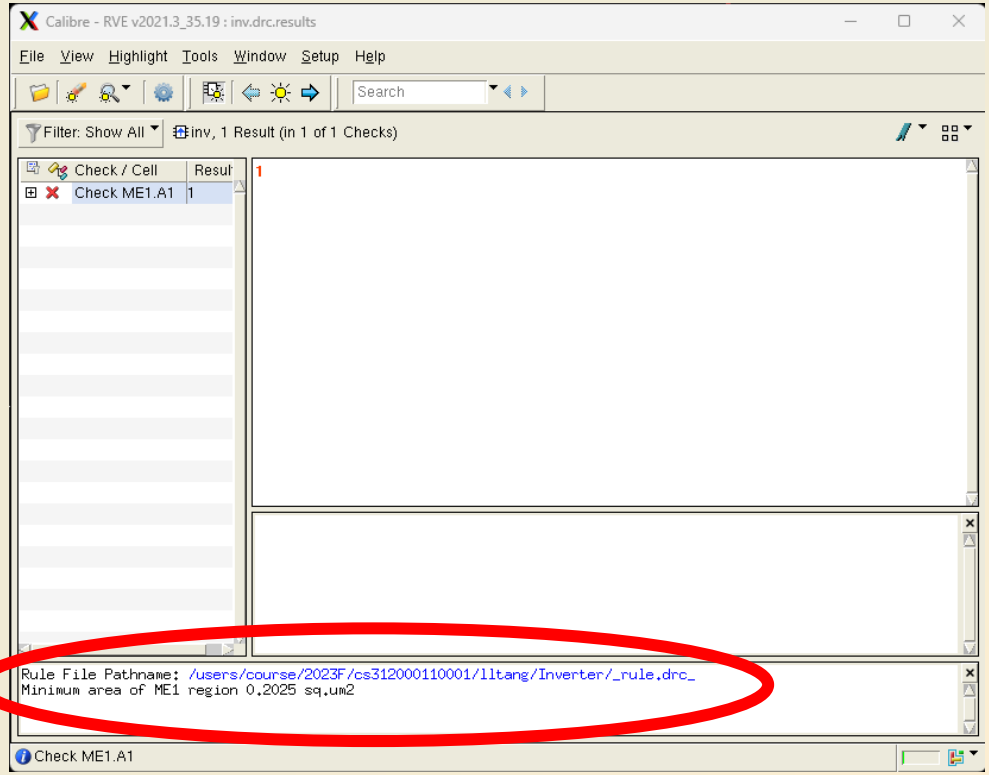




DRC error

- Minimum area of resource





Outline

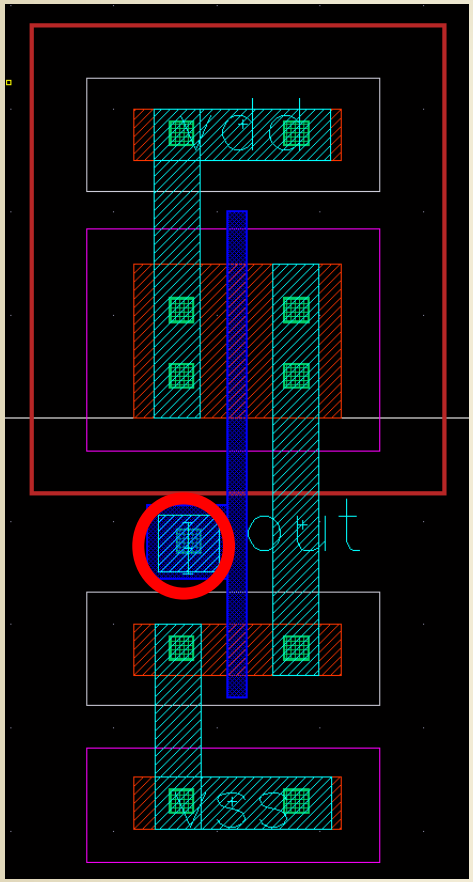
- Virtuoso
- User Interface
- Shortcut Key
- Inverter
- Design Rule Check
- **Layout Versus Schematic**
- Reference

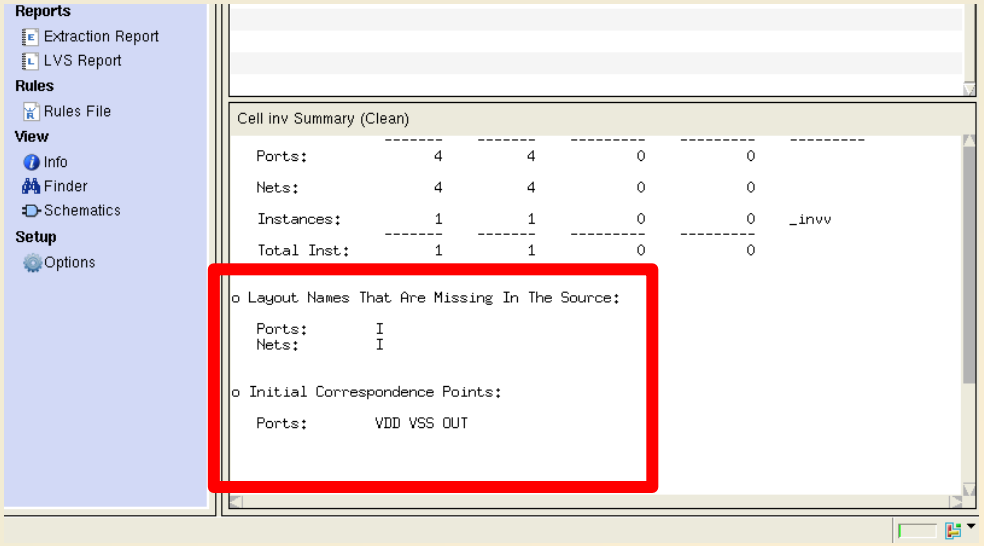
Layout Versus Schematic

- Layout Versus Schematic (LVS)
- Compare the layout with the schematic file
- Check the functionality and pins of layout
- Examples of LVS errors
  - Different pin name
  - Missing port
  - Size difference

Layout Versus Schematic

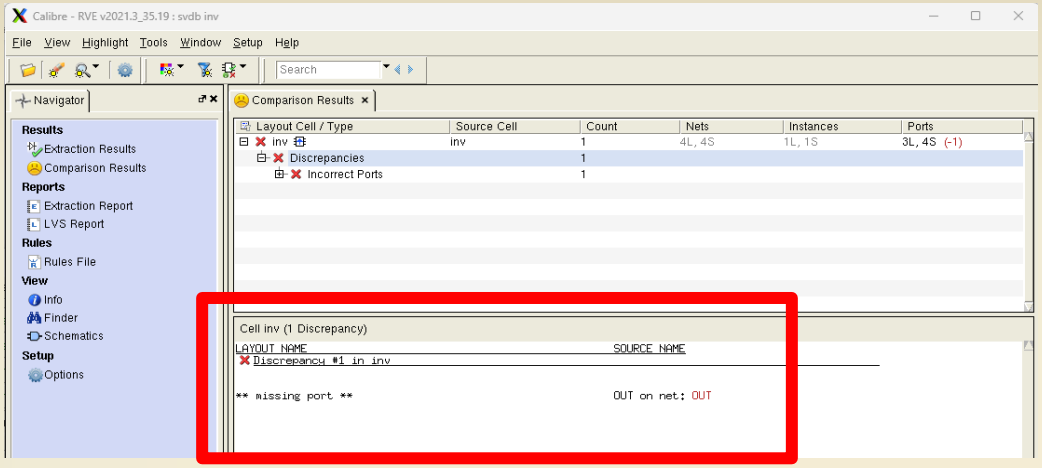
- Different pin name

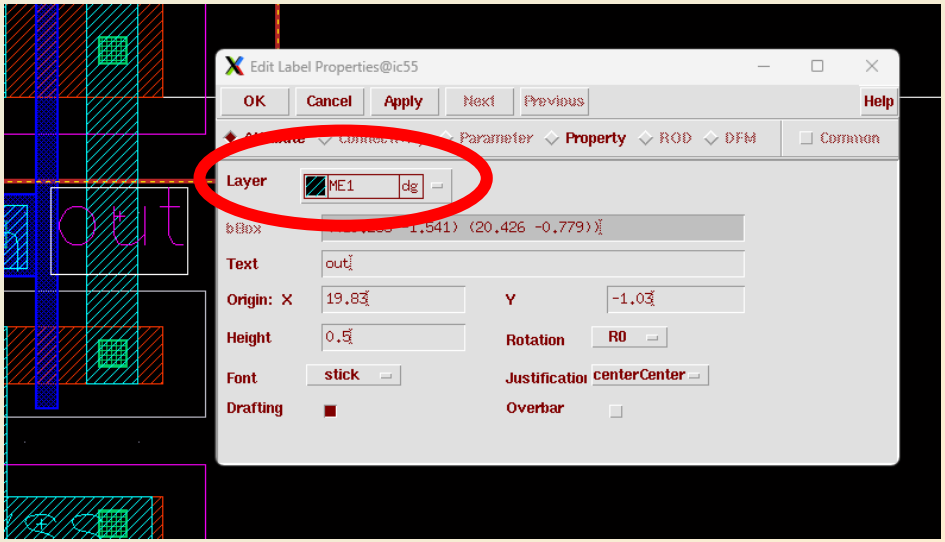




Layout Versus Schematic

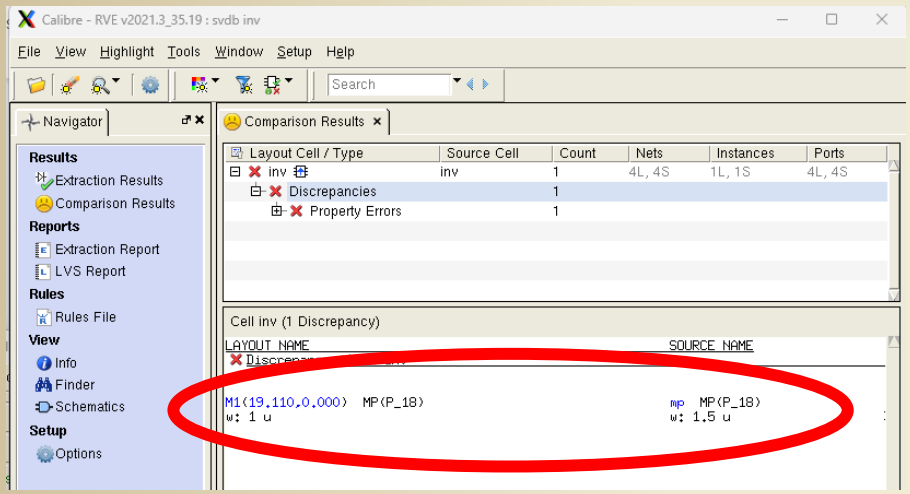
- Missing port

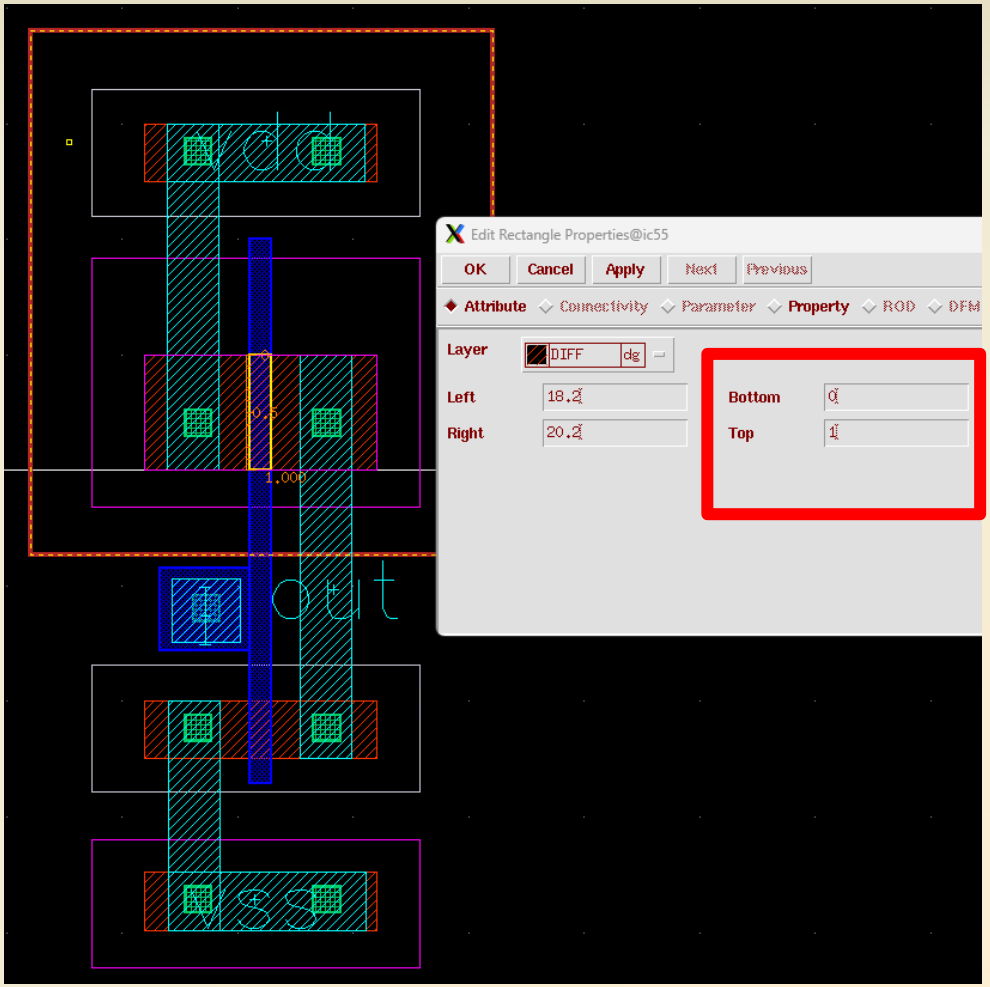




Layout Versus Schematic

- Size difference





Outline

- Virtuoso
- User Interface
- Shortcut Key
- Inverter
- Design Rule Check
- Layout Versus Schematic
- **Reference**

Reference

[1] Virtuoso layout suite datasheet. Available: https://www.cadence.com/en_US/home/resources/datasheets/virtuoso-layout-suite-ds.html

[2] Cadence ICFB Hot Keys. Available:

https://inst.eecs.berkeley.edu/~ee247b/sp19/homework/CadenceHotkeys.pdf