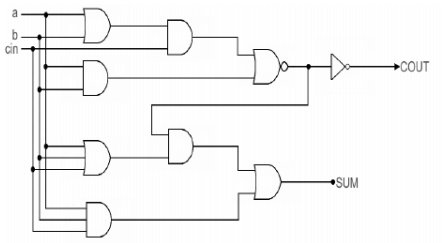
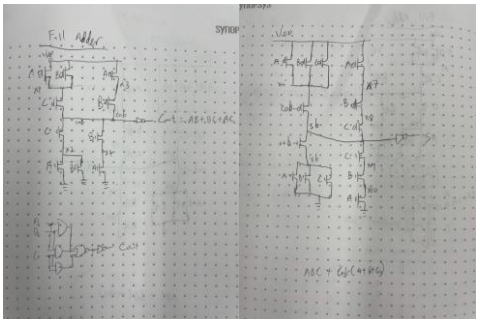
黃偉祥 X1136010

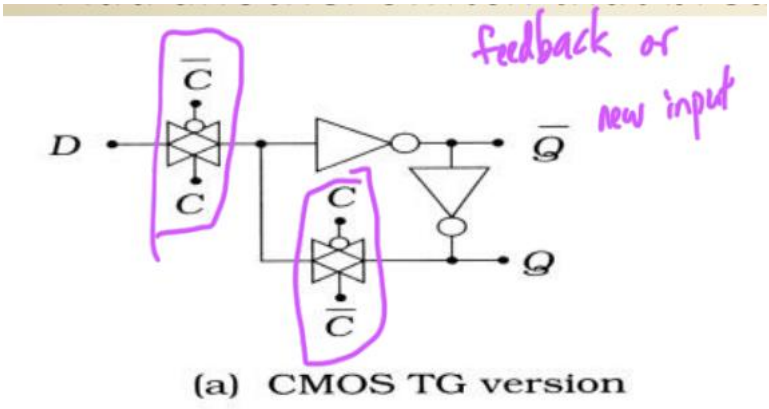
Full Adder





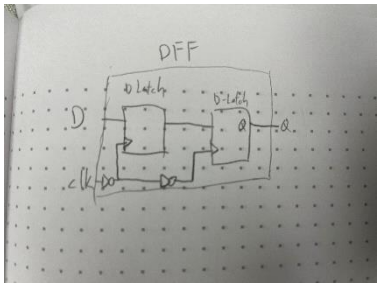
- I use the online Full adder version to design my full adder.
- For Multiple bits full adder, I just connect them together.

D Latch



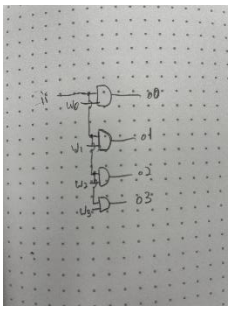
- I use ppt version of D Latch to design my DLatch_TG
- I use D-latch to store Weights.

D Flip Flop



- I use 2 D-latch to build my positive edge DFF

IdotW



- I just and ii with all w0, w1, w2, w3 separately.
- This use for every I * W in all column and row.

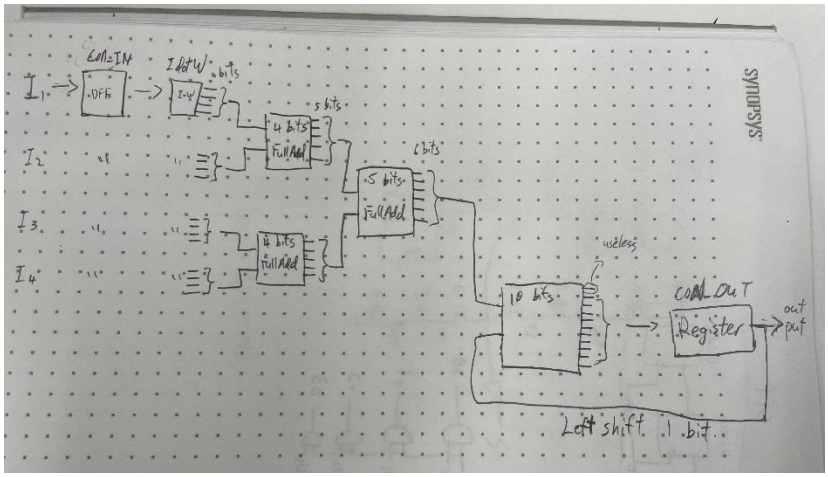
OUT_NOW

- I use 1 DFF to keep the previous IN_VAL, then check if previous IN_VAL is 1 and current IN_VAL is 0 ➔ Fall occurs.
- When Fall occurs then OUT_VAL need to be 1 for a cycle in the next cycle, so I use another DFF to output the OUT_VAL.

CON_IN & CON_OUT

- I use DFF to done this 2, the different is only CON_IN use IN_VAL to check while CON_OUT use RST to check.
- And CON_IN use 4 DFF while CON_OUT use 10 DFF.

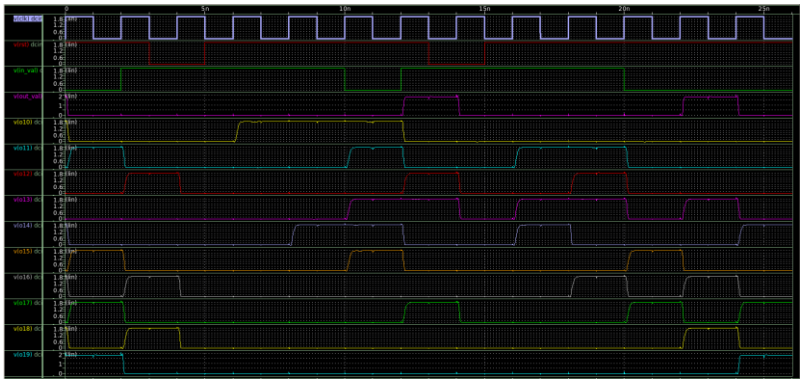
Design



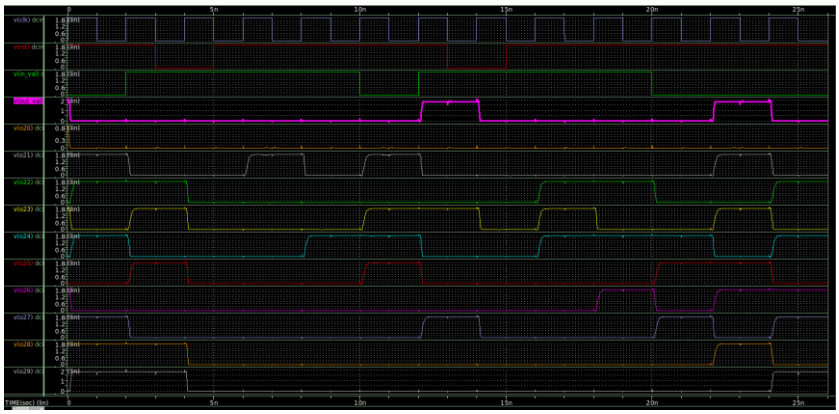
- I use all subcircuit that I show in above and connect them just like the figure above.

Waveform

1. Column 1 wave form



2. Column 2 wave form



Delay and Power

```
****** transient analysis tnom=  25.000 temp=  30.000 ******
td= 624.0792p  targ=   4.8206n   trig=   4.1965n
pwr=   1.6866m  from=   0.              to=  26.0000n

         ***** job concluded
```

1. Delay = 624.0792 p
2. Power= 1.6866 m

Transistors

```
******  Circuit Statistics  ******
# nodes       =    6232 # elements   =    2534
# resistors   =       0 # capacitors =       0 # inductors   =       0
# mutual_inds =       0 # vccs       =       0 # vcvs        =       0
# cccs        =       0 # ccvs       =       0 # volt_srcs   =       8
# curr_srcs   =       0 # diodes     =       0 # bjts        =       0
# jfets       =       0 # mosfets    =    2526 # U elements  =       0
# T elements  =       0 # W elements =       0 # B elements  =       0
# S elements  =       0 # P elements =       0 # va device   =       0
# vector_srcs =       0 # N elements =       0
```

- Total : 2526 mosfets

Bonus

```
******  Circuit Statistics  ******
# nodes       =  428942 # elements   =  173192
# resistors   =       0 # capacitors =       0 # inductors   =       0
# mutual_inds =       0 # vccs       =       0 # vcvs        =       0
# cccs        =       0 # ccvs       =       0 # volt_srcs   =       8
# curr_srcs   =       0 # diodes     =       0 # bjts        =       0
# jfets       =       0 # mosfets    =  173184 # U elements  =       0
# T elements  =       0 # W elements =       0 # B elements  =       0
# S elements  =       0 # P elements =       0 # va device   =       0
# vector_srcs =       0 # N elements =       0
```

- Total 173184 Mosfets

- Design

DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2
DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2
DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2
DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2
DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2
DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2
DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2
DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2	DCIM4_2

- I use the basic DCIM4_2 to build a DCIM32_2
  - DCIM4_2 is the DCIM in basic part
  - DCIM32_2 have 32 rows and 2 columns
- Then I use 8 * DCIM32_2 to build DCIM
  - This DCIM will take Input I1~I32, and output O10~O169
    - Total 32 inputs
    - Total 160 outputs
      - Each DCIM32_2 will produce 20 outputs * 8 DCIM32_2
- Weights is a bit different with basic, which can just for all column with same weight, so I set weights inside DCIM circuit
  - Xw1 ~ Xw16
- Then pass it to DCIM32_2 separately and initial it using .ic V(Xdcim.Xwx.wx)=xv

Hardness

1. The Full adder delay of my design, this gives me so much trouble when checking problem and debugging.
   甲、Thanks my friend helping me to get another kind of Full adder design and then everything done!
2. First I thought Latch and Flip-flop is the same thing, but then when TA time I knew that we need to use flip-flop instead of latch…
   甲、TQ TA, I will check the document properly next time…
3. I need more TA time and my email always get into dustbin…