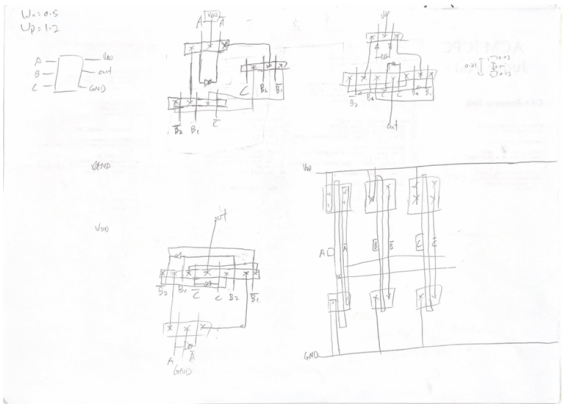
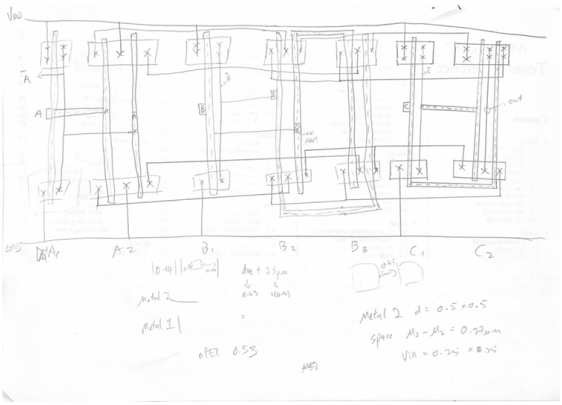
X1136010 黃偉祥

Basic & Bonus

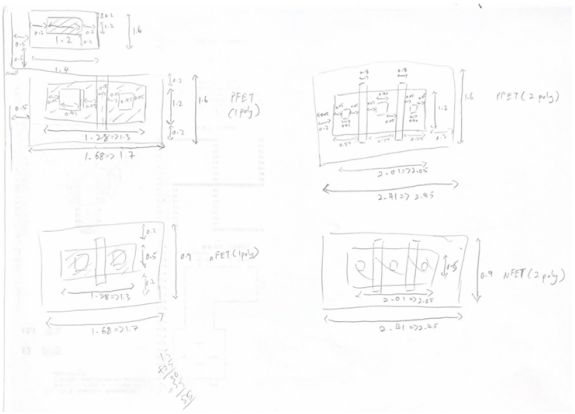
Basic



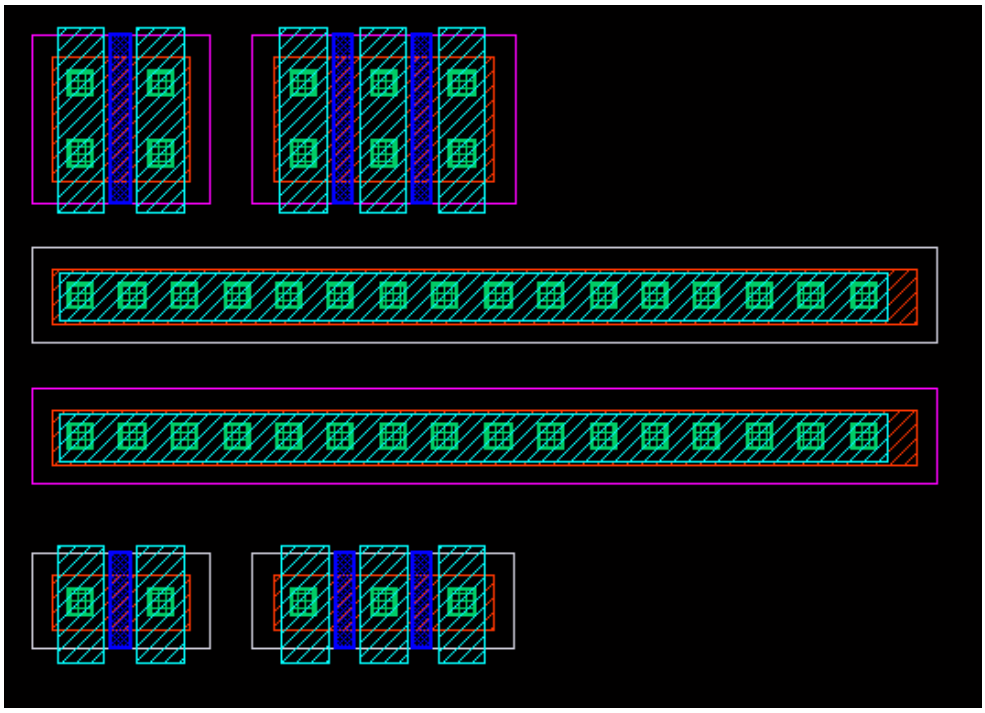
1. First I draw a very simply layout from the design in document.



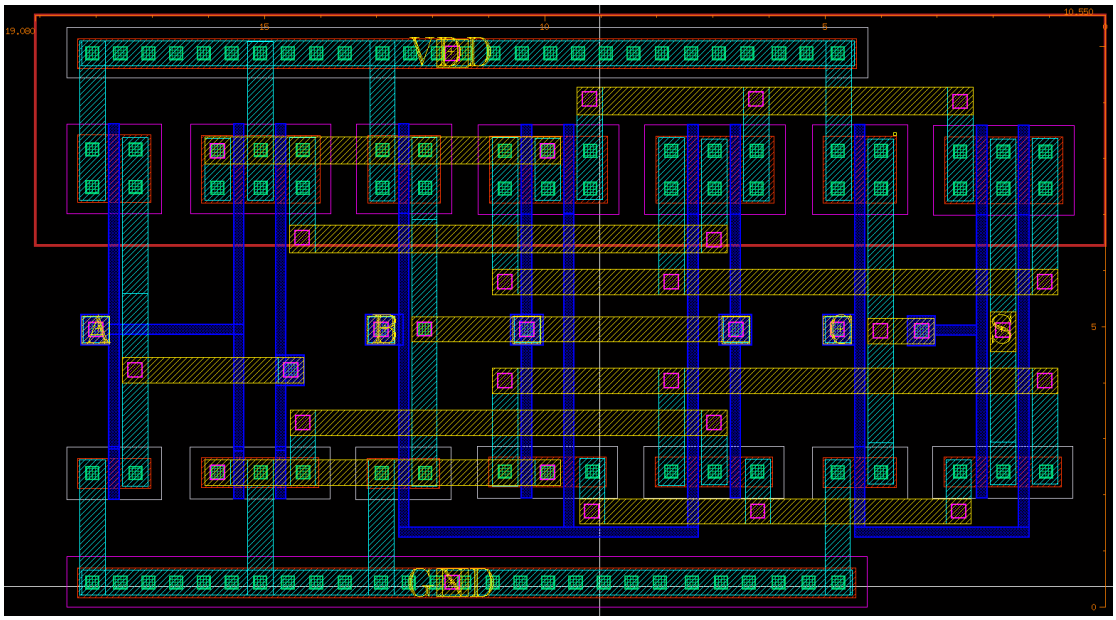
2. Then I convert into the more similar layout with using virtuoso.



3. From the second graph I knew that I only need 2 sizes of pFET and nFET to done the layout, so I calculate these 2 sizes of FETs.

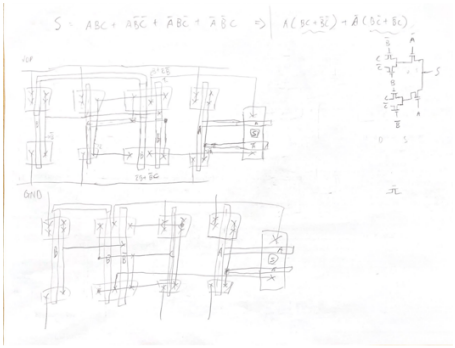


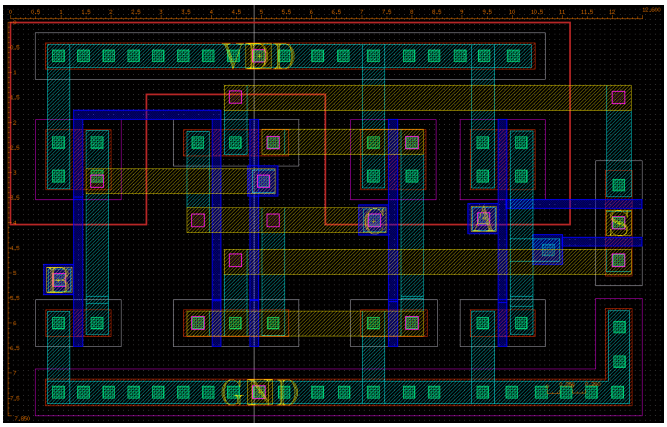
4. After that I start to draw these needed FETs, VDD and GND with virtuoso.



5. After that I use all the FETs in step 4 and combined the graph in step 2, and then everything done and start to run DRC, LVS and PEX and do the post simulation and check the wave of it.

Bonus

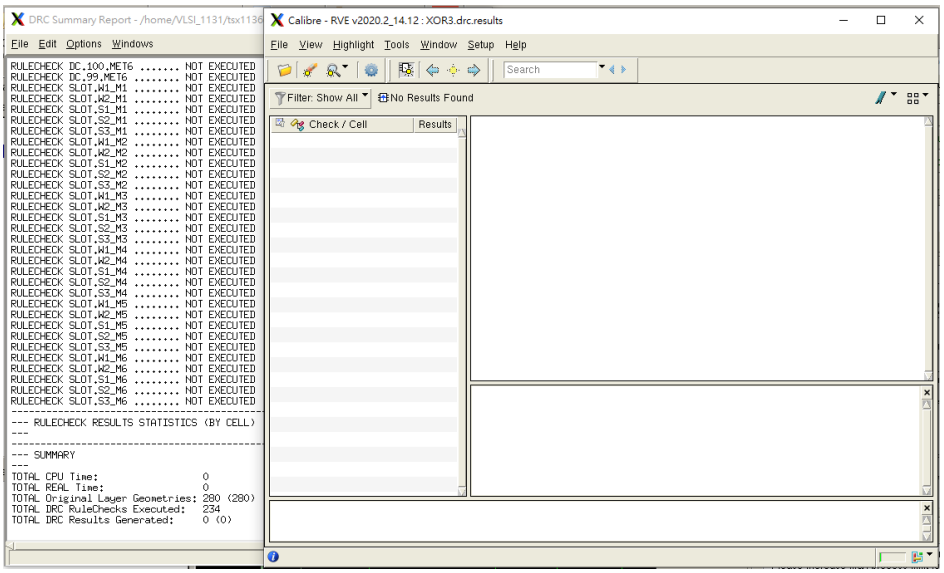




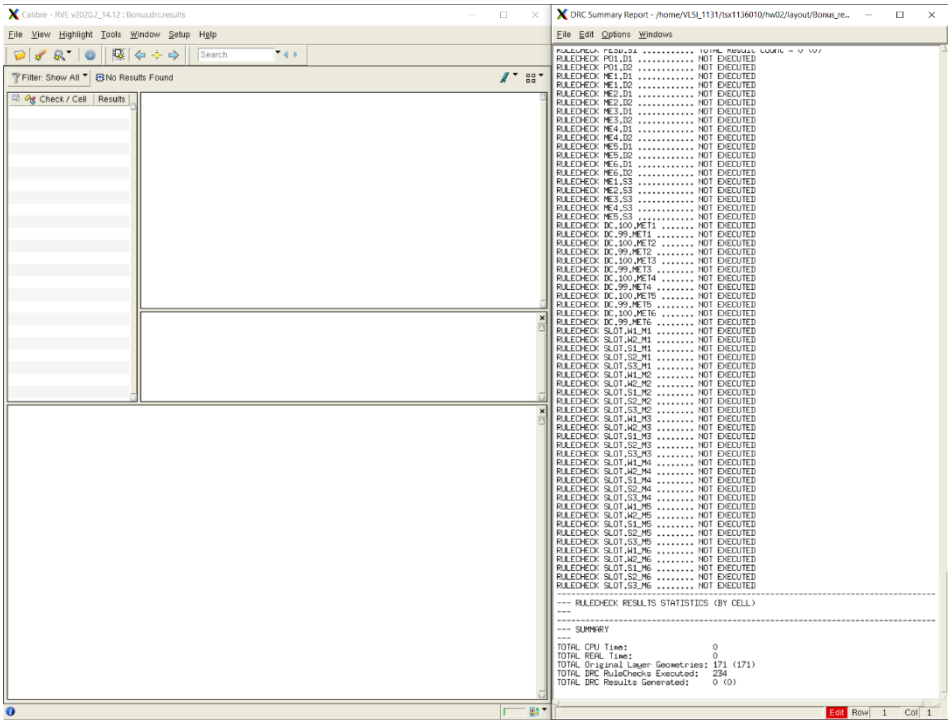
- Same method I used in basic part

DRC summary report

Basic

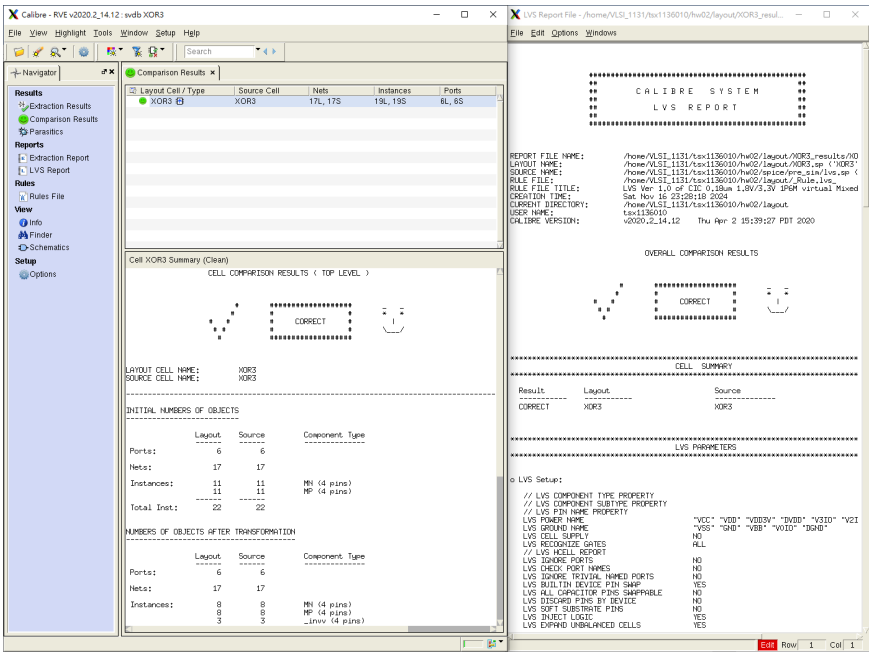


Bonus

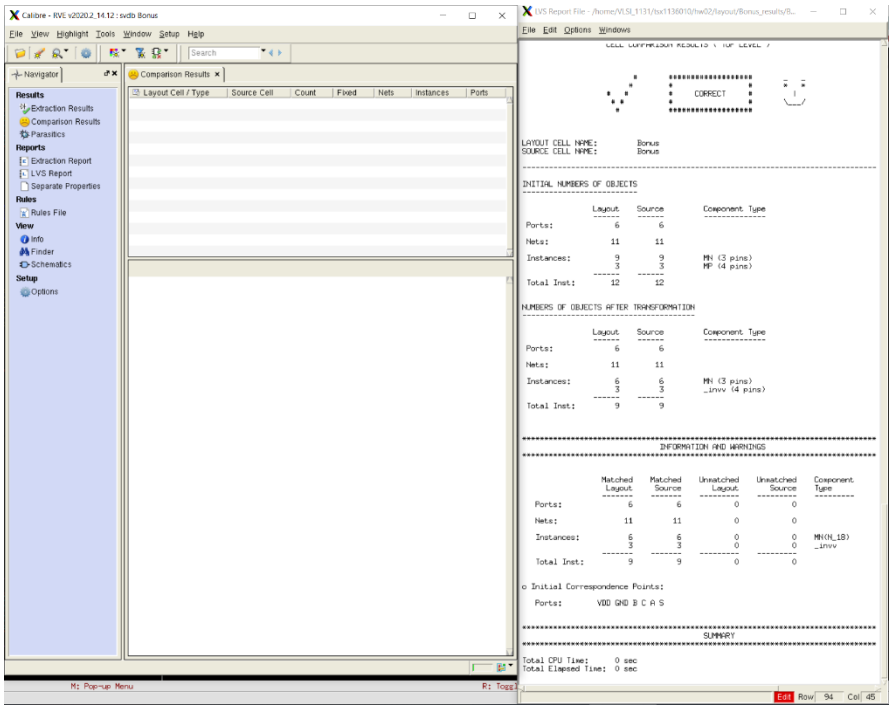


LVS report

Basic

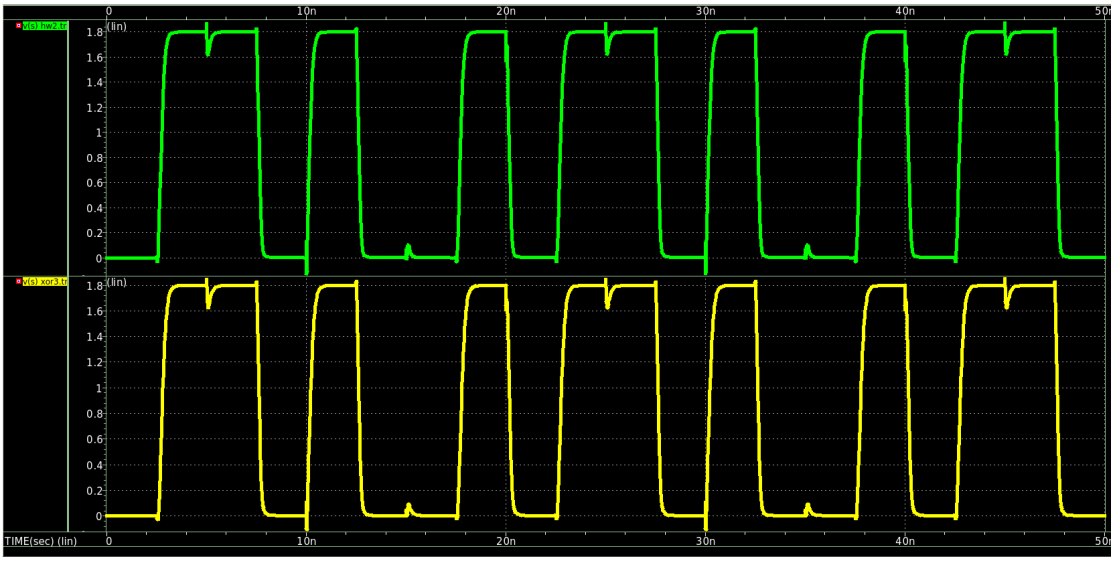


Bonus



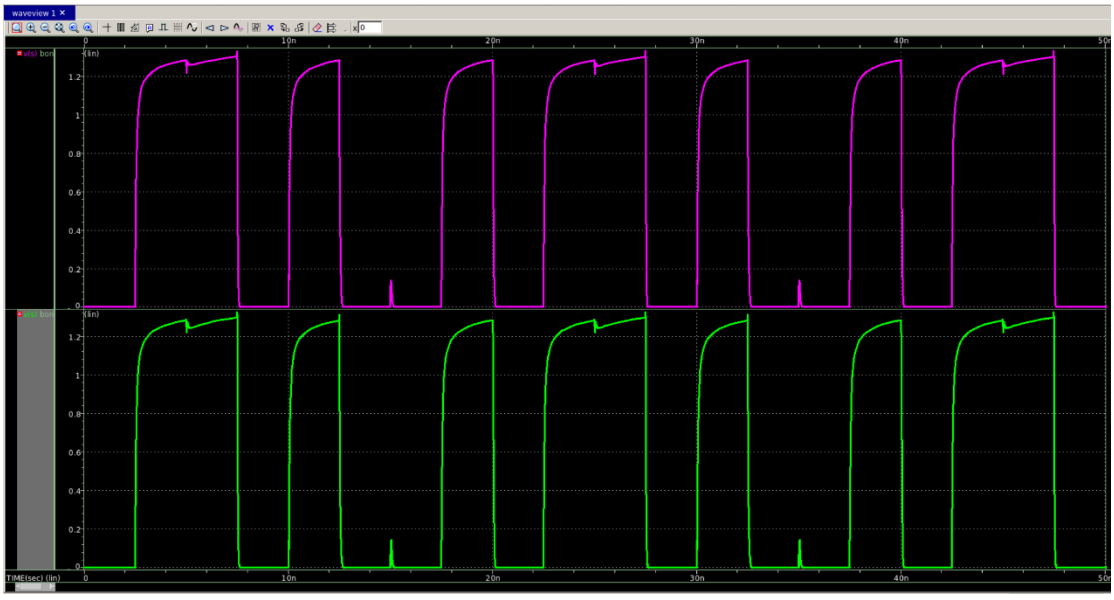
Pre-sim and Post-sim waveforms

Basic



- upper wave is pre-sim wave, and the below one is the post-sim wave

Bonus



- upper wave is pre-sim wave, and the below one is the post-sim wave

Post simulation result

Basic

```
******
**x1136010_hw2_xor**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power= 2.7719e-05  from= 0.0000e+00     to= 5.0000e-08
delay1_xor= 1.8770e-10  targ= 2.0203e-08   trig= 2.0015e-08
delay2_xor= 2.9904e-10  targ= 2.8040e-09   trig= 2.5050e-09

         ***** job concluded
******
**x1136010_hw2_xor**

****** job statistics summary tnom=  25.000 temp=  30.000 ******
```

Bonus

```
******
**x1136010_hw2_bonus**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power= 1.1784e-05  from= 0.0000e+00     to= 5.0000e-08
delay1_xor= 3.6559e-11  targ= 2.0052e-08   trig= 2.0015e-08
delay2_xor= 9.4209e-11  targ= 2.5992e-09   trig= 2.5050e-09

         ***** job concluded
******
**x1136010_hw2_bonus**

****** job statistics summary tnom=  25.000 temp=  30.000 ******
```

Delay time analysis

Basic

1. Delay1_XOR = 187 ps
2. Delay2_XOR = 299 ps
3. Diff abs = 112 ps

Bonus

1. Delay1_XOR = 36.56 ps
2. Delay2_XOR = 94.21 ps
3. Diff abs = 57.65 ps

Hardness

1. Unfamiliar with the software virtuoso
   - Thankyou the helping from TA, it let me get familiar with it.
2. Test bench file, I forget to define VDD in the test bench file and I get stuck in this bug (passed drc, lvs, pex but getting weird wave) for 3~4 hours.
   - Nothing surprise, just check from 0 to the end.
3. There is some weird bug in the LVS testing, I get incorrect in overall but correct at the bottom, I don’t know why but the TA explain there may be the tool error. Also even I reopen and run LVS test again and still getting the same result, but the PEX result and the wave is good even though this LVS test error occur.
   - Not overcome this problem, still getting stuck in the LVS error even the others works well and the wave form is good.