# CS312000 Introduction of Integrated Circuit Design

# Homework 1: HSPICE simulation

Due Date: 2024/10/20 (Sun.) 23:59:59

## Background

In Very-Large-Scale Integration (VLSI) design, logic gates play a fundamental role in processing and manipulating digital signals. Understanding the behavior of these gates under different conditions is essential for designing efficient and reliable integrated circuits. In this assignment, you will use HSPICE, a widely used electronic circuit simulation tool, to explore the waveforms generated by basic logic gates: AND, OR, and an inverter.

## Description

In this homework, you are asked to write an HSPICE program for simulating the circuit behavior of a logic function that consists of the logic gates (AND, OR, and inverter). Firstly, we observe the behavior of the logic gates by HSPICE simulation. After that, we will consider the compound gates as shown in Figure 4. You are also asked to simulate the behavior of the logic function by the program.

### • Inverter

Inverters are fundamental in digital logic. Create an HSPICE simulation to model the behavior of an inverter. An inverter takes a single binary input (0 or 1) and produces the logical complement of that input. You need to define input signals to test the inverter's functionality, including $(in1) = 0$ and 1.

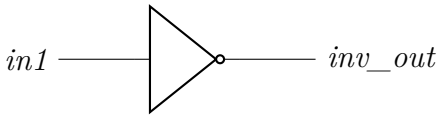


Figure 1: Inverter

### • AND and OR gates

The AND and OR gates take two binary inputs (0 or 1) and produce outputs based on their logical operation. You need to define appropriate input signals (voltages) to test

the two gate's functionality. The input should include the combinations of (in2, in3) and (in4, in5) = (0, 0), (0, 1), (1, 0), and (1, 1) in sequence.

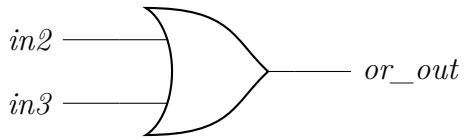


Figure 2: OR2 gate

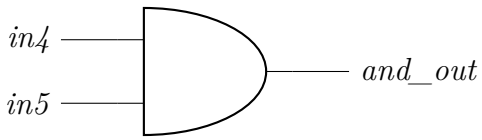


Figure 3: AND2 gate

## • Logic Function

The diagram of the specified logic function $d\overline{(b+\overline{c})} + c(\overline{b}+a)$ is shown in Figure 4, which consists of the eight logic gates mentioned above. You need to define appropriate input signals (voltages) to test the functionality of this logic function. The input should sequentially include the combinations of

$$\begin{aligned}(a,b,c,d) = &(0,0,0,0),(0,0,0,1),(0,0,1,0),(0,0,1,1),\\ &(0,1,0,0),(0,1,0,1),(0,1,1,0),(0,1,1,1),\\ &(1,0,0,0),(1,0,0,1),(1,0,1,0),(1,0,1,1),\\ &(1,1,0,0),(1,1,0,1),(1,1,1,0),(1,1,1,1).\end{aligned}$$

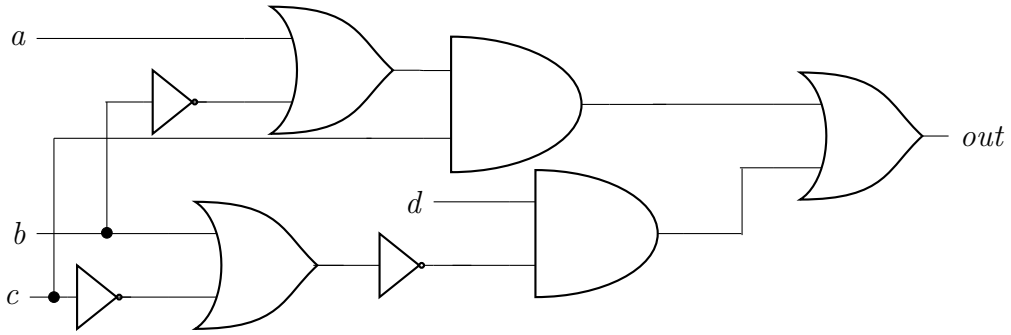


Figure 4: Logic Function $out = d\overline{(b+\overline{c})} + c(\overline{b}+a)$

After running the HSPICE simulation, you will obtain waveform plots for both input signals and outputs. Ensure that the simulation captures the gate's response to various input conditions and provides screenshots of the waveform plots for the logic gates and the logic function in your report.

# Bonus

Design a 4-to-1 MUX using three 2-to-1 transmission gate multiplexors. Please follow the naming rule as shown in Figure 5.

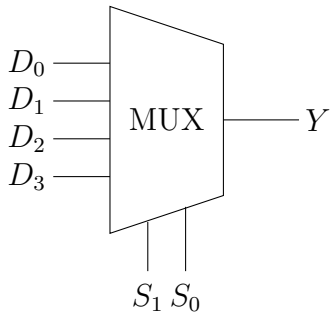


Figure 5: 4-to-1 MUX

# Limitations

Below are the guidelines that must be adhered to for this assignment. Any violation of these guidelines will result in 0 points for this HW.

- **Environment setup and parameters**

  i. You must complete this HW using the process file provided by us. (on the eeclass)

  ii. The operating voltage (VDD) is set to 1.8V

  iii. For transistors, please set the L=0.18um, while the minimum value of W is 0.25um and the value of W can be adjusted as needed.

- **Inputs and outputs**

  i. You must complete this HW using the process file provided by us. (on the eeclass)

  ii. The operating voltage (VDD) is set to 1.8V

- **Coding style**

```
** studentID_HW1 **
** Environment setting **
************************
*      Your code        *
************************
```

```
*** Inverter ***
.subckt INV in1 inv_out vdd vss
** Your code **
.ends

*** OR ***
.subckt OR2 in2 in3 OR vdd vss
** Your code **
.ends

*** AND ***
.subckt AND2 in4 in5 AND vdd vss
** Your code **
.ends

*** logic function ***
.subckt logic A B C F vdd vss
** Your code **
.ends
```

```
** studentID_HW1_bonus **
** Environment setting **
************************
*      Your code        *
************************

*** 4 to 1 MUX ***
.subckt MUX S0 S1 D0 D1 D2 D3 Y vdd vss
** Your code **
.ends

...
```

## Submission Requirement

You have to submit a source code file named StudID_HW1.sp (ex: 123456_HW1.sp) and a report named StudID_Name_HW1.pdf (ex: 123456_ 陳小明 _HW1.pdf). If you implement a bonus version, please separate it from the original version. Name your source

code file of the bonus version as StudID_HW1_bonus.sp (ex: 123456_HW1_bonus.sp) and upload it to ee-class with the original version. Note that the only acceptable report file format is .pdf, no .doc/.docx or other files are acceptable. **BE SURE to follow the naming rule mentioned above. Otherwise, your program will not be graded.**

We don' t restrict the report format and length. In your report, you must at least describe:

i. How to perform the simulation. (You can use a screenshot to explain)

ii. The completion of the assignment. (If you complete all requirements, just specify all)

iii. The waveform of OR gate, AND gate, inverter, and the specific logic function for every combination of inputs.

iv. The hardness of this assignment and how you overcame it.

v. Any suggestions about this homework?

vi. If you implement the bonus version, you have to provide the transistor-based schematic diagram in your report.

You can also put anything related to the HW in your report, such as pseudocode, programming developing thought, etc.

# Grading

The grading is as follows:

i. Correctness of your code: 48% (The outputs of the specific logic function according to 16 combinations of input and each for 3%)

ii. Readability of your code: 10%

iii. The report: 12%

iv. Demo session: 30%

v. Bonus (at most): 10%

Please submit your assignment on time. Otherwise, the penalty rule will apply:

- **Within 72hrs delay: 20% off**

- **More than 3 days: 0 point**

Be sure to attend a demo session (the time will be announced later). If you have questions, please contact us:

- **Yu-Guang Chen: andyygchen@ee.ncu.edu.tw**
- **TA Chi-Tse Pai: j37619821765321@gmail.com**

# References


[1] https://cseweb.ucsd.edu/classes/wi10/cse241a/assign/hspice_sa.pdf

[2] https://www.synopsys.com/content/dam/synopsys/verification/hspice-quickrefcard-M-2017-03.pdf

[3] https://hackmd.io/@azoo/hspice_tutorial