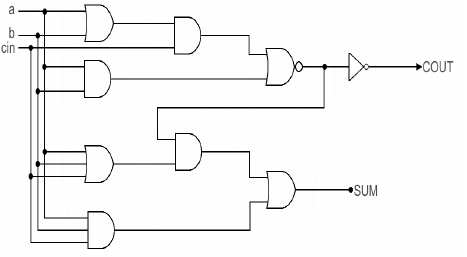
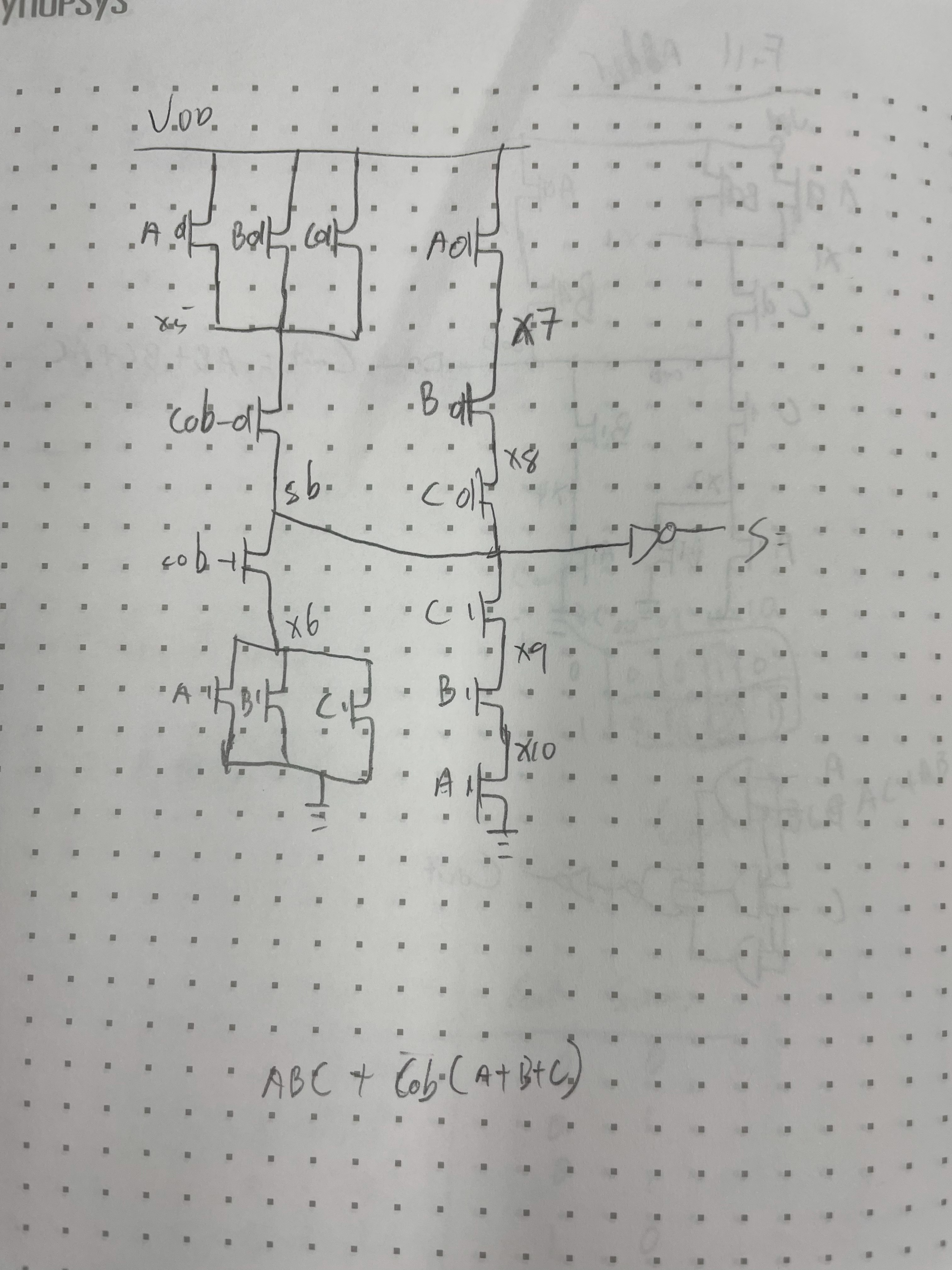
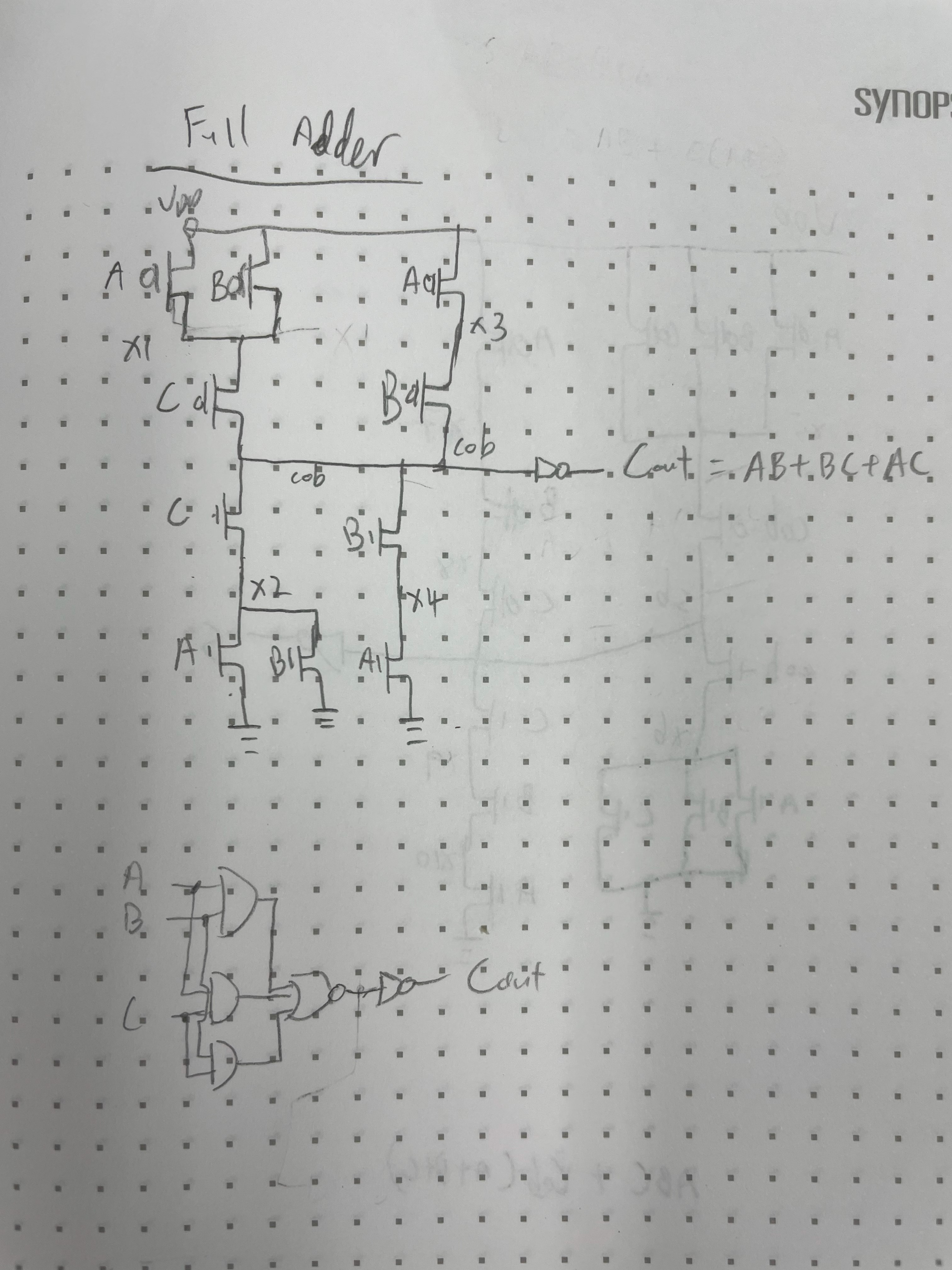
## 黃偉祥 X1136010

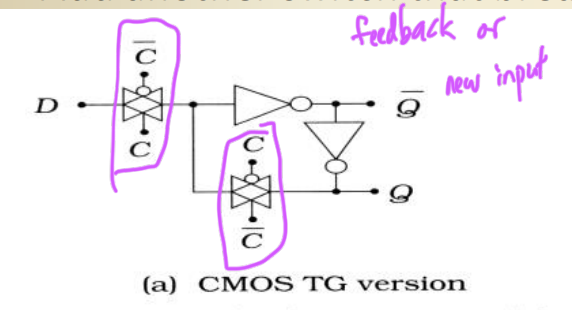
Full Adder





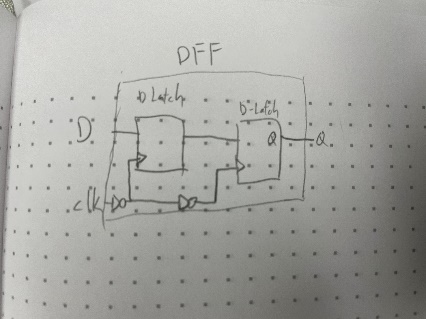
* I use the online Full adder version to design my full adder.
* For Multiple bits full adder, I just connect them together.

D Latch



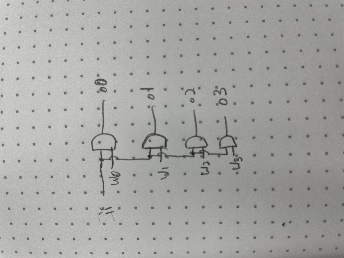
* I use ppt version of D Latch to design my DLatch\_TG
* I use D-latch to store Weights.

D Flip Flop



* I use 2 D-latch to build my positive edge DFF

IdotW



* I just and ii with all w0, w1, w2, w3 separately.
* This use for every I \* W in all column and row.

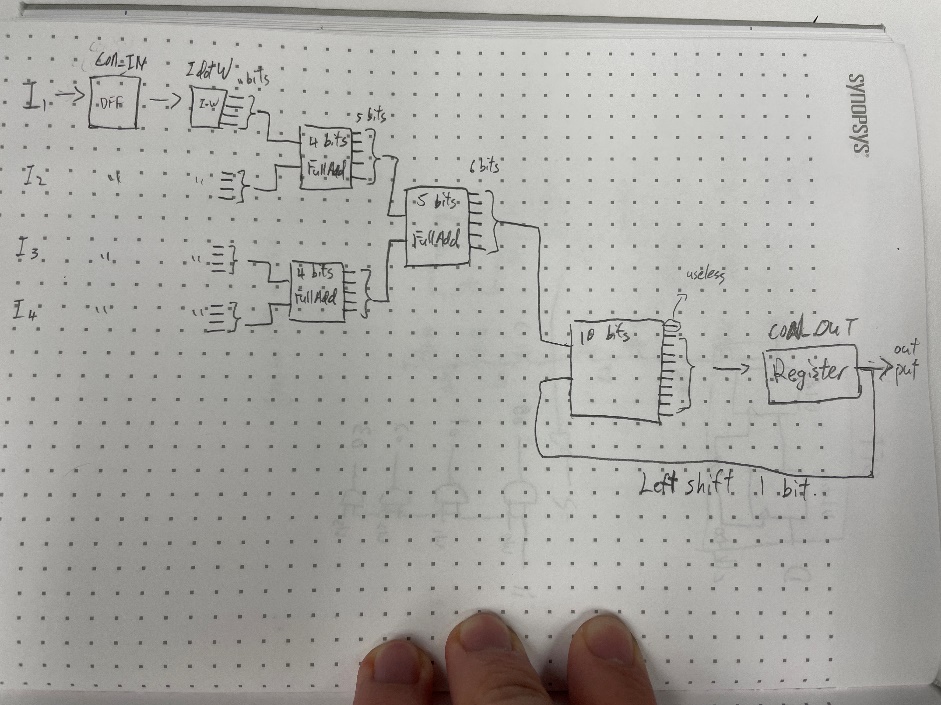
OUT\_NOW

* I use 1 DFF to keep the previous IN\_VAL, then check if previous IN\_VAL is 1 and current IN\_VAL is 0 🡺 Fall occurs.
* When Fall occurs then OUT\_VAL need to be 1 for a cycle in the next cycle, so I use another DFF to output the OUT\_VAL.

CON\_IN & CON\_OUT

* I use DFF to done this 2, the different is only CON\_IN use IN\_VAL to check while CON\_OUT use RST to check.
* And CON\_IN use 4 DFF while CON\_OUT use 10 DFF.

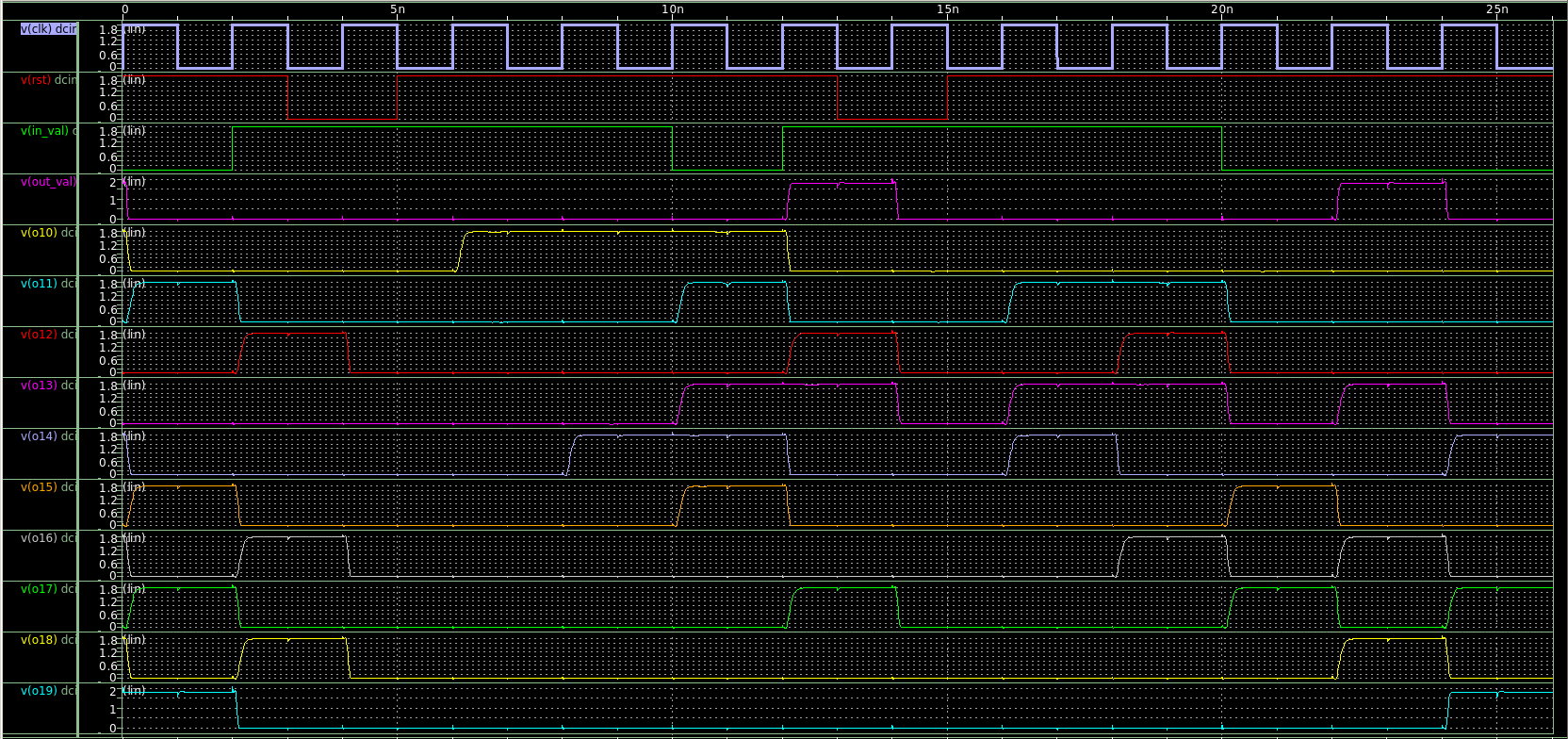
Design



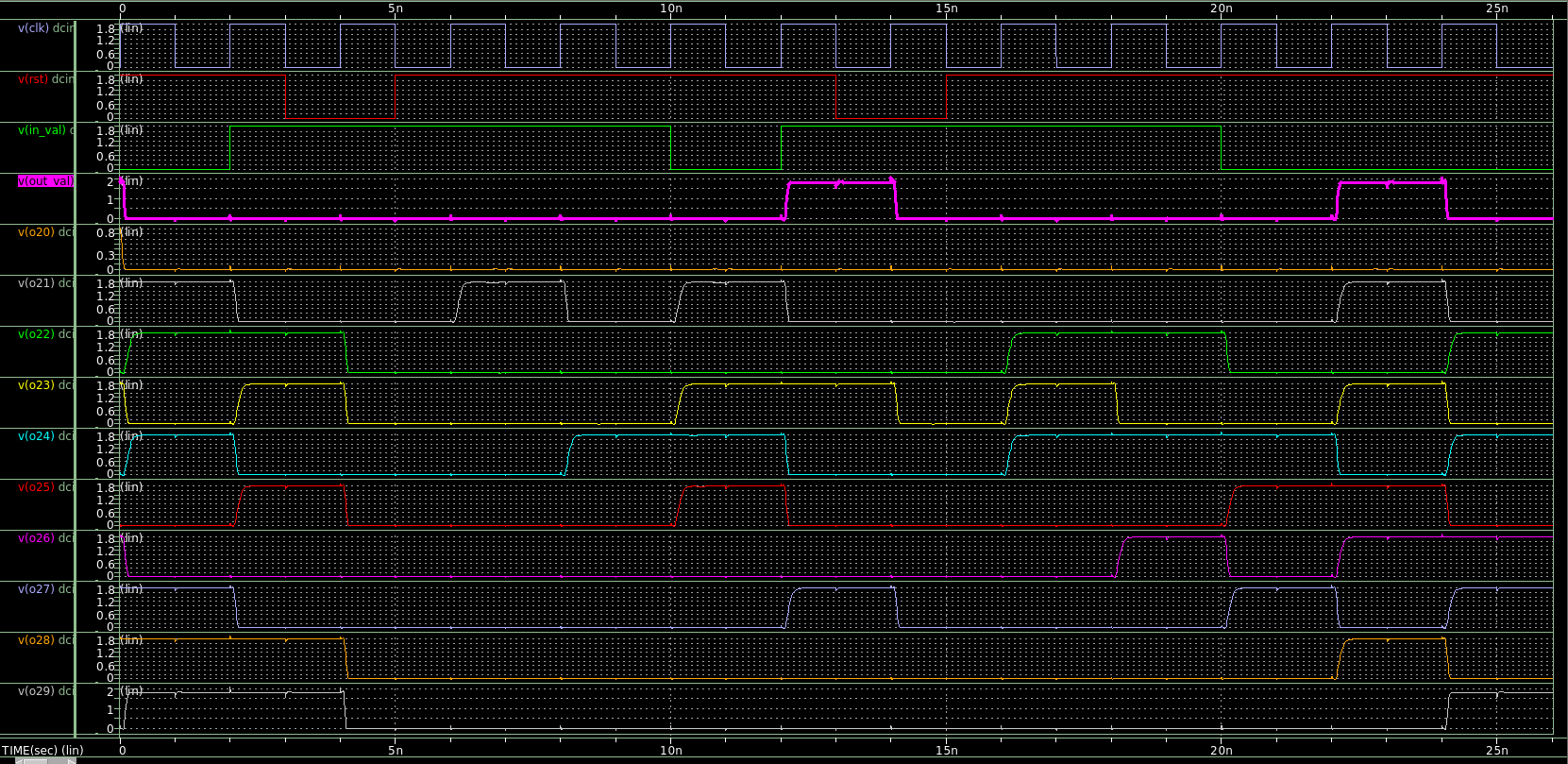
* I use all subcircuit that I show in above and connect them just like the figure above.

Waveform

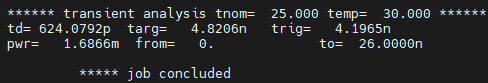
1. Column 1 wave form



1. Column 2 wave form

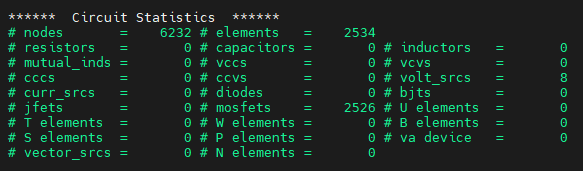


Delay and Power



1. Delay = 624.0792 p
2. Power= 1.6866 m

# Transistors



* Total : 2526 mosfets

Hardness

1. The Full adder delay of my design, this gives me so much trouble when checking problem and debugging.
   1. Thanks my friend helping me to get another kind of Full adder design and then everything done!
2. First I thought Latch and Flip-flop is the same thing, but then when TA time I knew that we need to use flip-flop instead of latch…
   1. TQ TA, I will check the document properly next time…
3. I need more TA time and my email always get into dustbin…