CS3120

Introduction of Integrated Circuit Design

Homework 2: Layout Design

Andy, Yu-Guang Chen

Associate Professor, Department of EE, National Central University

Adjunct Assistant Professor, Department of CS, National Tsing Hua University

andyygchen@ee.ncu.edu.tw

Slides Credit: TA 張孫婕

Outline

- Description
- Input/Output
- Report
- Grading
- DRC Rules
- Notice

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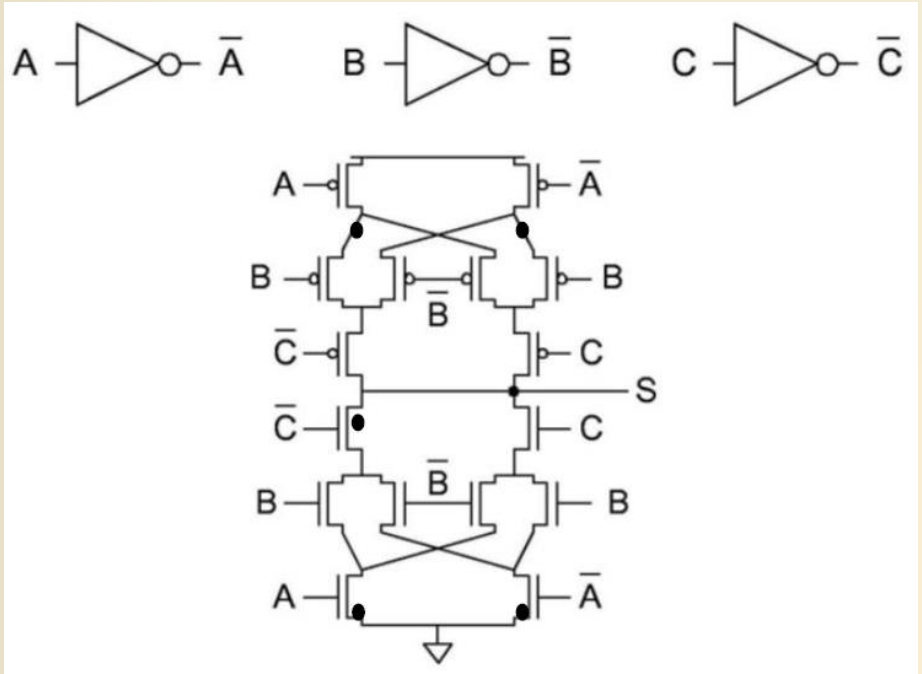
Description

- Design a 3-input XOR gate which drives a capacitance of 0.005pF
- Use the design form in the document



Description

- Operating voltage (VDD): 1.8V
- Operating temperature: 30˚C
- Capacitive of output S is 0.005pF
- For transistors
  - set L = 0.18um
  - The minimum value of W is 0.25um, and the value of W can be adjusted as needed

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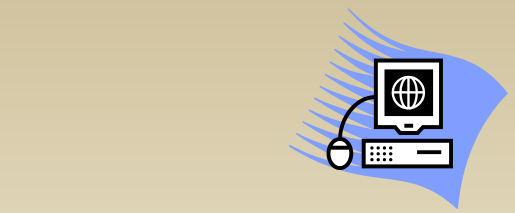
Input/Output

- The input should include the combinations of (C, B, A) = (0, 0, 0), (0, 0, 1), (0, 1, 0), (0, 1, 1), (1, 0, 0), (1, 0, 1), (1, 1, 0) and (1, 1, 1) in sequence
- The naming and pinouts of each input and output must match the figures provided in the document

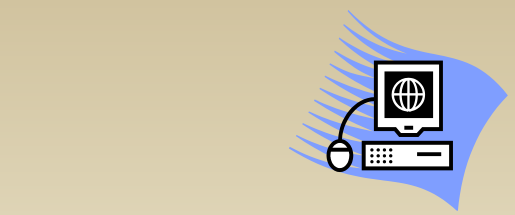


Input/Output

- Input signals:
  - 50% duty cycle
  - A operates at 200 MHz, B at 100 MHz, and C at 50 MHz
  - The order of input combinations (C, B, A) should match the orders in the document
  - Set rise/fall time of the input signals to 10ps

Input/Output

- Output signals:
  - Highest voltage must be larger than 0.9VDD
  - Lowest voltage must be lower than 0.1VDD



Input/Output

- Need to show the delay and the difference in delay between rising and falling delay in the 3-input XOR gate
  - Delay1_XOR: signal A and S are falling
  - Delay2_XOR: signal A and S are rising
  - |Delay1_XOR-Delay2_XOR | =_____ ps

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Report

1. The circuit diagram of your design and explaining your design
2. Pre-sim waveform
3. Screenshot of your layout
4. Screenshot of DRC summary report
5. Screenshot of LVS report include the message of passing LVS

Report

6. Post-sim waveform
7. Screenshot of the post-simulation result
8. Write down your delay and the difference in delay between rising and falling delay in the 3-input XOR gate
9. The hardness of this assignment and how you overcome it
10. Any suggestions about this programming assignment

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Grading

- Correctness: 40%
  - Pre-sim: 10%
  - DRC: 10%
  - LVS: 10%
  - Post-sim: 10%
- Performance: power, area 10%
- Readability of hspice code: 10%
- Report: 10%
- Demo session: 30%
- Bonus: 10%

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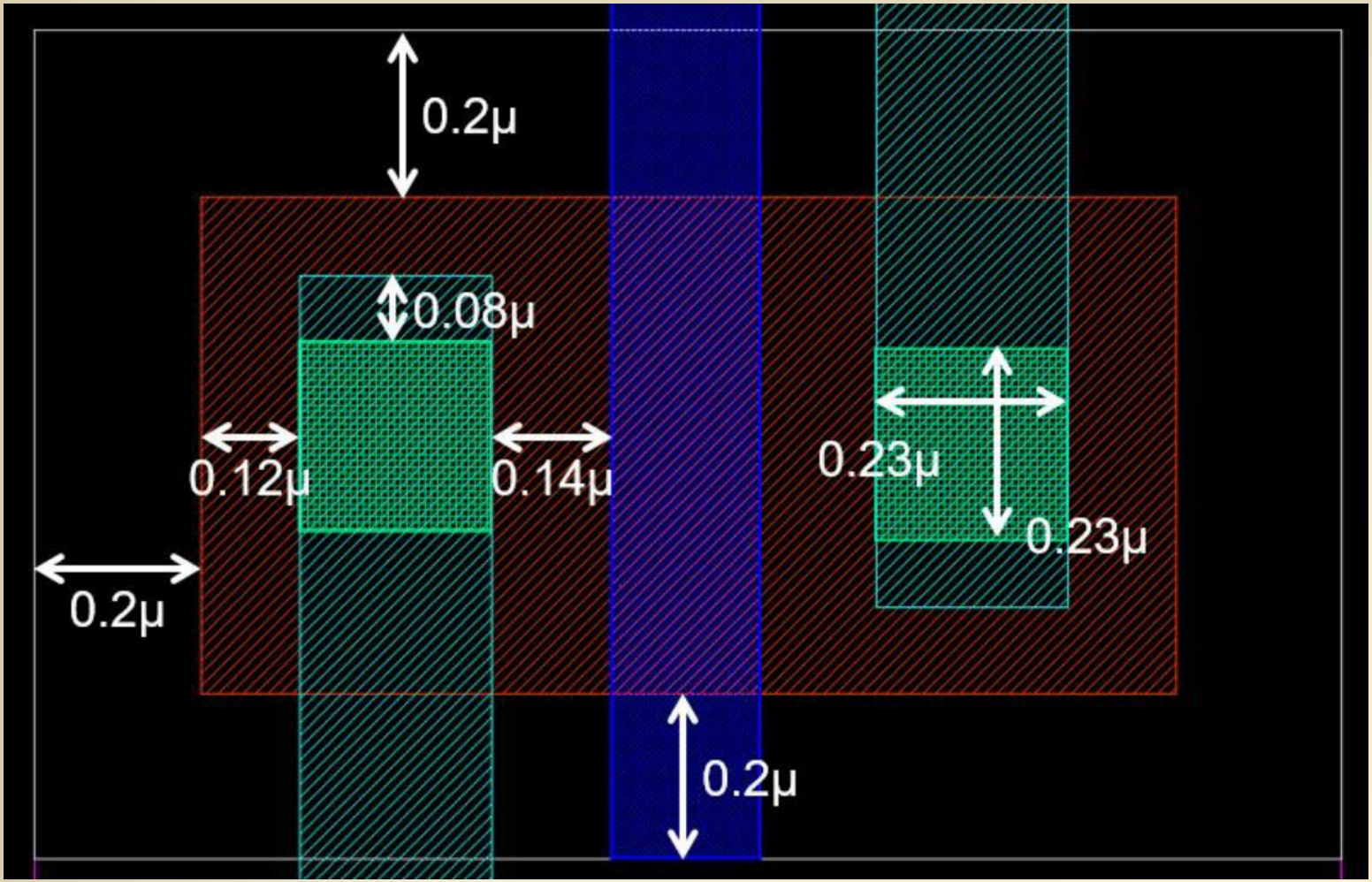
DRC Rules

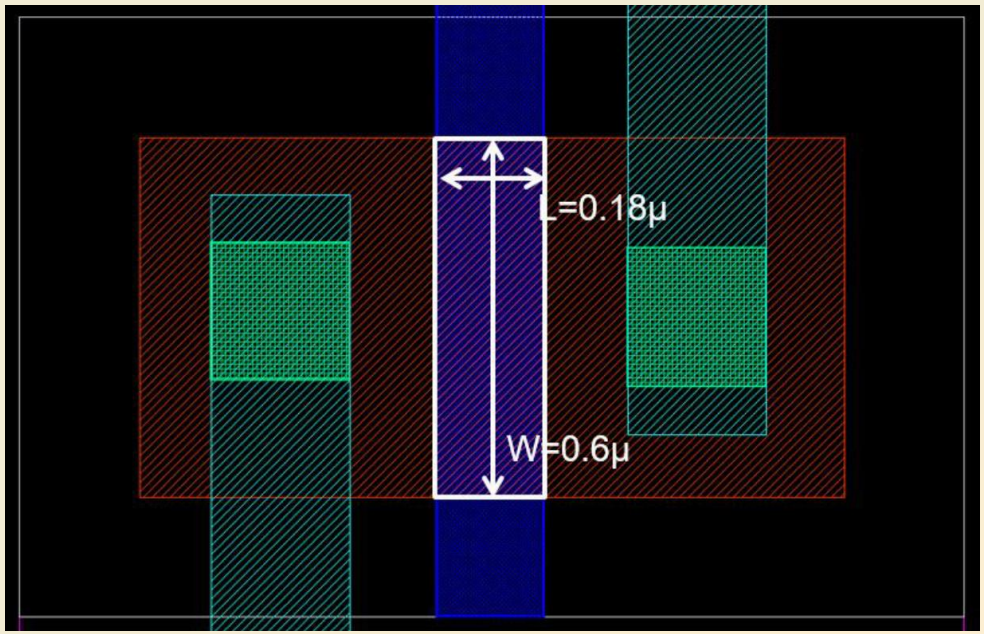
- cont width and length = 0.23µm
- Spacing between cont and diff > 0.12µm
- Spacing between Pimp/Nimp and diff > 0.2µm
- Spacing between poly and cont > 0.14µm
- Spacing between metal and metal > 0.24µm
- Spacing between cont and cont > 0.25µm

DRC Rules



DRC Rules

- The length of W is determined by your design
  - Will compare with the HSPICE code when you run LVS
- The W and L in your layout must be the same as the ones in HSPICE code



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Notice

- Only Metal 1、Metal 2 and Via can be used when routing
- You must use the same approach as 'cic018.l' and 'cic18.tf' in HW2 to do this assignment; otherwise, you will get 0 points
- BE SURE to follow the naming rule in the document; otherwise, your program will not be graded