CS3120

Introduction of Integrated Circuit Design

Final Project

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Outline

- Problem formulation
- Bonus
- Requirements
- Report
- Grading
- Spice

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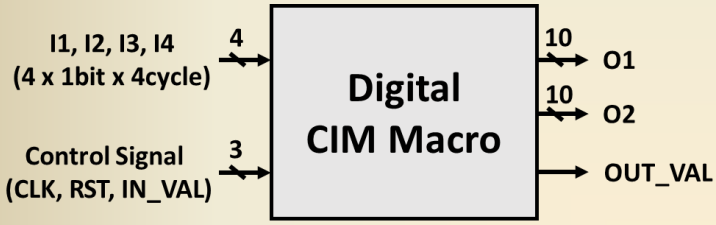
Problem formulation

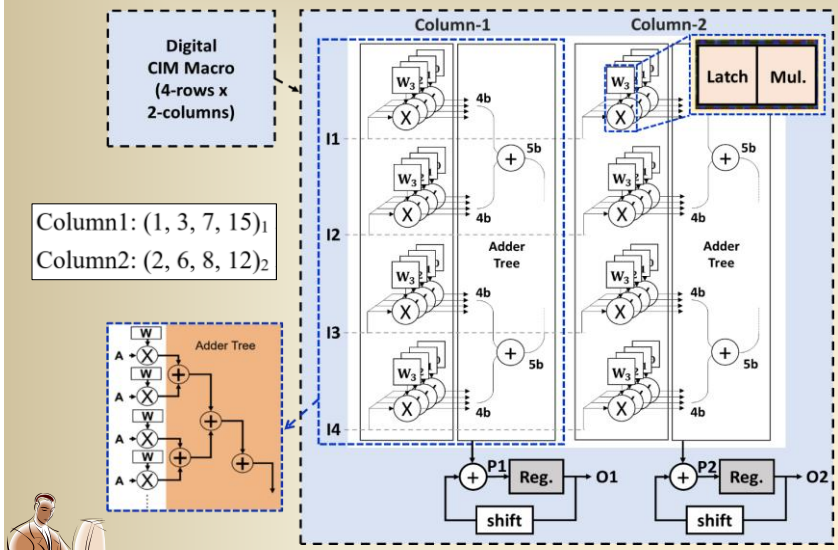
- Design a 4-rows x 2-columns Digital CIM for Vector-Matrix Multiplications



Problem formulation

- Inputs vector (I1, I2, I3, I4):
  - I1, I2, I3, I4 are 4 bits (serially given from MSB to LSB)
- Weights matrix (W):
  - 4 rows x 2 columns: $(W1, W2, W3, W4)_1$, $(W1, W2, W3, W4)_2$
  - All weights are 4 bits (stored in latches by initial conditions)
- Output (O1, O2):
  - O1, O2 are 10 bits
  - $O1 = (I1 \times (W1)_1) + (I2 \times (W2)_1) + (I3 \times (W3)_1) + (I4x (W4)_1)$
  - $O2 = (I1 \times (W1)_2) + (I2 \times (W2)_2) + (I3 \times (W3)_2) + (I4x (W4)_2$

Problem formulation



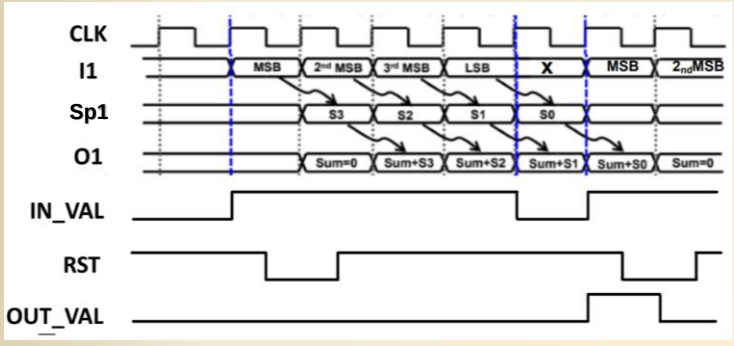
Problem formulation

◆Signals

Input signal	Bit width	Definition
I1, I2, I3, I4	1 bit each	Input serial signals
CLK	1 bit	Clock, period: 2 ns
RST	1 bit	Asynchronous active-low reset
IN_VAL	1 bit	Inputs are valid
Output signal	**Bit width**	**Definition**
O1, O2	10 bits each	Output signals
OUT_VAL	1 bit	O1 and O2 are valid (finished)
Other signal	**Bit width**	**Definition**
ii1, ii2, ii3, ii4	1 bit each	The input from flip-flop
P1, P2	10 bits each	The output before flip-flop

Problem formulation

◆Waveform



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Bonus

- Design a 32-rows x 16-columns Digital CIM for Vector-Matrix Multiplications
- Same functionality of original version

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Requirements

- Clock period in this program is set to 2 ns
- Rise and fall time will be 1 ps for all signals
- The operating voltage (VDD) is set to 1.8V, VSS is set to 0V, and the operating temperature is 30˚C
- For transistors, set L=0.18um, NMOS W=0.36 um, and PMOS W=0.72um
- You must use the “cic018.l” to do this assignment, otherwise you will get 0 point

Requirements

- Follow the naming rule below
  - SPICE code file name: DCIM.sp, DCIM_bonus.sp
  - Primary circuit name: DCIM
  - Cell name for your primary circuit: Xdcim
  - Signals in the program: named as we mention in page 7
- Complete this project using the process file provided by us. (on the ee-class)

```
*** call cell ***
Xdcim I1 I2 I3 I4 IN_VAL CLK RST O10 O11 O12 O13 O14 O15 O16 O17 O18 O19 O20 O21 O22 O23 O24 O25 O26 O27 O28 O29 OUT_VAL DCIM

*** DCIM block ***
.subckt DCIM I1 I2 I3 I4 IN_VAL CLK RST O10 O11 O12 O13 O14 O15 O16 O17 O18 O19 O20 O21 O22 O23 O24 O25 O26 O27 O28 O29 OUT_VAL
** Your code **

Xcontrol_in I1 I2 I3 I4 CLK RST ii1 ii2 ii3 ii4 INPUT_CON
Xcontrol_out1 P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 CLK RST O10 O11 O12 O13 O14 O15 O16 O17 O18 O19 OUTPUT_CON
Xcontrol_out2 P20 P21 P22 P23 P24 P25 P26 P27 P28 P29 CLK RST O20 O21 O22 O23 O24 O25 O26 O27 O28 O29 OUTPUT_CON
.ends
```


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Report

- The circuit diagram of your design and explaining your design (You can use screenshot to explain)
- The transistor level view of your CIM circuit and adder (You can just draw one of them and specified how you connect each)
- The bonus circuit if implemented
- Waveform of your simulation
- The delay and the power of the circuit
- The total number of transistors (NMOS and PMOS) you use in this program
- The hardness of this assignment and how you overcome it
- Any suggestions about this programming assignment

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Grading

- Correctness (60%)
  - 5 test cases for each 12%
- Performance (20%): 5% (delay time) + 5% (power) + 10% (area)
  - Delay time and power by your simulation result
  - Area for your number of transistors in your program
  - Score function: maximum_score*(your result percentage of the class)
  - Your performance score will be 0 if you failed the testcase.
- Readability of HSPICE code (10%)
- The report (20%)
- Bonus (10%)
  - 1 test case, the bonus score will be 10 if all correct, otherwise 0.

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Initial condition

- To initialize the voltage.
- .ic V(*your_node_name*)=*voltage*

```
.ic V(W10)=1.8v
```

- If your node is not the global signal, you can access it by *sub_circuit_name*. *your_node_name*

```
.ic V(Xdcim.Xcim_c11.W0)=1.8v
```

- You can also initialize more than one node in one .ic

```
.ic V(Xdcim.Xcim_c11.W0)=1.8v V(Xdcim.Xcim_c11.W1)=0v
```


Delay time

- Get the delay time from trigger signal to target signal (the first rising edge to half of voltage).
- .measure TRAN *element*
- +TRIG V(*trigger_signal*) VAL=0.9 RISE=1
- +TARG V(*target_signal*) VAL=0.9 RISE=1

```
.measure TRAN td
+ TRIG V(Xdcim.ii1) VAL=0.9 RISE=1
+ TARG V(Xdcim.P10)  VAL=0.9 RISE=1
```

Power

- Get the average power of the circuit.
- .measure TRAN *element* AVG POWER

```
.measure TRAN pwr AVG POWER
```


Simulation results

- You can find the simulation results in .lis file
- Delay time & power

```
****** transient analysis tnom=  25.000 temp=  30.000 ******
td= 243.3594p  targ=   4.3664n   trig=   4.1231n
pwr= 821.6744u  from=   0.             to=  20.0000n
```

- Number of transistor

```
******  Circuit Statistics  ******
# nodes        =    2683 # elements   =    1105
# resistors    =       0 # capacitors =       0 # inductors   =       0
# mutual_inds  =       0 # vccs       =       0 # vcvs        =       0
# cccs         =       0 # ccvs       =       0 # volt_srcs   =       8
# curr_srcs    =       0 # diodes     =       0 # bjts        =       0
# jfets        =       0 # mosfets    =    1097 # U elements  =       0
# T elements   =       0 # W elements =       0 # B elements  =       0
# S elements   =       0 # P elements =       0 # va device   =       0
# vector_srcs  =       0 # N elements =       0
```