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Experiments

Exp	Core Utilization	Clock Period	DRC Violations	Slack	Chip Area	Wire Length
1	0.5	600	0	3.443	56247.914	184883.84
2	0.45	600	0	3.443	56247.914	184883.84
3	0.45	600	0	3.443	56247.914	184883.84
4	0.2	600	1	8.117	122090.914	192436.324
5	0.8	600	9	5.238	32789.09	164368.1880
6	0.6	600	1	2.2	42877.797	185762.516
7	0.5	600	0	0.789	50916.999	190917.148
8	0.3	600	0	9.9	82695.023	192140.94
9	0.5	600	0	6.8	50916.999	188329.04
10	0.65	600	0	3.127	39775.298	180169.116
11	0.6	600	0	2.2	42877.797	185761.2080
12	0.6	100	153	-368.4	42877.797	224406.9280
13	0.6	400	1	-70.6	42877.797	222211.7920
14	0.6	800	0	42.953	42877.797	186532.928
15	0.7	800	2	25.734	37121.981	175343.06
16	0.6	500	0	-0	42877.797	192014.888
17	0.55	500	0	-0.064	50075.512	196172
18	0.6	520	0	0.237	42877.797	188904.124

Explanations

- Experiments with highlighted show us how clock period and core utilization affect the DRC violations, slack, chip area, and wire length.
  - Yellow show that core utilization affect more on chip area and wire length.
  - Purple & Green show that clock period cannot be too small and it affect more on slack.
- Clock period will have big impact on slack time, because (Slack Time = Required Time – Arrival Time), while (Required Time = Clock period - Setup).
- From the experiments clock period will also affect the DRC violations as

experiment 12 show that when clock period is very low (100), it takes very lot of time to place and route, but in the end still having slack violation and DRC violations.

- While Core Utilization affect more on Chip Area and Wire Length, the higher of the Core Utilization will give lower on Chip Area and Wire Length, but it will have higher chance to having Slack violation and DRC violations.
- In conclusion, Clock period will affect more on Slack, Core utilization will affect more on Chip area and Wire length. While DRC violations are affected by the place and route algorithm, and the algorithm will consider both clock period and core utilization, so both will affect some on DRC violations.

Well tap cell

- To prevent Latch-up condition, basically connect n-well with VDD and body(p-sub) with VSS to strengthen the PN junction between nMOS and pMOS.
- To protect the circuit from damage caused by static electricity, it give a path for electrostatic discharge.

Best result

1. Clock period = 520
2. Slack time = 0.237
3. Total area of chip = 42877.797 um^2
4. Total wire length = 188904.124 um
5. DRC violations = 0

Layout