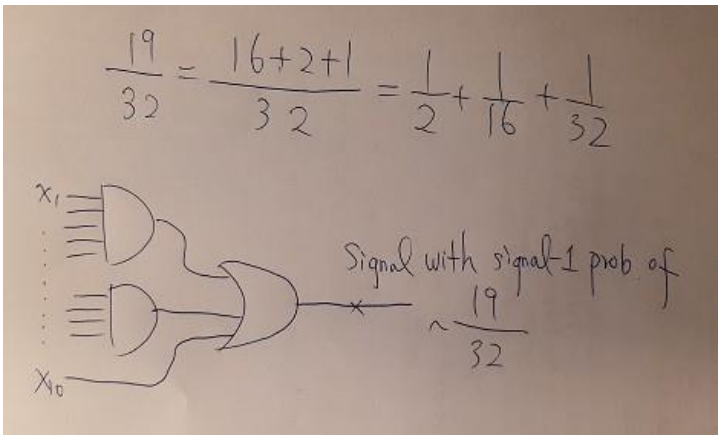
國立清華大學 電機工程學系碩博士班
109 學年度第一學期
EE-6250 超大型積體電路測試 VLSI Testing
期末考 Jan. 13, 2021 (總分 100 分)
(Closed-Book Examination)

1. (20%) Answer the following questions briefly.
   (a) Explain the **aliasing problem** in a logic BIST method. (5%)
   ➔ **The probability that faulty responses are compressed into a fault-free signature.**

   (b) (10%) Suppose we have 10 random signals produced by a **Linear Feedback Shift Register** (LFSR), denoted as $\{x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, x_9, x_{10}\}$. Show a logic circuit that can use these ten signals to produce a *weighted random signal* with the signal-1 probability roughly being 19/32 using only two AND gates and one OR gate. (5%)

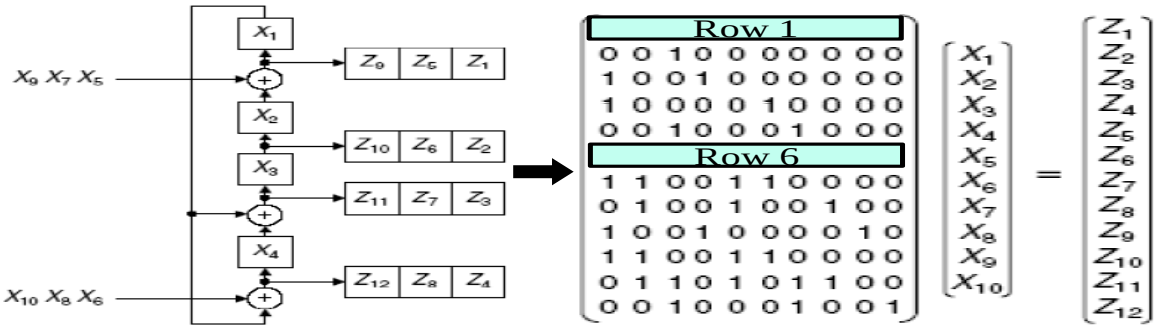


   (c) The reliability of a semiconductor device is often characterized by a "**bathtub curve**", with the entire lifetime divided into three stages, including "infant mortality stage", "normal lifetime stage", and a third stage. Give a name for the third stage and explain what it means briefly. (5%)
   ➔ **Wear-out or ageing stage, in which the failure rate increases due to the ageing of the device.**

   (d) To perform **voltage-drop monitoring**, we can use the power node under monitoring to drive the power pin of a Ring-Oscillator (RO), producing a clock signal, e.g., named *RO_clk*. What information in *RO_clk* during a monitoring session could be used to represent the "worst-case dynamic supply voltage level"? (5%)
   ➔ **The largest clock cycle time (during that monitoring session).**

2. (10%) Answer the following questions.
   (a) List the 5 basic input/output signals used in **IEEE Std. 1149.1**. (5%)
   ➔ **{TCK, TRST, TDI, TDO, TMS}**
   (b) A Boundary Scan Cell (BSC) in IEEE Std. 1149.1 is controlled by three important control signals, namely *ClockDR*, *ShiftDR*, and *UpdateDR*. For a BSC at a chip's input pin, which signal will determine the timing of data latching from the input pin of the chip to this BSC? (5%)
   ➔ **ClockDR**

3. (10%) Consider the **linear-decompression scheme** characterized by a de-compressor as shown below. Fill in the missing rows in its matrix form.



➔ **ROW-1: [0100100000]，ROW-6: [0010001000]**

4. (10%) Consider the test compression using "**broadcasting scan test**" for a test pattern in a circuit with 5 scan chains and the sub-patterns for the 5 scan chains are {p1=(11XX0), p2=(XX1X0), p3=(1XXX1), p4=(X10X1), p5=(X1XX0)}.
   (a) We can compress the above 5 sub-patterns into 2 common sub-patterns. Show the two common sub-patterns. (5%).
   ➔ **Common sub-pattern-1: (111X0) for {p1, p2, p5}**
   ➔ **Common sub-pattern-2: (110X1) for {p3, p4}**
   (b) What is the test compression ratio for this test pattern? Note that the test compression ratio is defined as the ratio of the "original test data volume" to the "compressed test data volume". We ignore the control bit volume during the test application in this calculation. (5%) ➔ **5/2 (or 2.5)**

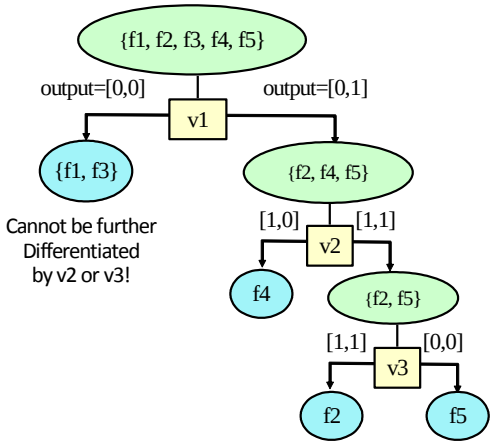
5. (10%) Consider the following **fault diagnosis** problem for a combinational circuit with 3 primary inputs {*x*1, *x*2, *x*3} and 2 primary outputs {*z*1, *z*2}. There are 5 stuck-at faults {*f*1, *f*2, *f*3, *f*4, *f*5} and 3 test patterns {*v*1, *v*2, *v*3} under consideration. The full-response fault dictionary is shown below. ➔ **see attached figure below**

   (a) Show the diagnostic tree assuming the following test response examination order: *v*1➔ *v*2➔ *v*3. (5%)

   (b) What are the possible "diagnostic resolution" using this cause-effect analysis? Note that the "diagnostic resolution is the "number of fault candidates" reported at the end of a fault diagnosis process. (5%)

   ➔ **Diagnostic resolution could be 1 or 2.**

Circuits	Output Response (z1, z2)		
	Pattern v_1	*Pattern* v_2	*Pattern* v_3
fault-free	(0, 1)	(1, 1)	(1, 0)
*f*1	(0, **0**)	(1, 1)	(1, 0)
*f*2	(0, 1)	(1, 1)	(1, **1**)
*f*3	(0, **0**)	(1, 1)	(1, 0)
*f*4	(0, 1)	(1, **0**)	(1, 0)
*f*5	(0, 1)	(1, 1)	(**0**, 0)



6. (10%) Answer the following questions about interconnect and clock network testing.

   (a) What is the test stimulus in **Pulse-Vanishing Test** (PV-test) for an interconnect? What symptom at the termination end of an interconnect is used as an indicator of the presence of a delay fault somewhere along the interconnect under test? (5%)

   ➔ **The test stimulus is a "short-pulsed signal" (畫圖說明也可以)**

   It is a faulty symptom when the pulse vanishes at the end of the interconnect

   (b) When we apply the **modified flush-test**, discussed in class, for detecting a Clock Delay Fault (CDF) somewhere on a clock network, the alternating 0-1 patterns are pumped through the scan chains following a "Scan-Excite-Scan" procedure. What is the key feature of the "Excite" cycle so that we can effectively excite a CDF? (5%)

   ➔ **A "short-pulsed clock cycle" (畫圖說明也可以)**

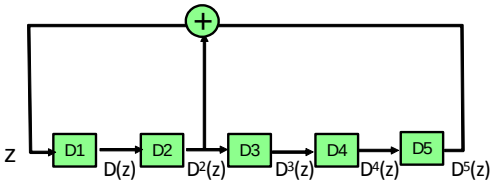
7. (15%) Answer the following questions related to **LFSR**.

(a) There are two basic requirements to produce (2^n-1) pseudo random patterns using a LFSR. One of them is to choose a LFSR with a primitive (or irreducible) polynomial. Name the other requirement. (5%)

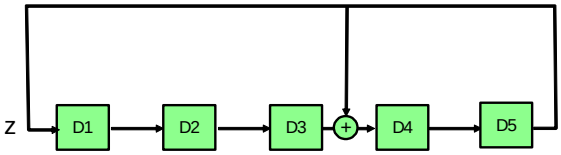
➔ **Avoid an All-'0' seed (i.e., one with every bit being '0').**

(b) Consider the design of a LFSR generating a maximum-length sequence of random patterns. The characteristic polynomial of such a LFSR shown below is represented as $p(x) = x^4 + x^1 + 1$, where x corresponds to a delay element in the circuit structure, meaning the "delay of one clock cycle". (Note: D1, D2, D3, D4 in the figure denotes 4 flip-flops). Try to generalize it and show the out-tap structure for a 5-stage maximum-length LFSR with a characteristic polynomial as $p(x)=x^5+x^2+1$. (Hint: This is an LFSR with a recursive formula as $z = D^5(z)+D^2(z)$. (5%)

(c) Convert the out-tap structure into its in-tap version. (5%)



(b) out-tap structure for $p(x)=x^5+x^2+1$



(c) in-tap structure for $p(x)=x^5+x^2+1$

8. (15%) Consider the **Hoffman encoding** for 8 symbols {s1, s2, s3, s4, s5, s6, s7, s8} in a test pattern. Their numbers of occurrences in the test pattern are {ϕ(s1)=5, ϕ(s2)=50, ϕ(s3)=22, ϕ(s4)=31, ϕ(s5)=3, ϕ(s6)=2, ϕ(s7)=1, ϕ(s8)=1}.

(a) State the principle of Hoffman encoding briefly. (5%)

➔ **Frequent symbols are assigned shorter codewords**

(b) What is the number of bits in the codeword for symbol s4 if using the basic Hoffman encoding scheme discussed in class? (5%)

➔ **2 bits for s4**

(c) What is the number of bits in the codeword for symbol s4 if using a "conditional Hoffman encoding scheme" which encodes only the symbols with a number of occurrences greater than 20 while leaving the others un-encoded? Use one extra "group bit" in the final codeword to show whether a symbol is encoded or un-encoded. Set the "group bit" to '0' for un-encoded symbols and '1' for encoded symbols. (5%)

➔ **3 bits for s4**