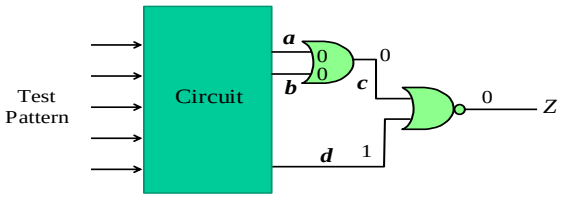
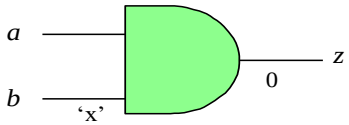
National Tsing Hua University, Taiwan
EE-6250 超大型積體電路測試 (VLSI Testing)
(Closed-Book) Midterm Exam., Fall Semester, 2021 (Nov. 11, 2021)

1. (30%) Answer the following questions.
   (a) What do the variables Y and T represent in the following popularly used estimation formula for modeling the **defect level**: DL = $1 - Y^{(1-T)}$ (5%)
   (b) For a circuit under test with k lines, there is a total of (3^k-1) faulty circuits if considering **multiple stuck-at faults**. Explain why? (5%)
   (c) **IDDQ test** is sometimes referred to as "canary in the coalmine for IC testing". Explain why briefly? (5%)
   (d) A **coupling fault** between two signals means that there is an unexpected "electrical effect" between the two lines so that when one (aggressor) signal is under transition (e.g., going from low voltage to high voltage), it may cause similar effect on its adjacent (victim) signal temporarily (e.g., with a glitch). What is this unexpected electrical effect? Simply answer if it is G (conducting), or C (capacitive), or L (inductive). (5%)
   (e) A decoder's output is supposed to produce a one-hot code at all times. Some may try to test whether this property holds for a fabricated decoder in an IC. For example, consider a test stimulus that will cause only output line $\mathbf{L_i}$ **to high**, but no others. **A fault model f($\mathbf{L_i/L_k}$)** means a faulty condition in which output line $\mathbf{L_k}$ goes high erroneously. Similarly, a fault model **f($\mathbf{L_i}$/0)** means a faulty condition in which no output line goes high at all. Based on this rationale, explain what fault model **f($\mathbf{L_i/L_{i+k}}$)** means. (5%)
   (f) Consider an AND gate with three inputs denoted as $\{x_1, x_2, x_3\}$ and output f. Show the only input combination in terms of $\{x_1, x_2\}$ that satisfies **Boolean difference** df/dx_3. (5%)

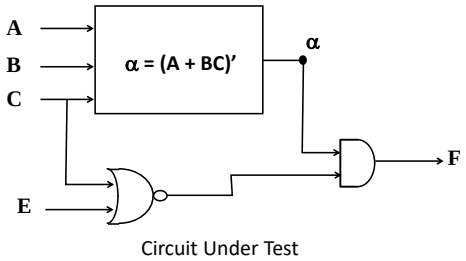
2. (10%) Complete the **deductive fault simulation** as indicated in the figure below to derive the final detected faults by the current test pattern. The fault-free values are {*a*=0, *b*=0, *c*=0, *d*=1, *Z*=0}, respectively.
   (a) Assume that the fault lists at signals *a*, *b*, and *d* have been derived and denoted symbolically as L_a, L_b, and L_d, respectively. Derive the fault list L_c as a formula of L_a and L_b with some union, complement, or intersession operators as discussed in class. (5%)
   (b) Derive the fault list L_z in terms of L_a, L_b, and L_d and some operators. Since Z is a primary output, L_z represents the final detected faults in response to the current applied test pattern. (5%)



3. (10%) Consider a two-input AND gate with two inputs {*a*, *b*} and output {*z*} in a 5-valued D-algorithm for ATPG.
   (a) What can we imply on **signal *b*** after assigning *a* to '1'? (5%)
   (b) Is there anything else we need to do in addition to the above signal value assignment? (5%)



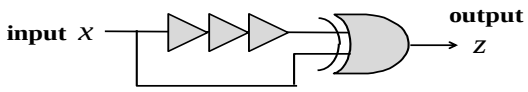
4. (10%) Answer the following questions about testing α stuck-at-1 fault in a circuit under test as shown below, using **5-valued D-algorithm**.
   (a) Derive the necessary signal value requirements on primary inputs C and E. (5%)
   (b) Represent all possible input patterns that can detect this fault as one **3-valued test pattern** in terms of (A, B, C, E). Use 'X' to denote a don't-care bit in your result. (5%)



5. (10%) Consider the **9-valued D-algorithm**.
   (a) In addition to {0, 1, X, D, D'} used in a traditional 5-valued D-algorithm, what other 4 values (that could be assigned to a signal during the ATPG process) are added in a 9-valued D-algorithm. (5%)
   (b) Consider an AND gate, *f*=ABC. For activating A-stuck-at-0 fault and propagate the fault effect across the AND gate to its output *f*, what 9-valued requirement is needed at B? (5%)

6. (10%) Answer the following questions about **test time**.
   (a) Why is test time important in VLSI testing? (5%)
   (b) Consider the full-scan methodology for a circuit with 99 flip-flops. A combinational ATPG program produces 123 vectors to fully test the logic. Compute the minimum number of clock cycles needed to apply these vectors, assuming that the system clock and test clock are the same and there is only one scan chain. (Note: the scan-in operation and scan-out operation are assumed to be overlapped whenever possible. In this calculation, we also ignore the cycles for applying the PI sub-vectors and the cycles for observing the PO sub-vectors.) (5%)

7. (10%) Consider the testing of a mono-stable multi-vibrator circuit (also known as *one-shot circuit*) as shown below.
   (a) Within a particular test clock cycle, we apply a low-to-high rising transition to the input signal. **Show the waveform of the output signal if the circuit is fault-free**. (5%)
   (b) To detect if the circuit is faulty or not, we can simply use a *"fault-detection circuit"* with only one "reset-able edge-triggered flip-flop". Note that this flip-flop is assumed to have been reset to '0' at the beginning of the test clock cycle and its output is assumed to be observable. **Show the** *"fault-detection circuit"* **properly connected to the circuit under test**. (5%)



8. (10%) Consider a LSSD design discussed in class.
   (a) Complete the LSSD design shown below. (5%)
   (b) The operational mode of this LSSD is not decided by a control signal like SC as in a MUX scan cell. Instead, it is decided by the clock waveforms of {CK1, CK2, CK3}. Draw typical clock waveforms of CK1, CK2 and CK3 when performing scan operation in the test mode. Hint: only one of the 3 clock signals can be active (or at a high voltage) at any given time. (5%)