清華大學 電機工程學系 碩博士班 111 學年度第二學期, Spring 2023

EE-6250 超大型積體電路測試 (VLSI Testing)

教師: 黃錫瑜 Shi-Yu Huang (syhuang@ee.nthu.edu.tw)

教材請上【國立清華大學-eeclass數位學習系統】https://eeclass.nthu.edu.tw/ 下載

上課時間與地點： 星期一 6:30-9:20pm @台達館 216 教室

若須採線上課程: https://meet.google.com/iip-jugm-tka

1. 課程說明 (General Description)

This course is devoted to the fundamental knowledge of testing Very Large-Scale Integrated circuits (VLSI). The emphasis is on the investigation of various technically feasible test solutions combining both Design-for-Testability hardware and Computer-Aided Design algorithms for test-pattern generation to make sure the overall testability and quality of manufactured ICs. It begins with the topics of fault modeling and fault simulation, followed by the algorithms of Automatic Test Pattern Generation (ATPG). Then, widely adopted Design-for-Testability (DFT) techniques in IC design industry, such as Scan Test, Built-In Self-Test (BIST), Test Compression, and IEEE-1149.1 Boundary Scan Test Standard will be elaborated. At the final stage, some selective advanced topics such as power & clock networks testing and logic fault diagnosis will also be discussed. Upon the completion of this course, the students will know how to apply all kinds of test solutions to make an IC easily testable and reliable in a cost-effective way.

2. 助教 (TAs) @ 台達館 923 實驗室

賴淇(chilai.asdf@gmail.com) 許志嘉(jesse16180@gmail.com) 鄧向凱(stan888957@gmail.com)

3. 先修課程 (Prerequisites)

程式設計，邏輯設計，積體電路設計導論

4. 修完此課程後之效益 (Benefits After Taking this Course)

Students who have taken this course will become knowledgeable about state-of-the-art VLSI test and diagnosis technologies that are often mandatory if working as an IC designer and/or IC testing or product engineer in the industry.

5. 主要參考書 (Textbook):

- L.-T. Wang, C.-W. Wu, and X. Wen, "VLSI Test Principles and Architectures: Design for Testability," Morgan Kaufmann, July 2006.

6. 教學方式 (Teaching Method)

以使用 PowerPoint 投影片為主的課堂討論 (Lectures using PowerPoint Slides)

7. 成績考核: 課堂出席情況 5%，作業 (實作型) 30%，期中考 30%，期末考 35%

8. 教學大綱 (Course Outline)

1. Introduction
2. Fault Modeling
3. Fault Simulation
4. Design-for-Testability (DFT) and Scan Test
5. Automatic Test Pattern Generation (ATPG)
6. Delay Test
7. Built-In Self-Test (BIST)
8. Test Compression
9. Boundary Scan Test
10. Testing Clock and Power Network
11. Fault Diagnosis
12. Scan Chain Diagnosis using Artificial Neural Network

A1: Review of Digital Circuit Design Methodology

A2: Quick-and-Cool Scan Test Methodology

A3: Optimization by Branch-and-Bound Search

9. 考試資訊: (上課教室) 6:30-8:10pm, Midterm Exam. on April 17, 2023, Final Exam. on June 12, 2023.

10. 進度表 (Schedule)

Feb. 20, 2023 先由助教播放錄影課程，複習 Cell-based design tools。

April 24, 2023 先由助教擔任 Tutorial 講師，介紹 Test Tool (Scan Insertion + ATPG) 之使用方式。

Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Month	Feb. 2023			March 2023				April 2023				May 2023					June 2023	
Date 星期一	13	20	27	6	13	20	27	3	10	17	24	1	8	15	22	29	5	12
預估進度	C1	C2	放假日	C3	C4	C5	C5	放假日	C6	期中考	C7	C7	C8	C9	C10	C11	C12	期末考