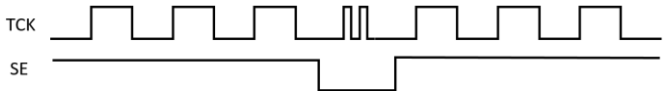
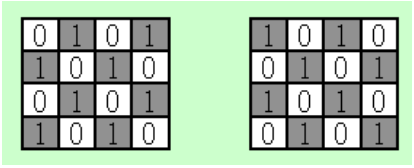
**國立清華大學 電機工程學系碩博士班**
**110 學年度第一學期**
**EE-6250 超大型積體電路測試 VLSI Testing**
**期末考 Jan. 13, 2022 (總分 100 分)**
**(Closed-Book Examination)**

1. (20%) Answer the following questions briefly.
   (a) Draw the **test clock signal** (TCK) and **Scan Enable** (SE) **waveforms** for supporting a typical **Launch-off-Capture (LoC)** delay test for a full-scan design with only 3 FFs. We assume that the FFs perform scan-shifting when SE is '1' and perform normal operation when SE is '0'. (Note that the delay test application can be viewed as a procedure consisting of 4 phases - scan-in, launch, capture, and scan-out). (5%)




   (b) Show the two **checkerboard test patterns** for a 4x4 memory cell array as discussed in class. Under these test patterns, bridging faults or coupling faults among bit cells are more likely to be activated and tested. (5%)



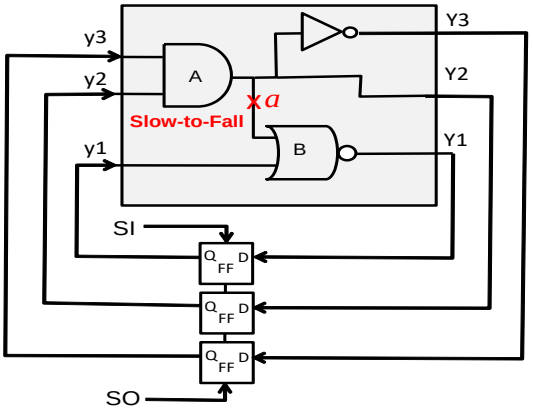

   (c) Logic BIST often employs pseudo-random test patterns and so the **fault coverage** may sometimes **insufficient**. In order to boost the fault coverage, some people may try to enhance it with additional stored ATPG patterns. In addition to that, what other method is also often used? (5%) ➔ Inserting test points.
   (d) Sometimes a fault diagnosis tool will report just a handful of fault candidates (or fault suspects). What is the **number of reported fault candidates** often referred to? Diagnostic resolution, success rate, first-hit index, or top-10 hit number? (5%) ➔ Diagnostic resolution

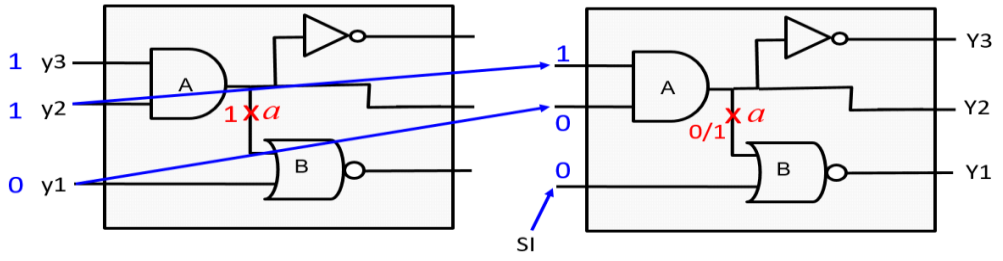
2. (15%) Answer the following questions about **delay test** for a full-scan design as shown below. There are three FFs, with the present-state lines denoted as {y1, y2, y3} and next-state lines as {Y1, Y2, Y3}. The scan chain order is (SI→y1→y2→y3→SO). We wish to generate a two-pattern test, denoted as (v1, v2), for "slow-to-fall fault at a branch signal *a*".

   (a) Assuming the **LoS (Launch-off-Shifting)** method, what is the basic logical relationship between the first vector v1 and the second vector v2? (5%) ➔ v2 is a one-bit shifting version of v1.

   (b) Draw a 2-time-frame expansion model for delay test generation while imposing the above LoS constraint on the model. (5%)

   (c) There is only one two-pattern test (v1, v2) for "slow-to-fall fault at a branch signal *a*". Derive it. Note that you have to show v1 and v2 clearly, in terms of their values associated with {y1, y2, y3}, respectively. (5%) ➔v1: (y1, y2, y3) = (011), v2: (y1, y2, y3) = (001).



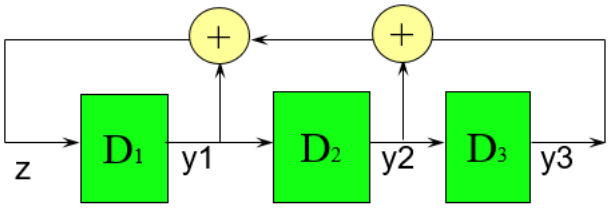




2-pattern-test for "slow-to-fall fault at *a*" using LoS:
Assign *a* to '1' in the 1st time frame and test *a* stuck-at-1 in the 2nd time frame
(SI, y1, y2, y3) = (0, 0, 1, 1)
➔ v1: (y1, y2, y3)=(0, 1, 1) and v2: (y1, y2, y3)=(0, 0, 1)

Answer 2(b) and 2(c)

3. (15%) Answer the following questions related to **LFSR**.
   (a) Consider a LFSR with a characteristic polynomial $g(x) = (x^2+1)(x+1)$. Drive its out-tap architecture with FFs and XOR gates. Denote the FFs along the shift registers as y1, y2, and y3, respectively. (5%)
   (b) View this LFSR as a finite state machine, with present-state as a column vector $(y1, y2, y3)^T$, and the next-state as a column vector $(Y1, Y2, Y3)^T$. Show matrix $A_{3x3}$ in the following a matrix equation
   $$(Y1, Y2, Y3)^T = A_{3x3} \times (y1, y2, y3)^T.$$
   (c) Operate this LFSR from a seed (y1, y2, y3) = (1, 0, 0). How many distinct patterns in terms of the contents of the 3 FFs can be produced at the most? (5%) ➔ 4 distinct patterns, {(100), (110), (011), (001)}.

$$g(x) = (x^2+1)(x+1) = x^3+x^2+x+1$$




Answer 3(a) – out-tap architecture for the LFSR

$$\begin{bmatrix} Y1 \\ Y2 \\ Y3 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \times \begin{bmatrix} y1 \\ y2 \\ y3 \end{bmatrix}$$

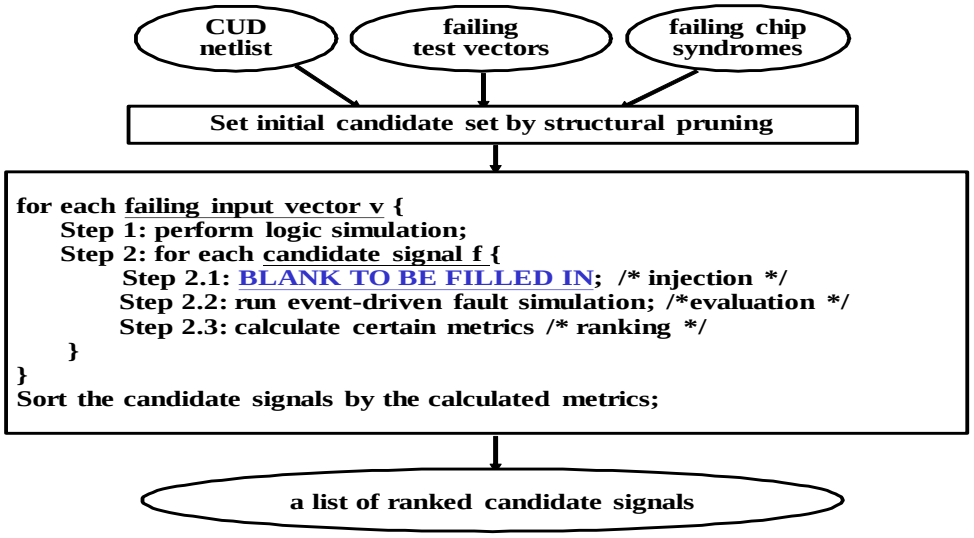
$A_{3x3}$

Answer 3(b) – Matrix form for the next-state-line function

4. (15%) Consider the following **Test Compression** problem.
   (a) Name one advantage of using test compression. (5%) ➔ Reduce the **test data volume**, reduce the **test time**, or reduce the **test memory requirement of the ATE**. (回答其一即可)
   (b) Golomb code is an improved zero-run-length code for test compression. Find the original test sub-pattern represented by a Golomb code of "11011", assuming that there are two tail bits. (Hint: For example "1001" denotes the 2nd pattern in group A2, which corresponds to an original sub-pattern of "000001".) (5%) ➔ "11011" is the Golomb code the 4th pattern in group A3, which is "000000000001"('1' trailing 11 '0s')
   (c) Find the maximum compatible set among the following five test sub-patterns, {A=(XXX00), B=(X0X10), C=(1XXX0), D=(X1XXX), E=(XX1XX)}. (Hint: Draw the compatibility graph first and then find the largest clique). (5%)➔{A, C, D, E} are the maximum compatible set.

5. (15%) Consider the **modified flush-test for Clock Delay Fault (CDF)** as discussed in class. Consider a scan chain with only 4 flip-flops, ordered as SI→F1→F2→F3→F4→SO. The modified flush-test will take 3 stages – namely (Stage 1) scan-in procedure of an alternating patterns "0101" into the scan chain, and thereby setting up (F1,F2,F3,F4)=(0101), (Stage 2) fault excitation cycle with the SI being '1', and (Stage 3) a scan-out procedure of the contents of the scan chain.
   (a) Name one unique feature of the test clock signal during stage 2 as compared to those in stage 1 and stage 3. (5%) ➔ A clock cycle with a short pulse-width
   (b) If there is a CDF affecting flip-flop F2 and the applied modified flush test is assumed to be able to trigger the fault, then what output bit-stream one will observe at the output SO pin of the scan chain? Order the bit-stream in a way that the rightmost bit is the first bit observed. (5%) ➔ 1110
   (c) In some sense, this test method can characterize the clock routing path from the clock source pin to each FF as a number called $P_{min}$. A FF with excessively large $P_{min}$ tends to have a CDF. What does $P_{min}$ stand for? (5%) ➔ $P_{min}$ stands for "minimum passing pulse-width".

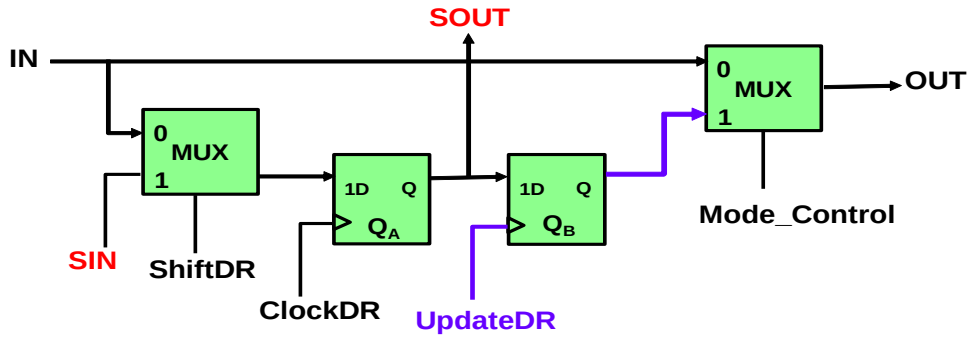
6. (10%) Consider the **logic diagnosis** problem.
   (a) In the following pseudo code for inject-and-evaluation paradigm, fill in the missing blank. (5%) ➔ Flip the value at *f*
   (b) Suppose that *v* is found to be a curable vector of a signal *f*, explain what it means. (5%) ➔ After the injection at signal *f*, the response of circuit model becomes exactly the same as that of the failing chip.



7. **(10%) Consider the IEEE 1149.1 Boundary Scan Test** Problem.

(a) Draw the circuit diagram of a Boundary Scan Cell (BSC) with 2 D-type flip-flip, $Q_A$ and $Q_B$, and 2 MUXes. Mark clearly the following signals {IN, OUT, SI, SO, ShiftDR, ClockDR, UpdateDR}. (5%)

(b) Consider 3 BSCs used to drive 3 output pins of a chip. Then, we wish to launch (010) combination to test these 3 output pins, then, we should scan in this pattern into the 3 BSCs first through a sequence of scan shifting cycles. After that, we launch them simultaneously in a clock cycle. At this moment, what type of signals should be assigned to the control signals {ClockDR, UpdateDR} of each of the 3 BSCs, respectively? The signal type could be '0', '1', 'stable', or 'rising edge'. (5%) ➔ {ClockDR is 'stable', UpdateDR is 'rising edge'}




Answer 7(a) – Boundary Scan Cell