Hw2

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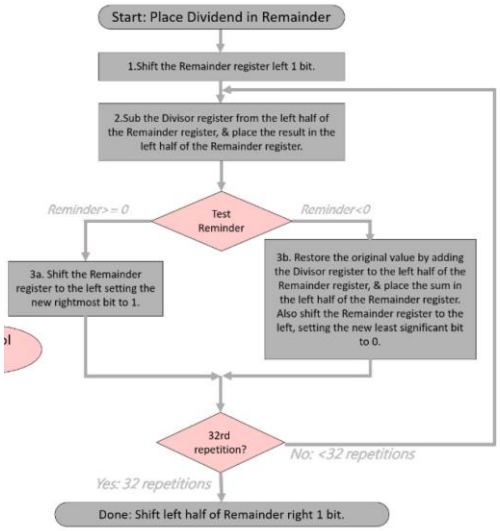
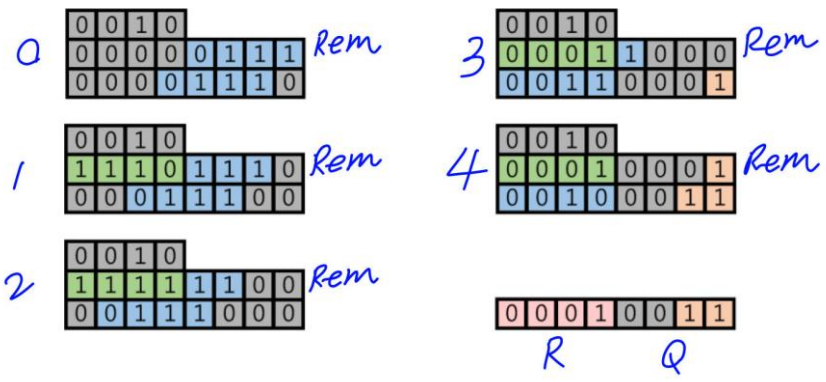
1. Write the RTL code in Verilog or VHDL that takes in two 8-bit positive integers, A[7:0]and B[7:0],and produces its quotient Q[7:0] and remainder R[7:0].

   Verilog code 如附件。

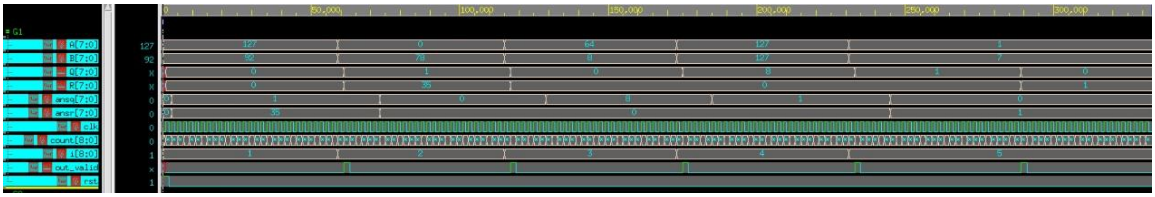
   此次是使用硬體最佳化除法，將餘數和商放在同個暫存器中，首先開出一個16bits的暫存器，將被除數放入[0:7]，接著向前進一位，並將[8:15]減去除數並檢查是否為正 i.e (MSB是否為0)。
   如果為負，就把原本還沒減過的16bits暫存器往右移1個bit。
   如果為正，則暫存器往右移1個bit並且加1。

   最後暫存器中[0:7]為商，暫存器[8:15]要往左移1個bit才是餘數。
   以下是flow chart以及一個4bits的小範例

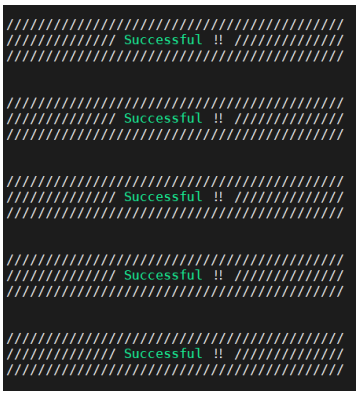




2. Verify the correctness of your RTL code by a testbench. You should try it out by at least 3 pairs of input numbers.



Testbench 測試資料為(127、92) (0、78) (64、8) (127、127) (1、7)。
由模擬可得知，5 個測資均為正確，並且沒有 time violation



3. Use asynthesis script to convert your RTL code into a gate-level netlist.Report the final gate count, the maximum operating speed(in MHz) and the estimated power dissipation in (mW) using *Design Compiler*.

Netlist檔如附件。

```
Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /home/m110/m110061576/process/CBDK_TSMC90GUTM_Arm_f1.0/orig_lib/aci/sc-x/synopsys/slow.db)

Number of ports:                           93
Number of nets:                           424
Number of cells:                          352
Number of combinational cells:            292
Number of sequential cells:                56
Number of macros/black boxes:               0
Number of buf/inv:                         78
Number of references:                      57

Combinational area:               1152.244832
Buf/Inv area:                      173.577605
Noncombinational area:             915.163191
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  2067.408023
Total area:                 undefined
1
```

```
Global Operating Voltage = 0.9
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 937.4755 uW   (94%)
  Net Switching Power  =  62.5234 uW    (6%)
                         ---------
Total Dynamic Power    =   1.0000 mW  (100%)

Cell Leakage Power     =   7.2373 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000           0.0000  (   0.00%)
register           0.8752        1.1256e-02          3.0287e+06           0.8895  (  88.31%)
sequential         0.0000           0.0000              0.0000           0.0000  (   0.00%)
combinational   6.2309e-02        5.1267e-02          4.2087e+06           0.1178  (  11.69%)
--------------------------------------------------------------------------------------------------
Total              0.9375 mW     6.2523e-02 mW     7.2373e+06 pW         1.0072 mW
1
```

```
 Startpoint: curr_state_reg_1_
             (rising edge-triggered flip-flop clocked by clk)
 Endpoint: remc_reg_8_
           (rising edge-triggered flip-flop clocked by clk)
 Path Group: clk
 Path Type: max

 Point                                          Incr       Path
 -----------------------------------------------------------------
 clock clk (rise edge)                          0.00       0.00
 clock network delay (ideal)                    0.00       0.00
 curr_state_reg_1_/CK (DFFHQX4)                 0.00       0.00 r
 curr_state_reg_1_/Q (DFFHQX4)                  0.11       0.11 f
 U222/Y (NOR2X2)                                0.06       0.17 r
 U374/Y (NOR2X2)                                0.03       0.20 f
 U236/Y (OR2X4)                                 0.06       0.26 f
 U262/Y (OR2X2)                                 0.09       0.35 f
 U239/Y (OR3X4)                                 0.11       0.47 f
 U220/Y (CLKINVX8)                              0.04       0.51 r
 remc_reg_8_/E (EDFFTRX1)                       0.00       0.51 r
 data arrival time                                         0.51

 clock clk (rise edge)                          0.91       0.91
 clock network delay (ideal)                    0.00       0.91
 remc_reg_8_/CK (EDFFTRX1)                      0.00       0.91 r
 library setup time                            -0.40       0.51
 data required time                                        0.51
 -----------------------------------------------------------------
 data required time                                        0.51
 data arrival time                                        -0.51
 -----------------------------------------------------------------
 slack (MET)                                               0.00
```

gate count
2607.4/2.8224=923.82

maximum operating speed
1/0.91=1.1GHz

estimated power dissipation
1.0072mW

4. Add the scan chain into your gate-level netlist obtained by part(c), report the resulting gate count, the maximum operating speed (in MHz) of your circuit. Compare to the non-scan version, and report the area overhead percentage and performance penalty due to scan chain insertion.

```
****************************************
Report : area
Design : div
Version: R-2020.09-SP5
Date   : Sun May 14 16:34:47 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /home/m110/m110061576/process/CBDK_TSMC90GUTM_Arm_f1.0/orig_lib/aci/sc-x/synopsys/slow.db)

Number of ports:                          95
Number of nets:                          434
Number of cells:                         352
Number of combinational cells:           292
Number of sequential cells:               56
Number of macros/black boxes:              0
Number of buf/inv:                        78
Number of references:                     58

Combinational area:               1176.235233
Buf/Inv area:                      173.577606
Noncombinational area:            1284.191990
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  2460.427223
Total area:                 undefined
```

```
Global Operating Voltage = 0.9
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.2552 mW   (95%)
  Net Switching Power  =  68.6089 uW    (5%)
                         ---------
Total Dynamic Power    =   1.3238 mW  (100%)

Cell Leakage Power     =   8.9942 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register           1.1885        1.9612e-02          4.6647e+06             1.2128  (  91.00%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational   6.6690e-02        4.8997e-02          4.3296e+06             0.1200  (   9.00%)
--------------------------------------------------------------------------------------------------
Total              1.2552 mW     6.8609e-02 mW     8.9942e+06 pW          1.3328 mW
1
```

```
Startpoint: curr_state_reg_1_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: rem_reg_1_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                     Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                     0.00       0.00
clock network delay (ideal)               0.00       0.00
curr_state_reg_1_/CK (SDFFHQX4)           0.00       0.00 r
curr_state_reg_1_/Q (SDFFHQX4)            0.12       0.12 f
U53/Y (NOR2XL)                            0.09       0.20 r
U379/Y (OR2X2)                            0.09       0.29 r
U384/Y (OAI2BB1X4)                        0.09       0.38 r
U12/Y (NAND2BX4)                          0.04       0.42 f
U266/Y (OR2XL)                            0.15       0.57 f
U297/Y (INVX2)                            0.06       0.63 r
U325/Y (AOI22XL)                          0.09       0.73 f
U59/Y (OAI2B11X1)                         0.06       0.79 r
rem_reg_1_/D (SDFFHQX8)                   0.00       0.79 r
data arrival time                                    0.79

clock clk (rise edge)                     0.91       0.91
clock network delay (ideal)               0.00       0.91
rem_reg_1_/CK (SDFFHQX8)                  0.00       0.91 r
library setup time                       -0.12       0.79
data required time                                   0.79
-----------------------------------------------------------
data required time                                   0.79
data arrival time                                   -0.79
-----------------------------------------------------------
slack (MET)                                          0.00
```

area overhead percentage

2607.4/2460.4=106.08%

maximum operating speed

1/0.91=1.1GHz

estimated power dissipation

1.3328mW

performance penalty

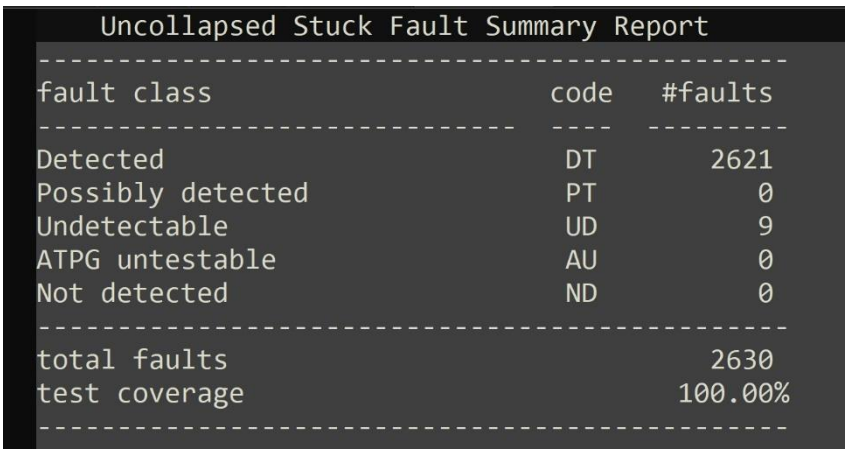
有沒有加scan chain的CLK period都相同，所以無performance penalty

可發現加了scan chain之後power跟area，不過疑惑的是timing沒有增加

所以沒有performance penalty

值得注意的是，asynchronous reset是不能加上scain chain的，必須要synchronous reset，這點非常疑惑

5. Run ATPG using a commercial tool available and report the fault coverage.



Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	2621
Possibly detected	PT	0
Undetectable	UD	9
ATPG untestable	AU	0
Not detected	ND	0
total faults		2630
test coverage		100.00%

組員分工:

111061642王煒翔:理解演算法、寫RTL、testbench、尋找最高速度、debug、撰寫一部分的報告 (50%)

111061622薛仲勛:理解演算法、跑後續DFT的流程、撰寫一部分的報告 (50%)