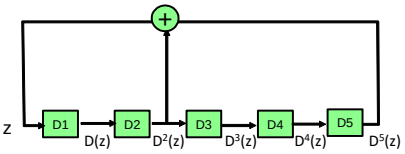
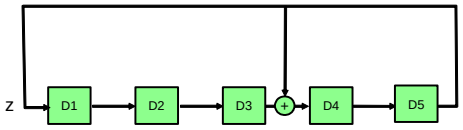
國立清華大學 電機工程學系碩博士班
111 學年度第二學期
EE-6250 超大型積體電路測試 VLSI Testing
期末考 June 12, 2023 (總分 100 分)
(Closed-Book Examination)

REFERENCE ANSWERS

1. (15%) Consider the **Liner-Feedback Shift-Register** problem.
   (a) There are two basic requirements to produce (2^n-1) **pseudo-random patterns** using an n-stage LFSR. One of them is to choose an LFSR with a primitive (or irreducible) polynomial. Name the other requirement. (5%)
   ➔ Use non-zero SEED
   (b) Draw an out-tap structure of the following LFSR with a characteristic polynomial of $p(x) = x^5 + x^2 + 1$. (5%)
   (c) Draw an in-tap structure of the following LFSR with a characteristic polynomial of $p(x) = x^5 + x^2 + 1$. (5%)

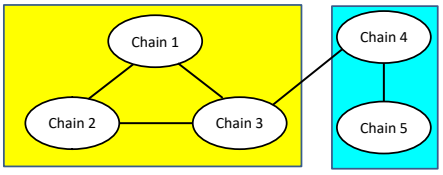


(b) out-tap structure for $p(x)=x^5+x^2+1$



(c) in-tap structure for $p(x)=x^5+x^2+1$

2. (10%) Consider a broadcast scan for test compression. A test pattern is composed of 5 sub-patterns (one for each of 5 scan chains): {Chain1=(101XX), Chain2=(XX10X), Chain3=(XXX0X), Chain4=(0X0X1), Chain5=(XX01X)}.
   (a) Draw a **compatibility graph** to describe the compatibility relations among these five sub-patterns. (5%)
   (b) If the broadcasting scan test is applied, then we can use only two **common sub-patterns** to fill out all 5 scan chains for this particular test pattern. If one of the common sub-pattern is (1010X), what is the other? (5%)

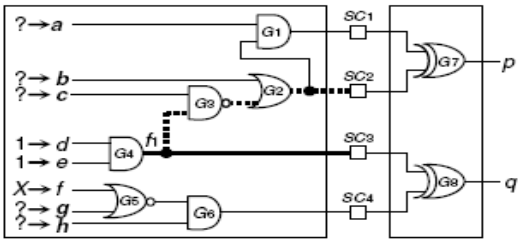


(a) Compatibility Graph

(b) 2nd common sub-pattern for Chain 4 and Chain 5 is (0X011)

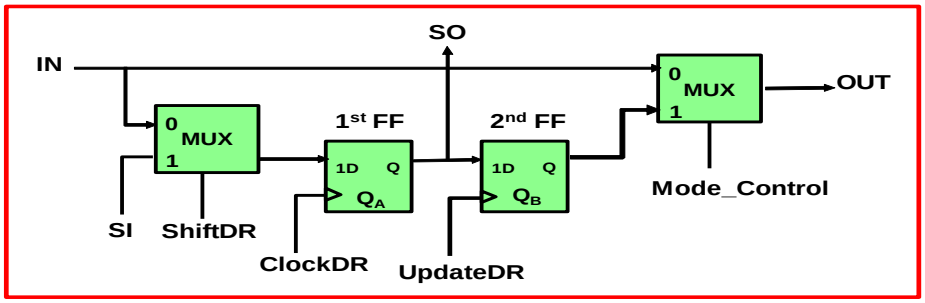
3. (10%) Consider the "output unknown" problem arising in the following circuit, where {SC1, SC2, SC3, SC4} are original scan chain outputs, while 'p' and 'q' are compacted outputs. ATPG is performed to detect 'f1-stuck-at-0' fault. Value assignments {d=1, e=1} have been made to activate the fault. We assume that there is an unknown value at input 'f', denoted as 'X', due to an unscanned flip-flop or bus signal.
   (a) If ('g', 'h') are assigned to ('0', '1') in the test pattern, what will we get at 'q' during the 5-valued fault simulation, {0, 1, X, D, D'}? Does it mean that we can have a conclusive fault effect, i.e., {D or D'}, at 'q'? (5%) ➔ X' or X, implying that we CANNOT have a conclusive fault effect at 'q'.

(b) What value can be assigned to signal 'g' to resolve this output-known problem? (5%) ➔*g*= 1(to block the 'X' source at *f*)



4. (10%) Consider the following **Power Network Testing** as discussed in class.
   (a) When the ring oscillator is used as a monitor in a circuit, its output clock waveform is analyzed to reflect the PVTA effect at the monitor site. Ignore the aging effect and assume that we have built a **process-specific ROCP (Ring Oscillation Clock Period) model** that describes how the temperature and the VDD affect the ROCP of the current RO-based monitor. How can we predict the temperature at the monitor site first? Please state your answer in terms of two parts – the operating condition and the metric to be measured by the CPM (clock period measurement) circuit for performing the inferencing on the process-specific ROCP model. (5%)
   ➔ To place the **IC in the idle mode**, **while measuring the average ROCP** for predicting the temperature.
   (b) Once the temperature at the monitor site has been determined, we can move on to derive the maximum VDD drop over a monitoring session. What metric is to be measured by the CPM circuit for this purpose for performing the inferencing on the process-specific ROCP model? ➔ **The largest (or worst-case) ROCP** which can be mapped to the worst-case VDD level on the process-specific ROCP model.

5. (15%) Consider the **IEEE 1149.1 Boundary Scan Test** Problem.
   (a) There are five IO signals, {TCLK, TRST, TDI, TDO, and TMS}. Which one is the main signal to determine the state transition of the TAP controller? (5%) ➔ TMS
   (b) Draw the circuit diagram of a Boundary Scan Cell (BSC) with 2 D-type flip-flop, with their output named Q_A and Q_B, and 2 MUXes. Mark clearly the following signals {IN, OUT, SI, SO, ShiftDR, ClockDR, UpdateDR, Mode_Control}. (5%)
   (c) There are three operation modes for a BSC, namely "Normal", "Scan", "Capture", and "Update". What is required of {ShiftDR, ClockDR, UpdateDR, Mode_Control} to enforce an "Update mode"? (Note a signal could have no requirement, denoted as 'x', or a requirement of '0', '1', 'stable', or 'rising edge'.). (5%)
   ➔ {ShiftDR, ClockDR, UpdateDR, Mode_Control} = {'x', 'stable', 'rising edge', '1'}.

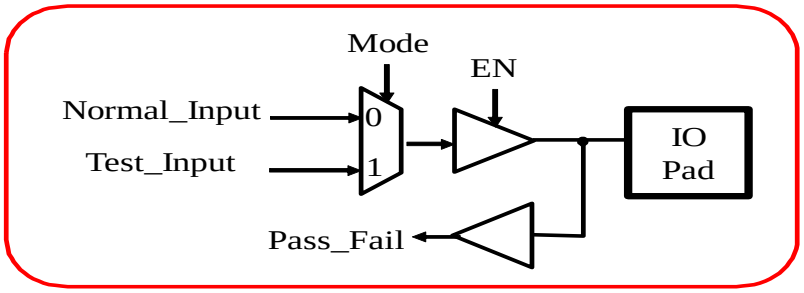


Answer (b)

6. (10%) Consider the **IO Leakage Test** Problem discussed in class.

(a) The entire test procedure is denoted as CAF-WAS or Charge-and-Float Wait-and-Sample. Draw the basic DfT circuit for an IO pad, including 1 MUX, 1 tri-state buffer, and 1 buffer gate. Denote the IO pad under test as a square box. Label the Input signals including {Normal_Input, Test_Input, Mode, EN} and the output signal {Pass_Fail}. When 'Mode' is '1'. The circuit is in test mode. Otherwise, it is in the normal mode. At the end of the test, the test result is at the output signal "Pass_Fail". Signal 'EN' turns on the tri-state buffer when it is '1'. (5%) ➔ As shown below.

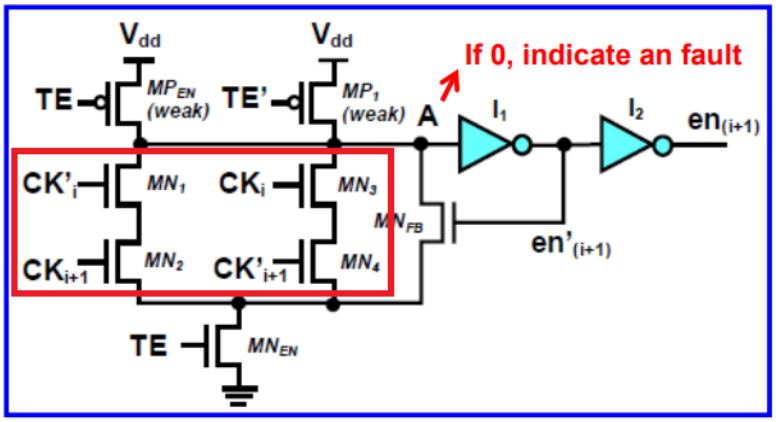
(b) Consider the testing of excessive leakage to the ground from the IO pad. During the Charge stage, we set (Test_Input, Mode, EN) = (1, 1, 1). After a while when the charge to VDD is complete, we turn off the tri-state buffer by setting EN to '0'. Then we wait for a certain amount of time before sensing the IO pad's voltage into a logic level through the buffer gate. **How many test clock cycles should we wait** when the test clock is 1MHz after the tri-state is turned off if the average leaking threshold is 1uA, while assuming the following parameters: the capacitance at the IO pad is 4pF, the VDD is 1V, and the switching threshold is 0.5V for the sensing buffer gate. (5%) ➔ (4pF*0.5V)/1uA = 2us, which is 2 test clock cycles of 1MHZ test clock.



Answer (a)

7. (15%) Consider the following **Clock Network testing** as discussed in class.

(a) Intel proposed a Duty-Cycle Error Detect and Latch (DCEDL) circuit for clock skew detection. It is used between two key clock points in the clock network. The output will become '0' when the skew of the two key clock points, e.g., CK1 and Ck2 in the figure, is larger than a threshold, say 30ps. Complete the schematic by filling in the missing **pull-down network** consisting of 4 nMOS transistors. Note that both positive and negative signals of CK1 and CK2 are available inputs to the pull-down network. (5%)



Answer 7.(a)

(b) If we want to make the DCEDL even more sensitive by reducing the test threshold even further, e.g., from 30ps to 10ps, should we increase or decrease the sizes of the pull-down network? (Note that increasing the size of the pull-down network will increase its driving strength of the output). (5%) ➔**Increase the sizes of the pull-down network**, so the DCEDL will latch to the failed state, i.e., A becomes '0', more easily.

(c) We also discussed in class a **modified flush test** for detecting a Clock Delay Fault (CDF) in the clock network. It incorporates a scan-excite-scan process. The scan-in and the scan-out are the same as the traditional flush test. The only difference is the "excite cycle". Describe the key feature of the "excite cycle". (5%) ➔Use a **short-pulse signal in the test clock signal** for the "excite cycle" to trigger the CDF effect since the FF affected by the CDF fault may not be able to receive the short-pulse signal.

8. (15%) Consider the **software-based chain diagnosis** for a faulty scan chain as shown below.

(a) During a flush-in stage with a bitstream of (00000000) with the rightmost bit going to a faulty scan chain first. What is the snapshot image (F1, F2, …, F8) if there is a stuck-at-1 fault at F3? (5%) ➔(F1, F2, …, F8)=(00111111)

(b) Now let us apply one "capture cycle". Assume that there are many other scan chains that are all fault free. Due to the interaction with these other scan chains, the "captured snapshot image" of the faulty scan chain could become very different, e.g., assumed to be (F1, F2, …, F8) = (10010001). The two bits marked with underlines are faulty. After we scan out this captured snapshot image, what observed image we will get at the SO pin, assuming that the rightmost bit comes out of the scan chain first? Indicate each faulty bit in the observed image with an underline. Note that F3 is stuck-at-1. (5%) ➔ The observed image is (11110001)

(c) Let us apply 1000 ATPG patterns with the above scan-capture-scan test procedure and derive the **faulty probability profile** of the faulty scan chain as (0.4, 0.33, 0.66, 0.01, 0.02, 0.05, 0.03, 0.01). Take the faulty probability of F1 for example, it is calculated as 0.4 to indicate that the F1 bit is faulty in 40% of the 1000 observed images. By examining this faulty probability profile, what reason can lead us to believe that F3 is very likely to be the fault site in this faulty scan chain? (5%) ➔ The upstream part (i.e., from SI to F3) has a high faulty probability, while the downstream part (from F3 to the SO) is mostly fault-free.