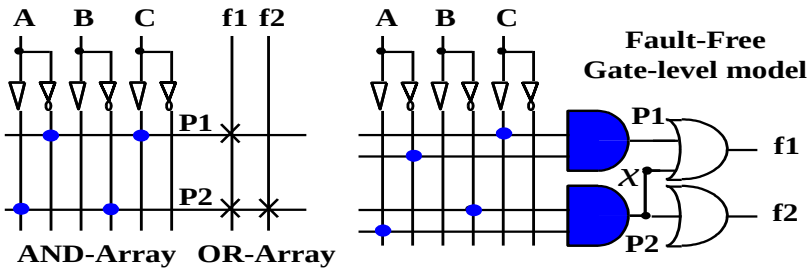
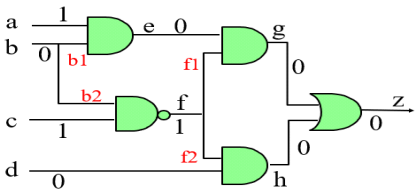
National Tsing Hua University, Taiwan
EE-6250 超大型積體電路測試 (VLSI Testing)
(Closed-Book) Midterm Exam., Fall Semester, 2023 (April 17, 2023)
(七大題，總分 100 分)

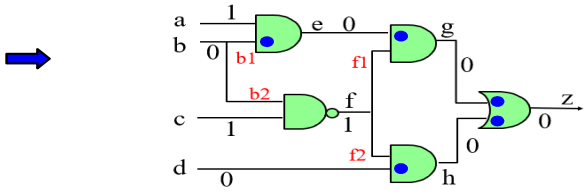
1. (10%) Answer the following questions.
   (a) Consider three stuck-at faults, {f_1, f_2, f_3} for a circuit under test. Assume that f_1 dominates f_2 and f_2 dominates f_3. By the transitive rule, we know f_1 dominates f_3 as well. If your manager asks you to define a priority order for these 3 faults during the ATPG, what priority order would you suggest? Provide the reason(s) for your answer. (5%) ➔ {$f_3 \rightarrow f_2 \rightarrow f_1$} The dominated faults are targeted first for ATPG. This may have a benefit to detecting the other easier faults that dominate it by the way.
   (b) Consider a NOR gate realizing $z=(a+b)'$. What dominance relations you can derive among the 6 stuck-at faults {*a-sa-0*, *b-sa-0*, *z-sa-1*}? (Hint: you can use any technique to derive the answer. One technique is to list the fault-free function and the faulty functions of the 6 stuck-at faults first. Then, the complete test set for each fault can be derived to find out the dominance relations among the 6 faults). (5%) ➔ z-stuck-at-1 dominates a-sa-0, and b-sa-0
2. (15%) Consider the fault modeling of a PLA with the symbolic schematic shown below. Note that product line P2 has two branches, the one driving output line f1 is particularly called *x* (as shown in the right-hand-side of the figure below).
   (a) Derive the fault-free Boolean function for output signal f1 of this PLA in the Sum-of-Product (SoP) form (5%). → f1 = A'C + AB'
   (b) On the left-hand side of the figure, if there is a missing cross-point fault at the cross-point of (vertical) input line A' and (horizontal) product line P1, then what is the faulty Boolean expression for output signal f1, (Note: denote the name of this faulty signal as f1-faulty? (5%) → f1-faulty = C + AB'
   (c) On the left-hand side of the figure, if there is a missing cross-point fault at the cross-point of (horizontal) product line P2 and (vertical) output line f1, then what stuck-at fault is this fault equivalent to on the circuit model on the right-hand-side? (Note: you have to specify the equivalent faulty signal name and the stuck-at value). (5%) → x stuck-at-0



3. (15%) Consider the technique of **critical-path tracing for fault simulation** based on the simulation results in response to an input vector (a,b,c,d)=(1,0,1,0) as shown below.
   (a) Draw the circuit on your answer sheet and mark every *sensitive input* of each gate with a dot like in the lecture notes. (5%) ➔ As shown below.
   (b) Derive the *critical lines*. Note that the critical-path tracing traverses the circuit from the outputs toward the inputs and stops whenever a stem is encountered. (5%) ➔ {g, h, e, b1, d}
   (c) Derive the *set of faults that can be detected* based on the information derived in (b). Follow the branch notations as shown in the figure. The faults on the primary inputs should also be considered. (5%) ➔ {g/1, h/1, e/1, b1/1, d/1}



Sensitive Inputs



4. (10%) Consider a circuit realizing a Boolean function, $f = (ab + c)$.
   (a) Derive the Boolean difference df/db. Express your answer as a Boolean expression. (Note: you can derive it by any technique.) (5%) ➔ ac'
   (b) Derive the only test pattern for *b* stuck-at 0. (5%) ➔ (a, b, c) = (1, 1, 0)

5. (20%) Consider the following questions related to the 5-valued D-algorithm for ATPG.
   (a) When a signal is labeled as D or D', it is referred to have a fault effect. What does D' mean? ➔ D' means **'0/1'**, or it is required to have a value of 0 in the fault-free circuit, and a value of '1' in the faulty circuit.
   (b) During the execution of the D-algorithm for a specific stuck-at fault, an AND-gate's output, signal *f*, has an assignment of '0' and is included in the J-frontier. What can you say about the inputs of this AND gate at this moment? ➔ Since *f* is in the J-Frontier, it is NOT JUSTIFIED YET. It follows that **none of this AND gate's input signals is a controlling value of '0'**.
   (c) There are two types of "decisions" in the D-algorithm. The first type is to choose one of the D-frontier for further fault effect propagation. What is the second type? ➔ To **choose a J-frontier signal** to further justified toward the PIs.
   (d) During the execution of the D-algorithm, what condition will lead us to claim that the current fault under consideration is indeed "untestable"? (Note: the condition consists of two sub-conditions that hold at the same time. One is about the D-frontier and the other about the J-frontier). ➔ The D-frontier is empty, while J-Frontier is not empty yet. All solution space has been exhausted yet, there is not valid test pattern.

6. (15%) Consider the following questions related to the PODEM algorithm for ATPG.
   (a) PODEM performs a direct search on the primary inputs. Two routines are especially important to guide the search process, namely *objective*() and *backtrace*(). The routine *objective*() is to set up an objective as a signal-value pair. Describe the function of *backtrace*(). (5%) ➔ According to an objective, find an all-x path to a PI, so that an assignment at that PI will be likely to contribute to the satisfaction of the current objective.
   (b) The SCOAP program, denoting SANDIA Controllability and Observability Analysis Program could provide useful guidance to speed up the PODEM search algorithm. Consider a two-input NAND-gate in the circuit under test, Z = (AB)'. If CC0(A), CC1(A), CC0(B), CC1(B) are 3, 6, 10, and 1, respectively. Compute CC0(Z). (5%) ➔ (6+1)+1 = 8
   (c) Unlike the controllability measure calculation that is performed using a forward sweep of the circuit under test, the observability measure calculation is done by a backward (PO-to-PI) sweep. If the observability of Z, denoted as CO(Z), has been calculated as 5, then what is

CO(A). (5%) → (5+1)+1 = 7

7. (15%) To detect a signal *f slow-to-rise transition delay fault*, a two-pattern test $<v_1, v_2>$ is required.
   (a) State what requirement needs to be satisfied for vector v_1 in the first time frame. (5%) -> v_1 needs to cause signal *f* to logic '0' (or excite signal *a* stuck-at-1 fault)
   (b) In the second time frame, the requirement of v_2 is equivalent to the detection of a single-stuck-at fault. Name the stuck-at fault. (5%) -> v_2 needs to be able to detect signal *f* stuck-at-0 fault in the 2nd time frame.
   (c) Suppose that $v_1=\{(y_1, y_2, y_3)=(1, 1, 0)\}$ and $v_2=\{(y_1, y_2, y_3)=(1, 1, 0)\}$ are two vectors satisfying all the above two requirements. Signals $\{y_1, y_2, y_3\}$ are PPI signals in the scan chain in the order of (SI $\rightarrow y_3 \rightarrow y_2 \rightarrow y_1 \rightarrow$ SO). Can we apply $<v_1, v_2>$ under the *Launch-off-Shifting* (LOS) scheme? Why? (5%) -> NO, v_1 cannot become v_2 after one cycle of scan shifting operation.