Hw2

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1. Write the RTL code in Verilog or VHDL that takes in two 8-bit positive integers, A[7:0]and B[7:0],and produces its quotient Q[7:0] and remainder R[7:0].

Verilog code 如附件。

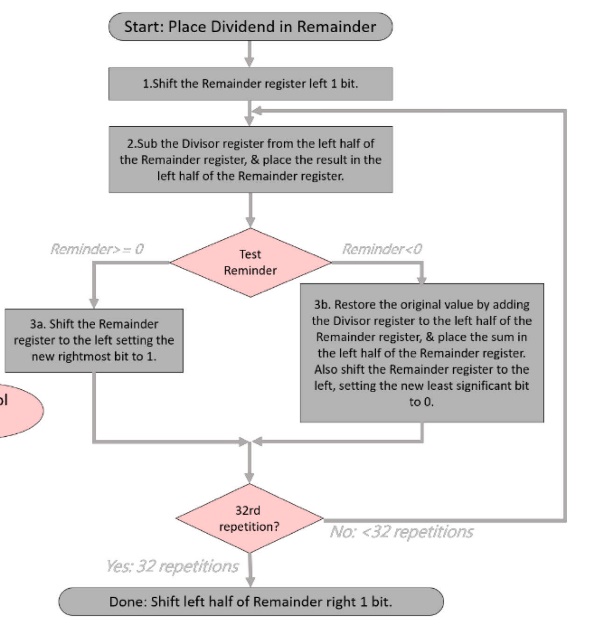
此次是使用硬體最佳化除法，將餘數和商放在同個暫存器中，首先開出一個16bits的暫存器，將被除數放入[0:7]，接著向前進一位，並將[8:15]減去除數並檢查是否為正 i.e (MSB是否為0)。

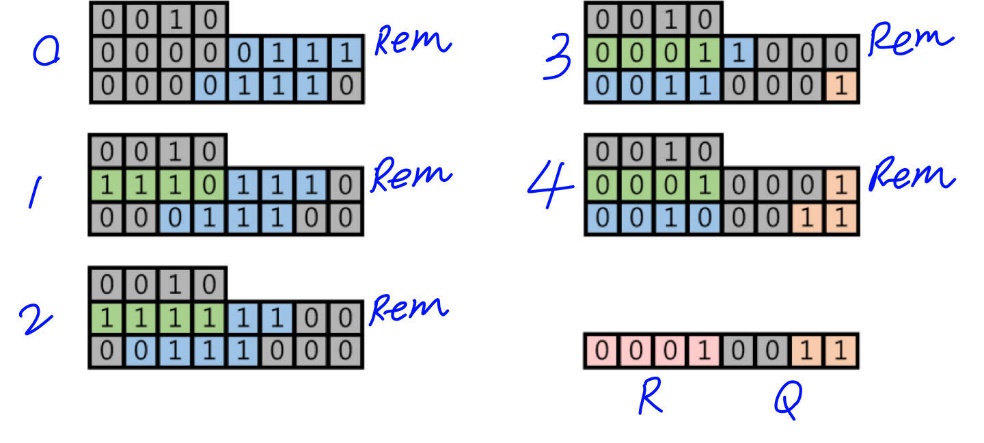
如果為負，就把原本還沒減過的16bits暫存器往右移1個bit。

如果為正，則暫存器往右移1個bit並且加1。

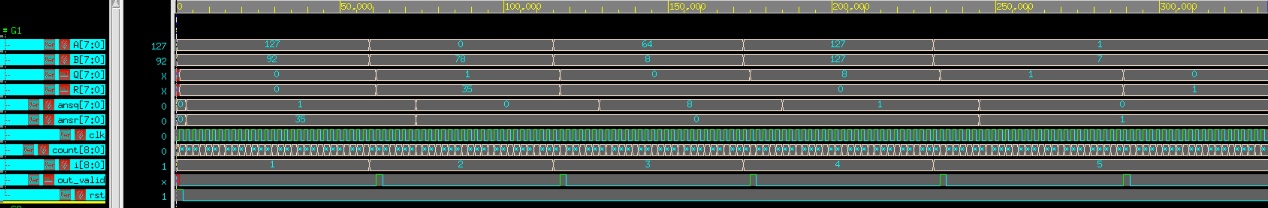
最後暫存器中[0:7]為商，暫存器[8:15]要往左移1個bit才是餘數。

以下是flow chart以及一個4bits的小範例



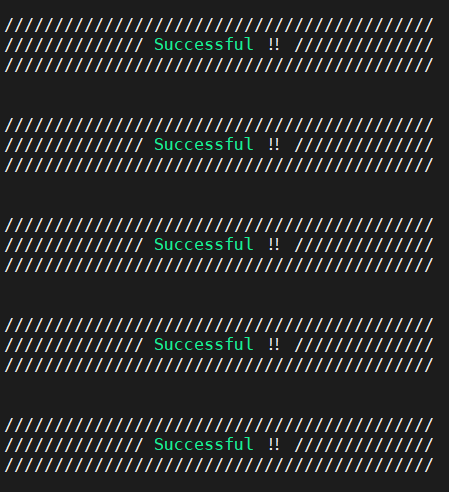


1. Verify the correctness of your RTL code by a testbench. You should try it out by at least 3 pairs of input numbers.



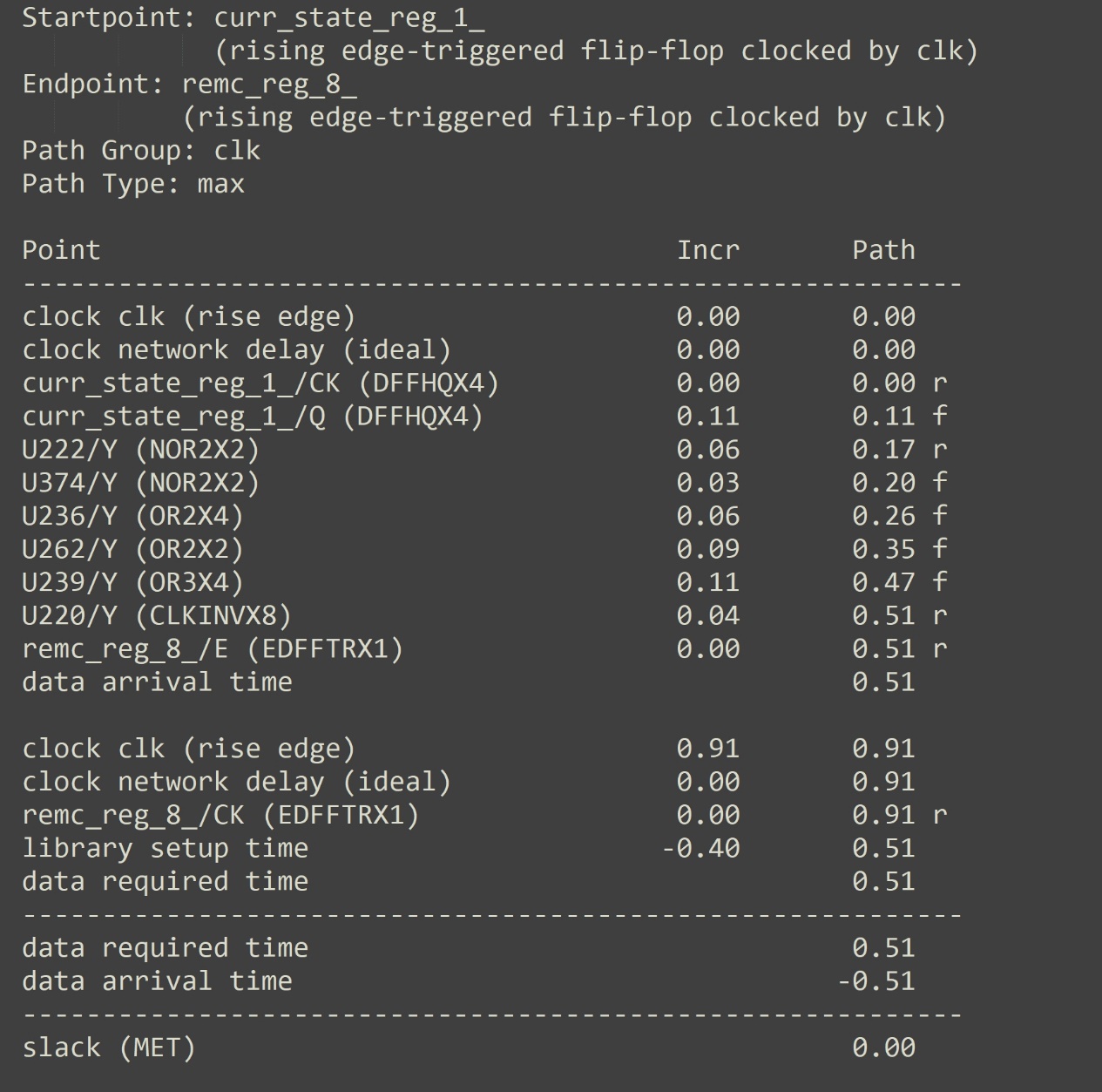
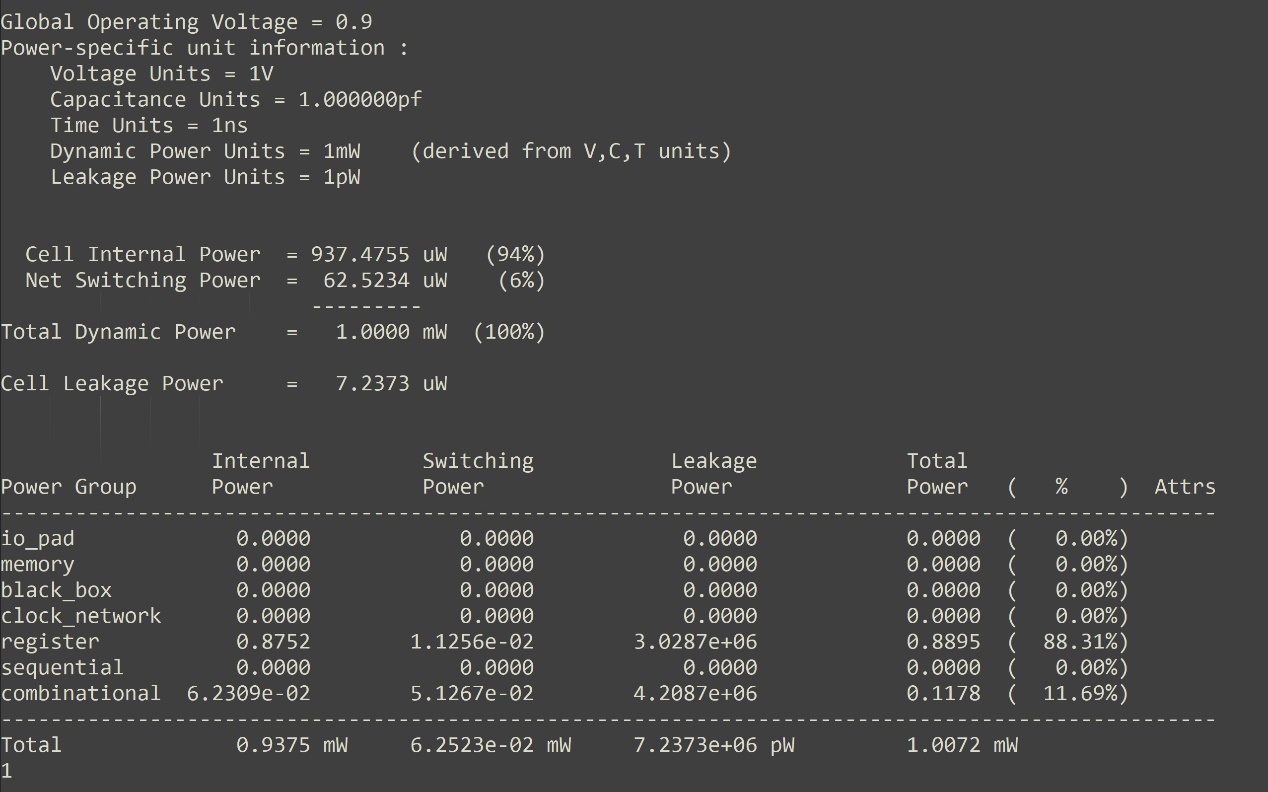
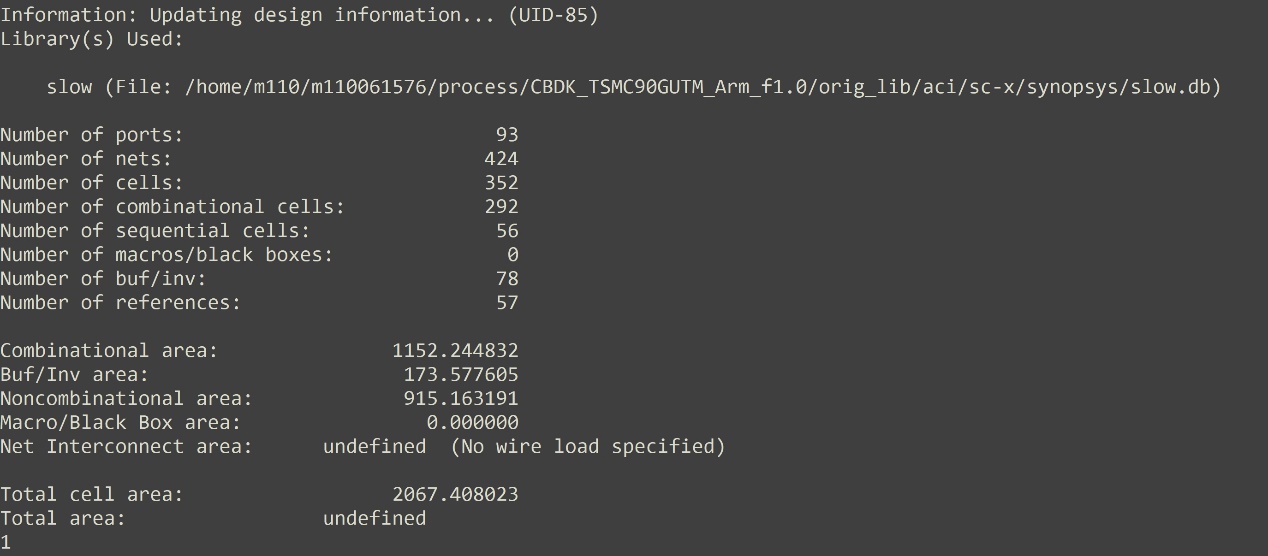
Testbench測試資料為(127、92) (0、78) (64、8) (127、127) (1、7)。

由模擬可得知，5個測資均為正確，並且沒有time violation



1. Use asynthesis script to convert your RTL code into a gate-level netlist.Report the final gate count, the maximum operating speed(in MHz) and the estimated power dissipation in (mW) using *Design Compiler*.

Netlist檔如附件。



gate count

2607.4/2.8224=923.82

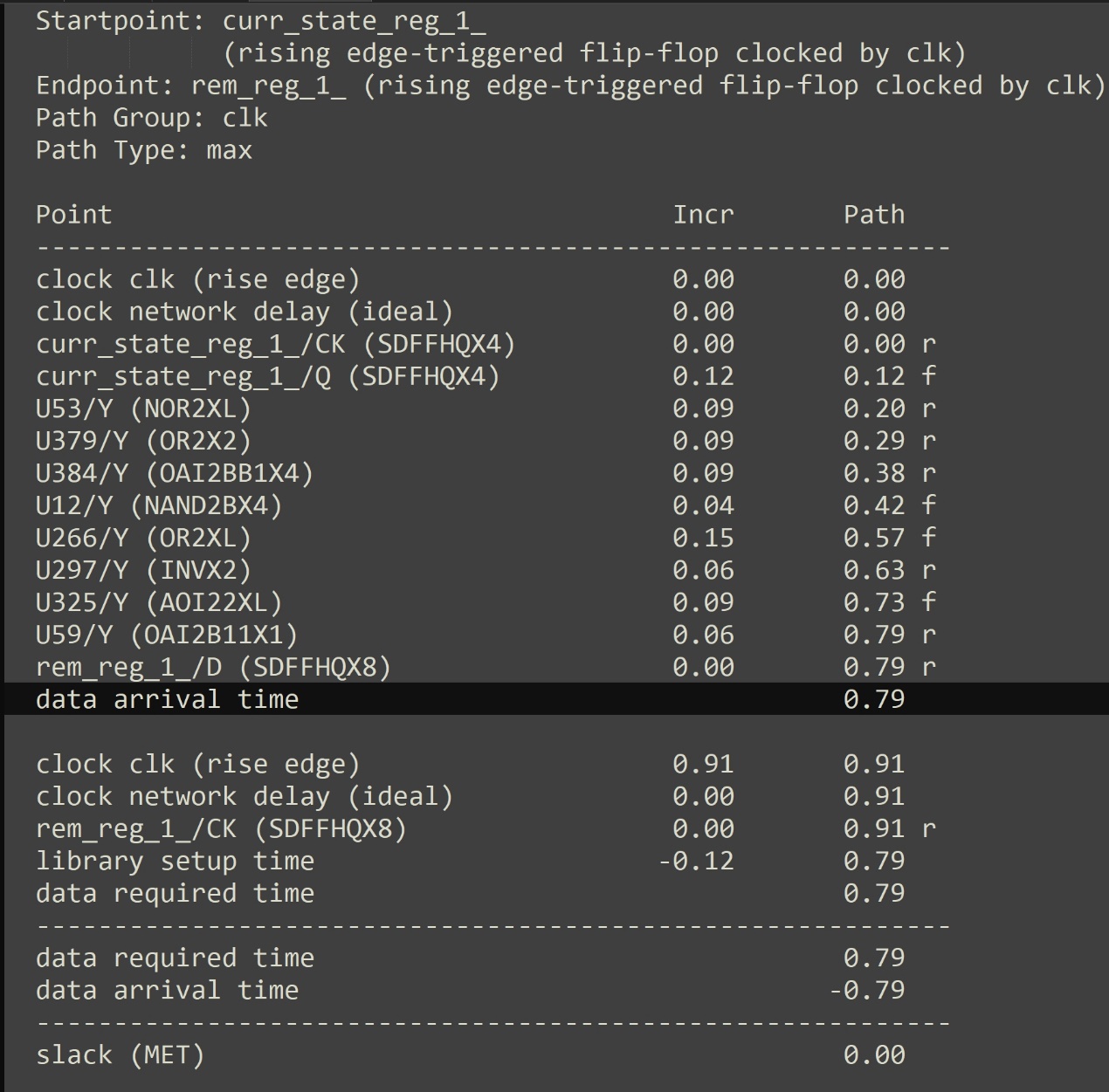
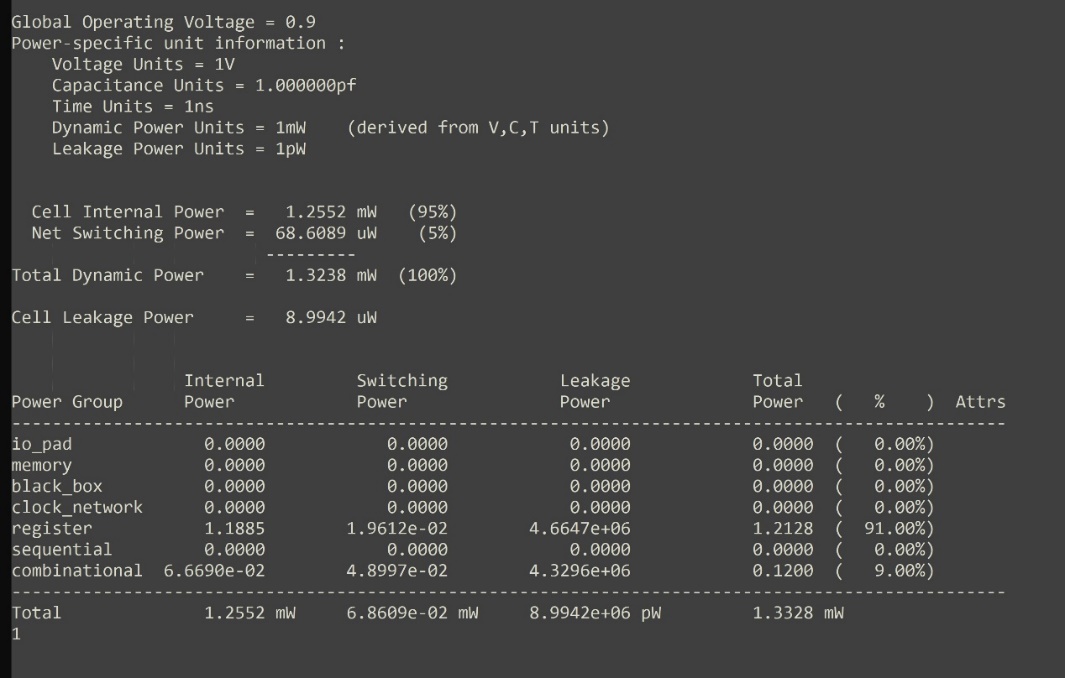
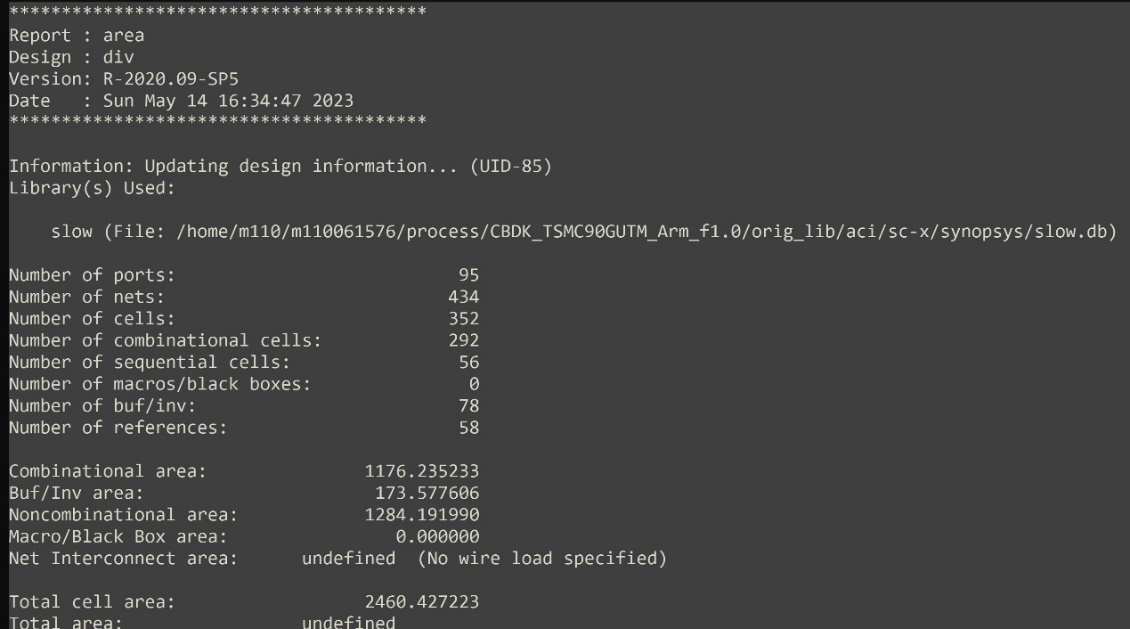
maximum operating speed

1/0.91=1.1GHz

estimated power dissipation

1.0072mW

1. Add the scan chain into your gate-level netlist obtained by part(c), report the resulting gate count, the maximum operating speed (in MHz) of your circuit. Compare to the non-scan version, and report the area overhead percentage and performance penalty due to scan chain insertion.



area overhead percentage

2607.4/2460.4=106.08%

maximum operating speed

1/0.91=1.1GHz

estimated power dissipation

1.3328mW

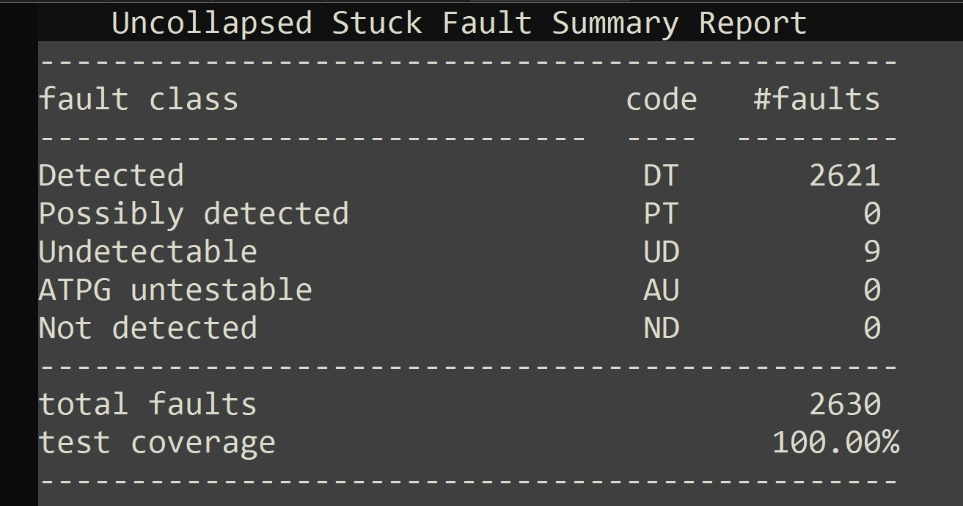
performance penalty

有沒有加scan chain的CLK period都相同，所以無performance penalty

* + - 1. 可發現加了scan chain之後power跟area，不過疑惑的是timing沒有增加
      2. 所以沒有performance penalty

值得注意的是，asynchronous reset是不能加上scain chain的，必須要

synchronous reset，這點非常疑惑

1. Run ATPG using a commercial tool available and report the fault coverage.
   1. 
   2. 組員分工:
   3. 111061642王煒翔:理解演算法、寫RTL、testbench、尋找最高速度、debug、撰寫一部分的報告 (50%)
   4. 111061622薛仲勛:理解演算法、跑後續DFT的流程、撰寫一部分的報告 (50%)