Olivia W. Hsu

owhsu@stanford.edu

Personal Website Google Scholar

Education

Stanford University (Stanford, CA) **Expected June 2025**

Ph.D. in Computer Science GPA: 4.042/4.0

Selected Coursework**:**

Machine Learning with Graphs (CS 224W), Continuous Mathematical Methods with an Emphasis on Machine Learning (CS 205L), Domain-Specific Programming Models and Compilers (CS 343D), Parallel Processors Beyond Multicore (CS 382A), Engineering Design Optimization (CS 361), Interactive Computer Graphics (CS 248), Machine Learning (CS 229)

University of California, Berkeley (Berkeley, CA) **May 2019**

B.S. in Electrical Engineering and Computer Science GPA**:** 3.921/4.0

Selected Coursework:

Programming Languages and Compilers (CS 164), VLSI Digital Signal Processing Architectures (CS 290C), Computer Architecture (CS 152)**,** Analog Integrated Circuits (EE 140), Operating Systems (CS 162), Digital Integrated Circuits and ASIC Lab (EECS 151), Digital Signal Processing (EE 123)

Thomas Jefferson High School for Science and Technology (Alexandria, VA) **May 2015**

Experience

Stanford Pervasive Parallelism Lab (Stanford, CA) – *Student Research Assistant* **Jan 2020 – Present**

- Co-advised by Professor Kunle Olukotun and Professor Fredrik Kjolstad on automatic compilation of sparse applications to domain-specific architectures, reconfigurable dataflow architectures, and hardware accelerators.
- Also working on compilation of sparse programs for CPU and GPU backends.

Samsung Semiconductor (San Jose, CA) – *Hardware Architecture Intern* **June 2023 – Sept 2023**

- Intern researching the programmability and characterization of sparse workloads on supercomputing systems.

Stanford University CS Department (Stanford, CA) – *Course Assistant* **Sept 2021 – Dec 2021**

- Course assistant (CA) for CS 149: Parallel Computing under Professors Kayvon Fatahalian and Kunle Olukotun

UC Berkeley Group Matching Project (Berkeley, CA) – *Student Researcher* **Aug 2020 – Aug 2021**

- Developed a scalable and inclusive group matching process for student collaboration under Professor Gireeja Ranade.
- The group matching technique first launched in the Fall 2020 offering of EECS 16A with 980+ students, with wider adoption presently occurring across the UC Berkeley EECS department in courses: CS 70, CS 61A, CS 168, and more.

Ayar Labs (Emeryville, CA) – *Hardware VLSI Intern* **June 2020 – Sept 2020**

- Digital VLSI intern working on designing digital circuit blocks in System Verilog to match provided specifications, digital block verification, and pushing blocks through the physical design process be DRC and LVS clean.

Stanford VLSI Research Group (Stanford, CA) – *Rotation Research Assistant* **Sept 2019 – Jan 2020**

- Researching novel ADC-based high-speed link equalization techniques under Professor Mark Horowitz

Apple Inc. (Cupertino, CA) – *CPU Design Verification Intern* **June 2019 – Sep 2019,**

- Created instruction set architecture pseudocode for the Apple CPU **May 2018 – Aug 2018**
- Developed a runtime co-simulation checker and debug features in a software functional model of the Apple CPU using C++

Berkeley Wireless Research Center (Berkeley, CA) – *Undergraduate Researcher* **Jan 2017 – July 2019**

- Designed photonic devices using the Berkeley Photonic Generator (BPG) and digital circuits for high speed communication in Verilog for an ultrasound receive array system taped out in a Global Foundries 45nm RFSOI process.

- Built a lab setup that tests the sensitivity of silicon photonic devices when disturbed with an ultrasonic wave.

UC Berkeley EECS Department (Berkeley, CA) – *Head Undergraduate Student Instructor* **Aug 2016 – Jan 2018**

- Head teaching assistant (TA) for an 850+ student introductory EE course, EECS 16A, in charge of 30+ other TAs and various duties including course administration, labs, exam creation, office hours, and grading/reader management.

NASA Jet Propulsion Laboratory (Pasadena, CA) – *Hardware Research Intern* **June 2016 – Aug 2016**

- Developed a sensor testbed that verified the communication systems on a rad-hard, deep-space CubeSat avionics board.

Publications

E. Hellsten, A. Souza, J. Lenfers, R. Lacouture, **O. Hsu**, A. Ejjeh, F. Kjolstad, M. Steuwer, K. Olukotun, and L. Nardi, "BaCO: A Fast and Portable Bayesian Compiler Optimization Framework," *to appear in Architectural Support for Programming Languages and Operating Systems (ASPLOS),* 2024.

M. Bansal, **O. Hsu**, K. Olukotun, and F. Kjolstad, "Mosaic: An Interoperable Compiler for Tensor Algebra," *in Programming Language Design and Implementation (PLDI), Proceedings of the ACM on Programming Languages (PACMPL),* 2023.
Distinguished Paper Award

O. Hsu, M. Strange, J. Won, R. Sharma, K. Olukotun, J. Emer, M. Horowitz, and F. Kjolstad, "The Sparse Abstract Machine," *in Architectural Support for Programming Languages and Operating Systems (ASPLOS),* 2023.

O. Hsu, A. Rucker, T. Zhao, K. Olukotun, and F. Kjolstad, "Stardust: Compiling Sparse Tensor Algebra to a Reconfigurable Dataflow Architecture," *Arxiv Preprint,* 2022.

S. Kohli, N. Ramchandran, A. Tudor, G. Tumushabe, **O. Hsu**, and G. Ranade, "Inclusive Study Group Formation at Scale," *in Special Interest Group on Computer Science Education (SIGCSE) Technical Symposium,* 2023.

R. Henry[1], **O. Hsu[1]**, R. Yadav, S. Chou, K. Olukotun, S. Amarasinghe, and F. Kjolstad, "Compilation of Sparse Array Programming Models," *in Object-Oriented Programming, Systems, Languages & Applications (OOPSLA), Proceedings of the ACM on Programming Languages (PACMPL),* 2021.

P. Zarkos, S. Buchbinder, C. Adamopoulos, S. Madhvapathy, **O. Hsu**, J. Whinnery, P. Bhargava, and V. Stojanović, "Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Imaging Applications in a Zero-Change 45nm CMOS-SOI Process," *in Symposium on VLSI Circuits (VLSI),* 2021

P. Zarkos, S. Buchbinder, C. Adamopoulos, **O. Hsu**, S. Madhvapathy, J. Whinnery, P. Bhargava, and V. Stojanović, "Monolithically Integrated Electronic-Photonic Ultrasound Receiver Using Microring Resonator," *in Conference on Lasers and Electro-Optics (CLEO),* OSA Technical Digest (Optical Society of America, 2021)

P. Zarkos, **O. Hsu**, and V. Stojanović, "Ring Resonator Based Ultrasound Detection in a Zero-Change Advanced CMOS-SOI Process," in *Conference on Lasers and Electro-Optics (CLEO)*, OSA Technical Digest (Optical Society of America, 2019), 2019

Honors and Awards

- 2019 IEEE-Eta Kappa Nu (HKN) Alton B. Zerby and Carol T. Koerner Outstanding Student Award
- 2019 National Science Foundation Graduate Research Fellow (NSF GRFP)
- 2018-2019 UC Berkeley EECS Arthur M. Hopkin Award Recipient
- 2017-2018 Outstanding Graduate Student Instructor Award UC Berkeley
- IEEE-Eta Kappa Nu (HKN) National Electrical Engineering Honor Society Officer
- Tau Beta Pi (TBP) National Engineering Honor Society Member
- Fall 2015 Cal Alumni Association Leadership Award Recipient

[1] Both authors contributed equally