Olivia Weiya Hsu

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Education

Stanford University (Stanford, CA) **Expected June 2024**

Ph.D. in Computer Science

Selected Coursework: Interactive Computer Graphics (CS 248), Introduction to Machine Learning (CS 229)

University of California, Berkeley (Berkeley, CA) **May 2019**

B.S. in Electrical Engineering and Computer Science **GPA:** 3.921/4.0

Selected Coursework: Programming Languages and Compilers (CS 164), Computer Architecture (CS 152)**,** Analog Integrated Circuits (EE 140), Operating Systems (CS 162), Digital Integrated Circuits and ASIC Lab (EECS 151), Digital Signal Processing (EE 123)

Experience

Stanford Pervasive Parallelism Lab (Stanford, CA) – *Rotation Student* **Jan 2020 – Present**

Stanford VLSI Research Group (Stanford, CA) – *Rotation Student* **Sept 2019 – Jan 2020**

- Researching novel ADC-based high-speed link equalization techniques under Professor Mark Horowitz

Apple Inc. (Cupertino, CA) – *CPU Design Verification Intern* **June 2019 – Sep 2019,**

- Created instruction set architecture pseudocode for the Apple CPU **May 2018 – Aug 2018**
- Developed a runtime co-simulation checker and debug features in a software functional model of the Apple CPU using C++

Berkeley Wireless Research Center (Berkeley, CA) – *Undergraduate Researcher* **Jan 2017 – July 2019**

- Designed photonic devices using the Berkeley Photonic Generator (BPG) and digital circuits for high speed communication in Verilog for an ultrasound receive array system taped out in a Global Foundries 45nm RFSOI process.
- Built a lab setup that tests the sensitivity of silicon photonic devices when disturbed with an ultrasonic wave.

UC Berkeley EECS Department (Berkeley, CA) – *Head Undergraduate Student Instructor* **Aug 2016 – Jan 2018**

- Head administrative, lab, and office hours teaching assistant for an 850+ student introductory EE course, EE 16A.

NASA Jet Propulsion Laboratory (Pasadena, CA) – *Hardware Research Intern* **June 2016 – Aug 2016**

- Developed a sensor testbed that verified the communication systems on a rad-hard, deep-space CubeSat avionics board.

Relevant Projects

Space Technologies at Cal (STAC) – *Co-Founder, President*, *Lead Electrical Engineer* **Aug 2016 – Present**

- Implemented electronics in a High Altitude Balloon (HAB) with a successful launch in partnership with NASA Ames and JPL.
- Won a Blue Origin payload launch and developed experiments that test laser ablation and biological effects in microgravity.

Image Communication Project **Jan 2018 – May 2018**

- Transmitted JPEG2000-like compressed images via radio using a modified AX25 packetization scheme and an AFSK modulation scheme with a baud rate of 1.6 kHz.

SOC Analog Peripheral Design **Jan 2018 – May 2018**

- Completed the schematic design for a low voltage bandgap, a temperature sensor, a programmable gain amplifier, analog and digital voltage regulators, a SAR ADC, and a capacitive DAC with two other people

Application Specific Integrated Circuits (ASIC) Processor Design **Jan 2017 – May 2017**

- Designed the best-performing three-stage pipelined RISC-V processor in Verilog for 28nm CMOS technology with a partner.
- Created a finite state machine that implemented a 64x512 bit direct mapped, write-back cache using SRAM standard cells.

Publications

- P. Zarkos, **O. Hsu**, and V. Stojanović, "Ring Resonator Based Ultrasound Detection in a Zero-Change Advanced CMOS-SOI Process," in *Conference on Lasers and Electro-Optics (CLEO)*, OSA Technical Digest (Optical Society of America, 2019)

Honors and Awards

- 2019 IEEE-Eta Kappa Nu Alton B. Zerby and Carol T. Koerner Outstanding Student Award
- 2019 National Science Foundation Graduate Research Fellow (NSF GRFP)
- 2018-2019 UC Berkeley EECS Arthur M. Hopkin Award Recipient
- IEEE-Eta Kappa Nu National Electrical Engineering and Tau Beta Pi National Engineering Honor Society Member
- Fall 2015 Cal Alumni Association Leadership Award Recipient