ETROC1 TDC Test Block Design Note

This document aims to provide information for ETROC1 TDC Test Block chip test.

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1 ETROC1 TDC Test Block chip overview

ETROC1 is the second prototype of ETROCn (Endcap Timing Readout Chip) that is being developed for the LGAD-based CMS Endcap Timing Layer (ETL) or HL-LHC. The ETROC1 TDC Test Block chip a crucial important test module for testing the function and specification of the Time-to-Digital (TDC). It is developed with TSMC 65 nm CMOS process with 1p9m-3x1u1z. All the building block have metal layers up to M7. The M8 and M9 metal layers are reserved for power supply ring.

The ETROC1 TDC Test Block chip is used to measure the leading edge arriving time (TOA) and time over threshold (TOT) of a pulse that was generated by analog front-end circuit. Each input pulse will be convert to three digital time, TOA digital time (10 bit), TOT digital time (9 bit), and Calibration digital time (10 bit), respectively. The Calibration digital time can be converted from 320 MHz input clock.

The ETROC1 TDC Test Block chip aims to provide a chance to test some important specification and characteristic of the design TDC. The tape-out date is in late August, 2019, and turnaround is 9 weeks. Figure 1 illustrates the function diagram of the ETROC1 TDC Test Block chip. The die size of the ETROC1 TDC Test Block chip is about 0.7 mm x 1.9 mm (including seal ring). It has 26 pads in total while the opening area of each pad is about 65 um x 130 um.

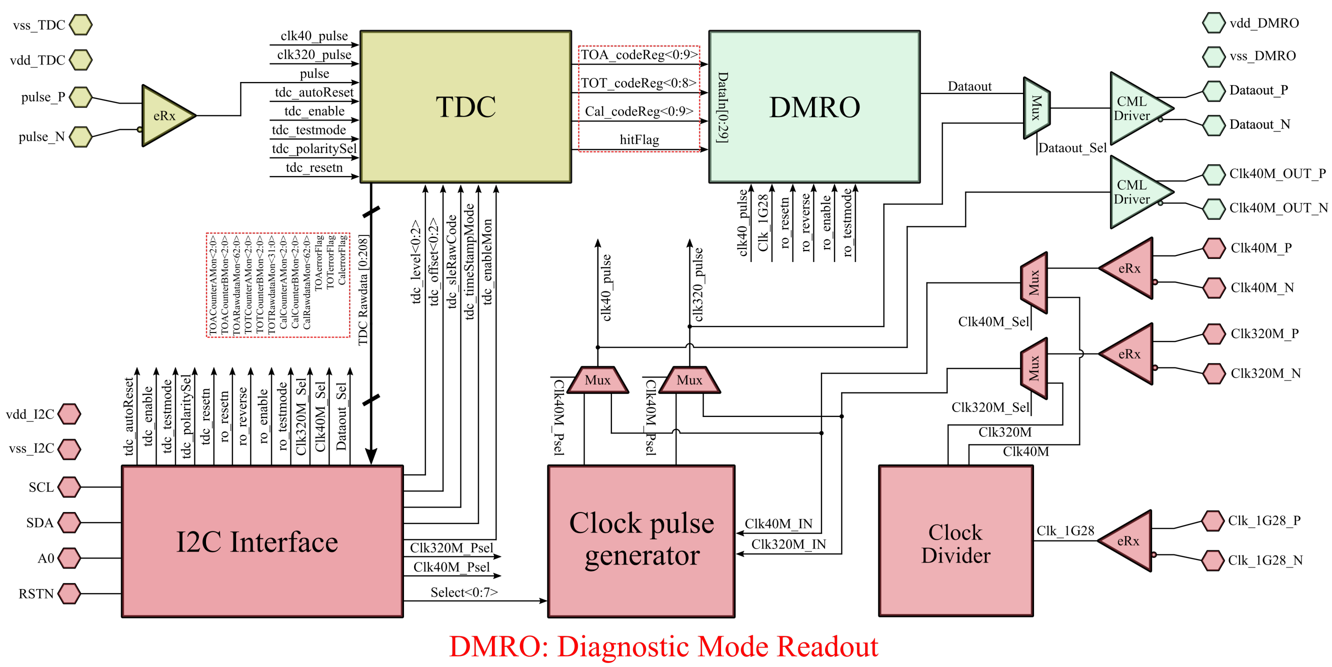

Figure 1: ETROC1 TDC Test Block chip function diagram

The ETORC1 TDC Test Block chip mainly includes 5 modules, Time-to-Digital (TDC), Diagnostic Mode Readout (DMRO), I2C Interface, Clock Pulse Generator, Clock Divider and GRO (Gate Ring Oscillator). The same color modules share a pair of power supply as shown in the Figure 1. The supply voltage of each power supply is 1.2 V.

The layout of ETROC1 TDC Test Block chip is shown as Figure 2. The Dataout_N pad is named as the pin 1, from the anti-clockwise direction, the pad number is increasing with the step 1, and the last pad GRO_Out_N is numbered as 26. The ETROC1 TDC Test Block is located at the upper right corner. The safe distance between pads and edge of ETROC1 chip is 60 um. There are four sets of power supply ring from left to right on the layout. GRO power ring, I2C power supply ring , TDC power supply ring and DMRO power supply ring, respectively. Figure 2 shows the ETROC1 TDC Test Block Layout.

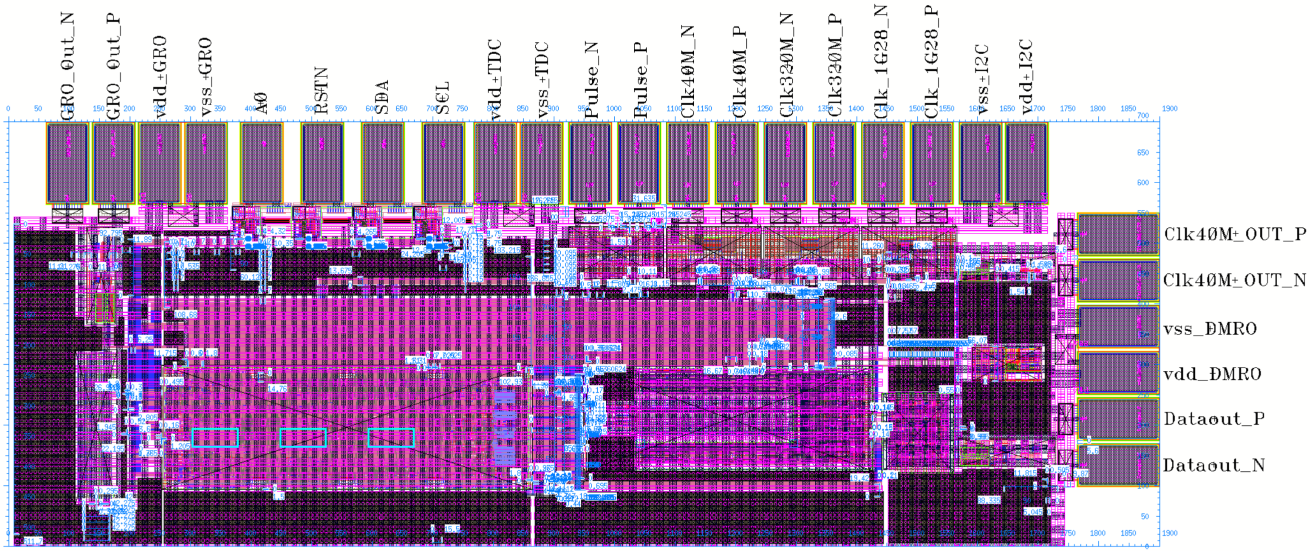

Figure 2: ETROC1 TDC Test Block chip layout

2 Pin Assignment

The ETROC1 TDC Test Block chip has 26 pads that can be divided into three types: general IO pads, differential IO pads, and power IO pads, respectively. The 26 pads are located on adjacent two sides of the square chip. The below table listed the detail pad information of the ETROC1 TDC Teset Block chip.

Table 1: ETROC1 TDC Test Block Chip pads information

NO.	Name	Location (x,y)	Type	Description
1	Dataout_N	(6872.21, 8373.85)	Digital Out	1.28G high speed serial data negative output
2	Dataout_P	(6872.21, 8450.03)	Digital Out	1.28G high speed serial data positive output
3	DMRO_VDD	(6872.21, 8526.21)	Power supply	Power supply for DMRO module, 1.2V
4	DMRO_VSS	(6872.21, 8602.39)	Ground	Ground for DMRO module
5	Clk40M_OUT_N	(6872.21, 8678.57)	Digital Out	40M clock negative output
6	Clk40M_OUT_P	(6872.21, 8754.75)	Digital Out	40M clock positive output
7	I2C_VDD	(6720.68, 8872.21)	Power supply	Power supply for I2C module and Clock modules, 1.2V
8	I2C_VSS	(6644.50, 8872.21)	Ground	Ground for I2C module and Clock modules
9	Clk_1G28_P	(6563.92, 8872.21)	Digital In	1.28G clock positive input
10	Clk_1G28_N	(6483.34, 8872.21)	Digital In	1.28G clock negative input
11	Clk320M_P	(6402.76, 8872.21)	Digital In	320M clock positive input
12	Clk320M_N	(6322.18, 8872.21)	Digital In	320M clock negative input
13	Clk40M_P	(6241.61, 8872.21)	Digital In	40M clock positive input
14	Clk40M_N	(6161.03, 8872.21)	Digital In	40M clock negative input
15	Pulse_P	(6080.45, 8872.21)	Analog In	Pulse positive input
16	Pulse_N	(5999.87, 8872.21)	Analog In	Pulse negative input
17	TDC_VDD	(5919.29, 8872.21)	Power supply	Power supply for TDC module, 1.2V
18	TDC_VSS	(5843.11, 8872.21)	Ground	Ground for TDC module
19	SCL	(5756.33, 8872.21)	Digital In	I2C module serial clock
20	SDA	(5651.26, 8872.21)	Digital In/Out	I2C module serial data
21	RSTN	(5546.18, 8872.21)	Digital In	I2C module reset, low active
22	A0	(5441.11, 8872.21)	Digital In	I2C module external address select
23	GRO_VDD	(5350.91, 8872.21)	Power supply	Power supply for GRO module, 1.2V
24	GRO_VSS	(5274.73, 8872.21)	Ground	Ground for GRO module
25	GRO_Out_P	(5198.55, 8872.21)	Digital Out	GRO positive output
26	GRO_Out_N	(5122.37, 8872.21)	Digital Out	GRO negative output

3 Time-to-Digital (TDC)

3.1 TDC overview

Time-to-digital converter (TDC) converts the time interval to the digital output. The TDC takes as input the discriminator output and records the time of arriving (TOA) and time over threshold (TOT) for a fixed discriminator threshold. The TOA and TOT TDC bin size should not exceed 30 ps and 100 ps, respectively. To allow improvements in particle identification in heavy ion collision events, the TDC measurement time window is extended to 12.5 ns and programmable.

The ETROC1 TDC consists of three parts: TDC Controller, TDC Delay Line, and TDC Encoder. Figure 3 shows the block diagram of TDC module and interconnection of each part.

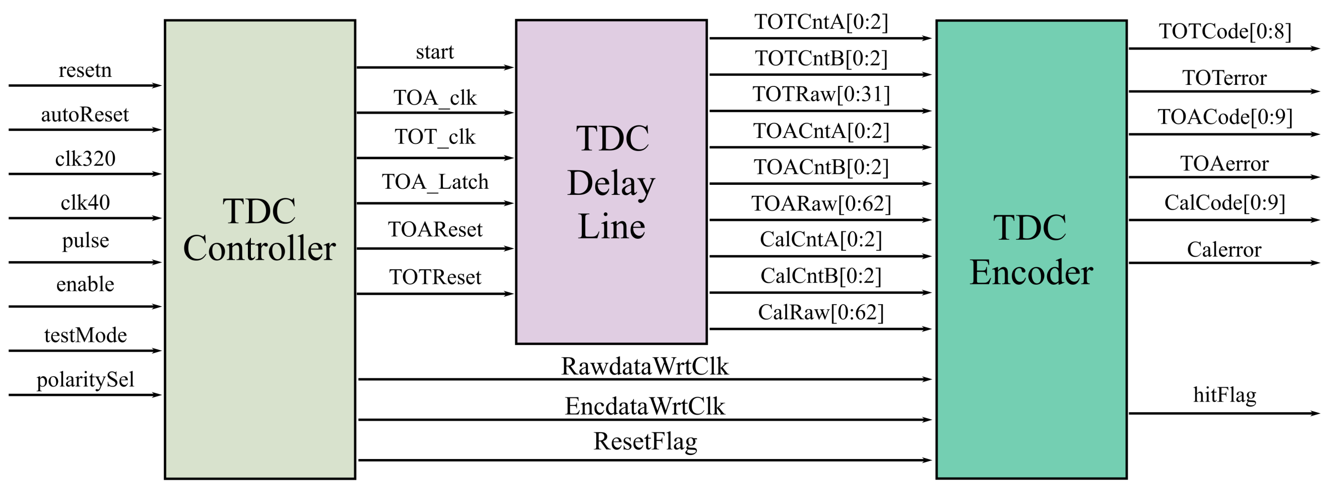

Figure 3: TDC block diagram

The layout of TDC is shown as Figure 4 and its area is about 467.2 um X 165.6 um. The read dashed line besieged part is the TDC Controller. The blue dashed line besieged part is the TDC Delay Line. The green dashed line besieged part is the TDC Encoder.

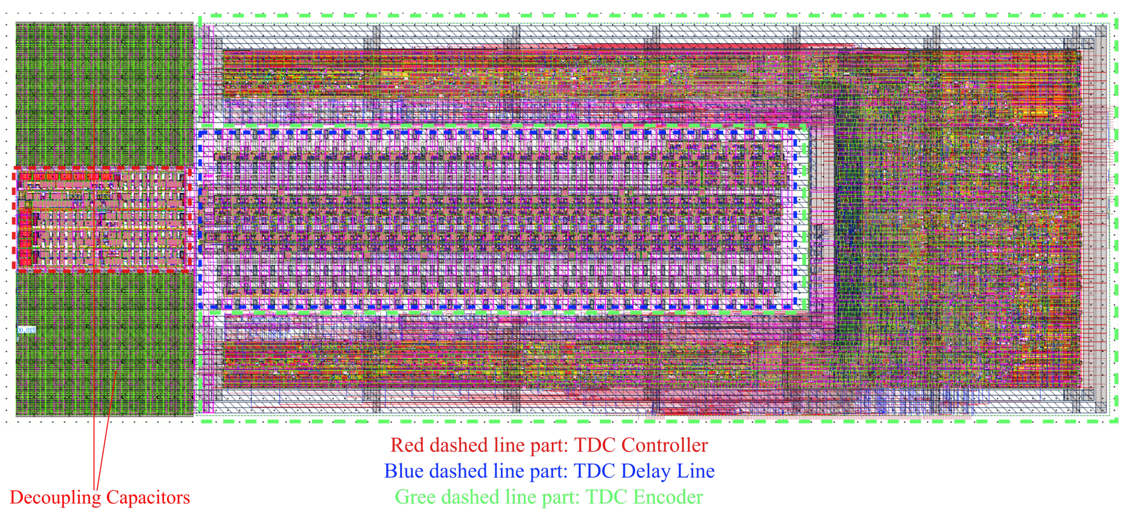

Figure 4: TDC Layout

3.2 TDC Controller

The TDC Controller generates two groups of signals: signal pulse/clock for TDC Delay Line and clock signal for TDC Encoder. The pulse is the measured signal and valid during the meaWindow that is the area between the falling edge of the clk40 and the first rising edge of clk320. The TOA is defined as time interval between leading edge of pulse signal and first rising edge of the clk320. The TOT is defined as the width of pulse signal. The clk320 is used to calibrate average bin size of the TDC Delay Line.

The block diagram of TDC Controller is shown as Figure 5. The TDC Controller mainly contains Measure Window Generating Logic, Reset Generator, Core Pulse Generator , and TDC Readout Controller. The Measure Window can disable or enable the whole TDC via enable control bit. In test mode, the Measure Window Generator generates a fixed test pulse without pulse input and in the working mode, the input pulse is from the external waveform generator or front-ended discriminator. The Reset Generator generates the sync reset signal to reset DFFs in the pulse generator. In auto reset mode, it reset for every $40\,\mathrm{MHz}$ clock period. The Core Pulse Generator receives valid input pulse signal and generates start signal, TOA/TOT sampling clock for delayline (GRO). The TDC Readout Controller generates readout clock and signal for TDC Encoder and delayline.

The details schematic and implementation will be discussed in the below sections.

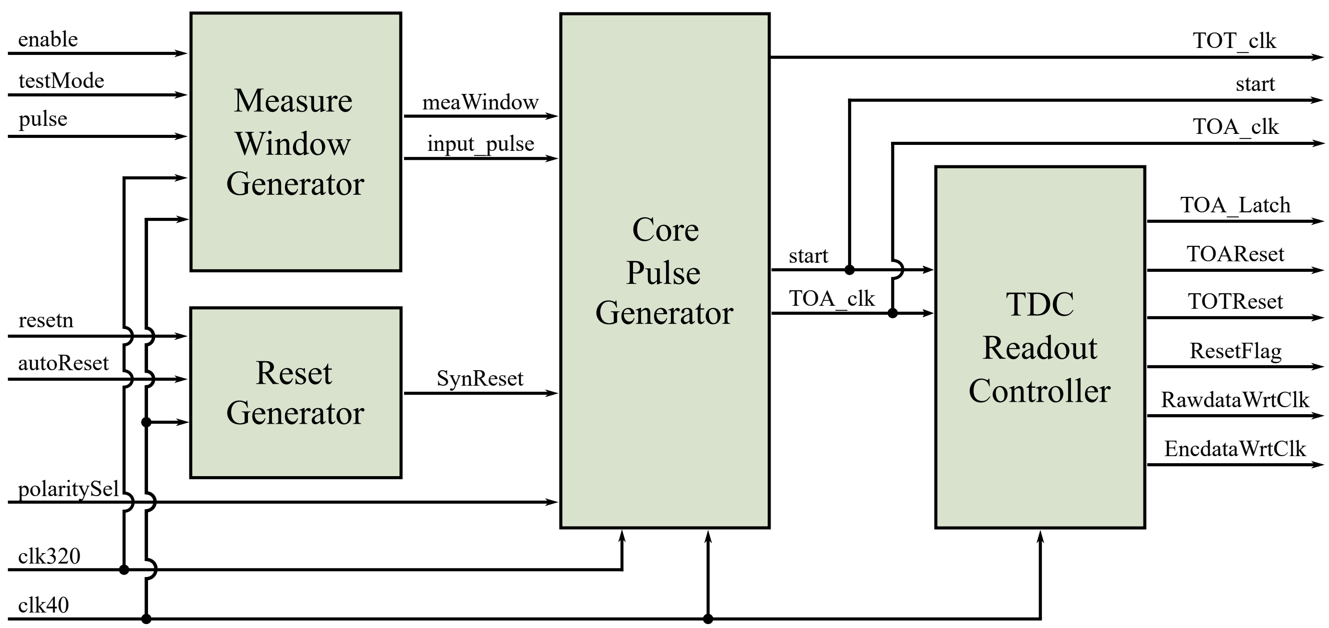

Figure 5: TDC Controller Block Diagram

3.2.1 Measure Window Generator

The Measure Window is a positive pulse signal to exclude the input signal beyond the pulse window. The width of the meaWindow is determined by the falling edge of $40\,\mathrm{MHz}$ clock and the first leading edge of $320\,\mathrm{MHz}$ clock, up to $12.5\,\mathrm{ns}$. The meaWindow width is programmable by shifting the clk32 clock phase with $3.125\,\mathrm{ns}$ setp which is implemented by global clock generator. When enable is deasserted, the meaWindow signal disables all the output signals. The schematic and timing of Measure Window Generator logic is shown as Figure 6.

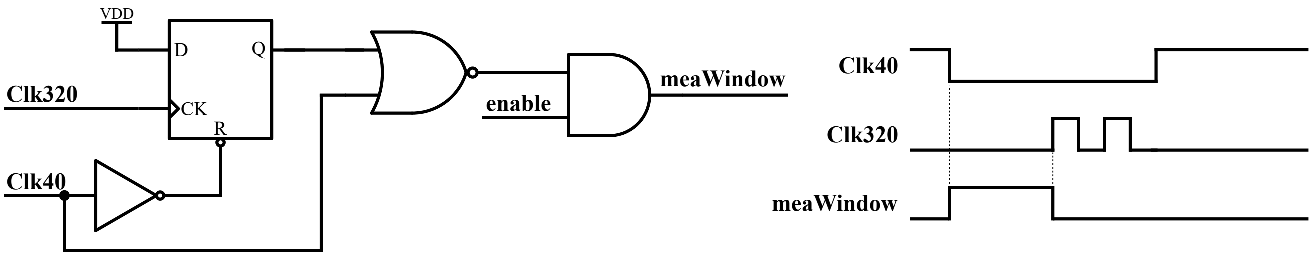

Figure 6: Schematic and timing of Measure Window Generator

When there are more than one pulse in the meaWindow, only the first pulse will be measured and other pulse will be neglected automatically. If the pulse beyond the meaWindow occurs, it will not disturb the next measurement.

3.2.2 Reset Generator

The Reset Generator has two reset modes that are the autoReset mode and the external reset mode. The synReset signal is active low. When autoReset is true, the Start Pulse Generator is reset for every $25\,\mathrm{ns}$ right before the measure window. In autoReset mode, the periodic reset signal (rstn_clk40) is a negative pulse generated at the falling edge of the $40\,\mathrm{MHz}$ clock. The delay time $t3$ is about $200\,\mathrm{ps}$. User also can reset the Start pulse generator with an external resetn signal that is asynchronous with the clk40. The schematic of Reset Generator is shown as the Figure 7.

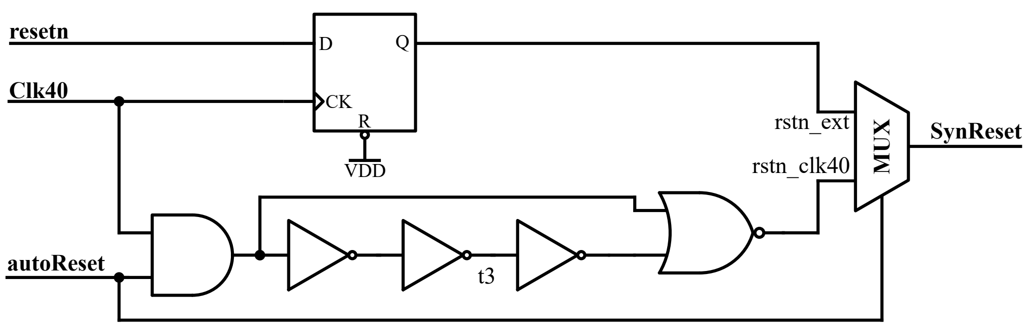

Figure 7: Schematic of Reset Generator

3.2.3 Start Pulse Generator Logic

In this section, we detail introduce the Pulse Generator Core Logic. The Pulse Generator Core Logic is used to generate Start pulse signal, TOA_clk, and TOT_clk, respectively. The Start pulse signal controls the delay line. When the Start pulse is asserted, the delay line oscillates. The TOA_clk signal is a clock signal to record the time interval between the leading edge of Start signal and the first rising edge of clk320. Similarly, the TOT_clk signal is also a clock signal to measure the time interval between leading edge and falling edge of Start pulse signal. The schematic of Start pulse generator logic is shown as Figure 8.

When testMode is asserted, Start pulse generator is in self test mode and a pulse signal copied from meaWindow with delay time of $\tau 0$ is tested. If the rising edge of input pulse is in the meaWindow pulse, the input pulse rising edge causes start from low level to high level and its falling edge causes TOT_clk from low level to high level; otherwise, the Start keeps low level.

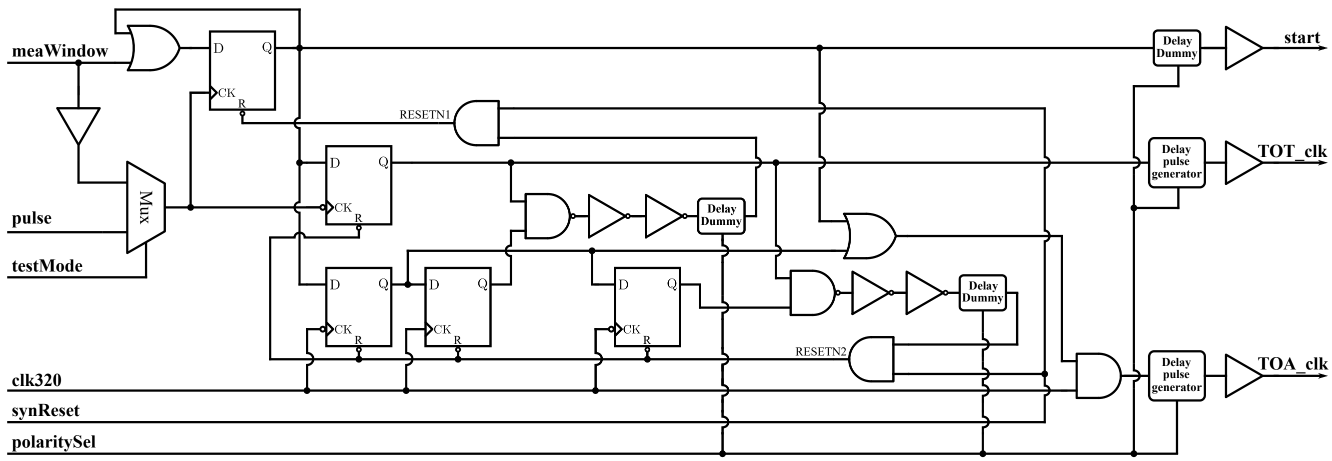

Figure 8: Schematic of Core Pulse Generator

After two rising edges of 320 MHz, when both QC1 = 1 and QC3 = 1, a resetn1 signal is generated. After two falling edges of 320 MHz, when both QC1 = 1 and QC4 = 1, a resetn2 signal is generated. A global reset (synReset) signal is used to reset all DFFs in the circuit.

When polaritySel is asserted, the TOA_clk and TOT_clk output signal are negative pulses generated at the rising edge of 320 MHz clock and the rising edge of input pulse, respectively. The negative pulse width ($\simeq 400$ ps) is enough for DFFs data setup, All clock output signals are extra delayed with $\tau 4$.

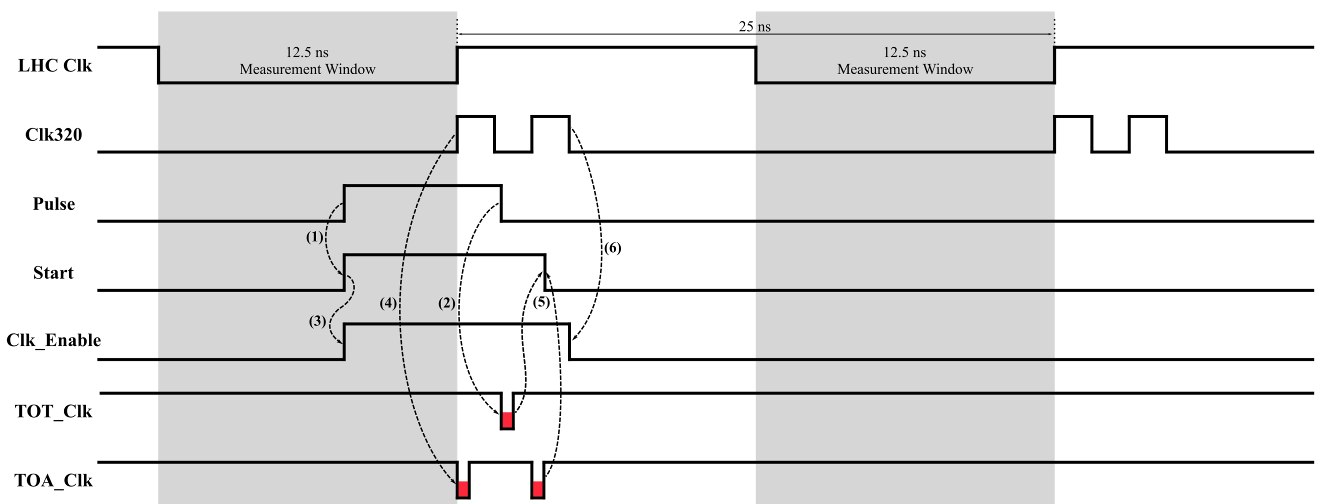

Figure 9: Timing diagram of Core Pulse Generator

The timing diagram of the Core Pulse Generator is depicted as Figure 9. The LHC Clk signal is generated by LHC detector with the frequency of 40 MHz. The low level half period of LHC Clk is used as a measurement window with the width 12.5 ns. When the rising edge of pulse occurs the measurement window, the clock signals (TOA_Clk and TOT_Clk) will be generated, otherwise, the clock signals will keep high level. The first rising edge of 320 MHz aligns with the rising edge of LHC Clk (40 MHz).

The 320 MHz is used to calibrate TDC Delay Line average bin size. At the first rising edge of 320 MHz Clock, We can record the digital code ($d1$) at this moment. Similarly, at the second rising edge of clk320, digital code ($d2$) is recorded by

TOA_ck clock signal. The width between the first and second rising edge of clk320 is constantly $3.125\,\mathrm{ns}$. The average bin size of Delay line is $3.125\,\mathrm{ns}/(d2 - d1)$.

3.2.4 TDC Readout Controller

The Readout Controller generates two groups of control signal for Delay Line and TDC Encoder, respectively. The TOA_Latch, TOAReset, and TOTReset are for TDC Delay Line and the RawdataWrtClk, EncdataWrtClk, and ResetFlag are for TDC Encoder. The Figure 10 shows the schematic of Readout Controller.

If the rising edge of start occurs, the QCP is high until QC1 is latched by falling edge of clk40 because the XOR gate senses the difference of QC1 and QC2. The QCP enable the RawdataWrtClk and EncdataWrtClk. If burst events occur, the ResetFalg is active after last event is record. The TOAReset and TOTReset negative width are $400\,\mathrm{ps}$, ensure the registers are reset before the sampling process. The internal DFFs output are accessible via slow control for debug and test purpose.

The RawdataWrtclk signal is used to latch the Delay Line sampling data at the rising edge and the EncdataWrtClk signal latches the encoded sampling data for output. The ResetFlag resets the hitFlag, TOAerrorFlag, TOTerrorFlag, and Calerror-Flag.

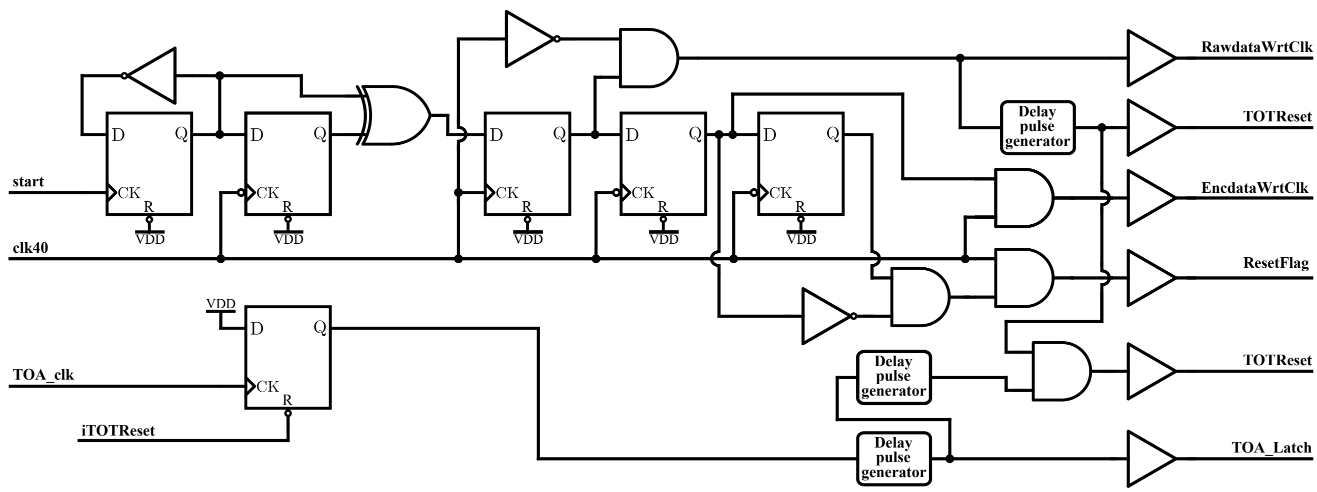

Figure 10: Schematic of TDC Readout Controller

3.3 TDC Delay Line

The TDC Delay Line is the main component of whole TDC. The resolution of TDC is determined by TDC Delay Line. The TDC Delay is composed by 63 Single Tap Delay Line as a Ring Oscillator. The TDC utilizes a combination of coarse time and fine time for the time measurement.

3.3.1 Single Tap Delay Line

The Single Tap Delay Line is composed by Two DFFs and one NAND. The NAND gate is used to generate minimum latency that is determined by the CMOS process and the two DFFs latch the TOA and TOT fine phase, respectively. The NAND gate and DFF are all ELT layout that has good performances. The Figure 11 shows the schematic of Single Tap Delay Line (red dashed line enclosed).

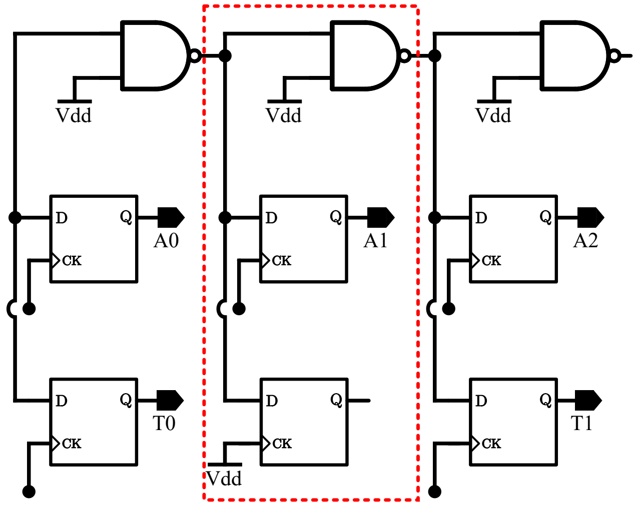

Figure 11: Schematic of Single Tap Delay Line

3.3.2 63 Tap Delay Line

A 63-tap gated ring oscillator (GRO) is used for the core TDC delay line, with uniform and uncontrolled **NAND** gate delay cells and 20 ps latency per cell. The load of all the nodes are well matched and the period of oscillator is about $2 * 62 * 20ps = 2.52ns$. This is a simple and fast GRO structure with no latency control logic, no DLL used. Instead, real time calibration will be used because each hit will be measured twice using two consecutive clocks. One delay line is used for both TOA/TOT measurements. TOA bin size is one cell delay latency ($\simeq$ 20 ps) and TOT bin size is twice the cell delay latency ($\simeq$ 40 ps). Dynamic range is configurable and up to 12.5 ns for both TOA and TOT measurement. TOA DNL estimated to be ± 0.15 LSB and INL is about ± 0.3 LSB. Figure 12 shows the schematic of 63 Tap delay line.

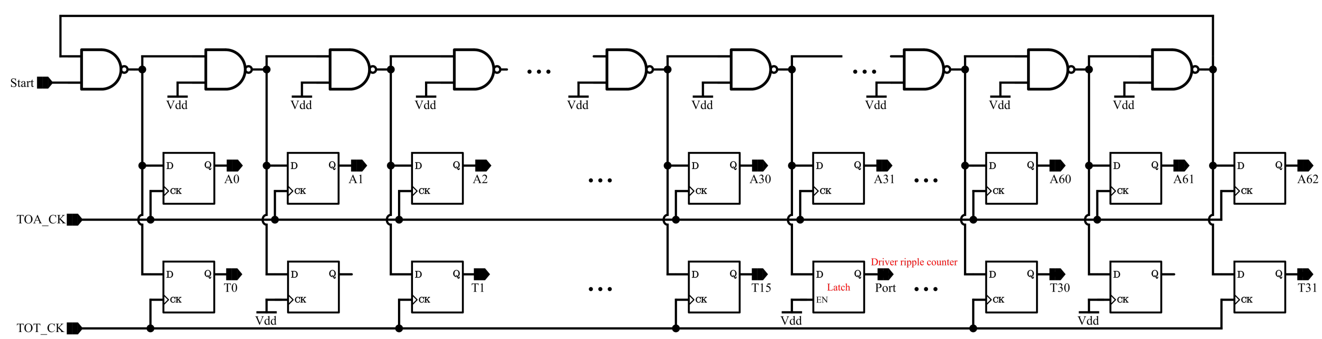

Figure 12: Schematic of 63 Tap Delay Line

When the Start is asserted, the NAND gated ring is oscillating with the period of 2.52 ns at post-layout simulation. The TOA_CK and TOT_CK are used to latch the TOA and TOT fine phase at the rising edge. The Start, TOA, and TOT signal are all generated by TDC Controller. The ripple counters was driven by the output of TOT Tap 31. The one is driven by the rising edge and the other one is driven by the falling edge of the output of TOT Tap 31.

3.3.3 Clock Tree Design

In order to decrease the clock skew and jitter of the TOA and TOT clock distribution on layout, we have adopted the most common and conservative clock distribution scheme, known as **T-tree**. The schematic of TOA clock T-tree is depicted as Figure 13.

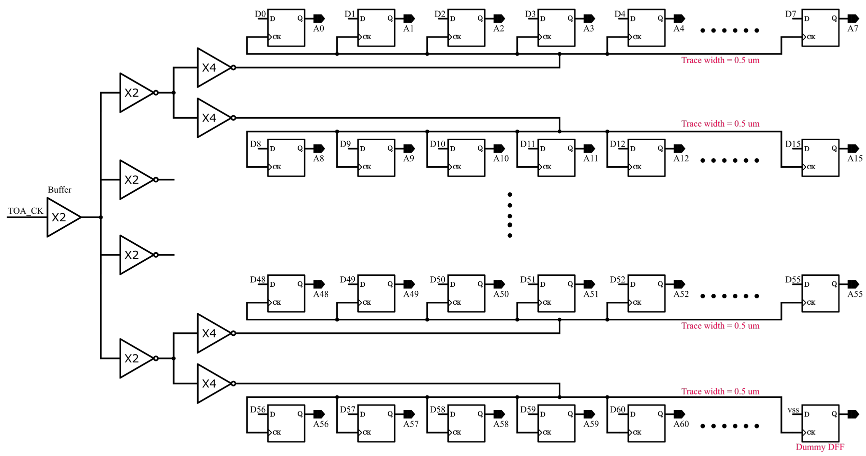

Figure 13: Schematic of TOA clock distribution

3.3.4 Coarse Counter

The TDC coarse counter that is a 3-bit ripple counter records the TDC delay line coarse phase. we used two ripple counter that have 180° to eliminate the metastability of itself. Figure 14 shows the schematic of coarse counter of delay line.

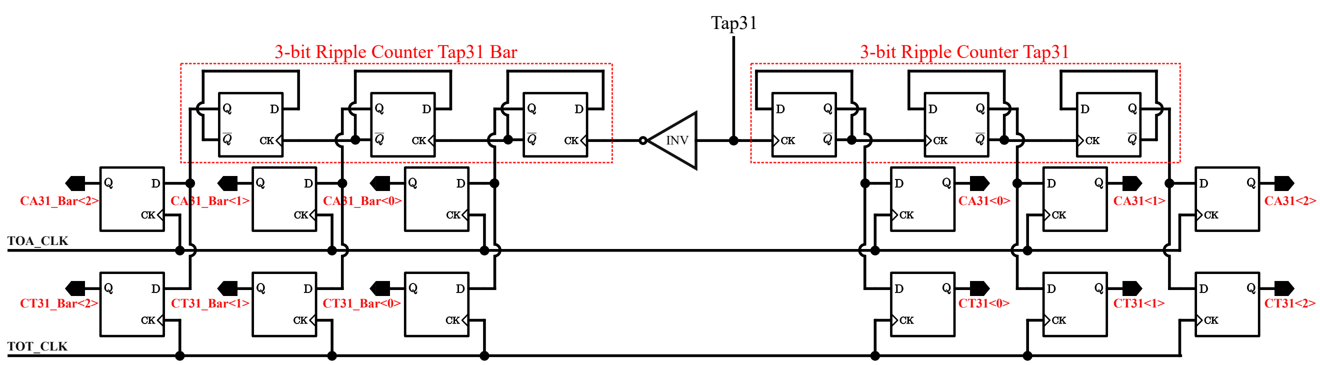

Figure 14: Schematic of TOA clock distribution

3.4 TDC Encoder

TDC Encoder is used to convert the TOA, TOT and Calibration sampling code into binary code (TOA is 10-bit, TOT is 9-bit and Calibration is 10-bit). The TOA and Calibration have the identical encoding logic. But the TOT encode logic is different form the TOA and Calibration encode logic. Each encode logic is pure combination logic. The block diagram of TDC encode is shown as Figure 15.

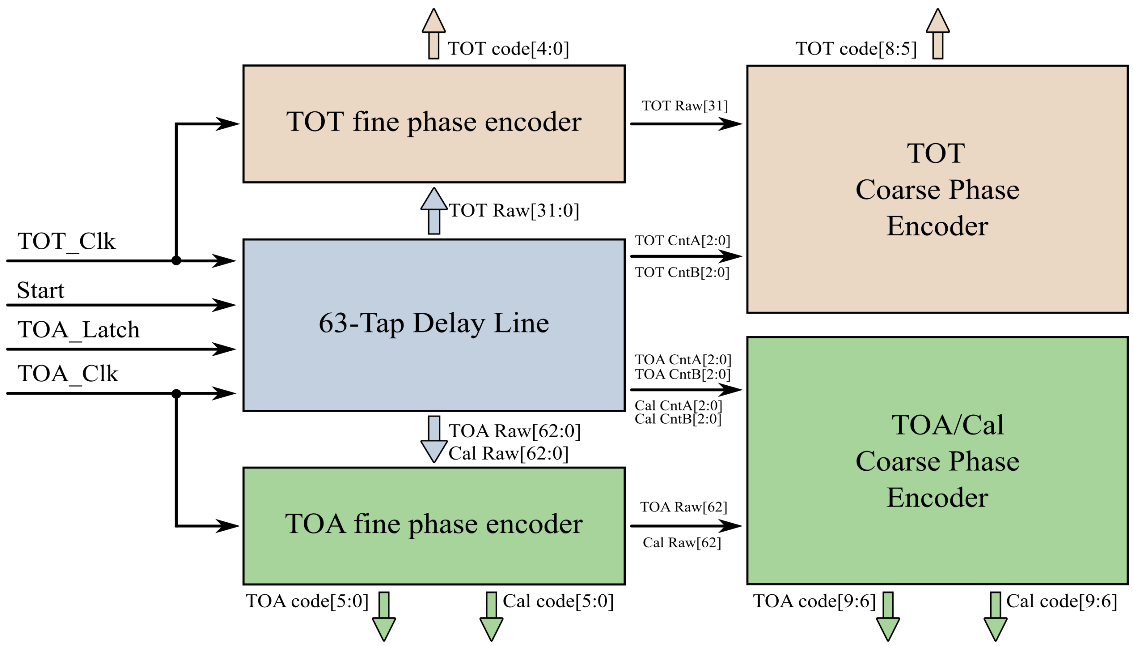

Figure 15: Diagram of Encoder logic

3.4.1 TOA and Calibration Encode Logic

The bit width of the TOA and Calibration raw data is 63 bits. The TOA and Calibration encoded fine phase data is used to select the reliable readout from the redundant counters as 3 bits coarse phase data to avoid potential metastability event. The Figure 16 shows the TOA and Calibration fine phase encode logic schematic.

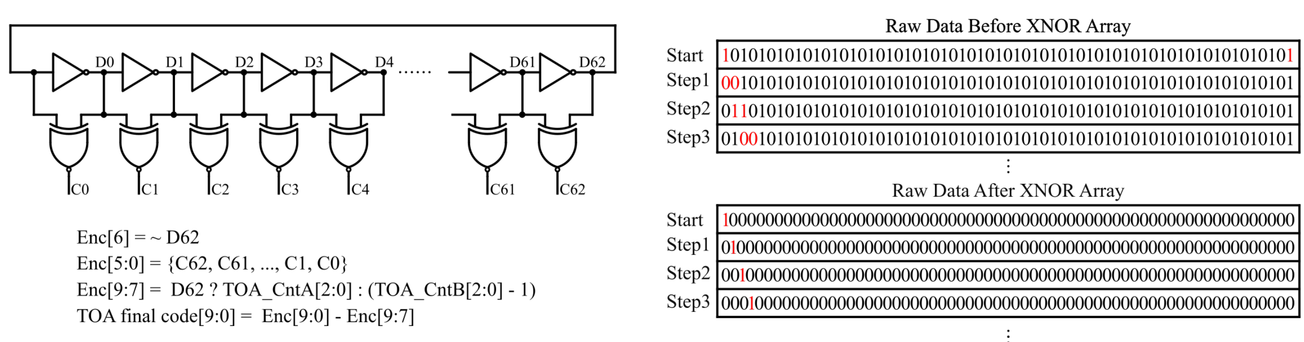

Figure 16: TOA/Cal fine phase encode logic

The inverse of the last digital of the MSB of the raw data is the phase data **Enc[6]**. 63 XNOR gates are used to generate 63 bits one-hot code which will be further encoded into 6 bits code **Enc[5:0]**. The raw data **D62** determines that which counter output is chosen by the TOA coarse phase encode logic as its input, so the **Enc[9:7]** is encoded by TOA_CntA[2:0] when D62 is equal to 1'b1 or {TOA_CntB[2:0] - 1} when D62 is equal to 1'b0. The final code **Enc[9:0]** equals **Enc[9:0] - Enc[9-7]** since the raw data after XNOR array is 63 bits.

3.4.2 TOT Encoder Logic

The bit width of the TOT raw data is 32 bits. The TOT encoded fine phase data is used to select the reliable readout from the redundant counters as 3 bits coarse phase data to avoid potential metastability event. The Figure 17 shows the TOT fine phase encode logic schematic.

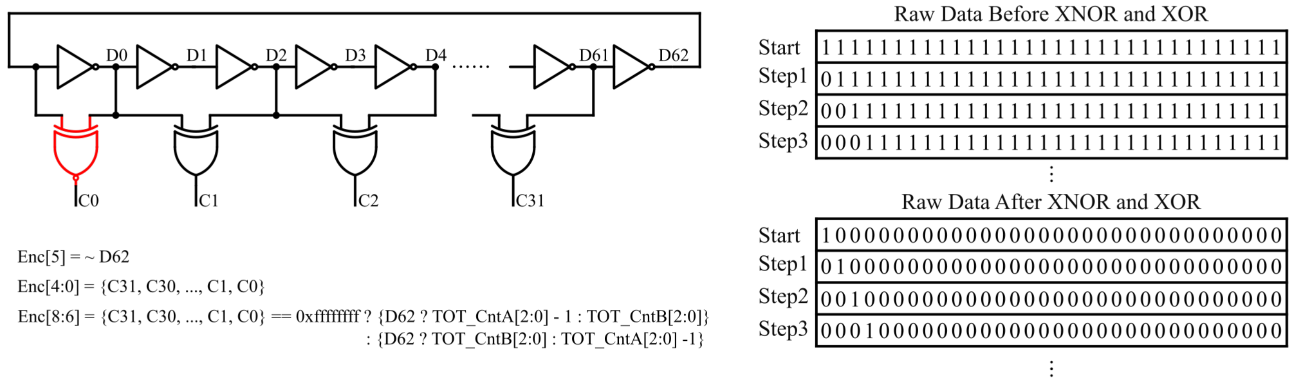

Figure 17: TOT fine phase encode logic

The inverse of the last digital of the MSB of the raw data is the phase data **Enc[5]**. One XNOR and 31 XOR gates are used to generate 32 bits one-hot code which is further encoded into 5 bits code **Enc[4:0]**. The raw data **D62** and {**C31, C30, ..., C1, C0**} commonly determine the **Enc[8:6]**.

3.4.3 Bubble Tolerance Logic

The one-hot code of TOA, Calibration, and TOT are encoded to 6 bits and 5 bits binary code by a pure combination logic with bubble tolerance function. The one-hot code to binary code encoder logic tolerates up to 3 **"1"** cluster in the one-hot code for robustness. The TOA one-hot code to binary code encode logic is shown as Figure 18.

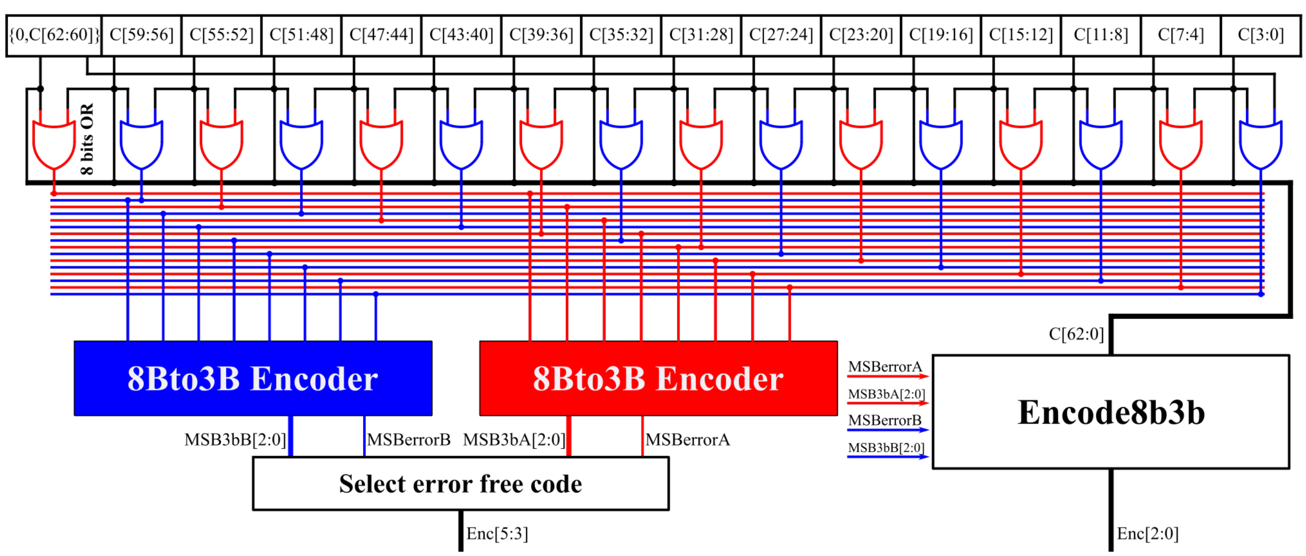

Figure 18: TOA bubble tolerance encode logic

The input of TOA bubble tolerance encode logic is 63 bits one-hot code C[62:0]. The two groups (GroupA and GroupB) of 8 bits input OR gates is to reduce resolution of one-hot code so its encode results as the **Enc[5:0]**. The **Enc[2:0]** comes from Encode8b3b encode logic.

The **Encode8Bto3B** encoder is a table-find logic. If there are more than one "1" in the 8-bit input, the encoder output error. Otherwise output 3 bits binary code of the one-hot input data. Two 8Bto3B Encoder in parallel but the input data are different. If there are not more than 4 continuous "1" in one-hot code at least one encoder is error free.

4 Diagnostic Mode Readout (DMRO)

The DMRO input comes form TDC Encoder ouput 30-bit data and its output is 1-bit high speed serial data. The DMRO block takes 30-bit data as the input at the rate of 40 MHz, scrambles the input data with the polynomial of $X^{58}+X^{39}+1$, adds two bits as the header of the word (**2'b10**), and finally serializes 32-bit word to a 1.28 GHz data stream. A PRBS7 generator is integrated for test ability consideration. MSB goes first when delivering a word serially. The Figure 19 shows the function block diagram of the DMRO.

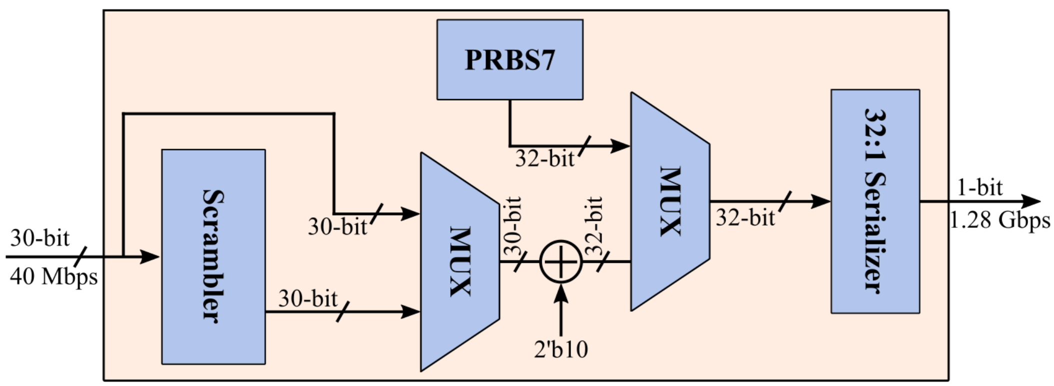

Figure 19: DMRO function block diagram

4.1 Scrambler

In telecommunications, a scrambler is a device that transposes or inverts signals encodes a message at the sender's side to make the message unintelligible at a receiver not equipped with an appropriately set descrambling device. Actually we use a polynomial of $X^{58} + X^{39} + 1$ to convert an input string into a seemingly output string of the same length, thus avoiding long sequences of bits of the same value. A scrambler is also referred to as a randomizer.

4.2 PRBS7 Generator

A pseudo-random binary sequence 7 (PRBS7) is integrated into the DMRO to test the function of the serializer. The PRBS7 sequence generating monic polynomials is $X^7 + X^6 + 1$. In this case, PRBS7 has a repetition period of 127 bits. When the DMRO **testMode** signal is asserted by user, the DMRO outputs the PRBS7 data.

4.3 Serializer

A high speed 32:1 serializer is also integrated into the DMRO to sent the TDC converted data to off-chip at 1.28 Gbps data rate speed. The serializer is completely implemented by digital flow.

5 Reference strobe Generator

TDC reference strobe generator is a block designed for arbitrary $\frac{1}{8}$ phase pulse generating. A $40\,\mathrm{MHz}$ clock is the reference clock. The rising edge of the $40\,\mathrm{MHz}$ clock is defined as the phase0. The synchronized $320\,\mathrm{MHz}$ clock and the delayed $40\,\mathrm{MHz}$ clock by DFF are used to generate the desired pulse. 8-bit control is adopted to select the output.

6 Clock Divider

The Clock Divider is a circuit that takes an input signal of a frequency, f_{in}, and generates an output signal of a frequency:

$$f_{out} = \frac{f_{in}}{n}$$

where n is an integer. The input signal frequency is $1.28\,\mathrm{GHz}$. The Clock divider has two output signals that are synthesised with the input signal, one is output signal of $320\,\mathrm{MHz}$ and the other is output signal of $40\,\mathrm{MHz}$. The Figure 20 shows the schematic of Clock Divider.

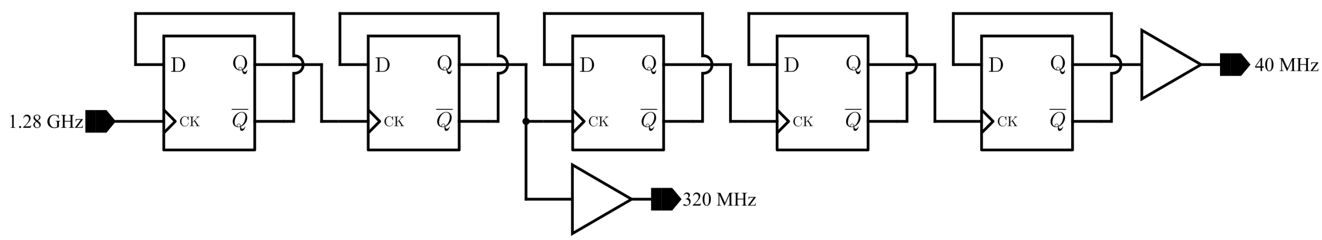

Figure 20: Clock Divider Schematic

7 Gated Ring Oscillator (GRO)

The Gated Ring Oscillator (GRO) is the test block that is used to test the specification and performance of the Delay Line. The Start signal controls the Gated Ring Oscillator and another signals keep high level. The output frequency is observed by Oscilloscope at different PVT.

8 I2C Interface

The ETROC1 TDC Test Block chip employs an I2C interface as slow control. The slave provides 32 bytes for writing and 16 bytes for reading by ETROC1. A 4-bit chip ID and a 4-bit chip reversion are available as well. The registers in the I2C are triplicated to mitigate SEU. The slave address is 7'b010001X (**0x22** or **0x23**), the LSB of the slave I2C address is determined by the external pad A0.

Table 2: ETROC1 TDC Test Block Chip I2C Register Map

NO.	**Name**	**Reg name**	**Description**	**Default value**	**Default value**
1	Dataout_disCMLDriver_BIAS	REG_00[0]	Disable Data output CML Driver	1'b0	0x00
2	Clk40Mout_disCMLDriver_BIAS	REG_00[1]	Disable Clk40M output CML Driver	1'b0	
3	TDC_offset$< 6 : 0 >$	REG_01[6:0]	TDC ripple counter meta-stability window offset	7'b0000000	0x80
4	TDC_enable	REG_01[7]	Enable TDC Controller	1'b1	

5	TDC_level$<2:0>$	REG_02[2:0]	TDC Encoder bubble tolerance	3'b001	
6	TDC_testMode	REG_02[3]	TDC test mode	1'b0	
7	TDC_selRawCode	REG_02[4]	Select TDC raw code, always "0"	1'b0	0x61
8	TDC_resetn	REG_02[5]	TDC reset signal	1'b1	
9	TDC_polaritySel	REG_02[6]	TDC controller output polarity select	1'b1	
10	TDC_autoReset	REG_02[7]	TDC automatic reset signal	1'b0	
11	Clk40Mout_AmplSel$<2:0>$	REG_03[2:0]	40 MHz clock CML output amplitude select	3'b001	
12	TDC_enableMon	REG_03[3]	Enable TDC raw data output	1'b1	0x19
13	TDC_timeStampMode	REG_03[4]	TDC Calibration data timeStamp mode	1'b1	
14	Dataout_AmplSel$<2:0>$	REG_04[2:0]	1.28 GHz Serial data output amplitude select	3'b001	
15	DMRO_testmode	REG_04[3]	DMRO test mode select	1'b0	
16	DMRO_enable	REG_04[4]	Enable DMRO	1'b1	0x51
17	DMRO_reverse	REG_04[5]	DMRO output data reverse	1'b0	
18	DMRO_resetn	REG_04[6]	DMRO reset, low active	1'b1	
19	DMRO_revclk	REG_04[7]	DMRO 40 MHz clock reverse	1'b0	
20	Dataout_Sel	REG_05[0]	1.28 GHz data output when asserted	1'b1	
21	Clk320M_Psel	REG_05[1]	320M pulse comes external pad when asserted	1'b1	
22	Clk40M_Psel	REG_05[2]	40M pulse comes external pad when asserted	1'b1	0x1F
23	Clk320M_Sel	REG_05[3]	320M clock comes internal when asserted	1'b1	
24	Clk40M_Sel	REG_05[4]	40M clock comes internal when asserted	1'b1	
25	Pulse_Sel$<7:0>$	REG_06[7:0]	320M clock pulse location select	8'b00000011	0x03
26	Clk40M_equalizer$<1:0>$	REG_07[1:0]	40M clock input eRx equalizer intensity	2'b00	
27	Clk40M_invertData	REG_07[2]	40M clock input eRx data invert	1'b0	
28	Clk40M_enableTermination	REG_07[3]	Enable 40M clock input eRx termination	1'b1	0x38
29	Clk40M_setCommonMode	REG_07[4]	Set 40M clock input eRx common mode	1'b1	
30	Clk40M_enableRx	REG_07[5]	Enable 40M clock input eRx	1'b1	
31	Clk320M_equalizer$<1:0>$	REG_08[1:0]	320M clock input eRx equalizer intensity	2'b00	
32	Clk320M_invertData	REG_08[2]	320M clock input eRx data invert	1'b0	
33	Clk320M_enableTermination	REG_08[3]	Enable 320M clock input eRx termination	1'b1	0x38
34	Clk320M_setCommonMode	REG_08[4]	Set 320M clock input eRx common mode	1'b1	
35	Clk320M_enableRx	REG_08[5]	Enable 320M clock input eRx	1'b1	
36	Clk1G28_equalizer$<1:0>$	REG_09[1:0]	1.28G clock input eRx equalizer intensity	2'b00	
37	Clk1G28_invertData	REG_09[2]	1.28G clock input eRx data invert	1'b0	
38	Clk1G28_enableTermination	REG_09[3]	Enable 1.28G clock input eRx termination	1'b1	0x38
39	Clk1G28_setCommonMode	REG_09[4]	Set 1.28G clock input eRx common mode	1'b1	
40	Clk1G28_enableRx	REG_09[5]	Enable 1.28G clock input eRx	1'b1	
41	Pulse_equalizer$<1:0>$	REG_0A[1:0]	TDC pulse input eRx equalizer intensity	2'b00	
42	Pulse_invertData	REG_0A[2]	TDC pulse input eRx data invert	1'b0	
43	Pulse_enableTermination	REG_0A[3]	Enable TDC pulse input eRx termination	1'b1	0x38
44	Pulse_setCommonMode	REG_0A[4]	Set TDC Pulse input eRx common mode	1'b1	
45	Pulse_enableRx	REG_0A[5]	Enable TDC Pulse input eRx	1'b1	
46	TDCRawData_Sel	REG_0B[0]	TDC Raw data group select	1'b1	
47	GRO_TOT_CK	REG_0B[1]	GRO TOT clock	1'b1	
48	GRO_TOTRST_N	REG_0B[2]	GRO TOT reset, low active	1'b1	
49	GRO_TOA_Latch	REG_0B[3]	GRO TOA Latch clock	1'b1	0x3F

50	GRO_TOA_CK	REG_0B[4]	GRO TOA clock	1'b1	
51	GRO_TOARST_N	REG_0B[5]	GRO TOA reset, low active	1'b1	
52	GRO_Start	REG_0B[6]	GRO Start signal, high active	1'b0	
53	GROout_disCMLDriverBIAS	REG_0C[0]	Disable GRO output CML Driver	1'b0	0x02
54	GROout_AmplSel$< 2:0 >$	REG_0C[3:1]	GRO output CML Driver Amplitude select	3'b001	

TDC Test Block read-only register:

Table 3: ETROC1 TDC Test Block Read-only Register Map

NO.	**Reg name**	**TDCRawData_Sel=0**	**TDCRawData_Sel=1**
1	REG_20[2:0]	CalCounterBMon[2:0]	TOACounterBMon[2:0]
2	REG_20[5:3]	CalCounterAMon[2:0]	TOACounterAMon[2:0]
3	REG_20[6]	CalerrorFlagReg	TOAerrorFlagReg
4	REG_21[7:0]	TOT_codeReg[7:0]	TOARawDataMon[7:0]
5	REG_22[7:0]	TOA_codeReg[6:0], TOT_codeReg[8]	TOARawDataMon[15:8]
6	REG_23[7:0]	Cal_codeReg[4:0], TOA_codeReg[9:7]	TOARawDataMon[23:16]
7	REG_24[7:0]	Cal_RawDataMon[31:29], Cal_codeReg[9:5]	TOARawDataMon[31:24]
8	REG_25[7:0]	Cal_RawDataMon[39:32]	TOARawDataMon[39:32]
9	REG_26[7:0]	Cal_RawDataMon[47:40]	TOARawDataMon[47:40]
10	REG_27[7:0]	Cal_RawDataMon[55:48]	TOARawDataMon[55:48]
11	REG_28[6:0]	Cal_RawDataMon[62:56]	TOARawDataMon[62:56]
12	REG_29[7:0]	HitFlag, TOTerrorFlagReg, TOTCounterAMon[2:0], TOTCounterBMon[2:0]	
13	REG_2A[7:0]	CalRawDataMon[7:0]	TOTRawDataMon[7:0]
14	REG_2B[7:0]	CalRawDataMon[15:8]	TOTRawDataMon[15:8]
15	REG_2C[7:0]	CalRawDataMon[23:16]	TOTRawDataMon[23:16]
16	REG_2D[7:0]	$< *3 >$Low, CalRawDataMon[28:24]	TOTRawDataMon[31:24]
17	REG_2E[5:0]	DBF_QC[5:0]	RO_DBF_QC[5:0]

9 Test Contents

ETROC1 TDC Test Block chip is mainly used to test the specifications and features of the TDC. The TDC Test contents are listed as below.

1. **Power-up quick test**. Measeure the current and on-board voltage of each power voltage.Compare with the following expected values:
   - I_DMRO = $27\,\mathrm{mA}$
   - I_GRO = $13\,\mathrm{mA}$
   - I_IO = $9\,\mathrm{mA}$
   - I_TDC = $4\,\mathrm{mA}$
2. **I2C quick test**. Write the default values and check if read value are equal to written values. Check if chipID is 4'b0011. Check if chipREV is 4'b0001. Check if reg2F is 8'b0000_0000.

3. **Clock quick test**. Input 1.28 GHz, 320 MHz, 40 MHz clocks. Change the clock MUX settings and check clock outputs.
   - Clk320M_Psel: 320M Pulse clock comes from external or internal.
   - CLK40M_Pse; 40M Pulse clock comes from external or internal.
   - Clk320M_Sel: 320M clock comes from internal divider or external.
   - CLK40M_Se; 40M Pulse clock comes from internal divider or external.
   - Set the reference strobe (RefStrSel[7:0]). Check the reference strobe waveform.
   - Measure the GRO output frequency (about 793 MHz).
   - Measure jitter of each clock.
4. **Serializer quick test**. input clocks and set the DMRO in PRBS7 mode (TestMode = 1'b1 (REG_06[4]), ro_testmode = 1'b1). Observe the DOUT eye diagram. Measure eye opening and jitter. Check if the waveform is PRBS7.
5. **TDC quick test**. Input a fixed-width, fixed-phase pulse. Verify TOA and TOT results.
6. **TDC full test**. Input a variable-width, variable-phase pulse. Measure TOA and TOT.
   - Resolution
   - Calibration
   - INL and DNL
7. **GRO full test**. Measure frequency and frequency stability.
8. Power consumption of each functional blocks at differen operational conditions.

10 Test platform and steps