

Research Plan

Introduction of my background

My name is Wei Zhang. I am major in Particle Physics and Nuclear Physics at Central China Normal University (CCNU) from September 1, 2017 to now. And I will go to the Southern Methodist University (SMU), Dallas, Texas, as an exchange visiting scholar for half a year.

My field of research

Physical Electronics relates to board-level and chip-level electronic designs to perform signal-shaping, massive and high-speed data acquisition, data transmission, and data storage, which is widely demanded and used in various situations in our daily life or scientific experiments. For example, the high-speed Ethernet Switch, data acquisition system for different systems in industrial productions, scientific experiments, medical equipment, and consumer electronics, etc.

To fulfill the demands mentioned above, the Printed Circuit Board (PCB), the topological structure and Application Specific Integrated Circuit (ASIC) of electrical system should be elaborately designed to tackle with high-speed signals and large-scale data channels. These two aspects constitute the main contents about my research direction.

Advisor's information

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Advisor's Research in SMU

Jingbo Ye, the professor sponsoring and inviting me as visiting scholar, will be my research advisor in SMU. He is a Physics Research Professor for SMU's Data Link Group in Department of Physics, collaborates with many institutions such as CERN, is in the lead of this research in the high energy physics community worldwide. The optical link system that are being developed, based on the Gigabit Transceiver (GBT) and LOC ASIC families for the phase-I upgrade program of the LHC experiments, including ATLAS, are the state-of-the-art in the field. Optical links for phase-I will operate at 5 to 10 times faster than the current systems in the LHC experiments. For the LHC phase-II upgrade, SMU and CERN, together with other institutions, form the lpGBT (low power GBT) common project and are developing ASICs for optical links that will double the speed of those in phase-I.

My research plan in SMU

I will go to work with Professor Ye's group in SMU to develop their readout circuits for the CMS Endcap-Timing-Layer detector that will be installed during its upgrade for the High-Luminosity LHC

data taking period. This is a project supported by the US-CMS Operation (through the Fermi National Laboratory) with a very tight schedule. The first prototype fabrication of the readout circuits must be submitted in March 2019.

At the end of my research in SMU, several high quality research papers are expected to be written and published. When I finish my research in SMU, I will go back to China to continue my Ph.D. study in CCNU. These papers would be important for me to get further personal development when I am back to CCNU.

To achieve the above mentioned research objectives, I arranged the research as follows, Time schedule and approach for the research:

- **September 15, 2018 to September 30, 2018**

Be familiar with the local environment. Search and read papers related to my research. Start the integrated circuit design for CMS Endcap-Timing-Layer detector.

- **October 1, 2018 to February 15, 2019**

Layout the design after comprehensive simulation and examination, and submit the DGS to foundry to tape out. write the design documents and user's guide. Design test PCB board and prepare test firmware and software.

- **February 16, 2018 to March 15, 2019**

Participate in the chip test and analyze the results of the test whether it is expected. Write the paper that will be published.

My return plan

After returning to China, the work at CCNU will be mainly focused on the following items:

- Make a further improvement on my work.
- Document all the work done in a clear and friendly way in a technical report both for future research and team partners or younger students in the lab.
- Finish a Ph.D. dissertation as a scientific report which should address research motivation problems, strategy methods and results of the project.