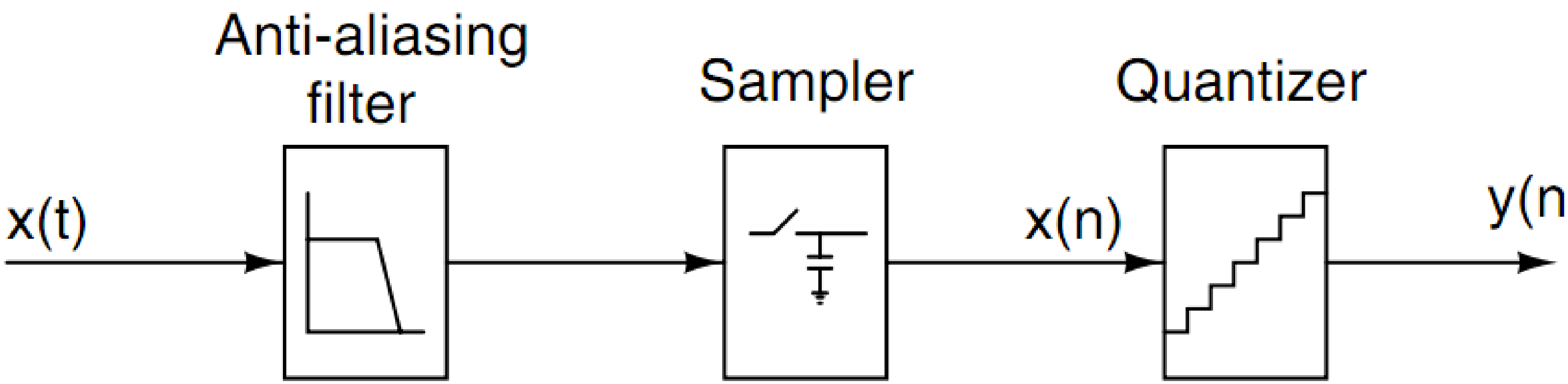
Principles of Sigma-Delta ADC

Quan Sun

Outline

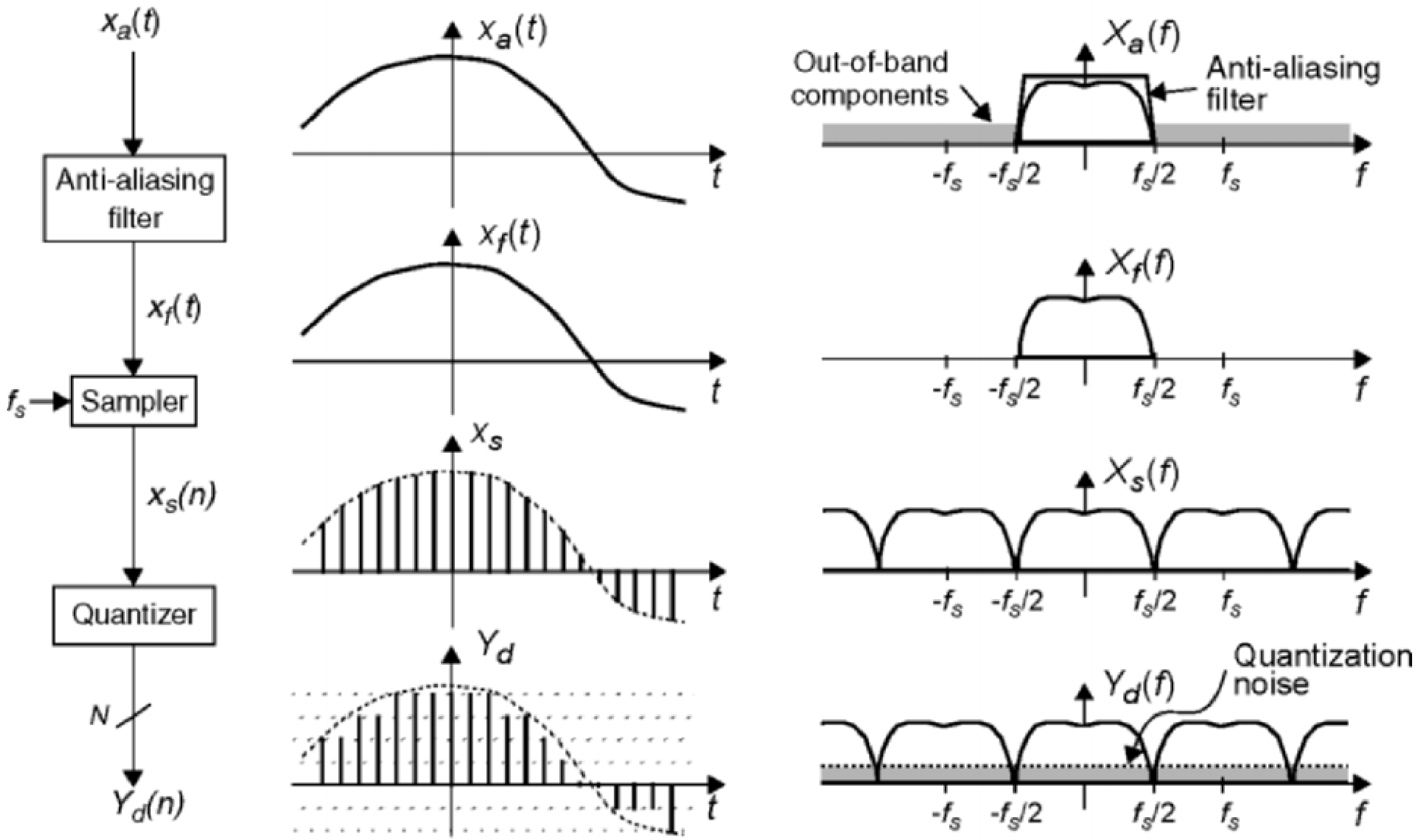
- Nyquist-rate Analog-to-Digital Converters
- Sigma-Delta Analog-to-Digital Converters
- 1st-order SD Modulator
- 2nd-order SD Modulator

Nyquist-rate A-to-D Converter



Operating at nyquist-rate :fs = $2f_b$ → high-order analog anti-aliasing filter
2^N discrete-value level mapping → hard to implement for large N

Nyquist-rate ADC Signal Flow

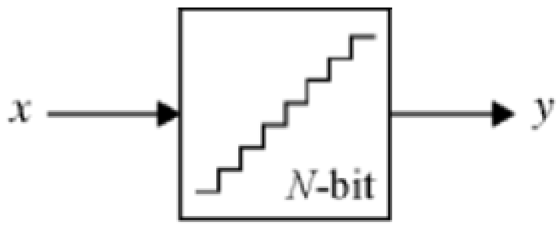


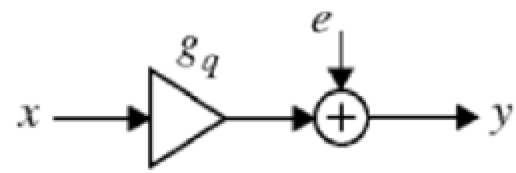
signal flow

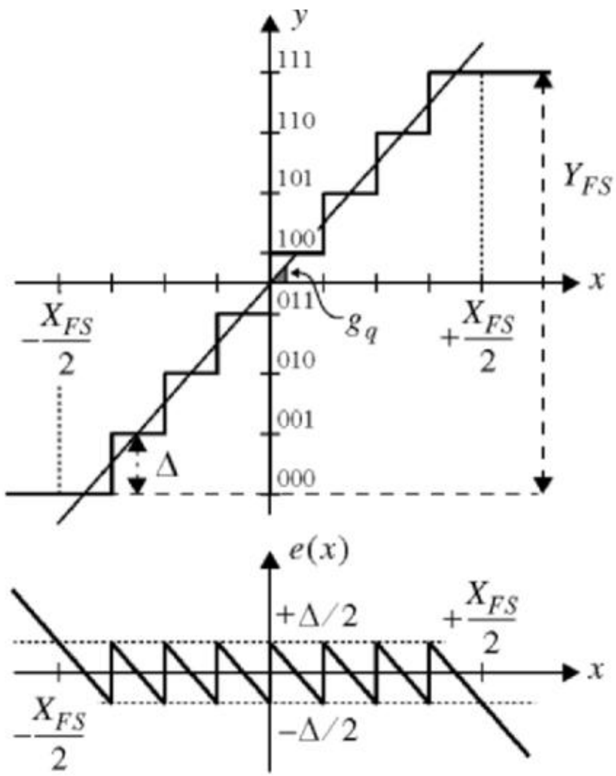
time domain

frequrecy domain

Quantization Noise(1)







$$y = g_q x + e(x)$$

g_q: quantizer gain
e(x): quantization noise, a non-linear function of input x
Δ: quantization step, $\Delta = Y_{FS}/(2^N - 1)$

e(x)~U(- Δ/2 , Δ/2): input is assumed to change randomly from sample to sample in the interval $\pm X_{FS}/2$

Quantization Noise(2)

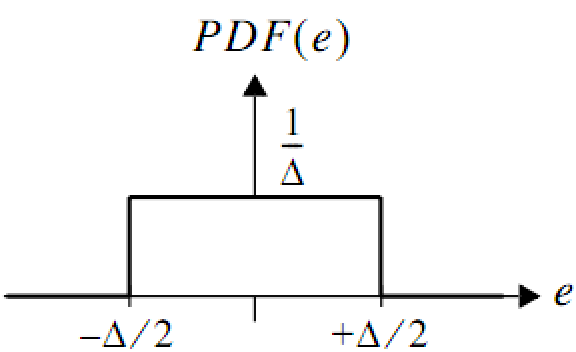
Power of e: $\overline{e^2} = \sigma^2(e) = \int_{-\infty}^{+\infty} e^2 PDF(e)de = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12}$

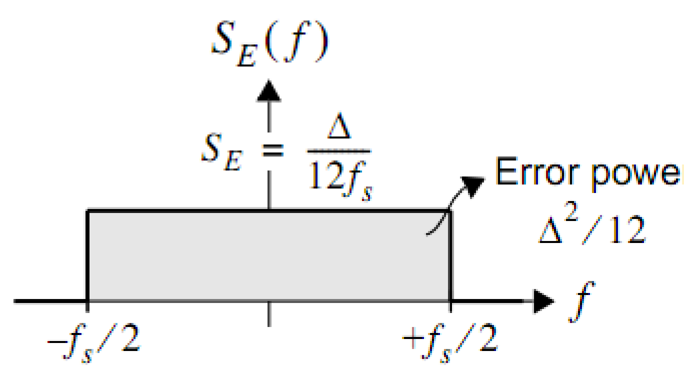
Power spectral density of e: $S_E(f) = \frac{\overline{e^2}}{f_s} = \frac{\Delta^2}{12 f_s}$

Signal bandwidth spreads over the band [-fs/2, +fs/2]

Power of in-band quantization noise: $P_Q = \int_{-f_b}^{f_b} S_E(f)df = \frac{\Delta^2}{12}$

SNR of a nyquist-rate ADC: $\frac{Y_{FS}^2}{8} \Big/ \overline{e^2} \approx \frac{3}{2} 2^{2N}$ → SNR|$_{dB}$=6.02N+1.72

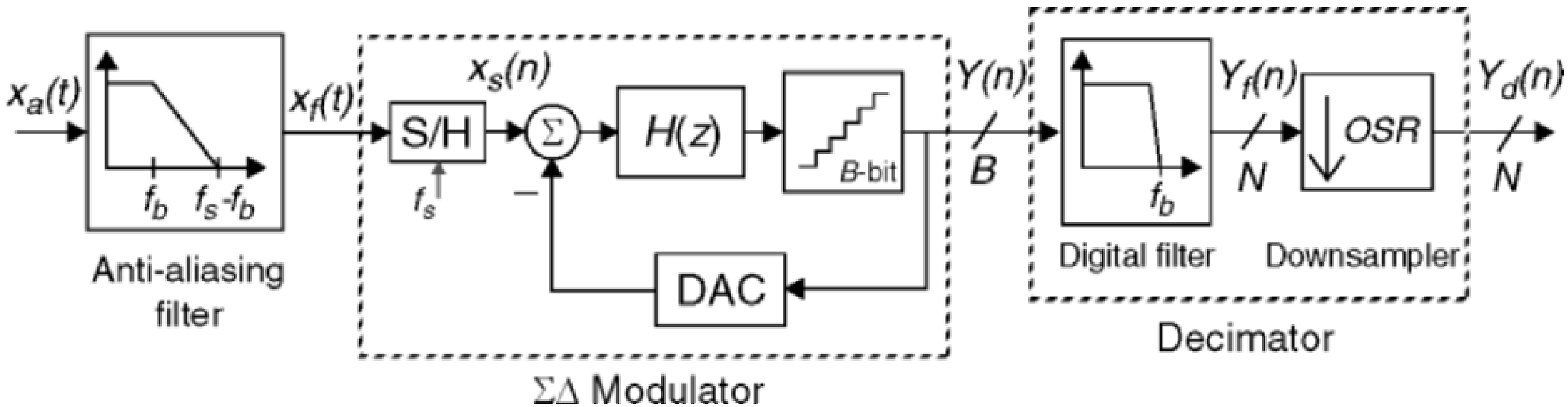




Summary of Nyquist-rate ADC

- Need for a high performance anti-aliasing filter to obtain high resolution and minimum distortion
- Hard to realize high resolution due to device mismatch

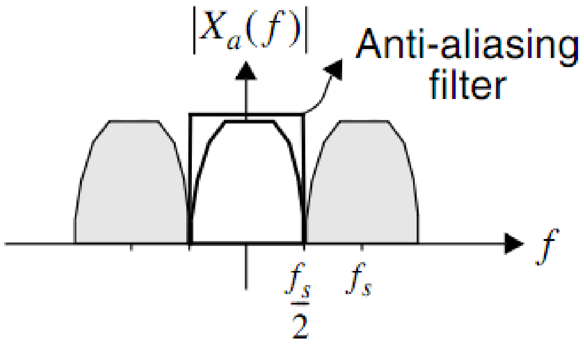
Sigma-Delta A-to-D Converter

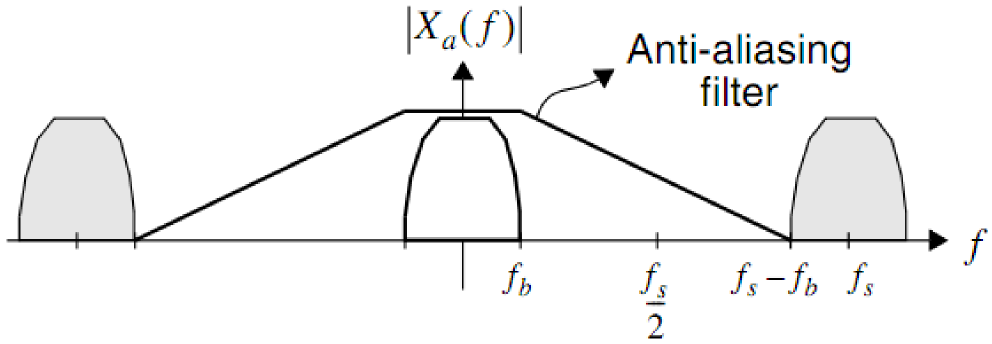


- ❑Modulator was proposed in 1962, not gained importance until development in digital VLSI
- ❑Using two basic ideas to increase the accuracy of A-to-D conversion:
  - ✓Oversampling: $OSR = f_s / f_N = f_s / 2 f_b$
  - ✓Noise-shaping: high-pass filter to decrease in-band quantization noise

Oversampling(1)

- Simplify anti-aliasing filter design
  - ✓ $f_b << f_s/2$ → frequency components in $[f_b, f_s - f_b]$ do not alias into signal band

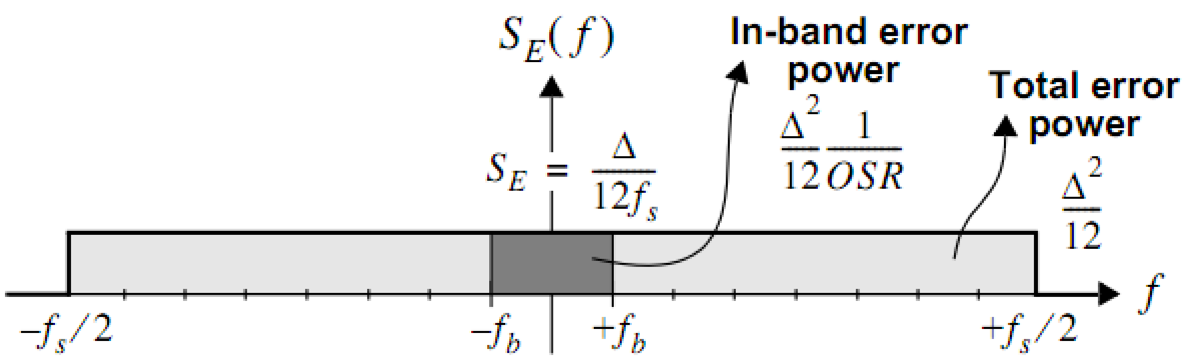




Oversampling(2)

- Push quantization noise to out-of-band
  - ✓ when a oversampled signal is quantized, the power of the quantization noise is still distributed in the range [$-f_s/2$, $f_s/2$], but only part of the total error is placed within the signal band.
  - ✓ In-band quantization noise power: $P_Q = \int_{-f_b}^{+f_b} S_E(f)df = \int_{-f_b}^{+f_b} \frac{\Delta^2}{12 f_s} df = \frac{\Delta^2}{12OSR}$
  - ✓ SNR of a oversampling ADC:

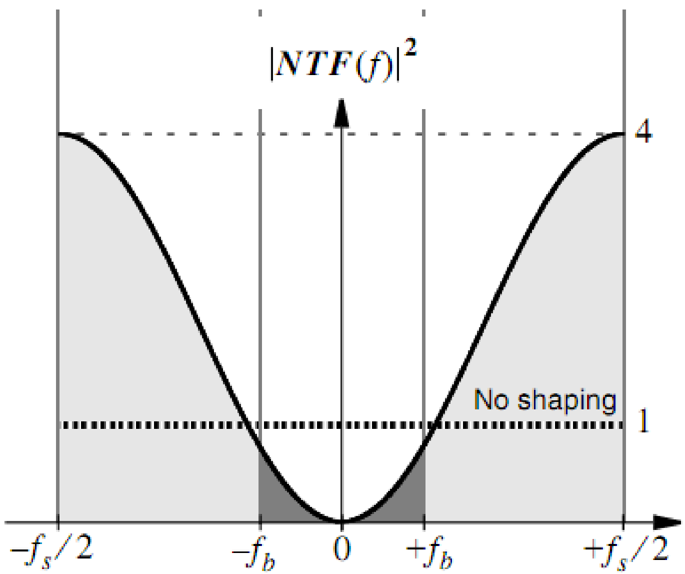
$$SNR = \frac{3}{2} 2^{2N} OSR \rightarrow SNR|_{dB} = 6.02N + 1.72 + 10\log_{10}(OSR)$$



Noise-shaping

- in-band quantization noise can be further reduced by high-pass filtered.
  - ✓ A simple first-order filtered noise: $e_{hp}(n)=e(n)-e(n-1)=e(n)(1-z^{-1})$
- General noise transfer function: $NFT(z)=(1-z^{-1})^L$
- Quantization noise power after apply oversampling and noise-shaping:

$$P_Q=\int_{-f_b}^{+f_b}\frac{\Delta^2}{12 f_s}NTF^2(f)df \approx \frac{\Delta^2}{12}\cdot\frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}}$$

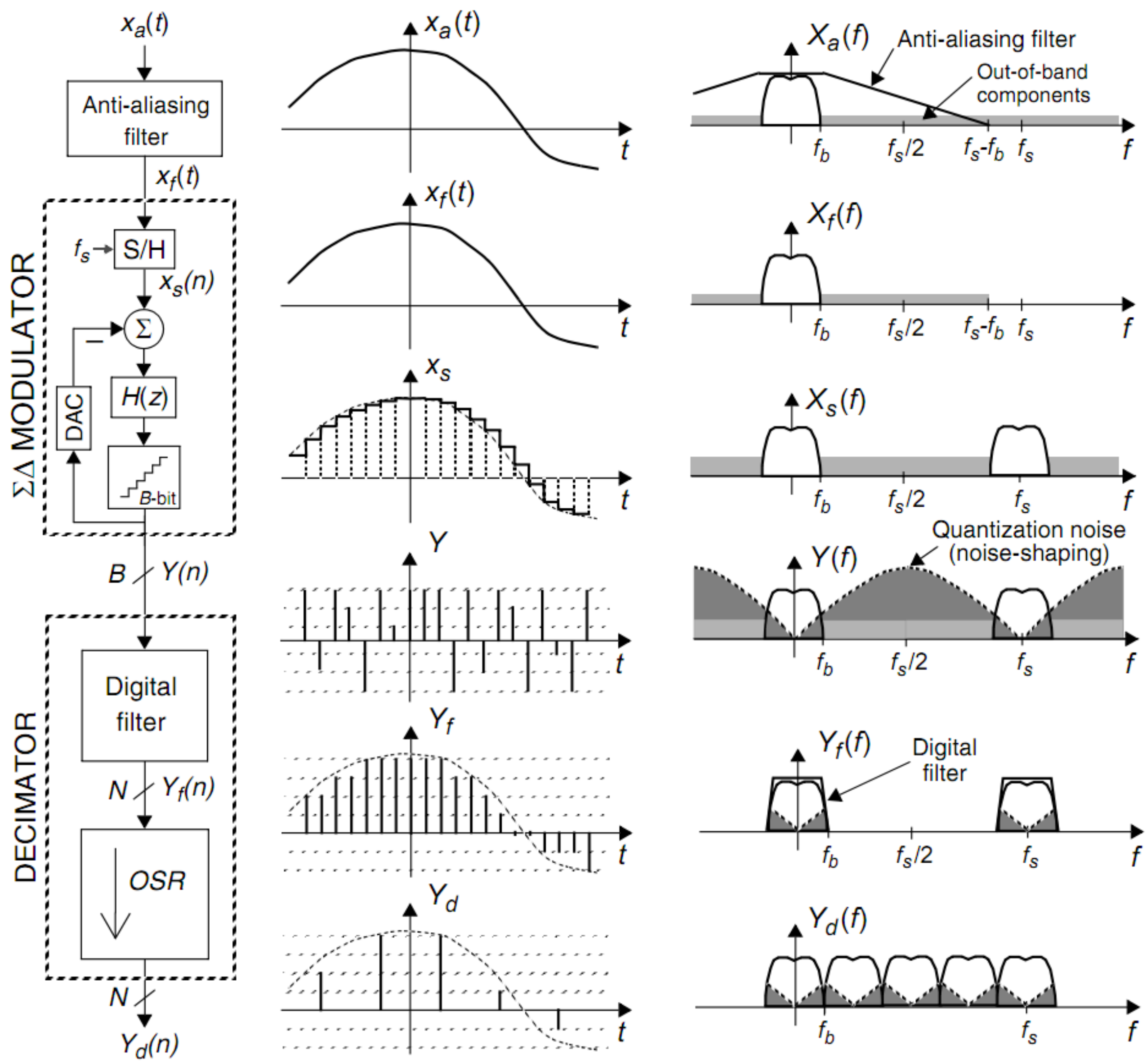


SNR of a ADC with oversampling and noise-shaping(Sigma-Delta):

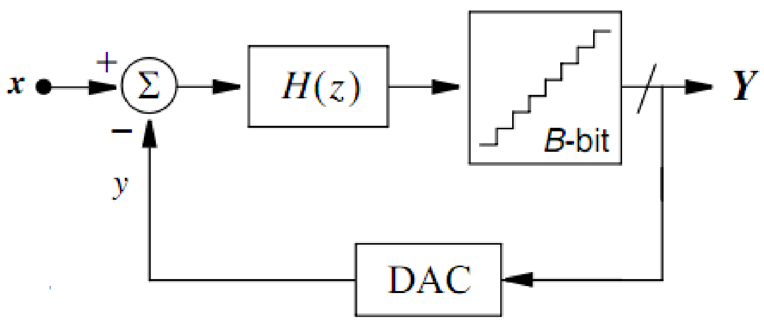
$$SNR=\frac{3}{2}2^{2N}\frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}}$$

$\rightarrow SNR|_{dB}=6.02N+1.72$
$+10\log_{10}(2L+1)/\pi^{2L}$
$+(2L+1)10\log_{10}(OSR)$

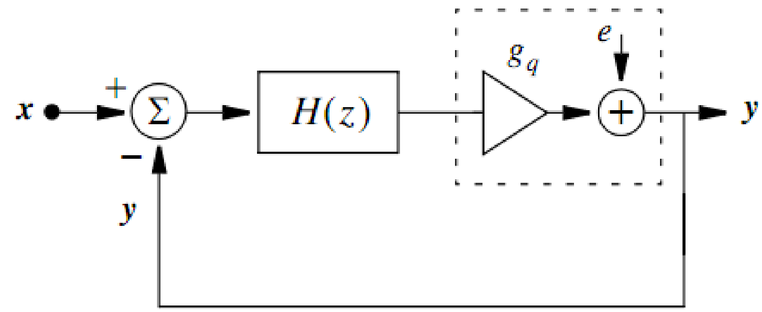
Sigma-Delta ADC Signal Flow



Sigma-Delta Modulator(1)



Basic architecture of SDM



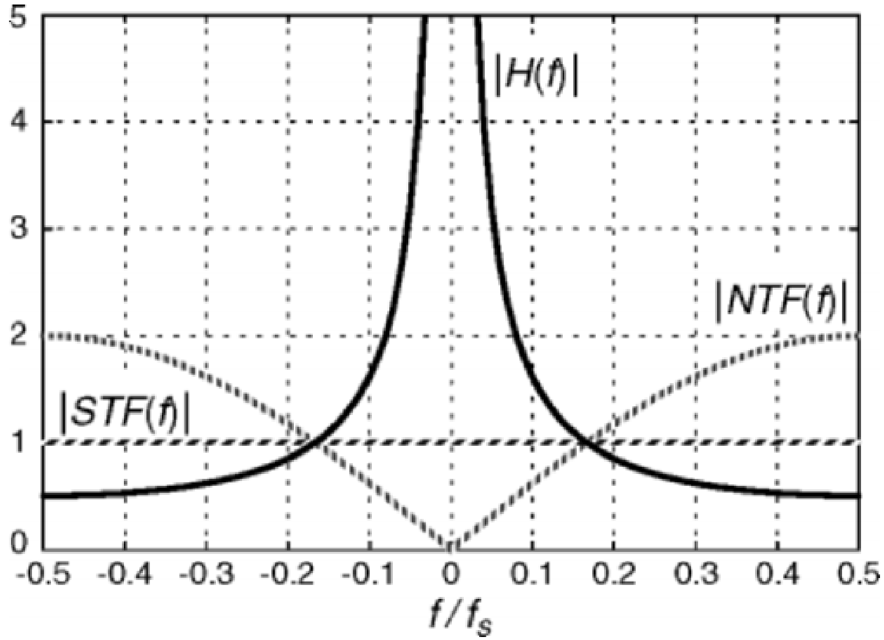
Linear model of SDM

- SDM is the ultimate responsible for the accuracy of A-to-D conversion
- SDM can be viewed as a 2 inputs(x,e), one output(y) system with TF:

$$Y(z) = STF(z)X(z) + NTF(z)E(z)$$

$$STF(z) = \frac{g_q H(z)}{1 + g_q H(z)} \qquad NTF(z) = \frac{1}{1 + g_q H(z)}$$

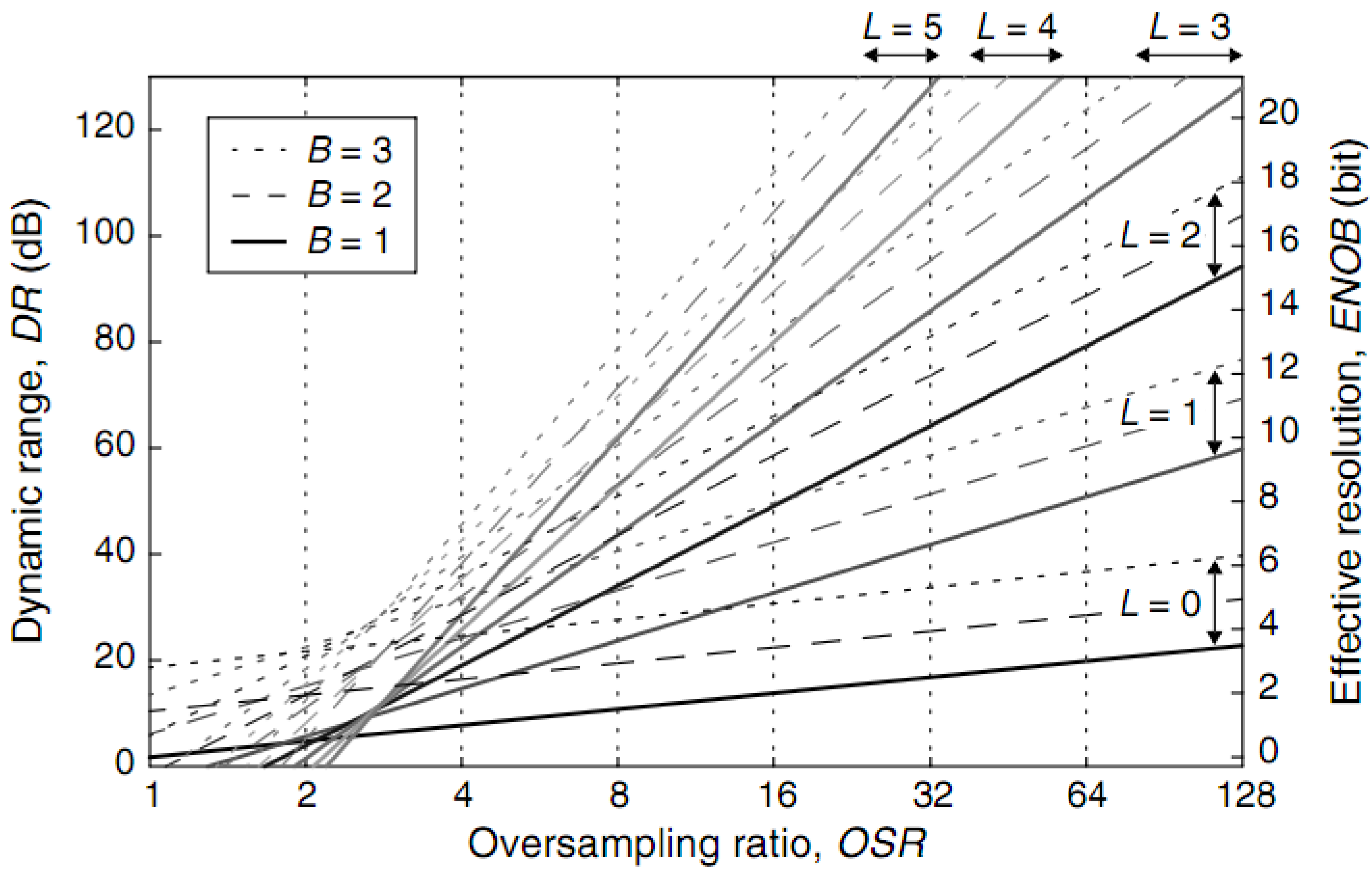
Sigma-Delta Modulator(2)



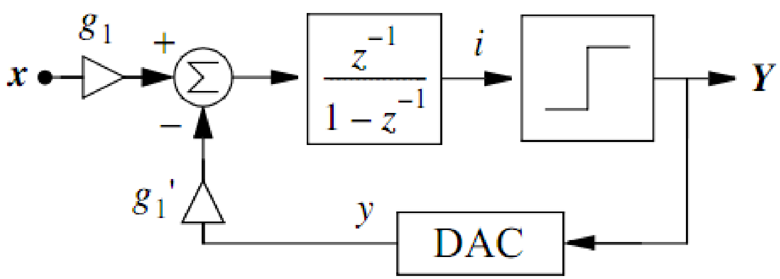
- Using a loop filter with large gain within signal band:

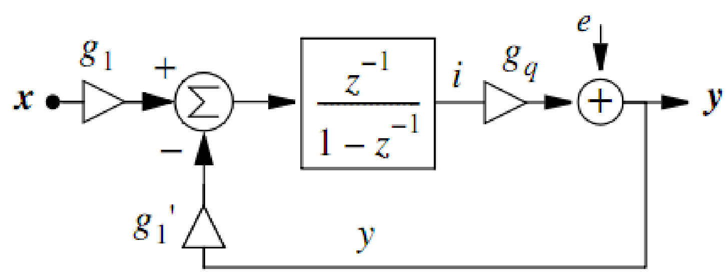
$$STF(z) \approx 1$$
$$NTF(z) = \frac{1}{1 + g_q H(z)} << 1$$

Sigma-Delta Modulator(3)



1st-order SD Modulator(1)



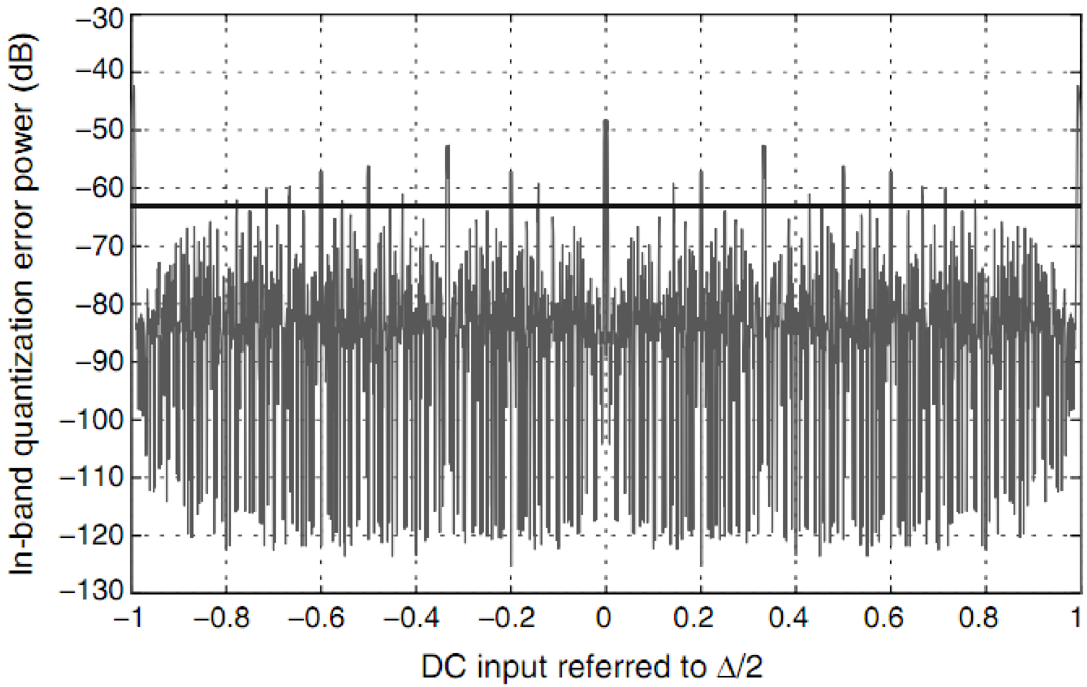


$$Y(z) = \frac{g_1 g_q z^{-1} X(z) + (1 - z^{-1}) E(z)}{1 - (1 - g_1' g_q) z^{-1}}$$

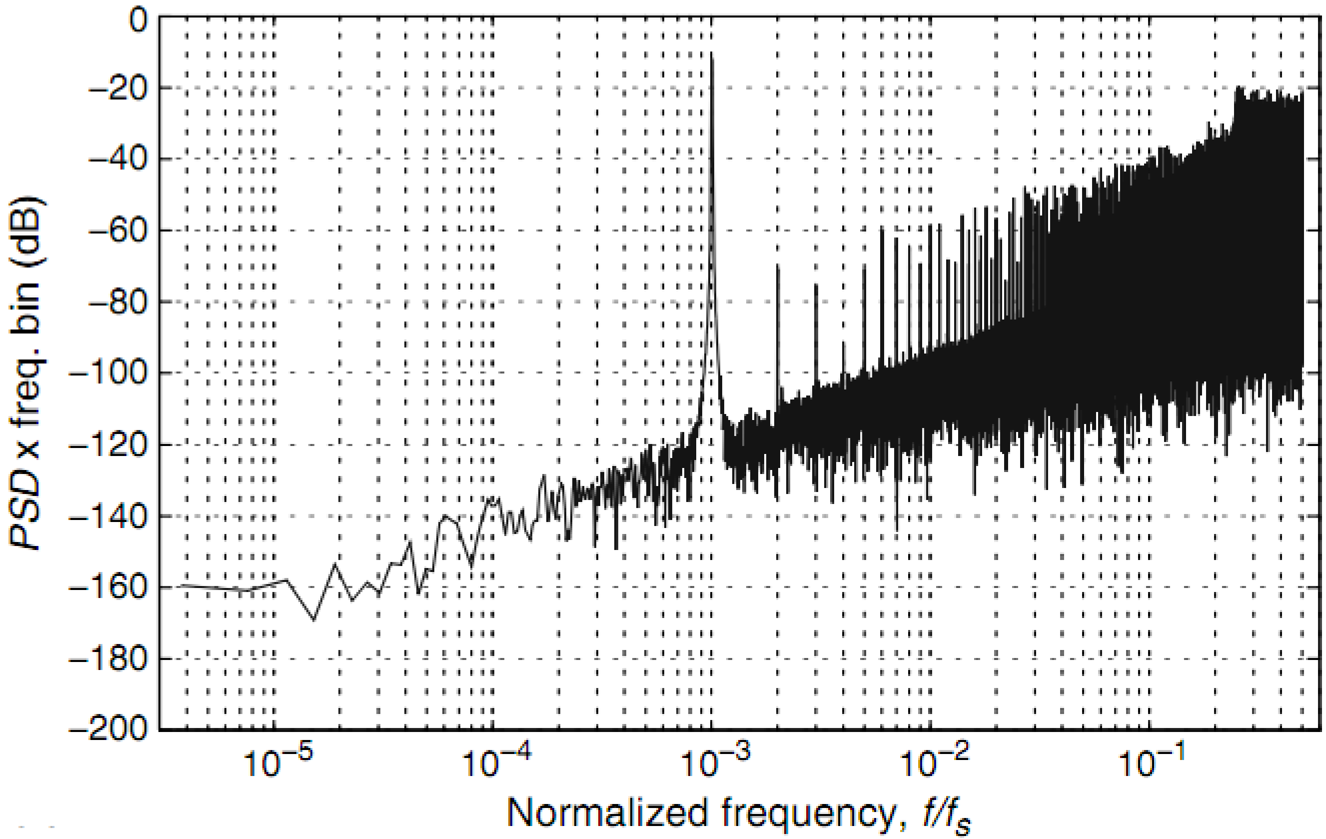
$$g_1' g_q = 1 \qquad \Rightarrow \qquad Y(z) = \frac{g_1}{g_1'} \cdot z^{-1} X(z) + (1 - z^{-1}) E(z)$$

1^{st}-order SD Modulator(2)

- Pattern noise or idle tone present when DC applied to 1^{st}-order SDM

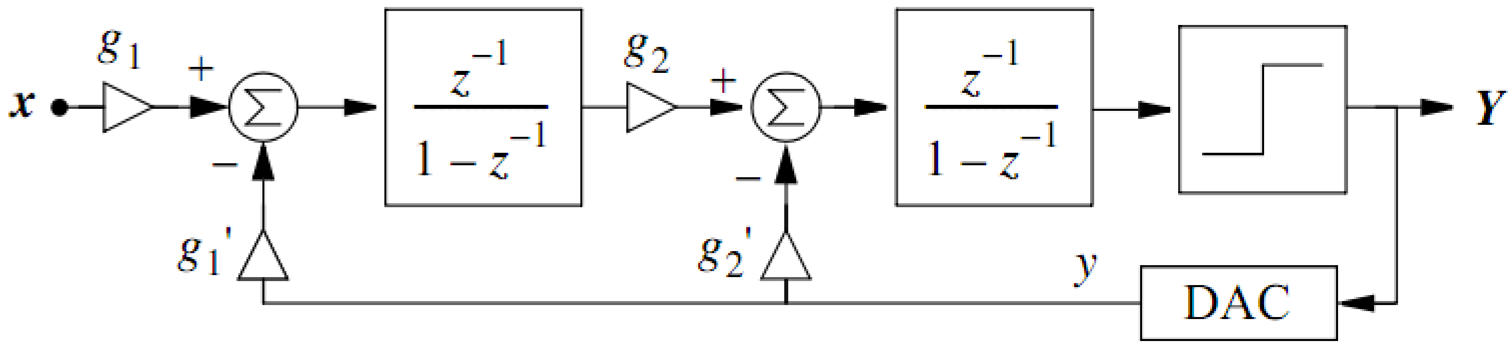


1st-order SD Modulator(3)



g1=g1’=1, OSR=128, Δ=2

2nd-order SD Modulator(1)



$$Y(z) = \frac{g_1 g_2 g_q z^{-2} X(z) + (1 - z^{-1})^2 E(z)}{1 + (g_2' g_q - 2) z^{-1} + (1 + g_1' g_2 g_q - g_2' g_q) z^{-2}}$$

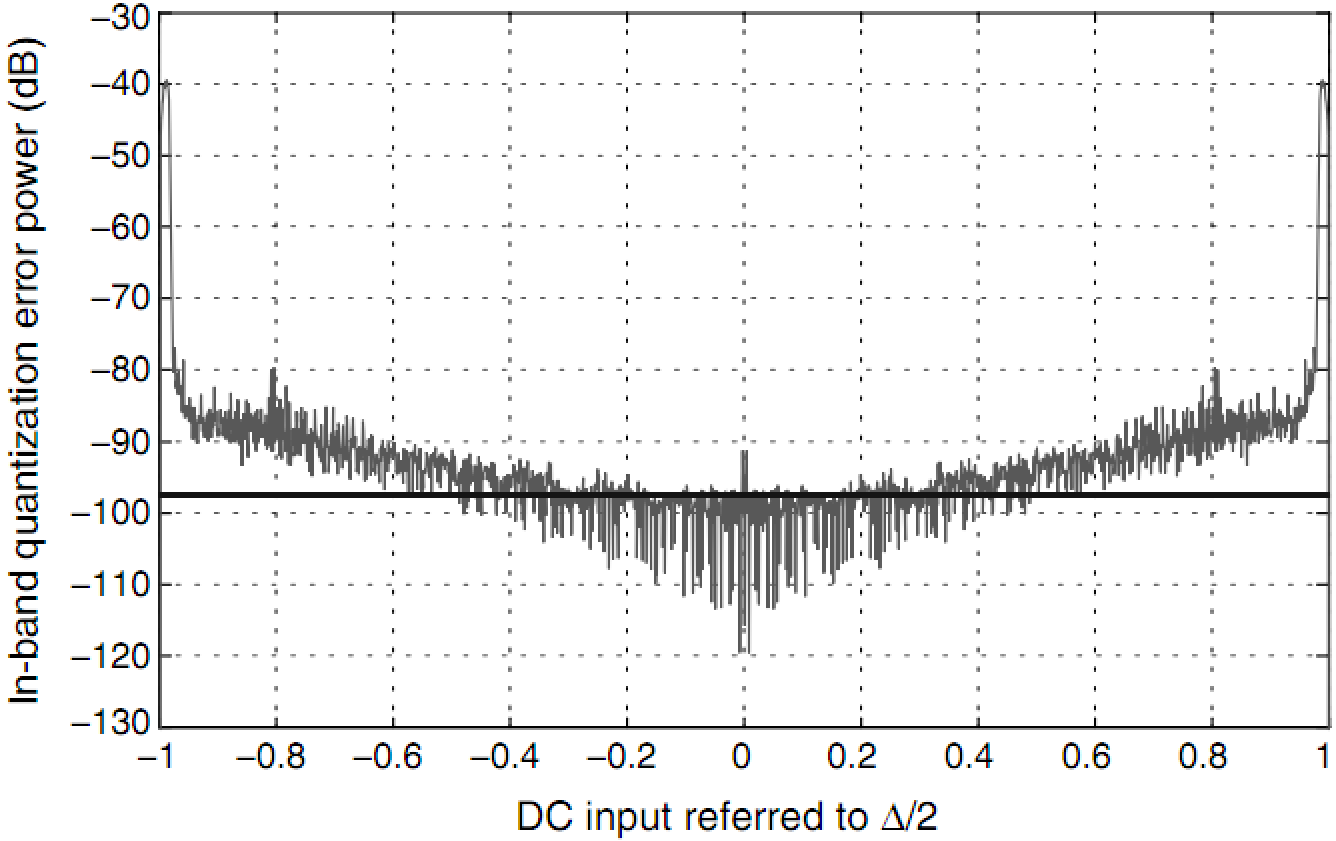
$$\left.\begin{aligned} g_1' g_2 g_q &= 1 \\ g_2' &= 2 g_1' g_2 \end{aligned}\right\} \Rightarrow Y(z) = \frac{g_1}{g_1'} \cdot z^{-2} X(z) + (1 - z^{-1})^2 E(z)$$

2^{nd}-order SD Modulator(2)

- Parameters should be selected carefully, some of important concerns:
  - ✓ Stability: 2^{nd}-order SDM is stable for input in the range[-0.9Δ/2, 0.9Δ/2], if $g_2' > 1.25 g_1 g_2'$
  - ✓ Easy to implement: integrator realized by SC circuits, consider match and area
  - ✓ Minimizing integrator output: supply, power consumption.

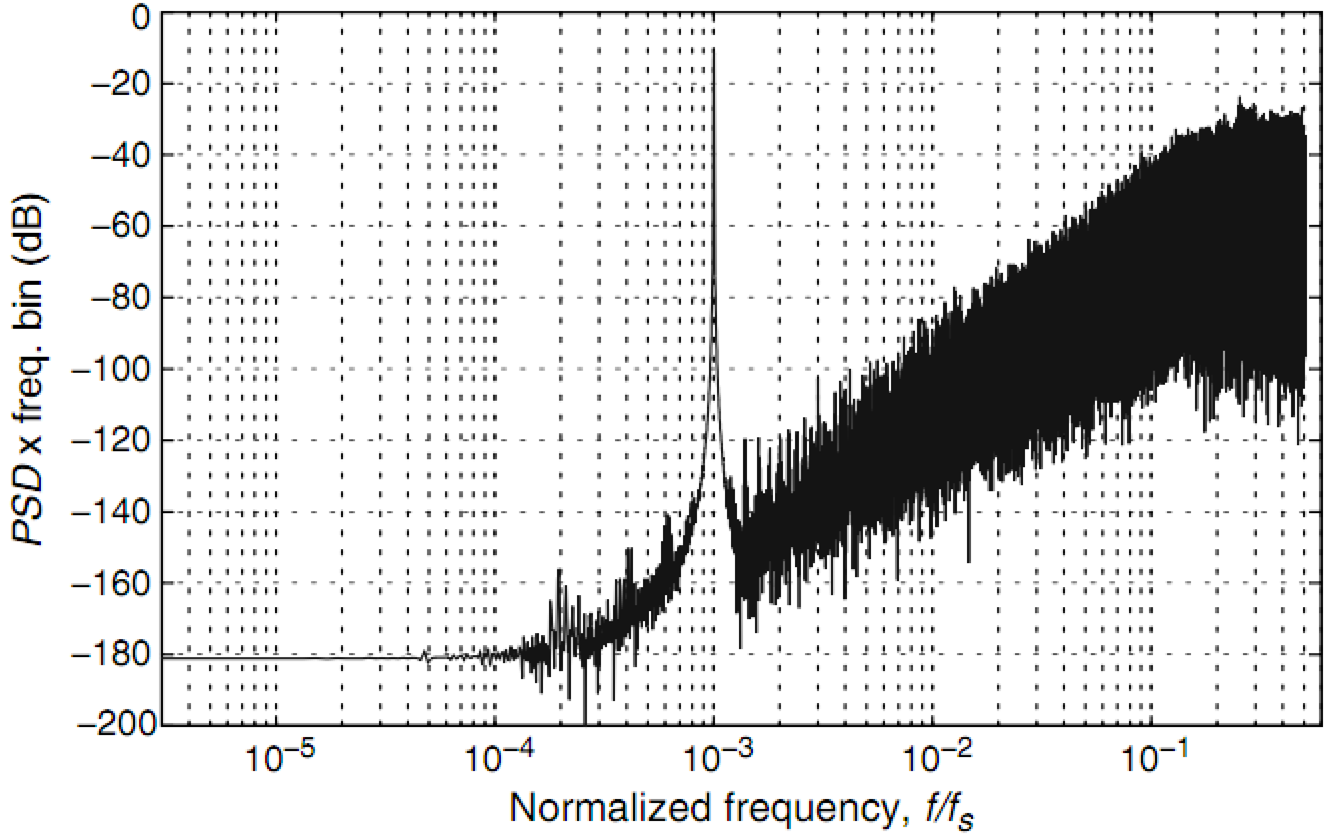
Selecting the coefficients of a SDM involves solving several trade-off among architectural, circuital, and technological aspects of the practical implementation.

2^{nd}-order SD Modulator(3)



g1=g1'=0.5, g2=g2'=0.5, OSR=128, Δ=2

2^{nd}-order SD Modulator(4)



g1=g1'=0.5, g2=g2'=0.5, OSR=128, Δ=2