

Characterization of the column-based priority logic readout of Topmetal-II CMOS pixel direct charge sensor

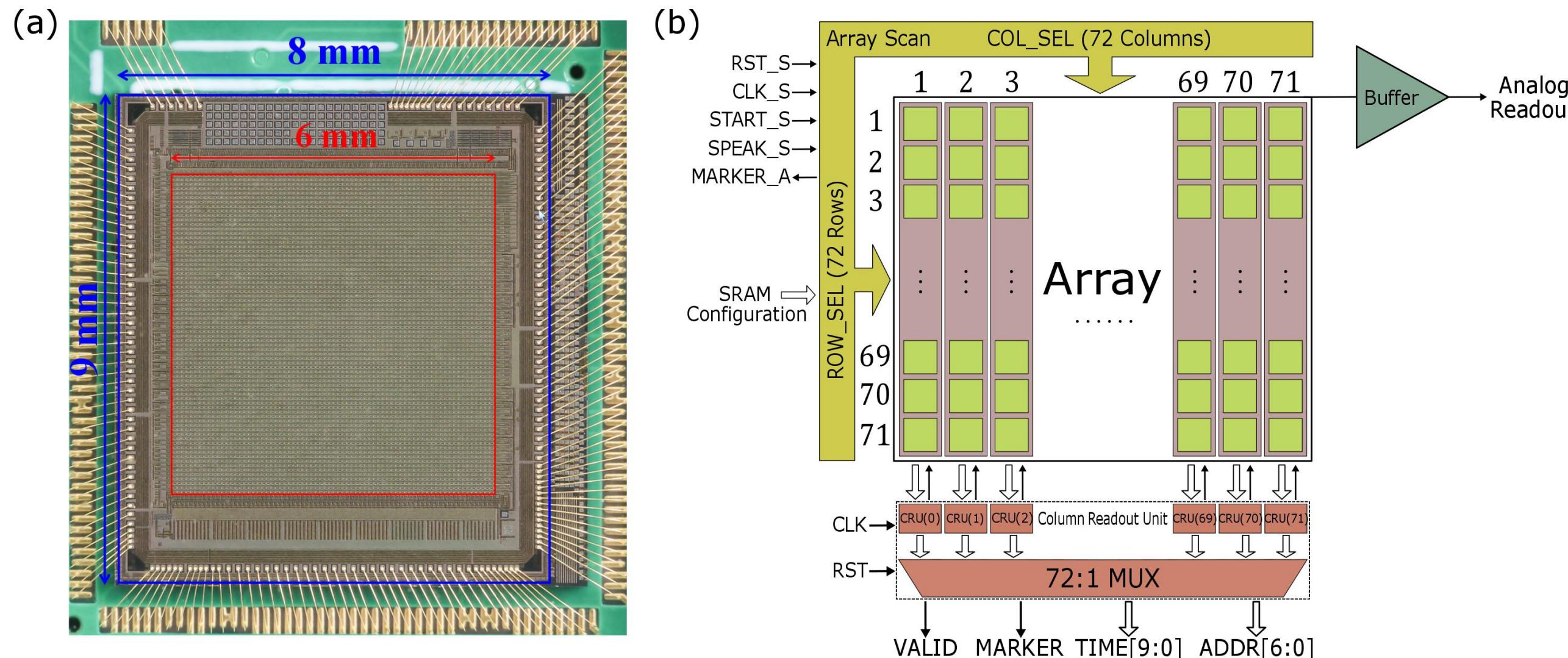
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Introduction

Topmetal-II is a highly pixelated sensor with $83\text{ }\mu\text{m}$ pitch between 72×72 pixels fabricated in a standard 350 nm CMOS technology without post-processing for direct charge collection and imaging through exposed metal electrodes in the topmost metal layer. In addition to the time-shared multiplexing readout of the analog output from Charge Sensitive Amplifiers (CSA) in each pixel, hits are also generated by pixel-local comparator with adjustable threshold and read out via a column-based priority logic, pertaining both hit location and time information.

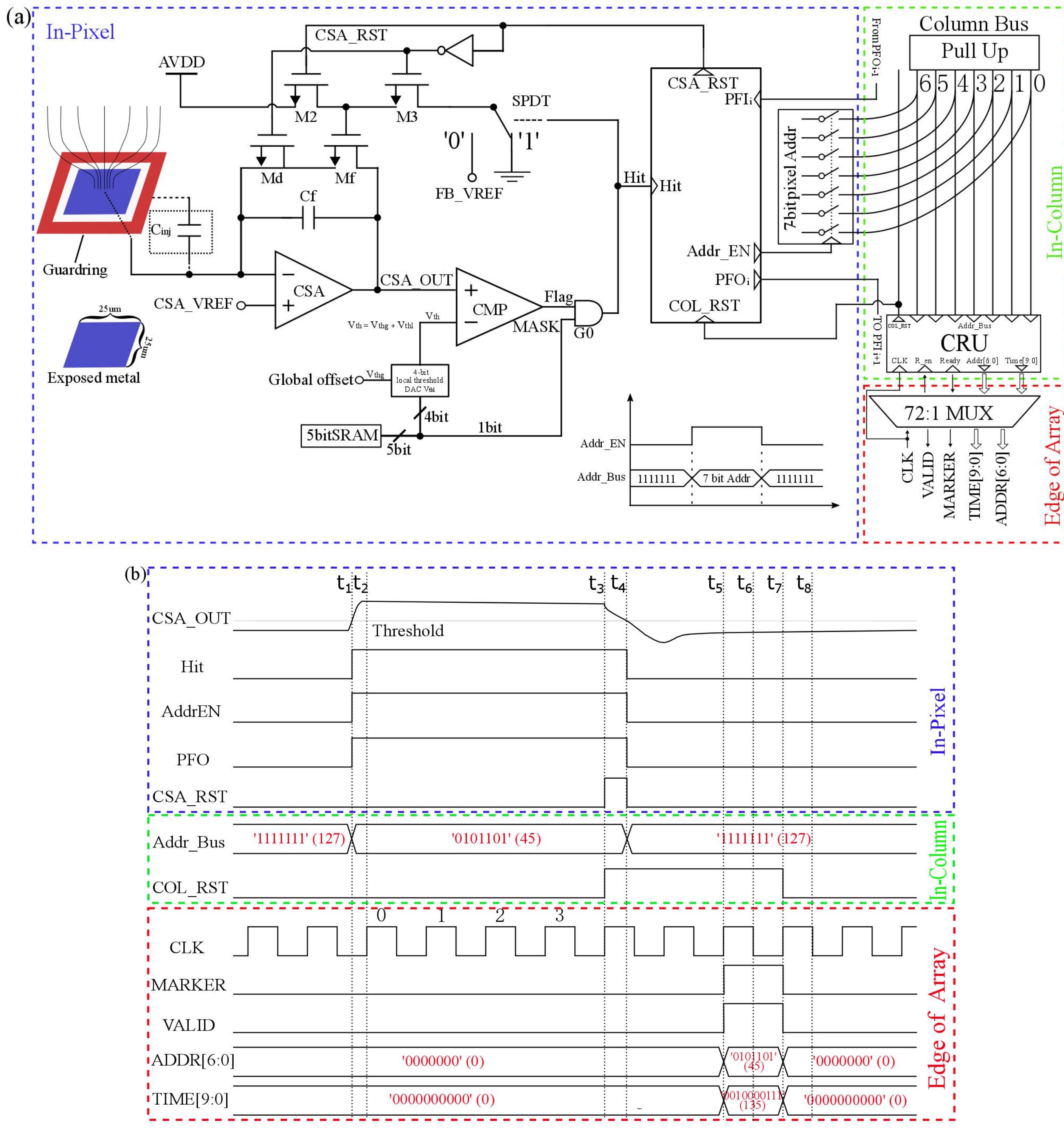
We study the detailed working behavior and performance of this readout scheme and demonstrate its potential in imaging applications.

Sensor photograph and Top-level block diagram



A photograph of one fully fabricated and wire-bonded *Topmetal-II* sensor is shown in Fig. (a), and its top-level block diagram is shown in Fig. (b). The sensor measures $8 \times 9\text{ mm}^2$ (blue box in Fig. (a)), in which a $6 \times 6\text{ mm}^2$ charge sensitive area (red box in Fig. (a)) containing 72×72 pixels is located in the center of the chip. Major functional units of the sensor are depicted in the top-level block diagram. The analog output from each pixel is fed to a single output Buffer via an array-wide row/column multiplexing circuitry. The digital output (hits) is registered at the each Column Readout Unit (CRU), then shipped off the sensor via a $72 : 1$ Multiplexer(MUX).

Single pixel structure and Timing diagram



The inner structure of the digital readout pathway from a single pixel to the edge of array is shown in Fig. (a). Structures at pixel, column and edge of array levels are indicated in the blue, green and red dashed boxes, respectively.

- **In-Pixel:**
- Exposed metal electrode and Guardring: A ring electrode (Guardring), which is in the same topmost metal layer as the *Topmetal*, surrounds the exposed metal electrode while being isolated from it.
- Charge Sensitive Amplifier (CSA): The CSA with $C_f = 5.1\text{ fF}$ (design value) converts the injected charge to voltage signal (CSA_OUT) and feeds it into the comparator.
- Comparator: The comparator compares CSA_OUT to a threshold(V_{th}) set by a pixel-local 4-bit DAC (V_{th}) on top of a common offset (Global offset V_{thg}) that is globally adjustable. ($V_{th} = V_{thg} + V_{th}$). When the threshold surpasses CSA_OUT, the Flag signal will be set to high.
- Priority logic: Each priority logic is a fully combinational logic that controls the CSA's reset upon the readout of a hit and drives the hit information through the column structure.

- **In-Column:**
- The 7-bit pixel local address will be delivered to the Column Bus when the Addr_EN signal is high.

- Each priority chain is terminated by a Column Readout Unit (CRU) at the bottom of the column, which is a sequential logic that shares a synchronous CLK with MUX.

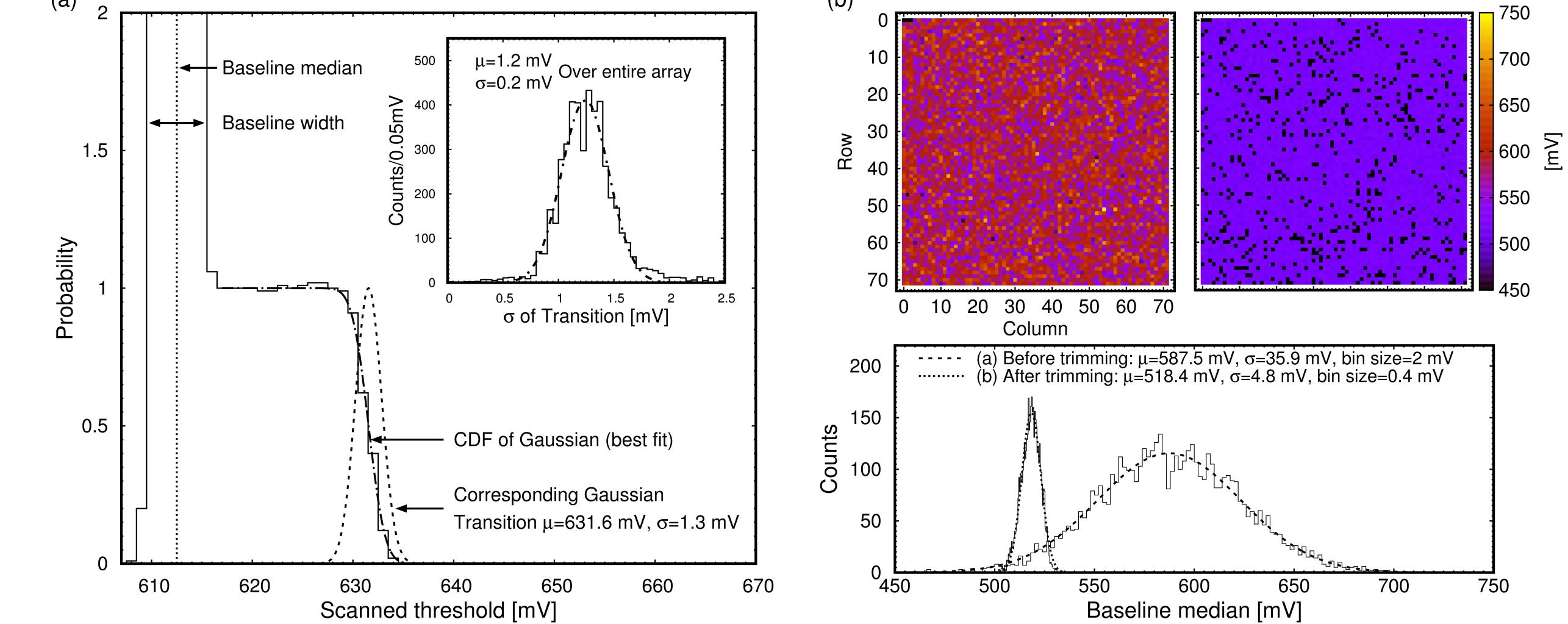
➤ Edge of Array:

- The multiplexer(MUX) sucessively polls every CRU with a synchronous CLK and ships the hit pixel's location and time information off the sensor.

Fig. (b) indicates the relevant signal activities during a hit and its readout. we assumed that the pixel located in the No. 45 column was hit and at this moment the time counter equals 0010000111_2 (135_{10}).

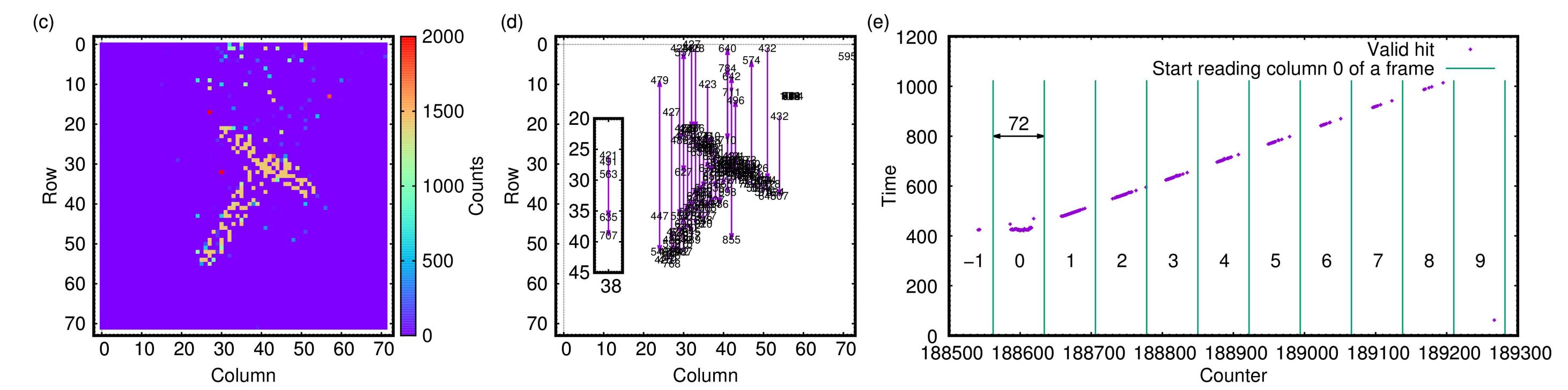
Experiments and Results

At the beginning of the test process, we disable all the 4-bit DACs. As shown in Fig. (a), an S-curve of a single pixel obtained by scanning the global offset (V_{th}) while recording the corresponding probability for the comparator and the subsequent logic to register a hit given a test pulse on the Guardring. Insert in Fig. (a) illustrates the distribution of the width of the transition (6). The width (6) of transition, which is an indicator of the noise of CSA output presented to the comparator, has a mean value of 1.2 mV . Baseline median distribution across the array in 2D and 1D histogram before and after trimming with a 4-bit DAC in every pixel is in Fig. (b). The results show a greatly reduced width in baseline median distribution.



After trimming with the optimized setting, we use a purple light LED to illuminate a *Topmetal-II* sensor. The purple light LED was placed $\sim 2\text{ cm}$ above the sensor and driven by a train of narrow pulses with $10\text{ }\mu\text{s}$ width and 50 ms interval. The sensor was covered by an opaque photo mask with a transparent T-shaped pattern. The T-shaped pattern is aligned with the center of the sensor.

We recorded many frames of hits induced by plenty of LED pulses. Hit location and time information are reconstructed from data that was collected by the Data Acquisition System. An image showing the T-shape is depicted in Fig. (c).



The Fig. (d) shows that time stamps printed at the location of corresponding pixels resulting from one light pulse. The T-shaped light hit pattern is clearly visible. Arrows connect hits in the same column, pointing from lower to higher time values. Insert in Fig. (d) illustrates the readout of column No. 38. In Fig. (e), the light pulse arrives at each pixel simultaneously, the initially registered time, which is from the highest priority pixel, is the same for all the CRUs. Only the hit time of the highest priority pixel is physically meaningful. It is worth noting that starting from the second-highest priority pixel, the time difference between the i th-priority pixel and the $(i+1)$ th-priority pixel in the same column equals the number of columns (72), which is the time interval between consecutive reads for a given CRU.

Conclusions and Outlook

We have successfully verified the behavior and performance of a column-based priority logic readout in the *Topmetal-II* sensor. Both the electrical measurements and imaging applications proved the validity of the readout scheme.

In the current design, although the in-array combinational logic can ship the hit pixel's address to the edge of the array with minimal latency, the sequential logic of the CUR and the MUX limits the time that is more than one clock to discover the hit information. To reduce the readout latency, the analog readout channel and combinational logic could be designed at the edge of the array to detect the activities in the Address Bus promptly. At the same time, the MUX could be replaced by fully combinational logic. We will investigate these options in future *Topmetal* sensor development in addition to improving the array uniformity.

Acknowledgments and References

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References

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