

Design of Multi-bit Sigma-Delta Modulators for Digital Wireless Communications

Bingxin Li

Stockholm, 2003

Submitted to KTH, Royal Institute of Technology, in partial fulfillment of the requirements for the degree of Doctor of Technology.

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Wireless Communications

ISBN 91-7283-641-5

ISRN KTH/IMIT/LECS/AVH-03/10--SE

ISSN 1651-4076

TRITA-IMIT-LECS AVH 03:10

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Kungl Tekniska Högskolan / Royal Institute of Technology
Department of Microelectronics & Information Technology
Laboratory of Electronics and Computer Systems
Electrum 229
SE-164 40 Kista
Sweden

Abstract

The ever advance of CMOS digital circuit process leads to the trend of digitizing an analog signal and performing digital signal processing as early as possible in a signal processing system, which in turn leads to an increasing requirement on analog-to-digital converter (ADC). A wireless transceiver is a such kind of signal processing system. Conventional transceivers manipulate (filter, amplify and mix) the signal mostly in analog domain. Since analog filters are difficult to design on-chip, the system integration level is low. Modern transceivers shift many of these tasks to digital domain, where the filtering and channel selection can be realized more accurately and more compactly. However the price for the high integration level is the critical requirement on the ADC, because the simplified analog part sends not only the weak signal but also the unwanted strong neighboring channel to the ADC. In order to digitize the needed signal in the presence of strong disturbances, a high dynamic-range and high-speed ADC is needed.

Sigma Delta ADCs are promising candidates for A/D conversion in modern wireless transceivers. They are naturally suitable for high-resolution narrow-band A/D conversions. With the development of processing and design techniques, sigma delta ADCs are expanding their applications to moderate-band area, such as wireless communication baseband processing. Currently mobile communication systems are migrating from 2G to 3G. In 2G systems the baseband width is in the order of hundred kHz, while in 3G systems the baseband width is in the order of MHz. To face the challenge of designing a high resolution sigma delta ADC with large bandwidth, a multi-bit internal quantizer is often used. In this thesis special design considerations on multi-bit sigma delta modulators are discussed. The biggest drawback of multi-bit sigma delta modulators is the need of an extra circuit to attenuate or compensate the internal multi-bit DAC non-linearity. This thesis provides a comprehensive analysis of the solution which combines a multi-bit quantizer with a 1-bit DAC in a sigma delta modulator. The theoretical analysis result is verified by measurement results. Another topic addressed in the thesis is how to reduce the multi-bit quantizer complexity. It is shown that by using a semi-uniform quantizer, the quantizer can reduce its complexity by one-bit yet still maintain the same modulator dynamic range. The performance of the semi-uniform quantizer is also verified by measurement results.

Acknowledgments

First I would like to thank my supervisor Professor Hannu Tenhunen for accepting me as a doctoral student in the Electronic System Design Laboratory (now LECS Lab). During all these years he has not only taught me on the subjects that I was working on, but also expanded my vision on the development of microelectronics science. It is a pleasant experience to study in the ESD Lab, which has a free and active atmosphere.

Thanks to Lena Beronius for all the excellent administrative work done for us. And also many thanks to Hans Berggren, Julio Mercado, Richard Andersson, and Peter Magnusson for maintaining a robust computer network and installing all the useful software for us.

Many thanks to all the nice and helpful colleagues Lirong Zheng, Li Li, Andreas Göthenberg, Johnny Öberg, Mikael Millberg, Xingzhong Duo, Meigen Shen, Zhonghai Lu, Yiran Sun and many others. The discussions with them broaden my knowledge and stimulate new ideas. Special thanks to Steffen Albrecht, Adam Strak, and Ana Rusu for their helpful comments to the thesis draft.

The author would like to thank Professor Mohammed Ismail, Professor Håkan Olsson, and Dr. Xiaopeng Li. It was a pleasant collaboration with them in the design work of a multi-standard sigma delta modulator chip. Also many thanks to Gang Xu in Lund University for the helpful discussions.

The author would like to thank Xing Liu and Roshan Weerasekera for their help in layout design of two chips.

Finally I would like to express sincere gratitude to my wife and my daughters. It is this warm family that supports me finishing my study during the years. I would also take the chance to thank my parents and my sister, for their love and support to me.

Bingxin Li
Stockholm, 2003

List of publication

Papers included in this thesis:

- (1) Bingxin Li and Hannu Tenhunen, "A second order multi-bit sigma delta modulator with single-bit feedback", *Journal of Analog Integrated Circuits and Signal Processing*, vol. 38, issue 1, pp. 63-72, January 2004.
- (2) Bingxin Li and Hannu Tenhunen, "Design of semi-uniform qauntizers and their application in sigma delta A/D converters", to appear in *Journal of Analog Integrated Circuits and Signal Processing*, 2004.
- (3) Bingxin Li and Hannu Tenhunen, "A structure of cascading multi-bit modulators without dynamic element matching or digital correction", in proc. of *2002 International Symposium on Circuits and Systems*, pp. III 711-714, Phoenix, May 2002.
- (4) Bingxin Li and Hannu Tenhunen, "Sigma delta modulators using semi-uniform quantizers", in proc. of *2001 International Symposium on Circuits and Systems*, pp. I 456-459, Sydney, May 2001.
- (5) Bingxin Li, Lirong Zheng, and Hannu Tenhunen, "An improved settling model of switched-capacitor integrator for high speed sigma-delta modulator simulation", in proc. of *2000 IEEEJ International Analog VLSI Workshop*, pp. 47-50, Stockholm, June 2000.
- (6) Bingxin Li, Lirong Zheng, and Hannu Tenhunen, "A design of operational amplifier for sigma delta modulators using 0.35um cmos process", in proc. *Tenth International Conference on Very Large Scale Integration*, pp. 23-34, Lisboa, December 1999.
- (7) Bingxin Li, Steffen Albrecht, Xiaopeng Li, Constantino Pala, Mohammed Ismail, and Hannu Tenhunen, A Front-End receiver sigma-delta modulator, 2001. *Granted swedish patent SE0002065*.
- (8) Bingxin Li, and Hannu Tenhunen, "A 2MS/s Second Order 5-bit Sigma Delta Modulator Using Single-bit DAC", submitted to *IEEE Transaction of Circuits and Systems II: Analog&Digital Signal Processing*, 2003.

Other publications

- (9) Bingxin Li and Hannu Tenhunen, "A second order sigma delta modulator using semi-uniform quantizer with 81db dynamic range at 32x OSR", in proc. of *2002 European Solide States Circuits Conference*, pp. 579-582, Florence, September 2002.
- (10) Bingxin Li and Hannu Tenhunen, "A second order multi-bit sigma delta modulator with single-bit feedback", in proc. of 20th Norchip Conference, pp. 241-246, Copenhagen, November 2002.
- (11) Bingxin Li and Hannu Tenhunen, "Signal scaling in multi-bit sigma delta modulators", in proc. of 19th Norchip Conference, pp. 204-209, Stockholm, November 2001.
- (12) Steffen Albrecht, Xiaopeng Li, Bingxin Li, Costantino Pala, Yonghong Gao, Mohammed Ismail, and Hannu Tenhunen, "A Dual-Standard GSM/DECT Baseband Sigma-Delta ADC", in proc. of 18th Norchip Conference, pp. 326-331, Turku, Finland, November 2000.
- (13) Sascha Thoss, Bingxin Li, and Hannu Tenhunen, "Loop coefficient optimization for cascaded sigma delta modulators - a case study", in proc. of 2000 IEEE International Analog VLSI Workshop, pp. 51-56, Stockholm, June 2000.
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List of Abbreviations

ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
CDMA	Code Division multiple Access
CMFB	Common-Mode FeedBack
CMFF	Common-Mode FeedForward
CMOS	Complementary-symmetry Metal-Oxide Semiconductor
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DECT	digital European cordless Telecommunications
DEM	Dynamic Element Matching
ENOB	Effective Number of Bit
FIR	Finite Impulse Response
FFT	Fast Fourier Transform
FOM	Figure of Merit
GSM	Global System for Mobile Communications
HDL	Hardware Description Language
IF	Intermediate Frequency
ITU	International Telecommunication Union
MASH	Multi-Stage Noise-Shaping
MSB	Most Significant Bit
NTF	Noise Transfer Function
Opamp	Operational Amplifier
OSR	Over Sampling Ratio
OTA	Operational Transconductance Amplifier
PSD	Power Spectral Density
RF	Radio Frequency
SI	Switched-Current

SC	Switched-Capacitor
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
STF	Signal Transfer Function
TDMA	Time Division Multiple Access
UMTS	Universal Mobile Telecommunications System

1 Introduction

1.1 Thesis background

1.1.1 Background

Though our world has an analog nature, nowadays information is very often stored, transferred, and processed digitally. The advantage is obvious: 1. digital signals are much more immune to noise than their analog counterparts. Noise and distortion will accumulate during the transfer or copy of an analog signal, while a digital signal can be losslessly copied or transferred as long as the noise and distortion are lower than the threshold which changes the digital value. 2. signal processing circuits can be implemented more easily, accurately and economically in digital domain thanks to the fast and continuous development of CMOS process. According to ITRS roadmap (International Technology Roadmap for Semiconductors), the mainstream CMOS process feature size will be scaled down to 32nm in the next 10 years, which is about one third of the current technology level (100nm, year 2003).

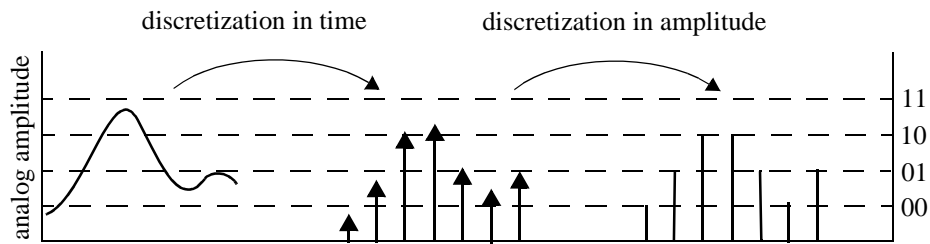


Fig 1.1 Sampling and quantization

As a result, analog to digital converters (ADC) and digital to analog converters (DAC) are needed to link the analog and digital domains. Information is first converted from analog to digital format, processed digitally, and then changed back to analog format again if required by the end user of the information. A digital signal is discrete in both amplitude and time, while an analog signal is continuous in both amplitude and time. Thus an A/D conversion includes two procedures as shown in Fig 1.1: *sampling*, which makes the signal discrete in time, and *quantization*, which makes the signal discrete in amplitude. Accordingly there are two important specifications for an ADC: speed and resolution. The speed represents how fast the discretization in time can be done. The resolution represents how accurate the discretization in amplitude can be done. ENOB (Effective Number of Bit) is often used to characterize the conversion

resolution.

According to Shannon's sampling theorem [Sha49], a band-limited analog signal must be sampled at least twice of its highest frequency component so that the signal can be reconstructed without loss. Many ADCs are designed to sample the signal just a little faster than the Nyquist frequency. These ADCs can be categorized as Nyquist-rate ADCs. They can operate at very high speed, resulting in a large bandwidth. Using a standard CMOS process, the conversion bandwidth is expanded to the range of Giga Hz [Pou02]. The main drawback of Nyquist-rate ADCs is their low resolution, which is limited by the matching of analog components. Practically 12~14 bit resolution can be economically (no calibration or trimming) achieved using Nyquist-rate ADCs [Pan00, Che01]. Another problem is the complex hardware structure. For a flash structure ADC, the hardware complexity (mainly contributed by the large number of comparators) exponentially increases with the resolution-in-bit. Using other structures like pipeline or folding can reduce the required number of comparators, which is however still large.

Developed in the 60's of last century [Ino62], Sigma Delta ADCs provide a robust and economical solution for high-resolution analog-to-digital conversion. Sigma Delta modulator is one kind of the so-called error feedback coder, meaning that the coarse quantization error is fed-back to the input. Many varieties of error feedback coders have been proposed in the last century. Although mathematically they all lead to a high-resolution, the practical implementation complexity is largely different. For example a Delta modulator [Jag52] realizes the same noise transfer function as a Sigma Delta modulator, but there the input signal is also filtered by the loop in the same way as the quantization error. In order to reconstruct the signal an extra inverse loop filter is needed. A Sigma Delta modulator arranges the loop filter in a way that the input signal and the quantization error see different transfer functions. The quantization error goes through a first order or higher order difference, yet the input signal is simply delayed. Theoretically the conversion resolution can be arbitrarily increased until the physical limitation of device thermal noise floor is reached. The high resolution is achieved through a feedback loop from the digitized output to the modulator input. Since there is a large gain in the forward path of the loop, the long-term average of the digitized output is forced to be very close to the modulator input. Furthermore, a Sigma Delta ADC does not require accurate analog component matching to achieve the superior resolution, which makes it suitable for standard CMOS processes. Sigma Delta ADCs have to operate at much higher frequency (oversampling) than the Nyquist frequency, therefore their main drawback is the narrow conversion bandwidth. Compared with the Giga Hz range of Nyquist-rate ADCs, Sigma Delta ADCs are currently capable of converting a signal within the range of Mega Hz [Kuo02], [Vel03].

With respect to circuit realization, Sigma Delta ADCs can be categorized into discrete-time structure and continuous-time structure. Using switched-capacitor (SC) circuits, discrete-time Sigma Delta ADCs can achieve very high resolution. But the circuit

speed is limited by the settling of switched-capacitor integrators. The future advanced CMOS process requires an ultra low supply voltage, which makes the realization of SC circuit more difficult. On the other hand continuous-time ADCs are more adaptive to low supply voltage. Input-signal sampling errors, like settling error and charge injection, and some other discrete-time problems do not exist in continuous-time circuits. The circuit can operate at a higher speed than its switched-capacitor counterpart. The drawback of continuous-time Sigma Delta ADCs is their sensitivity to clock jitter, which lowers the conversion resolution. But since the requirement on ADC resolution in wireless receivers is normally lower than applications like digital audio, this drawback does not prevent continuous-time Sigma Delta ADCs from being a good choice for receiver baseband conversion.

With respect to conversion signal-band, Sigma Delta ADCs can be categorized into low-pass ADCs and band-pass ADCs. Band-pass ADCs are especially suitable for converting a narrow-band signal which has a non-zero centre frequency. This character makes band-pass ADCs ideal for IF digitization in wireless communications. Recently many band-pass ADCs [Sal01], [Sch02] adopt the continuous-time structure to achieve a high centre frequency and large oversampling ratio, where the resolution requirement is moderate.

A complete Sigma Delta ADC includes a modulator (mostly analog) and a digital decimation filter. The modulator shapes the quantization error and the decimation filter reconstructs the signal in digital form. The focus of this thesis is on the modulator part.

1.1.2 Recent development

Fig 1.2 shows the performance increase of Sigma Delta ADCs in the past 16 years (1988-2003). Those chips that have the highest figure of merit (FOM) of the year are plotted. The FOM is calculated according to the formula:

$$FOM = \frac{2^{ENOB} \times (2 \times \text{signalband})}{\text{power}} \quad (1.1)$$

where ENOB is the effective number of bits, calculated according to the peak signal-to-noise-and-distortion-ratio (SNDR):

$$ENOB = (SNDR_{dB} - 1.76) / 6.02 \quad (1.2)$$

From Fig 1.2 it can be seen that in the past 16 years the FOM of Sigma Delta ADCs has increased by more than two order of magnitude. The performance is doubled roughly every two years. A detailed look shows that the achieved conversion resolution has not changed much. Already in the early 90's there was a 20-bit-resolution converter reported [Yam94]. It is the continuous increase of signal bandwidth and the

decrease of power consumption that boost the FOM. For example, compare the chip of 1988 and 2003, [Nor88] chip has a 13-bit resolution, while the [Vel03] chip only has 12-bit resolution. But the signal band of [Vel03] chip is 48 times as large as that of [Nor88] chip, and its power consumption is 1/16 of that of [Nor88] chip. The increase of conversion bandwidth and the decrease of power are two contradictory design targets. The simultaneous fulfillment of these two targets is a result of advance in process technology and new circuit topology. The [Nor88] chip is designed using 1.75 μm CMOS process, and the [Vel03] chip is in 0.18 μm CMOS process, which is 10 times smaller. When the process feature size is scaled down, the gate oxide thickness is also scaled down, leading to a larger gate capacitance C_{ox} . According to the equation (NMOS in saturation mode)

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (1.3)$$

With a fixed biasing current, using a smaller feature size process can provide a larger g_m , and in turn a higher speed. However not everything associated with the technology scale-down is favorable to analog circuits: 1. the thinner gate oxide layer requires a lower supply voltage to keep the electrical field strength constant. Many conventional circuit topologies are not suitable to work under such a low supply voltage. The circuit performance is often sacrificed. 2. the influence of short channel effect is more critical, and 3. the CMOS process parameters are often optimized to meet the requirement of digital circuits.

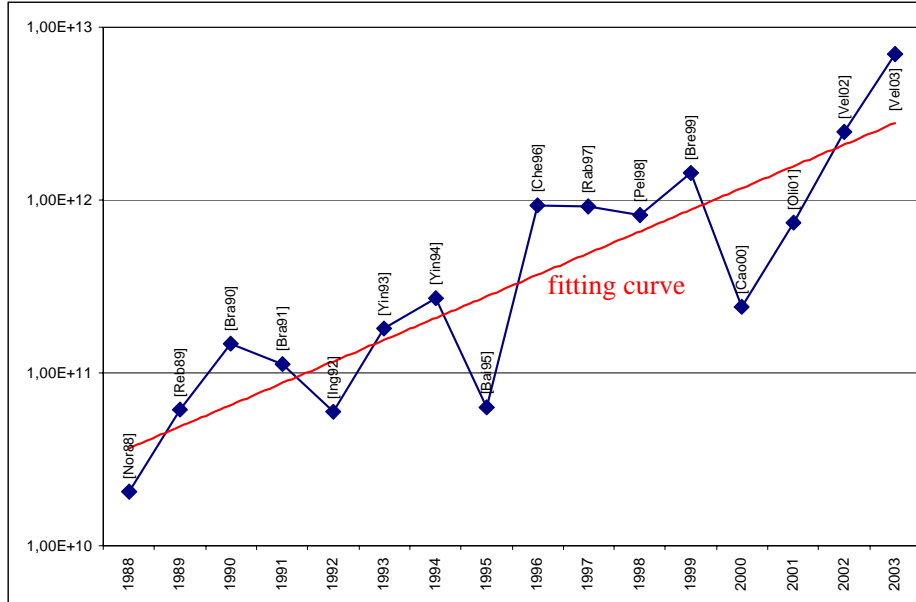


Fig 1.2 Sigma Delta ADC FOM

1.2 Motivation

1.2.1 Problem statement

Sigma Delta ADCs are inherently suitable for high-resolution narrow-band A/D conversions. Therefore Sigma Delta ADCs find their best application in the areas like digital audios [Bra91, Rit94, Fuj97] or instrument measurements [Yam94]. In modern wireless communication standards, the channel bandwidth is often in the order of hundreds of KHz (e.g. GSM, DECT), or even MHz (e.g. UMTS). Furthermore, it is often preferred in modern receivers to directly digitize the IF signal [Sen98], [Sal01] which ranges from tens of MHz to hundreds of MHz. Working at such a high frequency and achieving a high resolution and a low power is a critical challenge for even experienced designers.

1.2.2 Solutions

In order to achieve both a large bandwidth and a high resolution, one should increase the sampling frequency, the noise-shaping order, and the quantizer resolution separately or combined. This can be illustrated in the following equations.

With an ideal noise transfer function $(1-z^{-1})^n$, the maximum achievable SNR is:

$$SNR = \frac{3(2^m - 1)^2}{2\pi^{2k}}(2k + 1)OSR^{2k+1} \quad (1.4)$$

where m is quantizer resolution in bit, k is noise shaping order, and OSR is oversampling ratio. Replacing OSR by $f_s/2f_b$, where f_s is sampling frequency and f_b is signal bandwidth, we get:

$$SNR \cdot f_b^{2k+1} = \frac{3(2^m - 1)^2}{2\pi^{2k}}(2k + 1)\left(\frac{f_s}{2}\right)^{2k+1} = \text{const}(m, k, f_s) \quad (1.5)$$

The product of SNR and f_b^{2k+1} is a constant defined by m , k , and f_s . That means with a fixed noise-shaping order, quantizer resolution, and sampling frequency, there is always a trade-off between the achievable resolution SNR and signal bandwidth f_b . In order to increase both the SNR and f_b simultaneously, a larger m , k , and f_s have to be used separately or combined. These three methods are briefly discussed below.

1.2.3 Increase of sampling frequency

In a switched-capacitor realization of Sigma Delta ADCs, the sampling frequency is

mainly limited by the settling procedure of the integrator. Although theoretically it takes infinite time to perform a complete settling, in practice as long as the settling error is controlled to be small enough it will not significantly degrade the conversion resolution. When the settling error is not negligible but the settling is linear, it causes a gain error, which changes the noise transfer function and increases the in-band noise. If the settling error is so large that the settling becomes non-linear, the converter output will contain harmonic distortions [Reb90]. In a continuous-time Sigma Delta ADC there is no such switched-capacitor integrator settling procedure. The integrator output is continuously changing in a way much more slowly than in a switched-capacitor integrator. As a result, a continuous-time Sigma Delta ADC can sample the input at a higher frequency.

In both switched-capacitor and continuous-time Sigma Delta ADCs, the bottleneck of speed increase is the Opamp. Commonly used Opamp structures are two-stage OTAs and single-stage folded-cascode OTAs. A folded-cascode OTA has a simple structure because it skips the inter-stage compensation capacitors as well as the common-mode-feedback circuit for the outer stage. It provides a high unit-gain-frequency and high slew-rate, yet the output swing is lower than that of the two-stage OTA due to the use of cascaded current mirrors. Until now folded-cascode OTAs remain the most popular choice in Sigma Delta ADC designs. In future deep-submicron processes where the supply voltage is below 1V, it is difficult for folded-cascode OTAs to provide a reasonably large output swing. Two-stage OTAs distribute the gain requirement into two stages, therefore each stage only needs to provide a moderate gain. But the existence of inter-stage compensation capacitor and two common-mode-feedback circuits complicate the design. Both folded-cascode and two-stage OTAs have their dominant pole located at g_m/C_c , where g_m is the OTA input transistor's transconductance, and C_c is the compensation capacitor (for folded-cascode OTA C_c is the load capacitance). As mentioned in equation 1.3 the process advance brings a thinner gate oxide and therefore a larger g_m . As a result, the sampling speed f_s of a Sigma Delta ADC is continuously increasing. In early 90's of last century the typical sampling frequency is tens of Mega-hertz [Bra90], [Bra91a]. Nowadays above hundred-Mega-hertz switched-capacitor Sigma Delta ADCs are implemented [Vel03].

1.2.4 Increase of noise-shaping order

The noise-shaping order k is defined by the number of integration stages. Ideally the noise-shaping order can always be increased so that the target resolution is achieved even with a low oversampling ratio. But in practice the noise-shaping order of a low-pass single-stage Sigma Delta modulator is seldom higher than 4 or 5. The main concern is the stability problem. In a high order Sigma Delta modulator the signal goes through a long path and experiences a long delay before it is quantized, so the quantized signal does not accurately predict the current input. When the quantized signal is fed-back and compared with the current input, the error is large. This phenomenon is

similar to a low-phase-margin in a general negative-feedback system. Since the comparison error is accumulated by the following integrators, the larger the error, the higher the possibility for the integrators to reach a state of saturation. If the integrators saturate for a long time the whole modulator will oscillate and become unstable. Even if the integrators saturate for only a short time, the signal information is partly lost and distortions will appear at the output.

Even though high order single-stage Sigma Delta ADCs have been successfully designed, their stability condition is still poorly understood. Currently the stability is analyzed using the linear model of the modulator. Due to the highly non-linear character of the quantizer, the linear model of a Sigma Delta modulator is only a coarse approximation. Furthermore, even using a linear model it is currently impossible to predict the stability for modulators with orders higher than 2 [Wan92]. Numerical simulations are widely used to evaluate the modulator stability, but since it is impossible to simulate all the input combinations, the evaluation is not comprehensive.

One solution to build high order Sigma Delta modulator is to adopt the cascaded structure, where a single-stage high-order integrator chain is broken into several low-order stages. As long as each low-order stage is stable, the whole modulator is stable. In such a cascaded structure the overall resolution is often limited by the mismatch error between the analog filter and the digital filter, which can be larger than the quantization error or thermal noise.

1.2.5 Thesis focus - increase of quantizer resolution

The resolution m of the internal quantizer and DAC in a Sigma Delta ADC is often only 1-bit, taking the advantage that a 1-bit DAC is inherently linear since it has only two output levels. The other benefits are the simple circuit structure and low power consumption. A high-bit quantizer may contain tens of comparators and is often the largest contributor to the total chip area and power of an ADC. In the case where the resolution can no longer be further (economically) improved by increasing sampling frequency or noise-shaping order, a multi-bit quantizer finds its position. Using an N -bit quantizer instead of 1-bit quantizer can reduce the quantization error by a factor of 2^N , thus increase the resolution by $6.02N$ dB. Note that this resolution increase is not related to the modulator order or oversampling ratio. This character is especially helpful under a low oversampling ratio, where the increase of noise-shaping order is less effective. Other advantages include the increased stability and the relaxed requirement on integrators. Since the multi-bit quantizer gives a more accurate prediction of the current input than a 1-bit quantizer does, the input to the integrators are smaller. As a result the integrator has lower possibility to saturate and the stability is improved. Also because the integrator input is smaller, the integrator output swing is reduced, therefore the requirement on Opamp slew rate is relaxed.

For a multi-bit Sigma Delta modulator the biggest problem to solve is the multi-bit

DAC non-linearity, which is not noise-shaped. To handle the DAC non-linearity problem, earlier multi-bit sigma Delta ADCs adopt the cascaded structure [Bra91b], where the last stage uses a multi-bit quantizer and the previous stages use single-bit quantizers. The DAC non-linearity error is noise-shaped by the previous stages and becomes negligible.

To solve the non-linearity problem of a single-stage multi-bit modulator, one method is to use digital corrections [Sar93], [Sil02]. The DAC output is calibrated and the error value is stored in a RAM. The main drawback is the extra calibration procedure and the need of memory. Another method is to use Dynamic Element Matching (DEM) circuits [Mil03], [Uen02], [Kuo02]. A DEM circuit can randomize or noise-shape the DAC non-linearity. This method does not need calibration, but the DEM circuit still increases the circuit complexity. A third method is to use a multi-bit quantizer combined with a single-bit DAC [Les90]. A multi-bit quantizer reduces the quantization error, and a single-bit DAC eliminates the non-linearity error. Compared with other methods, it has the lowest circuit complexity. Its drawback is that in practical implementations, the achievable resolution is reduced by signal scaling [Li02a]. However this method still provides a competitive solution compared with same-hardware-complexity modulators using digital correction or DEM circuits. Since the proposal of this structure in 1990 there has been no reported design adopting this structure, until the recently measured chips [Li04a], [Li03a] verified the feasibility and advantage of it. It is shown that an optimal signal scaling balances the modulator stability and conversion resolution. A second order N -bit modulator using a 1-bit DAC achieves a resolution $(N-2)*6$ dB higher than a conventional 1-bit modulator.

Most multi-bit modulators use a uniform quantizer, whose quantization levels have equal distance (quantization step) between each other. A non-uniform quantizer has small quantization steps for small inputs and large quantization steps for large inputs [Zha91]. In this thesis a new type of non-uniform quantizer, semi-uniform quantizer, is introduced and analyzed [Li01a], [Li02b]. Based on the fact that the quantizer input distribution follows a Normal Distribution in most cases, a semi-uniform quantizer provides a higher dynamic range compared with a uniform quantizer. The circuit structure and hardware complexity are similar to those of a conventional uniform quantizer. Measurement results [Li02b] confirm its feasibility and performance. A Sigma Delta modulator using N -bit semi-uniform quantizer achieves the same dynamic range as a modulator using a $(N+1)$ -bit uniform quantizer.

1.3 Thesis outline

The thesis is organized as follows. Chapter 2 illustrates the principle of Sigma Delta ADCs and the fundamentals of quantizer characters. Chapter 3 provides an overview of wireless communication history and wireless transceiver structures, as well as the applications of Sigma Delta ADCs in wireless communications. The focus is on the design topics of multi-bit modulators in such applications, such as combining a multi-bit quantizer with a single-bit DAC, and semi-uniform quantization. Chapter 4 discusses some design challenges that we will face in the near future. Chapter 5 concludes the thesis.

2 Sigma Delta ADC Overview

2.1 Sigma Delta ADC principle

2.1.1 Methods to reduce in-band quantization error power

The principle and advantage of a Sigma Delta ADC can be illustrated with an example. Assume that a N -bit ADC samples at a frequency of $f_s = 2f_b$, where f_b is the signal bandwidth. A pure sine wave with a frequency f_i is sent to this ADC as an input. In frequency domain this input signal is shown in Fig 2.1 as a single tone located at f_i .



Fig 2.1 Spectrum of input signal

After the A/D conversion, the digital signal contains both the input signal and the quantization error. Assume that the quantizer output range is normalized as $-1 \sim +1$, the quantization step Δ of a N -bit quantizer is $1/2^{(N-1)}$. Assume that the quantization error is a white noise, the power of the N -bit quantization error is:

$$P_e = \int_{-\Delta/2}^{\Delta/2} \frac{1}{\Delta} e^2 de = \frac{\Delta^2}{12} \quad (2.1)$$

and the quantization noise floor is determined by its spectrum density:

$$\rho(f) = \frac{\sqrt{P_e}}{\sqrt{f_s/2}} = \frac{\Delta}{\sqrt{12f_b}} = \frac{1}{2^{N-1} \sqrt{12f_b}} \quad (2.2)$$

In the spectrum of the digital signal, the input signal tone is still at its original position, but the noise floor is increased by the quantization error, as shown in Fig 2.2.

Fig 2.2 Spectrum of N -bit quantized signal

One way to reduce the noise power is to use a higher resolution converter. Using a M -bit ($M > N$) converter will reduce the quantization step and in turn lower the noise floor as shown in Fig 2.3.

Fig 2.3 Spectrum of M -bit ($M > N$) quantized signal

Another way is to use oversampling to reduce the in-band noise, without the need of a higher resolution quantizer. In Fig 2.4 the sampling frequency is increased by OSR times: $f_s = 2f_b \cdot OSR$, corresponding to a oversampling ratio of OSR . Since the total quantization error power is now distributed in an OSR times wider frequency range, the noise floor is lowered.

$$\rho(f) = \sqrt{\frac{P_e}{f_s/2}} = \frac{\Delta}{\sqrt{12f_b \cdot OSR}} = \frac{1}{2^{N-1} \sqrt{12f_b \cdot OSR}} \quad (2.3)$$

As a result the in-band noise power is reduced by a factor of OSR

$$P_{inband} = \int_0^{f_b} \rho^2(f) df = \frac{\Delta^2}{12f_b \cdot OSR} = \frac{\Delta^2}{12 \cdot OSR} = \frac{P_e}{OSR} \quad (2.4)$$

When the resolution is not limited by distortion, every doubling of sampling frequency would reduce the in-band noise power by half, or in other words, increase the resolu-

tion by about 3dB. Obviously this is not an efficient method to achieve a high resolution.

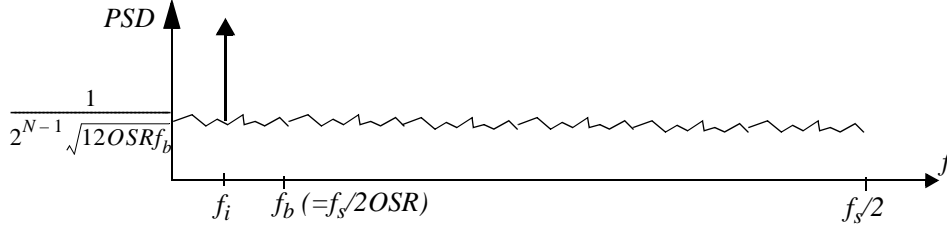


Fig 2.4 Spectrum of oversampled and quantized signal

Although oversampling is very seldom used alone, it is the pre-condition to use the noise shaping technique. Fig 2.5 shows the spectrum of a noise-shaping modulator output. The noise floor follows a sine shape. In the low frequency range this shaped noise floor is much lower than the pure oversampled noise floor. In the high frequency range the shaped noise floor becomes higher, but the noise power in that range will be digitally filtered out. The remaining in-band noise power depends on the oversampling ratio and noise-shaping order.

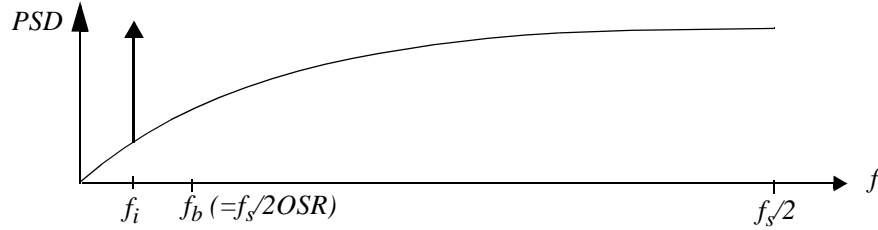


Fig 2.5 Noise shaped quantizer output

2.1.2 Noise shaping

In a Sigma Delta A/D converter the quantization error is fed-back to the input of the converter, thus the quantization error is shaped by the noise transfer function (NTF). The basic form of a NTF is:

$$NTF(z) = (1 - z^{-1})^k \quad (2.5)$$

Here k is the modulation order. Note that $k=0$ is the special case in which no noise-shaping is performed. The frequency response of such a NTF is

$$NTF(f) = \left[2 \sin\left(\pi \frac{f}{f_s}\right) \right]^k \quad (2.6)$$

Fig 2.6 plots the frequency response of NTF with different order k .

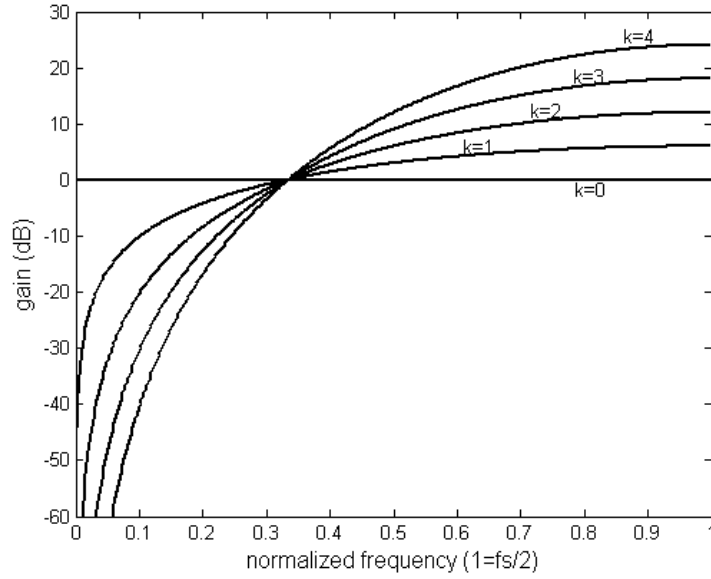


Fig 2.6 Noise transfer function

The in-band noise power is

$$P_{inband} = \int_0^{f_b} \rho^2(f) NTF^2(f) df = \int_0^{f_b} \frac{\Delta^2}{6f_s} \left[2 \sin\left(\pi \frac{f}{f_s}\right) \right]^{2k} df$$

$$\text{when } f_s \gg f_b \quad \text{we have} \quad \sin\left(\pi \frac{f}{f_s}\right) \approx \pi \frac{f}{f_s}$$

So,

$$P_{inband} \approx \frac{\Delta^2}{12} \frac{\pi^{2k}}{(2k+1)} \left(\frac{2f_b}{f_s}\right)^{2k+1} = P_e \frac{\pi^{2k}}{2k+1} \frac{1}{OSR^{2k+1}} \quad (2.7)$$

Compared with Equation 2.4, where the input signal is only oversampled without noise shaping, the in-band quantization error power is much smaller. From this equation we can also see that oversampling is the essential condition for a noise shaping

modulator, because if $OSR=1$ (means no oversampling) then P_{inband} becomes

$$P_{inband} = P_e \frac{\pi^{2k}}{2^{k+1}} > P_e \quad (2.8)$$

It is now possible to derive the maximum achievable SNR for an ideal Sigma Delta modulator, which is used in Equation 1.4. For a normalized full-scale range of -1~+1 input sinusoidal signal, the maximum signal power is

$$P_s = \left(\frac{\sqrt{2}}{2} \cdot 1 \right)^2 = \frac{1}{2}$$

For a m -bit quantizer, the quantization step is

$$\Delta = \frac{2}{(2^m - 1)}$$

Therefore

$$SNR = \frac{P_s}{P_{inband}} = \frac{1/2}{\frac{4}{(2^m - 1)^2} \frac{\pi^{2k}}{12(2k+1)} \frac{1}{OSR^{2k+1}}} = \frac{3(2^m - 1)^2}{2\pi^{2k}} (2k+1) OSR^{2k+1} \quad (2.9)$$

Equation 2.9 shows that even with a coarse 1-bit quantizer, superior SNR can be achieved by combining a large oversampling ratio with a high noise shaping order. However, the real performance can be significantly lower than the equation prediction due to three main reasons: 1. circuit non-idealities make the noise transfer function deviate from its ideal form. 2. with stability considerations high order modulators are often designed to have extra poles in their noise transfer functions, which increases the in-band noise power [Rit90]. For MASH structure modulators, the inter-stage signal scaling has the same effect of increasing in-band noise power. 3. circuit thermal noise and flicker noise put a fundamental limit on the highest SNR that can be achieved, no matter what the oversampling ratio or noise shaping order is.

2.1.3 Modulator topology

An integrator is a basic building block to construct a Sigma Delta modulator. Fig 2.7 shows a first order Sigma Delta modulator.

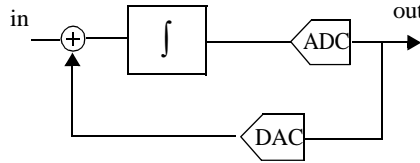


Fig 2.7 First order modulator

Higher order modulators can be constructed in two ways. The first is to place integrators in a single loop, one following another. Feed-forward path can be added from signal input to each integrator, and feed-back path can be added from DAC output to each integrator, as shown in Fig 2.8. Please note that each feed-forward or feed-back path has a coefficient associated with it, which is not shown in the figure for simplicity.

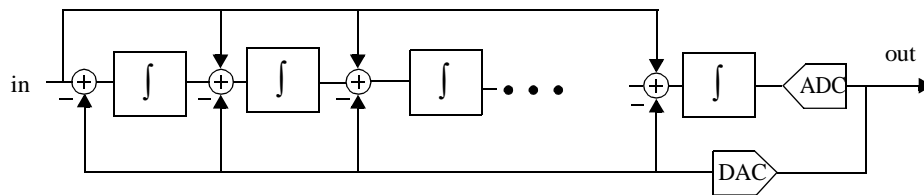


Fig 2.8 Single-loop modulator

The modulator in Fig 2.8 forms a noise transfer function NTF with all its zeros located at dc ($z=1$). It is possible to add some local resonator feedbacks as shown in Fig 2.9 to move some of the NTF zeros away from dc, and as a result the in-band noise power can be reduced.

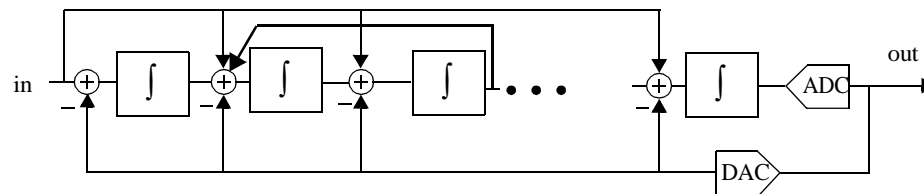


Fig 2.9 Modulator with local feedback

The other way to construct a higher order modulator is to place the integrators in several loops [Hay86] as shown in Fig 2.10. This is the so-called MASH (multi-stage noise-shaping) structure, or cascaded structure.

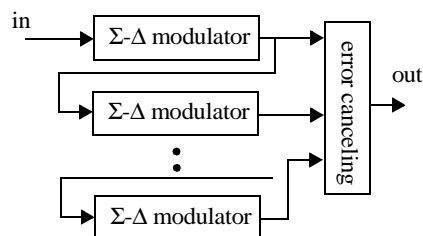


Fig 2.10 MASH structure modulator

Each loop in Fig 2.10 forms an independent Sigma Delta modulator. The output of each modulator is sent to the error cancelling circuit. The overall noise-shaping order is the sum of the noise-shaping orders of all stages.

2.1.4 Decimation filter

Decimation is a step to recover the narrow band signal from a high frequency data stream (very often a bit stream) generated by a Sigma Delta modulator [Sar88], [Sar90], [Kar92]. The decimation filter should provide enough attenuation to out-of-band noise, meaning that the design task of the low-pass filter is shifted from analog domain to digital domain. However in digital domain designing such a filter is much easier. The character of the filter depends solely on the digital coefficients rather than on the analog component matching. A widely used design method for Sigma Delta modulator decimation filter is to combine a comb filter with a FIR filter [Cro81]. This method achieves both circuit simplicity and linear phase response.

A comb filter reduces the digital data rate from $OSR \cdot f_N$ down to about 2~8 times of f_N , where f_N is the Nyquist frequency. The word length is increased accordingly. The successive FIR filter further reduces the sampling frequency to f_N . The reason why a comb filter is especially effective for Sigma Delta modulator is illustrated in Fig 2.11.

In Fig 2.11a the general specification of a decimation filter is shown. The sampling frequency should be reduced from f_s to an intermediate frequency f_D . To avoid aliasing, large attenuation is required outside the band $0 \sim f_D/2$. The transition band ($f_b \sim f_D/2$) is very narrow compared to the sampling frequency f_s . A large number of taps is needed if a FIR filter is used instead. However, the signal band between f_b and $f_D/2$ will be filtered-out by the successive FIR filter. This means the noise aliased into this range will not increase the final in-band noise power, as long as the successive FIR filter provides enough stop band attenuation. As shown in Fig 2.11b the band $if_D \cdot f_b \sim if_D + f_b$ ($i=1,2,\dots$) should have enough attenuation because they will alias back to the signal band, while the other bands become "don't care" region. This leads to the use of a comb filter which has a frequency response as shown in Fig 2.11c.

The comb filter has a z-domain transfer function of:

$$H(z) = \frac{1}{d^F} \left(\frac{1-z^{-d}}{1-z^{-1}} \right)^F \quad (2.10)$$

where d is the decimation factor and F is the filter order. The frequency response of a comb filter with order 1~3 is plotted in Fig 2.12.

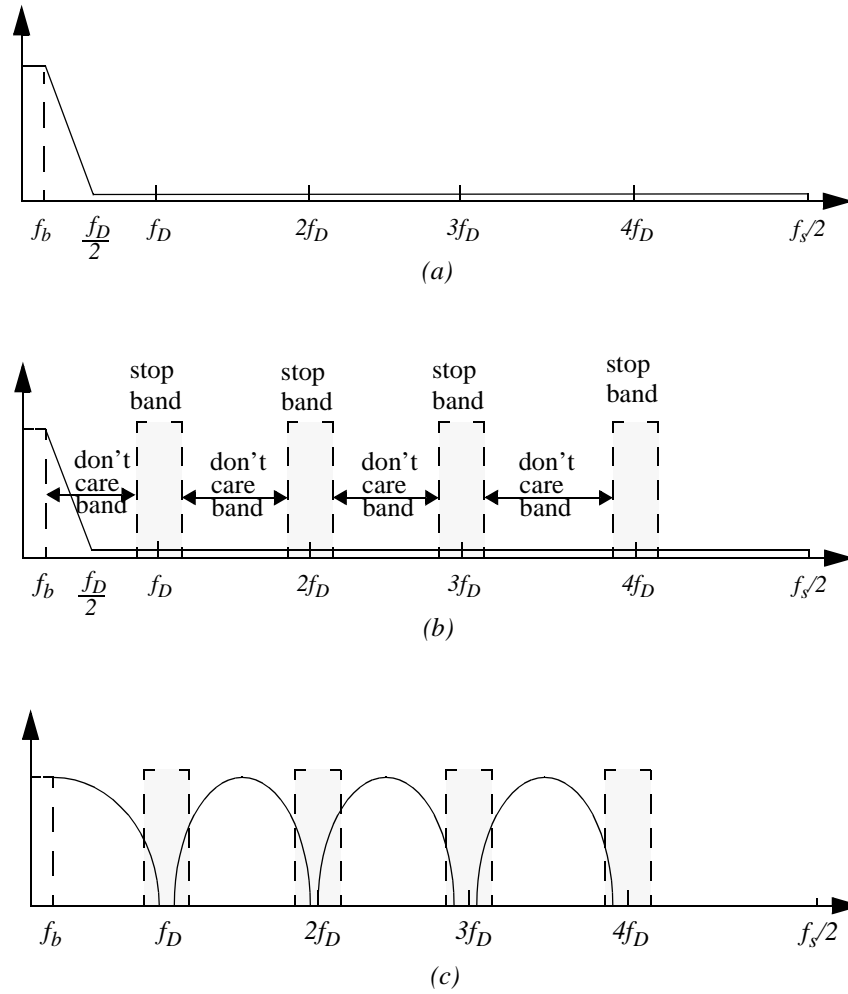


Fig 2.11 Anti-aliasing in comb filter

(a) filter specification

(b) don't-care band

(c) comb filter frequency response

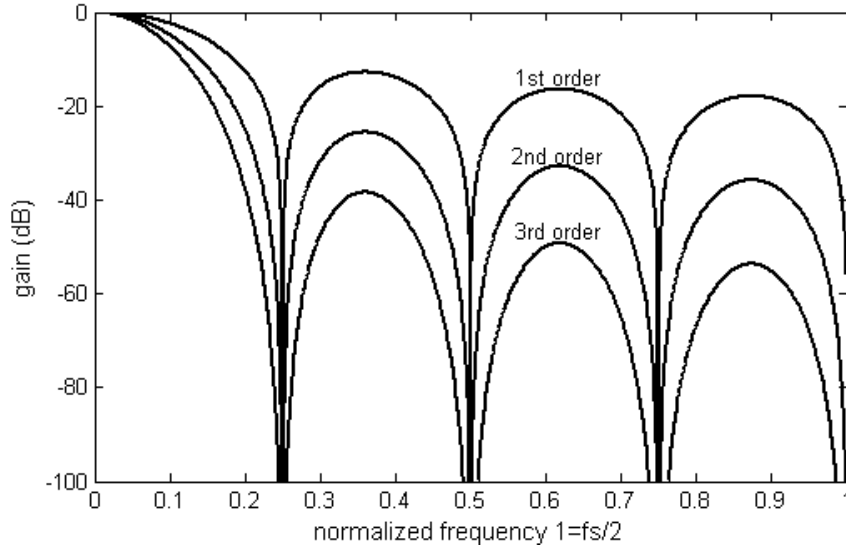


Fig 2.12 Comb filter response

It is proved [Can86] that for a modulator with an order k , a comb filter needs an order at least $k+1$ to achieve enough stop band attenuation. The transfer function of quantization error for combined Sigma Delta modulator and comb filter is thus

$$H(z) = \frac{1}{d^{k+1}} \frac{(1-z^{-d})^{k+1}}{(1-z^{-1})}$$

and this will increase the equivalent in-band noise to

$$\rho'(f) = \rho(f) \left[\frac{\text{sinc}(f/f_s)}{\text{sinc}((df)/f_s)} \right]$$

In an oversampling Sigma Delta converter normally $df/f_s \leq 1/4$, so the factor $\frac{\text{sinc}(f/f_s)}{\text{sinc}((df)/f_s)}$ is very close to 1 and the in-band noise increase is negligible.

Following the comb filter one (or several) FIR filter is normally used. This FIR filter further reduces the sampling frequency to Nyquist frequency and truncates the output word length to the specified value.

2.2 Quantizer characters

2.2.1 Quantizer transfer curve

A N -bit quantizer maps its input analog level to one of 2^N digital codes. In the special case of 1-bit quantizer, there are only two output codes. The transfer curve represents how the quantizer maps the input level to a specific output code. Fig 2.13 shows a typical example of a 3-bit quantizer transfer curve. The input values where the output code has a transition are thresholds of the quantizer. The output is digital levels, but it has its analog equivalent. The analog equivalent of the distance between adjacent digital codes is called quantization step Δ . The curve that crosses the midpoints of the quantization levels defines the gain of the quantizer. Most multi-bit quantizers have a gain of unit. For a single-bit quantizer, since there are only two output levels, the gain can be arbitrary value.

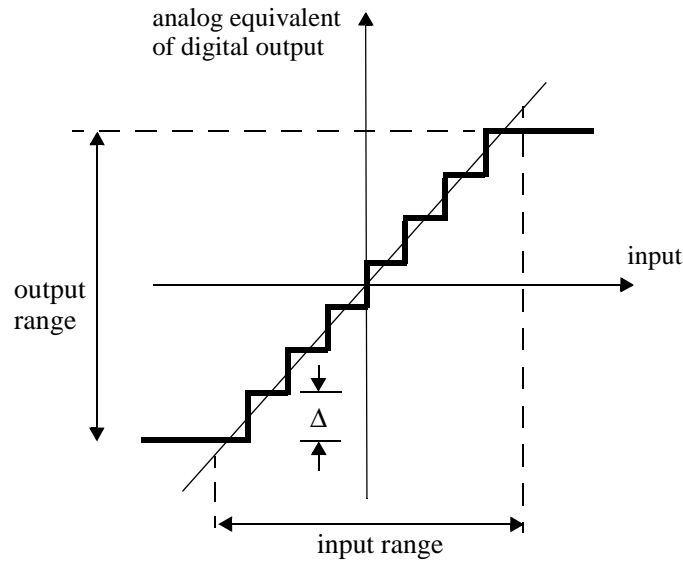


Fig 2.13 Quantizer transfer curve

The quantization error is defined as the difference between the quantizer input and the analog equivalent of the quantizer output. Fig 2.14 shows the quantization error corresponding to the transfer curve shown in Fig 2.13. When the quantizer is not overloaded the quantization error is bounded within the range $-\Delta/2 \sim +\Delta/2$. The quantizer's input range is defined as the range where the quantizer is not overloaded, that is $-1-\Delta/2 \sim 1+\Delta/2$ (normalized).

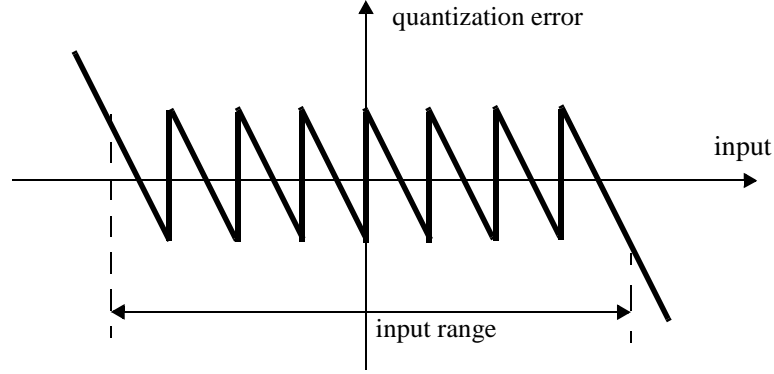


Fig 2.14 Quantization error

Under certain conditions [Wid56],[Sri77] the quantization error can be approximated as a white noise. Although in practice these conditions are never fully met, the white noise model is still very useful and often gives reasonably accurate prediction of the performance. In this white noise model, the quantization error has two characteristics:

- The amplitude of the quantization error is evenly distributed over the range of $-\Delta/2 \sim +\Delta/2$.
- The spectrum of the quantization error is evenly distributed over the range of $0 \sim f_s/2$, where f_s is the sampling frequency.

2.2.2 Quantization error power

Within the non-overload range, the quantization error $\epsilon(x)$ is a periodic function of the quantizer input x , and its value is bounded between $-\Delta/2$ and $\Delta/2$. The power of the quantization error is defined as:

$$P_\epsilon = \int_{-\infty}^{\infty} \rho(x) \epsilon^2(x) dx \quad (2.11)$$

where $\rho(x)$ is quantizer input distribution. Obviously, P_ϵ is related to both $\rho(x)$ and $\epsilon(x)$. But since $\epsilon(x)$ is a periodic function of x when the quantizer is not overloaded, we can prove that the quantization error power is not related to its distribution, provided that the number of quantization levels (for a k -bit quantizer it is 2^k) is large enough, and the quantization step Δ is small enough. In the narrow range $x \in i\Delta \sim (i+1)\Delta$ the

probability density $\rho(x)$ can be approximated as a constant ρ_i , where $i \in [-2^{k-1}, 2^{k-1} - 1]$. This is shown in Fig 2.15.

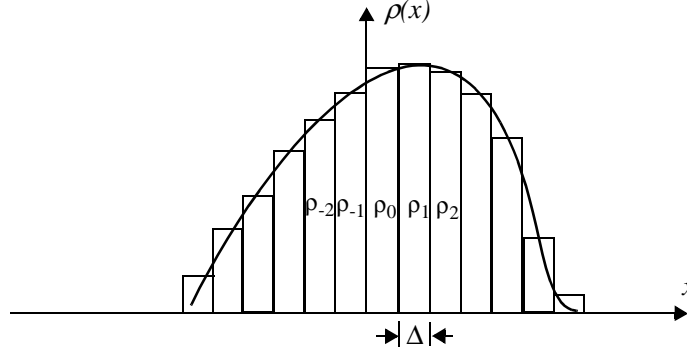


Fig 2.15 Approximation of quantizer input distribution

Therefore we have:

$$\begin{aligned}
 P_\epsilon &= \int_{-\infty}^{\infty} \rho(x) \epsilon^2(x) dx = \sum_{i=-2^{k-1}}^{2^{k-1}-1} \int_0^\Delta \rho(x+i\Delta) \epsilon^2(x+i\Delta) dx = \sum_{i=-2^{k-1}}^{2^{k-1}-1} \int_0^\Delta \rho(x+i\Delta) \epsilon^2(x) dx \\
 &= \left(\sum_{i=-2^{k-1}}^{2^{k-1}-1} \rho_i \right) \cdot \int_0^\Delta \left(\frac{\Delta}{2} - x \right)^2 dx = \frac{1}{\Delta} \int_0^\Delta \left(\frac{\Delta}{2} - x \right)^2 dx = \frac{1}{\Delta} \left[\frac{\Delta^3}{4} - \frac{\Delta^3}{2} + \frac{\Delta^3}{3} \right] = \frac{\Delta^2}{12} \quad (2.12)
 \end{aligned}$$

This result concludes that the total quantization error power is only related to the value of the quantization step Δ , and it is not signal dependent.

2.2.3 Quantizer gain

As mentioned in 2.2.1, a single-bit quantizer does not have a fixed gain. In its linear model the quantizer gain is determined by the loop coefficients based on the unit-loop-gain assumption. Fig 2.16 is an example of the linear model of a second order single-bit modulator. In the linear model, the 1-bit quantizer is modelled as a gain block α plus a white noise source e . Since the two-level quantizer can not define a fixed gain, α can take arbitrary value. But in practice, one often uses unit-loop-gain assumption to assign a virtual linear gain to α . The unit-loop-gain assumption assumes that the product of integrator gain and the quantizer gain along the outer feedback loop is unit, or in Fig 2.16, $b_1 a_2 \alpha = 1$. This leads to $\alpha = 1/b_1 a_2$. So the 1-bit quantizer linear gain is defined by the modulator loop coefficients. This brings freedom to signal scaling procedure, where the loop coefficients are adjusted to change the internal signal swing while the specified noise transfer function is kept constant. Since α can be set to any

value, the product b_1a_2 can be adjusted to scale the internal signal swing.

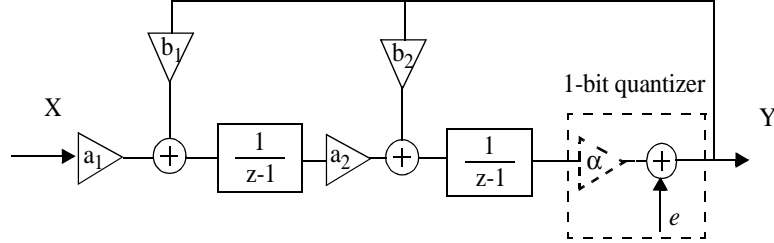


Fig 2.16 Linear model of 1-bit modulator

In a multi-bit modulator, the quantizer gain is fixed, and in most cases it is unit. Therefore the value of α is 1. As a result, in signal scaling the product b_1a_2 is fixed to achieve the required noise transfer function. Accordingly, the linear model is much more accurate with a multi-bit quantizer. In general, the higher the quantizer bit-number, the more accurate the linear model. In the extreme case where the quantizer has infinite number of bit, the model becomes perfectly linear.

2.2.4 Quantizer input distribution

For a Sigma Delta modulator, its input signal is unknown. Therefore the input distribution is also unknown. However the quantizer's input distribution does have certain common characters, no matter what the modulator input is. Fig 2.17 shows the simulated quantizer input distribution of a second order modulator, with input signal set to sinusoidal, random, and *dc* respectively.

It is clear that all the distributions have a similar shape -- a Normal Distribution. The following analysis proves that when the modulator input signal amplitude is less than half of quantizer LSB (Least Significant Bit) Δ , then its distribution does not significantly influence the distribution of the quantizer input, which is similar to a Normal Distribution.

In a Sigma Delta A/D converter the quantizer input is determined by both the input signal and the quantization error, due to the existence of the feedback loop. Generally for a k th order Sigma Delta modulator whose output in z -domain is

$$Y(z) = X(z)z^{-k} + \epsilon(z)(1 - z^{-1})^k$$

the quantizer input Q can be expressed as

$$Q(z) = X(z)z^{-k} + \epsilon(z)[(1 - z^{-1})^k - 1]$$

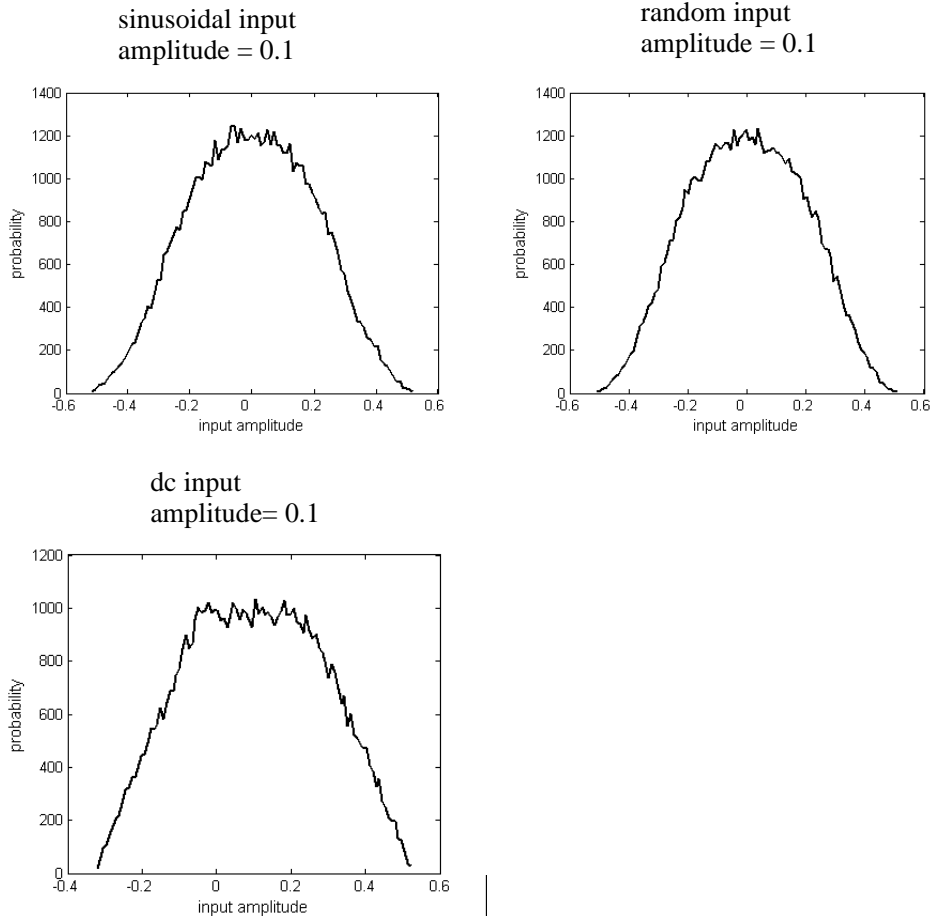


Fig 2.17 Quantizer input histogram

With a specific example of a 2nd order modulator,

$$Q(z) = X(z)z^{-2} + \varepsilon(z)(-2z^{-1} + z^{-2})$$

Rewrite this equation in time domain,

$$Q_n = X_{n-2} + (-2\varepsilon_{n-1} + \varepsilon_{n-2}) \quad (2.13)$$

Under the white noise assumption, the quantization error ε_{n-1} and ε_{n-2} are not correlated to input signal x_{n-2} . Note that ε_{n-1} and ε_{n-2} are related to each other since $\varepsilon(z)z^{-2}$ is

simply the one-sample-delayed version of $\mathcal{E}(z)z^{-1}$. However at each specific sample time the values of ε_{n-1} and ε_{n-2} are not correlated provided that the white noise model holds. Therefore when we discuss the power and distribution of the quantizer input Q_n , the variables x_{n-2} , ε_{n-1} and ε_{n-2} can be treated as three independent variables.

Based on Equation 2.13, we have for uniform quantizer:

$$\sigma_q^2 = \sigma_x^2 + (2^2 + 1^2)\sigma_\varepsilon^2 = \sigma_x^2 + 5\sigma_\varepsilon^2 = \sigma_x^2 + \frac{5}{12}\Delta^2 \quad (2.14)$$

The power of quantizer input σ_q^2 is the sum of input power σ_x^2 and five times of quantization error power σ_ε^2 . When σ_x is less than $\Delta/2$, σ_q is mainly determined by quantization error power. Fig 2.18 shows the simulated quantizer input power of a 2nd order 3-bit Sigma Delta modulator, compared with the calculated value using Equation 3.4. When the signal amplitude is less than $\Delta/2$ the quantizer input power curve is almost flat, which means the quantizer input power is dominated by the quantization error power. When the signal amplitude exceeds $\Delta/2$ the quantizer input power increases rapidly and is dominated by the signal power.

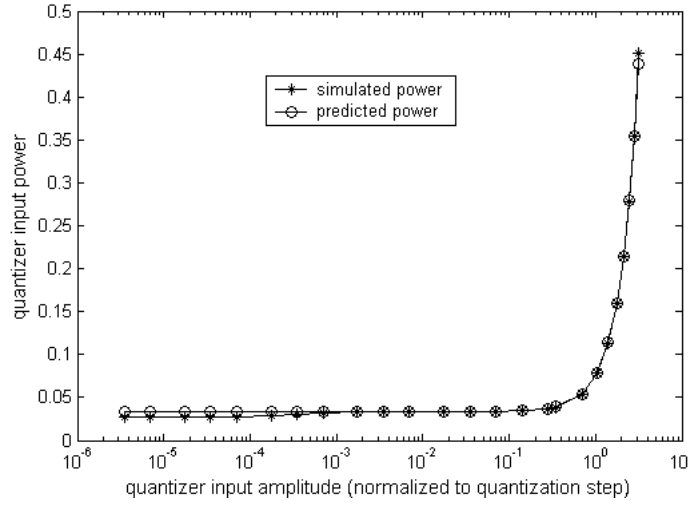


Fig 2.18 Quantization error power

Not only the power but also the distribution of quantizer input Q is determined by both the input signal and the quantization error. We will first focus on the quantization error part in equation 3.3. Since $-2\varepsilon_{n-1}$ (denoted as e_1 later) and ε_{n-2} (denoted as e_2 later) are treated as white noise, if we define $y=e_1+e_2$, the distribution ρ_y can be expressed as:

$$\rho_y(k) = \begin{cases} 0 & \text{when } |k| > (3\Delta)/2 \\ \frac{\left(\frac{3}{2}\Delta + k\right)}{(2\Delta^2)} & \text{when } (-3\Delta/2) \leq k \leq (-\Delta/2) \\ \frac{1}{2\Delta} & \text{when } (-\Delta/2) \leq k \leq (\Delta/2) \\ \frac{\left(\frac{3}{2}\Delta - k\right)}{(2\Delta^2)} & \text{when } (\Delta/2) \leq k \leq (3\Delta/2) \end{cases} \quad (2.15)$$

The detailed derivation of the above equation is presented in the attached paper 2.

Fig 2.19 shows the simulated quantizer input distribution of a 2nd order 3-bit modulator compared with the calculated curve using equation 2.15, when the input signal amplitude is negligible.

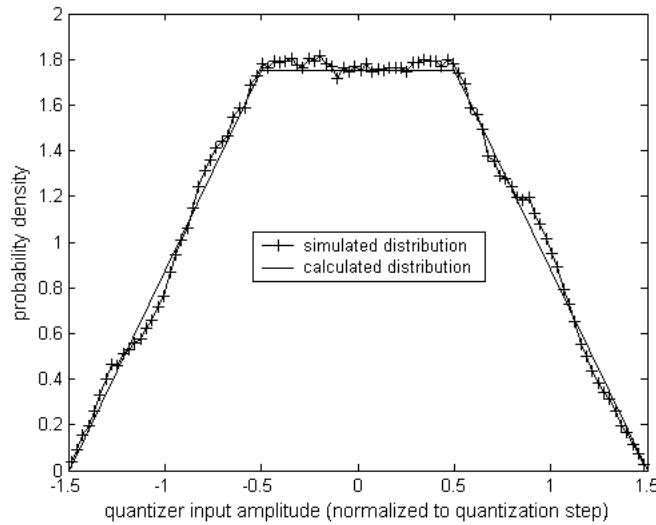


Fig 2.19 Quantizer input distribution

When the input signal is also taken into consideration the distribution of Q becomes much more complicated. It is not possible to give a close form of Q 's distribution because the input signal x is an unknown waveform. But generally if the amplitude of x is relatively small compared with $\Delta/2$, the distribution of Q will be similar to the one in Fig 2.19 but have a larger value at the center and a smaller value at the sides, given that x and ε are not correlated. Thus the distribution of Q would appear more similar to a Normal Distribution (Gaussian distribution), or in other words, Q is more likely

to have a small amplitude than a large amplitude. As will be discussed later, this is the essential condition to take the advantage of non-uniform quantization.

2.2.5 Quantizer non-idealities

A real quantizer always has non-idealities such as offset, gain error, and non-linearity as shown in Fig 2.20, and hysteresis which is not shown in the figure. The hysteresis is related to the 'memory' of the quantizer, meaning that the current quantization result is influenced by the previous quantization result. Since the errors caused by these non-idealities are presented before the DAC (feedback loop), they are noise-shaped by the modulator together with the quantization error. And since they are normally much smaller than the quantization error, they will not become the dominant error source. This is different from DAC errors which are not noise-shaped and often limit the conversion resolution.

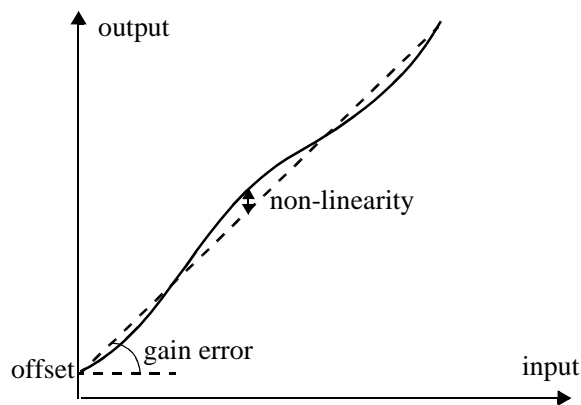


Fig 2.20 Non-ideal quantizer transfer curve

2.2.6 Construction

A quantizer compares the input voltage against a set of threshold voltages, or reference voltages. The reference voltages are generated by a set of unit elements like resistors and capacitors. The circuit realization is straightforward. An example is shown in Fig 2.21.

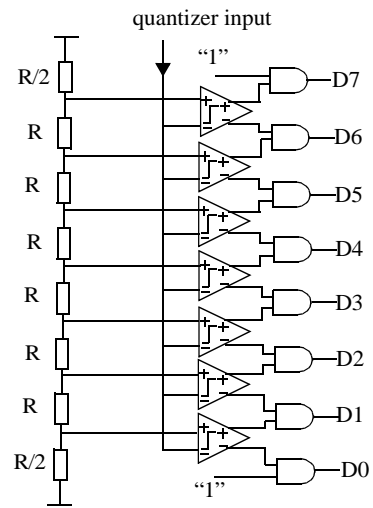


Fig 2.21 Quantizer realization

3 Multi-bit Modulators for Wireless communications

3.1 Wireless communication history

According to ITU's (International Telecommunication Union) definition, *Telecommunication* is any transmission and/or emission and reception of signals representing signs, writing, images and sounds or intelligence of any nature by wire, radio, optical or other electromagnetic systems. When the media is radio, it is called wireless communication or radio communication. The history of wireless communication can be traced back to the nineteenth's century. The following list shows some of the important milestones in the early stage of wireless communication:

- 1820 *Discovery of electromagnetism by Hans Christian Oersted and Andre-Marie Ampere.*
- 1864 *James Clerk Maxwell proved the existence of electromagnetic waves.*
- 1887 *Heinrich Hertz sent and received wireless waves.*
- 1895 *Guglielmo Marconi sent morse radio signals.*
- 1901 *Marconi received the morse message sent across the Atlantic.*
- 1907 *Commercial Trans-Atlantic Wireless Service put into use.*
- WWI *Rapid development of communications intelligence, intercept technology, cryptography.*
- 1915 *Wireless voice transmission from New York to San Fransisco.*
- 1920 *Marconi discovered short wave radio.*
- 1920 *First commercial radio broadcast (in Pittsburgh)*
- 1921 *Police car dispatch radios, Detroit.*
- 1930 *BBC began television experiments.*
- WWII *Rapid development of radio technology.*

3.1.1 Technology evolution

In the early phase, the transceivers were realized using vacuum tubes (an receiver example is shown in Fig 3.1) or later discrete semiconductor devices (an receiver example is shown in Fig 3.2). The large space and power consumption as well as the cost make it impossible to realize the idea of *personal communication*. With the invention and fast development of integrated circuit (IC) technique, more and more signal processing (analog or digital) functions can be integrated into a single tiny chip. The mobile transceivers are made small enough to put into pocket, low-power enough to use batteries, and cheap enough to be affordable by normal domestic users.

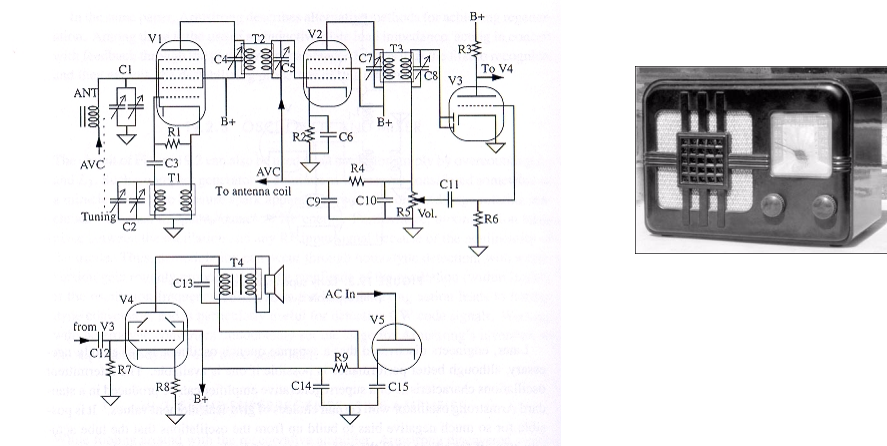


Fig 3.1 "All-american" 5-tube radio

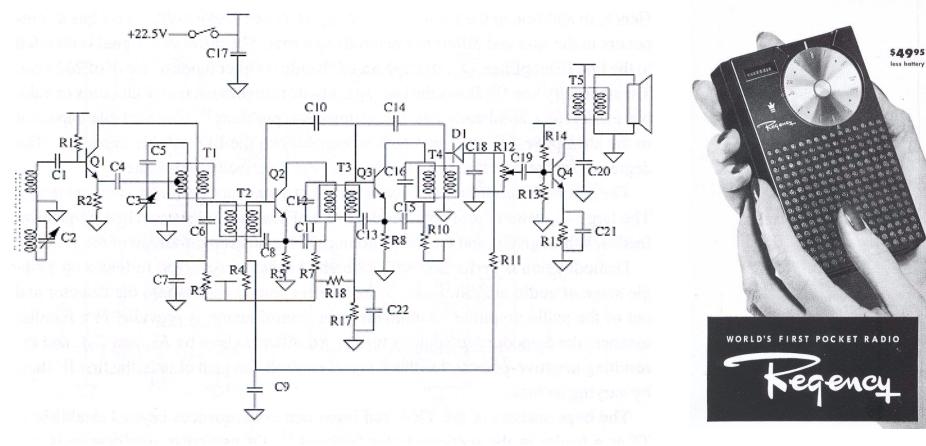


Fig 3.2 Early pocket radio

3.1.2 Spectrum allocation

The hardware development is only one of the essential conditions for the realization of personal communication. Another problem to be solved is the spectrum management. The radio spectrum available for public use is limited while the demand of it is huge, considering that thousands of people need to talk through mobile phones at the same moment. This problem is cleverly solved by the cellular technique, which was

first developed and experimented in the Bell Laboratory. The basic idea is that a service area (e.g. a city) is spitted into many cells. In each cell there is a base station communicating with mobile terminals. The power of the base station signal is so small that the signal will not spread much further out of that particular cell. As a result, the frequency band used in this cell can be re-used in other cells that are far away from it. A concept diagram of a cellular system is shown in Fig 3.3.

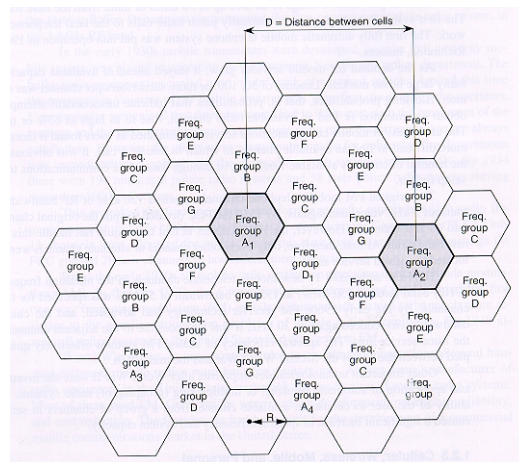


Fig 3.3 Concept of cellular technique

3.1.3 Three generations of cellular systems

In the short history of cellular systems, three generations have been developed.

1G (1st Generation) systems

Using the cellular technique, the 1G systems have higher capacity and greater mobility support than earlier wireless radio networks. The 1G systems are analog systems, meaning that the signal is processed and transported in analog format. Examples of 1G systems are NAMTS in Japan, NMT-450 (later NMT-900) in Scandinavia, AMPS in USA, C-450/NETZ-C in Germany, and TACS in UK.

2G systems/2.5G systems

The second generation (2G) wireless systems are characterized by the use of digital radio transmission. Using hierarchical cell structures and multiple access technologies like CDMA and/or TDMA, the system capacity is further extended compared with 1G systems. The largest 2G system currently in operation is the GSM family, including the original GSM 900MHz system, the higher frequency GSM 1800 MHz system which is also called DCS1800 (Digital Communication System), and the US version

of DCS1800 - GSM 1900MHz, which is also called PCS1900 (Personal Communication System). As shown in Fig 3.4, by February 2003 the GSM family holds 70 percent of the global cellular phone market. The second largest system is the IS-95 CDMA, which dominates the US market. Different from GSM, which uses time-division-multiple-access technique, the IS-95 system uses code-division-multiple-access technique. Beside GSM, In US there are other TDMA systems, e.g. IS-54 (later IS-136). In Japan the main system is PDC (Personal Digital Cellular).

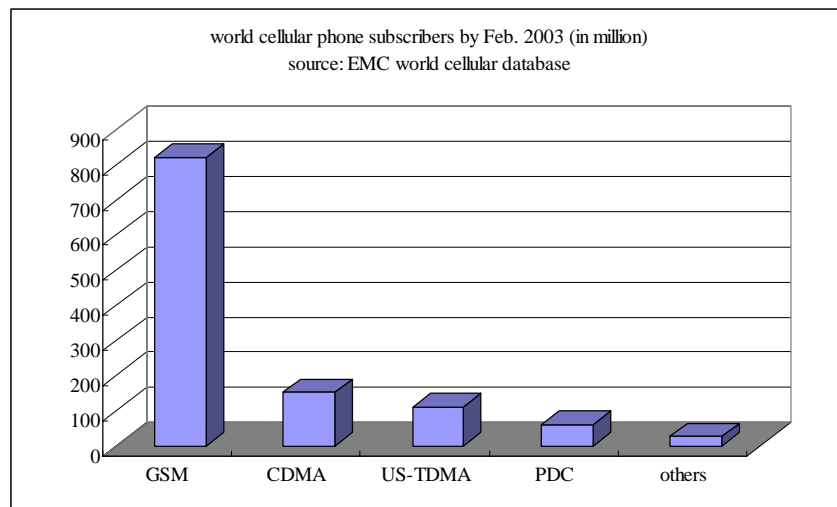


Fig 3.4 World cellular phone subscribers

The 2.5G systems are updates of 2G systems with improved data communication capability. In GSM system the data rate is only 9.6 kbps. The HSCSD (High Speed Circuit Switched Data) system is an update of GSM by using several time slots simultaneously when sending or receiving data from mobile users. The speed can be up to 57.6 kbps. Similar to GSM, HSCSD still uses circuit-switching technology to transfer data. In circuit switching, a communication channel is opened and dedicated to a user for the duration of the communication. A more revolutionary development is the GPRS (General Packet Radio Service) and EDGE (Enhanced Data rates for Global Evolution) systems, both using packet-switching technology. Packet switching splits the user's data into small parts called packets. Packet switching uses the communication system more effectively and enables users to be "always online" without the need of dial-up. The theoretical data rate is 144 kbps for GPRS and 384 kbps for EDGE.

3G systems

The data rates provided by 2G or 2.5G systems are not enough in cases like large image or video transfer. The 3G systems are developed to satisfy such requirements. There are three 3G standards under development: WCDMA proposed in Europe,

CDMA2000 proposed in America, and TD-SCDMA proposed in China. They all use CDMA access technique and support up to 2Mbps data rate. The standards of 3G systems are still under development and the commercial operation has just started.

3.2 Wireless receiver structure

3.2.1 Superheterodyne structure

Nearly all wireless receivers adopt the "superheterodyne" structure, where a radio frequency (RF) signal is frequency-translated to a much lower intermediate frequency (IF) signal using a mixer. A traditional superheterodyne digital receiver's block diagram is shown in Fig 3.5.

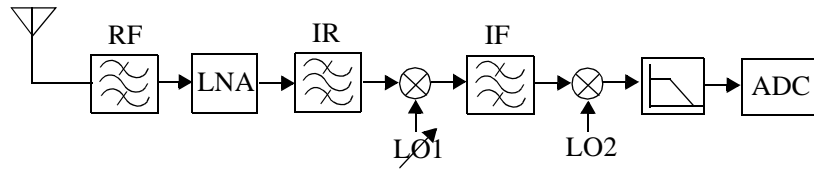


Fig 3.5 Superheterodyne receiver

Since the IF signal frequency is fixed, the gain stage and IF filter are easy to design. The requirement on the ADC is low because the neighboring channels are filtered out. Due to its superior performance, the superheterodyne structure is the dominant choice in transceiver design. However the main drawback of the conventional superheterodyne structure is the low integration level. The RF filter, IF filter and IF filter are not easy to be integrated into transceiver front-end chips with a reasonable performance in current technology level. It is the need of low cost, small size, and low power that stimulates the development of new transceiver structures with reduced number and/or requirement on filters. In a traditional superheterodyne transceiver the channel selection is done in analog domain by IF filters. To largely attenuate the out-of-band signal or noise, the IF filter needs a sharp edge, making it difficult to be integrated. On the other hand, since the input to the ADC is already channel-selected, only the wanted signal is there and the requirement on the ADC is low. If not only the wanted signal but also the neighboring channel is sent to the ADC and converted to digital signal, then the channel selection is performed in digital domain. In digital domain it is much easier to make the channel selection programmable, and the cost is lower. The drawback is that the wanted signal must be converted together with the much larger neighboring channel or blocker signal, putting a very strict dynamic requirement (normally above 12bit) on the ADC. The ultimate target of the so-called "software radio" is to eliminate all the analog components in a receiver except the RF filter and the LNA. The

filtered RF signal is directly converted by a super-ADC. The converted signal is then digitally channel-selected and processed. The bandwidth and resolution requirement on the ADC in such a software radio is so high that it is impossible to realize in the near future. Even if it becomes technically feasible to design such an ADC in the future, it would take longer time to make it economically feasible. The currently feasible and often used high-integration structures are low-IF and direct conversion structures.

3.2.2 Direct conversion (homodyne) structure

The direct conversion structure is also called zero-IF structure, or homodyne structure. The RF signal is directly mixed to base-band. The IF stage is cancelled and the signal is the image of itself. It is much simpler compared with traditional superheterodyne receivers as shown in Fig 3.6, and the required external components are largely reduced. The main drawbacks are 1) the mixer output might contain large dc offset caused by self-mixing of the leakage oscillator signal with the oscillator signal itself, and 2) the flicker noise ($1/f$ noise) of the mixer can not be filtered since the mixer output is centered at dc. Therefore although it has a relatively long history, this structure is not widely used until recently. Nowadays many mobile receivers (e.g. from Alcatel, Ericsson, Nokia) adopt the homodyne structure.

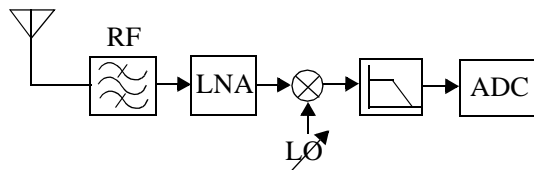


Fig 3.6 Homodyne receiver

3.2.3 Low-IF structure

The low-IF structure is somewhere between the traditional superheterodyne structure and the homodyne structure, as shown in Fig 3.7. It has a much lower-than-normal IF frequency, and thus avoids the main drawbacks of homodyne at dc. The whole IF band can be directly converted by a ADC, which can be either low-pass or band-pass. Like a homodyne, a low-IF receiver needs fewer external components and is easier to be integrated compared with the traditional superheterodyne structure. The drawback is that the image signal cancelling has to be performed by an image-rejection mixer, whose performance varies with process variations and temperature changes.

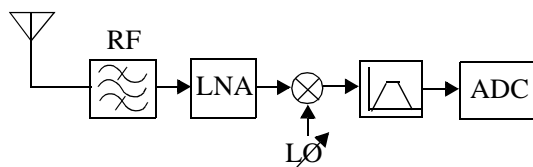


Fig 3.7 Low-IF receiver

3.3 Sigma Delta ADC in receivers

Table-1 lists some of the recently reported Sigma Delta ADCs or modulators designed for wireless transceivers/receivers. Their characteristics are summarized in the table.

Table 1:

Ref	RF stand.	RF struc.	process μm	ADC struc.	order	BW KHz	DR dB	SNDR dB	power mW	FOM $\times 10^{10}$
[Dez03]	WCDMA GPRS	zero-IF	0.13	SC 3-bit	3	1920 100	70 82	64 81	4.3 2.4	116
[Vel03]	EDGE, CDMA 2000, UMTS	low-IF/ zero-IF	0.18	CT 1-bit	5	200, 1228, 3840	92, 83, 74	92, 83, 74	3.8, 4.1, 4.5	699
[phi03]	bluetooth	low-IF	0.18	CT 1-bit	5	1000	76	75.5	4.4	221
[mil03]	CDMA		0.18	SC 6-bit	2	615		77	30	26
[Vel02]	UMTS	zero-IF	0.18	CT 1.5-bit	4	2000	70	68	3.3	249
[Gom02]	GSM, UMTS		0.13	SC 5-level	2	200, 2000	79, 50	75, 49	2.4, 2.9	76.6
[Bur01]	GSM, UMTS	superhet- erodyne	0.25	SC 1-bit	2	200, 3840	86, 54	72, 52	11.5, 13.5	18.5
[Oli01]	GSM, EDGE	low-IF	0.35 BiC- MOS	SC 1-bit	2-2	189	84	84	5	74.1
[Sal01]	GSM, UMTS	superhet- erodyne	0.35	SC 1-bit	2	270, 3840	80, ?	70, 43.3	61.2	2.2

When designing receivers for 2G systems, like GSM or CDMA, the signal bandwidth is within several hundred KHz. In that kind of bandwidth range, 12~16 bit resolution can be well achieved with current design and process technology. When migrating to 3G systems, the signal bandwidth goes into MHz range. The achievable resolution is reduced. As described before, in a receiver the higher resolution and bandwidth an ADC can achieve, the lower requirement it is for the RF front-end. Therefore to implement a high-integration-level 3G receiver, further increase in resolution is needed for current Sigma Delta ADCs, and at the same time the power consumption of ADCs must be kept reasonably low. A multi-bit Sigma Delta ADC is a promising candidate for these applications.

3.4 Non-uniform quantization

Most of quantization performed in A/D conversion is uniform quantization, which means the quantization steps are equal. This is natural because the numbering system we use are uniform systems where the distances between adjacent numbers are the same. The quantizer characters that are discussed in the previous section are all based on uniform quantizers.

Although uniform quantizer is almost the exclusive choice in Sigma Delta ADCs, possible applications of non-uniform quantizers were explored [Zha91]. Non-uniform quantizers have different quantization steps for inputs with different amplitudes. To take the advantage of non-uniform quantization in Sigma Delta ADCs, the quantization steps should be arranged in such a way that small-amplitude input is quantized by small quantization steps and large-amplitude inputs by large steps.

3.4.1 Precondition to use non-uniform quantizer

The reason to use non-uniform quantizer is to reduce the overall quantization error power, which is expressed in equation 2.11 and repeated here:

$$P_{\varepsilon} = \int_{-\infty}^{\infty} \rho(x) \varepsilon^2(x) dx$$

As proved in section 2.2.2, for a uniform quantizer this power is a constant. However for a non-uniform quantizer this conclusion does not hold. For a non-uniform quantizer, its quantization error $\varepsilon(x)$ is smaller than that of a uniform quantizer when the amplitude of x is small, and its $\varepsilon(x)$ is larger than that of a uniform quantizer when the amplitude of x is large. Therefore the precondition to use a non-uniform quantizer is that the quantizer input distribution concentrates in the small-amplitude range, so that the overall noise power can be reduced by using a non-uniform quantizer. Fortunately this precondition is satisfied in a Sigma Delta modulator. In section 2.2.4 it is proved that when the modulator input signal amplitude is small the quantizer input distribution always has a form similar to a Normal Distribution, which means the quantizer input is more likely to have a small amplitude rather than a large amplitude.

3.4.2 μ -law quantizer

[Zha91] proposed to arrange the quantization steps corresponding to μ -law. Such a quantizer has an exponential input-output transfer curve, and its corresponding DAC has a logarithmic input-output transfer curve. It is especially suitable for applications like voice processing. But to generate the threshold voltages for such a quantizer is not easy. First, the largest quantization step could be tens of times larger than the smallest step. Matching the quantization steps in such a wide range is difficult. Second, the different quantization steps are not linearly changing, therefore it is not possible to use unit element to match these steps.

3.4.3 semi-uniform quantizer

The name "semi-uniform" means that there are only two different-size quantization steps [Li01a] [Li03b], making it very similar to a conventional uniform quantizer. The small quantization step is for small inputs and the large step for large inputs. Specifically, for a k -bit semi-uniform quantizer with normalized full-scale range of $-1 \sim +1$, the center $2k+1$ quantization steps have a step size of $\Delta_1 = \frac{2}{2^{k+1}-1}$, and the outer $2k-1$ quantization steps have a step size of $\Delta_2=3\Delta_1$.

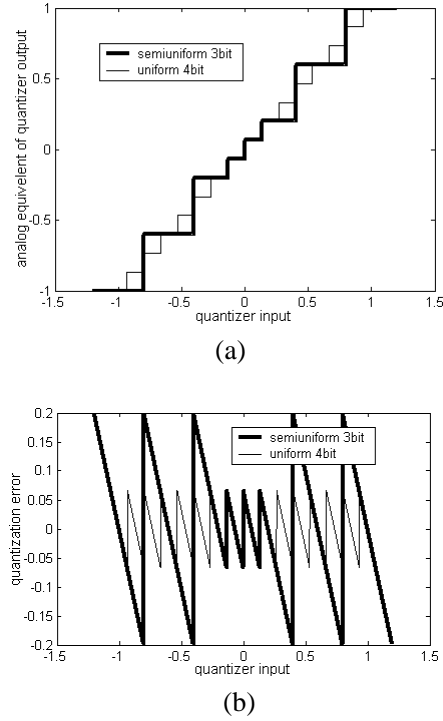


Fig 3.8 Semi-uniform quantization
(a) transfer curve (b) quantization error

Fig 3.8a and Fig 3.8b show the quantization levels and quantization error of a 3-bit semi-uniform quantizer, compared with that of a 4-bit uniform quantizer. It can be seen that actually the 3-bit semi-uniform quantizer's 8 quantization levels are all "borrowed" from the 4-bit uniform quantizer's 16 levels. As a result, the quantization error of the semi-uniform quantizer is also closely related to that of a uniform quantizer. At the four center steps the quantization error of both the 3-bit semi-uniform and 4-bit uniform quantizers are the same, while at the outer steps the semi-uniform quantization error can be three times as

large as that of the 4-bit uniform quantizer. This implies that if most of the quantizer inputs fall into those small quantization steps, a k -bit semi-uniform quantizer could achieve the same dynamic range as a $(k+1)$ -bit uniform quantizer, as will be demonstrated shortly.

When using a semi-uniform quantizer, the quantization error ε is a function of the quantizer input x . When x falls into those smaller quantization steps,

$$\varepsilon(x) = \frac{1}{2^{k+1}-1} - \text{mod}\left[x, \frac{2}{2^{k+1}-1}\right]$$

Here $\text{mod}(a,b)$ is the modulo function with b as modulo. When x falls into those larger quantization steps and quantizer is not overloaded,

$$\varepsilon(x) = \frac{3}{2^{k+1}-1} - \text{mod}\left[\text{sign}(x)\left(|x| - \frac{2^{k-1}+2}{2^{k+1}-1}\right), \frac{6}{2^{k+1}-1}\right]$$

Here $\text{sign}(a)$ is the sign function. When the quantizer is overloaded,

$$\varepsilon(k) = \text{sign}(x)(1 - |x|)$$

3.4.4 Semi-uniform quantizer/DAC design

One of the advantages of semi-uniform quantizer is its simple structure. The circuit of a semi-uniform quantizer can be constructed in the same way as a uniform quantizer. They use the same number of comparators. The only difference is how the thresholds for the comparators are generated. When using unit elements (e.g. resistor) to generate the threshold voltages, a semi-uniform quantizer needs double number of unit elements compared with a same resolution uniform quantizer. Since there are only two quantization steps, and the bigger one is three times as large as the smaller one, matching is easy to realize. Fig 3.9 shows a 3-bit uniform/semi-uniform dual-mode quantizer. In both modes the same set of comparators is used. The different threshold voltages are generated by two resistor ladders. The number and value of unit elements in two ladders are different. One of the two sets of threshold voltages is selected by a switch and fed to the comparator array.

Similarly, a 3-bit uniform/semi-uniform dual-mode DAC can be constructed, as shown in Fig 3.10. Two resistor ladders generate two sets of output analog voltages according to the input digital code. Through a switch, the selected one is sent to DAC output.

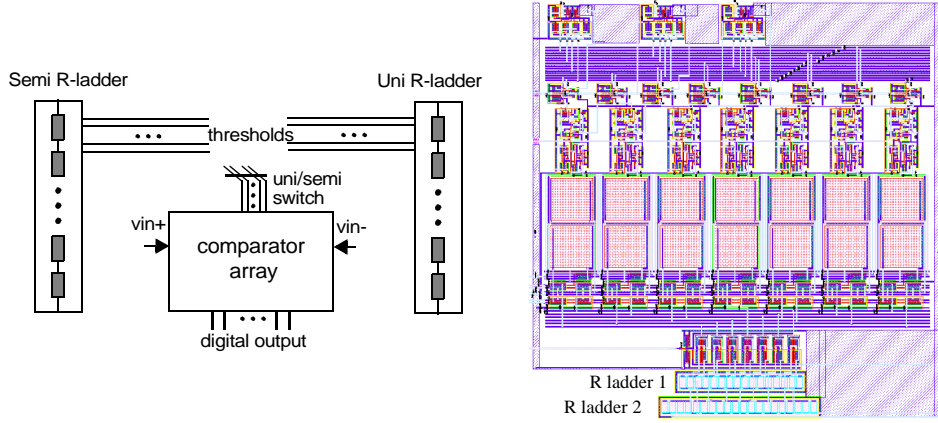


Fig 3.9 Dual-mode quantizer

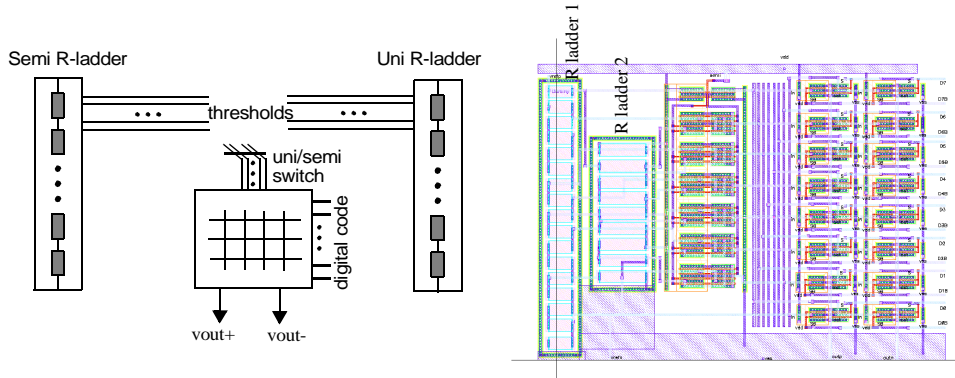


Fig 3.10 Dual-mode DAC

3.4.5 Measured performance

The advantage of semi-uniform quantizer is verified by a second order modulator using the demonstrated 3-bit dual-mode quantizer and DAC. At a 3V supply voltage the power consumption is 9.3mW. Simulation results show that about 32% of the power is consumed by the 3-bit quantizer and 41% by the two OTAs. The active chip area is 0.23mm^2 . At 6.4MHz sampling frequency and 32x oversampling ratio, the signal bandwidth is 100kHz. Using a semi-uniform quantizer achieves a peak SNDR of 63.8dB and a dynamic range of 81dB. Using a uniform quantizer achieves a peak SNDR of 54.1dB and a dynamic

range of 70dB. Fig 3.11 shows the measured SNDR versus input amplitude. Comparing the spectrum of the modulator outputs with both quantizers in Fig 3.12, it can be seen that the noise floor is significantly lower when using the semi-uniform quantizer.

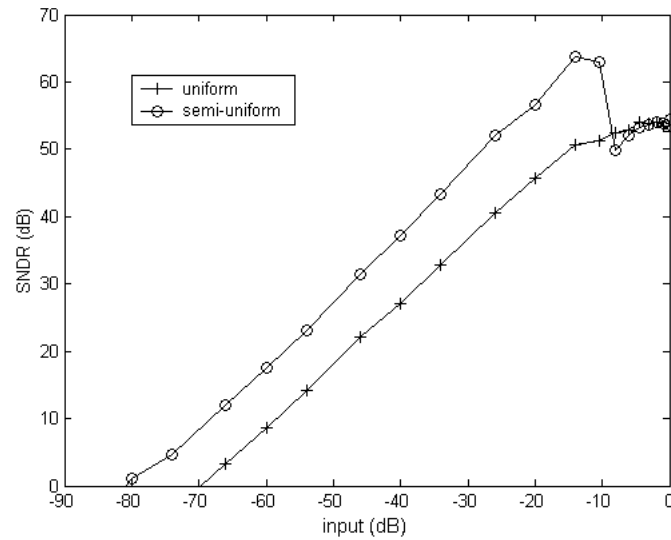


Fig 3.11 SNDR comparison

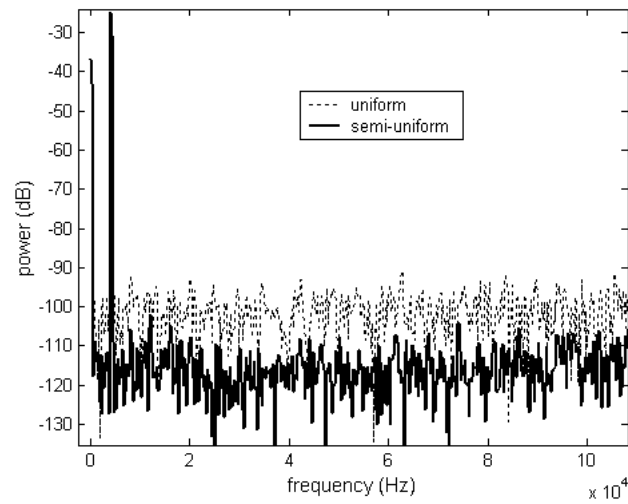


Fig 3.12 Noise floor comparison

3.5 Multi-bit modulator with 1-bit DAC

The biggest problem associated with a multi-bit Sigma Delta modulator is the multi-bit DAC nonlinearity problem. Since the DAC is located in the feedback loop, the error caused by its non-idealities e.g. gain error, offset, and non-linearity will not be noise-shaped, which is the case for quantizer non-idealities. But the influence of these DAC non-idealities are not the same. An offset causes a dc error at the modulator output, which is of no importance in most cases. A gain error adds extra poles to the noise transfer function, and hence changes the in-band quantization error power slightly. Its influence is often negligible. A non-linearity, however, is signal correlated. For each specific digital code, the DAC has a specific non-linearity error. This one-to-one determinacy between the non-linearity error and DAC input code causes distortion, instead of noise, in the modulator output as shown in Fig 3.13.

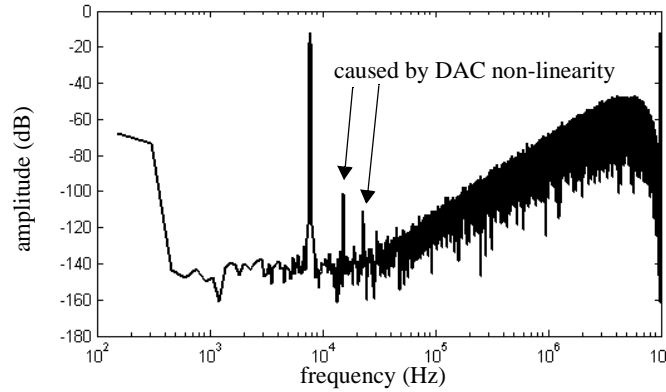


Fig 3.13 Second order 3-bit modulator output spectrum with 0.1% DAC non-linear error and -6dB input

Dynamic Element Matching (DEM) is the most popularly used circuit technique to reduce the influence of DAC non-linearity. The basic idea is to break the one-to-one determinacy between the non-linearity error and DAC input code, and thus break its signal-dependence. As a result, the non-linearity will no longer cause in-band distortion. Instead it will cause either an increased noise floor or out-of-band distortions. Basic DEM algorithms include randomization [Car88], individual level averaging [Leu92], and data weighted averaging [Bai95].

3.5.1 DEM algorithms

The randomization algorithm randomly chooses a set of DAC elements at each clock cycle so that the DAC non-linearity error is turned into a white noise, whose power is mainly

out-of-band and will be digitally filtered. Compare its spectrum in Fig 3.14 with Fig 3.13, it can be observed that the distortions disappear but the noise floor is increased slightly.

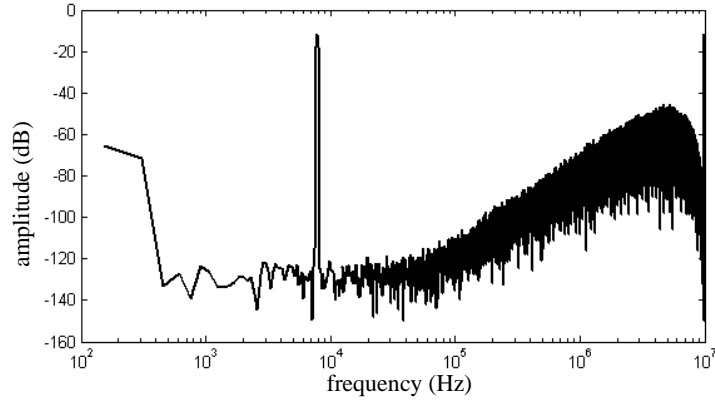


Fig 3.14 Second order 3-bit modulator output spectrum with randomization DEM

The individual level averaging algorithm sets a pointer for each DAC input digital code to make sure that all the DAC elements are equally used for each digital input code. The DAC non-linearity error is partly noise-shaped, so its noise floor shown in Fig 3.15 is lower than that using randomization algorithm.

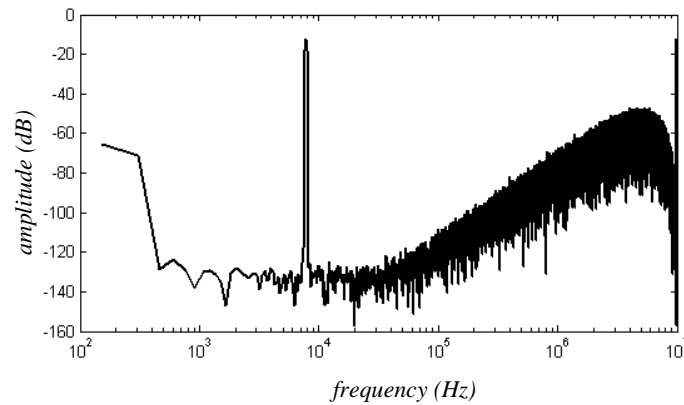


Fig 3.15 Second order 3-bit modulator output spectrum with individual level averaging DEM

The data weighted averaging algorithm sets one pointer to record the position of the DAC element that was last used, and each DAC element is guaranteed to be used equally often. The DAC non-linearity error goes through a first-order noise shaping, therefore its noise floor as shown in Fig 3.16 is the lowest.

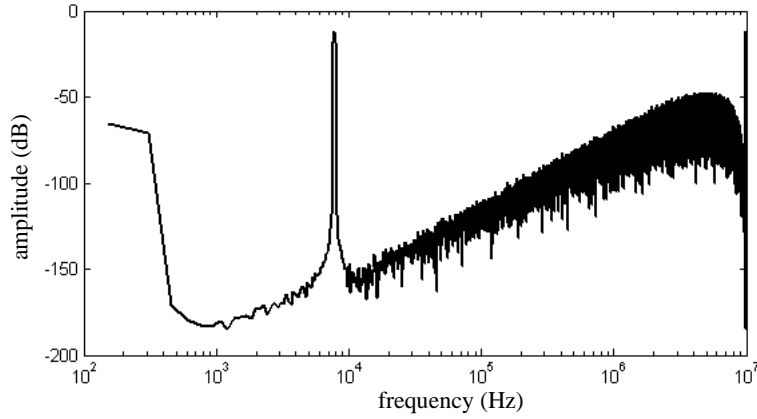


Fig 3.16 Second order 3-bit modulator output spectrum with data weighted average DEM

3.5.2 Derivation

One way to solve the DAC non-linearity problem on circuit level is to use a 1-bit DAC in a multi-bit Sigma Delta modulator [Les90]. The derivation of such a structure can be illustrated in two ways.

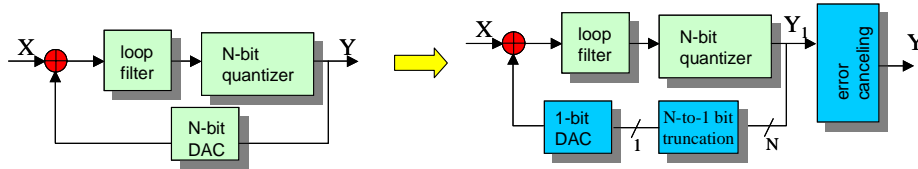


Fig 3.17 Derivation from single-stage multi-bit modulator

The left side of Fig 3.17 is a conventional N -bit single-stage Sigma Delta modulator. In the feedback a N -bit DAC is used. If the data length is truncated from N -bit to 1-bit, a 1-bit DAC can now be used. The truncation error needs to be compensated digitally in the error-cancelling block.

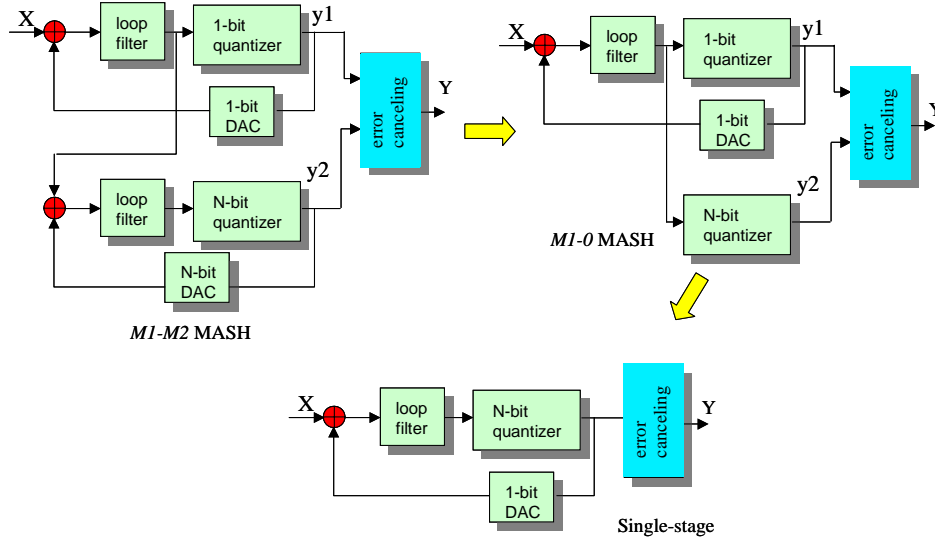


Fig 3.18 Derivation from MASH structure

Another way to understand the function of this structure is to start from a MASH structure modulator, as shown in Fig 3.18. The orders of the two stages are M_1 and M_2 , which is noted as M_1 - M_2 MASH. The first stage uses a 1-bit quantizer, while the second stage uses a N -bit quantizer. The outputs from the two quantizers are combined in the error-cancelling block to generate the modulator output. If the order of the second stage is reduced to 0, then we get a M_1 -0 MASH structure. As a result, the loop filter and N -bit DAC in the second stage are skipped, only the N -bit quantizer remains. Since now the two quantizers have exactly the same input, the 1-bit quantizer can be physically skipped because the output of the 1-bit quantizer is always equal to the MSB (Most Significant Bit) of the N -bit quantizer. Now it becomes a single-stage modulator with a N -bit quantizer and a 1-bit DAC.

3.5.3 Linear model before signal scaling

In his original paper [Les90], Leslie provided a linear model analysis of the modulator using multi-bit quantizer and 1-bit DAC. The conclusion is that ideally this structure will achieve exactly the same resolution as a conventional multi-bit modulator. In that linear model the quantizer is assumed to have a unit gain. For a conventional multi-bit modulator this assumption is always true. For a 1-bit modulator the quantizer linear gain is defined by the loop coefficients. Assuming a unit quantizer gain means that no signal scaling is performed to the modulator. Such a modulator can not be implemented and used, because the required internal signal swing is too large. After signal scaling, a 1-bit quantizer always has a linear gain larger than unit. A modulator combining a multi-bit quantizer and 1-bit DAC is basically a 1-bit modulator plus an extra multi-

bit quantizer, as can be seen from Fig 3.18. Therefore the unit-quantizer-gain assumption does not hold for the modulator combining multi-bit quantizer and 1-bit DAC. For example, the linear model of such a second-order modulator before signal scaling and its integrator output histogram is shown in Fig 3.19. The reference voltage is normalized to ± 1 . It can be observed that the quantizer is severely overloaded.

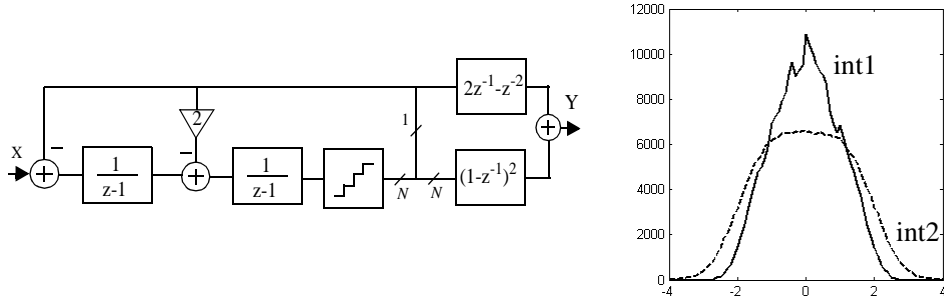


Fig 3.19 Linear model before signal scaling

3.5.4 Linear model after signal scaling

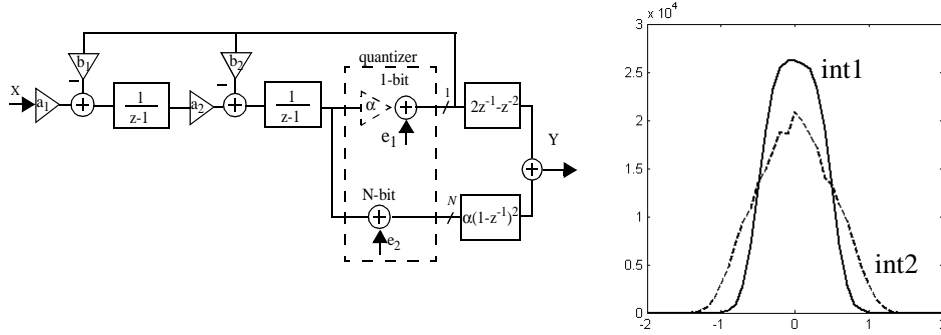


Fig 3.20 Linear model after signal scaling

In the linear model shown in Fig 3.20 the coefficients a_1 , a_2 , b_1 and b_2 are used to adjust the internal signal swing. Here the N -bit quantizer is modelled as two separate ones: a N -bit quantizer and a 1-bit quantizer. The output of the 1-bit quantizer is used to drive the feedback. This makes the model easier to analyze, and makes it clear that it is basically a 1-bit modulator plus a N -bit quantizer. Therefore the signal scaling procedure is similar to that of a 1-bit modulator instead of a multi-bit modulator. For the N -bit quantizer, its gain is unit. For the 1-bit quantizer, its gain α is determined by the

coefficient b_1 and a_2 : $\alpha=1/(b_1a_2)$. To reduce the internal signal swing b_1 and a_2 have to be small enough. A common choice is to set $a_1=a_2=b_1=b_2=0.5$. The two integrator output histograms show that most quantizer inputs are bounded between \pm reference voltages. But since the 1-bit quantizer gain α is set to be larger than unit, the N -bit quantization error is enlarged by a factor of α in the final modulator output:

$$Y = Xz^{-2} + \alpha(1 - z^{-1})^2 e_2 = Xz^{-2} + \frac{(1 - z^{-1})^2 e_2}{b_1a_2}$$

A design consideration here is to optimize the value of α so that the quantization error is not enlarged too much, while at the same time the internal signal swing is kept low to ensure modulator stability [Rit90]. Generally, when the modulator order increases (in a single stage) the loop coefficients have to be scaled smaller to control the internal signal swing, which leads to a larger α and therefore larger in-band quantization error power. For the second order modulator shown in Fig 3.20 the α is 4, introducing a 12dB resolution reduction. For higher order single-stage modulators optimized using the MATLAB toolbox provided by Richard Schreier [Sch88], a third, forth, and fifth order modulator has a quantizer gain of 23, 164, and 1428 respectively. It is obvious that the resolution reduction is not affordable for a modulator order higher than 3. This implies that a low order modulator can take more advantage by combining a multi-bit quantizer with a 1-bit DAC. In fact a first order Sigma Delta modulator is most suitable for such a structure because it does not need to do signal scaling and thus its quantizer gain is unit. Unfortunately a first order modulator suffers from the problems of tones as well as high in-band quantization power, thus it is seldom used in practice.

3.5.5 Measured performance

The simulated performance of a second order modulator using 1~6 bit quantizers and 1-bit DAC is plotted in Fig 3.21. The sampling frequency is 32MHz and the oversampling ratio is 16, corresponding to a signal band of 1MHz. The input sinusoidal signal is at 30kHz. Also plotted in the figure are measured results of such a modulator using 5-bit quantizer and 1-bit DAC [Li03a]. Fig 3.22 compares the measured noise floors of the output spectrum using a 5-bit quantizer and a 1-bit quantizer respectively. When using a 5-bit quantizer the quantization error is much smaller than that of a 1-bit quantizer, as a result the noise floor is pushed down.

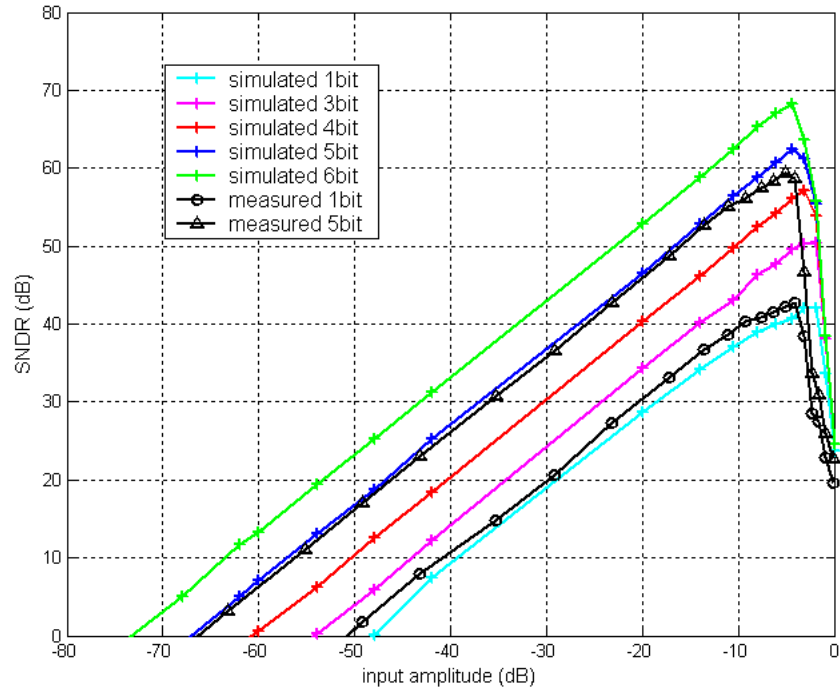


Fig 3.21 Measured 2nd order modulator SNDR

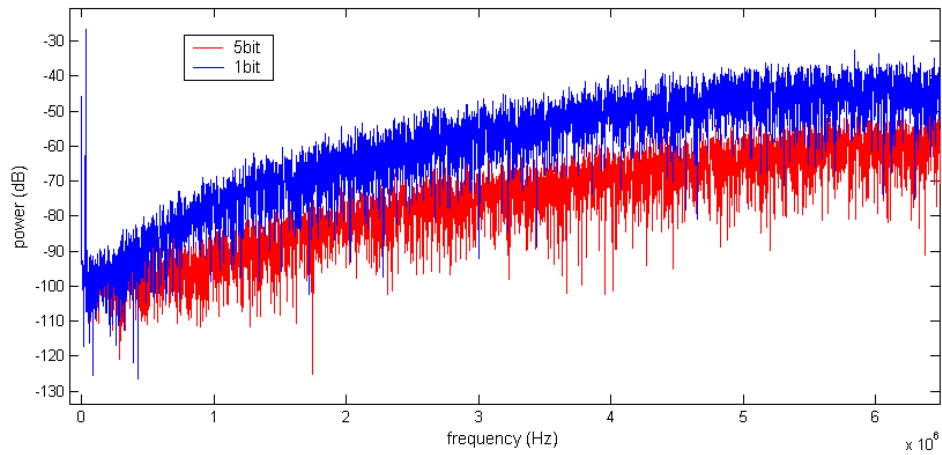


Fig 3.22 Measured 2nd order modulator spectrum

4 Future Design Challenges

4.1 Ultra low voltage design

4.1.1 Background

In the past decades the development of CMOS technology closely follows Moore's law. Most experts expect that this trend will continue at least in the near future. One aspect of the technology advance is the continuous decrease of gate oxide thickness. In order to prevent the electric field strength from being too high, the supply voltage should be reduced in a similar scale. According to the ITRS (International Technology Roadmap for Semiconductors) roadmap 2001, the predicted gate oxide thickness, process feature size, and supply voltage are shown in Fig 4.1.

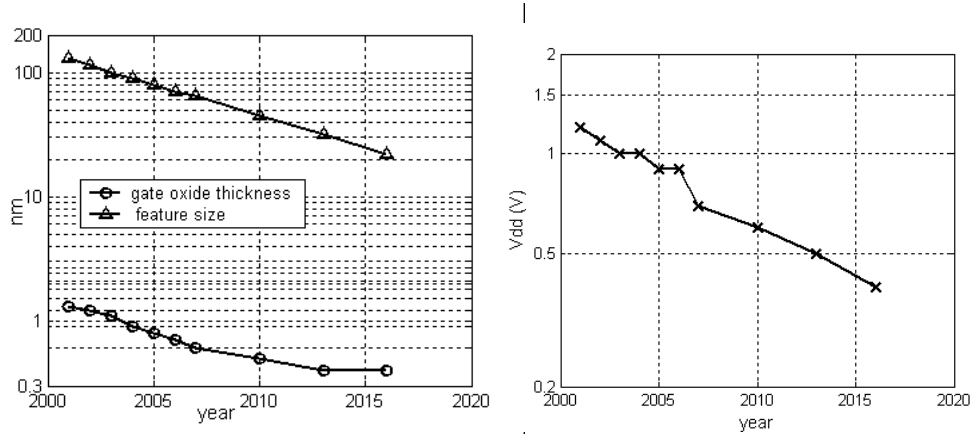


Fig 4.1 ITRS roadmap prediction

In 10 years from now the supply voltage for CMOS circuits will drop to 0.5V, meaning that many widely used analog circuit topologies will no longer be applicable.

4.1.2 Design problems in Sigma Delta modulator

Using switched-capacitor circuit is the most robust way to construct a high resolution Sigma Delta modulator. To make it work, the charge stored in capacitors must be transferred through switches. In a switched-capacitor circuit the switches can be divided into two types, as shown in Fig 4.2 with the example of an integrator. Switches s_2 , s_3 have one of their terminals connected to GND. Therefore as long as $V_g > V_{GND} + V_t$,

the switch will conduct. Switch s_4 has one of its terminals connected to the virtual ground of the Opamp, therefore it can also be treated as connecting to the GND. For this type of switch a single NMOS transistor can be used. Switch s_1 and s_5 however have both of their terminals 'floating', not connected to a fixed voltage level. Since the signal level can be any value between the power rails, a complementary switch has to be used. The transconductance of such a complementary switch is shown in Fig 4.3. When $V_{dd} > V_{t,n} + V_{t,p}$, there is a signal range in which both the NMOS and PMOS transistor conducts. When $V_{dd} = V_{t,n} + V_{t,p}$ there is only one transistor conducting at any time. In the case $V_{dd} < V_{t,n} + V_{t,p}$, there is a signal range in which none of the transistors conducts, meaning the switch fails to work. Therefore the supply voltage must be larger than the sum of PMOS and NMOS threshold voltages to keep the complementary switch function properly. At an ultra low supply voltage, this condition is difficult to meet. The design of OTA and comparator also becomes more difficult under a ultra low supply voltage.

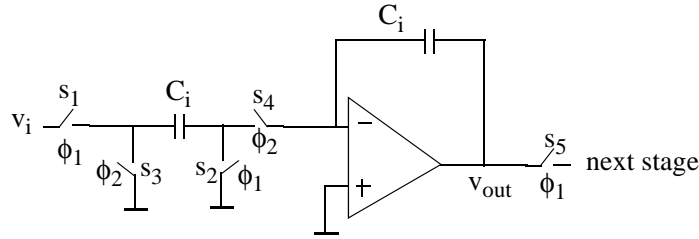


Fig 4.2 Switched-Capacitor Integrator

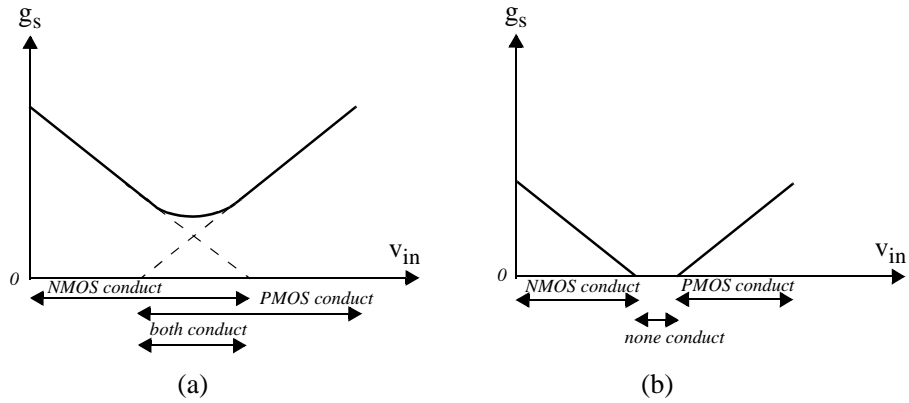


Fig 4.3 Complementary switch transconductance

a) $V_{dd} > V_{t,n} + V_{t,p}$ b) $V_{dd} < V_{t,n} + V_{t,p}$

4.1.3 Voltage multiplier

Using a voltage multiplier [Cas01] or bootstrapping [Des01] circuit to provide a high gate voltage for switches is currently often adopted. Only a small part of the circuit works under a high voltage and the rest part of the circuit sees a normal supply voltage. The drawback of this solution is obvious: 1. it is not a true low voltage design. The high gate voltage might break down the gate oxide layer, causing reliability problem. 2) the voltage multiplier or bootstrapping circuit requires a large chip area and power. So this solution is not a robust one when the process is further scaled down.

4.1.4 Switched opamp

One solution to the switch conducting problem is to replace the switch of S5 in Fig 4.2 by a sample-and-hold buffer [Cro94], [Pel97]. The buffer samples the previous Opamp output at one clock phase, and buffer it to the next stage at another clock phase. The circuit is shown in Fig 4.4. Since now all the switches have one of its terminals connected to GND, they are able to conduct as long as $V_{dd} > V_{t,n}$. The price for the solution is that the Opamp has to be switched on and off every clock cycle, because its output will be shortened to GND in one of the phases. This causes the drawback of low speed. Currently the switched-opamp circuit speed is around 10MHz. [Che02].

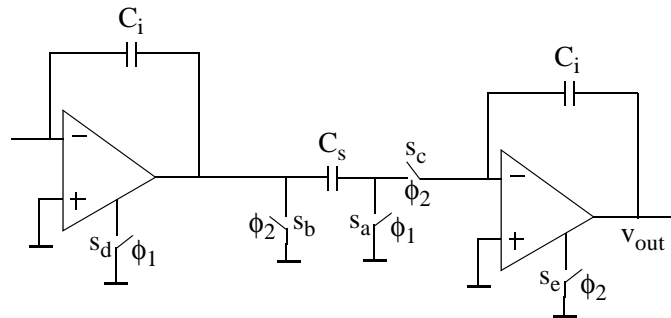


Fig 4.4 Switched-opamp circuit

4.1.5 Low/Zero V_t process

Since the supply voltage V_{dd} must be larger than $V_{t,n} + V_{t,p}$ to make the switch function correctly, the most straightforward solution is to use low- V_t or even zero- V_t process [Ada90], [Baz95a]. This kind of process also eases the design of Opamp and comparator. Nowadays many circuits are designed with multi- V_t process, where low- V_t MOS transistors can be used when needed. The cost of such processes are higher than standard CMOS processes. But with the continuous advance of processing technology, the increase need for such multi- V_t processes will make it become a commonly used stan-

dard. Once widely adopted, the process cost will be reduced dramatically. Another concern about the low/zero V_t process is the leakage current. The subthreshold current of a MOS transistor is:

$$I_{DS} = I_{st} e^{\left(\frac{V_{GS} + \sigma V_{DS} - V_t}{nkt/q} \right)}$$

The coefficient I_{st} and parameters σ and n are determined empirically. It can be observed that 1) the subthreshold current drops exponentially with V_{GS} , and 2) the subthreshold current is closely related to the value of V_t . When V_t is reduced, leakage current increases dramatically. For a switched-capacitor integrator a leakage current causes a charge-leakage, which in turn causes an output voltage change.

The subthreshold current can be well controlled within the order of pA, by using series transmission gate [Baz95b] or increasing the source to substrate voltage [Baz95a]. As a rule of thumb, a 100dB SNR switched-capacitor circuit with a power supply of 1V and an switch-on-resistance of 10kOhm requires a subthreshold current less than 1nA [Baz95b]. Therefore the leakage current will not become the performance bottleneck when using low/zero- V_t process.

4.2 Substrate coupling

With the development of design and process technique, a Sigma Delta ADC can be made smaller and less power consuming. Hence it is easier to embed a Sigma Delta ADC into a complex mixed-signal chip. The noise coupled from digital part will influence the function of sensitive analog circuit, e.g. a ADC.

4.2.1 Coupling noise source

The noise can couple from digital part to analog part through substrate in two manners as shown in Fig 4.5. The first way is that digital block switching noise can be injected into substrate and then coupled into the analog circuit. The second way is that digital circuit switching current causes di/dt noise on the digital power rails. Although the digital part and analog part may have physically separated power rails, the di/dt noise can still couple to the analog power rails through the common substrate. And once the power rails are contaminated with noise, the whole analog circuit will be influenced. Therefore the latter coupling path is often the most critical coupling path.

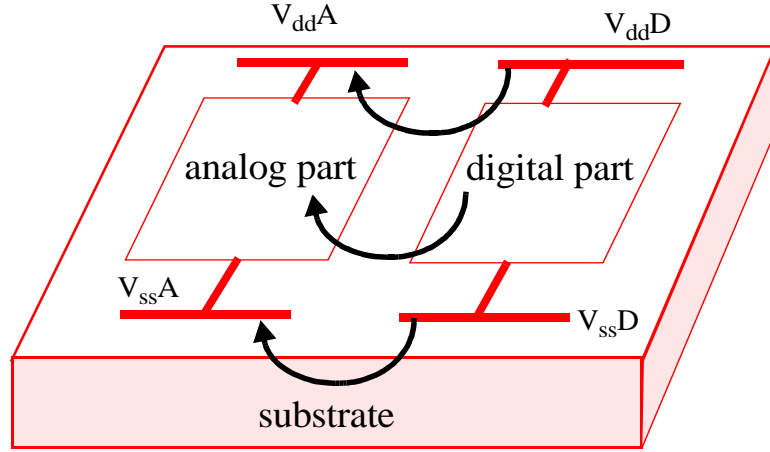


Fig 4.5 Coupling noise path

4.2.2 Substrate model

The substrate coupling is strongly influenced by the layout floorplan, substrate material characteristic and biasing voltages.

Two types of wafer are usually used in semiconductor process: lightly-doped wafer and heavily-doped wafer. The latter kind of wafer is good for avoiding latch-up. The exploration of substrate characteristic can be carried out using device-level simulator like MEDICI. However its capability is limited to small circuits and it takes very long time to do a simulation. In order to find the coupling noise influence on a circuit, the substrate model should be integrated into SPICE-like circuit-level models. Starting from Poisson's equation [Ver93] or from simplified Maxwell's equation [Ver96], the following description of the substrate can be derived:

$$\epsilon \frac{\partial}{\partial t} (\nabla E) + \frac{1}{\rho} \nabla E = 0$$

where E is the electric field intensity vector, ρ and ϵ are the sheet resistivity and dielectric constant of the semiconductor respectively. It is impossible to give a closed-form analytical solution of this substrate description in practice. A practical way is to decompose the whole substrate into a 3-D mesh and use numerical calculation to find a reasonably accurate solution. An element of such a mesh is shown in Fig 4.6:

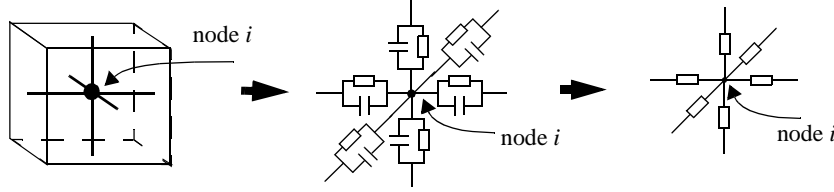


Fig 4.6 Mesh element of substrate model

Each substrate element has six resistor-capacitor pairs connecting to its six neighboring elements. When the system operation speed is under the order of GHz, the capacitors in the model can be neglected without causing much degradation to the modeling accuracy. The equation describing the relation between node i and one of its neighbor j is

$$\sum_j \left[\frac{(v_i - v_j)}{R_{ij}} + C_{ij} \left(\frac{\partial V_i}{\partial t} - \frac{\partial V_j}{\partial t} \right) \right] = 0$$

The density of the mesh network directly determines the substrate modelling accuracy. In practice the available computation capability limits the mesh node number. In [Cle94] a non-uniform density mesh structure is proposed so that the sensitive area would have a higher density. But even this method could only handle relatively small circuits. In particular, consider the case of Sigma Delta converter, thousands of clock cycles need to be simulated to do an accurate FFT analysis. This limits the substrate node number to be in the same order of circuit device number. To solve this problem, a macro model has to be used, where the substrate macro model is extracted only for the sensitive nodes in the analog circuit [Li99a].

4.2.3 Substrate macro model example

For analysis purpose a 5th order single stage 1-bit Sigma Delta modulator has been designed. The loop coefficients are optimized for both performance and stability [Li98a]. This noise shaper consists of multiple switched-capacitor integrators, of which the first integrator is realized with a fully differential OTA as shown in Fig 4.7.

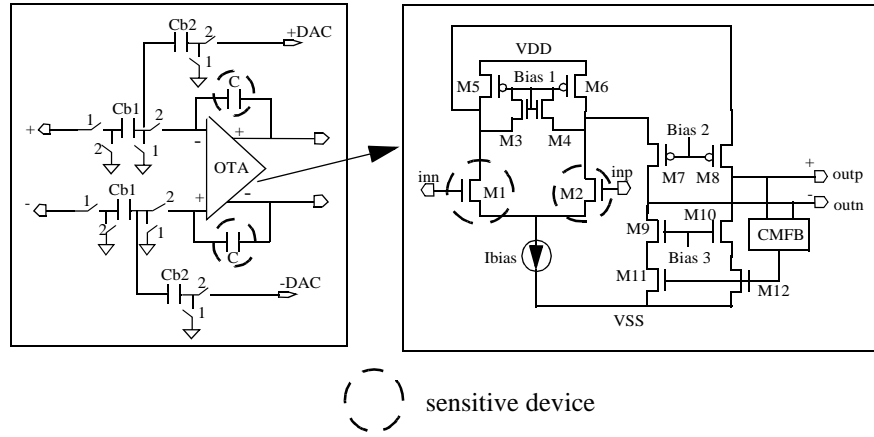


Fig 4.7 Sensitive devices to coupling noise

In this specific example the noise source is a clock line, and the selected sensitive devices are the integrator capacitors and input transistors of the amplifier as shown in Fig 4.7. Fig 4.8 shows the substrate coupling macro models. The substrate has a heavily-doped layer which is modelled as a single node. The parasitic capacitances and resistances connecting the sensitive devices and the noise source are extracted using the Quasi-Static EM analysis method. Note that some resistances and capacitances are not shown in the figure for simplicity.

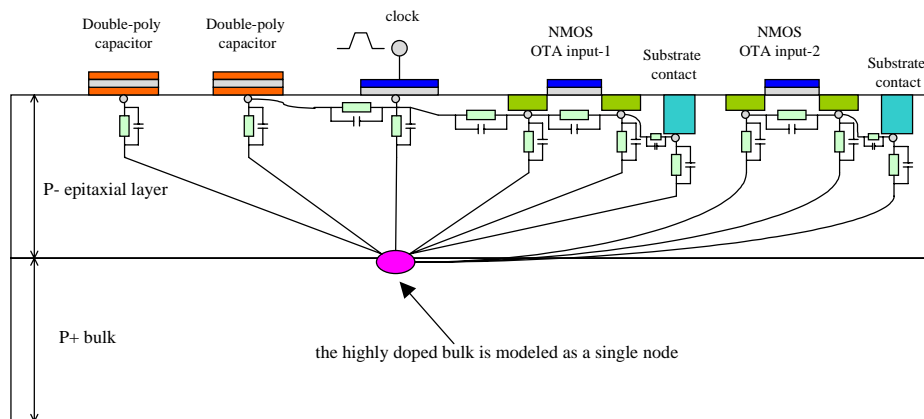


Fig 4.8 Substrate macro model

When the clock switches the voltage level switching will inject noise into the substrate. Through the coupling path generated by those parasitic resistances and capacitances, the noise will appear at the terminals of the sensitive nodes. How large this coupling noise is depends on a lot of factors such as the clock switching voltage levels and edge slope, layout floorplan of noise source and sensitive devices, and the circuit connection of these sensitive devices. These factors are changed to perform comparative simulations. The changed parameters include the clock edge slope, distance between transistors and the clock signal line, and the position of substrate contact. The waveforms of the integrator output nodes are plotted in Fig 4.9. The coupling noise on two differential outputs has a peak voltage of about 70mV. But the differential voltage is only about 20mV. The advantage of differential circuit and symmetrical layout in noise-rejection is obvious. Fig. 4.10 shows five of the simulated cases with different layout floorplan and timing.

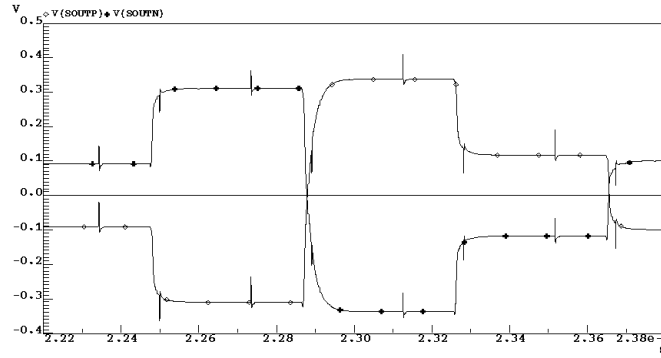
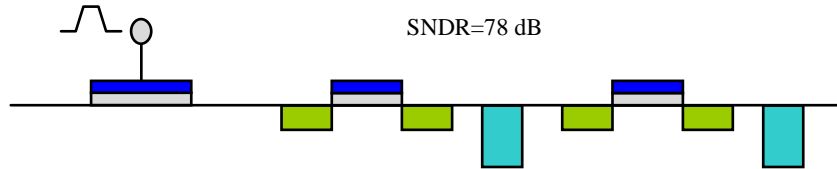
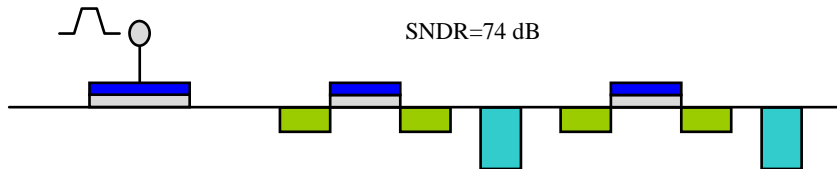


Fig 4.9 Coupling noise on integrator output

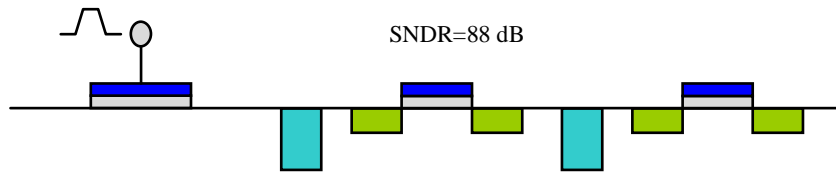
Case 1. The clock is $2\mu\text{m}$ away from the left NMOS. The rising/falling edge is 1ns



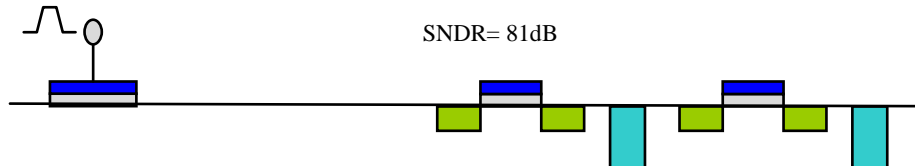
Case 2. The same as case 1, except that the clock edge is set to 0.1ns



Case 3. The same as case 1, except that the substrate contact is shift to the left side (closer to clock)



Case 4. The same as case 1, except that the clock is $12\mu\text{m}$ away from the left transistor



Case 5. The same as case 1, except that the capacitors are also taken into account, which is $5\mu\text{m}$ away from the clock

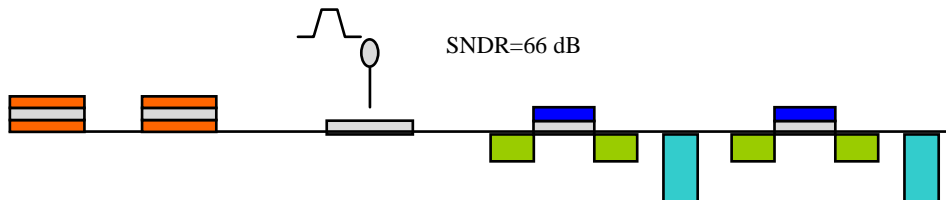


Fig 4.10 Simulated layout floorplan

5 Conclusions

5.1 Thesis summary

Software radio is the target of high-integration wireless transceiver design. In such a transceiver the analog circuit is reduced to a minimum, and most of the filtering and channel selection tasks are performed by digital circuits. Although there is still a long way to go before the realization of a true software radio, many current transceiver designs follow the same idea: shift the signal processing from analog domain to digital domain, so that the receiver is more robust and multi-standard compatible. One of the most critical bottlenecks in such designs is the realization of a high-speed high-resolution analog-to-digital converter.

In this thesis several high-integration wireless receiver structures are introduced. They have a common character: the channel selection is performed by digital filters. In this way the large and off-chip analog filters can be skipped. Chip area as well as power can be saved. At the same time the channel selection can be made programmable and very precise. But now the ADC faces not only the wanted channel but also the un-filtered neighboring channels, which can be larger than the wanted channel. Therefore a high dynamic range is needed for the ADC to recognize and quantize a weak signal with the existence of strong disturbances. Currently the most robust solution to provide such a high dynamic range is to use a Sigma Delta ADC. But Sigma Delta ADC is not naturally suitable for wireless communication because there is a wide signal band to be converted, which can range from hundred of kHz to MHz. A large signal bandwidth means a low oversampling ratio. Under an oversampling ratio below 16, the advantage of high order noise-shaping is not efficiently utilized. The use of multi-bit internal quantizer provides an alternative to achieve sufficiently high resolution even with a low oversampling ratio.

In the thesis the most important quantizer characteristics are explained. Generally speaking in a Sigma Delta ADC the requirement on the quantizer is not critical because its non-idealities will be noise-shaped by the loop filter. The biggest problem in a multi-bit Sigma Delta ADC is its internal DAC non-linearity, which causes large distortions in the signal band. In this work a systematic analysis is provided on the solution of combining a multi-bit internal quantizer and 1-bit internal DAC. It is shown that this solution is best suitable for a second order single-stage modulator, or MASH modulators with their last stage being a first-order loop, considering the influence of signal scaling. Although the achieved resolution might be lower than a conventional multi-bit ADC, the much simpler hardware structure still makes it an attractive choice. In such a structure, the complex multi-bit DAC is replaced by a 1-bit DAC, which is simply a switch. The originally needed dynamic element matching circuit is also skipped, bringing extra simplification. The measured performance of a second order single-stage modulator using 5-bit quantizer and one-bit DAC shows that its resolution

is 18dB higher than a 1-bit modulator.

In the thesis the principle of semi-uniform quantization is presented. Uniform quantizer is almost the exclusive choice in analog-to-digital convertors. In error feedback coders like Sigma Delta modulator, the input to the quantizer exhibits a certain distribution, which has high probability for small inputs and low probability for large inputs. To take the advantage of this distribution, a semi-uniform quantizer has small quantization step for small inputs and large quantization step for large inputs. The overall quantization error power is reduced. Compared with other types of non-uniform quantizers, a semi-uniform quantizer has a much simpler structure. The circuit and layout realization is almost the same as a uniform quantizer except that the threshold voltages are generated by slightly different resistor ladder. Measured performance of a second order modulator with 3-bit semi-uniform quantizer and DAC shows that its dynamic range is 6dB higher than a modulator with uniform quantizer.

Some future design challenges are illustrated in the thesis, including substrate noise coupling problem and ultra low voltage design for future deep submicron processes. As a result, ADC designers are required to have an understanding of e.g. physical design issues and digital circuit design.

5.2 Future work

Low-voltage/low-power is an increasingly important aspect of state-of-the-art VLSI (Very Large Scale Integration) chips. The advance of modern CMOS process leads to continuously decreasing supply voltage. According to the ITRS (International Technology Roadmap for Semiconductors) roadmap, the supply voltage will drop to 0.5V by 2013. Low-power is a common requirement of all VLSI chips, but it becomes critical when the chip works at super-high speed, or when the chip is powered by batteries or even powered wirelessly. Therefore the research of low-voltage/low-power design is of extreme importance for the VLSI development in the future. The research will allow chip designers to take the full advantage of deep-sub-micron process in the next decades, and it will enable VLSI chips to improve and change our daily life tremendously.

The next generation ADCs will be expected to work under lower voltage and power, and to provide higher resolution as well as larger conversion bandwidth. They will be suitable for a vast range of applications like instrument measurement, wireless transceiver, medical care solutions, military applications, and environment monitoring. Ideas that are currently un-realizable will be turned into reality, e.g. micro medical sensors and smart-dusts. A micro medical sensor can be planted into human body and collects required information, which is converted into digital signals and then stored or transmitted. Smart-dusts are tiny wireless sensors. Sprinkling thousands of such tiny sensors on a battlefield can monitor enemy movements without alerting the enemy of

their presence. The development of next generation low-voltage/low-power ADCs requires fundamental research on topics like ultra-low voltage analog circuit topology, leakage current control in low- V_T process, and adaptive power control mechanism.

The future research will focus on ultra-low voltage Sigma Delta ADC using low/zero- V_T process. Switched-Capacitor circuit is the most robust structure to realize a Sigma Delta ADC. However SC circuit faces a severe design challenge when using an ultra-low supply voltage. For example, when the supply voltage is lower than the sum of threshold voltages of PMOS and NMOS transistors, a complementary MOS switch will not function correctly. One solution is to use Switched-Opamp structure, which has its own drawbacks. The circuit speed is low because the Opamp has to be switched off in every clock cycle. Using low/zero- V_T transistors, a complementary MOS switch will function well even with an ultra-low supply voltage, and the Opamp and comparator designs are made easier. But when using a low/zero- V_T process the leakage current is un-negligible, which breaks the charge conservation in a SC circuit. In a Sigma Delta ADC this might cause distortions. The influence of leakage current is to be evaluated in the research. The lowest supply voltage of a Sigma Delta ADC reported so far is 0.7V. With the use of low/zero- V_t process a supply voltage of 0.5V is within the target.

6 Summary of papers

Paper 1.

Multi-bit Sigma Delta modulators suffer from the DAC non-linearity problem and often need complicated Dynamic Element Matching (DEM) circuits. Combining a multi-bit quantizer and a single-bit DAC eliminates the need of DEM circuits, simplifies the design, and reduces the power consumption. In this paper the influence of signal scaling is analyzed and a design example given. A second order 3-bit modulator is fabricated in 0.35 μ m CMOS process, achieving 82dB dynamic range at OSR=128 and a peak SNDR of 73.1dB. Technical background is provided in section 2.2 and 3.5 of this thesis.

Author's contribution: The author came up with the idea, performed all the work of simulation, circuit design, measurements, and wrote the manuscript. The author would like to thank Xing Liu and Roshan Weerasekera for the contribution on part of the layout design work.

Paper 2.

In this paper a new type of nonuniform quantizer, semi-uniform quantizer, is introduced. The use of semi-uniform quantizer achieves about 1-bit higher dynamic range compared with a conventional quantizer, while the hardware complexity of them is the same. The measurement results of a prototype chip in 0.35 μ m CMOS process confirm the simulation results. At 32x oversampling ratio the 2nd order modulator achieves 81dB dynamic range, 63.8dB peak SNDR with a 3-bit semi-uniform quantizer. With a 3-bit uniform quantizer the dynamic range is 70dB and the peak SNDR is 54.1dB. Technical background is provided in section 3.4 of this thesis.

Author's contribution: The author came up with the idea, performed all the work of simulation, circuit design, measurements, and wrote the manuscript. The author would like to thank Xing Liu and Roshan Weerasekera for the contribution on part of the layout design work.

Paper 3.

A new structure of cascading multi-bit Sigma Delta modulators is proposed in this paper. Using a multi-bit quantizer in each stage, the modulator's performance is largely improved. Furthermore this structure does not require any dynamic element matching or digital correction circuit to attenuate the non-linearity error. This is because the modulator's first stage uses a multi-bit quantizer, but only the most significant bit is used to generate the feedback. By this way the non-linearity error is eliminated. Simulation results are demonstrated with circuit non-idealities considered. Technical back-

ground is provided in section 3.5 of this thesis.

Author's contribution: The author came up with the idea, performed all the work of analysis, simulation, and wrote the manuscript.

Paper 4.

A semi-uniform quantizer for multi-bit Sigma Delta modulator is proposed. It has smaller quantization steps for smaller inputs and vice versa. The use of a k -bit semi-uniform quantizer achieves roughly the same performance as using a $(k+1)$ -bit uniform quantizer over main part of the input signal amplitude range. The semi-uniform quantizer can easily be constructed in the same way as constructing a uniform quantizer. Technical background is provided in section 3.4 of this thesis.

Author's contribution: The author came up with the idea, performed all the work of analysis, simulation, and wrote the manuscript.

Paper 5.

This paper presents an improved settling model of switched-capacitor integrator. It takes into account the impact of MOS switches' conducting resistance, which influences both the final settling error and the settling curve shape at the initial phase. The State-Space method is used to describe the model and implemented with a MATLAB block for high level simulations of sigma-delta modulators. The simulation result of the proposed model is compared with that obtained from the SPICE simulation. The final settling error is within 0.02%. Such a settling model was used to do fast and accurate simulation for all the chips that was measured and reported in this thesis.

Author's contribution: The author came up with the idea, performed all the work of analysis, simulation, and wrote the manuscript. The author would like to thank Lirong Zheng for the discussion on simulation methods.

Paper 6.

An operational amplifier designed with 0.35 μ m CMOS technology is presented. All the transistors are realized with minimum or near-minimum channel length. The op amp is designed to meet the requirement of a high-speed high-resolution Sigma Delta modulator. It has a folded-cascode first stage and a class-A output stage. It features a DC gain of 78dB, an open-loop unity-gain frequency of 266MHz, a slew rate of 650V/ μ s, and consumes 10.2mW from a ± 1.5 V power supply. This design procedure is applied to all the OTAs in the chips that are reported in the thesis.

Author's contribution: The author came up with the idea, performed all the work of analysis, simulation, and wrote the manuscript.

Paper 7

The invention relates to a Sigma Delta modulator, which is operative in different standard modes for processing signals of different communication standards. The modulator comprises a 1-bit quantizer and a multi-bit quantizer, and a switching mechanism for switching between said quantizer independence of the standard mode. The invention further relates to an A/D convertor comprising such a modulator, a multi standard RF receiver comprising such an A/D convertor, and a method for signal processing of communication signals of different communication standards. Technical background is provided in section 3.2 and 3.3 of this thesis.

Author's contribution: The author is one of the main contributors to the invention. The author took part in all the procedures of invention development and patent manuscript drafting.

Paper 8.

In a multi-bit Sigma Delta modulator the internal DAC non-linearity problem can be solved by combining a multi-bit quantizer and 1-bit DAC. In this paper a circuit optimization theme is provided for such structures. The internal signal scaling is carried out considering both the stability and resolution requirements. A second order Sigma Delta modulator using 5-bit internal quantizer and 1-bit internal DAC is designed and fabricated in 0.35 μ m CMOS process. At 32MHz sampling frequency and 16x oversampling ratio, the modulator achieves 66.4dB dynamic range and 59.3dB SNDR over a 2MHz Nyquist bandwidth, and the chip consumes 45.5mW power. Technical background is provided in section 2.2 and 3.5 of this thesis.

Author's contribution: The author came up with the idea, performed all the work of simulation, circuit design, measurements, and wrote the manuscript.

7 References

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