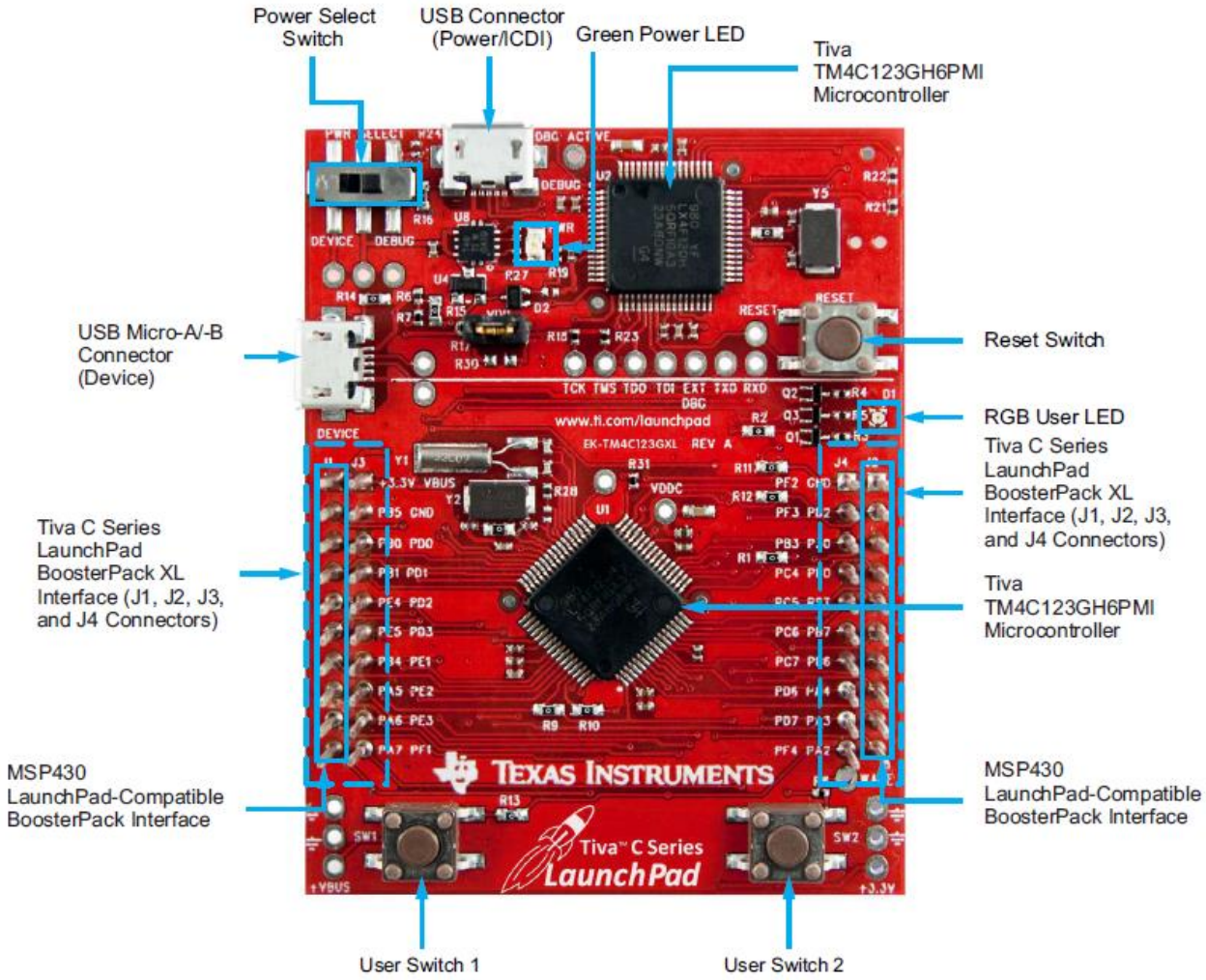
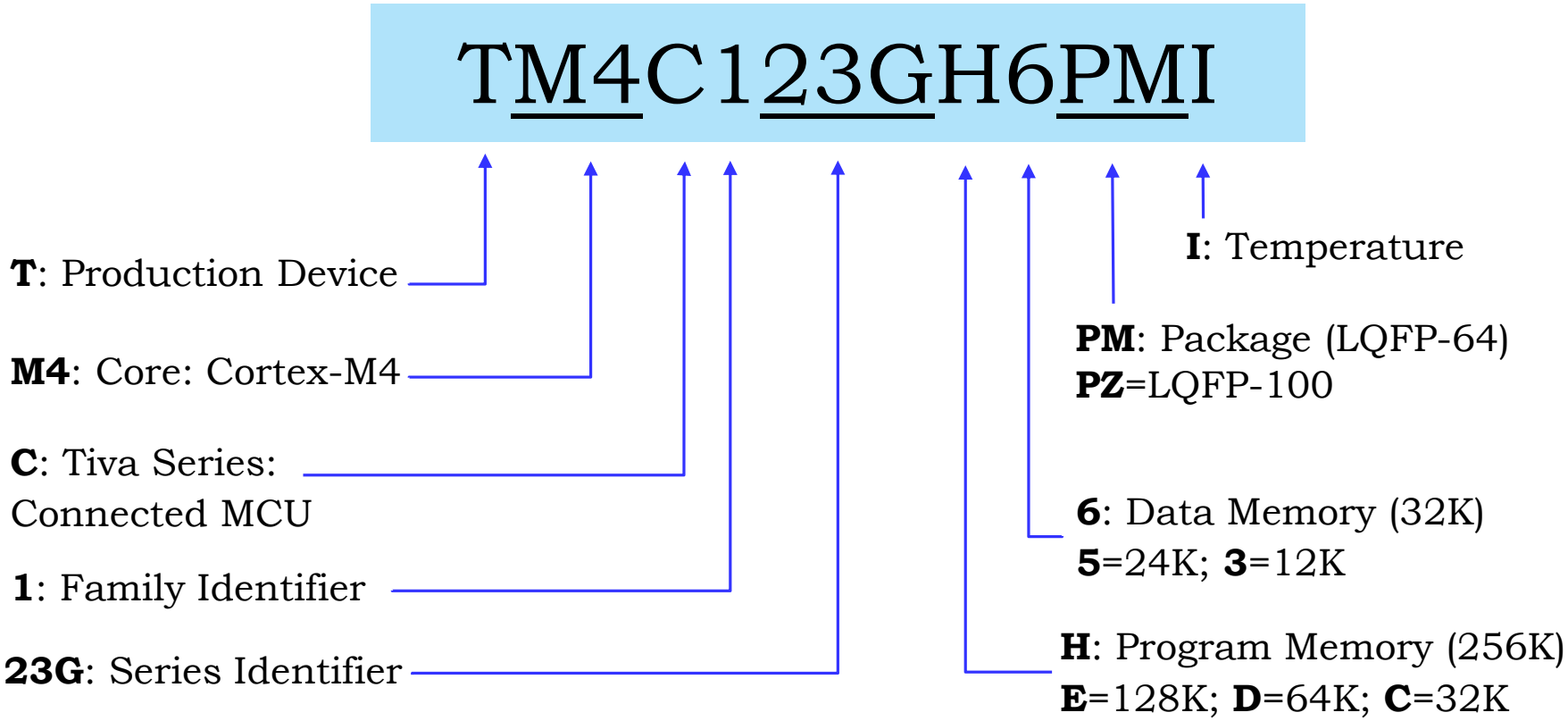
TI Tiva LaunchPad

Tiva C Series TM4C123G

Tiva C Series TMC123G (LaunchPad)

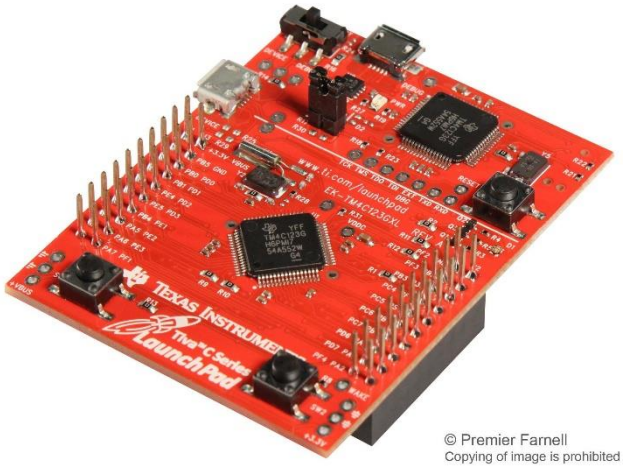


Tiva C Series TMC123G



Tiva LaunchPad

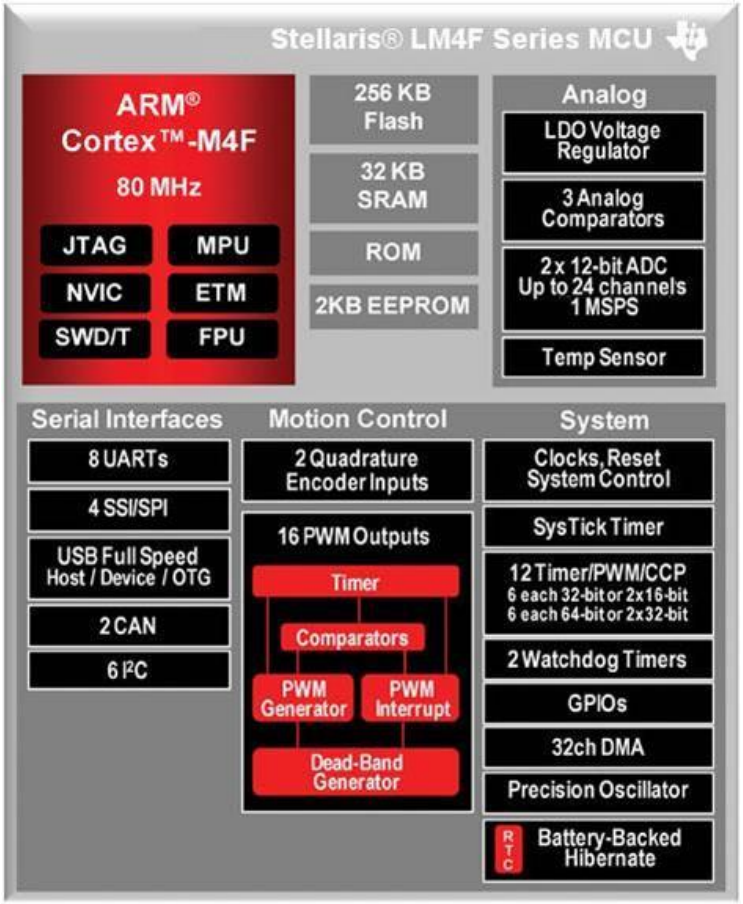
- **ARM Cortex M4F** Processor, 64-pin, **80MHz** Texas Instrument TM4C123GH6PM.
- **On-board programming & debug through USB port** - ICDI (In-Circuit Debug Interface)
- USB device port – switchable through device/ICDI switch.
- **2 user push buttons**, SW1 & SW2 (SW2 connected to WAKE pin).



- Reset button.
- 3 user LEDs (implemented as 1 **tri-color LED**).
- Current measurement test-points.
- **16MHz main oscillator crystal**.
- 32KHz RTC crystal.
- Power selection through switch – either through ICDI or USB device.
- On-board 3.3V regulator.

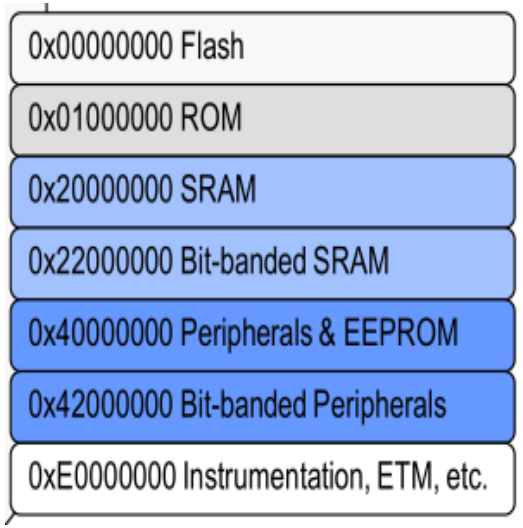
Tiva TM4C123G: MCU Core & FPU

- **32-bit ARM Cortex M4F** based.
- Programmable up to **80MHz** clock speed.
- Low power consumption – as low as 370uA/MHz.
- **Flexible clocking system**:
  - Internal precision clock
  - External oscillator with PLL support.
  - Internal low-frequency oscillator.
  - RTC support.
- Read-Modify-Write using bit-banding (to access single-bits in memory).
- **FPU**: single-cycle multiply & hardware divider.



TM4C123GH6P: Memory

- **Flash Memory** (0x0000.0000)
  - 256K bytes
  - Single cycle reads of up to 40MHz clock.
  - Organized as 1K byte blocks that can be individually erased.
  - Blocks can be marked as read-only or execute only (different levels of protection).
  - Pre-fetch buffer & speculative branching for performance improvement.
- Internal ROM (0x0100.0000) loaded with TivaWare software
  - Bootloader, Peripheral driver library.
- SRAM 32K bytes (0x2000.000) with bit-banding *(for efficient bit access)*.
- EEPROM (0x4000.0000)
  - 2K bytes (32 blocks of 16-word blocks).
  - Each block is individually protectable.



TM4C123GH6PM: Peripherals

- **General Purpose Input-Output** (GPIO)
  - Up to **43 GPIO**s.
  - Any GPIO can be **external edge or level triggered** interrupt source.
  - GPIO can initiate an ADC sample sequence or µDMA transfer .
  - **Toggle rate up to CPU clock speed on the AHB bus**.
  - 5V-tolerant inputs (except for PD0, PB1 and USB data pins when configured as GPIOs).
  - Programmable drive strengths (**2, 4, 8 mA or 8mA** with slew rate control)
  - **Programmable weak pull-up, pull-down** and tri-state.

TM4C123GH6P: Peripherals

- **Timers**
  - 2 watchdog timers with separate clocks
  - **24-bit SysTick timer**.
  - **6 32-bit & 6 64-bit general purpose timers.**
  - CCP (Capture-Compare-PWM) & PWM modules.
  - Support for daisy-chaining of timers.
- Memory Protection Unit (MPU)
  - Generates a Memory Management Fault on incorrect access to memory regions.
- Direct Memory Access controller (called µDMA)
  - Up to 32 channels
  - Supports memory-to-memory, memory-to-peripheral & peripheral-to-memory transfers in various modes:
    - Basic (simple data transfers), Ping-pong (continuous data transfer) & scatter-gather modes (up to 256 arbitrary transfers).
  - Support for 8, 16 and 32-bit data sizes.
  - Interrupt enabled.

TM4C123GH6P: Peripherals

- **Nested Vectored Interrupt Controller** (NVIC)
  - 7 exceptions
  - 71 interrupts with **8 programmable priorities**.
  - Tail-chaining and other low-latency features.
  - Deterministic - always 12 cycles or 6 with tail-chaining.
  - Automatic system save and restore.
- Motion Control Modules (x2)
  - 8 high-resolution PWM outputs (4 pairs).
  - H-bridges dead-band generators and hardware polarity control.
  - Quadrature encoder inputs (QEI).
  - Inter-module synchronization.

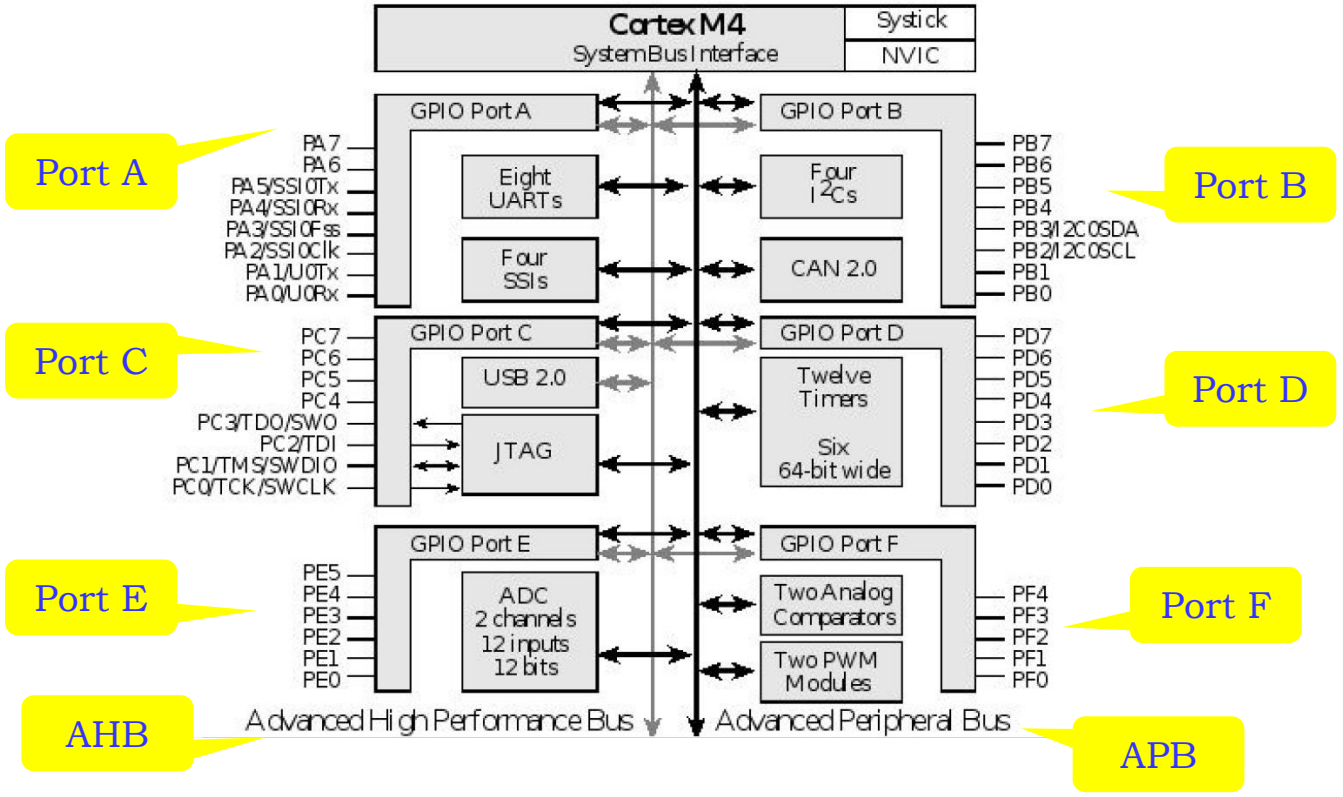
TM4C123GH6P: Peripherals

- **Analog-to-Digital Convertors** (ADC)
  - **2 12-bit ADCs, up to 1M bps sampling rate.**
  - **12 shared inputs**
  - Single ended & differential measurements.
  - Internal temperature sensor.
  - **4 programmable sample sequencers.**
  - **Flexible trigger controls: SW, timers, GPIO, ..**
  - VDDA/GNDA voltage reference.
  - 3 analog & 16 digital comparators
  - µDMA enabled.

TM4C123GH6P: Peripherals

- Serial Connectivity:
  - USB 2.0 support for OTG, Host, Device modes.
  - 8 UART.
  - 6 I^2C interfaces.
  - 4 SPI, Microwire or TI synchronous serial interfaces.
  - 2 CAN bus interfaces.

Tiva LaunchPad Block Diagram



- TM4C123 has 2 on-chip buses from CPU core to the peripherals:
  - **Advanced Peripheral Bus (APB)**
  - **Advanced High-Performance Bus (AHB)**
- GPIO ports can be programmed to be connected to the APB or AHB,

Multiple Buses – APB, AHB

- GPIO pins can be connected to either the **APB** & **AHB** buses.
  - APB: (legacy bus)
    - Port pin can change/toggle every 2 clock cycles.
  - AHB:
    - Port pin can change every clock cycle.

- How do we select a GPIO port to be connected to either APB or AHB bus?
  - Through one of the system control registers … *see next slide.*

GPIO High-Performance Bus Control (GPIOHBCTL)

GPIO High-Performance Bus Control (GPIOHBCTL)

Base 0x400F.E000
Offset 0x06C
Type RW, reset 0x0000.7E00

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved										PORTF	PORTE	PORTD	PORTC	PORTB	PORTA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PORTA	RW	0	Port A Advanced High-Performance Bus This bit defines the memory aperture for Port A. Value Description 0 Advanced Peripheral Bus (APB). This bus is the legacy bus. 1 Advanced High-Performance Bus (AHB)

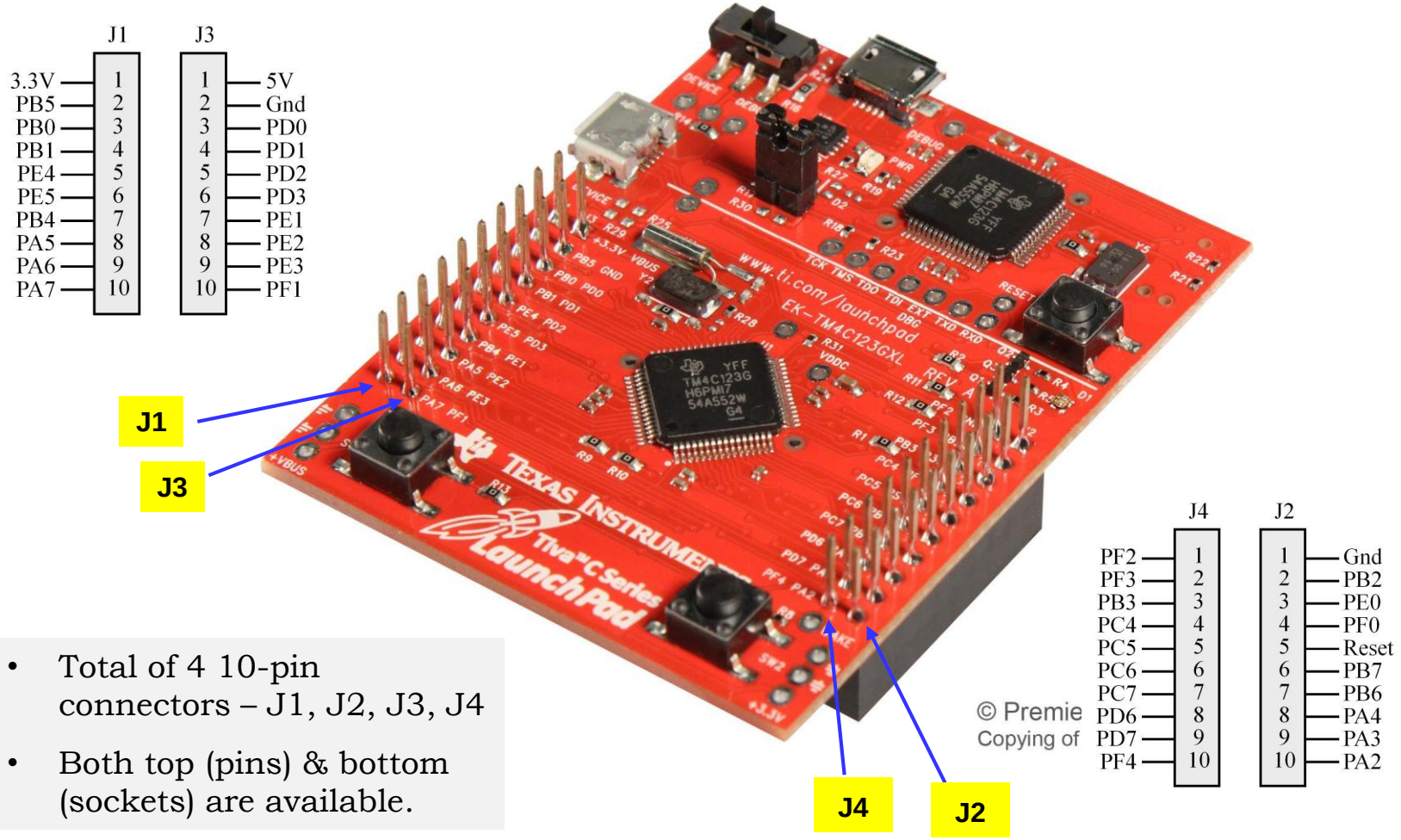
default

Source: TM4C123GH6PM7 Datasheet, pg 258 (spmu376e.pdf)

LaunchPad Pins

- Total of **43** GPIO pins on CPU chip
- **35** GPIO pins are available for use on Tiva LaunchPad.
- All pins can be GPIOs.
  - PA[7:0] – 8 pins
    - PA0 & PA1 used for Virtual COM port (not brought out on LaunchPad).
  - PB[7:0] – 8 pins
  - PC[7:0] – 8 pins
    - PC[3:0] used for JTAG debug (not brought out on LaunchPad).
  - PD[7:0] – 8 pins
    - PD[5:4] used for USB signals (not brought out on LaunchPad).
  - PE[5:0] – 6 pins
  - PF[4:0] – 5 pins

Tiva LaunchPad



- Total of 4 10-pin connectors – J1, J2, J3, J4
- Both top (pins) & bottom (sockets) are available.

GPIO Pins

- GPIO pins can function as a **digital** pin, re-mapped to an **alternate function**, or as an **analog** pin.
- Alternate Function:
  - Pins can be assigned to as many as 8 different I/O functions.
  - Many of the pins can be configured for more than one function – alternate functions
  - Alternate functions include:
    - digital I/O
    - analog input
    - timer I/O
    - serial I/O
    - and so on ….

LaunchPad GPIO Pins Functions

- **Analog Function:**
  - GPIO pins can have a configuration bit in the **GPIOAMSEL** (GPIO Analog Mode Select) register.
  - Purpose is to connect port pin to the ADC or analog comparator.
- **Digital Function:**
  - Each pin has **4 bits** in the **GPIOPCTL** (GPIO Port control) register to specify the alternate function for the pin.
  - Note: 0 means regular I/O function.
  - Not every pin can be connected to alternate functions.
- Most alternate functions exist on only one pin (e.g. UORx on PA0).
- But there are some that can be mapped to two or more pins (e.g CAN0Rx mapped to PB4, PE4 or PF0).

Port pins PC0 to PC3 are used for JTAG debugger. Cannot be used for regular I/O functions. *(see slide 23)*

LaunchPad Pins Functions

Analog Function

GPIOCTL reg bits (4 bits) – selects GPIO function

GPIO Port pin on LaunchPad

IO	Ain	0	1	2	3	4	5	6	7	8	9	14
PA0		*Port*	*U0Rx*							*CAN1Rx*		
PA1		*Port*	*U0Tx*							*CAN1Tx*		
PA2		Port		SSI0Clk								
PA3		Port		SSI0Fss								
PA4		Port		SSI0Rx								
PA5		Port		SSI0Tx								
PA6		Port			I_2C1SCL		M1PWM2					
PA7		Port			I_2C1SDA		M1PWM3					
PB0	*USB0ID*	*Port*	*U1Rx*						*T2CCP0*			
PB1	*USB0VBUS*	*Port*	*U1Tx*						*T2CCP1*			
PB2		Port			I_2C0SCL				T3CCP0			
PB3		Port			I_2C0SDA				T3CCP1			
PB4	Ain10	Port		SSI2Clk		M0PWM2			T1CCP0	CAN0Rx		
PB5	Ain11	Port		SSI2Fss		M0PWM3			T1CCP1	CAN0Tx		
PB6		Port		SSI2Rx		M0PWM0			T0CCP0			
PB7		Port		SSI2Tx		M0PWM1			T0CCP1			
PC4	C1-	Port	U4Rx	U1Rx		M0PWM6		IDX1	WT0CCP0	U1RTS		
PC5	C1+	Port	U4Tx	U1Tx		M0PWM7		PhA1	WT0CCP1	U1CTS		
PC6	C0+	Port	U3Rx					PhB1	WT1CCP0	USB0epen		
PC7	C0-	Port	U3Tx						WT1CCP1	USB0pflt		

Example:

- To select CAN1Rx as the alternate function for GPIO port pin PA0, we write 8 to the GPIO CTL register bits (PMC0) for Port A.
- If GPIOCTL bits is set to 0, it select the GPIO pin as a digital I/O pin (default).

Source: TM4C123GH6PM7 Datasheet, pg 651 (spmu376e.pdf)

LaunchPad Pins Functions

Analog Function

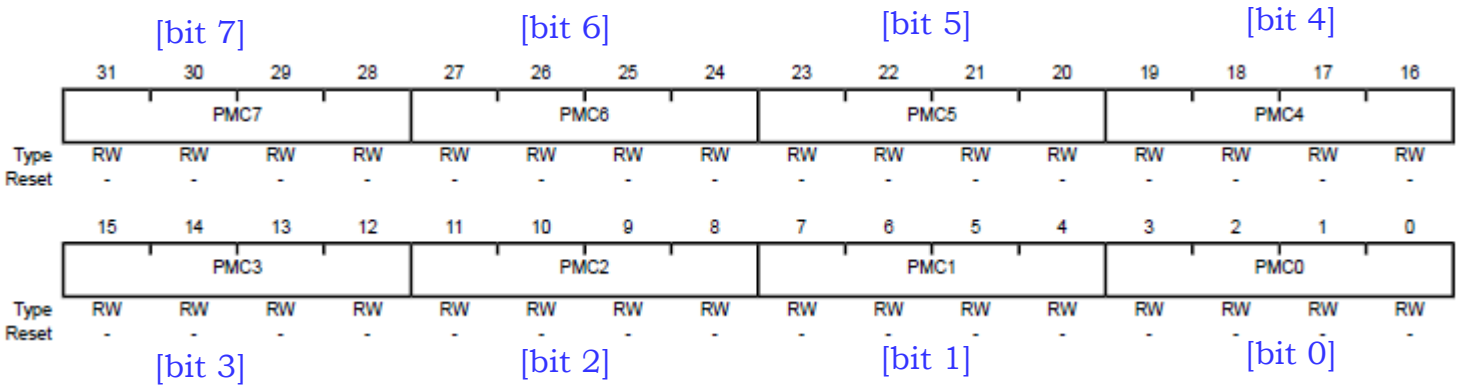
GPIOCTL reg bits (4 bits)L selects GPIO function

GPIO Port pin on LaunchPad

IO	Ain	0	1	2	3	4	5	6	7	8	9	14
PD0	Ain7	Port	SSI3Clk	SSI1Clk	I_2C3SCL	M0PWM6	M1PWM0		WT2CCP0			
PD1	Ain6	Port	SSI3Fss	SSI1Fss	I_2C3SDA	M0PWM7	M1PWM1		WT2CCP1			
PD2	Ain5	Port	SSI3Rx	SSI1Rx		M0Fault0			WT3CCP0	USB0epen		
PD3	Ain4	Port	SSI3Tx	SSI1Tx				IDX0	WT3CCP1	USB0pflt		
PD4	*USB0DM*	*Port*	*U6Rx*						*WT4CCP0*			
PD5	*USB0DP*	*Port*	*U6Tx*						*WT4CCP1*			
PD6		Port	U2Rx			M0Fault0		PhA0	WT5CCP0			
PD7		Port	U2Tx					PhB0	WT5CCP1	NMI		
PE0	Ain3	Port	U7Rx									
PE1	Ain2	Port	U7Tx									
PE2	Ain1	Port										
PE3	Ain0	Port										
PE4	Ain9	Port	U5Rx		I_2C2SCL	M0PWM4	M1PWM2			CAN0Rx		
PE5	Ain8	Port	U5Tx		I_2C2SDA	M0PWM5	M1PWM3			CAN0Tx		
PF0		Port	U1RTS	SSI1Rx	CAN0Rx		M1PWM4	PhA0	T0CCP0	NMI	C0o	
PF1		Port	U1CTS	SSI1Tx			M1PWM5	PhB0	T0CCP1		C1o	TRD1
PF2		Port		SSI1Clk		M0Fault0	M1PWM6		T1CCP0			TRD0
PF3		Port		SSI1Fss	CAN0Tx		M1PWM7		T1CCP1			TRCLK
PF4		Port					M1Fault0	IDX0	T2CCP0	USB0epen		

Source: TM4C123GH6PM7 Datasheet, pg 651 (spmu376e.pdf)

GPIO Port Control Register (GPIOPCTL)



- Port Control Register is used together with the GPIOAFSEL register to select the specific peripheral assigned for each GPIO.
- GPIOPCTL selects one of the set of peripheral functions assigned to the GPIO pin.
  - PMC7 = Port Mux control for GPIO pin 7.
  - PMC6 = Port Mux control for GPIO pin 6.
  - PMC5 = Port Mux control for GPIO pin 5.
  - PMC4 = Port Mux control for GPIO pin 4.
  - PMC3 = Port Mux control for GPIO pin 3.
  - PMC2 = Port Mux control for GPIO pin 2.
  - PMC1 = Port Mux control for GPIO pin 1.
  - PMC0 = Port Mux control for GPIO pin 0.

Source: Tiva TM4C123GH6PM Microcontroller Data Sheet (spmu376e.pdf, p689)

User Switches & LED

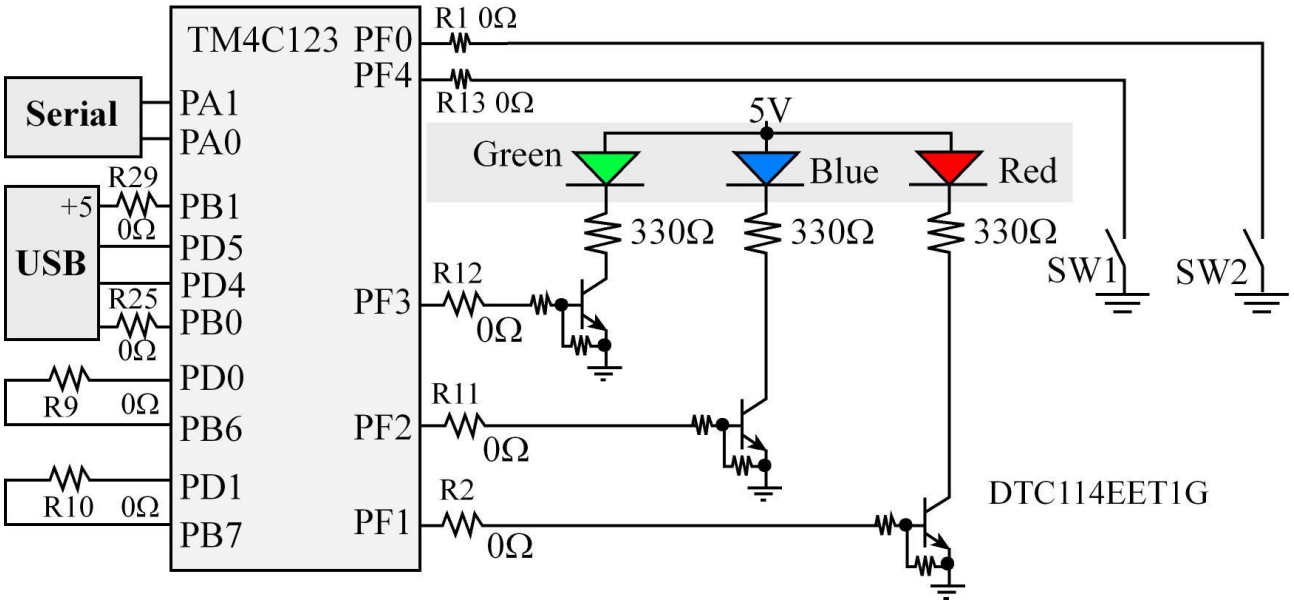
- 2 on-board switches:
  - SW1 to **PF4**, SW2 to **PF0**
  - Logic L when switch pressed.
  - Requires internal pull-up configuration (through the PUR register.
- Port pins PF1, PF2 & PF3 controls a single colour LED.
  - PF1 – red; PF2 – blue; PF3 - green

Table 2-2. User Switches and RGB LED Signals

GPIO Pin	Pin Function	USB Device
PF4	GPIO	SW1
PF0	GPIO	SW2
PF1	GPIO	RGB LED (Red)
PF2	GPIO	RGB LED (Blue)
PF3	GPIO	RGD LED (Green)

Source: Tiva C Series TM4C123G LaunchPad Evaluation Board – User Guide (spmu296.pdf)

Tiva LaunchPad



The following 0Ω resistor can be used to configure the LauchPad:

- R1, R13 connect PF0, PF4 to SW2,SW1
- R2, R11, R12 connects PF1, PF2, PF3 to the 3-color LED
- R25, R29 connect PB1, PB0 to the USB.
  - R25, R29 is not populated when shipped which leaves PB1 & PB0 available to use as GPIOs.

ICDI Debug

GPIO Pin	Pin Function
PC0	TCK/SWCLK
PC1	TMS/SWDIO
PC2	TDI
PC3	TDO/SWO

- On-board program debugging through Integrated In-Circuit Debug Interface (ICDI)
- Only JTAG debugging is supported.
- External debug interface can be connected for Serial Wire Debug (SWD) and SWO (trace).

J1 Connector

J1 Pin	GPIO	Analog Function	On-board Function	Tiva C Series MCU Pin	GPIOPCTL Register Setting										
		GPIO AMSEL			1	2	3	4	5	6	7	8	9	14	15
1.01	3.3 V														
1.02	PB5	AIN11	–	57	–	SSI2Fss	–	M0PWM3	–	–	T1CCP1	CAN0Tx	–	–	–
1.03	PB0	USB0ID	–	45	U1Rx	–	–	–	–	–	T2CCP0	–	–	–	–
1.04	PB1	USB0VBUS	–	46	U1Tx	–	–	–	–	–	T2CCP1	–	–	–	–
1.05	PE4	AIN9	–	59	U5Rx	–	I2C2SCL	M0PWM4	M1PWM2	–	–	CAN0Rx	–	–	–
1.06	PE5	AIN8	–	60	U5Tx	–	I2C2SDA	M0PWM5	M1PWM3	–	–	CAN0Tx	–	–	–
1.07	PB4	AIN10	–	58	–	SSI2Clk	–	M0PWM2	–	–	T1CCP0	CAN0Rx	–	–	–
1.08	PA5	–	–	22	–	SSI0Tx	–	–	–	–	–	–	–	–	–
1.09	PA6	–	–	23	–	–	I2C1SCL	–	M1PWM2	–	–	–	–	–	–
1.10	PA7	–	–	24	–	–	I2C1SDA	–	M1PWM3	–	–	–	–	–	–

(1) Shaded cells indicate configuration for compatibility with the MSP430 LaunchPad.

Source: Tiva C Series TM4C123G LaunchPad Evaluation Board – User Guide (spmu296.pdf)

J3 Connector

J3 Pin	GPIO	Analog Function / GPIO AMSEL	On-board Function	Tiva C Series MCU Pin	GPIOPCTL Register Setting										
					1	2	3	4	5	6	7	8	9	14	15
3.01	5.0 V														
3.02	GND														
3.03	PD0	AIN7	–	61	SSI3Clk	SSI1Clk	I2C3SCL	M0PWM6	M1PWM0	–	WT2CCP0	–	–	–	–
	PB6	–	Connected for MSP430 Compatibility (R9)	1	–	SSI2Rx	–	M0PWM0		–	T0CCP0	–	–	–	–
3.04	PD1	AIN6	–	92	SSI3Fss	SSI1Fss	I2C3SDA	M0PWM7	M1PWM1	–	WT2CCP1	–	–	–	–
	PB7	–	Connected for MSP430 Compatibility (R10)	4	–	SSI2Tx	–	M0PWM1	–	–	T0CCP1	–	–	–	–
3.05	PD2	AIN5		63	SSI3Rx	SSI1Rx	–	M0FAULT0	–	–	WT3CCP0	USB0EPEN			
3.06	PD3	AIN4	–	64	SSI3Tx	SSI1Tx	–	–	–	–	WT3CCP1	USB0PFLT	–	–	–
3.07	PE1	AIN2	–	8	U7Tx	–	–	–	–	–		–	–	–	–
3.08	PE2	AIN1	–	7	–	–	–	–	–	–	–	–	–	–	–
3.09	PE3	AIN0	–	6	–	–	–	–	–	–	–	–	–	–	–
3.10	PF1	–	–	29	U1CTS	SSI1Tx	–	–	M1PWM5	–	T0CCP1	–	C1o	TRD1	–

(1) Shaded cells indicate configuration for compatibility with the MSP430 LaunchPad.

Source: Tiva C Series TM4C123G LaunchPad Evaluation Board – User Guide (spmu296.pdf)

J4 Connector

J4 Pin	GPIO	Analog Function	On-board Function	Tiva C Series MCU Pin	GPIOPCTL Register Setting										
		GPIO AMSEL			1	2	3	4	5	6	7	8	9	14	15
4.01	PF2	–	Blue LED (R11)	30	–	SSI1Clk	–	M0FAULT0	M1PWM6	–	T1CCP0	–	–	–	TRD0
4.02	PF3	–	Green LED (R12)	31	–	SSI1Fss	CAN0Tx	–	M1PWM7	–	T1CCP1	–	–	–	TRCLK
4.03	PB3	–	–	48	–	–	I2C0SDA	–	–	–	T3CCP1	–	–	–	–
4.04	PC4	C1–	–	16	U4Rx	U1Rx	–	M0PWM6	–	IDX1	WT0CCP0	U1RTS	–	–	–
4.05	PC5	C1+	–	15	U4Tx	U1Tx	–	M0PWM7	–	PhA1	WT0CCP1	U1CTS	–	–	–
4.06	PC6	C0+	–	14	U3Rx	–	–	–	–	PhB1	WT1CCP0	USB0EPEN	–	–	–
4.07	PC7	C0–	–	13	U3Tx	–	–	–	–	–	WT1CCP1	USB0PFLT	–	–	–
4.08	PD6	–	–	53	U2Rx	–	–	–	–	PhA0	WT5CCP0	–	–	–	–
4.09	PD7	–	–	10	U2Tx	–	–	–	–	PhB0	WT5CCP1	NMI	–	–	–
4.10	PF4	–	USR_SW 1 (R13)	5	–	–	–	–	M1FAULT0	IDX0	T2CCP0	USB0EPEN	–	–	–

Source: Tiva C Series TM4C123G LaunchPad Evaluation Board – User Guide (spmu296.pdf)

J2 Connector

J2 Pin	GPIO	Analog Function / GPIO AMSEL	On-board Function	Tiva C Series MCU Pin	GPIOPCTL Register Setting										
					1	2	3	4	5	6	7	8	9	14	15
2.01	GND														
2.02	PB2	–	–	47	–	–	I2C0SCL	–	–	–	T3CCP0	–	–	–	–
2.03	PE0	AIN3	–	9	U7Rx	–	–	–	–	–	–	–	–	–	–
2.04	PF0	–	USR_SW2/ WAKE (R1)	28	U1RTS	SSI1Rx	CAN0Rx	–	M1PWM4	PhA0	T0CCP0	NMI	C0o	–	–
2.05	RESET														
2.06	PB7	–	–	4	–	SSI2Tx	–	M0PWM1	–	–	T0CCP1	–	–	–	–
	PD1	AIN6	Connected for MSP430 Compatibility (R10)	62	SSI3Fss	SSI1Fss	I2C3SDA	M0PWM7	M1PWM1	–	WT2CCP1	–	–	–	–
2.07	PB6	–	–	1	–	SSI2Rx	–	M0PWM0	–	–	T0CCP0	–	–	–	–
	PD0	AIN7	Connected for MSP430 Compatibility (R9)	61	SSI3Clk	SSI1Clk	I2C3SCL	M0PWM6	M1PWM0	–	WT2CCP0	–	–	–	–
2.08	PA4	–	–	21	–	SSI0Rx	–	–	–	–	–	–	–	–	–
2.09	PA3	–	–	20	–	SSI0Fss	–	–	–	–	–	–	–	–	–
2.10	PA2	–	–	19	–	SSI0Clk	–	–	–	–	–	–	–	–	–

(1) Shaded cells indicate configuration for compatibility with the MSP430 LaunchPad.

Source: Tiva C Series TM4C123G LaunchPad Evaluation Board – User Guide (spmu296.pdf)