Review Questions: PLL

Week 3

Review Questions - PLL

1. Which are the 2 clock sources that can be used to drive the PLL on the LaunchPad?
   - Main oscillator (MOSC) & Precision Internal Oscillator (PIOSC).

2. What function does the PLLSTAT register serve?
   1. PLLSTAT register is a 32-bit RO register. Only one bit – LOCK bit – is used. It gives indication if the PLL has been locked.

3. What do we mean when we say a 'PLL has locked' ?
   - It means thee PLL has reached it's final intended steady output clock frequency.

4. If DIV400 bit in RCC2 is '1', what is the maximum system division possible? Show how you get the number. What is the resultant processor clock speed?
   - Maximum division = 2^7 = 128.
   - 400MHz/128 = 3.125 MHz.

Review Questions - PLL

5. What is the USERCC2 bit in RCC2 register used for?
   - The USERCC2 bit needs to be set in order to use the RCC2 register.
6. I would like to set a bus speed of 25MHz, what is the system clock divisor value to use in RCC2? Assume DIV400 = '1'. Write the C code line to set the bus speed.
   - Divisor = 400MHz / 25 MHz = 16.
   - C code:

```
SYSCTL->RCC2 |= 1UL << 30; // set DIV400=1 (use 400MHz VCO clock)
SYSCTL->RCC2 |= (15U<<22); // set divisor (7 bits)
```

7. I would like to set a bus speed of 20MHz, what is the system clock divisor value to use in RCC2? Assume DIV400 = '0'. Write the C code line to set the bus speed.
   - Divisor = 200MHz / 20 MHz = 10.
   - C code:

```
SYSCTL->RCC2 &= ~ (1UL << 30); // reset DIV400 (use 200MHz VCO clock)
SYSCTL->RCC2 |= (9U<<23);      // set divisor ( 6 bits)
```