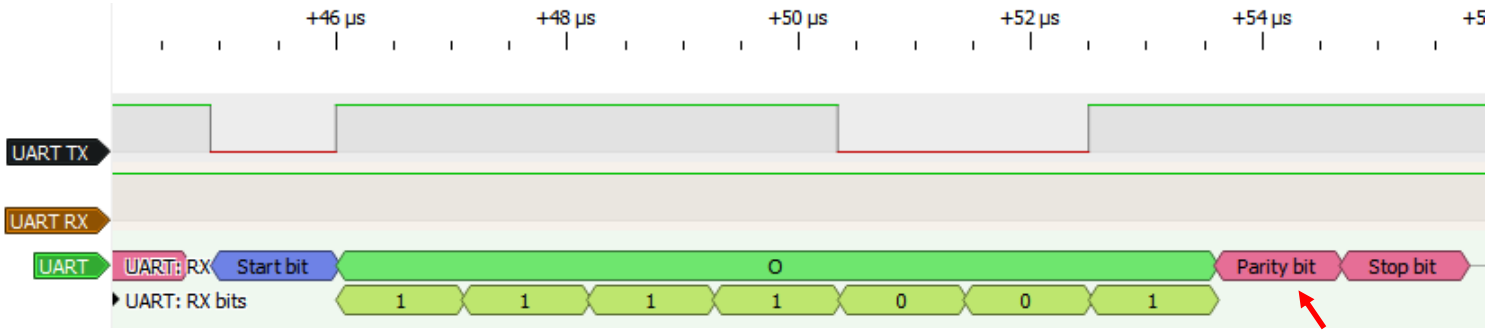
Review Questions: Serial Protocols - UART

UART

1. Explain what you understand by **half duplex** and **full duplex** serial communications.
   - In **half duplex** communication, both sender & receiver can be active but NOT at the same time. Only one party can send at any one time. E.g. I^2C.
   - In **full-duplex** communication, both sender & receiver can be active at the same time. Both sender and receiver can send at the same time. E.g. SPI.

2. Explain how parity works during UART communications.
   - Parity is sent as an extra bit during UART communications. and used as a form of error detection.
   - Odd parity: data bits plus parity bit has odd number of 1's.
   - Even parity: data bits plus parity bit has even number of 1's.
   - *See illustration in next slide …*

UART



EVEN parity: parity bit inserted so that total '1's is EVEN.

3. How many UARTs are implemented on the Tiva LaunchPad? Name them.
   - 8 possible UARTs on TM4C123G (UART0 to UART7).
   - All UART pins are multiplexed with GPO pins.
4. What advantage(s) does a FIFO offer in UART communications?
   - FIFO reduces program (SW) overhead & response time requirements of the operating system to service the UART port hardware.
     - During transmit, SW is able to write to fill up the FIFO before or while the data is being transmitted.
     - During Receive, SW can allow received data to fill up FIFO before reading data.

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5. What is the data width of the Transmit FIFO?
   - Data width = 8 bits.

6. Why is the data width of the Receive FIFO larger than that of the Transmit FIFO? What are the extra bits for?
   - During a Read, 8 Data bits & 4 Status bits are pushed to the Receive FIFO, giving a total of 12-bits.
   - The 4 additional bits reflect **Error Status**:
     - Break Error (**BE**), Framing Error (**FE**), Parity Error (**PE**), Overrun Error (**OE**).

7. At a system clock of 80 MHz, how can you program UART1 on the LaunchPad to provide a baud rate of 115,200 bits/s?

   Assume *Clock Division* = 16 (HSE bit = '0').

   $Baud\ Rate\ Divider\ (BRD) = \frac{80{,}000{,}000}{16 \times 115{,}200} = 43.40278$

   Integer part = **DIVINT** = 43

   Fractional part = **DIVFRAC** = int (0.40278 x 64 + 0.5) = 26

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8. For the above implementation, what is the error rate?

$$Actual\ Baud\ Rate = \frac{80{,}000{,}000}{16\ \times (43 + \frac{26}{64})} = 115{,}190.7847\ bits/s$$

$$Error\ Rate = \frac{|115{,}200 - 115{,}190.7847|}{115{,}200} \times 100\% = 0.008\%$$

9. Write a short program to initialize the relevant **GPIO pins** to function as the Transmit and Receive pins for UART1 on the LaunchPad.
   - UART1 Tx is mapped to either **PC5** (PMCx field = 2), or PB1 (PMCx field = 1).
   - UART2 Rx is mapped to either **PC4** (PMCx field = 2) or PB0 (PMCx field = 1).
   - For this Question, let's use Port C.

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```
#define PC_UART1_RX         4U      // PC4
#define PC_UART1_TX         5U      // PC5

void Port_Init( void )
{
    /* enable Ports C provide clocks   */
    SYSCTL->RCGCGPIO |= SYSCTL_RCGCGPIO_R2;
    /* Wait for GPIOC to be ready */
    while( 0 == (SYSCTL->PRGPIO & SYSCTL_PRGPIO_R2)){};

    /* Enable clock to UART1   */
    SYSCTL->RCGCUART |= SYSCTL_RCGCUART_R1;
    /* Wait for UART1 to be ready */
    while( 0 == (SYSCTL->PRUART & SYSCTL_PRUART_R1) );

    GPIOC->AFSEL |= BIT(PC_UART1_RX) | BIT(PC_UART1_TX);
    GPIOC->DEN |= BIT(PC_UART1_RX) | BIT(PC_UART1_TX);
    GPIOC->AMSEL &= ~( BIT(PC_UART1_RX) | BIT(PC_UART1_TX) );
    /* clear Port C config bits  */
    GPIOC->PCTL &= ~( GPIO_PCTL_PC4_M | GPIO_PCTL_PC5_M );
    GPIOC->PCTL |= GPIO_PCTL_PC4_U1RX | GPIO_PCTL_PC5_U1TX;
}
```

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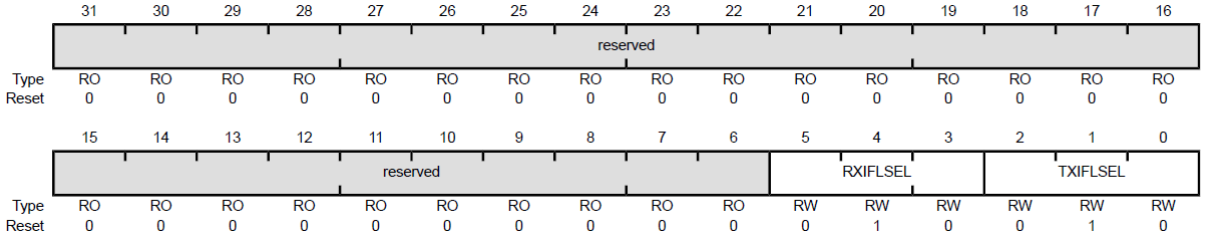
10. Which register is used to set the TX FIFO trigger level for a UART? What value should be written to the register to set the RX FIFO to trigger at ¼ full and the TX FIFO to trigger at ¼ full?
    - Both TX & RX FIFO trigger levels are set through the UART Interrupt FIFO Level Select (**UARTIFLS**) register.
    - To set to trigger RX FIFO at ¼ full and TX FIFO at ¼ empty, set UARTIFLS = 0x0B. (RXIFLSEL = 0x01; TXIFLSEL = 0x03).



UART Interrupt FIFO Level Select (UARTIFLS) register

UART Receive Interrupt FIFO Level Select
The trigger points for the receive interrupt are as follows:

Value	Description
0x0	RX FIFO ≥ ⅛ full
0x1	RX FIFO ≥ ¼ full
0x2	RX FIFO ≥ ½ full (default)
0x3	RX FIFO ≥ ¾ full
0x4	RX FIFO ≥ ⅞ full
0x5-0x7	Reserved

UART Transmit Interrupt FIFO Level Select
The trigger points for the transmit interrupt are as follows:

Value	Description
0x0	TX FIFO ≤ ⅞ empty
0x1	TX FIFO ≤ ¾ empty
0x2	TX FIFO ≤ ½ empty (default)
0x3	TX FIFO ≤ ¼ empty
0x4	TX FIFO ≤ ⅛ empty
0x5-0x7	Reserved

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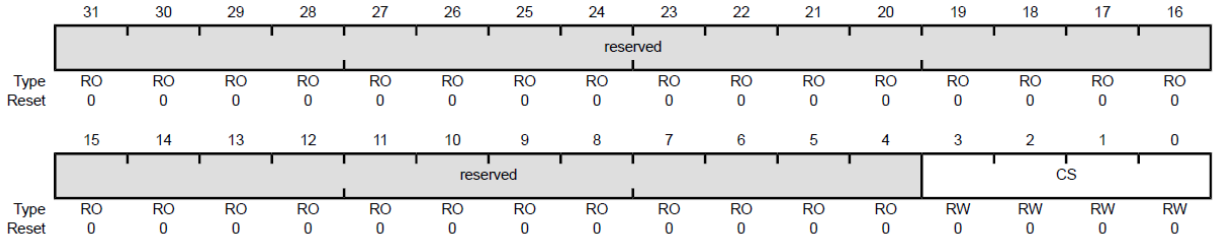
11. Which register is used to set the UART Baud Rate clock to use the PIOSC clock source? What value should you write to the register?
    - UART Clock Configuration (UARTCC) register.
    - Set CS file (4 bits) to 0x05.



UART Clock Configuration (UARTCC) register

CS	RW	0	UART Baud Clock Source The following table specifies the source that generates for the UART baud clock:

Value	Description
0x0	System clock (based on clock source and divisor factor)
0x1-0x4	reserved
0x5	PIOSC
0x5-0xF	Reserved

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12. The figure below shows a UART data frame with LSB bit transmitted first.
    - What is the ASCII character ('DATA') sent by the UART?
        - DATA sent is ASCII character 'g' (0x67).
    - Is the data sent with Even or Odd parity? Explain your reasoning.
        - Parity = ODD. Total number of '1's (data bits + parity) = 5.