Embedded Systems

CS 397

TRIMESTER 3, AY 2021/22

STM32F7 ETH (Ethernet 802.3): MAC (Media Access Control) with DMA Controller

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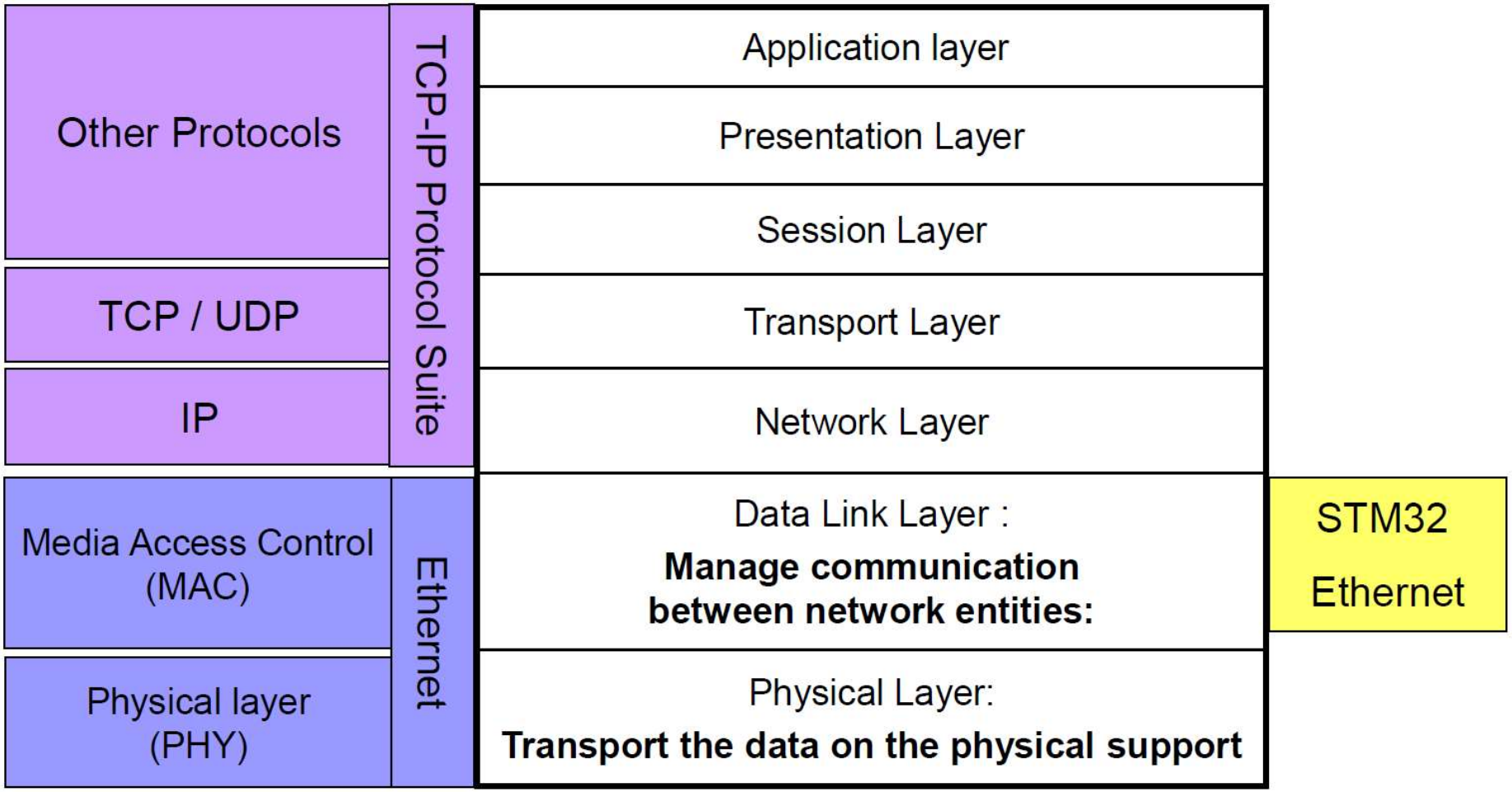
STM32F7 ETH

Overview

The OSI (Open System Interconnection) model



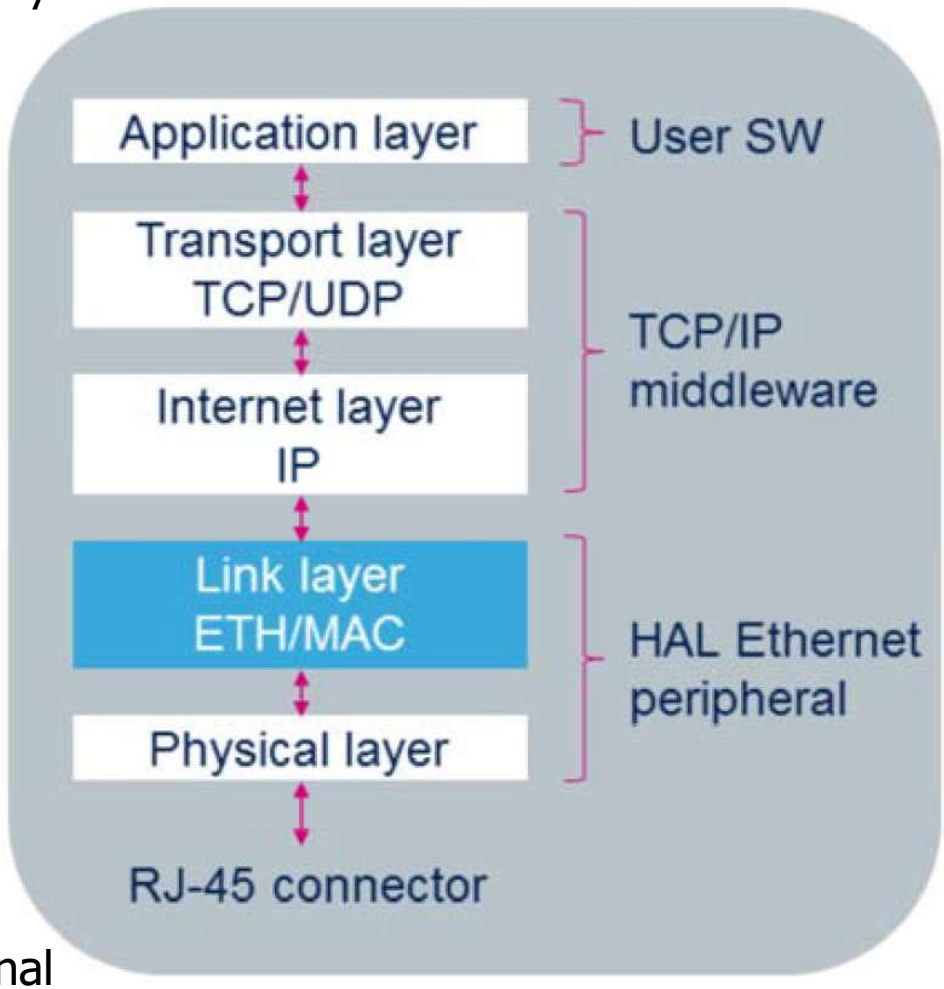
- The OSI model is developed by ISO (International Standards Organization).
- The STM32F7's ETH MAC peripheral is in charge of the Media Access Control layer of the Ethernet communication.

STM32F7 ETH

Overview

MII: Media Independent Interface
RMII: Reduced Media Independent Interface

- The STM32F7's MAC for Ethernet protocol is fully compliant with the IEEE 802.3-2002 standard.
- The MAC enables the efficient development of applications based on TCP/IP model.
- The MAC embeds its own DMA and provides the link layer for TCP/IP communication.
- Upper layers are managed by software. E.g., Transport and Internet layers can be managed by the popular LwIP (a lightweight TCP/IP) stack.
- The MAC supports both MII and RMII to external PHY (physical layer). The PHY is implemented by external components and linked to an RJ45 connector.

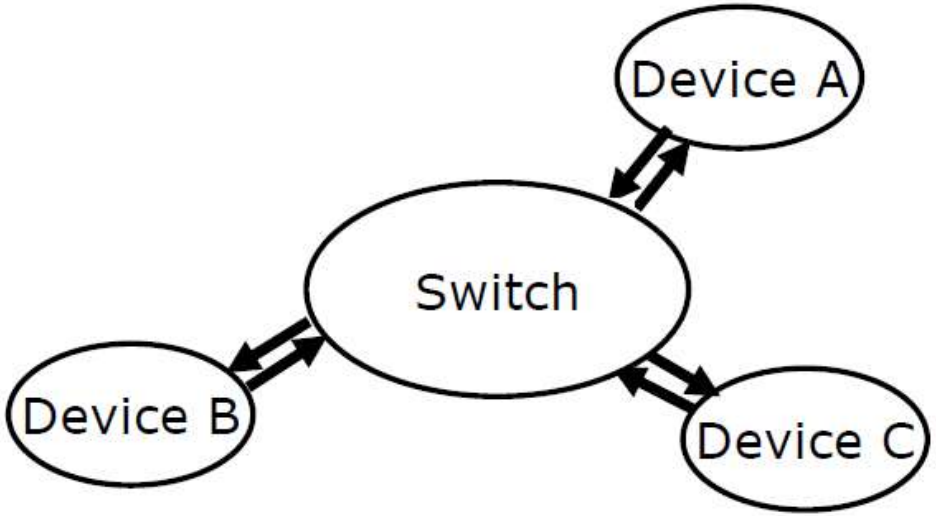


A typical TCP/IP Ethernet Implementation

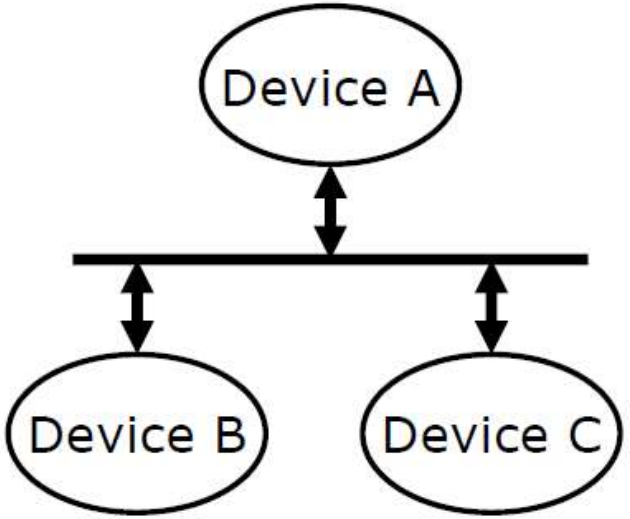
LwIP: https://savannah.nongnu.org/projects/lwip/

Full Duplex Vs. Half Duplex

- Full Duplex
  - A network with a star architecture
  - Point to point connection between each device



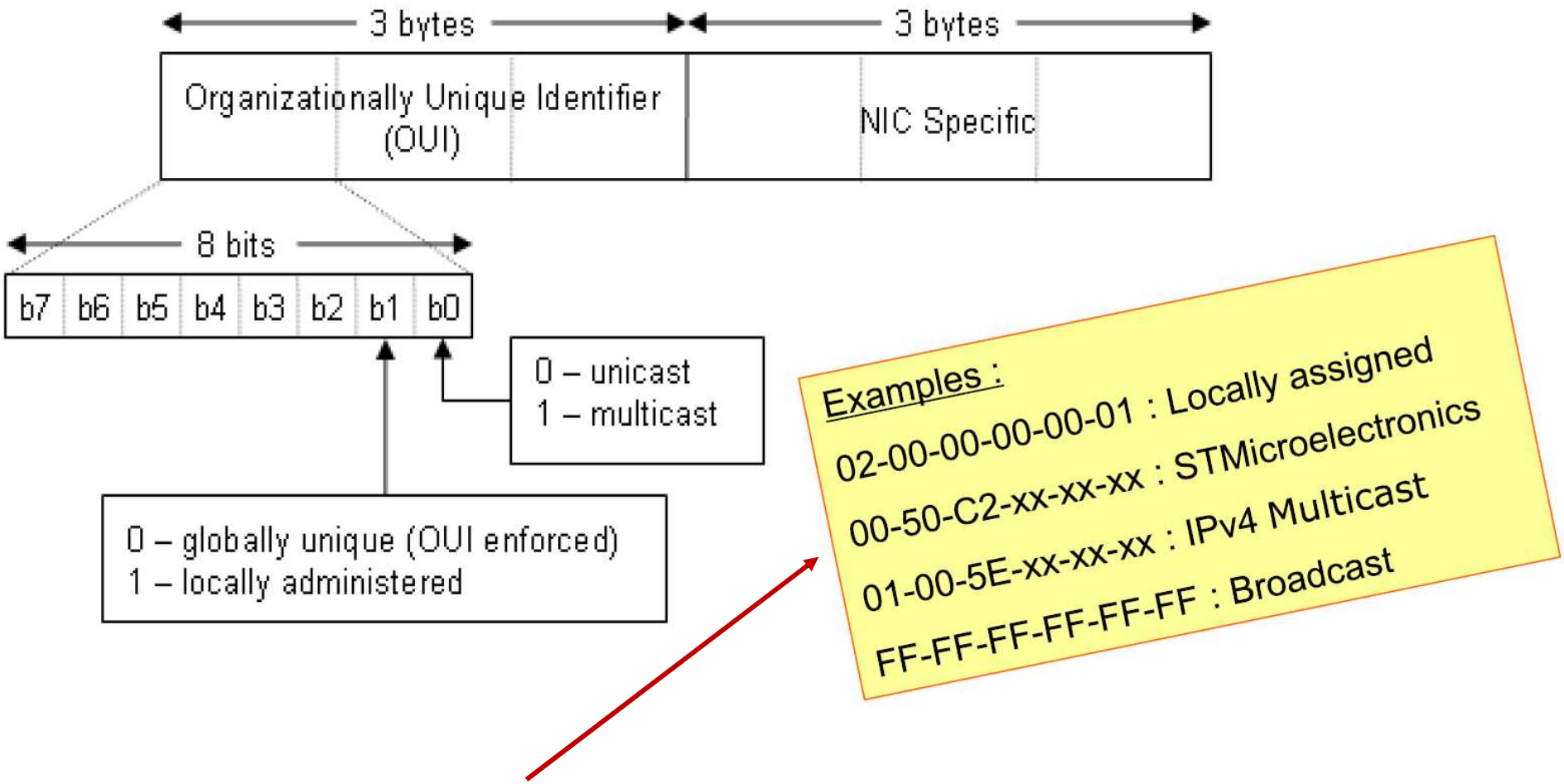
- Half Duplex
  - A network with a bus architecture
  - Use a carrier sensing scheme with collision detection CSMA/CD



Source: STMicroelectronics Training Notes

Ethernet Frame (MAC Addresses)

The MAC address (XX–XX–XX–XX–XX–XX) that acts like a name for a particular network adapter

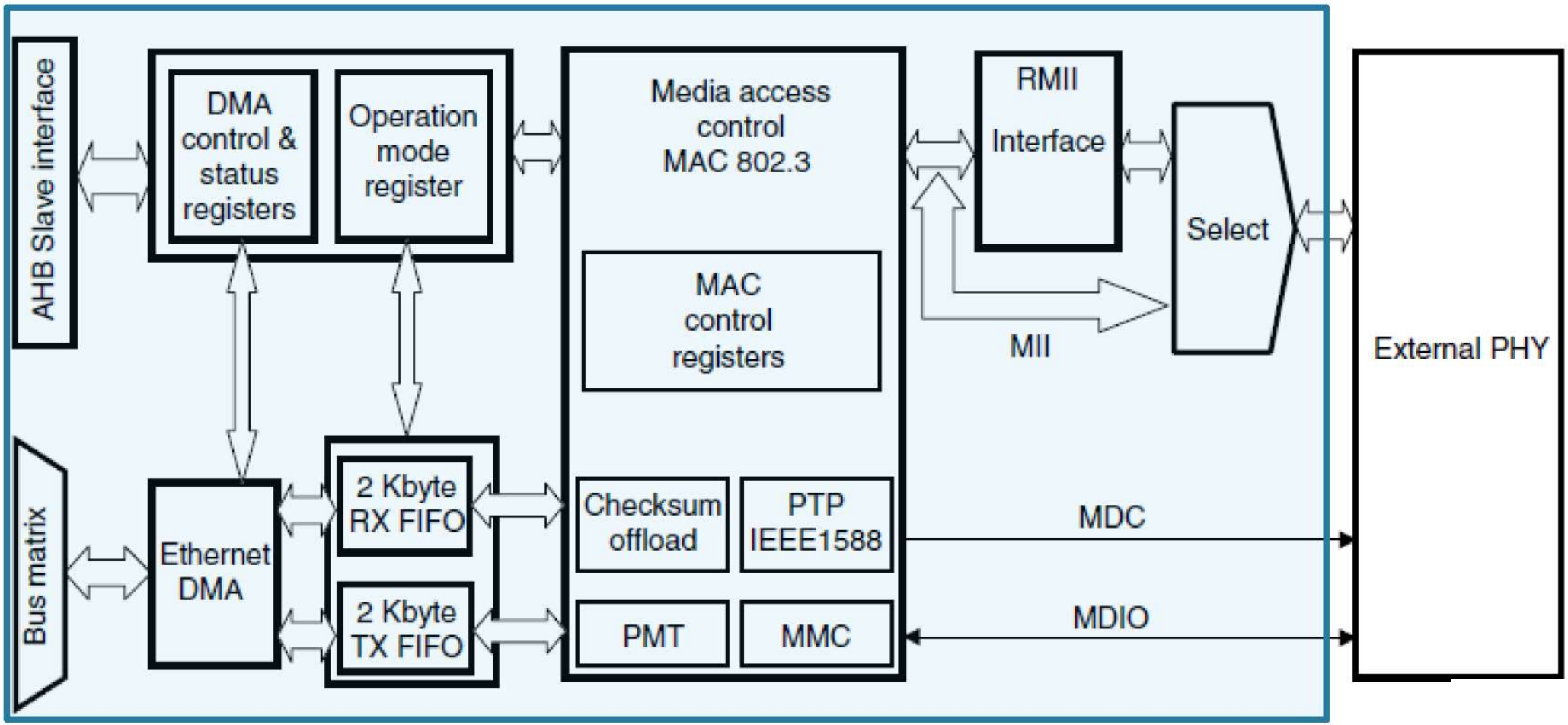


STMicroelectronics: 00-80-E1-XX-XX-XX

Source: STMicroelectronics Training Notes

STM32F7 Ethernet Block Diagram

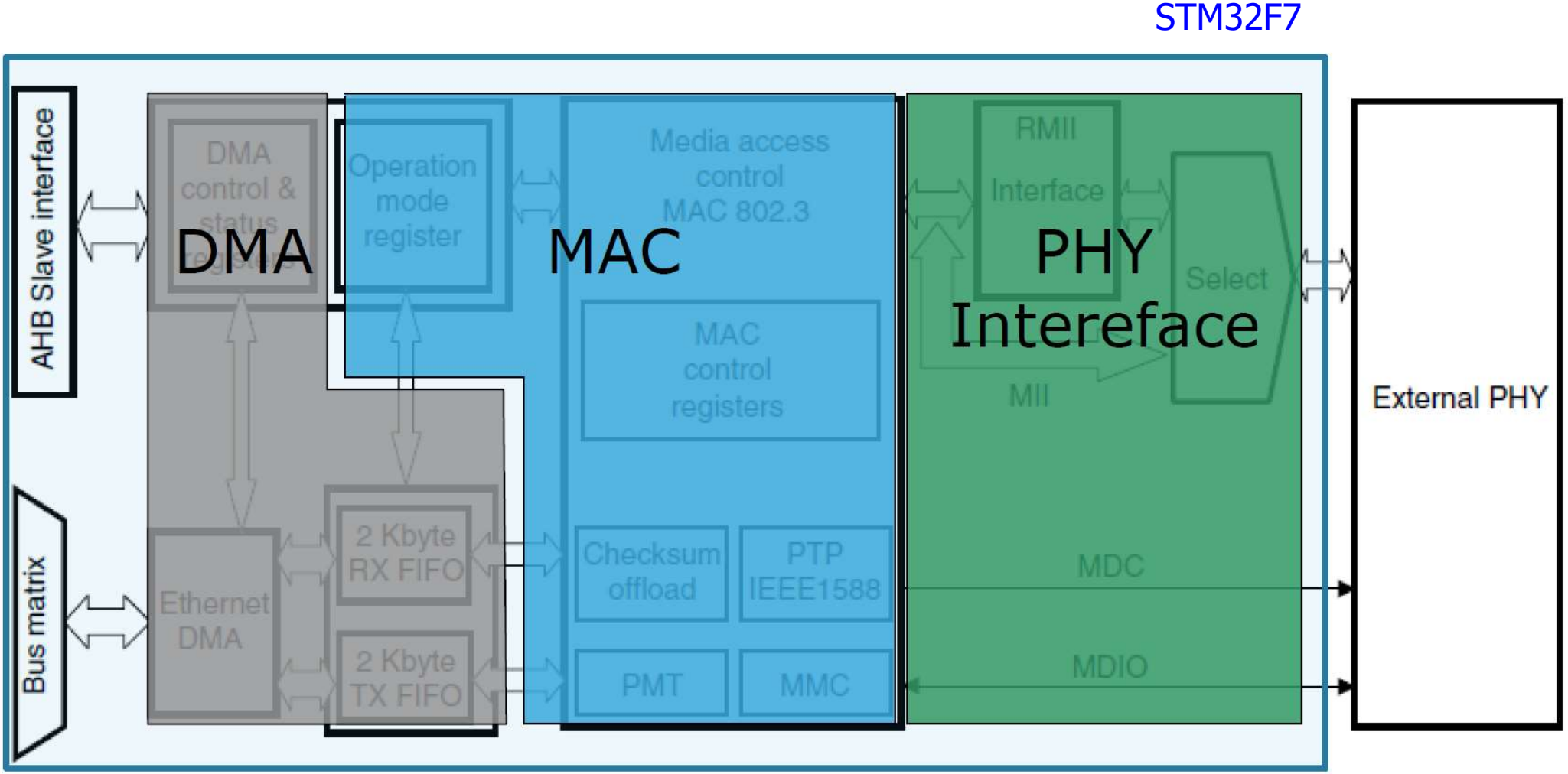
STM32F7



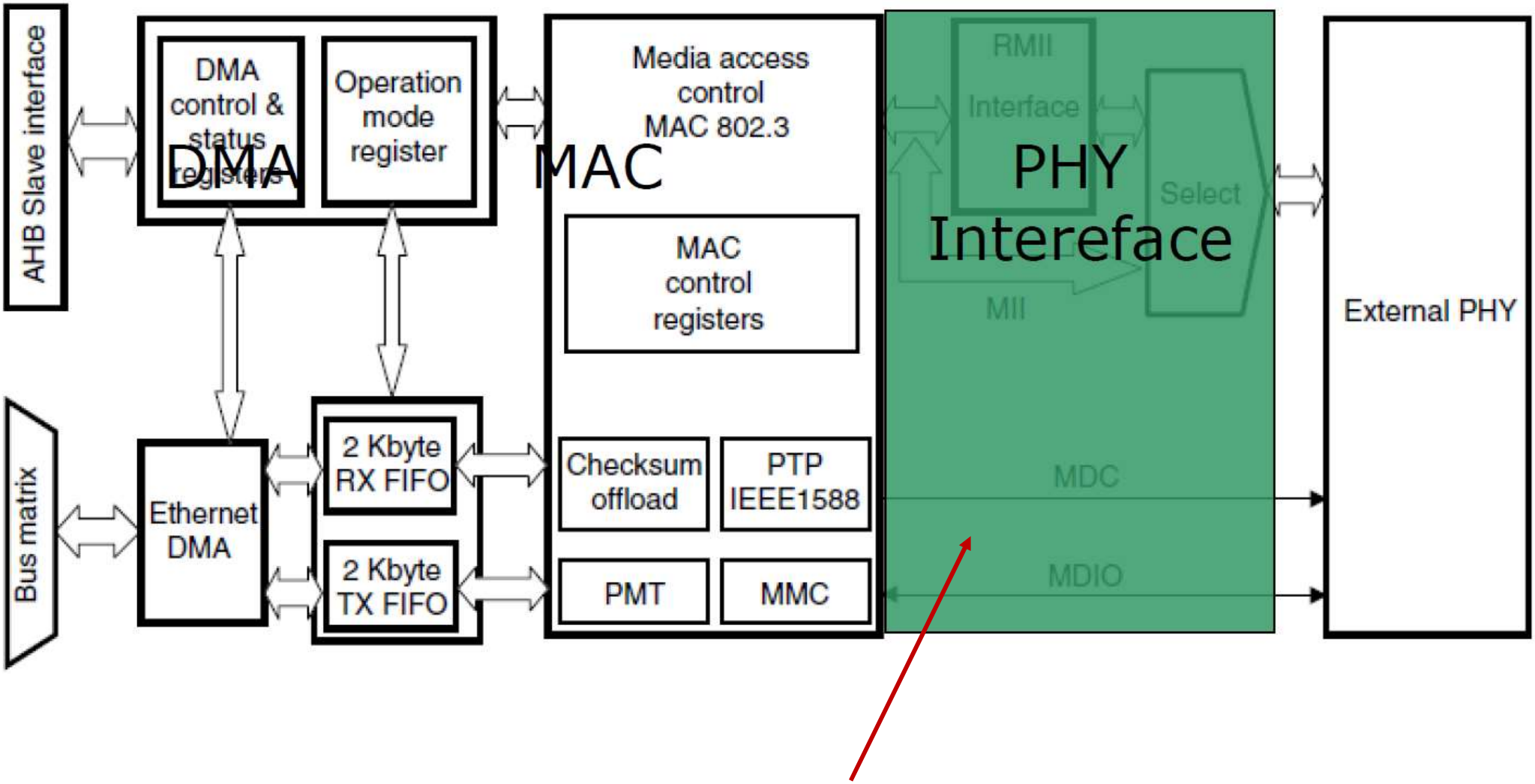
DMA: Direct Memory Access
MAC: Media Access Control
PTP: Precision Time Protocol
PMT: Power Management
MMC: MAC Management Counters

MII: Media Independent Interface
RMII: Reduced Media Independent Interface
MDC: Management Data Clock
MDIO: Management Data Input/Output
PHY: Physical Layer
FIFO: First-In-First-Out

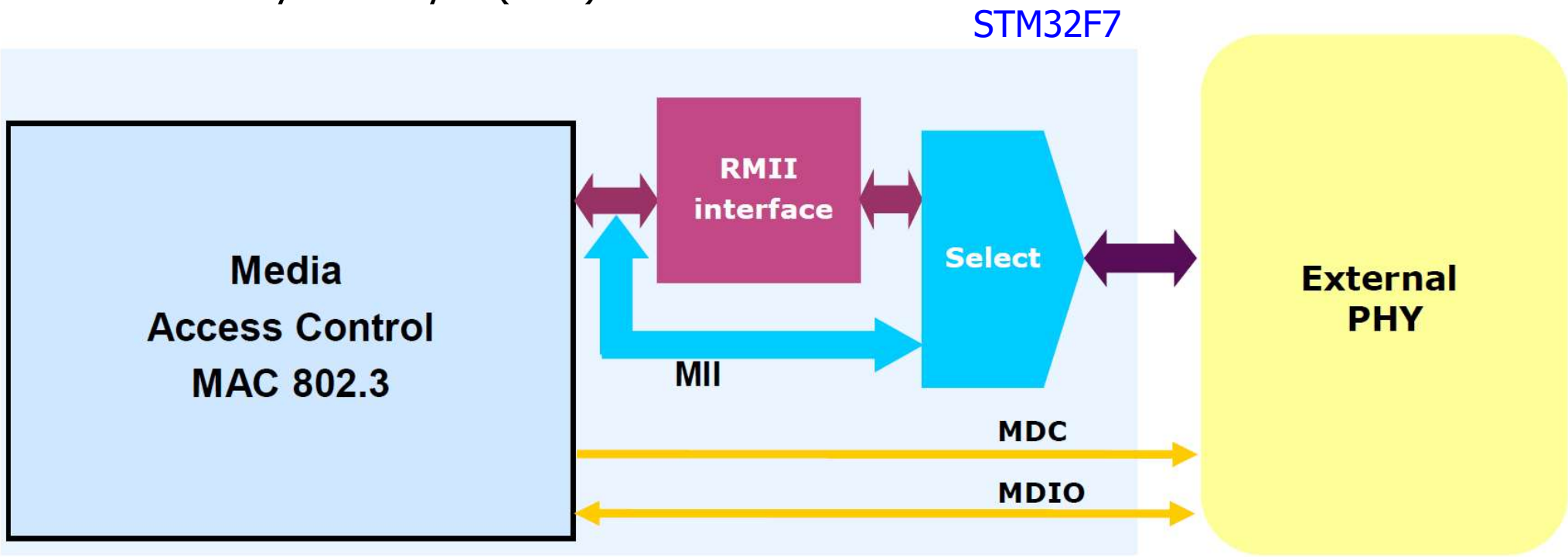
STM32F7 Ethernet Block Diagram



STM32F7 Ethernet Block Diagram



STM32F7 Physical Layer (PHY) Interface



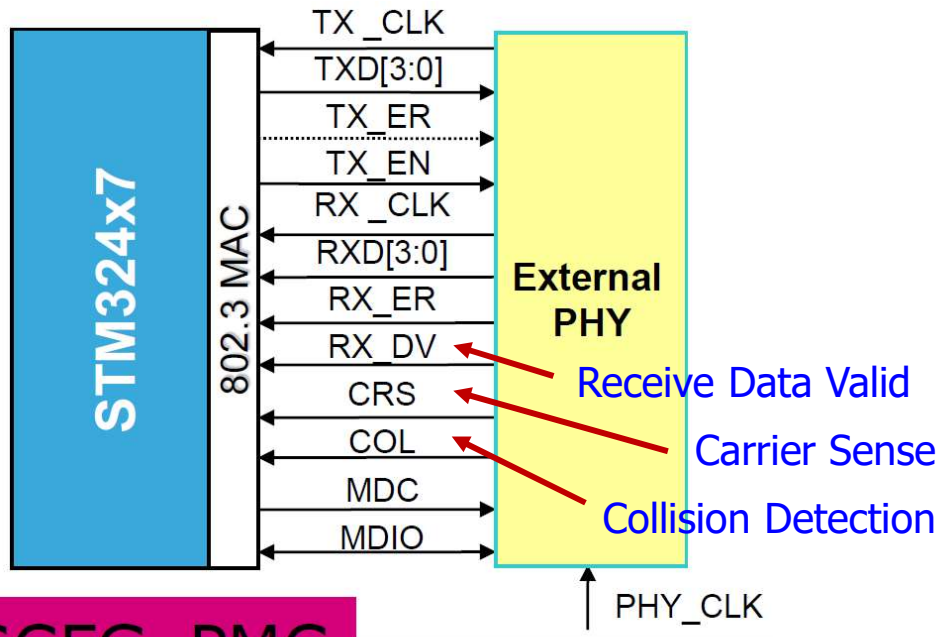
- Supports both Media Independent Interface (MII) and Reduced Media Independent Interface (RMII).
- RMII is a lower pin count alternative, which targets multi-port applications and low-cost design.
- Internal loopback on the MII for debugging.
- MDC/MDIO for the PHY configuration

MDC: Management Data Clock
MDIO: Management Data Input/Output

SYSCFG: System Configuration Controller
PMC: Peripheral Mode Configuration Register

STM32F7 Physical Layer (PHY) Interface

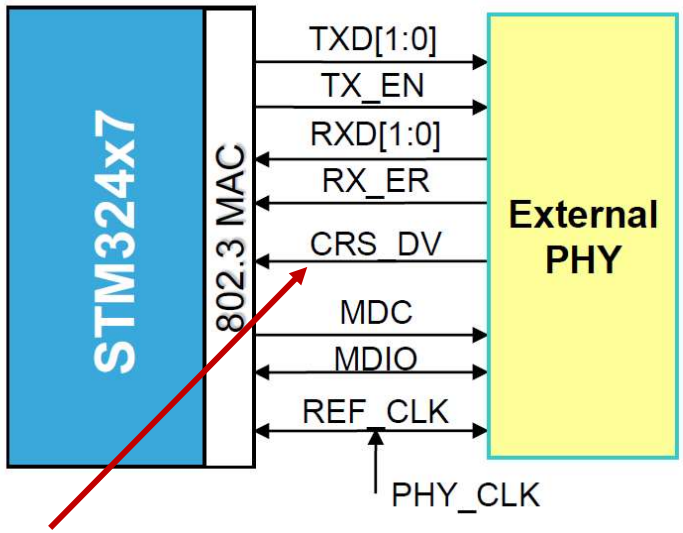
- MII = 18 pins
  - 8 data pins
  - 6 control pins
  - 2 Clock signals
  - 2 for PHY configuration
  - TX_ER(optional, rarely used, STM32 don't have this pin)



Selected in SYSCFG_PMC

Bit 23: MII_RMII_SEL = 0 (MII) or 1 (RMII)

- RMII = 10 pins
  - 4 data
  - 3 control
  - 1 for the clock
  - 2 for PHY configuration
  - RX_ER(optional on switches)

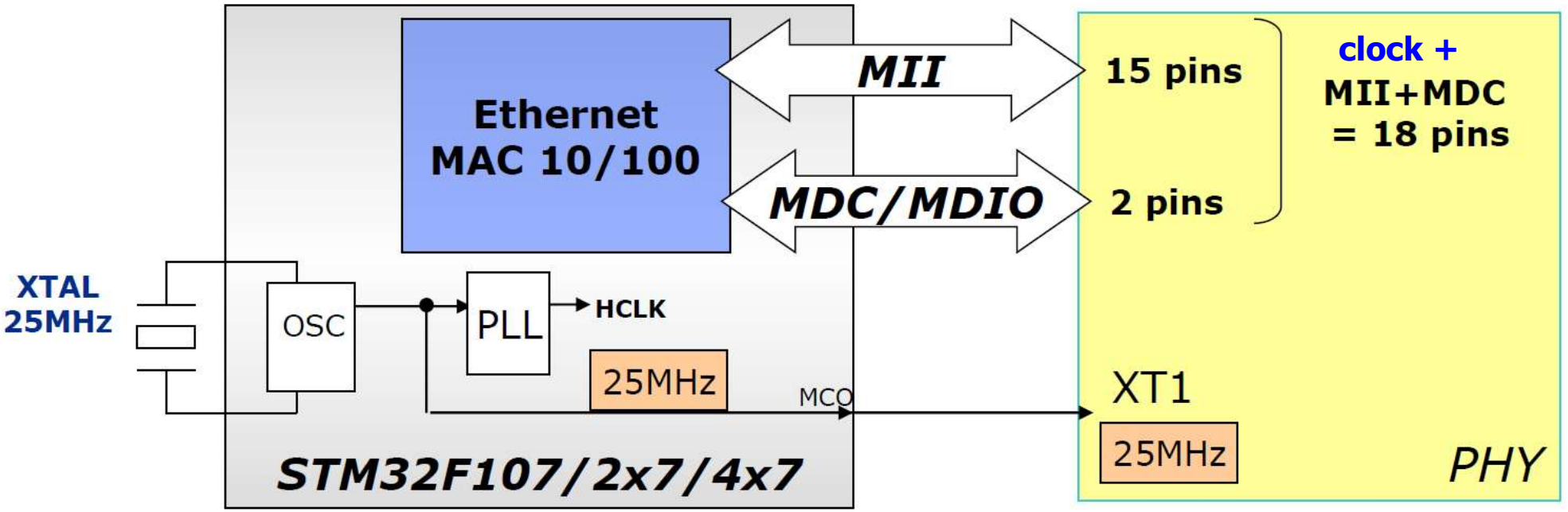


RMII Receive Error (optional connection to MAC)

RMII Carrier Sense/Receive Data Valid

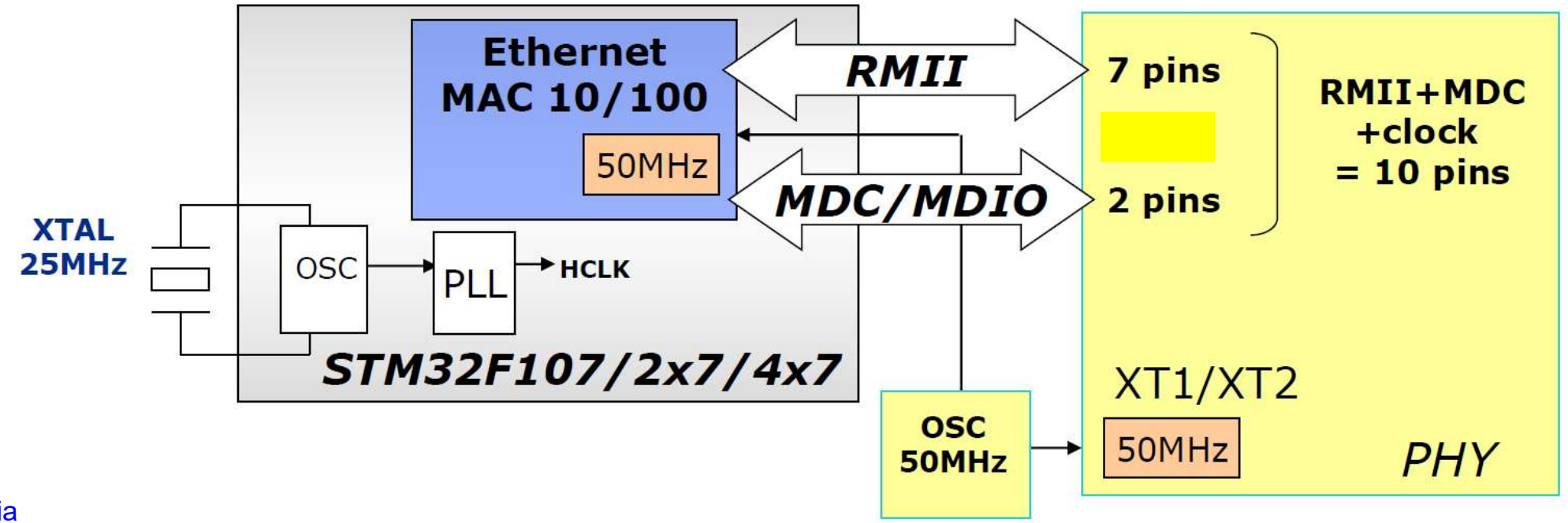
STM32F7 Ethernet Interface Block Diagram (MII) (1/6)

- One 25MHz external crystal (internal oscillator)
  - The internal PLL to generate HCLK (Core, peripherals…)
  - Connected to the MCO to provide the 25MHz to the PHY



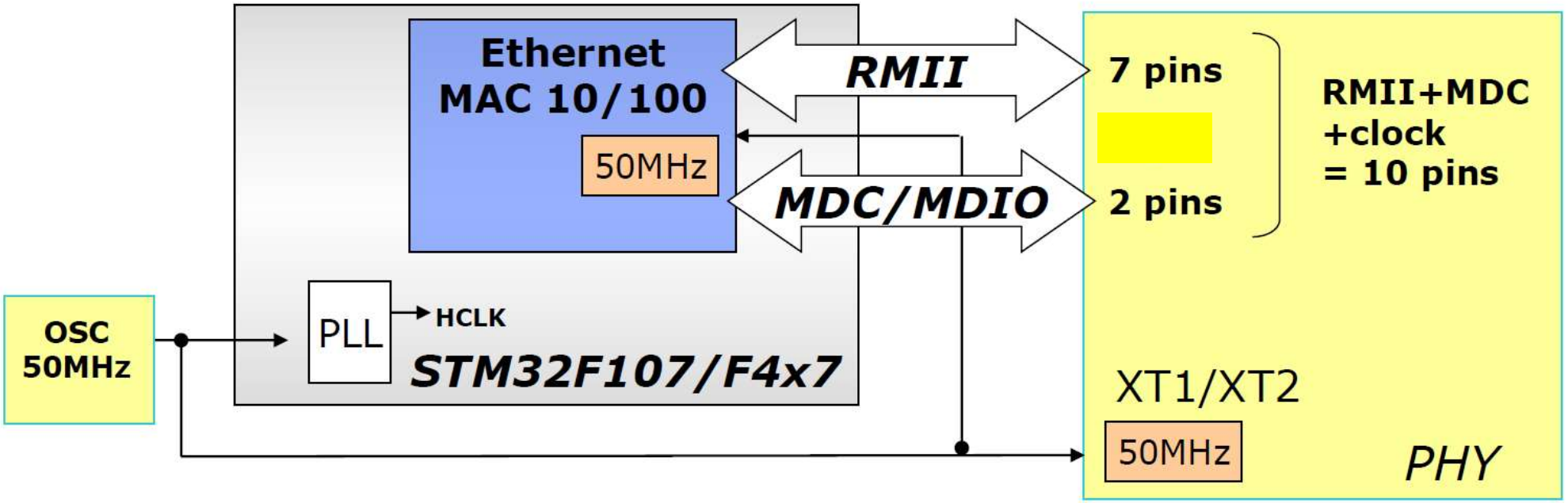
STM32F7 Ethernet Interface Block Diagram (RMII) (2/6)

- One 50MHz external oscillator
  - This 50MHz output clock is provided to the MAC and PHY
- One 25MHz external crystal (internal oscillator)
  - The internal PLL to generate HCLK (Core, peripherals…)
- RMII interface
  - 7 pins for the communication between the MAC and PHY
  - 2 pins for the MDC and MDIO (PHY control)
  - 1 pin for the 50MHz clock input



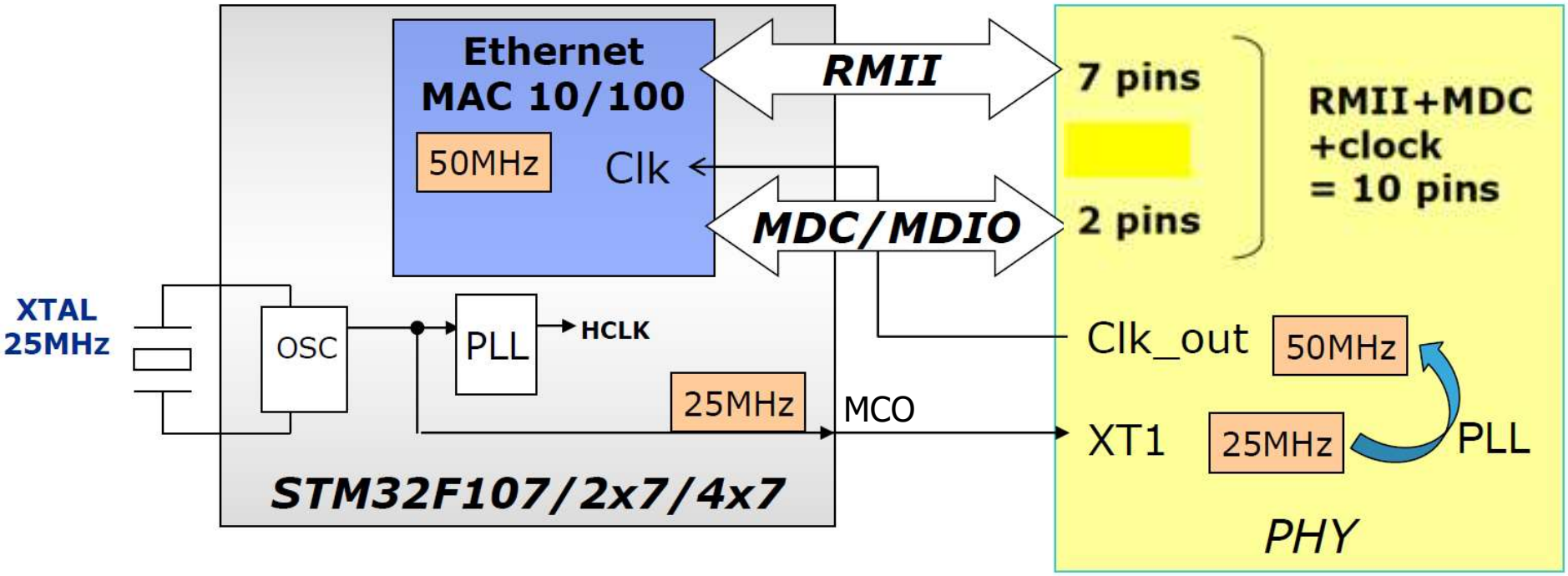
STM32F7 Ethernet Interface Block Diagram (RMII) (3/6)

- One 50MHz external oscillator
  - Connected to the PLL to generate HCLK (Core, peripherals…)
  - This 50MHz output clock is also provided to the MAC and PHY

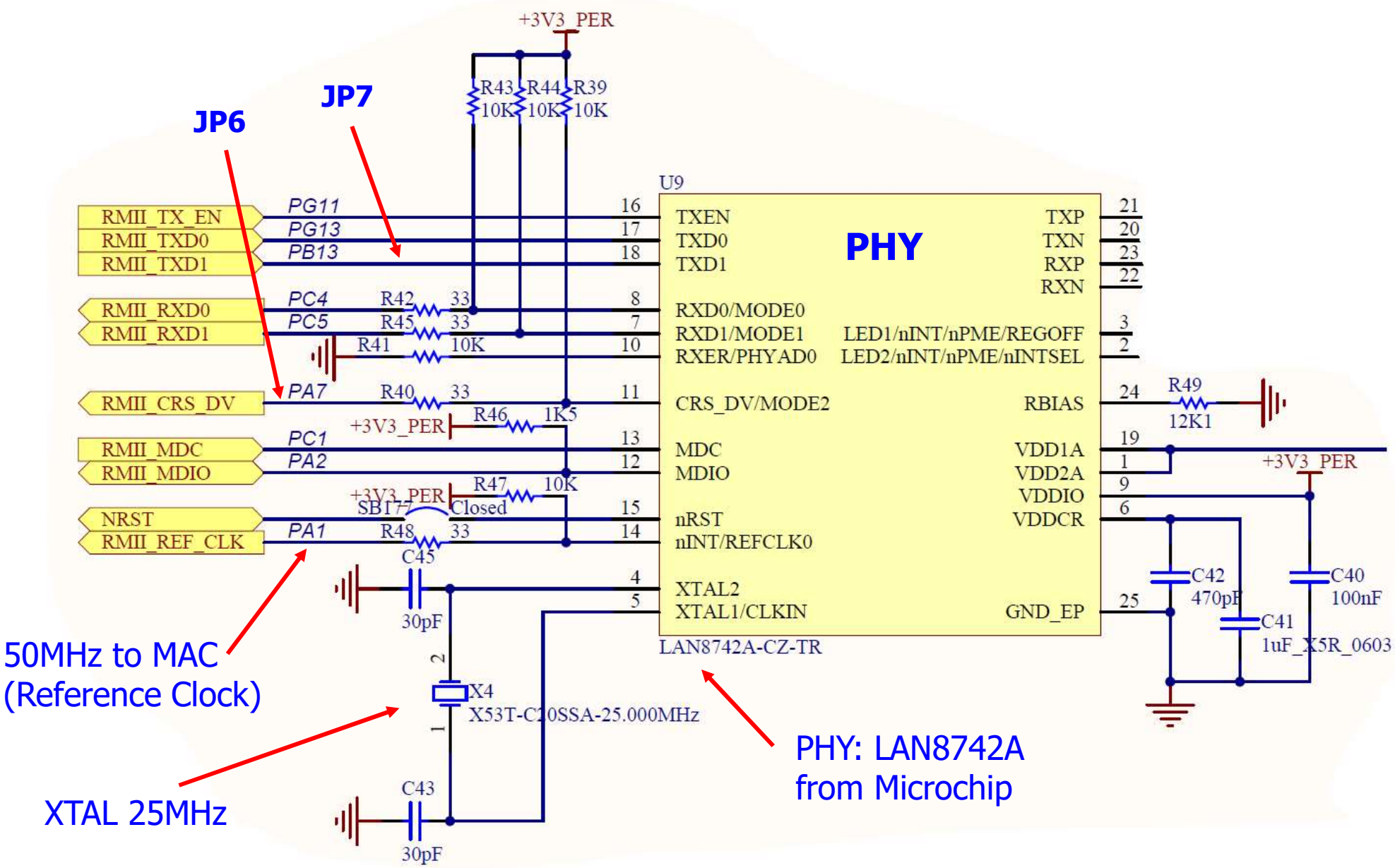


STM32F7 Ethernet Interface Block Diagram (RMII) (4/6)

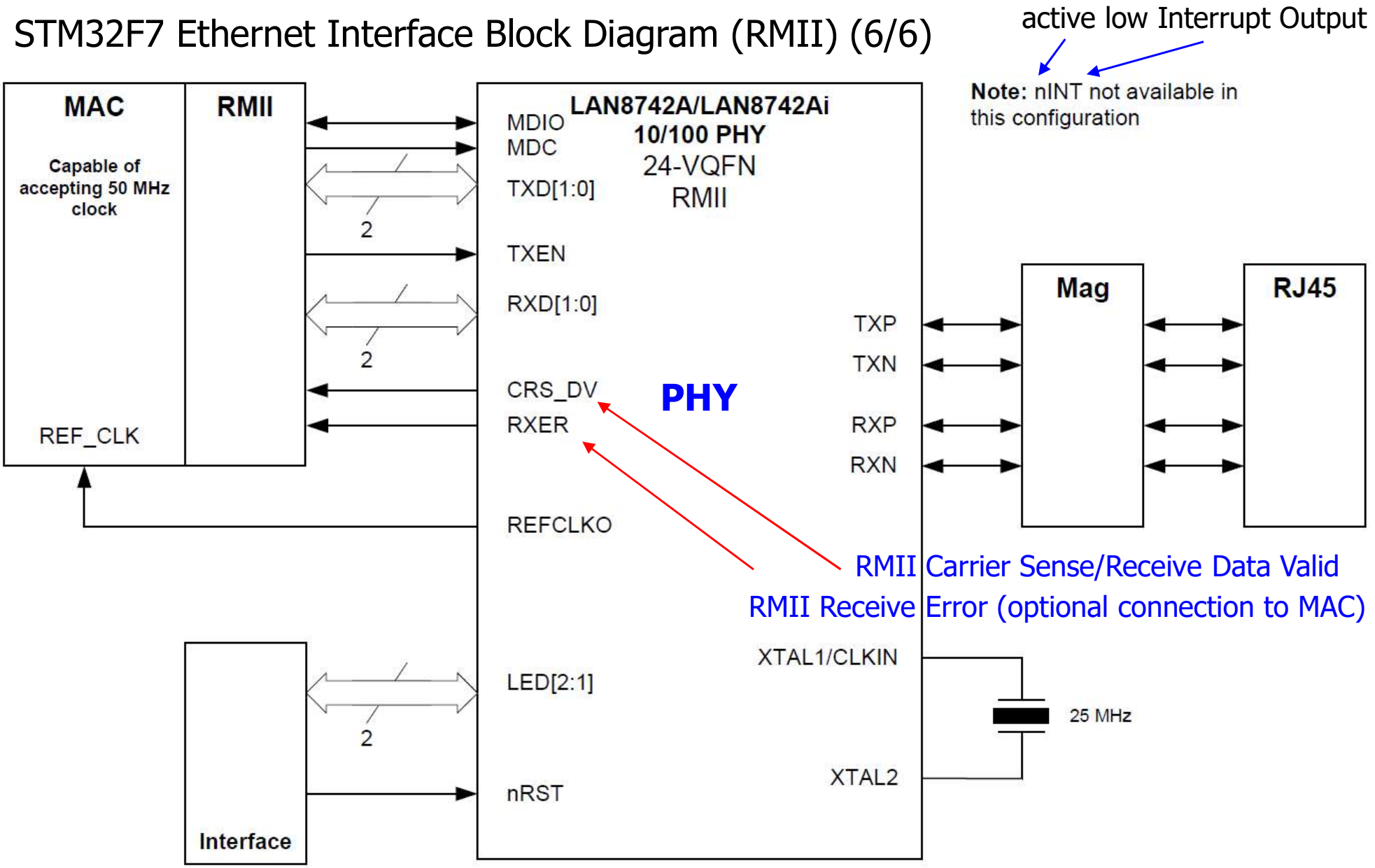
- One 25MHz external crystal (internal oscillator)
  - The internal PLL to generate HCLK (Core, peripherals…)
  - Connected to the MCO to provide the 25MHz to the PHY
  - The PHY then generate the 50MHz reference clock to MAC
- RMII interface
  - 7 pins for the communication between the MAC and PHY
  - 2 pins for the MDC and MDIO (PHY control)
  - 1 pin for the 50MHz clock output to MAC



STM32F7 Ethernet Interface Block Diagram (RMII) (5/6)



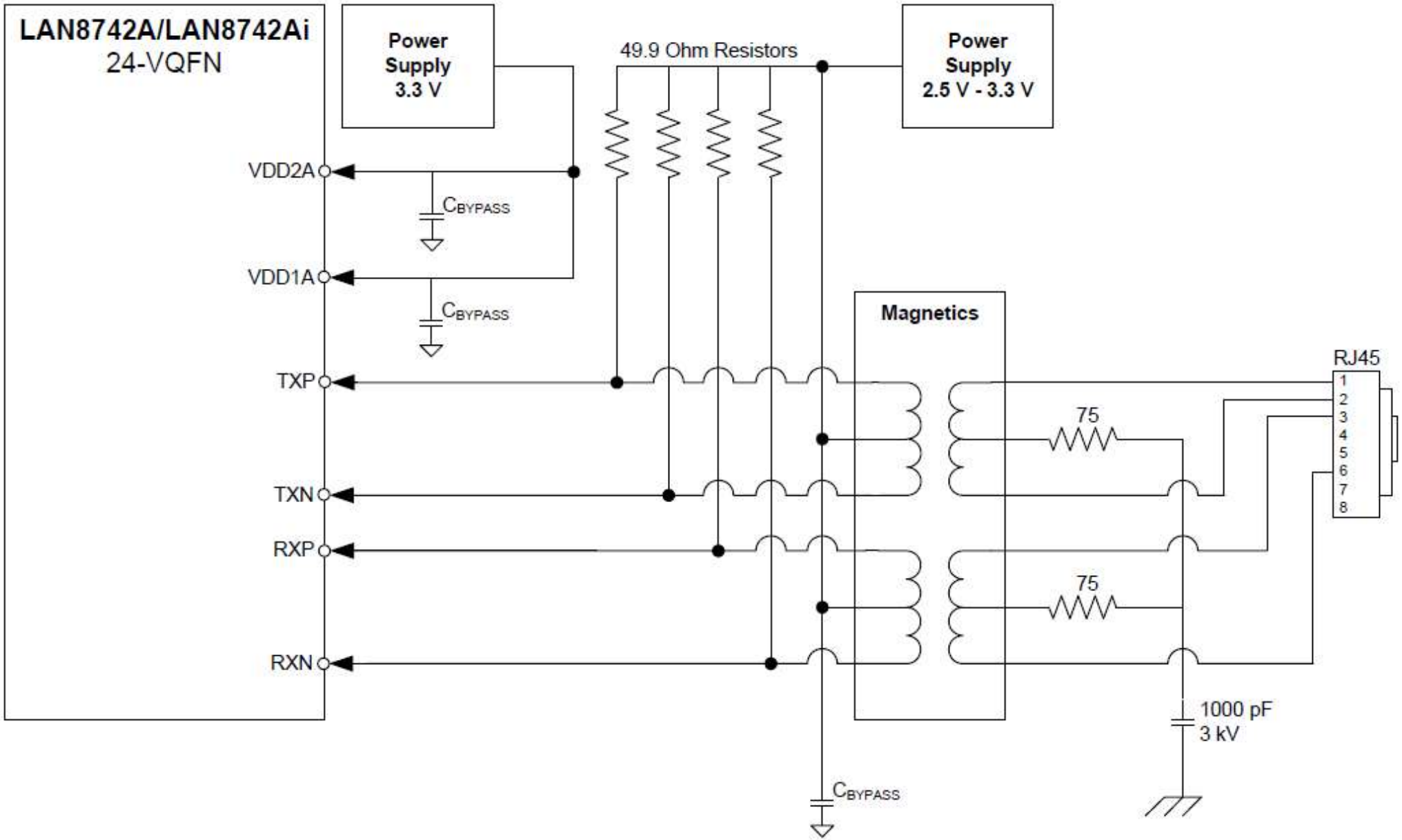
STM32F7 Ethernet Interface Block Diagram (RMII) (6/6)



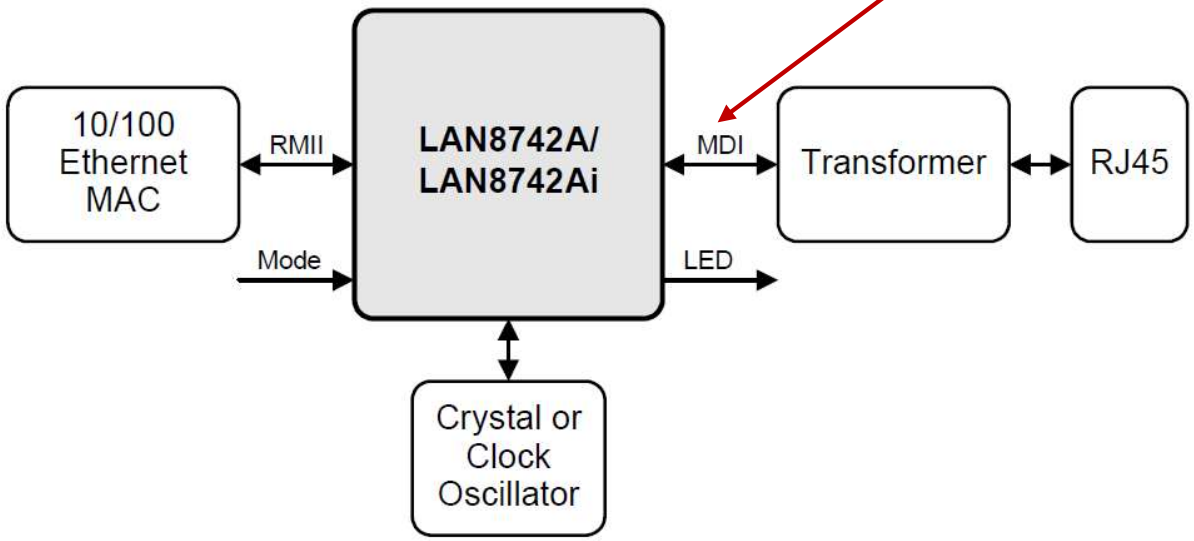
Sourcing REF_CLK from a 25MHz Crystal (REF_CLK Out mode, nINTSEL = 0)

Note: The REFCLKO pin is multiplexed with the nINT pin. In REF_CLK Out mode, the nINT functionality is disabled, and the output REFCLKO is a 50MHz clock to the MAC.

PHY LAN8742A: Twisted-pair Interface Diagram (dual power supplies)

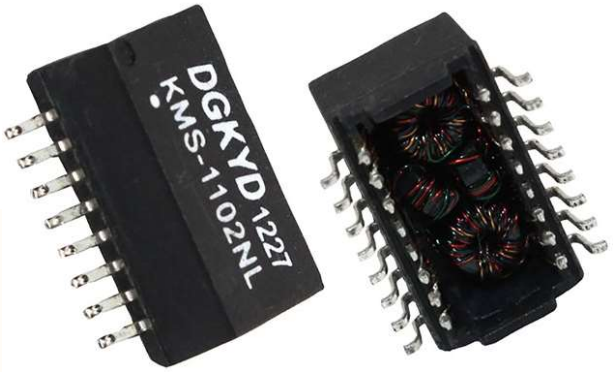


Ethernet PHY Connection

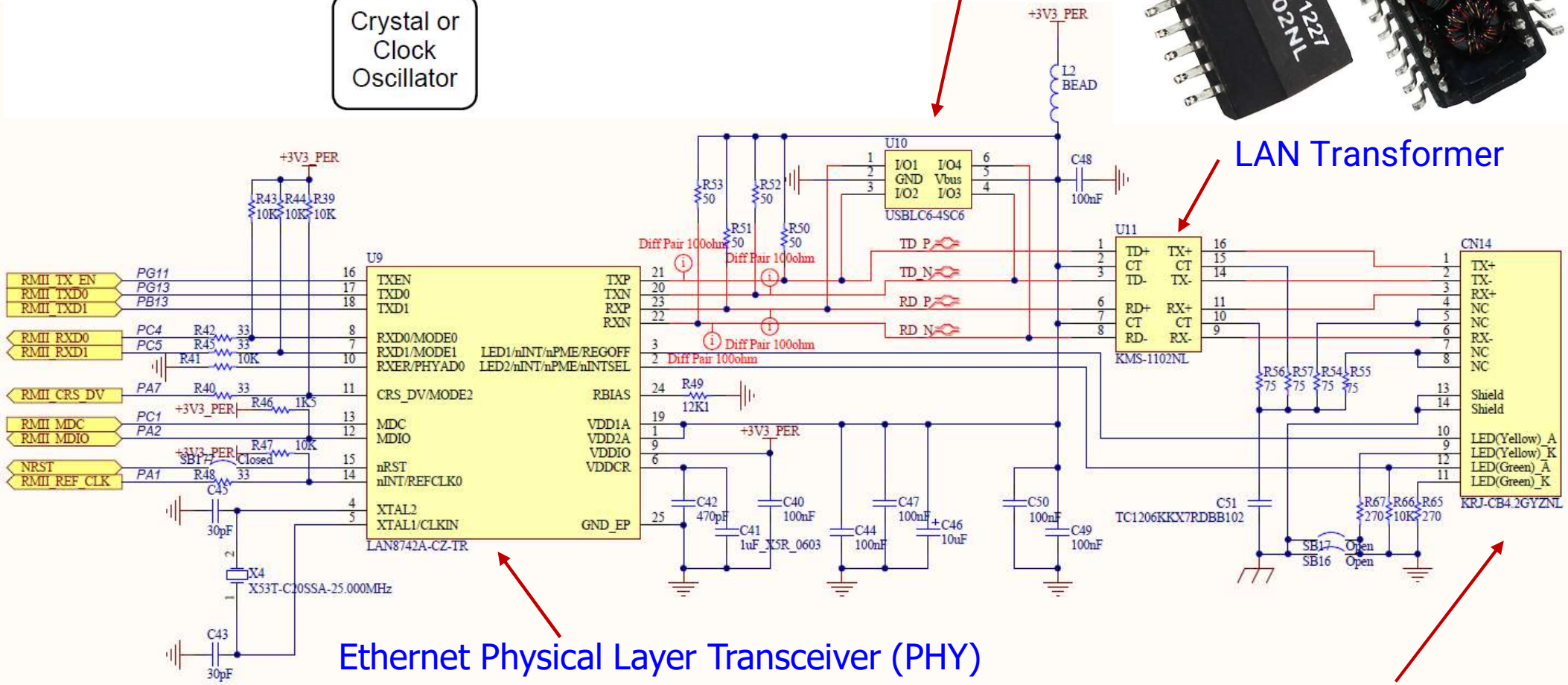


medium dependent interface

ESD (Electrostatic discharge) protection of high-speed interfaces



LAN Transformer



Ethernet Physical Layer Transceiver (PHY)

RJ45 connector

CRS_DA = Carrier Sense / Receive Data Valid

The Ethernet PHY to RJ45 Connection [Ref_05-2]

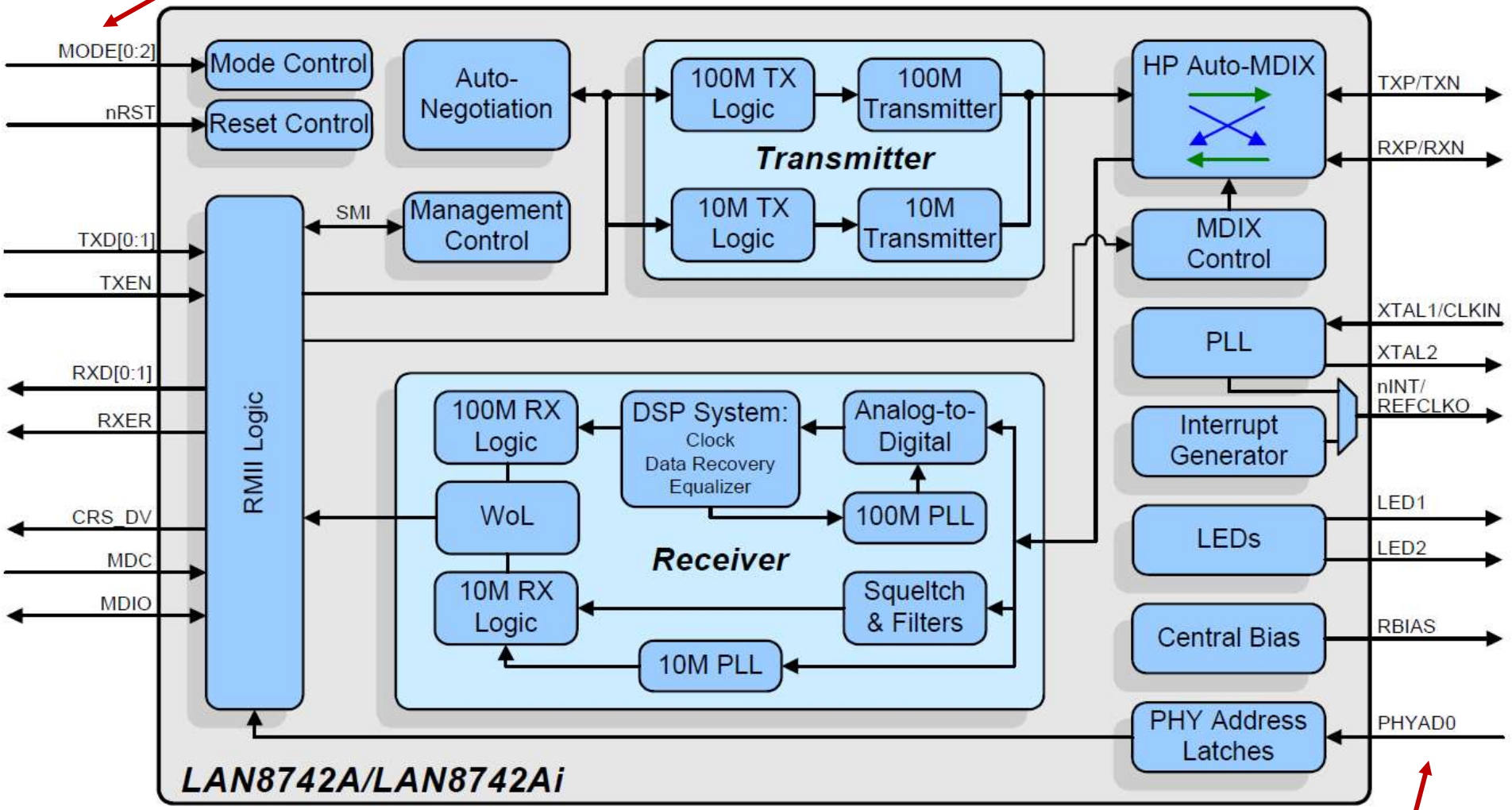
PHY (Ethernet Transceiver) Registers

- The PHY Registers are :
  - Initialized by the Bootstrap configuration
  - Can be accessed by the MCU (need to know the PHY address)
- There are 3 types of Registers :
  - Basic
  - Extended
  - Vendor Specific
- It is possible to change PHY settings with the ST's driver

LAN8742A (PHY): Architectural Overview

011 : 100BASE-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.

111 : All capable. Auto-negotiation enabled



The PHYAD0 bit is driven high or low to give each PHY a unique address.

Serial Management Interface: MDC & MDIO

LAN8742A (PHY): Control and Status Registers (Table 4-2: SMI Register Map)

Register Index (Decimal)	Register Name	Group
0	Basic Control Register	Basic
1	Basic Status Register	Basic
2	PHY Identifier 1 Register	Extended
3	PHY Identifier 2 Register	Extended
4	Auto Negotiation Advertisement Register	Extended
5	Auto Negotiation Link Partner Ability Register	Extended
6	Auto Negotiation Expansion Register	Extended
7	Auto Negotiation Next Page TX Register	Extended
8	Auto Negotiation Next Page RX Register	Extended
13	MMD Access Control Register	Extended
14	MMD Access Address/Data Register	Extended
16	EDPD NLP/Crossover TimeRegister	Vendor-specific
17	Mode Control/Status Register	Vendor-specific
18	Special Modes Register	Vendor-specific
24	TDR Patterns/Delay Control Register	Vendor-specific
25	TDR Control/Status Register	Vendor-specific
26	Symbol Error Counter Register	Vendor-specific
27	Special Control/Status Indications Register	Vendor-specific
28	Cable Length Register	Vendor-specific
0x1D 29	Interrupt Source Flag Register	Vendor-specific
30	Interrupt Mask Register	Vendor-specific
0x1F 31	PHY Special Control/Status Register	Vendor-specific

Read the Auto-Negotiation's Result of LAN8742A (PHY) (1/3)

4.2.22 PHY SPECIAL CONTROL/STATUS REGISTER

Index (In Decimal): 31 Size: 16 bits

Bits	Description	Type	Default
15:13	**RESERVED**	RO	-
12	**Autodone** Auto-negotiation done indication: 0 = Auto-negotiation is not done or disabled (or not active). 1 = Auto-negotiation is done.	RO	0b
11:5	**RESERVED - Write as 0000010b, ignore on read.**	R/W	0000010b
4:2	**Speed Indication** HCDSPEED value: 001 = 10BASE-T half-duplex 101 = 10BASE-T full-duplex 010 = 100BASE-TX half-duplex 110 = 100BASE-TX full-duplex	RO	XXXb
1:0	**RESERVED**	RO	-

Read the Auto-Negotiation's Result of DP83848C (PHY) (2/3)

Table 6-18. PHY Status Register (PHYSTS), address 10h (continued)

Bit	Bit Name	Default	Description
4	AUTO-NEG COMPLETE	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation complete. 0 = Auto-Negotiation not complete.
3	LOOPBACK STATUS	0, RO	**Loopback:** 1 = Loopback enabled. 0 = Normal operation.
2	DUPLEX STATUS	0, RO	**Duplex:** This bit indicates duplex status and is determined from Auto-Negotiation or Forced Modes. 1 = Full duplex mode. 0 = Half duplex mode.(1)
1	SPEED STATUS	0, RO	**Speed10:** This bit indicates the status of the speed and is determined from Auto-Negotiation or Forced Modes. 1 = 10 Mb/s mode. 0 = 100 Mb/s mode.(1)
0	LINK STATUS	0, RO	**Link Status:** This bit is a duplicate of the Link Status bit in the BMSR register, except that it will not be cleared upon a read of the PHYSTS register. 1 = Valid link established (for either 10 or 100 Mb/s operation). 0 = Link not established.

(1) Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.

How to Change PHY with ST's Driver (3/3)

- When PHY is changed, the user must update the value accordingly based on the selected external PHY

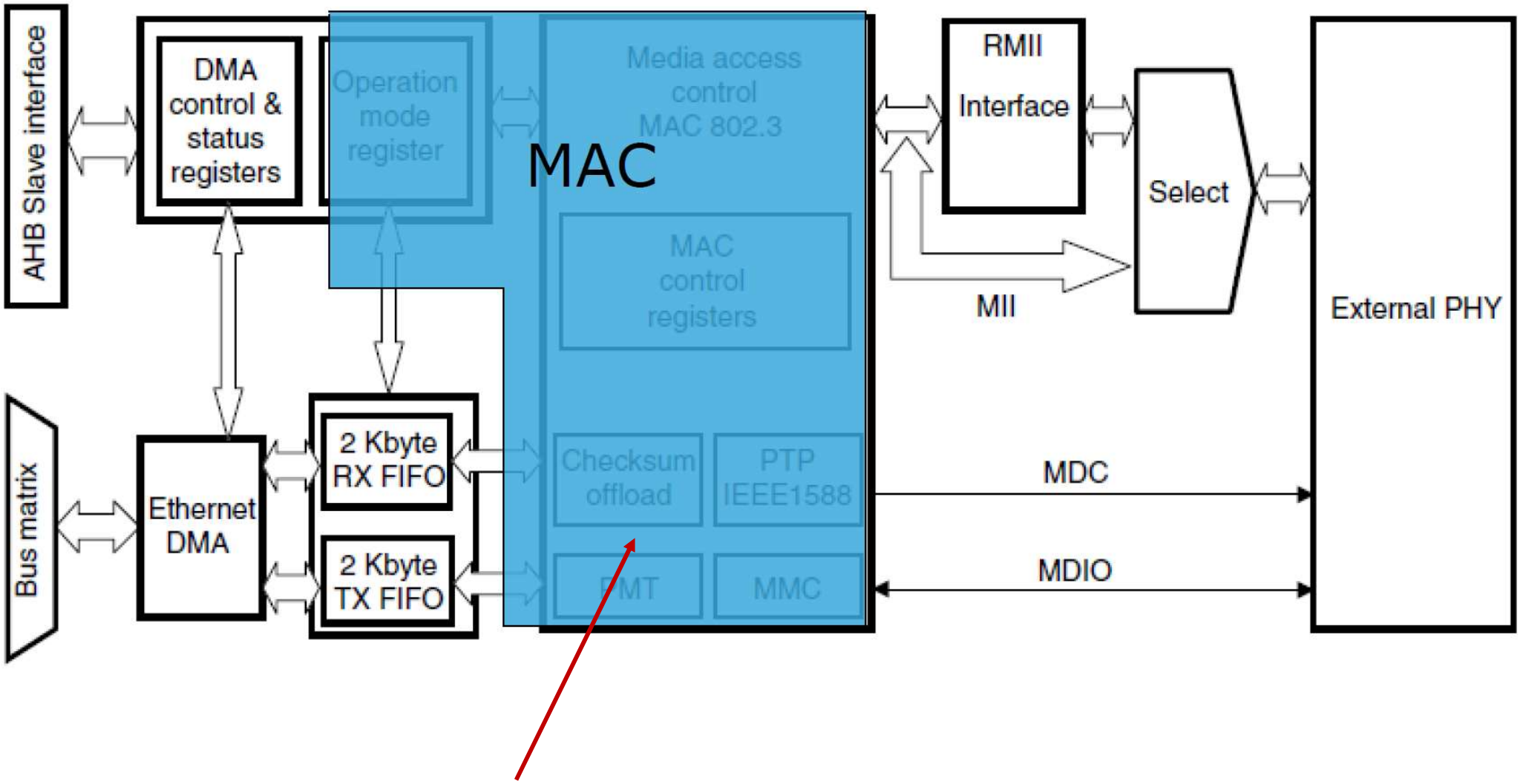
- In file "**stm32f7xx_hal_conf.h**"

```
/* The DP83848 PHY status register */
#define PHY_SR ((uint16_t)0x10)   /* PHY status register Offset */
#define PHY_SPEED_STATUS ((uint16_t)0x0002)   /* PHY Speed mask */
#define PHY_DUPLEX_STATUS ((uint16_t)0x0004)  /* PHY Duplex mask */
```

stm32f7xx_hal_conf.h (old) for LAN8742A Check new implementation: **lan8742.h**

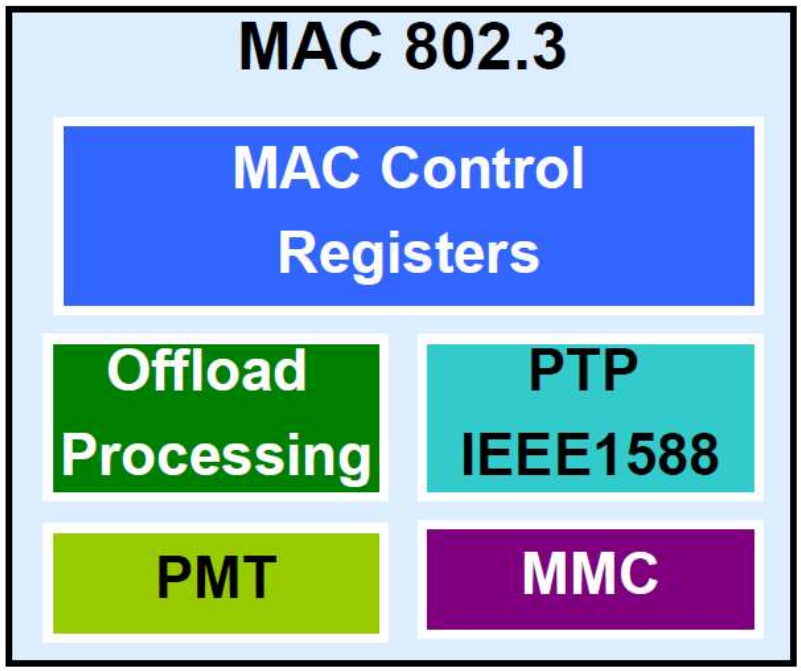
```
/* Section 4: Extended PHY Registers */
#define PHY_SR  ((uint16_t)0x1FU)    /*!< PHY status register Offset  */

#define PHY_SPEED_STATUS  ((uint16_t)0x0004U)  /*!< PHY Speed mask   */
#define PHY_DUPLEX_STATUS ((uint16_t)0x0010U)  /*!< PHY Duplex mask  */

#define PHY_ISFR ((uint16_t)0x001DU) /*!< PHY Interrupt Source Flag register
Offset */
#define PHY_ISFR_INT4  ((uint16_t)0x000BU)  /*!< PHY Link down interrupt */
```

Media Access Control (MAC)



PTP: Precision Timing Protocol
PMT: Power Management
MMC: MAC Management Counters

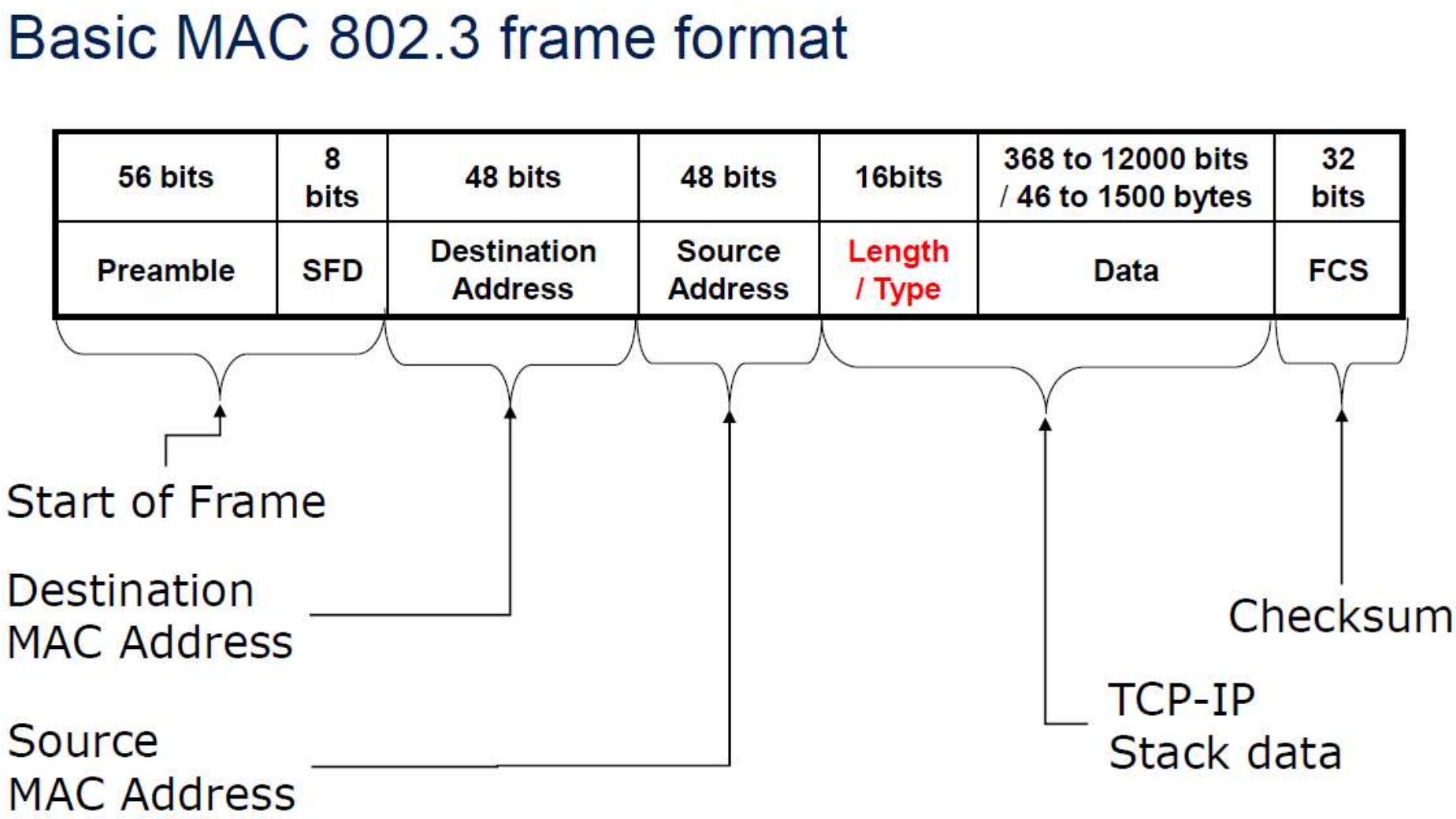
Media Access Control (MAC)



- Operation modes and PHY support
  - 10/100Mbps data rate
  - Full-duplex and half-duplex operations
  - MII and RMII interface to external PHY
- Offload processing
  - Start-of-frame (preamble and SFD) data insertion or deletion
  - Checksum checking of IPv4 header and TCP, UDP, or ICMP payload
  - Calculates and inserts IPv4 header and TCP, UDP, or ICMP payload checksums
- Low power mode
  - Remote wakeup packet and AMD Magic Packet detection
- Processing control
  - MAC address filtering
  - IEEE 802.3-2002 standard for ETH MAC
  - IEEE 1588-2008/PTPv2 support
  - Supports network statistics with RMON/ MIB counters (RFC 2819 / RFC 2665)

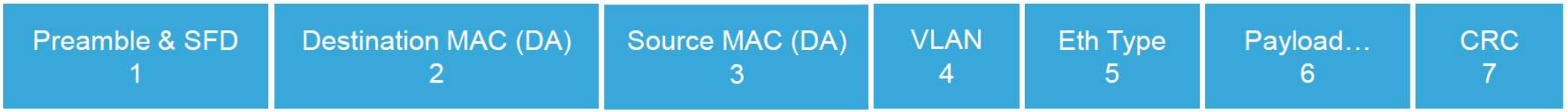
RMON: Remote Monitoring
MIB: Management Information Base
RFC: Request for Comments

Ethernet (MAC 802.3) Frame Format



Source: STMicroelectronics Training Notes

Offload Features: Ethernet Datagram Management Overview

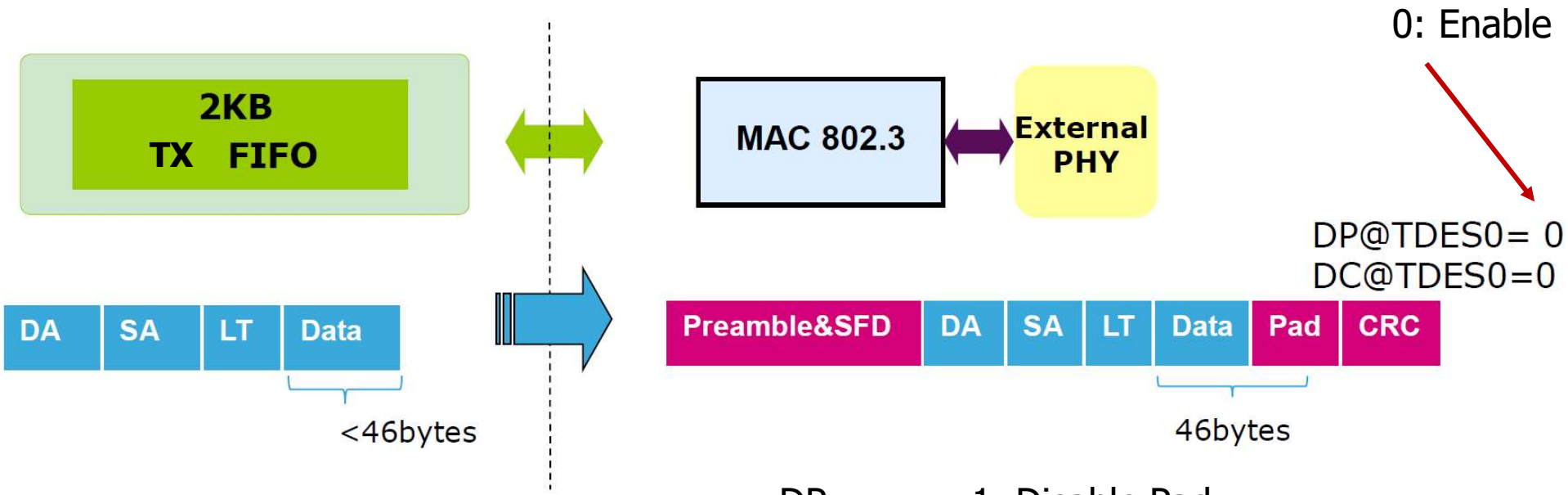


- Ethernet datagram offload processing
  1. Preamble & Start Frame Delimiter (SFD) are inserted (Tx) or deleted (Rx) automatically
  2. Destination MAC address filtering (select only the relevant frames for your application)
  3. Source MAC address filtering
  4. VLAN tag detection of received frame
  5. Checks frame length and type (Rx) or Insert field (Tx)
  6. Ethernet payload Checksum computation and insertion (Tx) or checking (Rx) for:
     - IPv4 header
     - TCP/UDP/ICMP payload
  7. Datagram CRC computation (Tx) and checking (Rx) for the whole datagram without taking into account the start-of-frame (preamble and SFD) tag

Note that most of the non-payload parts of the datagram are efficiently managed in hardware.

Automatic CRC and Pad Generation

- When the number of bytes received from the application falls below 60 [DA (6) + SA (6) + LT (2) + Data (min. 46)], zeros are appended to the transmitting frame to make the data length exactly 46 bytes to meet the minimum data field requirement of IEEE 802.3.

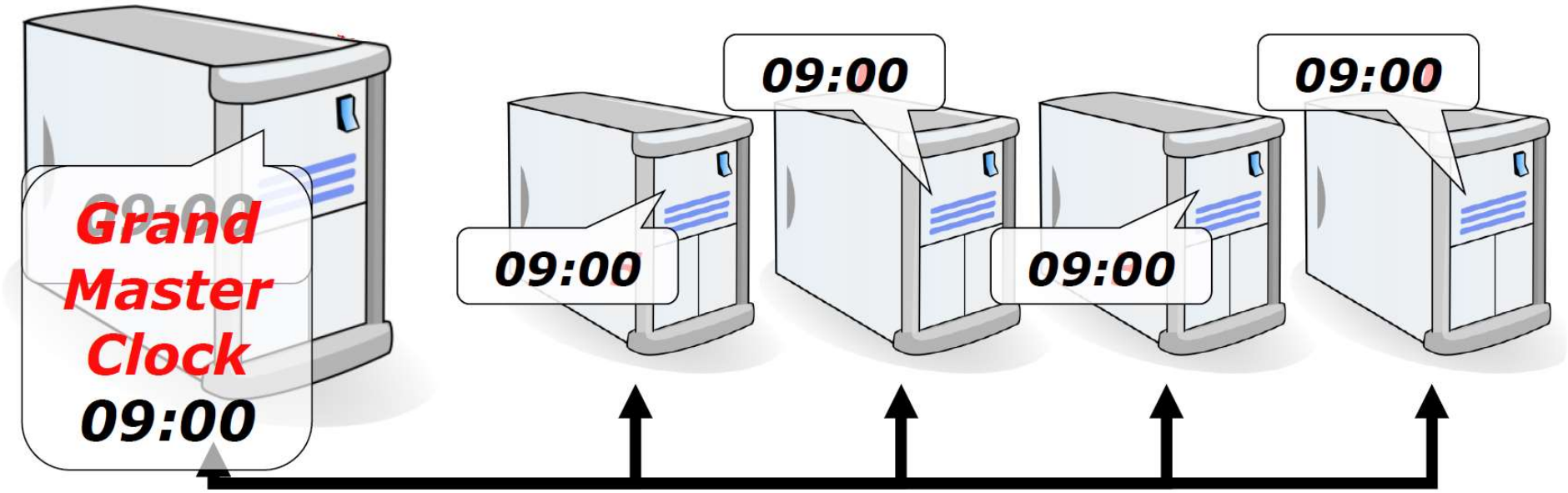


DP: = 1, Disable Pad
DC: = 1, Disable CRC
TDES0: Transmit Descriptor Word0

Note: The TDES0 can be under Normal Transmit (TX) DMA Descriptor or Enhanced Transmit (TX) DMA Descriptor if time stamping is activated.

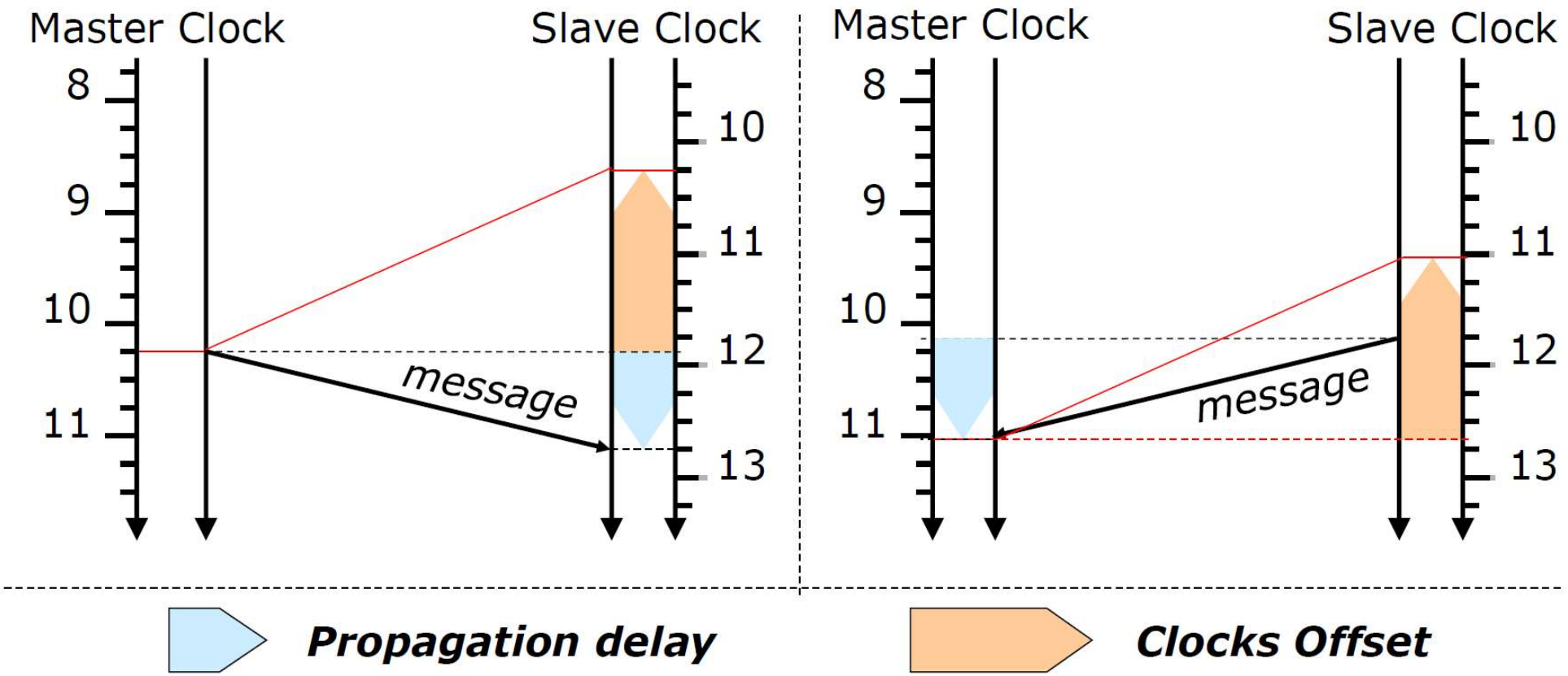
Precision Time Protocol (IEEE 1588)

- It is a protocol designed to synchronize real-time clocks of the devices in a network.
- The synchronization is done with the most accurate clock found in a packet-based network, and it is called the **Grand Master Clock**.



Precision Time Protocol (IEEE 1588)

- Examine the transmission of messages
  - From the master clock point of view
  - From the slave clock point of view



Precision Time Protocol (IEEE 1588)

The computation is done by the slave

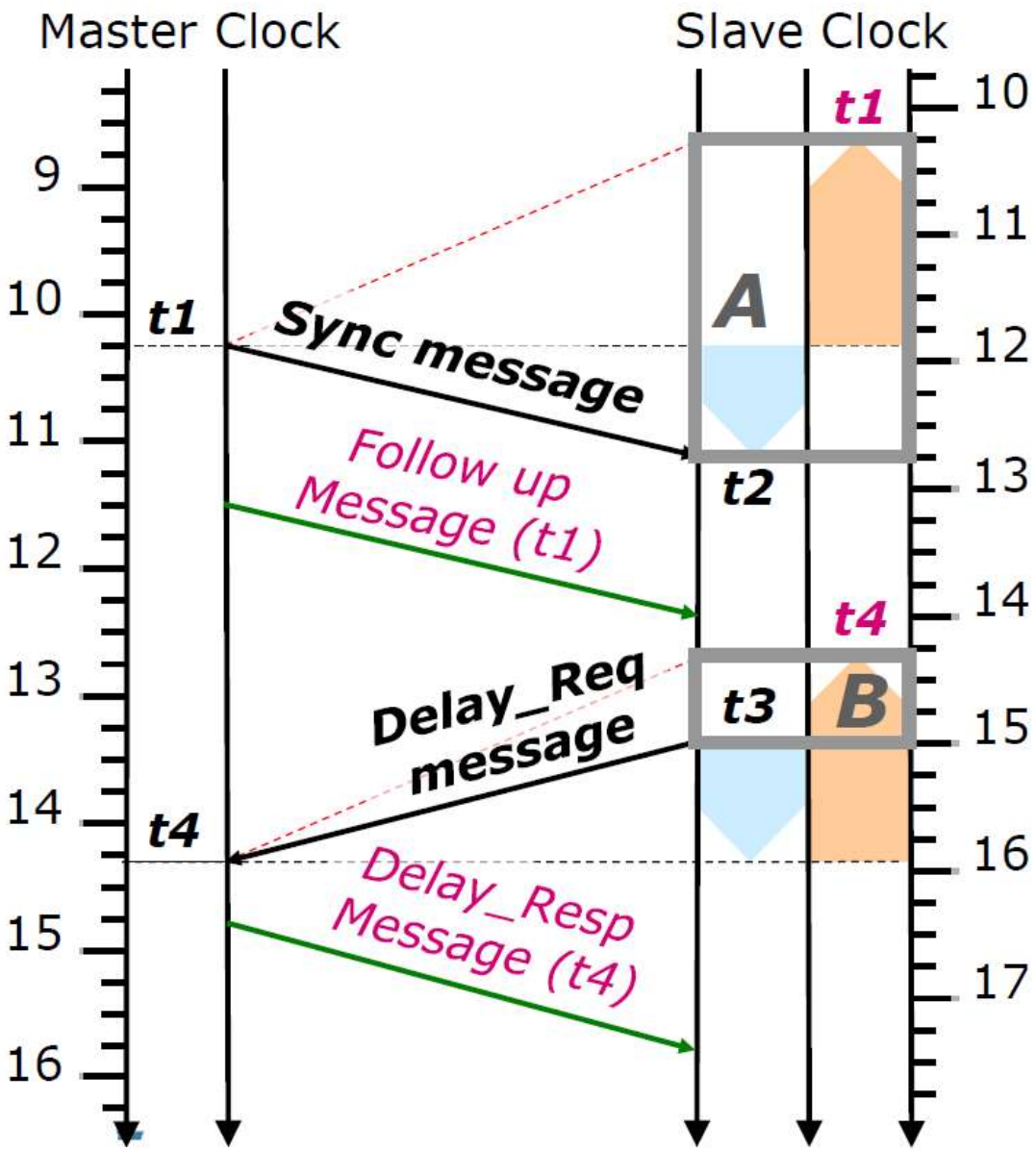
A = t2 – t1 = Offset + Delay

B = t3 – t4 = Offset – Delay

Delay = (A – B) / 2

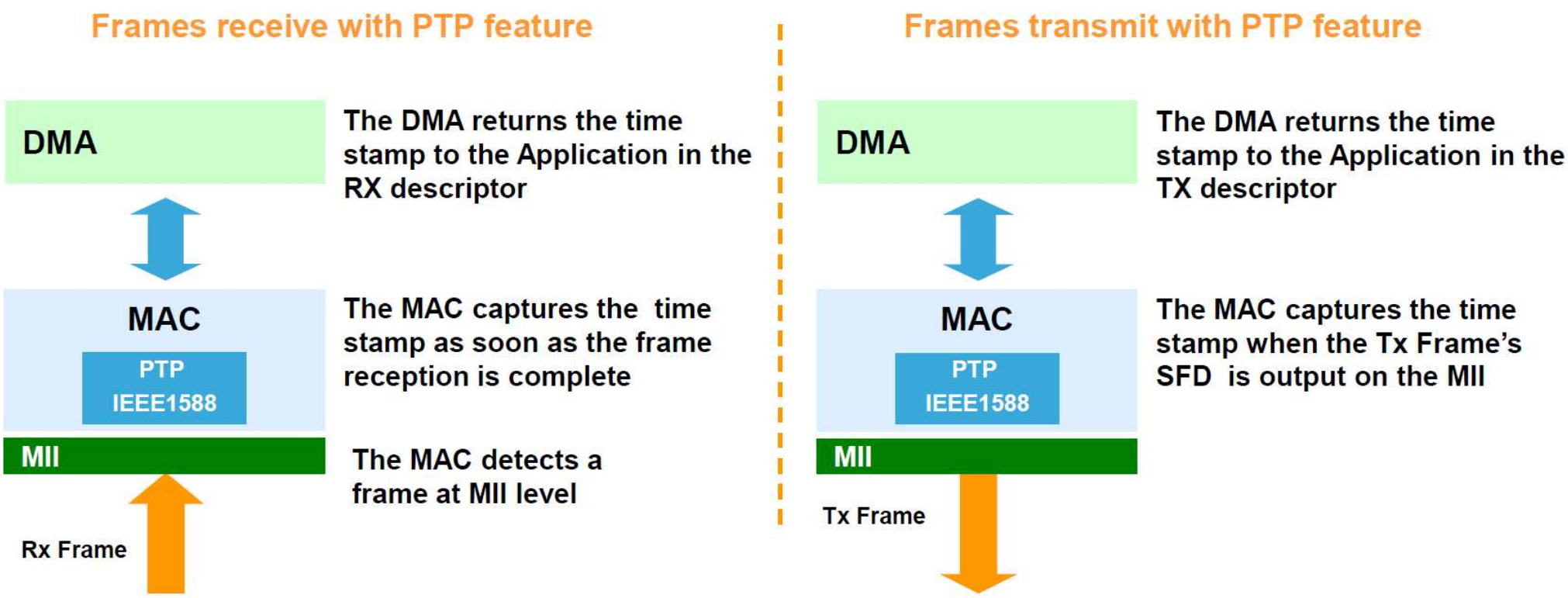
Offset = (A + B) / 2

This allows the time synchronization of master and slave with a sub-µ second precision.



Precision Time Protocol (IEEE 1588) – Time Stamping

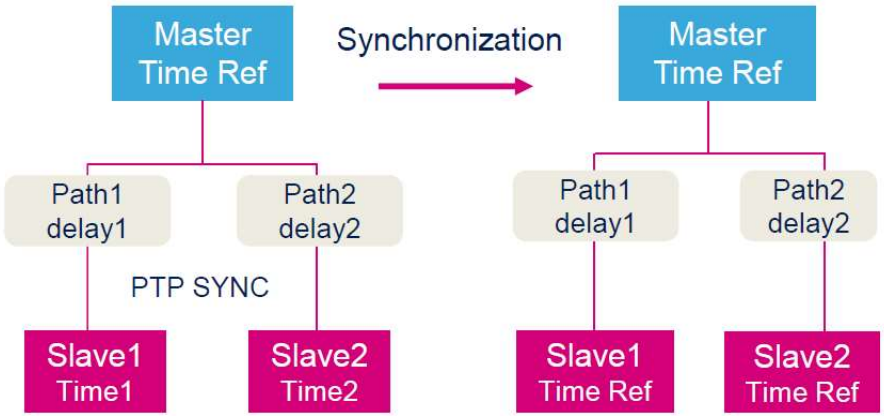
- Time stamp is captured by hardware
  - Frames receive: As soon as the reception is complete
  - Frames transmit: When the SFD of start-of-frame is output on the MII



Precision Time Protocol (IEEE 1588)

- Precision Time Protocol (PTP) Objective
  - Synchronize all nodes in a local network area (LAN) with very high accuracy (<1us) by use of HW time stamping
  - PTP protocol defines synchronization messages between nodes and routers.

- STM32F7 MAC features
  - MAC is compliant with PTPv2 (IEEE 1588-2008) messages
  - Accurate timing reference is based on hardware counter
    - 64 internal bits (32 bits for second and 32 bits for nanosecond counter)
    - Counter accuracy on HCLK is down to ~ 5 ns (@ 200MHz)
    - Export timing reference through output pulse-per-second (PPS) signal



Low-Power Modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop	The Ethernet peripheral is able to detect frames while the system is in the Stop mode, provided that the EXTI line 19 is enabled.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

Power Management – Remote Wake-up Frame Detection

- Power down stop mode state
  - Ethernet DMA and transmit state machine are switched-off
  - PHY, MII interface and MAC Rx remain active
- Wake-up
  - Wake-up is controlled by the network
  - Wake-up packets are
    - AMD Magic packet
    - User defined
  - Wake-up frame detection is an event that can wake-up the system from stop mode