Review Questions: Periodic Mode

Timer – Part 1

Periodic Mode

1. How many 16/32-bit Timers are there in the Tiva TM4C123G microcontroller?
   - Total of 6 16/32-bit Timers. They are labelled as Timer 0A & 0B to Timer 5A & 5B.
   - Note that each set of Timers A and B can operate as independent Timers.
   - However they can also be concatenated to be one wider Timer. E.g. Two 16-bit Timers can be concatenated to be a single 32-bit Timer.
   - When concatenated, Timer A registers are used to control the 32-bit Timer.
2. Which bit and register should be set to program a Timer to count DOWN?
   - Assuming Timer A, we set Timer A Mode register (TAMR), bit TACDIR to 0. TACDIR = Timer A Count Direction.
3. Timer 0 has TWO outputs: T0CCP0 and T0CCP1. Why are there two outputs?
   - There are two outputs, one for Timer A and the other for Timer B. Output name ending with '0' denotes Timer A while a '1' denotes Timer B.
   - Both Timers can functions as independent 16-bit Timers.

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4. Which register and bit(s) do we use to enable/disable a Timer?
   - To disable Timer A, we reset (put to '0') TAEN bit of the GPTMCTL register.
5. Why do we disable a Timer during initialization?
   - We disable a Timer during initialization to prevent unexpected Timer behavior due to changes in any of the registers.
6. Can a Pre-scalar be used in 32-bit mode for a 16/32-bit GPTM module?
   - No. Pre-scaler is not used.
   - Pre-scalers are not used when Timers are concatenated.
7. Which register is used to enable the clock to a GPTM timer module?
   - RCGCTIMER register.
   - RCGC1 register can also be used but not preferred. This is a legacy register.
8. Which register and bit(s) do we use to check that the Timer 5 is ready to be accessed?
   - PRTIMER register, bit 5 (R5).

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9. Which register and bit(s) is used to set a GPTM to be in Periodic mode?
   - Set Mode register (GPTM*n*MR), T*n*MR bit to 0x02 to set Timer to Periodic mode.
10. Which register and bit(s) sets the GPTM to count DOWN?
   - Set Mode register (GPTMT*n*MR), T*n*DIR bit to 0.
11. For a 16-bit count-DOWN Timer clocked at a bus speed of 40 MHz with a 8-bit pre-scalar, what is the maximum interval between timer interrupts? Show your working.
   - With 8-bit pre-scalar, clock is divided by 256.
   - 40 MHz/256 = 156.25 KHz.
   - Maximum interval = 2^{16} x 1/156.25 KHz = 419.43 ms.
12. The GPTM Timer modules run at system clock frequency.
   - TRUE.

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13. Describe how Timer 0A operates as a DOWN counter in Periodic mode.
    - Timer counter begins counting from the value loaded in GPTMTAILR (Interval Load Register).
    - It counts DOWN till counter value reaches 0 (Time-Out event).
    - When 0 is reached, Timer counter is reloaded with value in GPTMTAILR register & GPTMTAPR (Prescalar) register at the next clock cycle.
    - Upon Time-Out event, TATORIS (Time-Out Raw Interrupt Status) flag in GPTMRIS register is set. TATOMIS bit is set if interrupt is enabled.
        - MIS/RIS & IMR status cleared by writing '1' to the GPTMICR register.
    - Counting starts again at the next clock cycle.

14. Describe how a Timer Match interrupt can be generated.
    - Match interrupt is generated when Timer value equals the value loaded to the GPTMTnMATCHR (Timer Match) & GPTMTnPMR (Prescale Match) registers.
    - Interrupt status bits are updated through the RIS & MIS registers.

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15. Write the C codes to enable T4CCP0 pin on Timer 4. Consider the GPIO alternate function and control register settings.

```
#define PC_T4CCP0    0;  /* PC0  */
GPIOC->AFSEL |= BIT (PC_T4CCP0); /* enable alternate fn */
GPIOc->PCTL &= ~GPIO_PCTL_PC0_M; /* PC0 mask   */
GPIOC->PCTL |= GPIO_PCTL_PC0_T4CCP0;
```

16. Write the C code to enable the clock to Timer 4.

```
SYSCTL->RCGCTIMER |= SYSCTL_RCGCTIMER_R4;
```

17. What is the pre-defined name for the interrupt handler for Timer 5?
    - `TIMER5A_Handler` and `TIMER5B_Handler` .

Review Questions

Prescaler:

18. At 25MHz bus clock, if Pre-scalar (**TAPR**) = 0x7F and a Preload (**TAILR**) value of 0x33AA (16 bits), what is the time interval that the counter increments?
    - At 25 MHz, period = 1/25 MHz = 40 ns
    - When Timer is counting UP, the pre-scaler acts as a time extension => it becomes the MSB bits.
    - Thus counter load value = 0x7F33AA (24 bits) = 8,336,298
    - Time interval = (8,336,298 + 1) × 40 ns = 0.333 s.

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19. A GPTM is programed to operate in 16-bit, Periodic, count DOWN mode. It is required that a time-out interrupt occur at every 7ms. What are the values we should program to the **TAPR** and **TAILR** registers? Assume 80 MHz bus clock. Show your working.

- At 80MHz bus clock, period = 12.5 ns.
- With a 16-bit count DOWN Timer,
  - maximum count = 2^{16}
  - maximum interval = $2^{16} \times 12.5$ ns = 0.8192 ms.
- Since 7 ms > 0.8192 ms, we need to make use of a pre-scaler.

$$\frac{7ms}{0.8192ms} = 8.54 \longrightarrow$$

Choose a pre-scaler division = 9.
Thus, **TAPR** = 9 – 1 = 8

$$\frac{7ms}{12.5ns \times 9} = 62{,}222$$
$$= 0xF30E \longrightarrow$$

Reload Value (**TAILR**) = 0xF30E – 1 = 0xF30D